

8		7		6	
BOM Variants					
BOM NUMBER	BOM NAME			BOM OPTIONS	
685-0054	COMMON, MLB-4GB, J44			J44_COMMON	
685-0053	DPV, MLB-4GB, J44			XDP_CONN	
639-4878	PCBA, MLB-4GB, 2.4G, 4GB-HYNIX, J44			BASE_BOM, CPU_HSW:2.4G, RAM_4G_HYNIX_H, CAMDRAM:HYNIX_H	
639-4879	PCBA, MLB-4GB, 2.4G, 4GB-ELPIDA, J44			BASE_BOM, CPU_HSW:2.4G, RAM_4G_ELPIDA, CAMDRAM:ELPIDA	
639-4880	PCBA, MLB-4GB, 2.4G, 4GB-MICRON, J44			BASE_BOM, CPU_HSW:2.4G, RAM_4G_MICRON, CAMDRAM:MICRON	
639-5272	PCBA, MLB-4GB, 2.6G, 4GB-HYNIX, J44			BASE_BOM, CPU_HSW:2.6G, RAM_4G_HYNIX_H, CAMDRAM:HYNIX_H	
639-5273	PCBA, MLB-4GB, 2.6G, 4GB-ELPIDA, J44			BASE_BOM, CPU_HSW:2.6G, RAM_4G_ELPIDA, CAMDRAM:ELPIDA	
639-5274	PCBA, MLB-4GB, 2.6G, 4GB-MICRON, J44			BASE_BOM, CPU_HSW:2.6G, RAM_4G_MICRON, CAMDRAM:MICRON	
639-5275	PCBA, MLB-4GB, 2.8G, 4GB-HYNIX, J44			BASE_BOM, CPU_HSW:2.8G, RAM_4G_HYNIX_H, CAMDRAM:HYNIX_H	
639-5276	PCBA, MLB-4GB, 2.8G, 4GB-ELPIDA, J44			BASE_BOM, CPU_HSW:2.8G, RAM_4G_ELPIDA, CAMDRAM:ELPIDA	
639-5277	PCBA, MLB-4GB, 2.8G, 4GB-MICRON, J44			BASE_BOM, CPU_HSW:2.8G, RAM_4G_MICRON, CAMDRAM:MICRON	
685-0074	VCORE, FET, VSHV, J44			VCORE_FET:VSHV	
685-0075	VCORE, FET, REN, J44			VCORE_FET:REN	

DEVELOPMENT/BASE BOM					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0054	1	J44 MLB COMMON BOM	BASE	CRITICAL	BASE_BOM
985-0053	1	J44 MLB DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SUB-BOMS					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0074	1	VCORE,FET,VSHY,J44	VCOREFETS	CRITICAL	VCORE_FETS

Alternate Parts				
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
685-0075	685-0074		ALL	RENEVAS ALT TO VISHAY


DRAM PARTS				
333S0704	8	1C, 8DRAM, 40BT, 250M14, 2003-1400, P, D16, 96P80A	CRITICAL	4G ELPIDA
333S0700	8	1C, 8DRAM, 40BT, 250M14, 2003-1400, JHP80A, 96P80A	CRITICAL	4G_HYNTX_H
333S0698	8	1C, 8DRAM, 40BT, 250M14, 2003-1400, R0Y, 8, 96P80A	CRITICAL	4G_MICRON
333S0715	8	1C, 8DRAM, 40BT, 250M14, 2003-1466, P, D16, 96P80A	CRITICAL	4G_ELPIDA 1866
333S0717	8	1C, 8DRAM, 40BT, 250M14, 2003-1466, JHP80A, 96P80A	CRITICAL	4G_HYNTX_H 1866
333S0720	8	1C, 8DRAM, 40BT, 250M14, 2003-1466, R0Y, 8, 96P80A	CRITICAL	4G_MICRON 1866

DRAM SPD Straps		
BOM GROUP	BOM OPTIONS	
RAM_4G_ELPIIDA	4G_ELPIIDA, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:L, PPDDR:1V35	
RAM_4G_HYNIX_H	4G_HYNIX_H, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:H, PPDDR:1V35	
RAM_4G_MICRON	4G_MICRON, RAMCFG3:L, RAMCFG2:L, RAMCFG1:H, RAMCFG0:L, PPDDR:1V35	
RAM_4G_ELPIIDA.1866	4G_ELPIIDA.1866, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:L, PPDDR:1V5	
RAM_4G_HYNIX_H.1866	4G_HYNIX_H.1866, RAMCFG3:L, RAMCFG2:L, RAMCFG1:L, RAMCFG0:H, PPDDR:1V5	
RAM_4G_MICRON.1866	4G_MICRON.1866, RAMCFG3:L, RAMCFG2:L, RAMCFG1:H, RAMCFG0:L, PPDDR:1V5	

13" MBP VARIABLE BOM GROUPS	
BOM GROUP	BOM OPTIONS
J44_COMMON4	SMCBOARDID:8

DRAM SPD Straps	
BOM GROUP	BOM OPTIONS
CAMDRAM:HYNIX_H	CAMDRAM_TYPE:HYNIX_H
CAMDRAM:ELPIDA	CAMDRAM_TYPE:ELPIDA
CAMDRAM:MICRON	CAMDRAM_TYPE:MICRON

DRAM Parts					
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
33380700	1	1C,SDRAM,4GBIT,DOR3L-1600,HBM4, 96B FRGA	U4000	CRITICAL	CAMDRAM_TYPE HYPERX_H
33380704	1	1C,SDRAM,4GBIT,DOR3L-1600,DIE, P 96B FRGA	U4000	CRITICAL	CAMDRAM_TYPE ELPIDA
33380698	1	1C,SDRAM,4GBIT,DOR3L-1600,REV, E, 96B FRGA	U4000	CRITICAL	CAMDRAM_TYPE MICRON

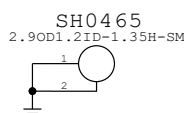
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BOM Configuration			
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DRAWING <BRANCH>		PAGE 3 OF 120	
SHEET 3 OF 78			



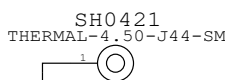
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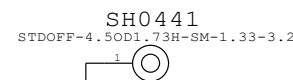
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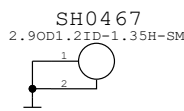
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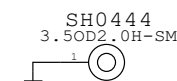
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5.00D2.0H-SM



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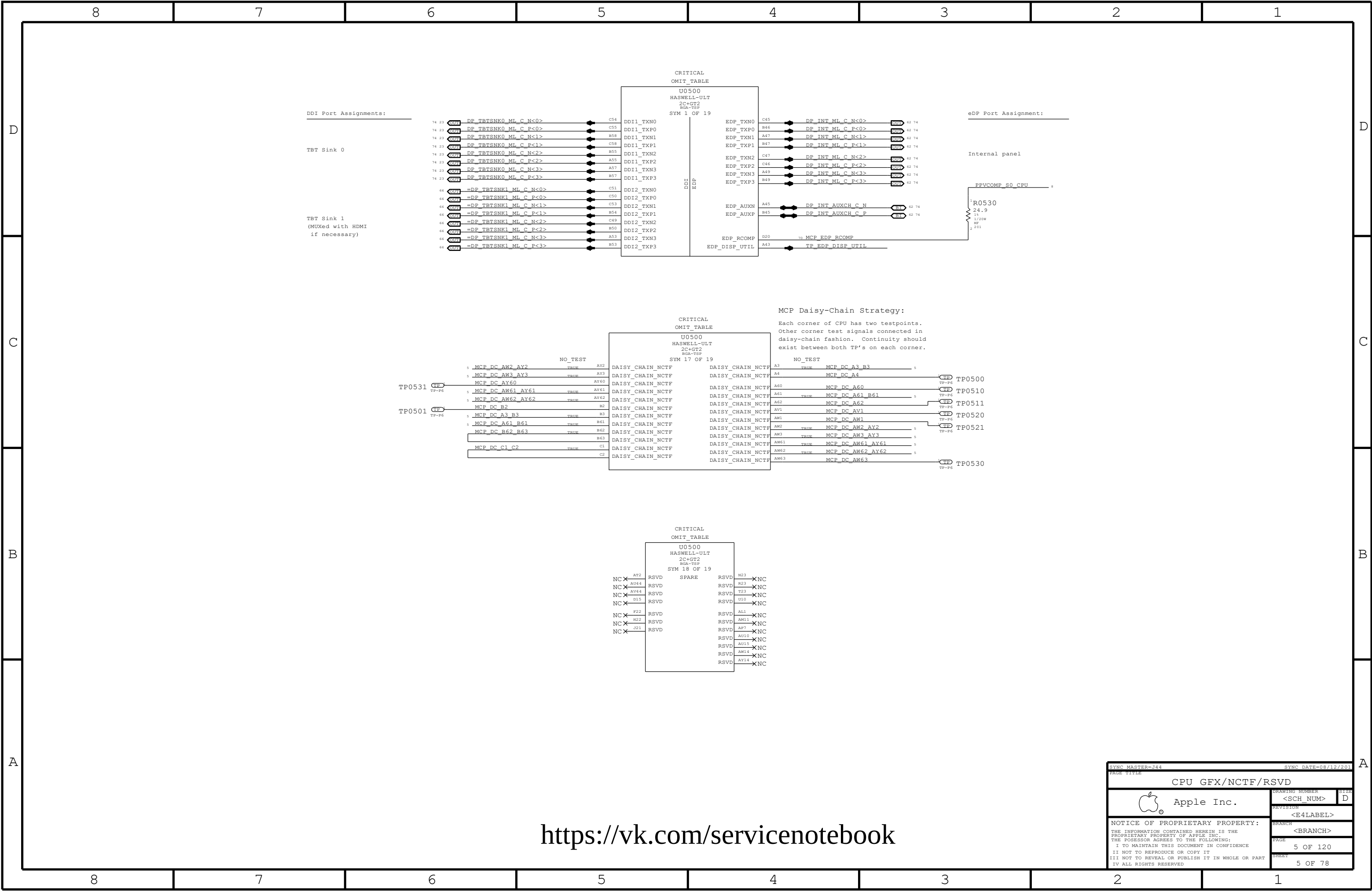


SH0443
3.50D2.0H-SM



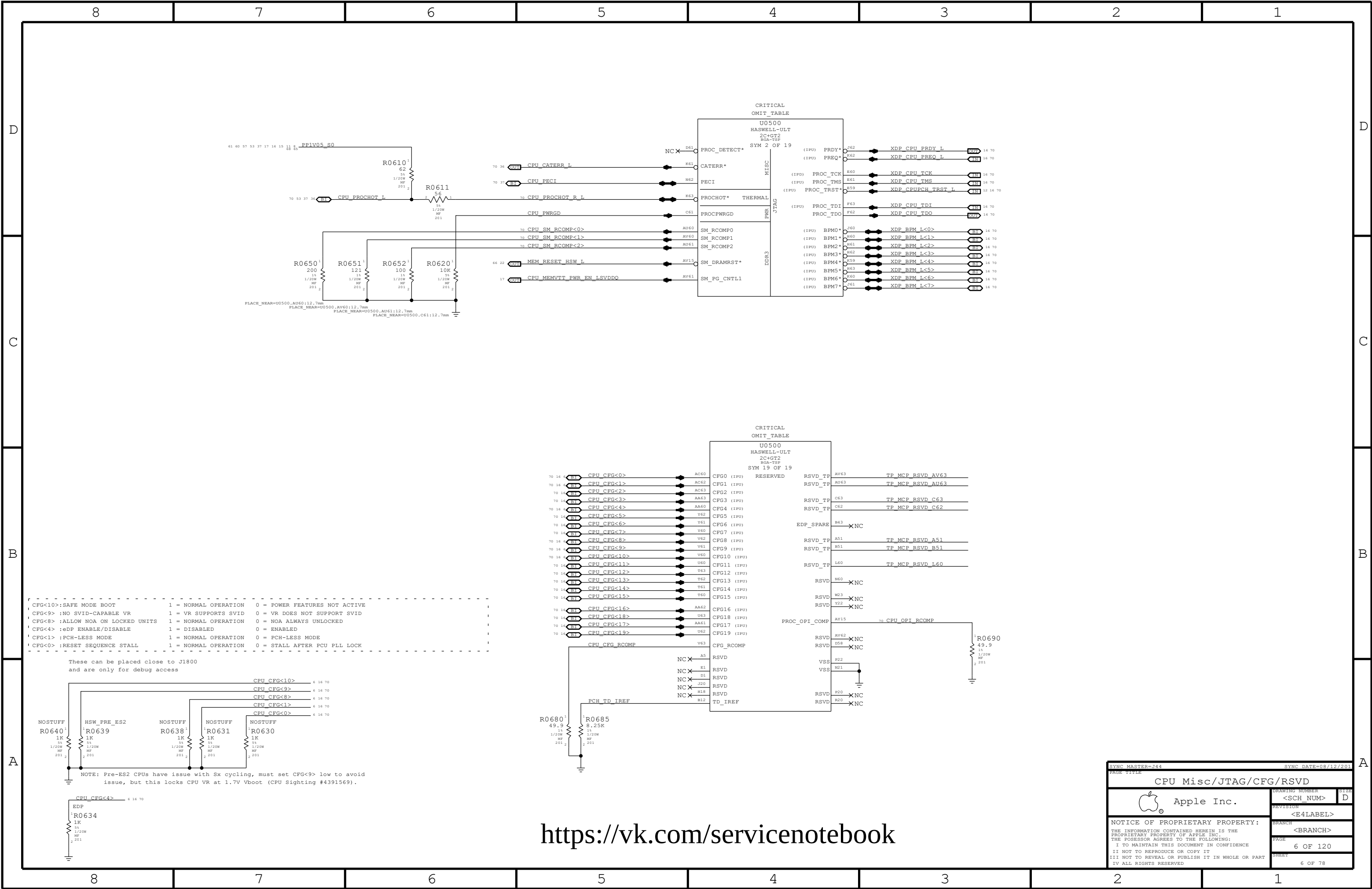
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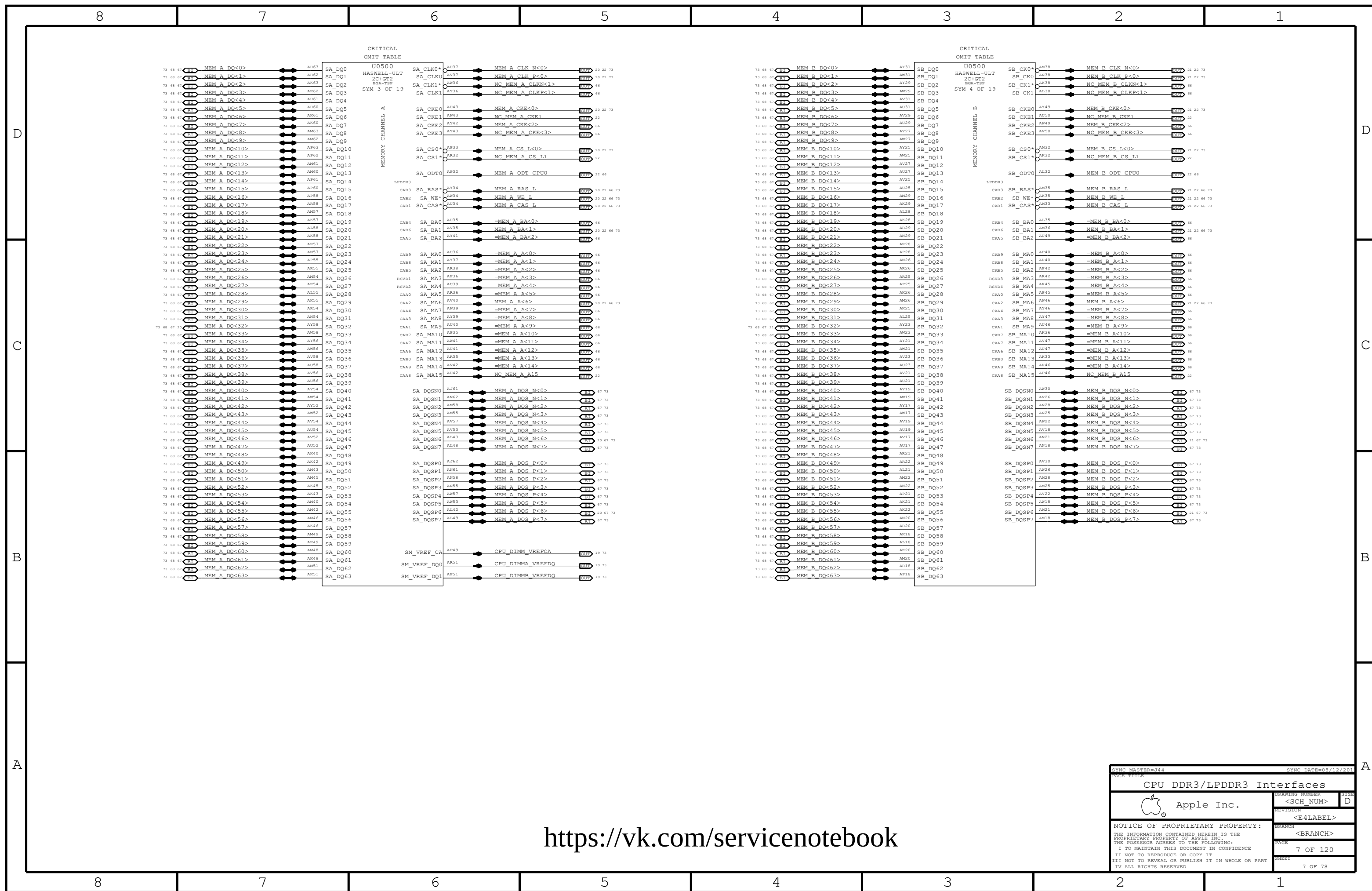


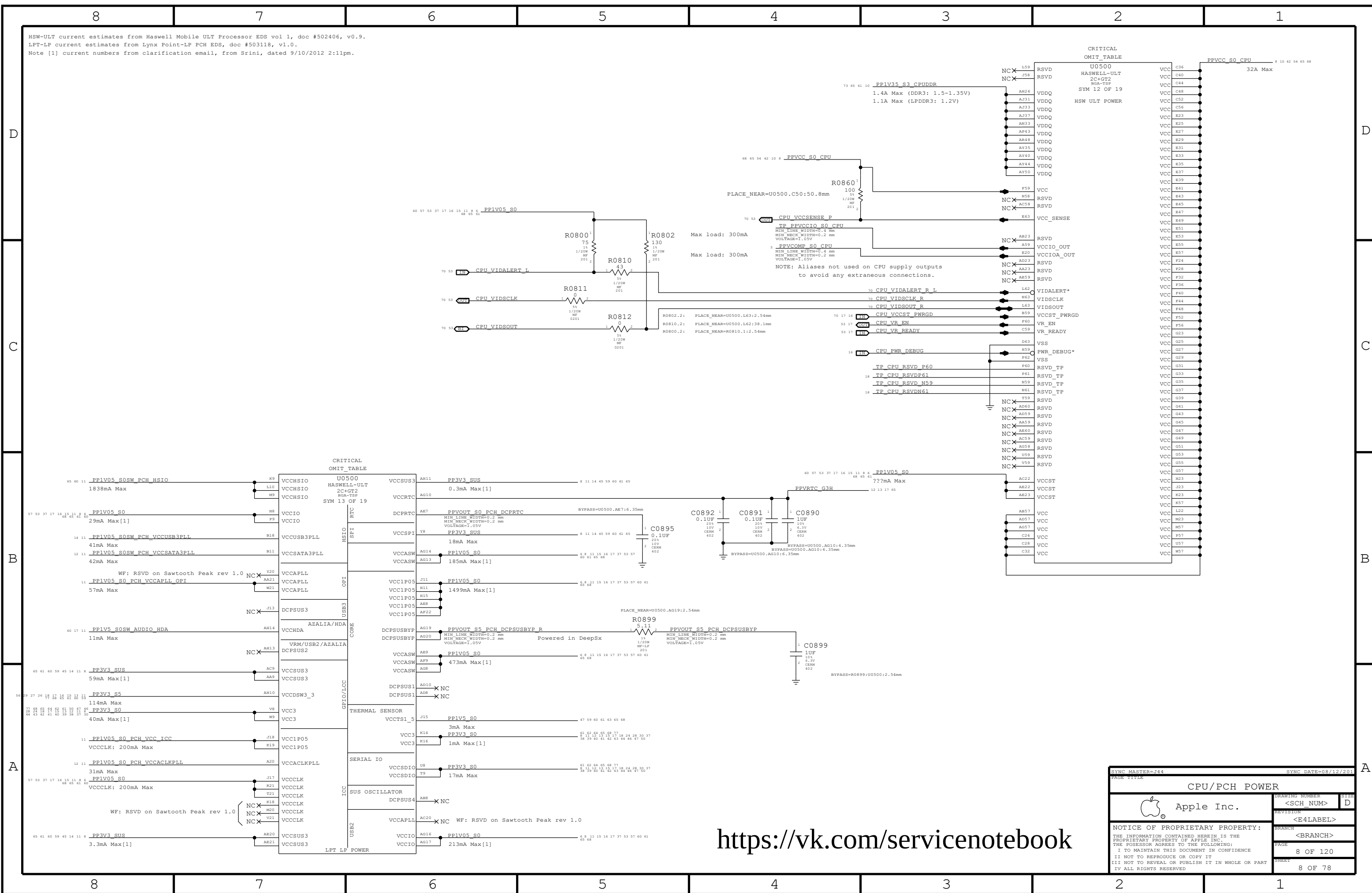
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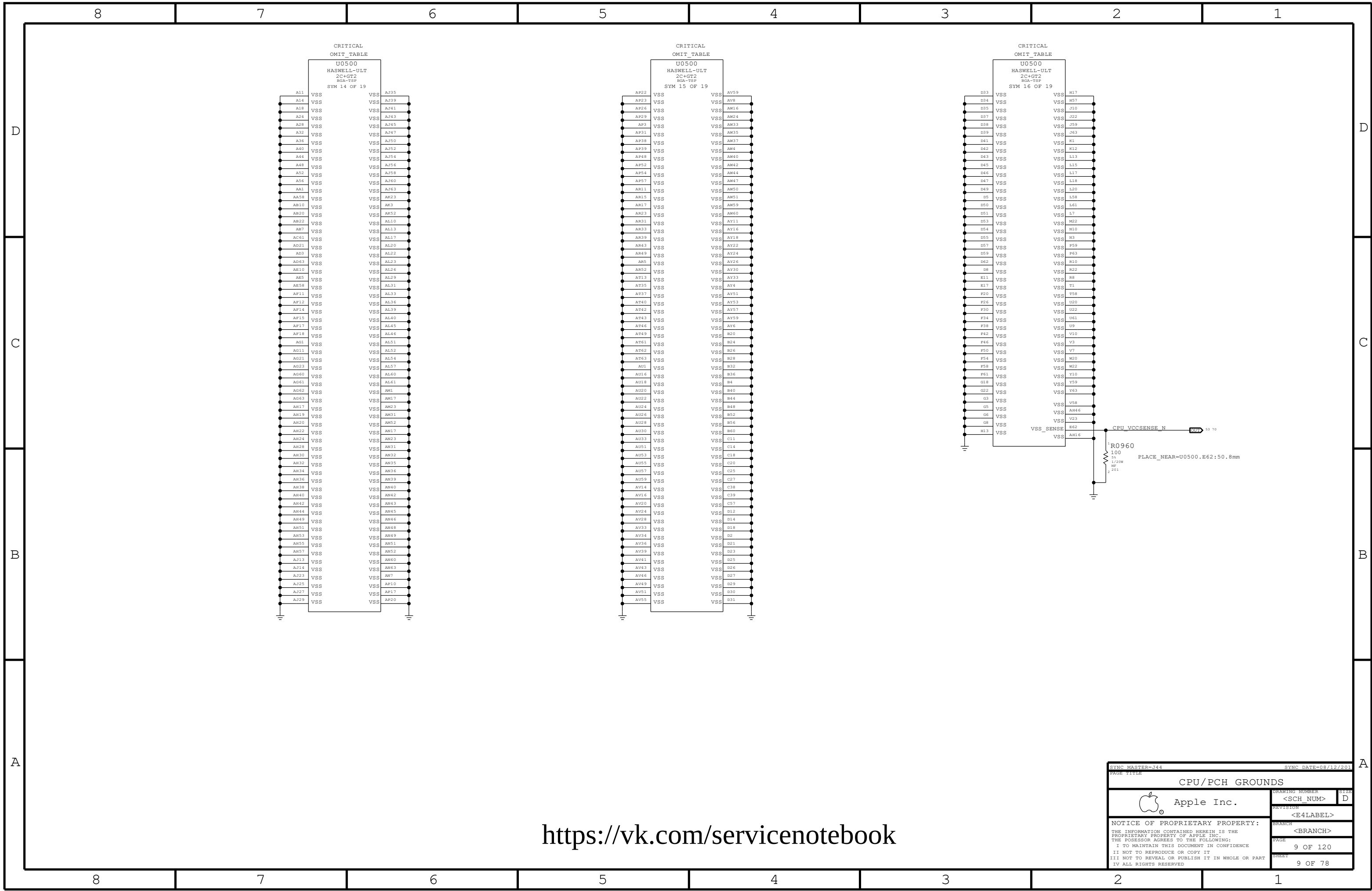
SYNCH MASTER-144		SYNCH DATE-08/12/2013	
PAGE TITLE			
CPU GFX/NCTF/RSVD			
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		DATE	6 OF 78





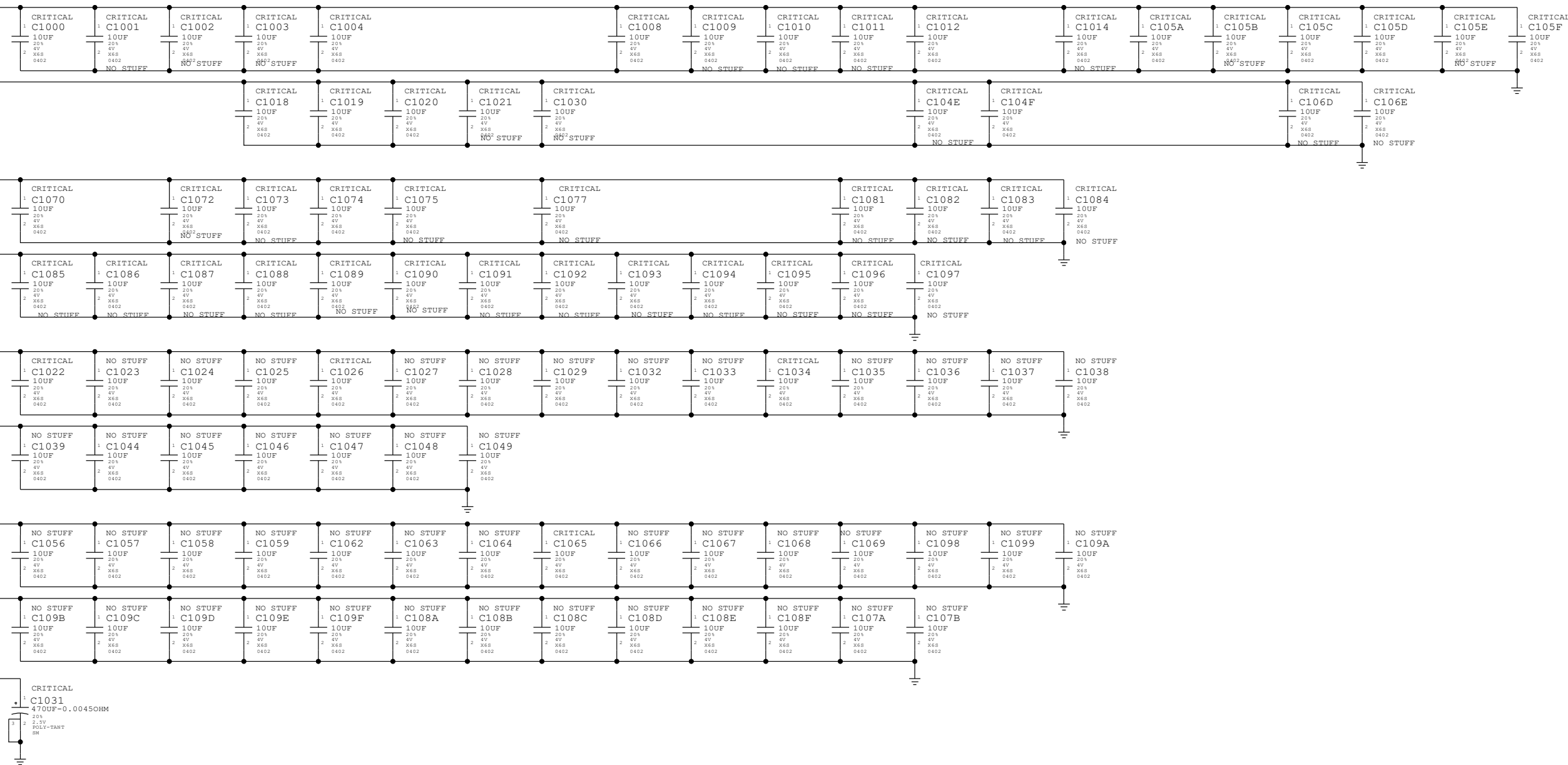


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PAGE		9 OF 78	

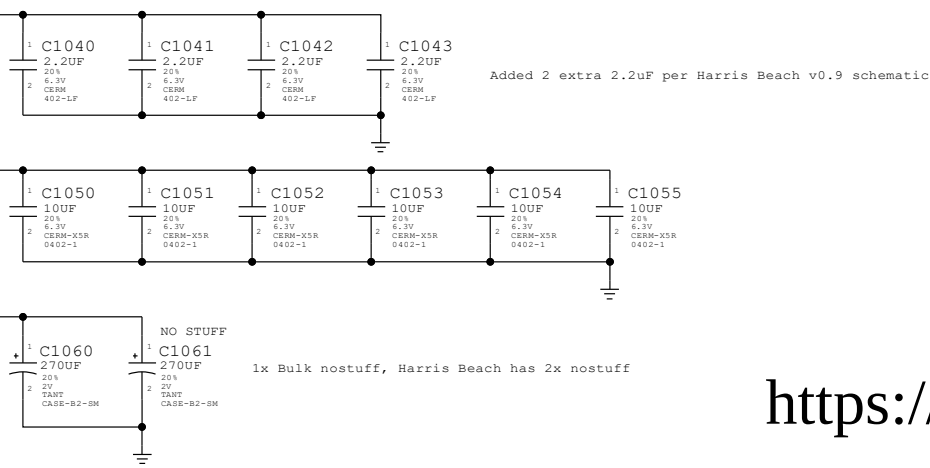
CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 22uF 0603 stuff, 80x 22uF 0603 nostuff



CPU VDDQ DECOUPLING

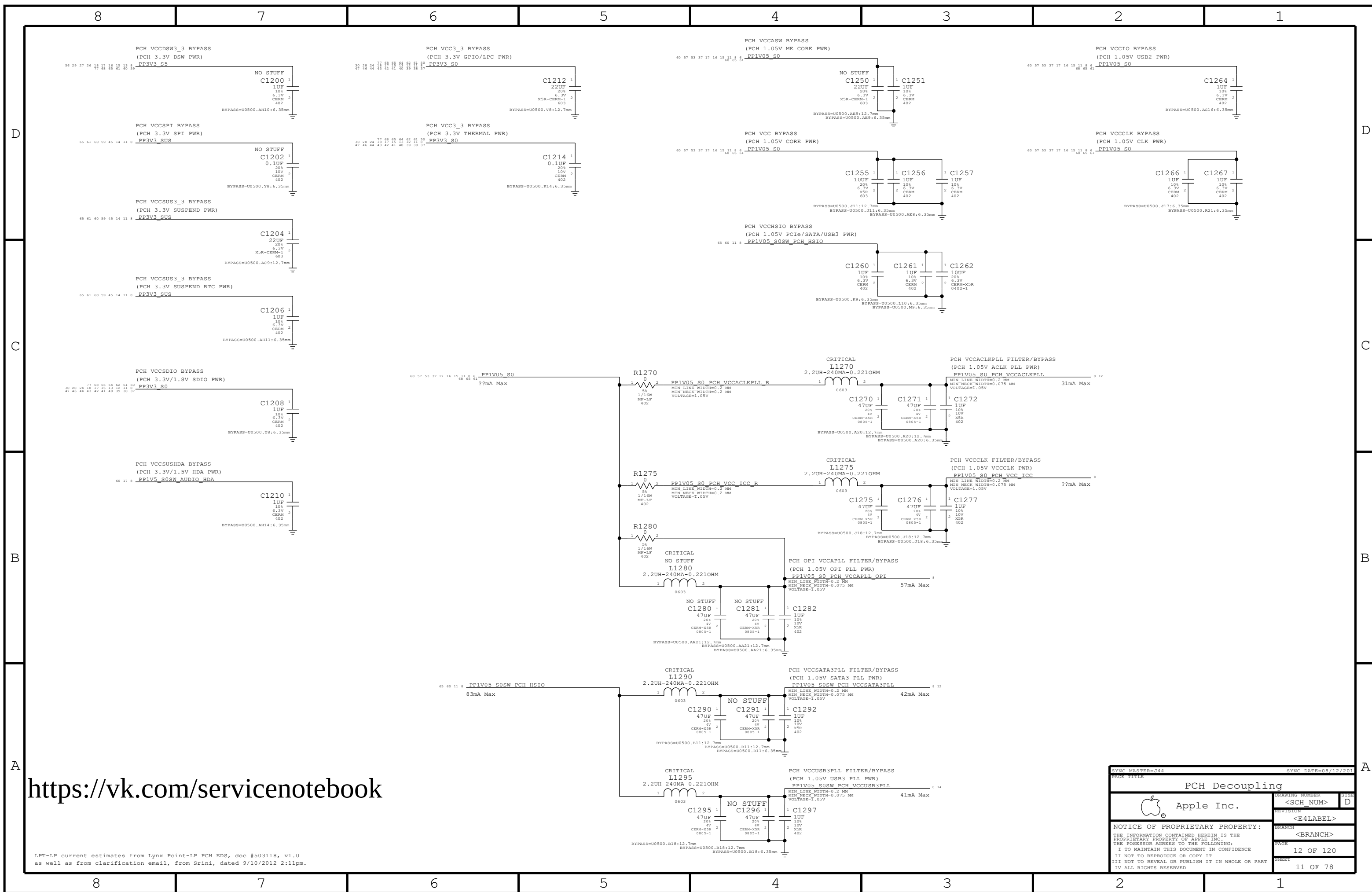
Intel recommendation (Table 5-4): 2x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 2x 2.2uF 0402, 6x 10uF 0402

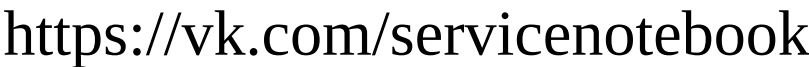


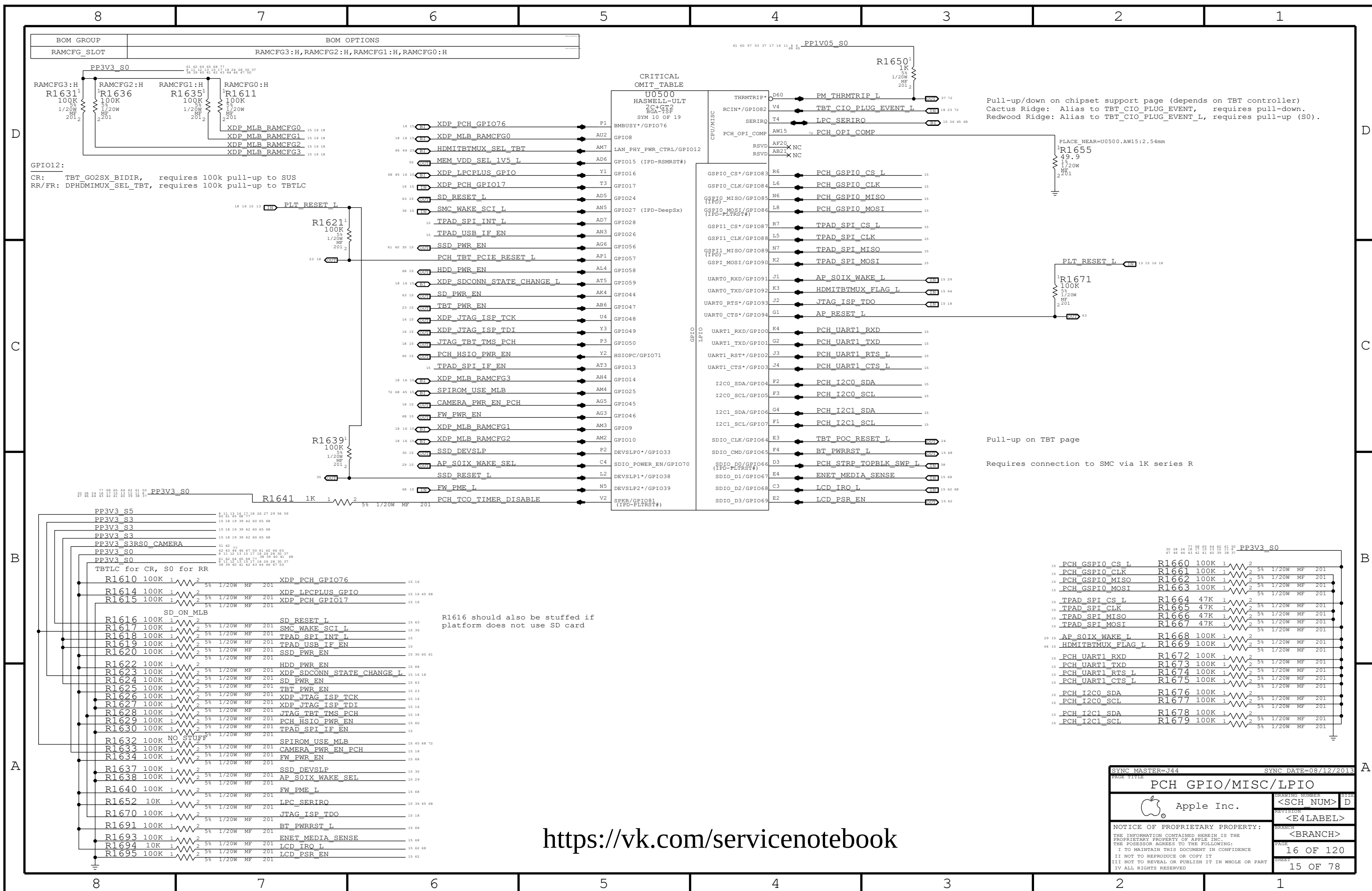
CPU VCC Decoupling

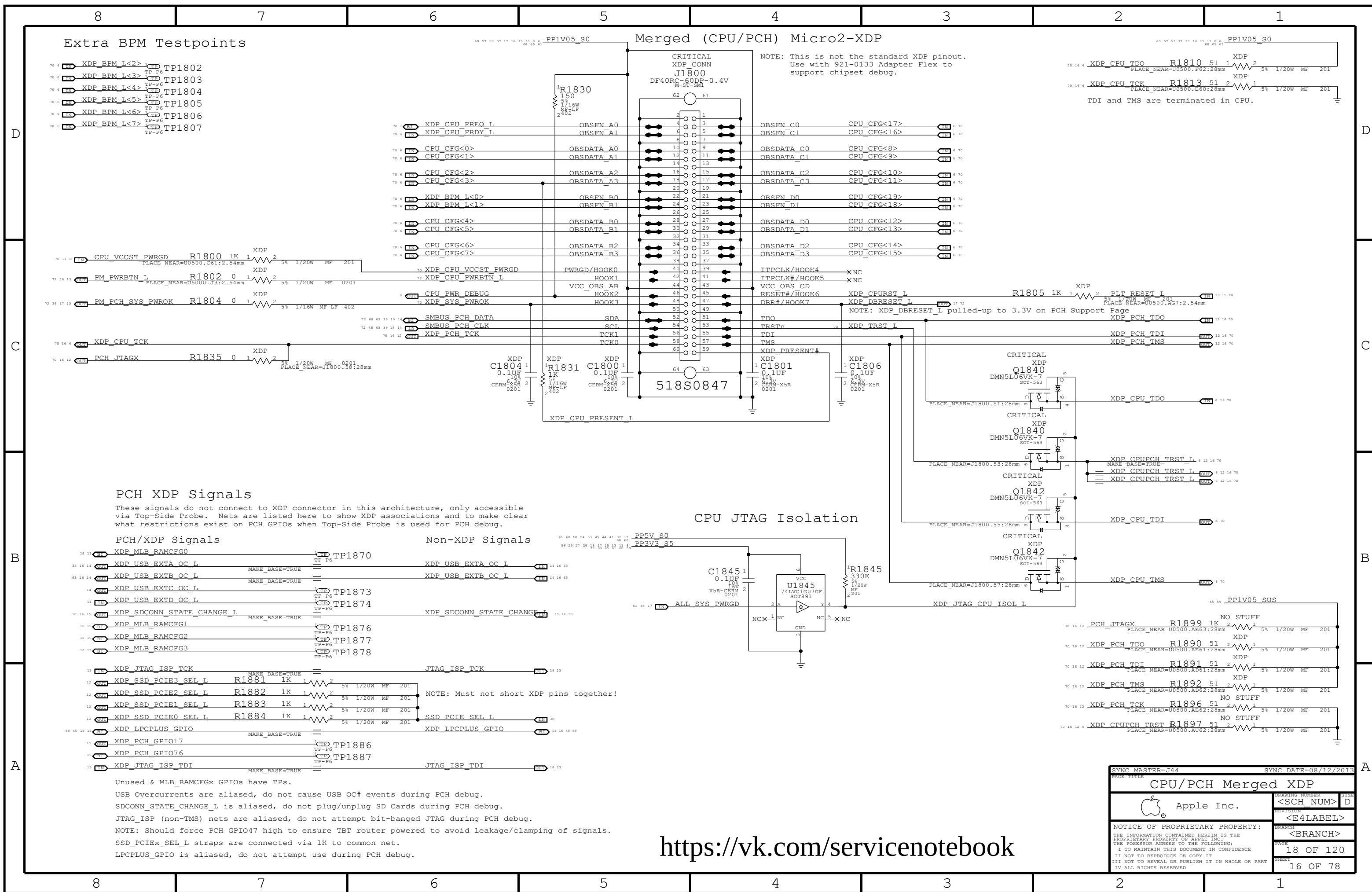
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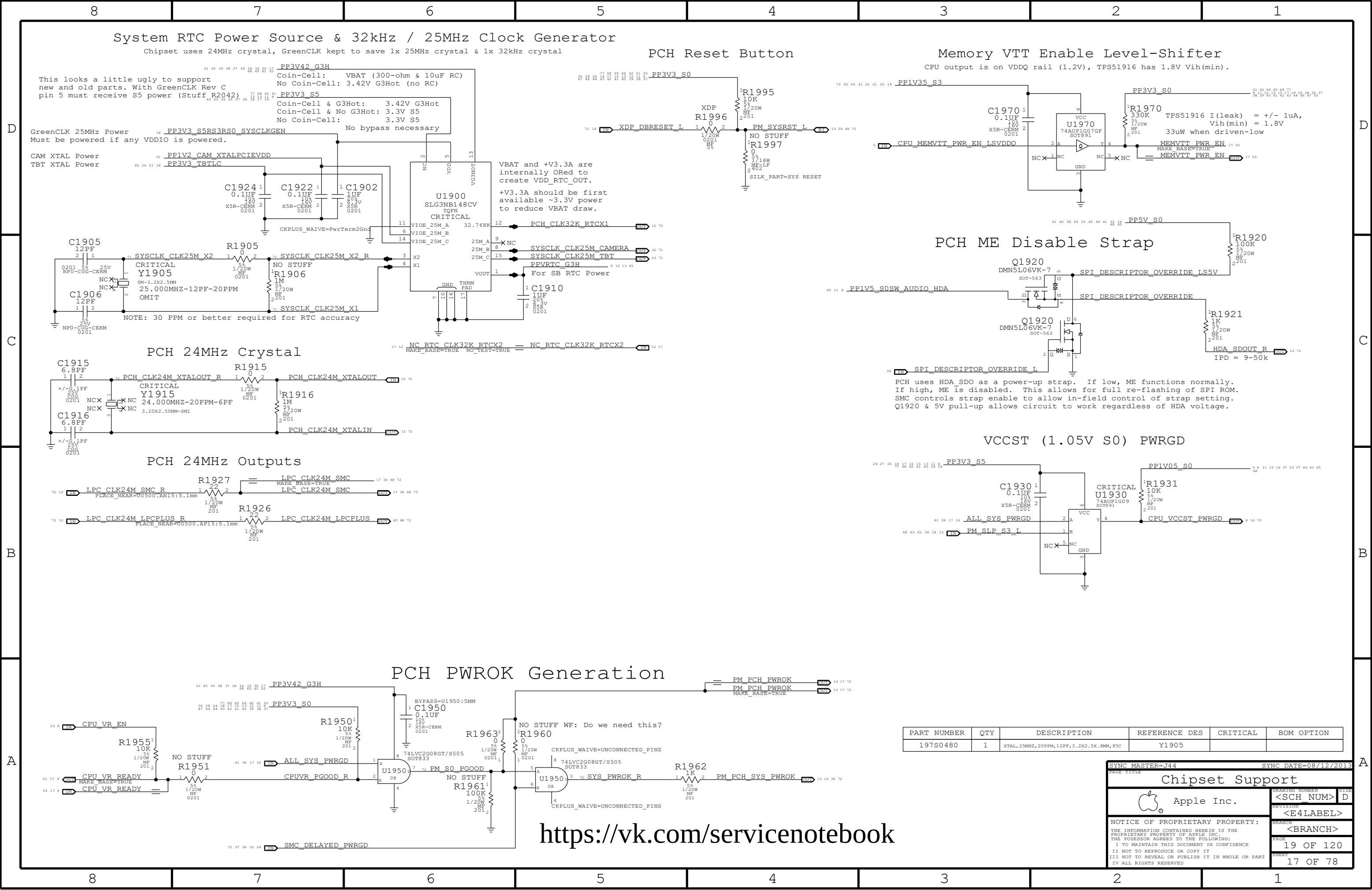
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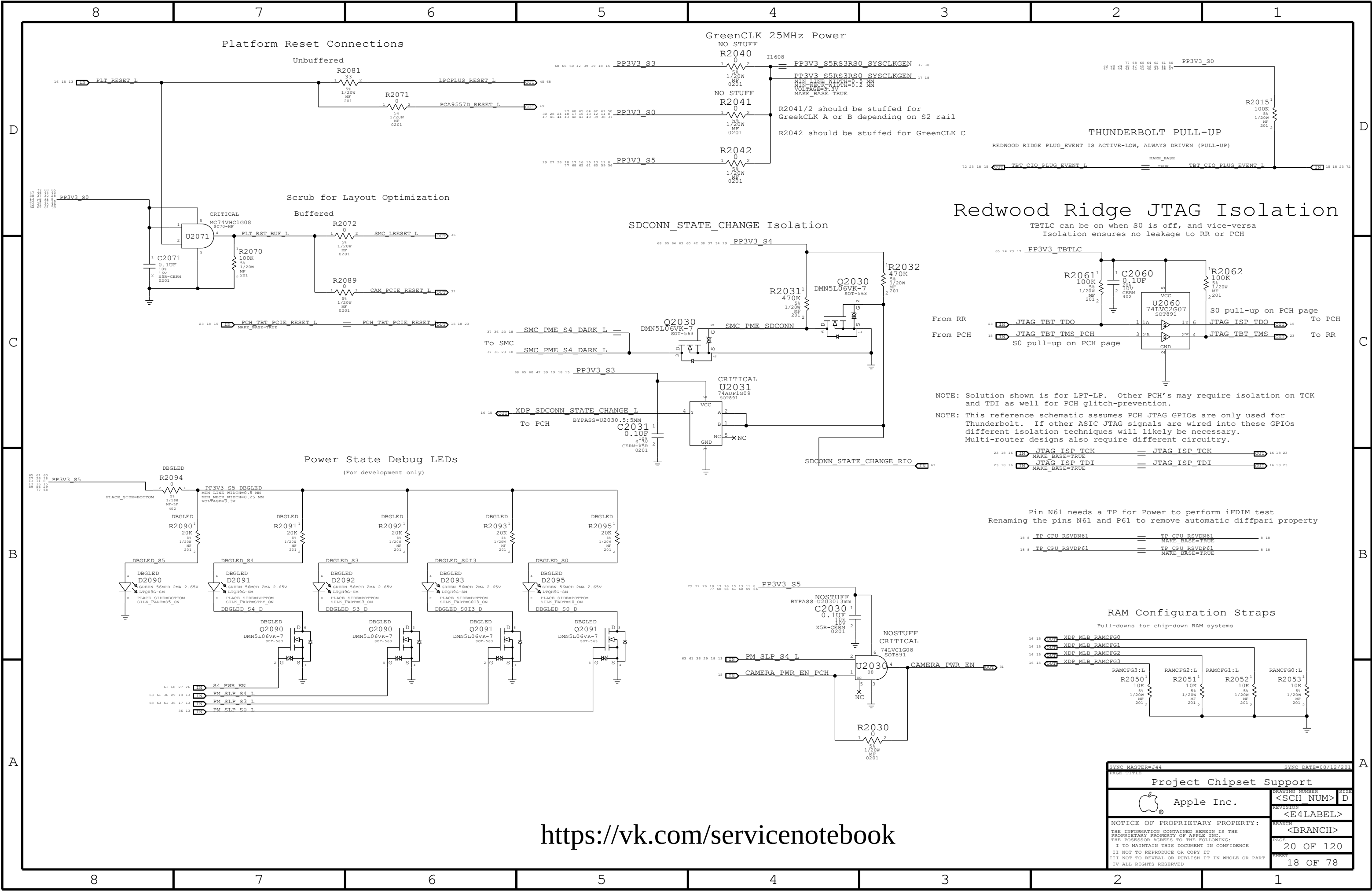







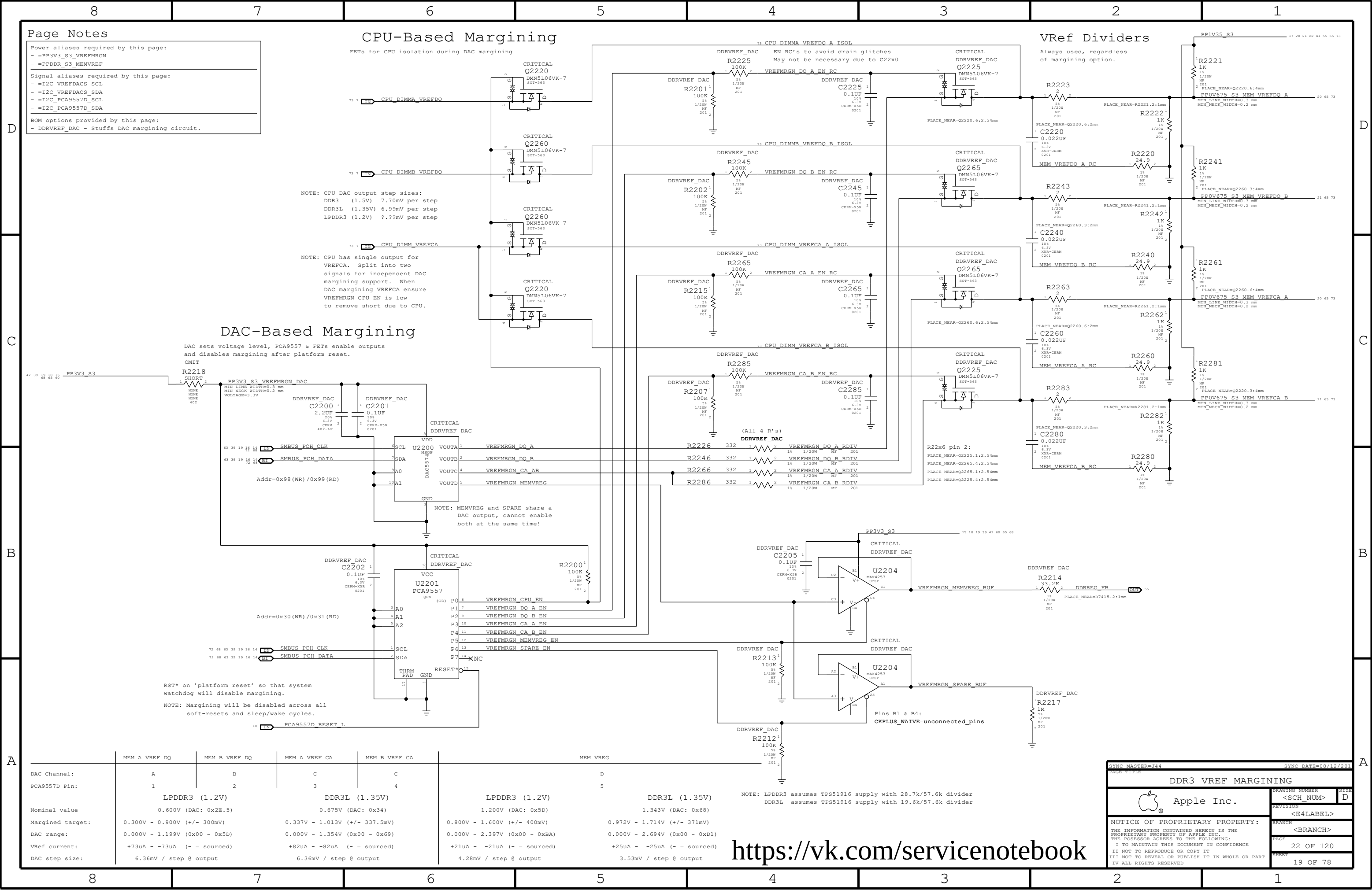


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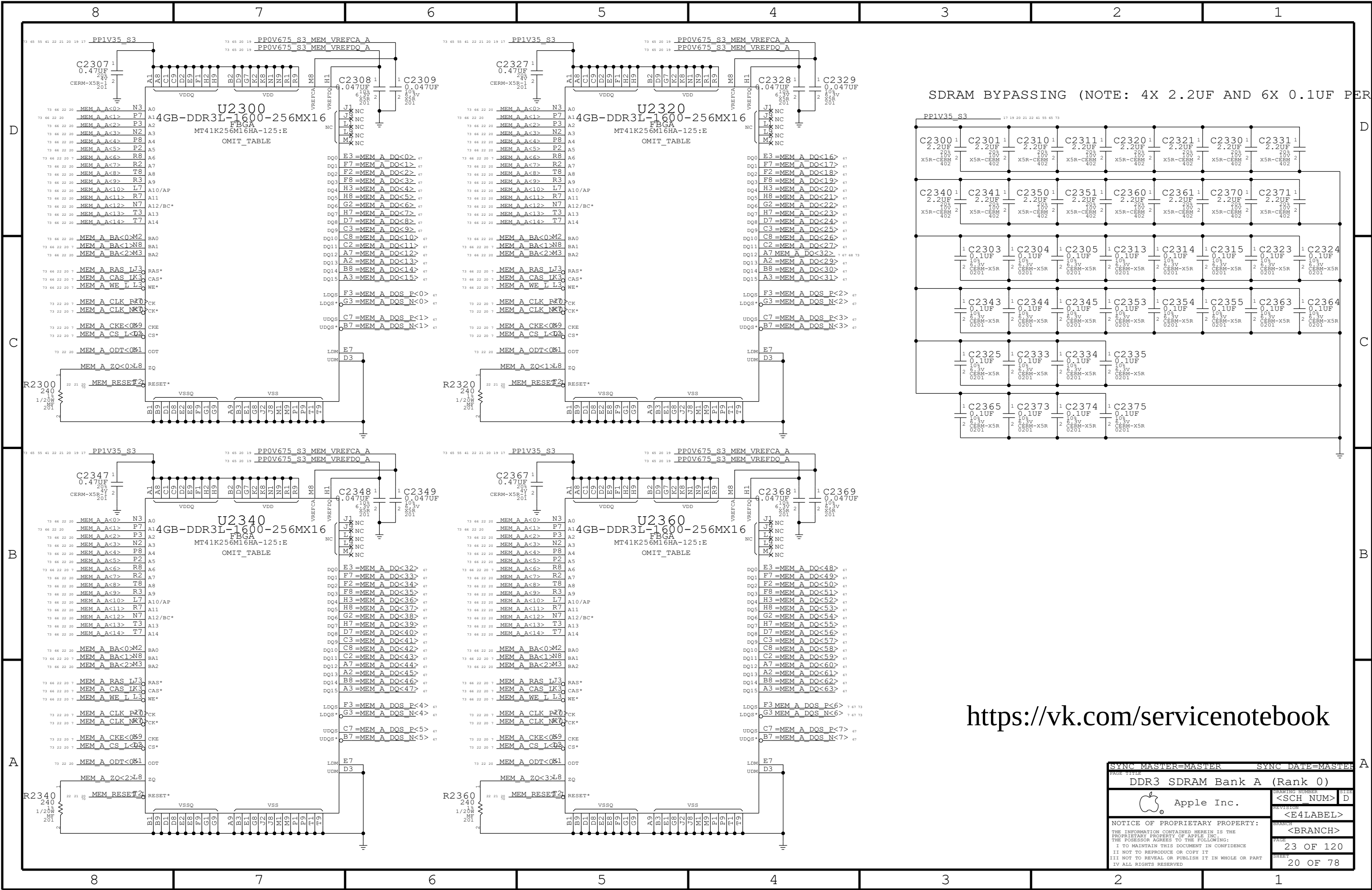


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SYMC MASTER-144		SYMC DATE-08/12/2017	
PAGE TITLE		Project Chipset Support	
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		PAGE	20 OF 120
		FILE	18 OF 78



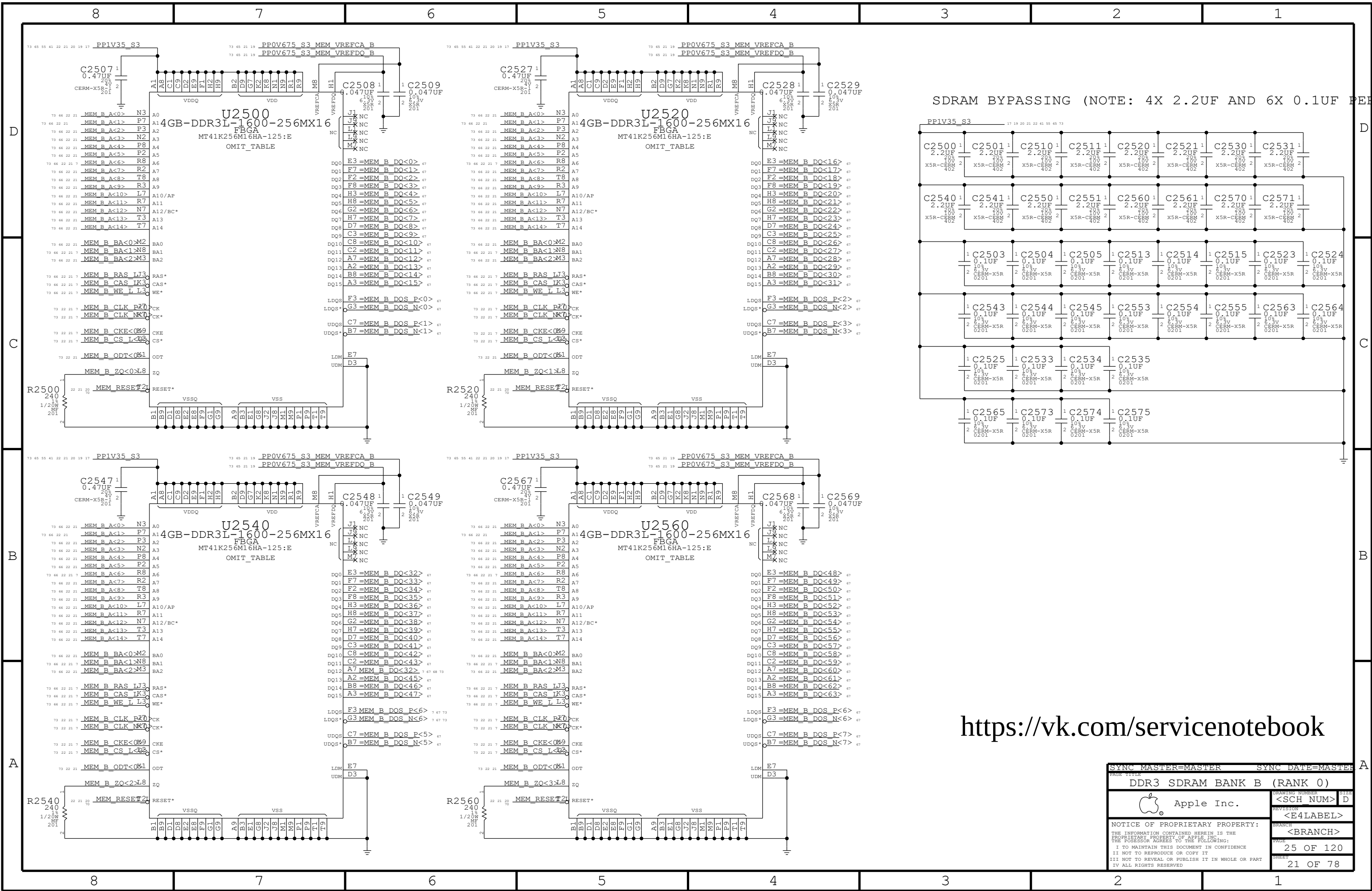
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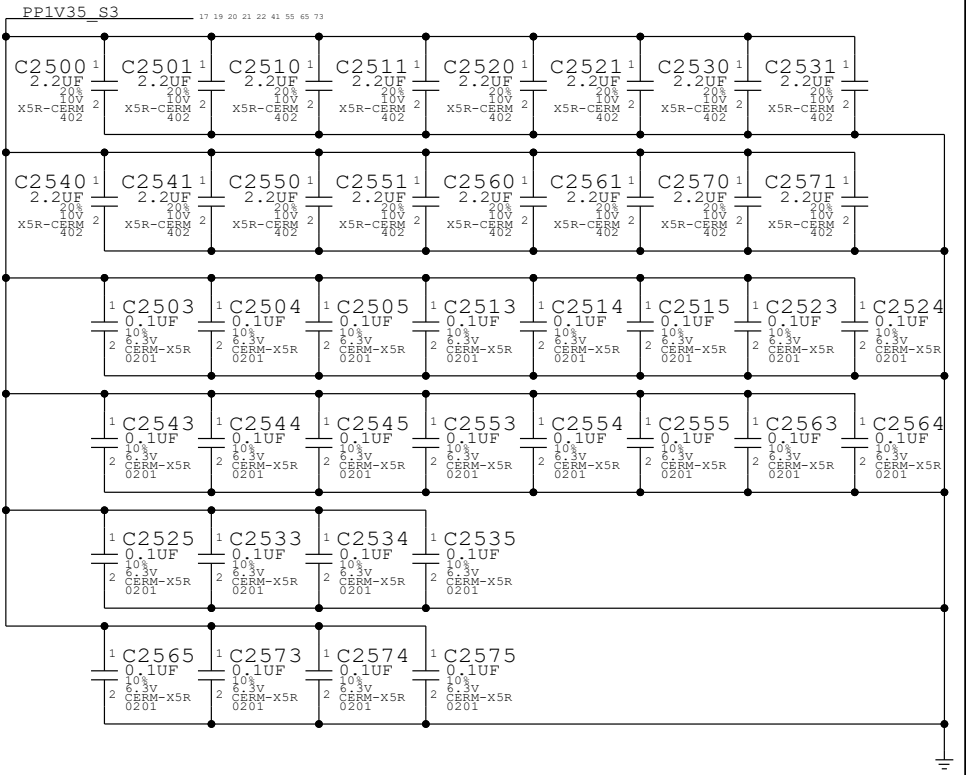
SDRAM BYPASSING (NOTE: 4X 2.2UF AND 6X 0.1UF PER CHIP)

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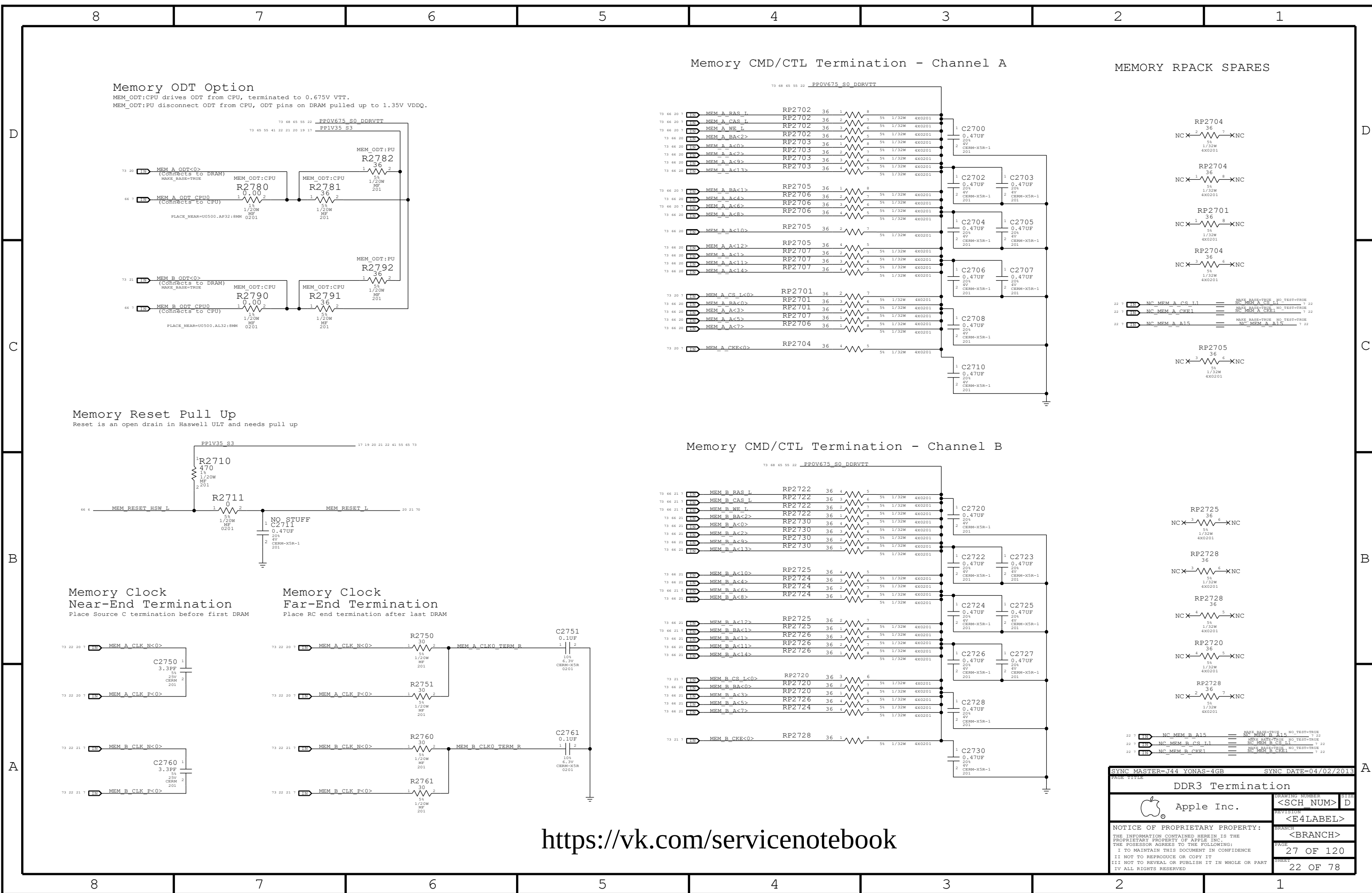


SDRAM BYPASSING (NOTE: 4X 2.2UF AND 6X 0.1UF PER CHIP)

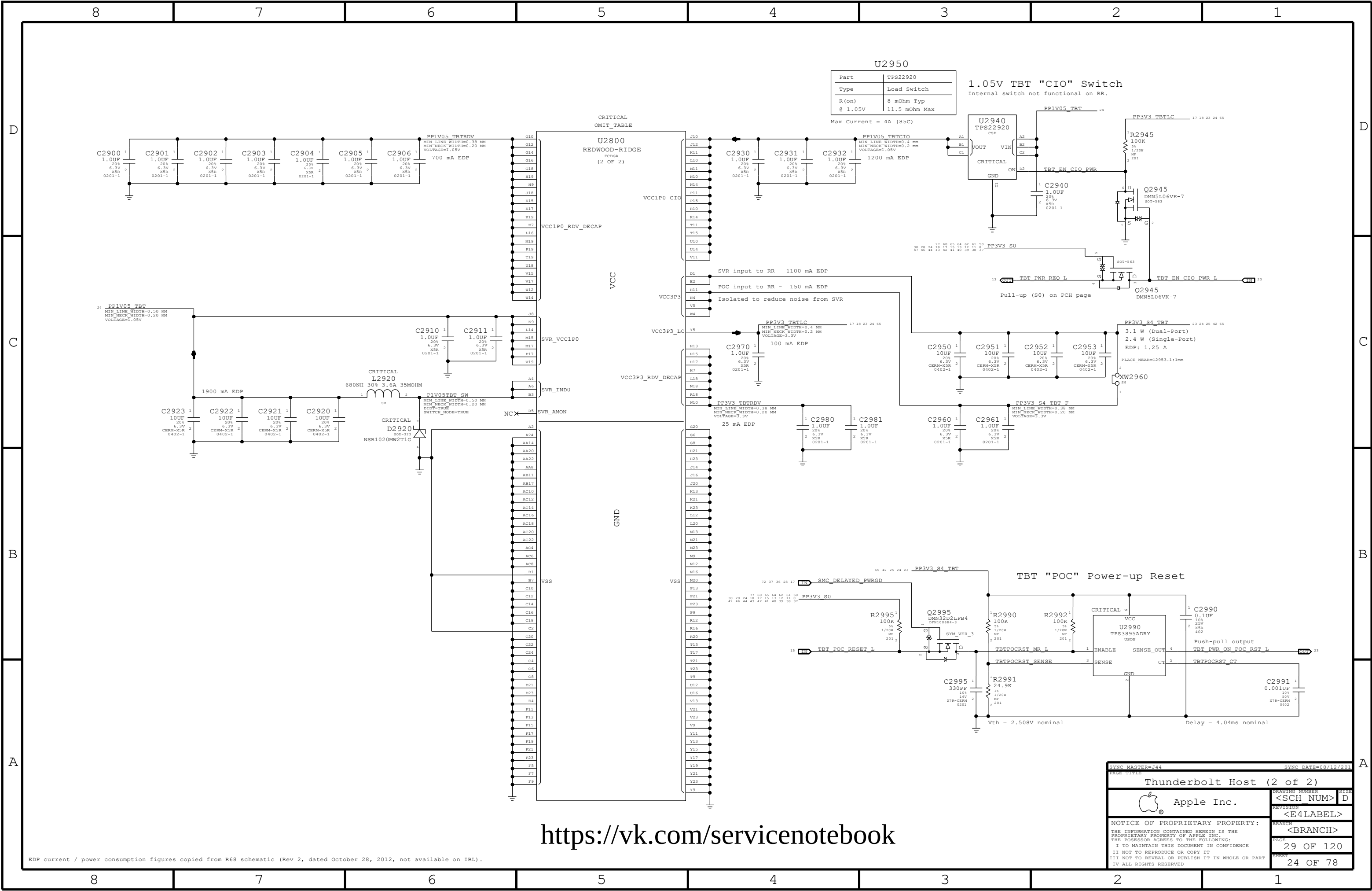


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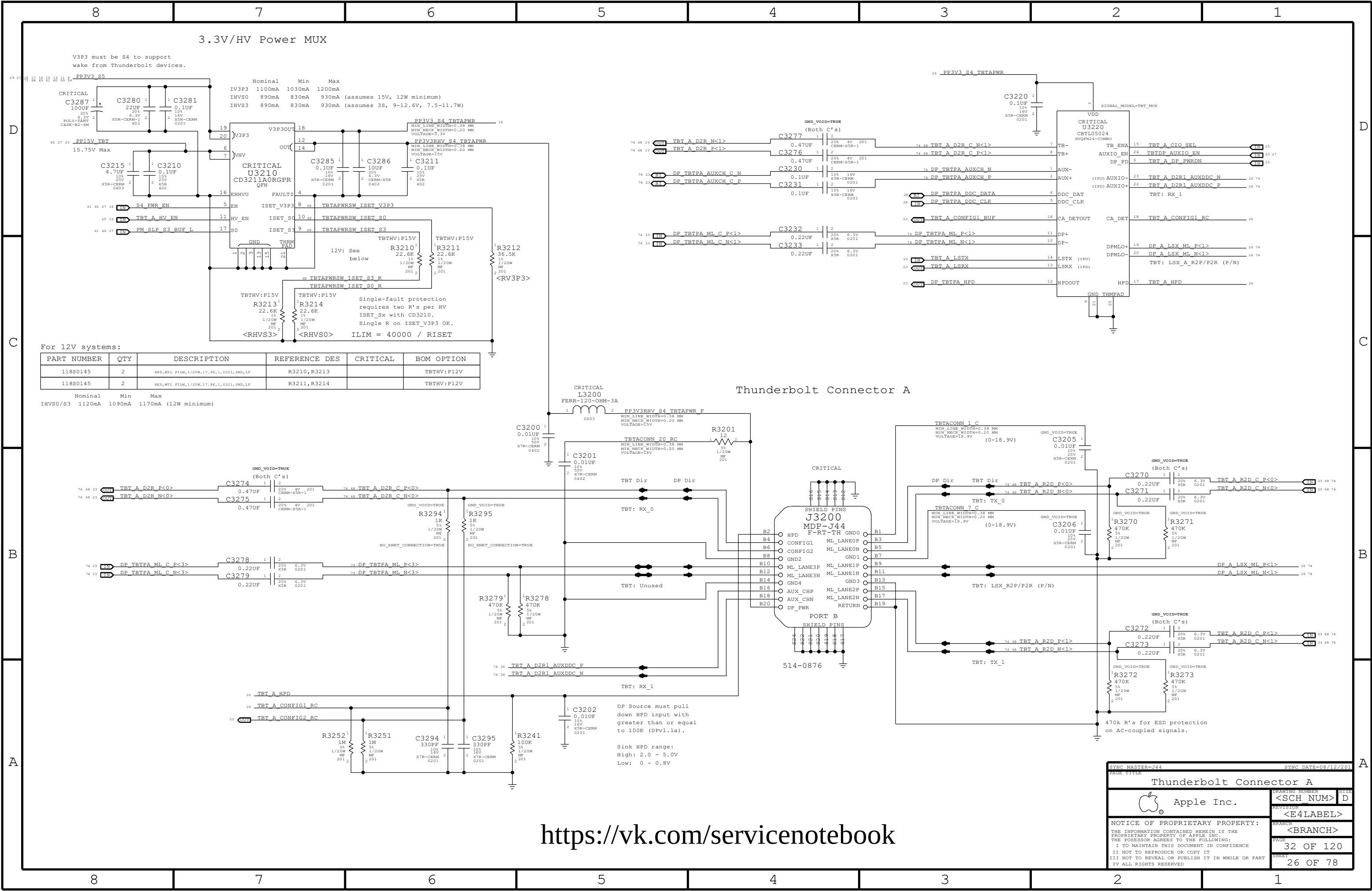




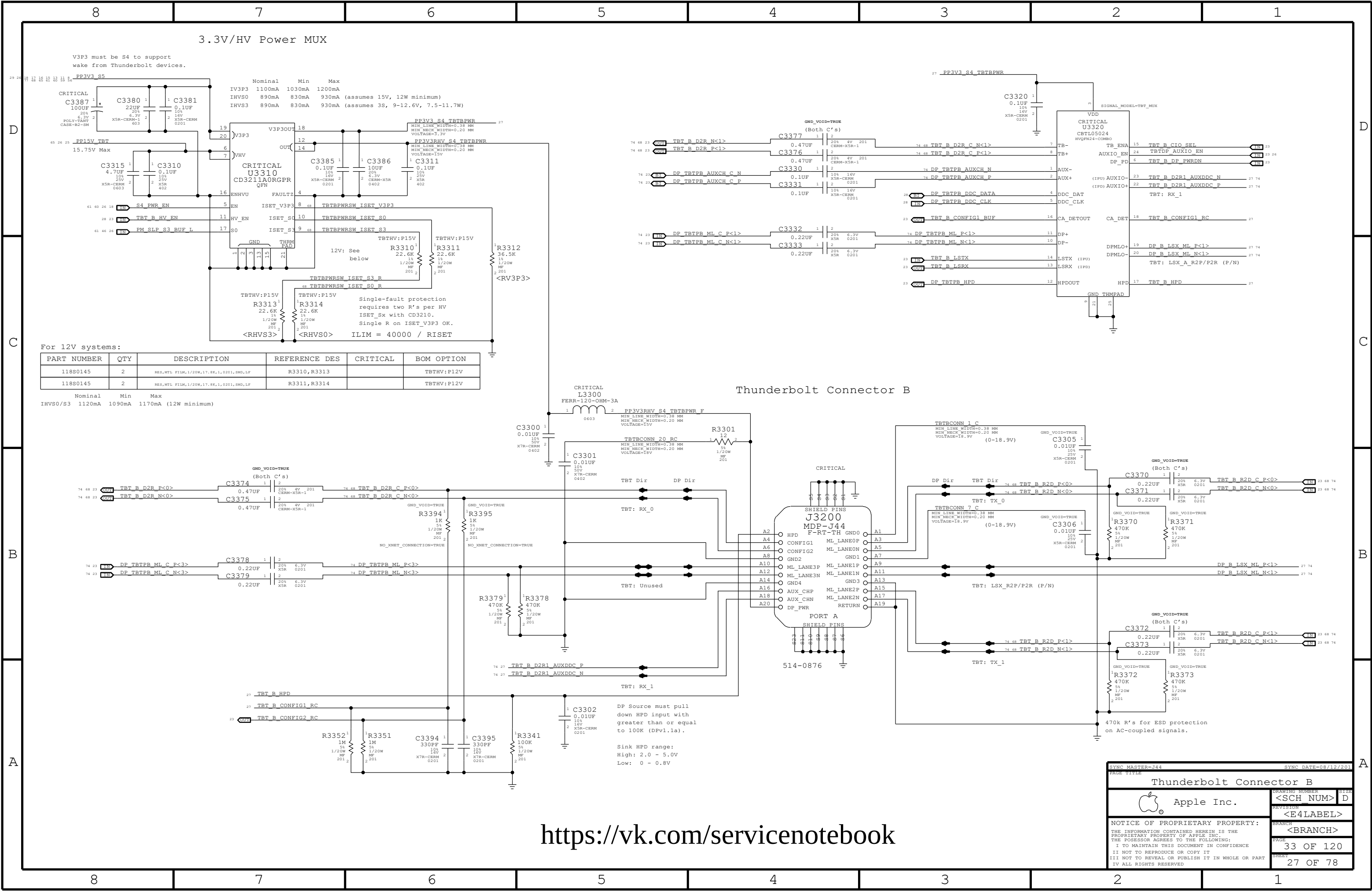


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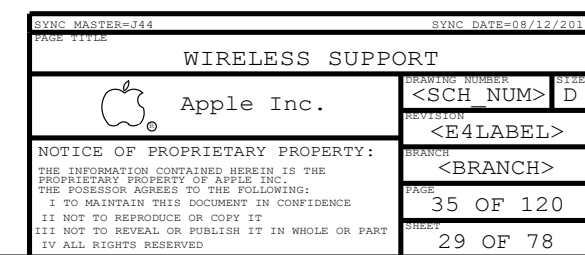
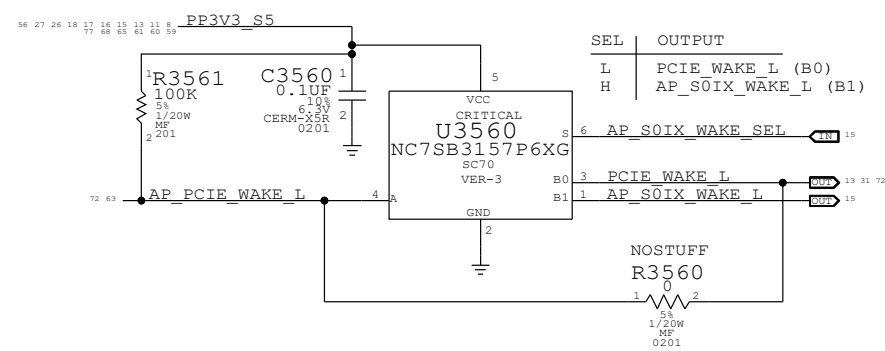
EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).



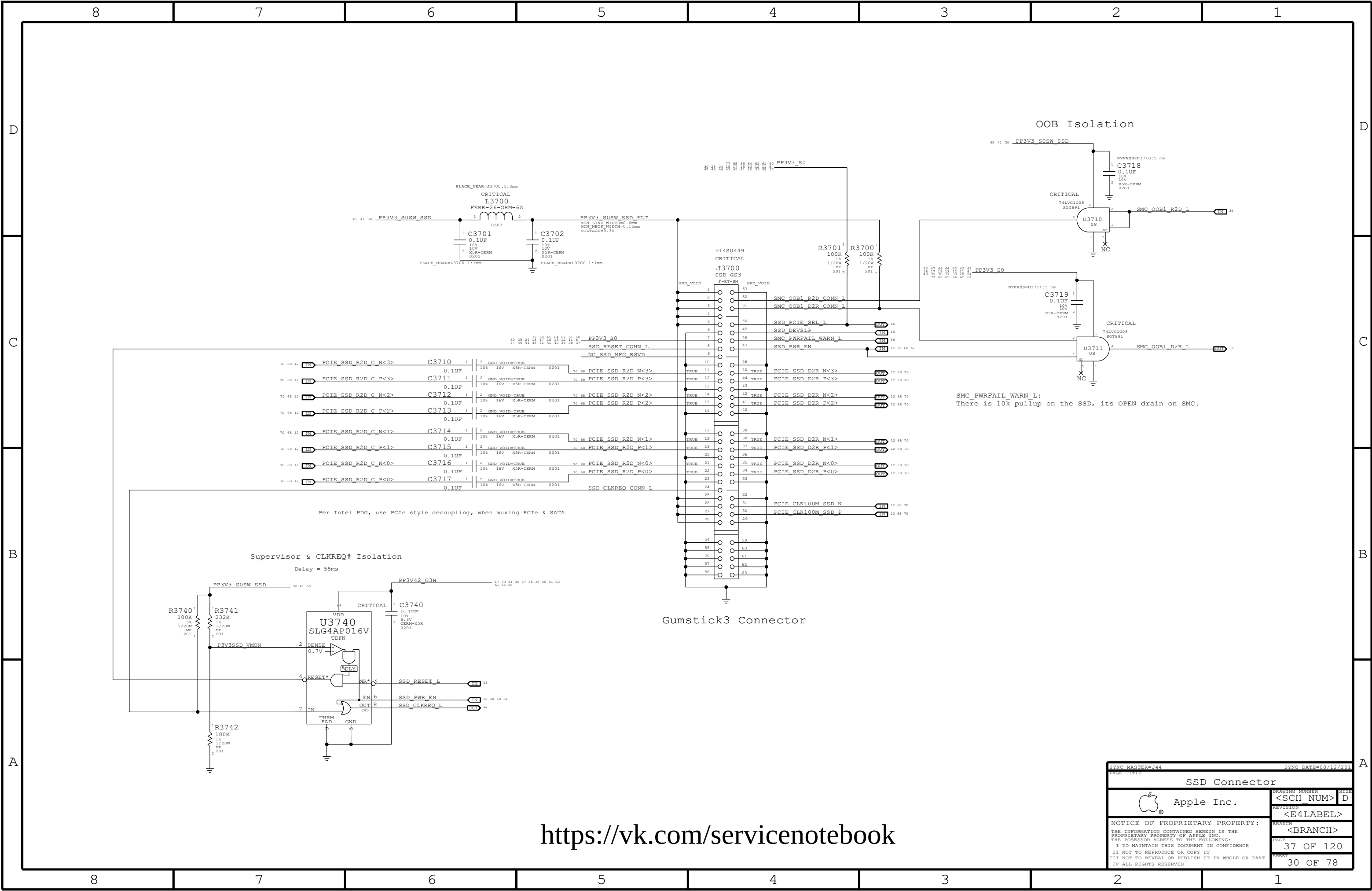
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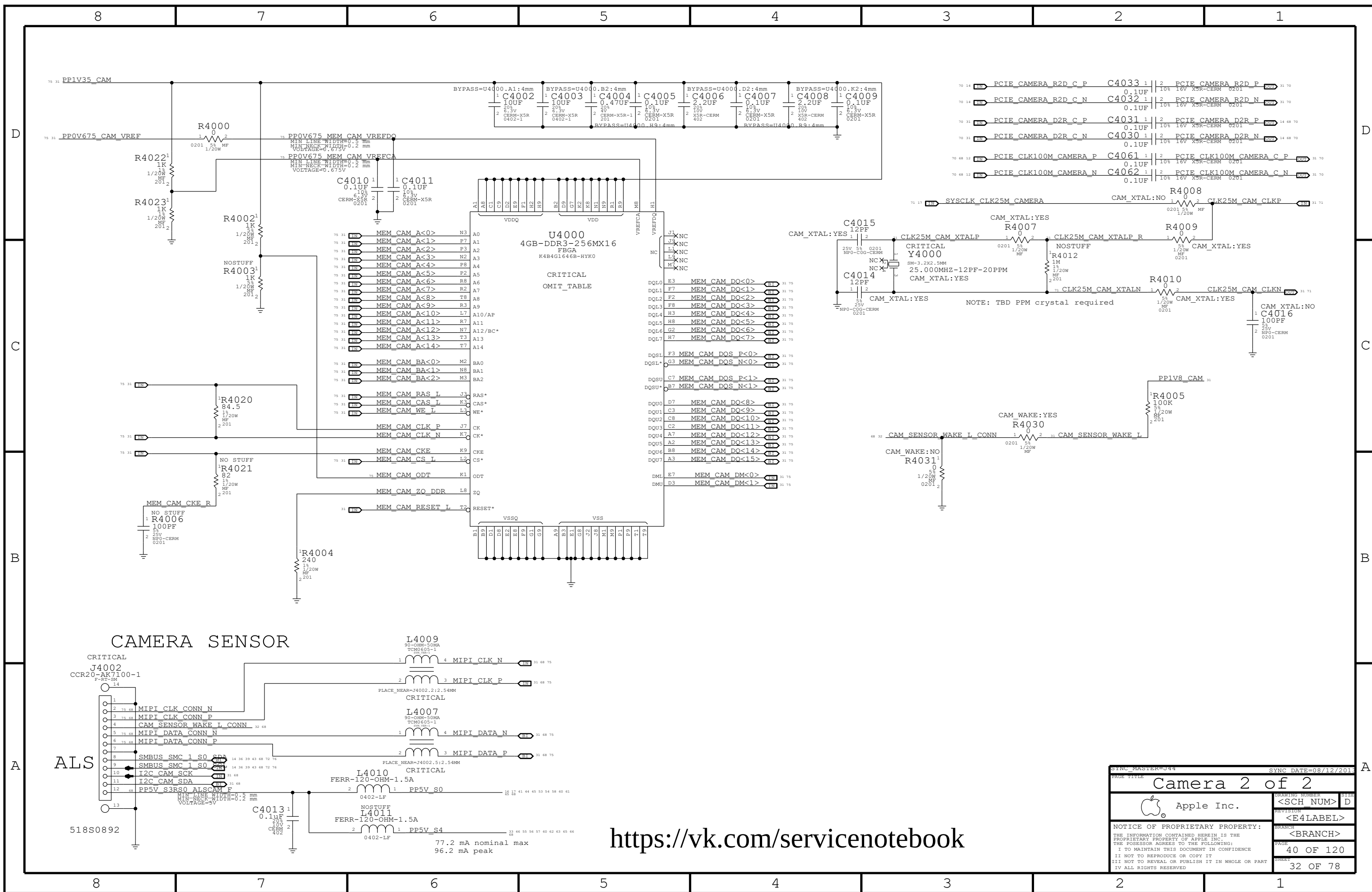
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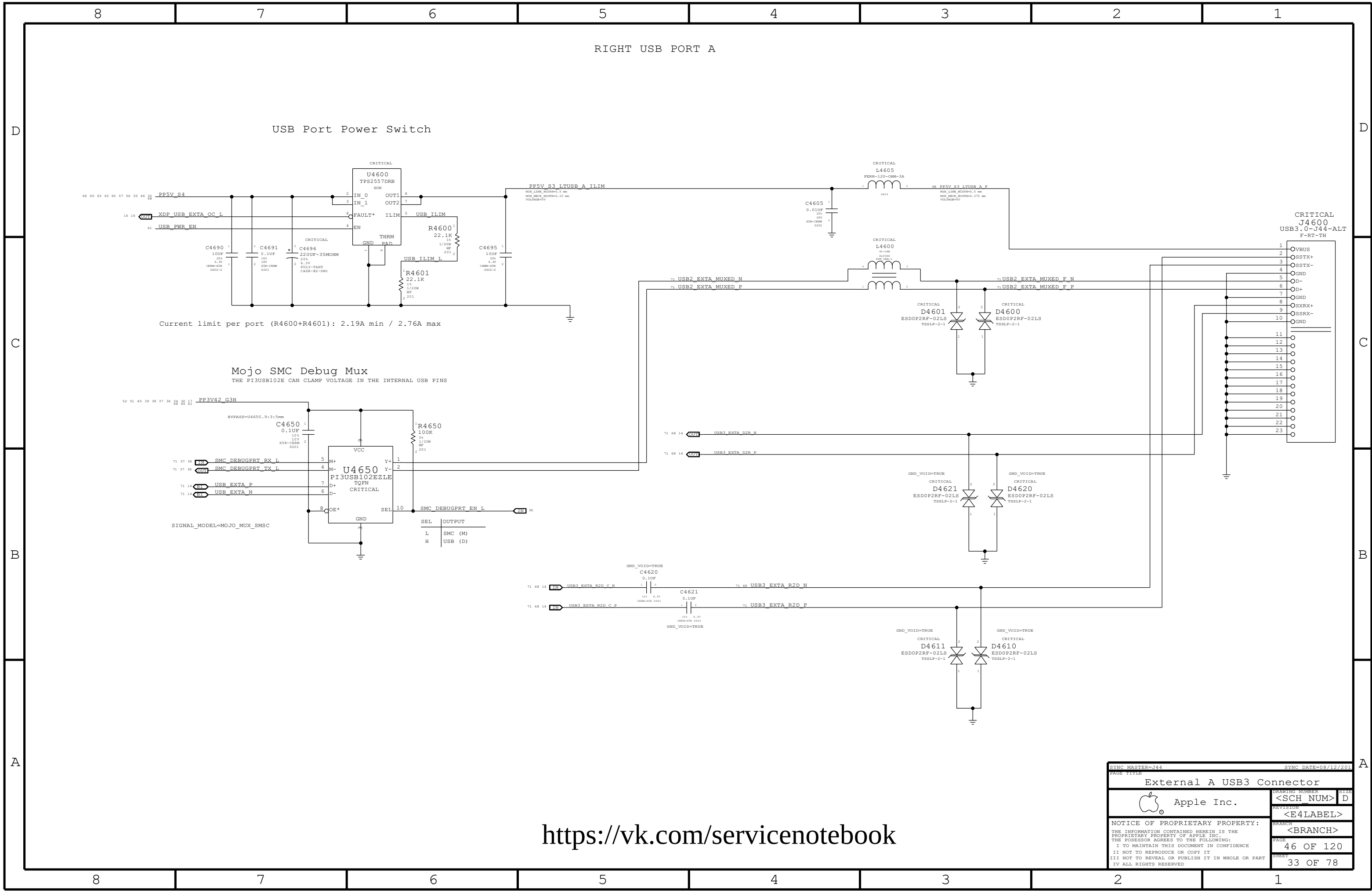


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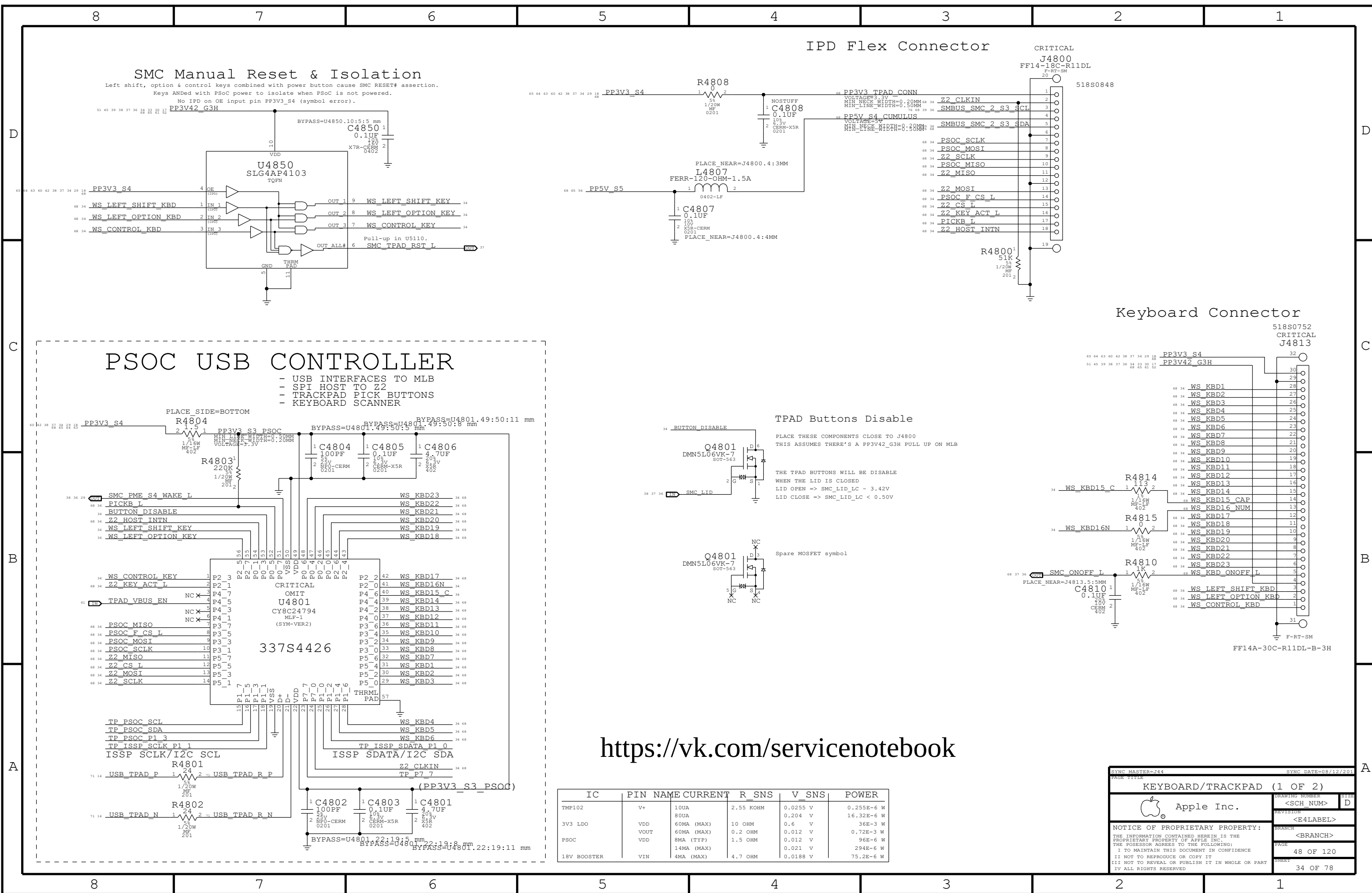


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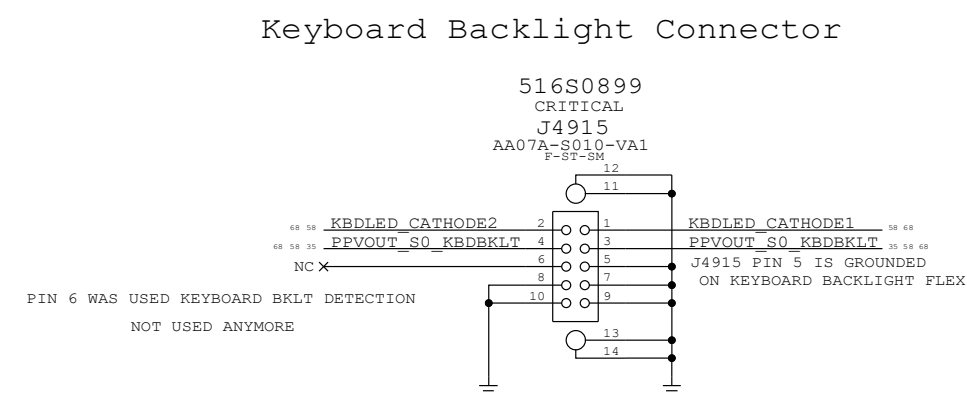


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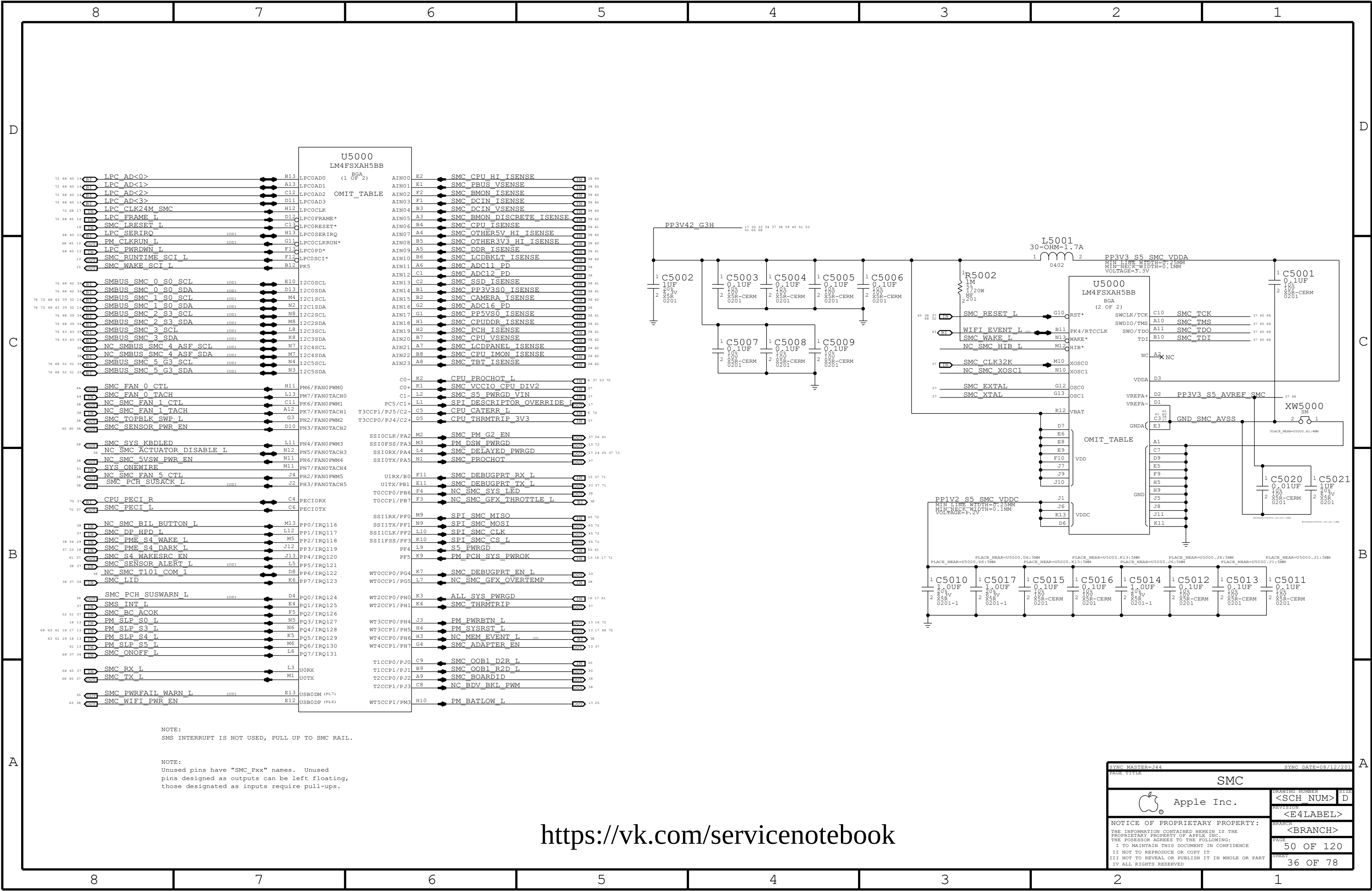
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TMPL02	V+	100A		2.55	KOHM	0.0255	V	0.255E-6 W
		100A				0.2025	V	1.632E-6 W
3V3 LDO	VDD	60MA (MAX)	10	OHM	0.6	0.168	V	1.632E-6 W
	YOUT	60MA (MAX)	2	OHM	0.012	V	0.72E-3 W	
PSOC	VDD	8MA (TYP)	1.5	OHM	0.012	V	96E-6 W	
		14MA (MAX)			0.021	V	294E-6 W	
18V BOOSTER	VIN	4MA (MAX)	4.7	OHM	0.188	V	75.2E-6 W	

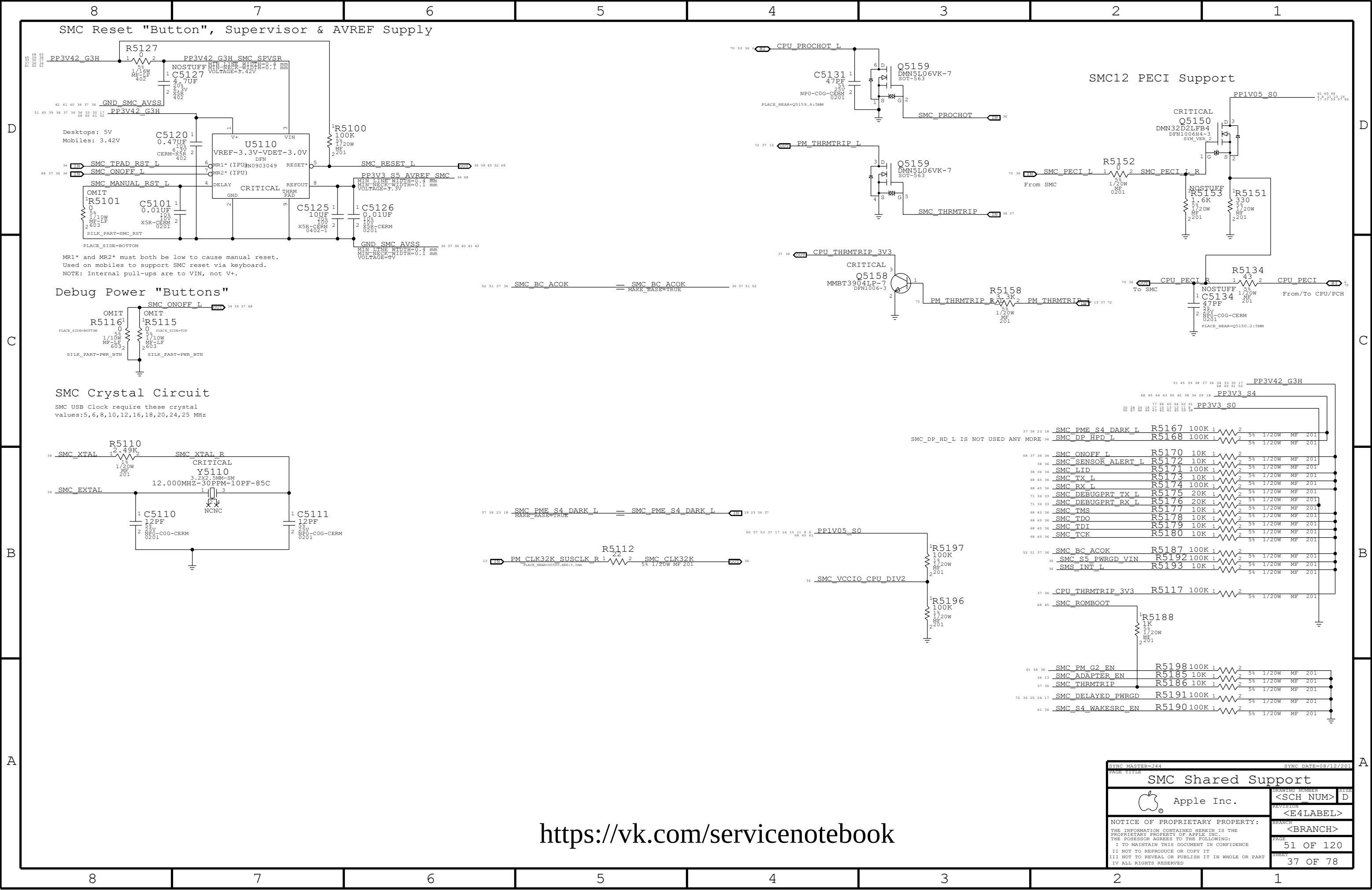
NYC-MASTER-144		NYC DATE=08/12/2011	
PAGE TITLE			
KEYBOARD/TRACKPAD		(1 OF 2)	
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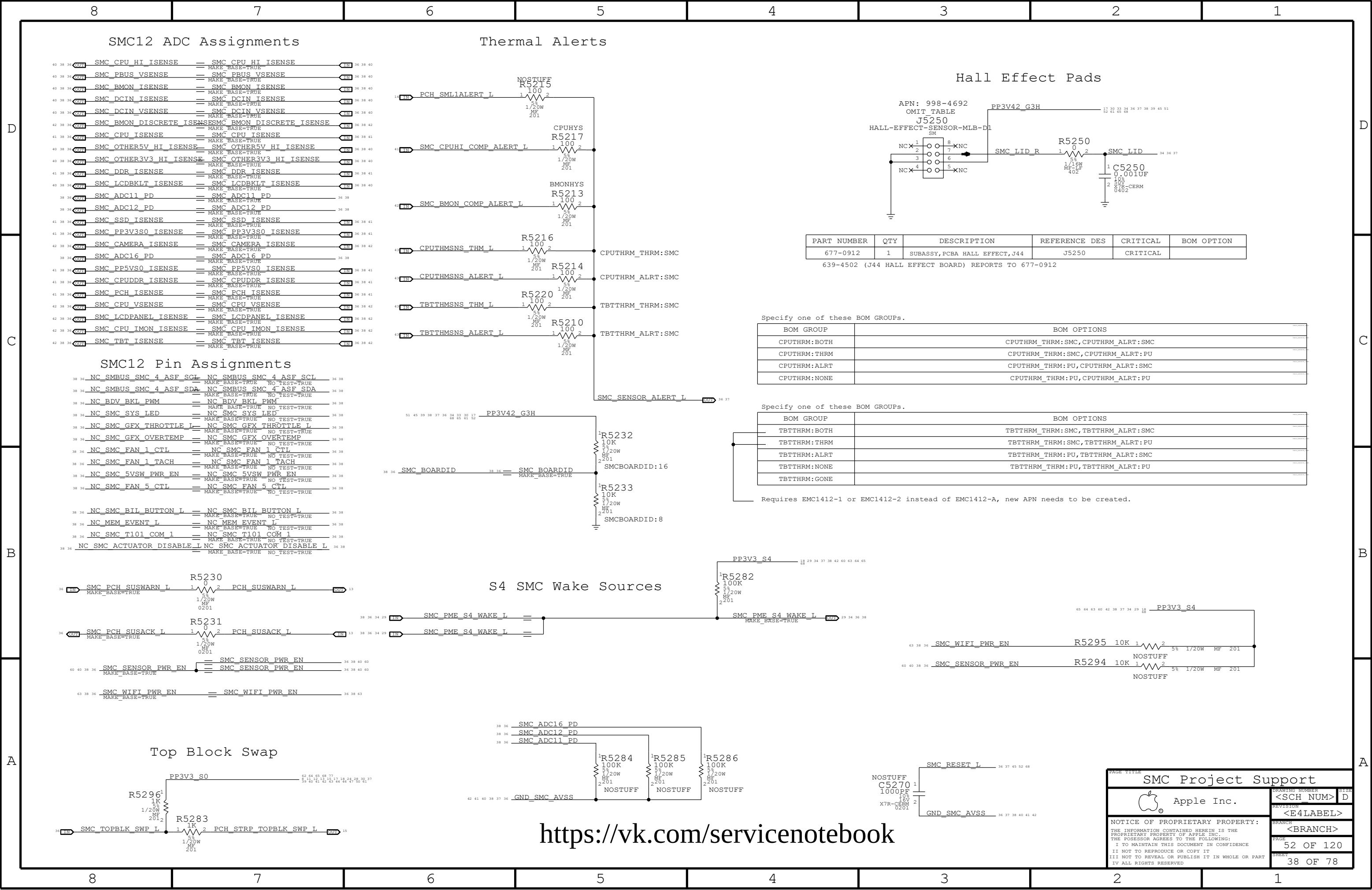
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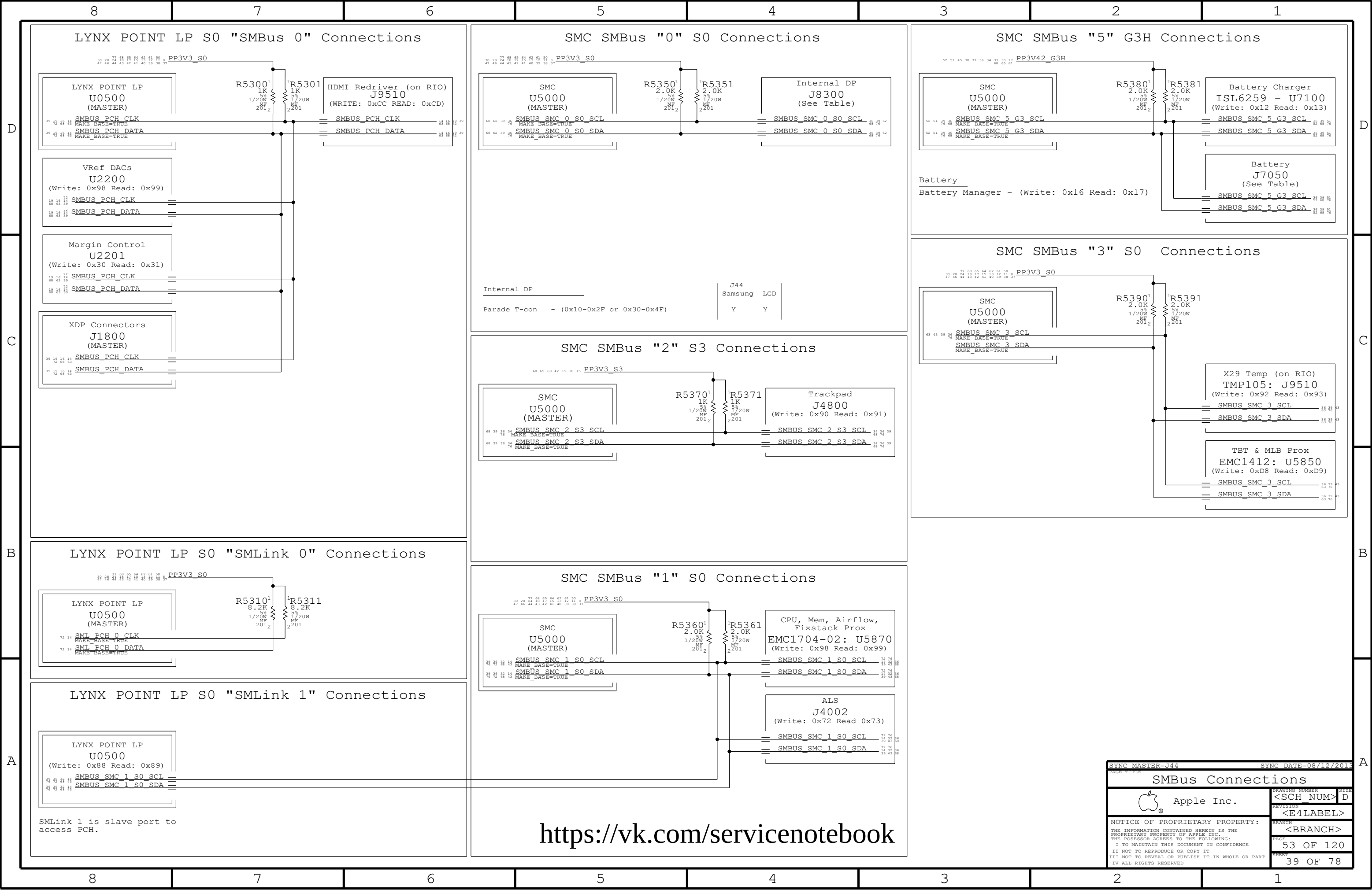


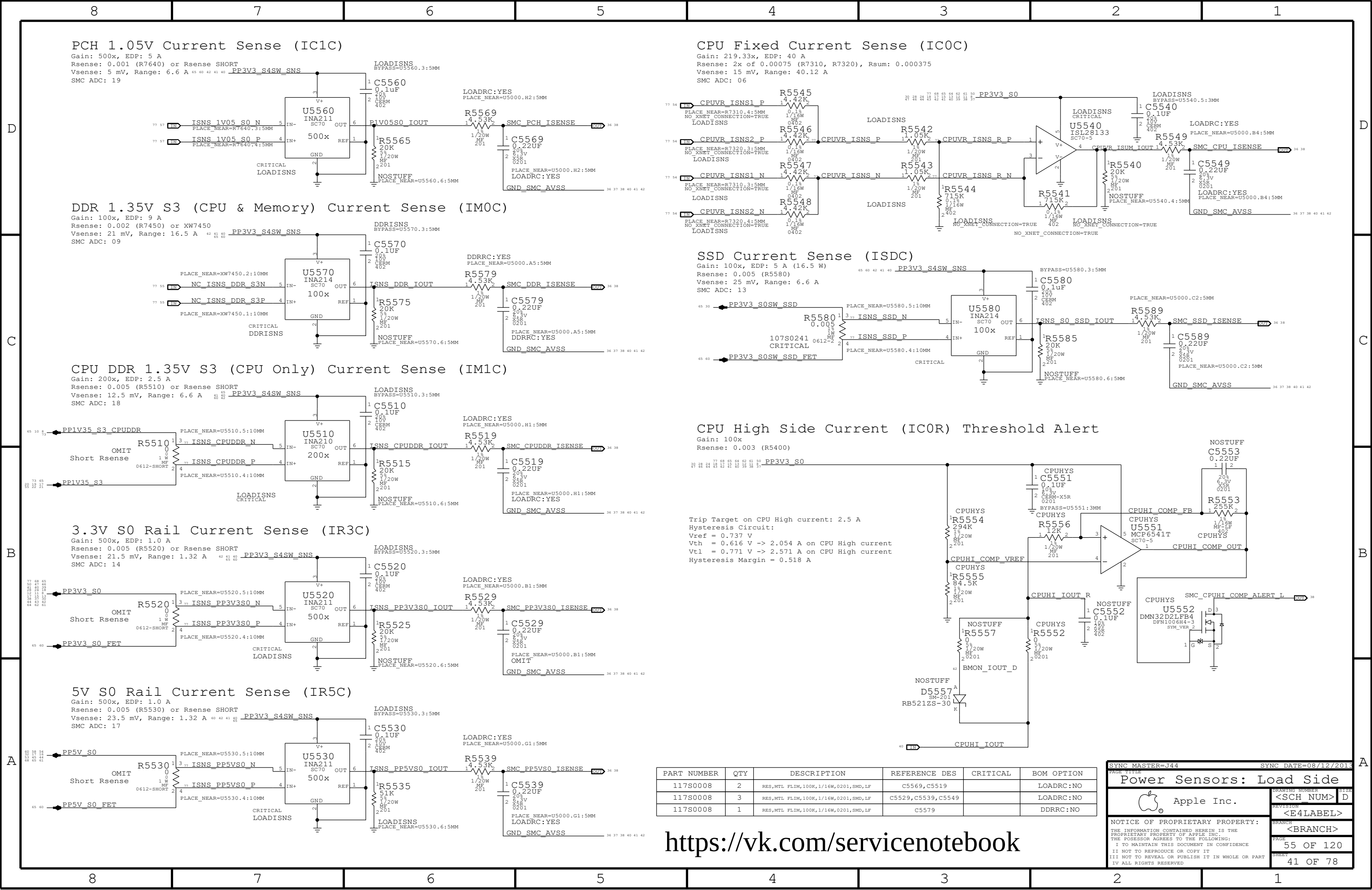


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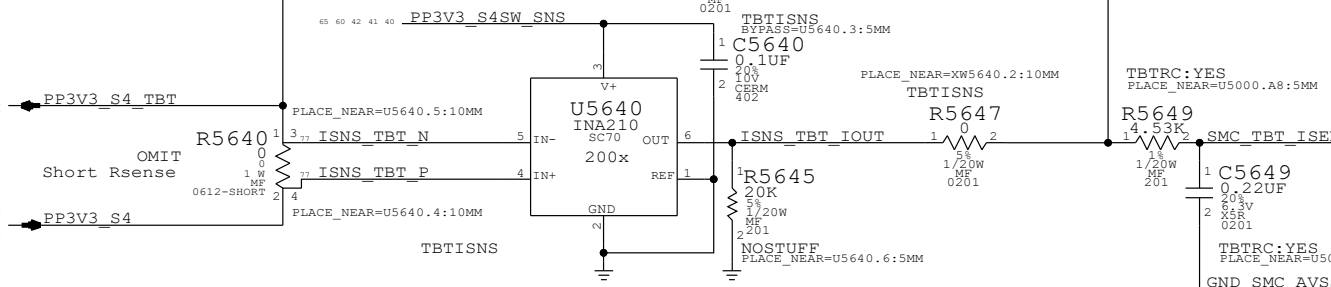


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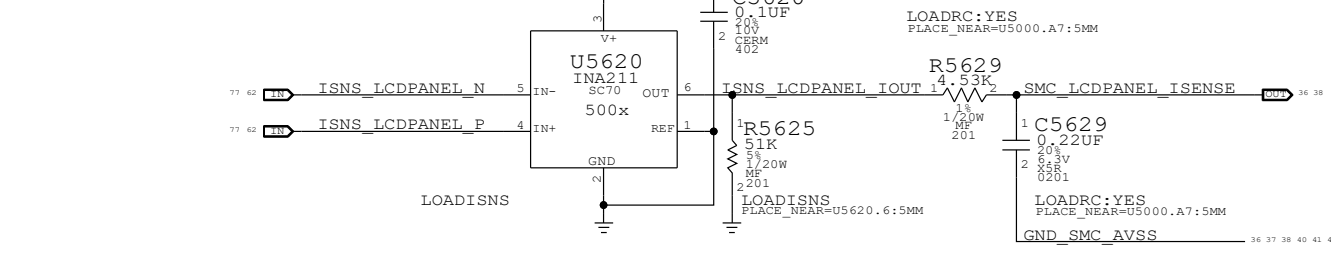
Thunderbolt TBT Current/Voltage Sense (IHSC/VHSC)

Gain: 200x. EDP: 2.0 A
Rsense: 0.005 (R5640) or Rsense SHORT XW5640
Vsense: 14 mV, Range: 3.3
SMC AD: 23



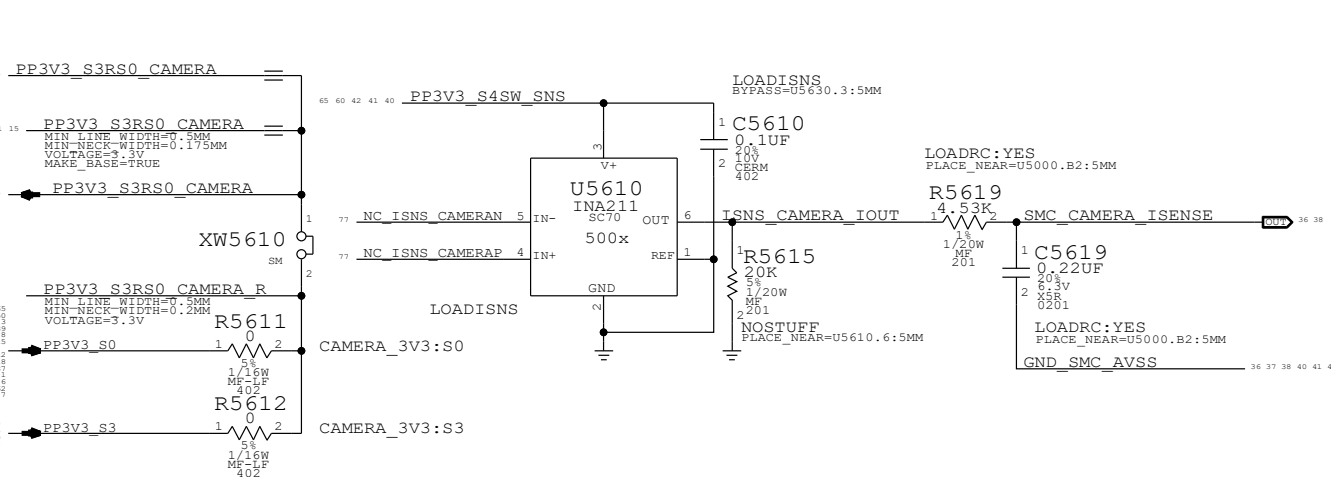
LCD Panel Current Sense (ILDC)

Gain: 500x. EDP: 1 A
Rsense: 0.005 (R8320) or Rsense SHORT
Vsense: 5 mV, Range: 1.32 A
SMC AD: 21



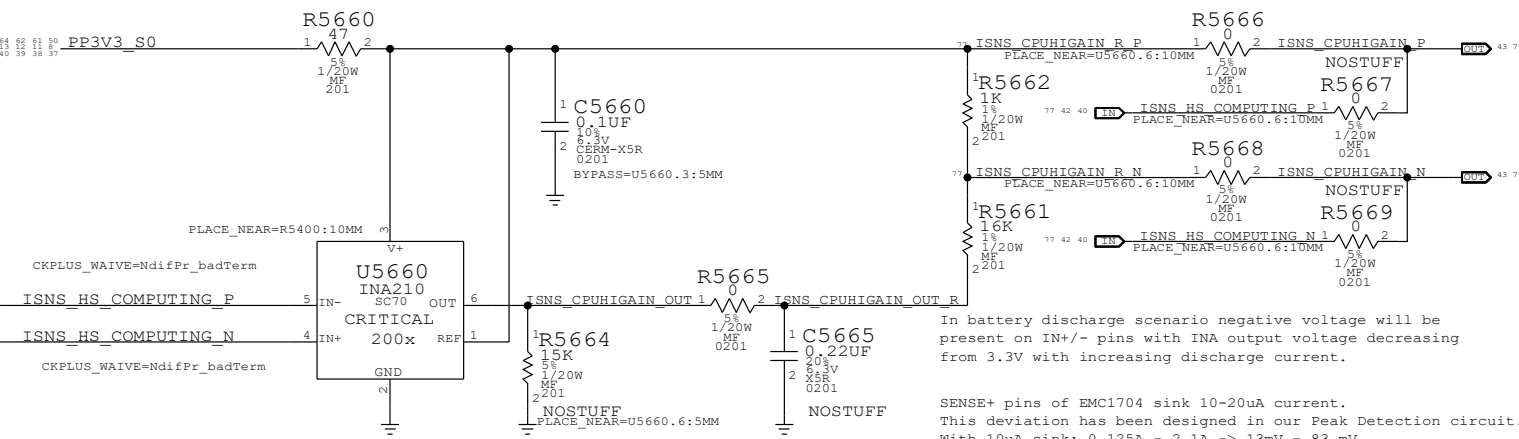
Camera (S2 Controller) Current Sense (ICMC)

Gain: 500x. EDP: 0.82 A
Rsense: 0.005 (R5610) or XW5610
Vsense: 4.1 mV, Range: 1.32 A
SMC AD: 15



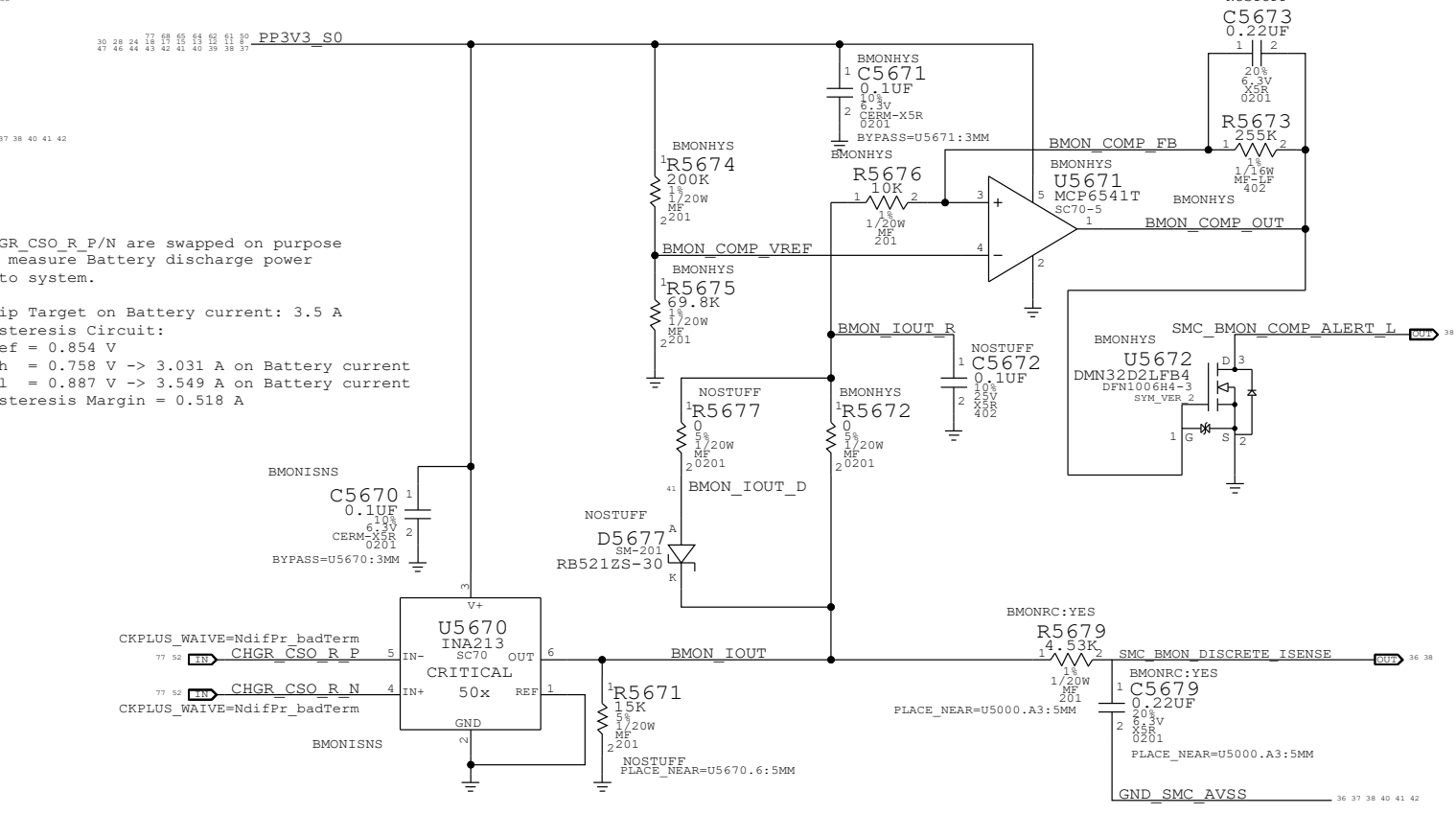
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL F12M,100K,1/16W,0201,SMD,LF	C5619,C5629,C5649		
117S0008	1	RES,MTL F12M,100K,1/16W,0201,SMD,LF	C5679		

CPU High Side (IC0R) Peak Detection Support

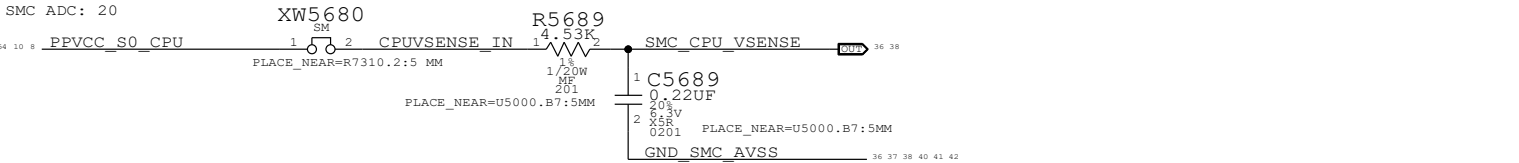


Battery BMON Discrete Current Sense (IPOR) & Threshold Alert

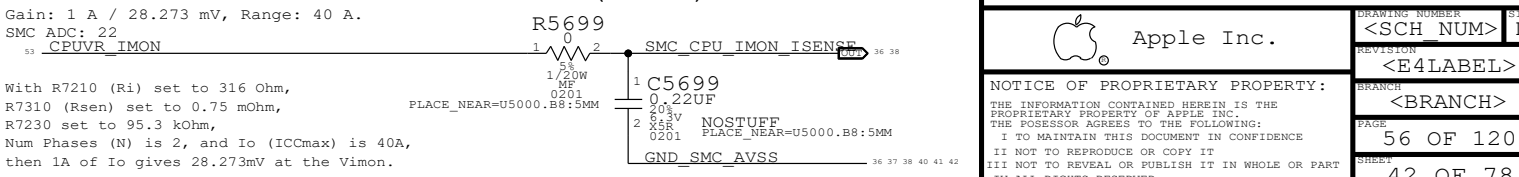
Gain: 50x. EDP: 8 A
Rsense: 0.005 (R7150)
Vsense: 50 mV, Range: 13.2 A
SMC AD: 05



CPU Core Voltage Sense (VC0C)



CPU Core IMON Current Sense (IC2C)



SYMC MASTER-144SYMC DATE=08/12/2013

Power Sensors: Extended

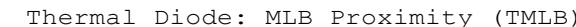
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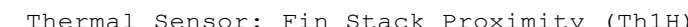
REVISION: 1114
<SCH NUM> D
<E4LABEL>
<BRANCH>
PAGE 56 OF 120
42 OF 78

I2C Write: 0xD8, I2C Read: 0xD9


The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AA8.



CPU Proximity,

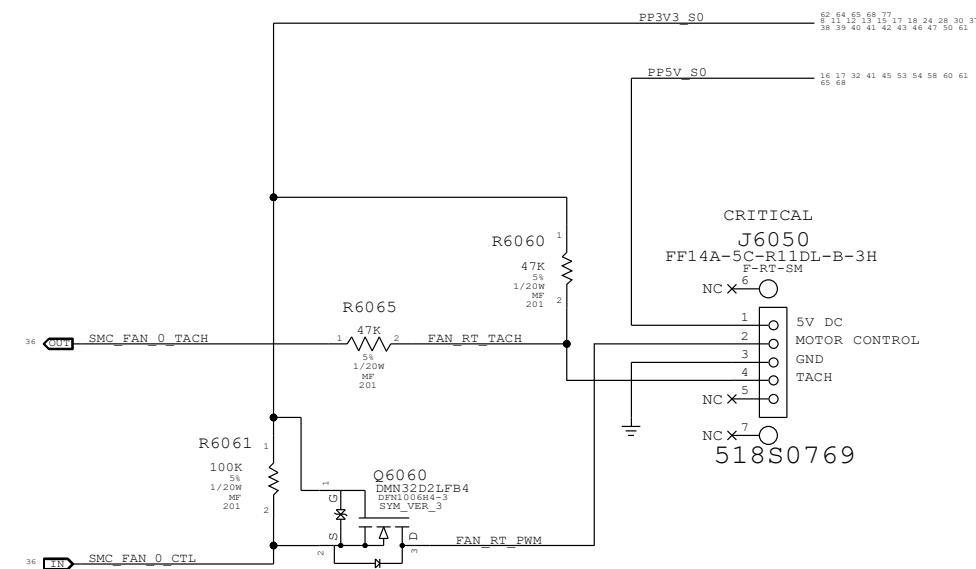


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PAGE 11111			
<h1>Thermal Sensors</h1>			
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		INDEX 43 OF 78	

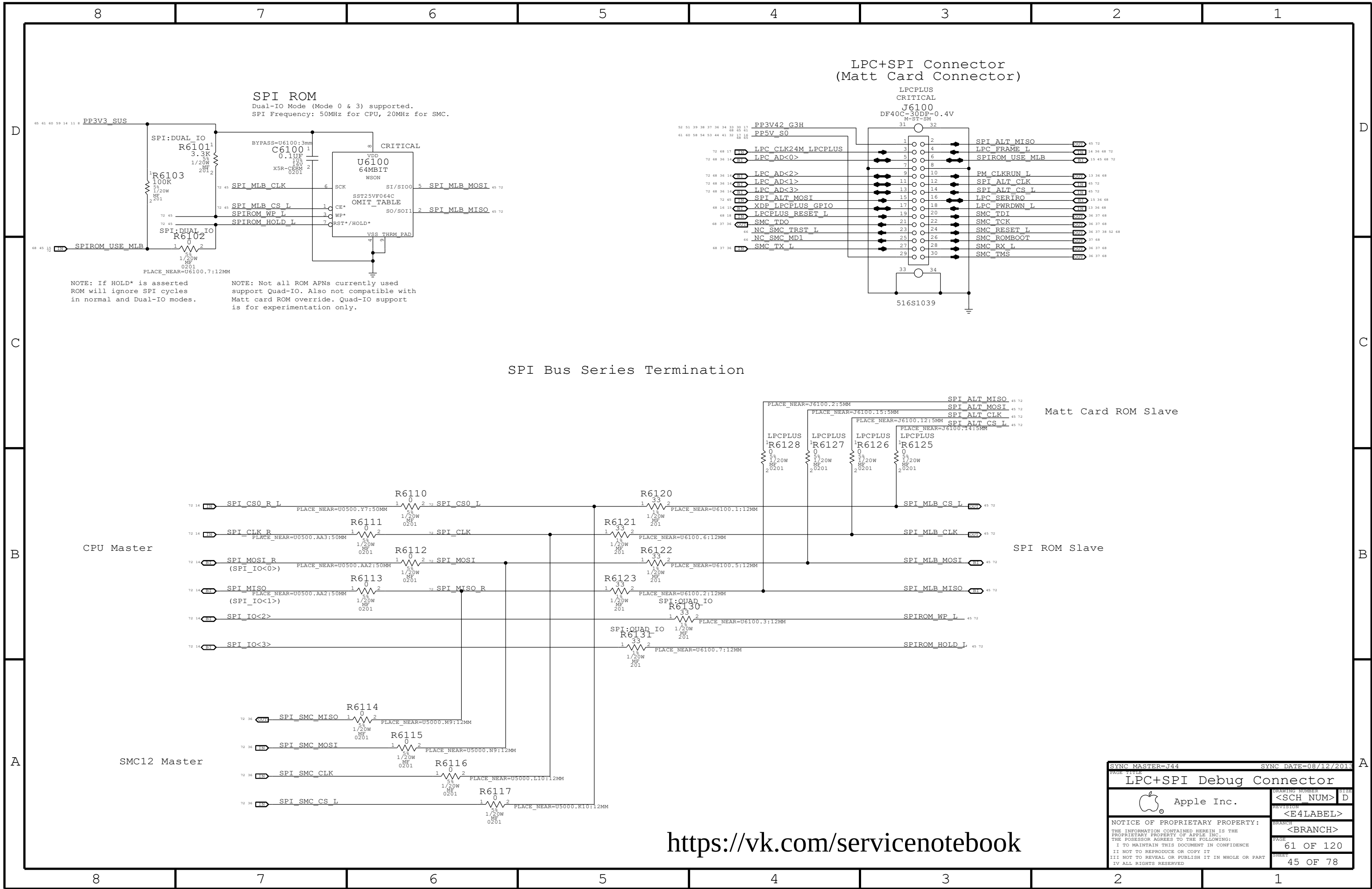
FAN CONNECTOR

KEEP THE 5 PIN CONNECTOR FROM D1



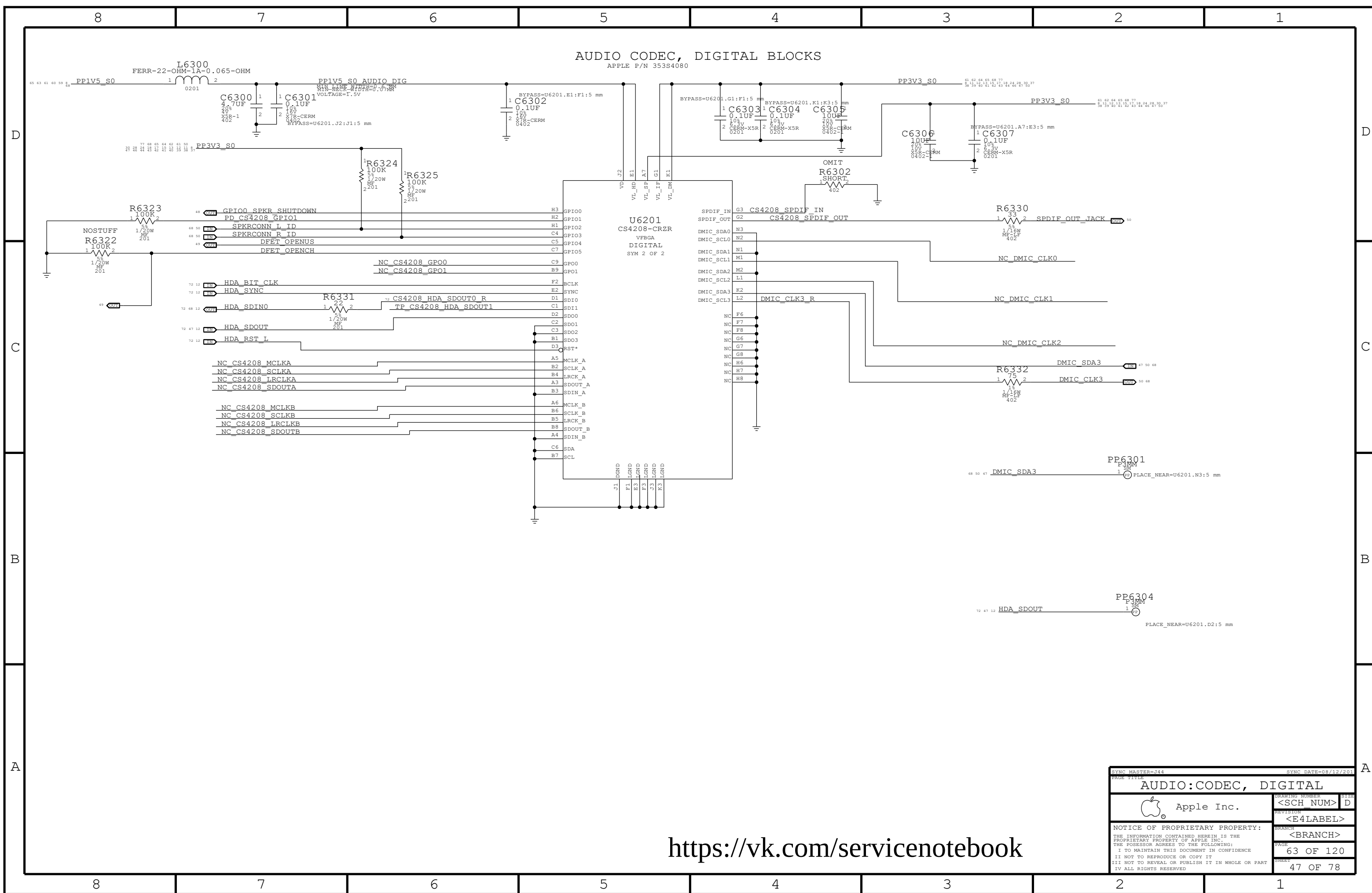
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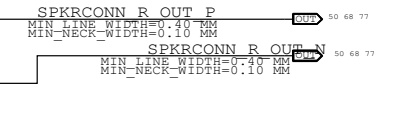
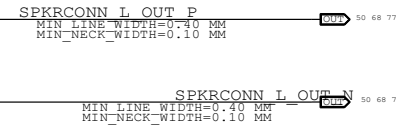
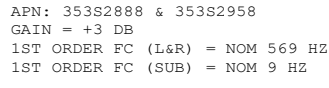
SYN: MASTER-344		SYN: DATE=08/12/2011	
PAGE 111111			
		Fan	
Apple Inc.		DRAWING NUMBER <SCH NUM>	ITEM D
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		60 OF 120	44 OF 78




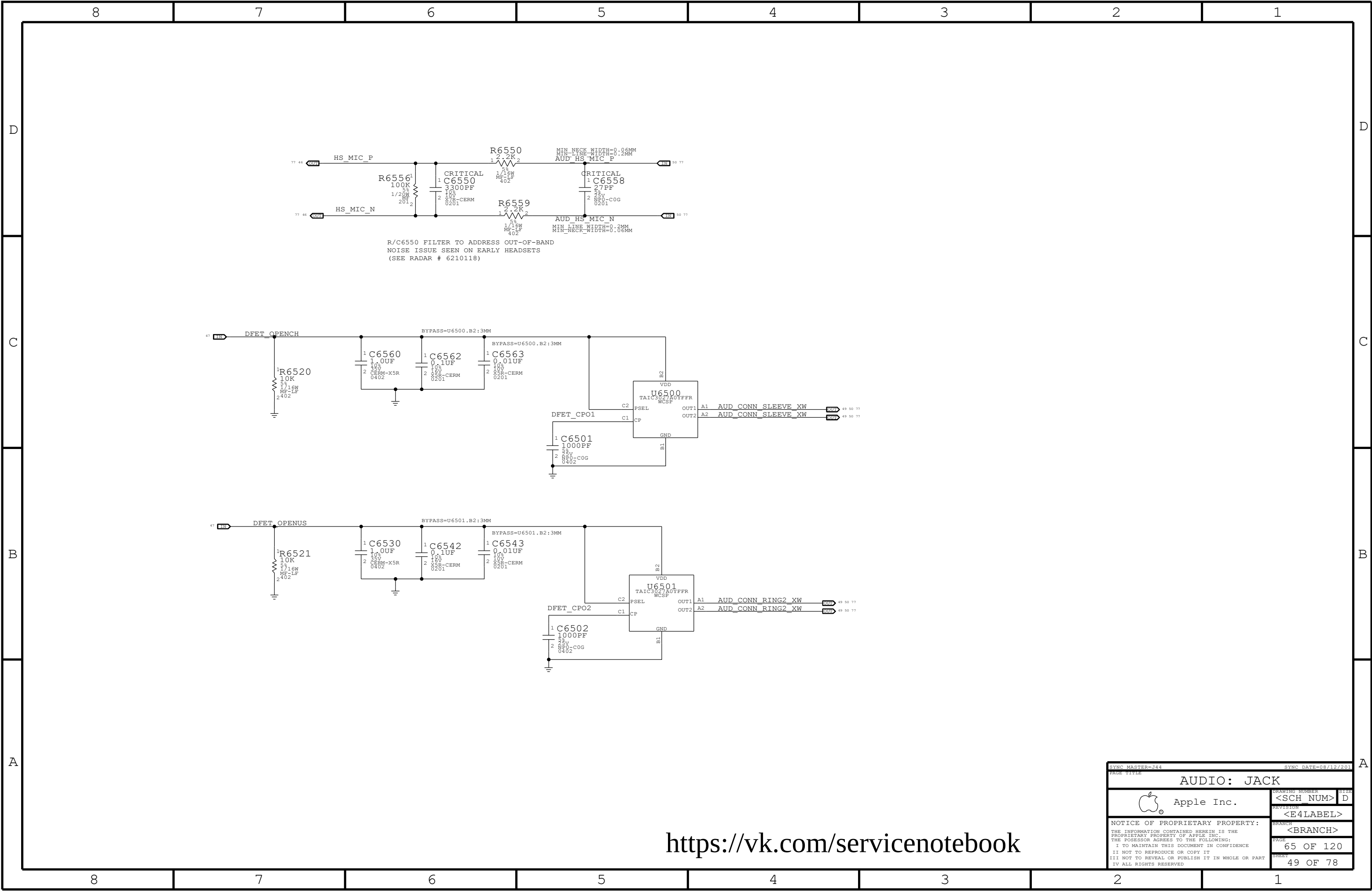
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SYNC MASTER-344		SYNC DATE-08/12/2013	
LPC+SPI Debug Connector		REV: 1.1	
Apple Inc.		<SCH NUM> D	
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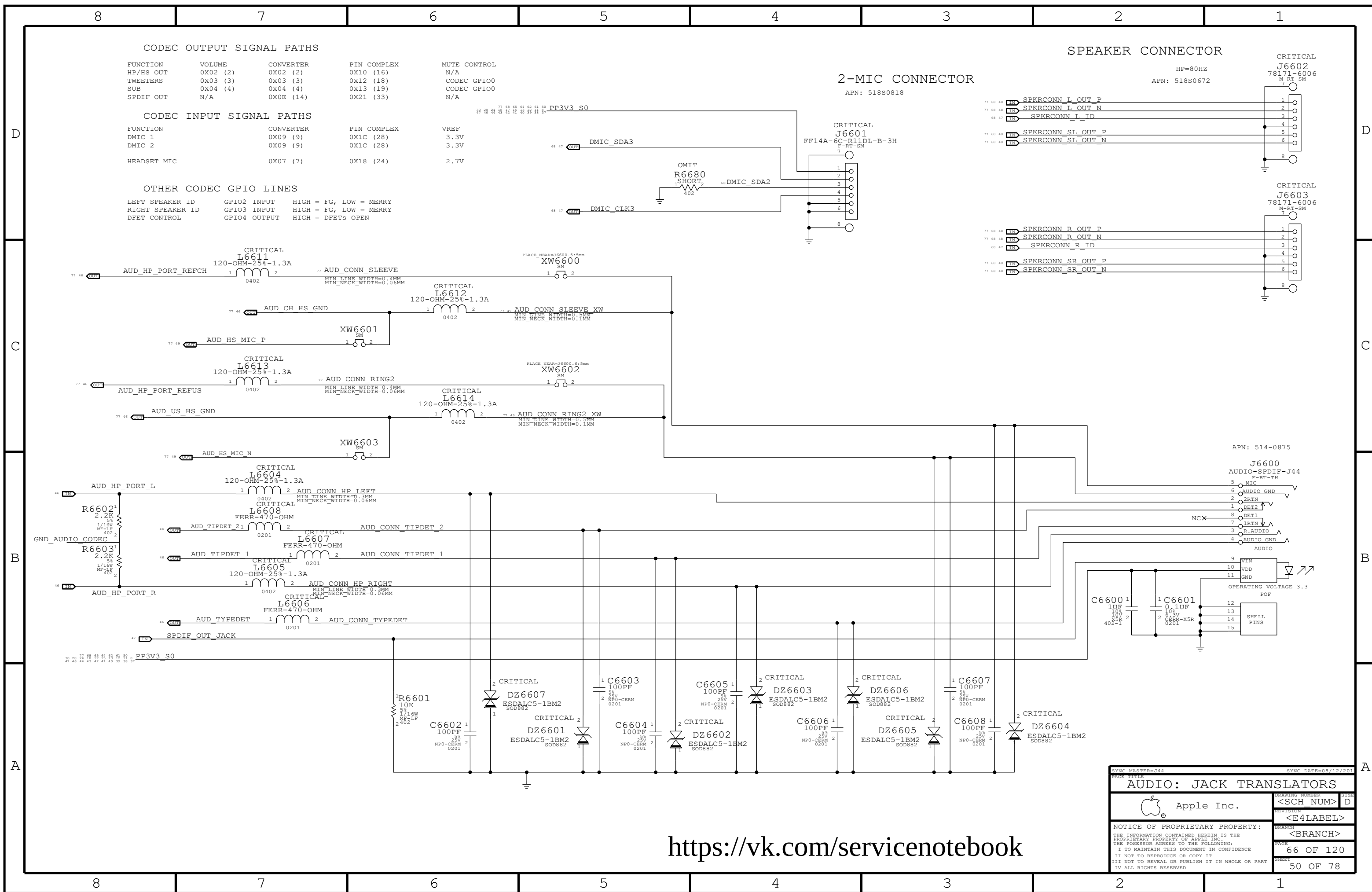


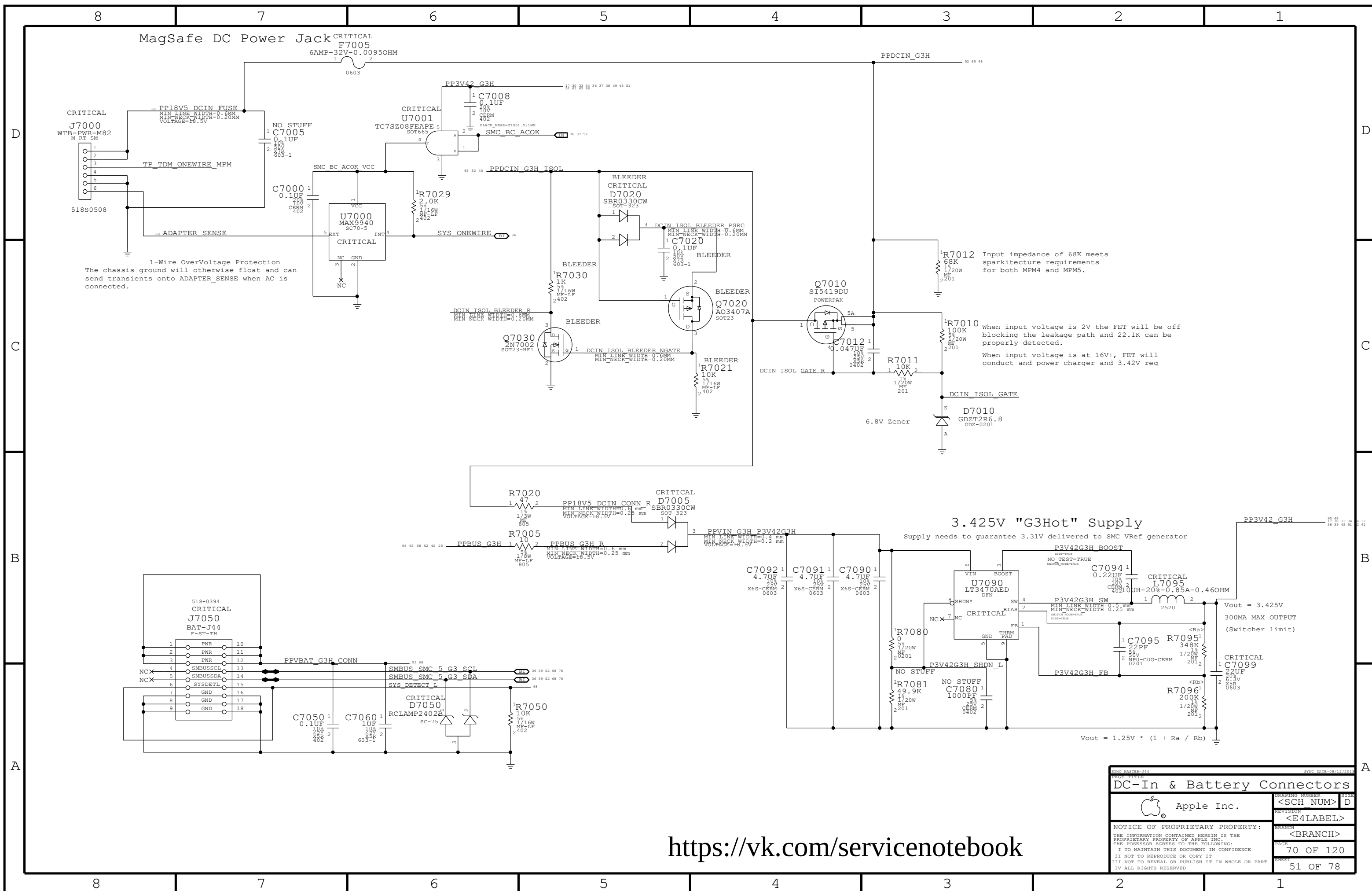
VIN# MASTER-744 MAKE TITLE		SYNC DATE-08/12/2011	
<h1>AUDIO: SPEAKER AMP</h1>			
 Apple Inc.		DRAWING NUMBER <SCH NUM>	TITLE D
		REVISION <E4LABEL>	
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		STREET 48 of 78	

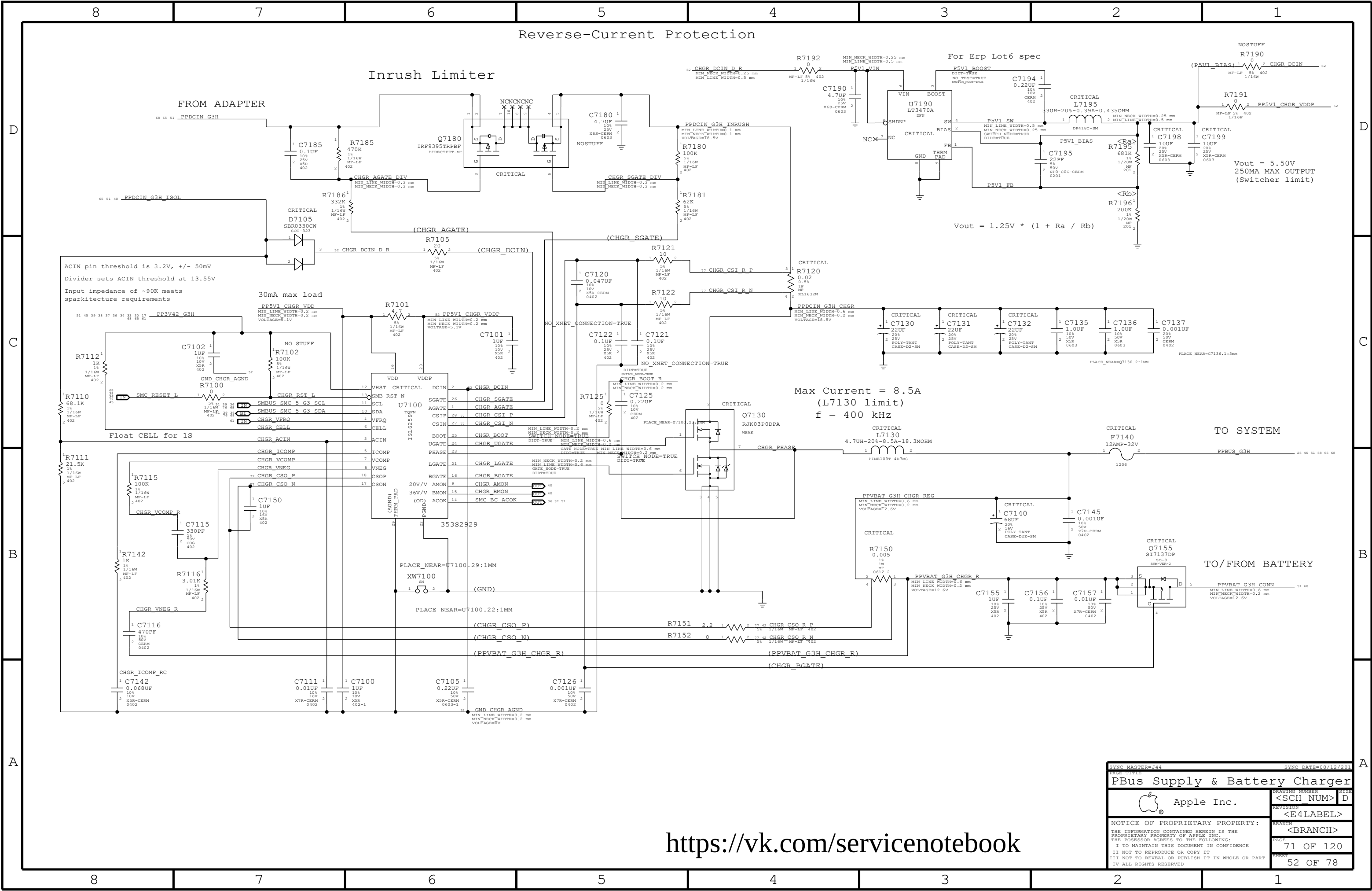


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 Apple Inc.	DRAWING NUMBER		0110
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		<BRANCH>	
		PAGE	65 OF 120
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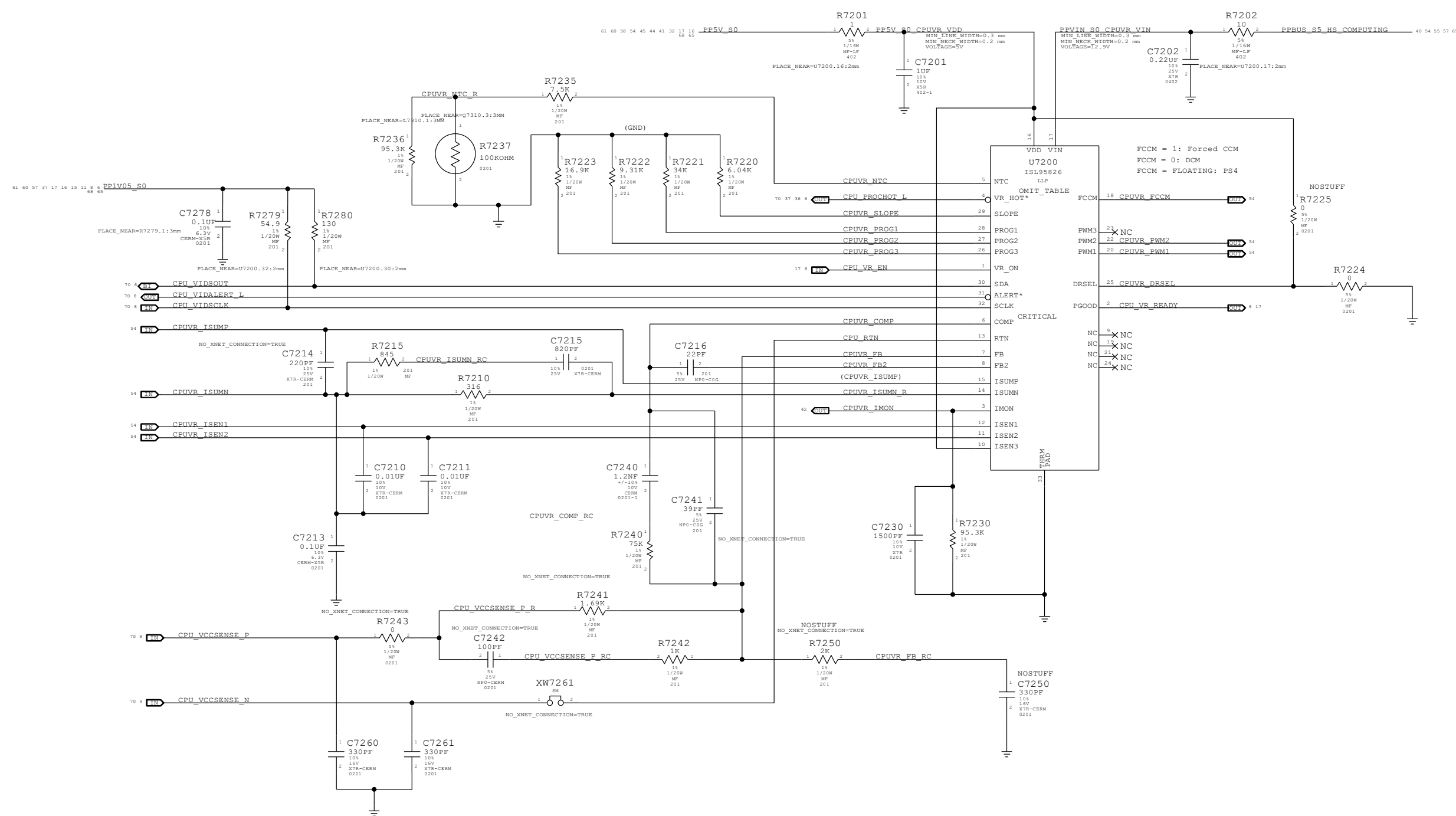







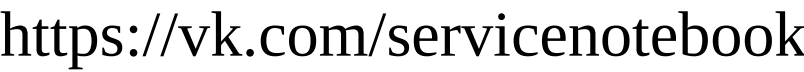
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC, ISL95826R6200, PPM, PGOOD, SCREN, 32P, QFN	U7200	CRITICAL	

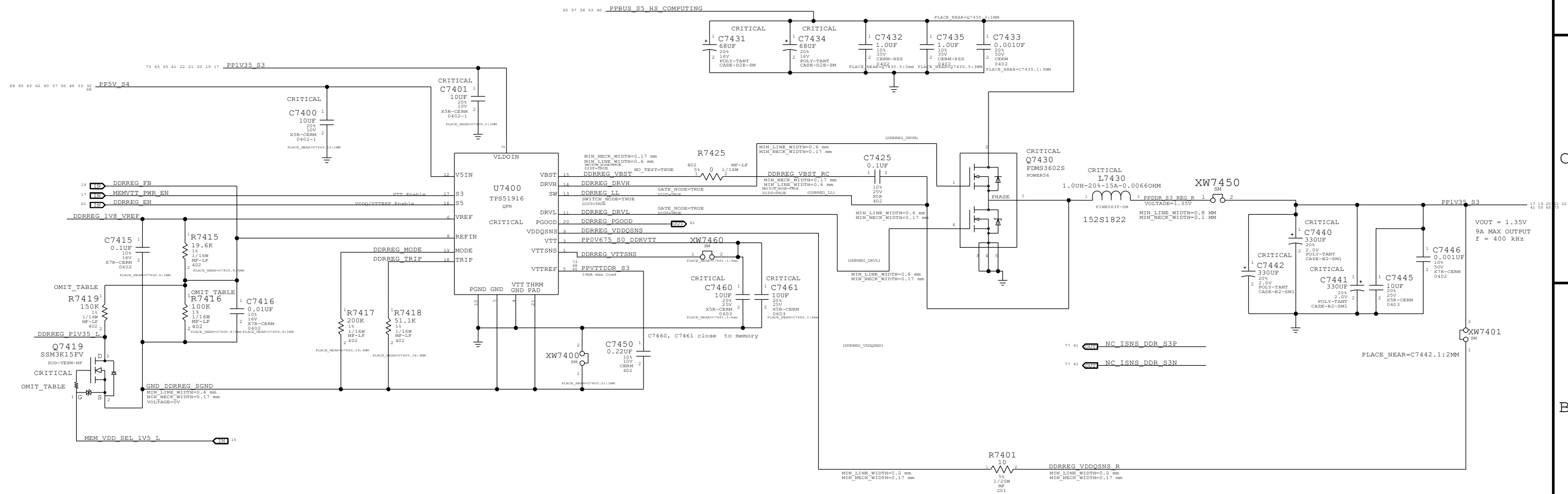


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SYNC MASTER=544 NAME=TYPE SYNC DATE=08/12/2010	
CPU VR12.6 VCC Regulator IC	
 Apple Inc.	DRAWING NUMBER <SCH NUM> D
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BRANCH <BRANCH> NAME 72 OF 120 SHEET 53 OF 78	



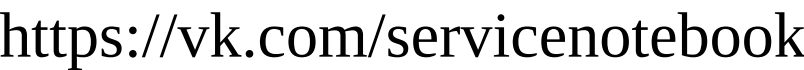
DDR3L (1V35 S3) REGULATOR

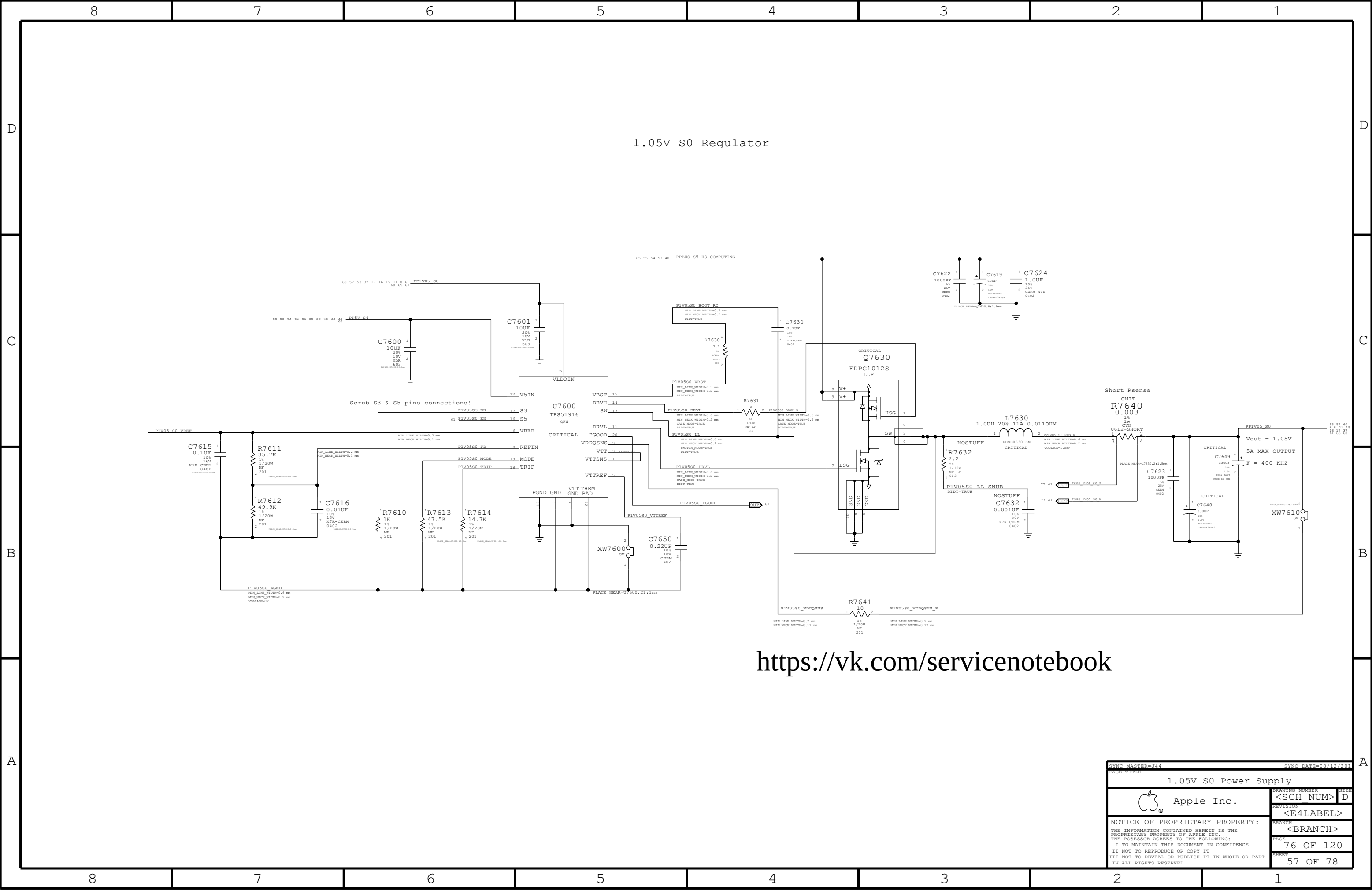


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
11480411	1	RES,MTL FILM,1/16W,100K,1,0402,SMD,LF	R7416	CRITICAL	PPDDR:1V5
11480391	1	RES,MTL FILM,1/16W,60.4K,1,0402,SMD,LF	R7416	CRITICAL	PPDDR:1V35
37680612	1	MOSFET,N-CH,30V,100MA,7.00MM,SOT-223,NS	Q7419	CRITICAL	PPDDR:1V5
11480428	1	RES, MTL FILM,1/16W,150K,0402,SMD,LF	R7419	CRITICAL	PPDDR:1V5

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PAGE TITLE		PAGE NUMBER	
1.35V DDR3 SUPPLY		5115	
Apple Inc.		<SCH NUM> D	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,HTL FLM,0 OHM,1A MAX,0402,SMD	R7720,R7721	CRITICAL	BKLT:PROD

```

KBDLED_CATHODE1 35 68
MIN_LINE_WIDTH=0.3 MM
MIN_NECF_WIDTH=0.2 MM

C001
KBDLED_CATHODE2 35 68
MIN_LINE_WIDTH=0.3 MM
MIN_NECF_WIDTH=0.2 MM

```

```

KBDLED_CATHODE2      35 60
MIN_LINE_WIDTH=0.3  001
MIN_RECT_WIDTH=0.2  001

```

2

XW7720

SW

1 PLACE NEAR=07720 X:200

371S0572
CRITICAL

RB16M-60G
PLACE, NHA=7720, 21500

PLACEMENT NOTE:

T-BONE C7726 AND C7727
 PLACE_NEAR=D7720.K:5984 PLACE_NEAR=D7720.K:5984
 SANDWICH C7723 AND C7724
 PLACE_NEAR=D7720.K:5984 PLACE_NEAR=D7720.K:5984 PLACE_NEAR=D7720.K:5984

KBD BKLT LINE WIDTHS

REF ID: A66666

```

MIN_LTRK_WIDTH=0.5 MM
MIN_NCKK_WIDTH=0.25 MM
VOLTAGE=30V
SWITCH_HOOK=TRUE      DIOT=TRUE

```

50

PPVOUT SO KBDKLT 35 58 68
MIN LINE WIDTH 0.5 MM

 Apple Inc.

58 62 68 MIN_NECK_WIDTH=0.2 MM
VOLTAGE=60V
PPVOUT BKLT FB2
MIN_LINE_WIDTH=0.4 MM 58


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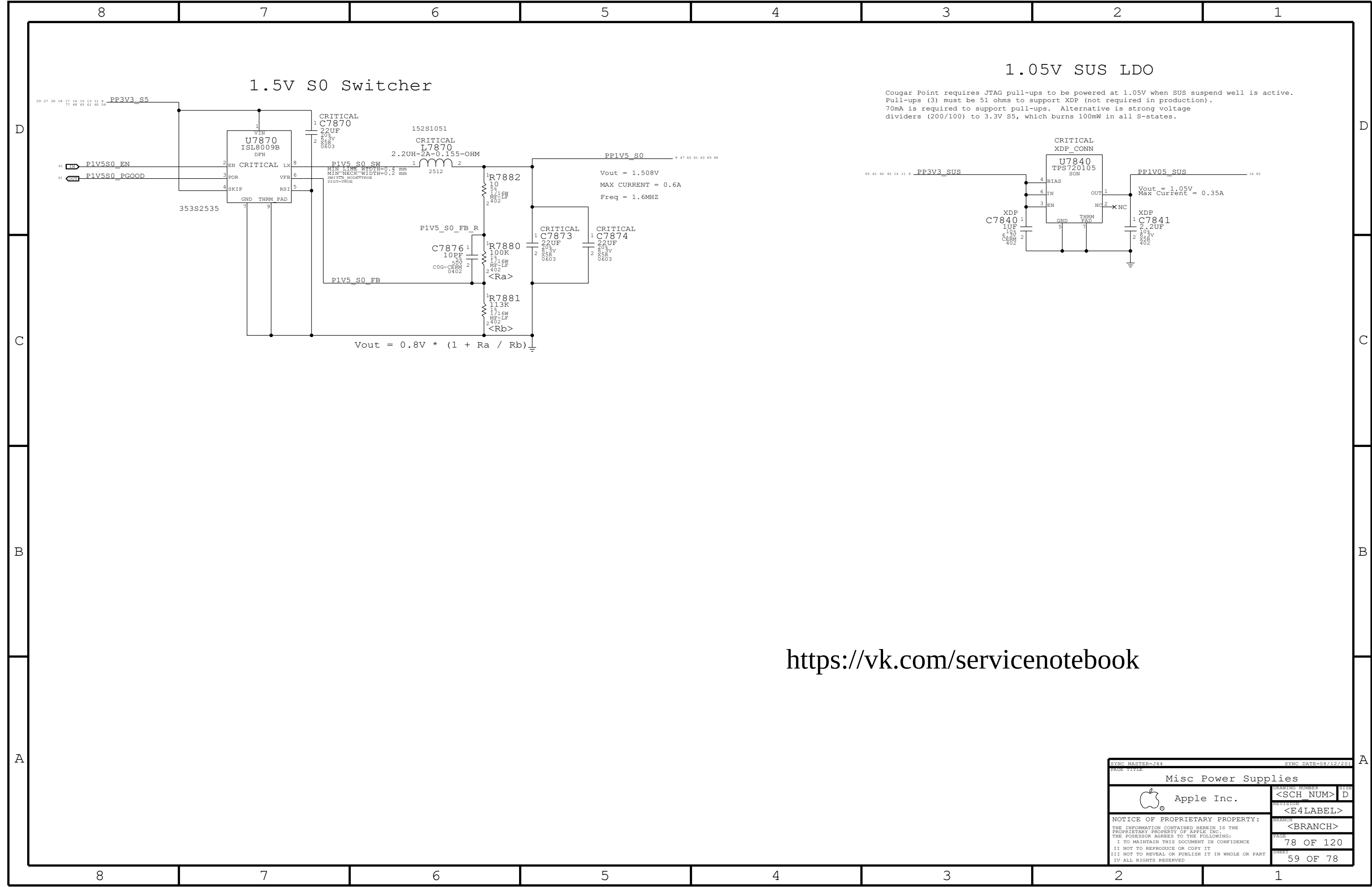
MIN Neck Width=0.25 MM
VOLTAGE=40V

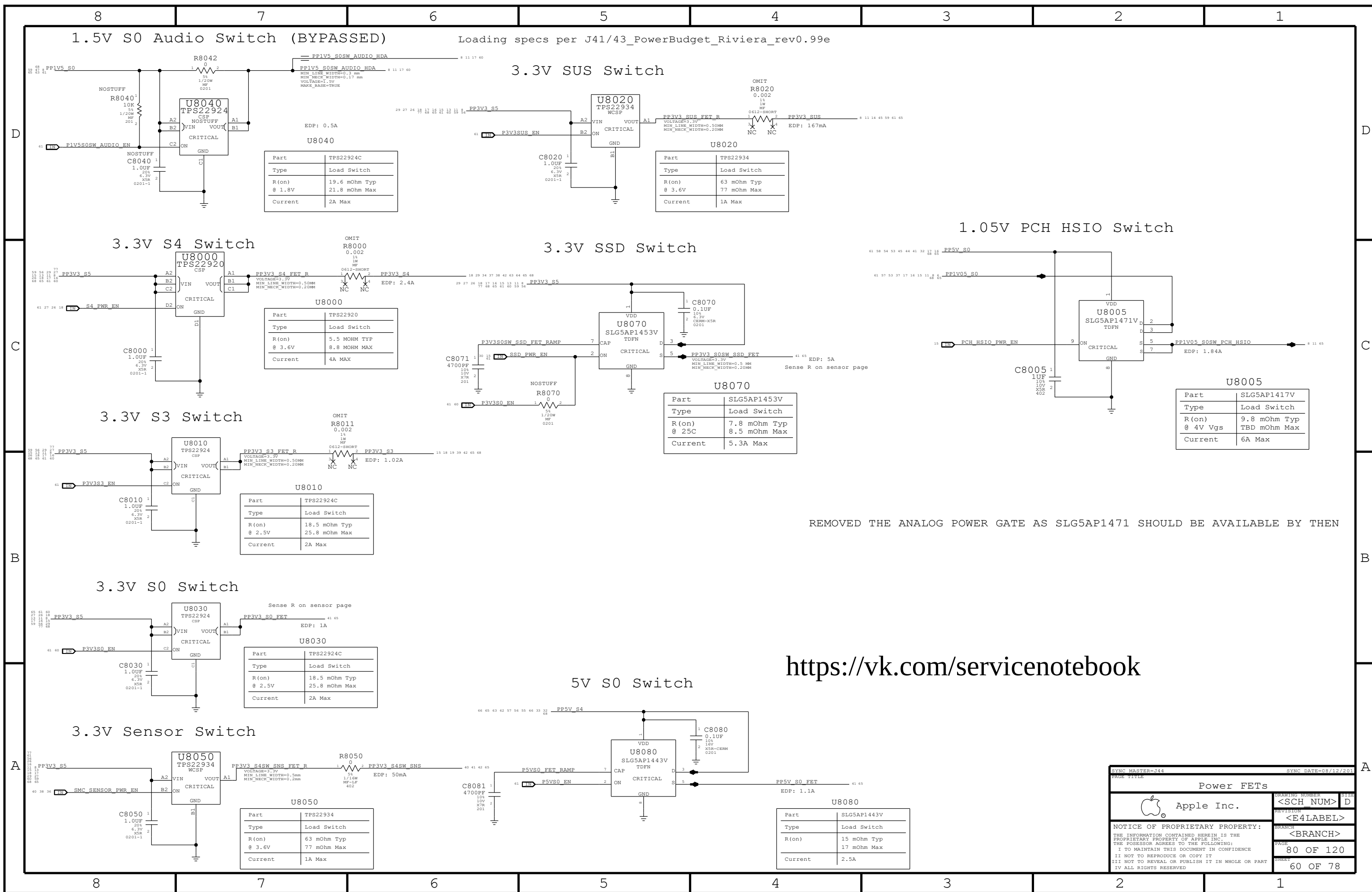
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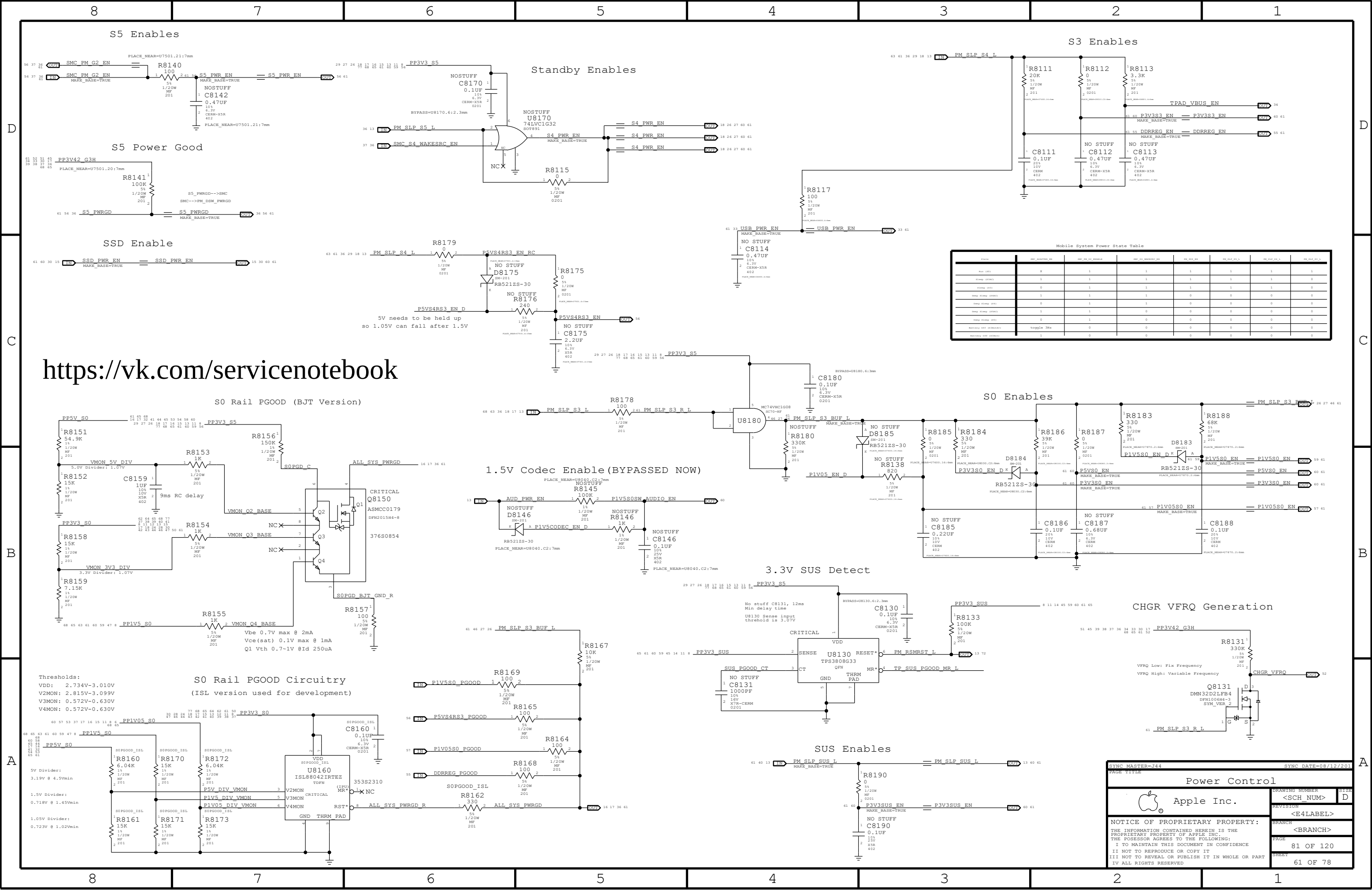
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3	2	
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JNC MASTER-344		SYMC DATE=08/12/2001	
NAME TITLE			
LCD AND KBD BKLT DRIVER			
 Apple Inc.		ORIGINATOR NUMBER	FILE
		<SCH NUM>	D
		REVISION	
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		<BRANCH>	
		PAGE	
		77	120
		SHEET	
		58	78

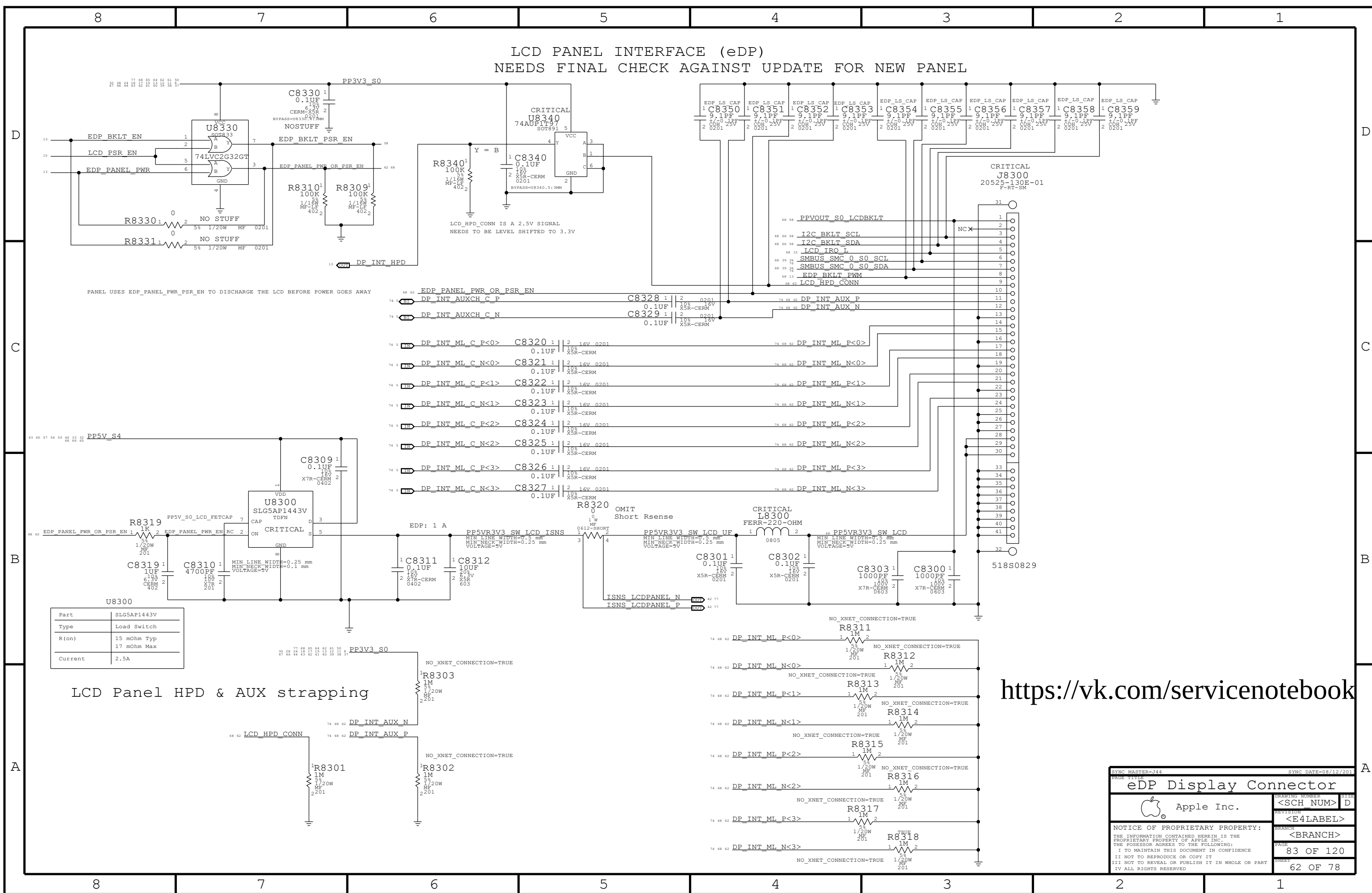


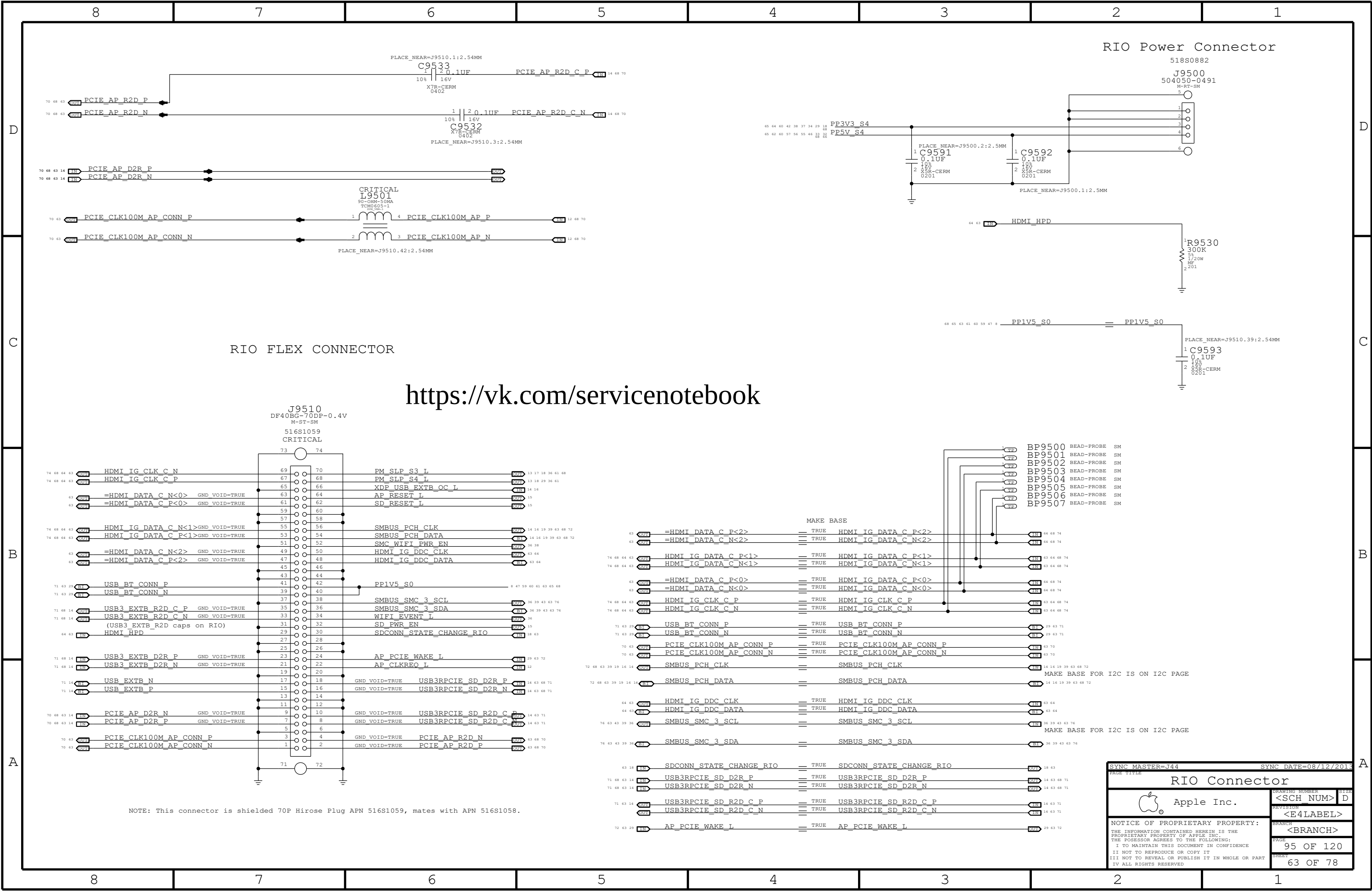




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SYNC MASTER-144		SYNC DATE-08/12/2017	
PAGE TITLE		Power Control	
	<SCH_NUM>		D
	<E4LABEL>		
	<BRANCH>		
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SYNC MASTER-344

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PAGE TITLE

RIO Connector

 Apple Inc.

REVISION

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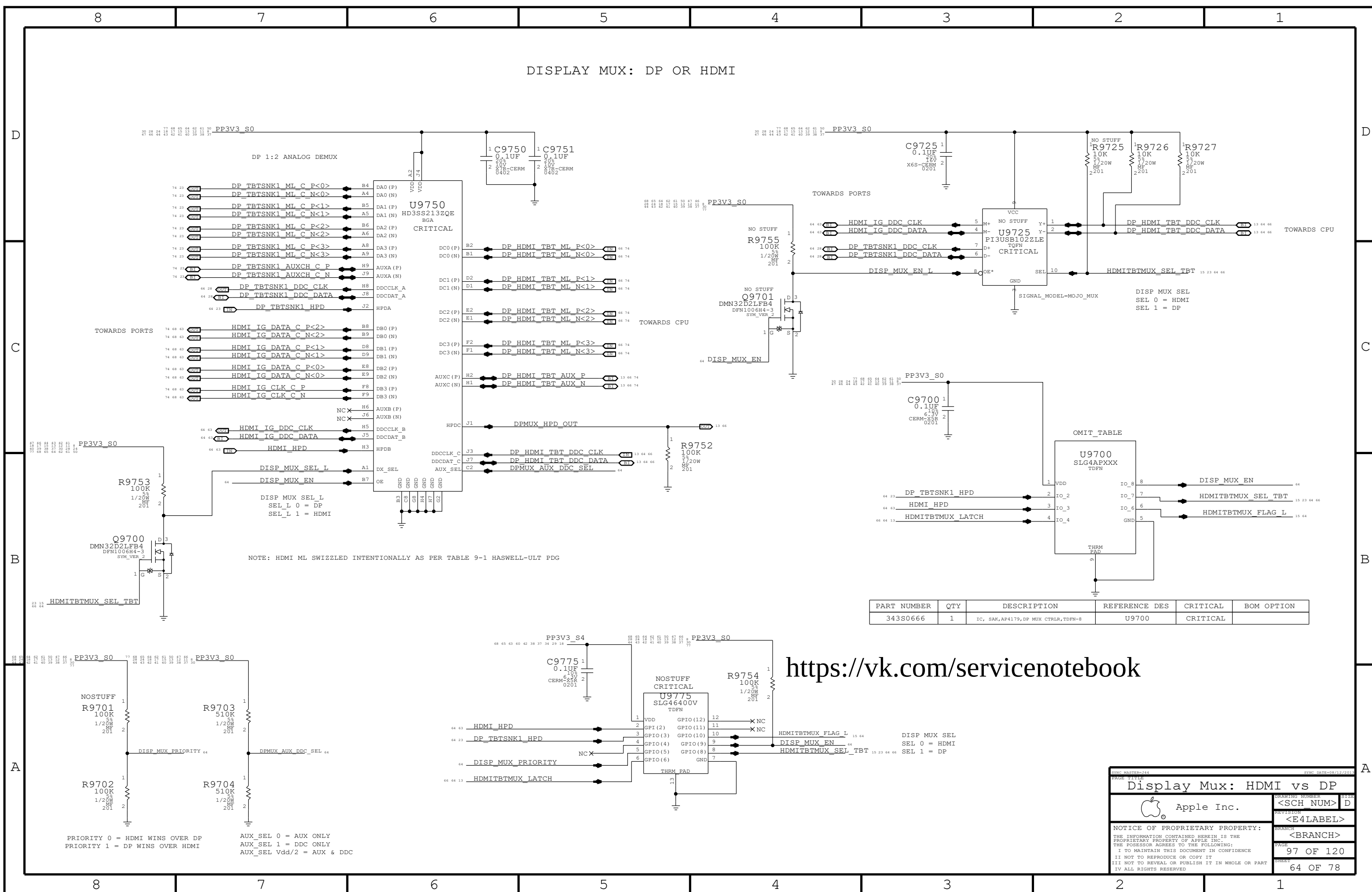
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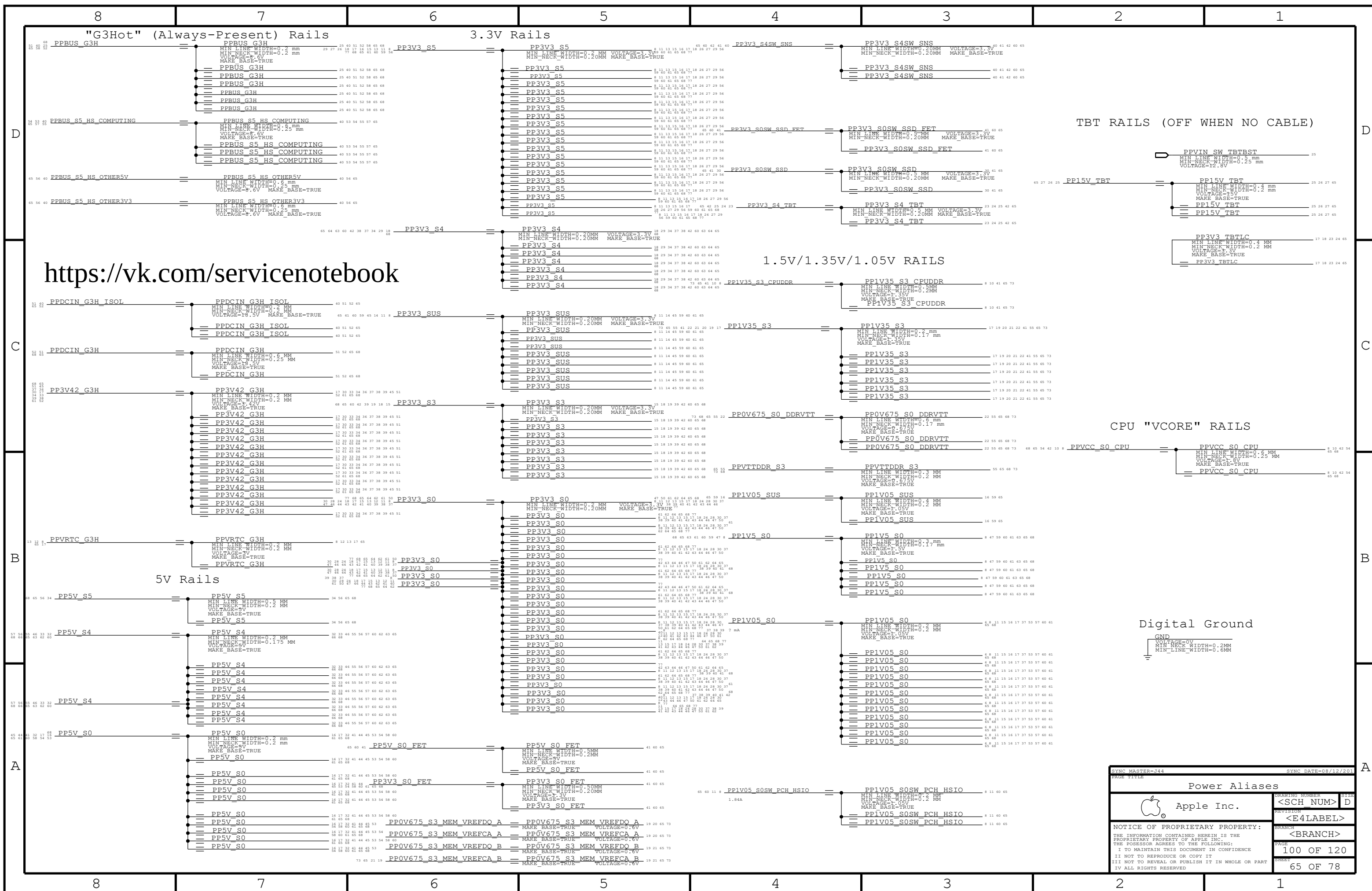
PAGE

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PAGE

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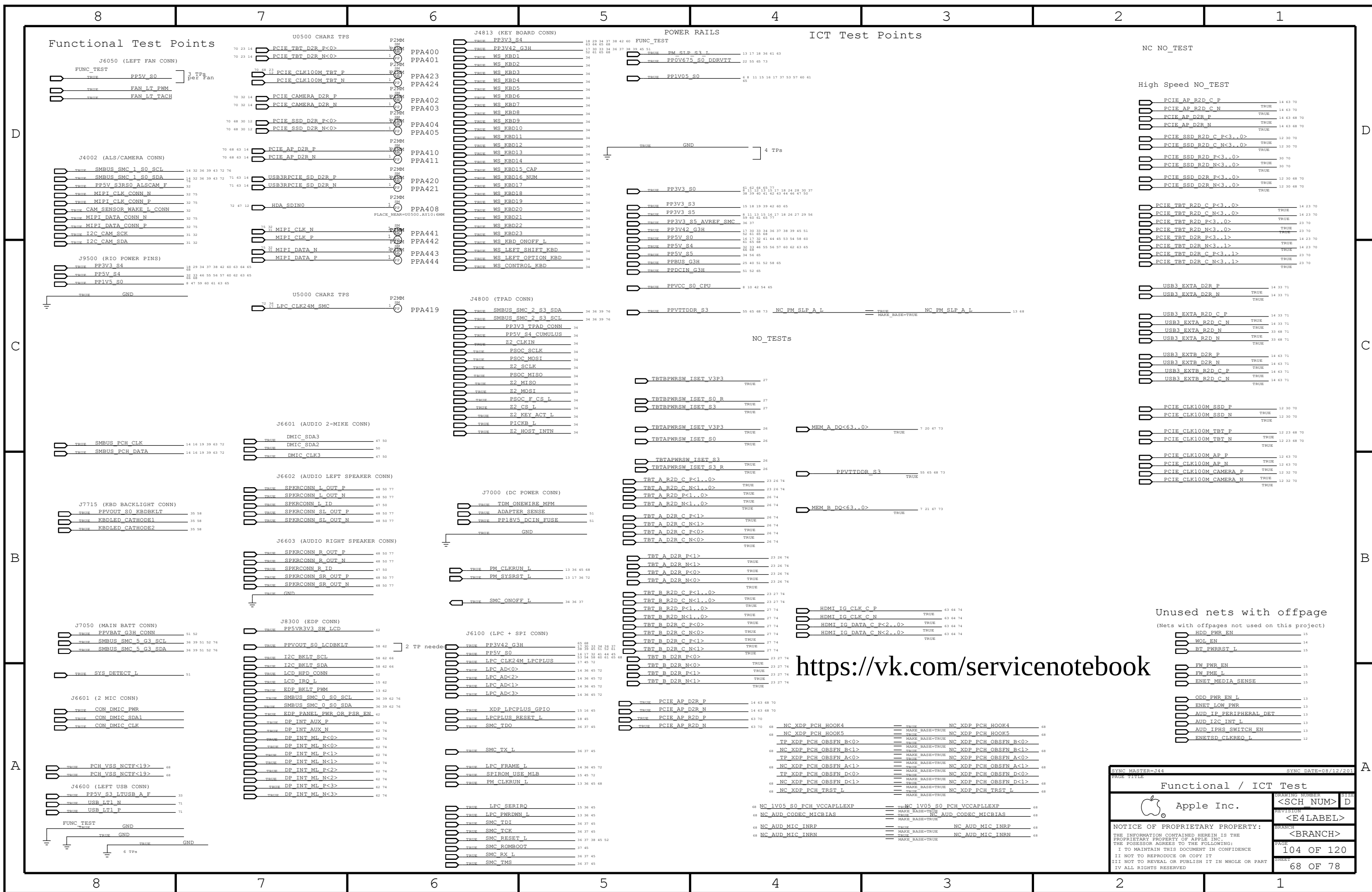




	8	7	6	5	4	3	2	1	
D	Memory Bit/Byte Swizzle								D
C									C
B									B
A									A

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PAGE TITLE			
Memory Bit/Byte Swizzle		E4LABEL	
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8		7		6		5		4		3		2		1	
J44 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS															
BOARD LAYERS				BOARD AREAS				BOARD UNITS (MIL OR MM)		ALLEGRO PRECISION					
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA, P65BGA, BGA_MEM				MM		16.5					

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?


Stackup-Defined Spacing Rules
Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	.	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1X_DIELECTRIC	TOP, BOTTOM	0.058 MM	?
1X_DIELECTRIC	ISL2, ISL4, ISL5, ISL10	0.053 MM	?
1X_DIELECTRIC	ISL2, ISL4, ISL5, ISL10, ISL11	0.101 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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SYNC MASTER-J44		SYNC DATE-08/12/2017	
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PCB Rule Definitions			
 Apple Inc.	DRAWING NUMBER		FILE
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	BRANCH		<BRANCH>
		PAGE	110 OF 120
		PAGE	69 OF 78

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27F4S	*	=27F4_OHM_SE	=27F4_OHM_SE	=27F4_OHM_SE	=27F4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE	*	25 MIL	?

PCI Express Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=3X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER
PCIE_TX	*_RX	*	PCIE_TXRX
PCIE_RX	*_TX	*	PCIE_TXRX

CPU Signal Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING
XDP_TCK0	CPU_45S	CPU_18MIL
XDP_TCK0	CPU_45S	CPU_18MIL
XDP_TCK1	CPU_45S	CPU_18MIL
XDP_TDO	CPU_45S	
XDP_TDO	CPU_45S	
XDP_TDI	CPU_45S	
XDP_TDI	CPU_45S	
XDP_TMS	CPU_45S	
XDP_TMS	CPU_45S	
XDP_TRST_I	CPU_45S	
XDP_TRST_I	CPU_45S	
XDP_PRDY_I	CPU_45S	
XDP_PRDY_I	CPU_45S	
CPU_VCCST_EWRGD	CPU_45S	CPU_08MIL
CPU_VCCST_EWRGD	CPU_45S	CPU_08MIL
CPU_BFM	CPU_45S	CPU_12MIL
CPU_BFM_PP	CPU_45S	
CPU_RCOMP_SM	CPU_27F4S	CPU_25MIL
CPU_RCOMP_RBP	CPU_27F4S	CPU_25MIL
CPU_RCOMP_OBT	CPU_27F4S	CPU_12MIL
CPU_PROCHOT	CPU_45S	CPU_08MIL
CPU_PROCHOT	CPU_45S	CPU_08MIL
CPU_CATERR	CPU_45S	CPU_08MIL
CPU_VIDALERT	CPU_45S	CPU_18MIL
CPU_VIDALERT	CPU_45S	CPU_18MIL
CPU_VIDSCIK	CPU_45S	CPU_18MIL
CPU_VIDSCIK	CPU_45S	CPU_18MIL
CPU_VIDSOUT	CPU_45S	CPU_18MIL
CPU_VIDSOUT	CPU_45S	CPU_18MIL
CPU_PECT	CPU_45S	CPU_18MIL
CPU_PECT	CPU_45S	CPU_18MIL
CPU_PECT_SMC	CPU_45S	CPU_18MIL
CPU_PECT_SMC	CPU_45S	CPU_18MIL
CPU_CFG	CPU_45S	
CPU_CFG_ED	CPU_45S	
CPU_CFG	CPU_45S	
CPU_CFG_ED	CPU_45S	
CPU_CFG_3	CPU_45S	
CPU_CFG	CPU_45S	
CPU_CFG_ED	CPU_45S	
CPU_MEM_RESET	CPU_45S	CPU_08MIL
CPU_VCCSENSE	CPU_27F4S	CPU_VCCSENSE
CPU_VCCSENSE	CPU_27F4S	CPU_VCCSENSE

PCI Express Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING
PCIE_SSD_D2R	PCIE_85D	PCIE_RX
PCIE_SSD_D2R	PCIE_85D	PCIE_RX
PCIE_SSD_D2R_BP	PCIE_85D	PCIE_RX
PCIE_SSD_D2R_BP	PCIE_85D	PCIE_RX
PCIE_SSD_R2D	PCIE_85D	PCIE_TX
PCIE_SSD_R2D	PCIE_85D	PCIE_TX
PCIE_SSD_R2D	PCIE_85D	PCIE_TX
PCIE_SSD_R2D	PCIE_85D	PCIE_TX
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX
PCIE_TBT_D2R	PCIE_85D	PCIE_RX
PCIE_TBT_D2R	PCIE_85D	PCIE_RX
PCIE_TBT_D2R	PCIE_85D	PCIE_RX
PCIE_TBT_R2D	PCIE_85D	PCIE_TX
PCIE_TBT_R2D	PCIE_85D	PCIE_TX
PCIE_TBT_R2D	PCIE_85D	PCIE_TX
PCIE_TBT_R2D	PCIE_85D	PCIE_TX
PCIE_AP_R2D	PCIE_85D	PCIE_TX
PCIE_AP_R2D	PCIE_85D	PCIE_TX
PCIE_AP_R2D	PCIE_85D	PCIE_TX
PCIE_AP_R2D	PCIE_85D	PCIE_TX
PCIE_AP_D2R	PCIE_85D	PCIE_RX
PCIE_AP_D2R	PCIE_85D	PCIE_RX
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAMERA	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAMERA	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAMERA	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAMERA	CLK_PCIE_85D	CLK_PCIE
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27F4S	*	=27F4_OHM_SE	=27F4_OHM_SE	=27F4_OHM_SE	=27F4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_08MIL	*	0.203 MM	?
CPU_12MIL	*	0.305 MM	?
CPU_18MIL	*	0.457 MM	?
CPU_25MIL	*	0.635 MM	?

PCI Express Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=3X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER
PCIE_TX	*_RX	*	PCIE_TXRX
PCIE_RX	*_TX	*	PCIE_TXRX

CPU Signal Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING
XDP_TCK0	CPU_45S	CPU_18MIL
XDP_TCK0	CPU_45S	CPU_18MIL
XDP_TCK1	CPU_45S	CPU_18MIL
XDP_TDO	CPU_45S	
XDP_TDO	CPU_45S	
XDP_TDI	CPU_45S	
XDP_TDI	CPU_45S	
XDP_TMS	CPU_45S	
XDP_TMS	CPU_45S	
XDP_TRST_I	CPU_45S	
XDP_TRST_I	CPU_45S	
XDP_PRDY_I	CPU_45S	
XDP_PRDY_I	CPU_45S	
CPU_VCCST_EWRGD	CPU_45S	CPU_08MIL
CPU_VCCST_EWRGD	CPU_45S	CPU_08MIL
CPU_BFM	CPU_45S	CPU_12MIL
CPU_BFM_PP	CPU_45S	
CPU_RCOMP_SM	CPU_27F4S	CPU_25MIL
CPU_RCOMP_RBP	CPU_27F4S	CPU_25MIL
CPU_RCOMP_OBT	CPU_27F4S	CPU_12MIL
CPU_PROCHOT	CPU_45S	CPU_08MIL
CPU_PROCHOT	CPU_45S	CPU_08MIL
CPU_CATERR	CPU_45S	CPU_08MIL
CPU_VIDALERT	CPU_45S	CPU_18MIL
CPU_VIDALERT	CPU_45S	CPU_18MIL
CPU_VIDSCIK	CPU_45S	CPU_18MIL
CPU_VIDSCIK	CPU_45S	CPU_18MIL
CPU_VIDSOUT	CPU_45S	CPU_18MIL
CPU_VIDSOUT	CPU_45S	CPU_18MIL
CPU_PECT	CPU_45S	CPU_18MIL
CPU_PECT	CPU_45S	CPU_18MIL
CPU_PECT_SMC	CPU_45S	CPU_18MIL
CPU_PECT_SMC	CPU_45S	CPU_18MIL
CPU_CFG	CPU_45S	
CPU_CFG_ED	CPU_45S	
CPU_CFG	CPU_45S	
CPU_CFG_ED	CPU_45S	
CPU_CFG_3	CPU_45S	
CPU_CFG	CPU_45S	
CPU_CFG_ED	CPU_45S	
CPU_MEM_RESET	CPU_45S	CPU_08MIL
CPU_VCCSENSE	CPU_27F4S	CPU_VCCSENSE
CPU_VCCSENSE	CPU_27F4S	CPU_VCCSENSE

PCI Express Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING
PCIE_SSD_D2R	PCIE_85D	PCIE_RX
PCIE_SSD_D2R	PCIE_85D	PCIE_RX
PCIE_SSD_D2R_BP	PCIE_85D	PCIE_RX
PCIE_SSD_D2R_BP	PCIE_85D	PCIE_RX
PCIE_SSD_R2D	PCIE_85D	PCIE_TX
PCIE_SSD_R2D	PCIE_85D	PCIE_TX
PCIE_SSD_R2D	PCIE_85D	PCIE_TX
PCIE_SSD_R2D	PCIE_85D	PCIE_TX
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX
PCIE_TBT_D2R_0	PCIE_85D	PCIE_RX
PCIE_TBT_D2R	PCIE_85D	PCIE_RX
PCIE_TBT_D2R	PCIE_85D	PCIE_RX
PCIE_TBT_D2R	PCIE_85D	PCIE_RX
PCIE_TBT_R2D	PCIE_85D	PCIE_TX
PCIE_TBT_R2D	PCIE_85D	PCIE_TX
PCIE_TBT_R2D	PCIE_85D	PCIE_TX
PCIE_TBT_R2D	PCIE_85D	PCIE_TX
PCIE_AP_R2D	PCIE_85D	PCIE_TX
PCIE_AP_R2D	PCIE_85D	PCIE_TX
PCIE_AP_R2D	PCIE_85D	PCIE_TX
PCIE_AP_R2D	PCIE_85D	PCIE_TX
PCIE_AP_D2R	PCIE_85D	PCIE_RX
PCIE_AP_D2R	PCIE_85D	PCIE_RX
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_AP	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAM	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAMERA	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAMERA	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAMERA	CLK_PCIE_85D	CLK_PCIE
PCIE_CLK100M_CAMERA	CLK_PCIE_85D	CLK_PCIE
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX
PCIE_CAMERA_D2R	PCIE_85D	PCIE_RX
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX
PCIE_CAMERA_R2D	PCIE_85D	PCIE_TX

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CPU & PCIe Constraints

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USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?

USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5X_DIELECTRIC	?

SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

USB Constraints

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
USB_RT	USB_85D	USB	USB_RT_P	14 59
USB_RT	USB_85D	USB	USB_RT_N	14 59
USB_RT	USB_85D	USB	USB_RT_CONN_P	14 59
USB_RT	USB_85D	USB	USB_RT_CONN_N	14 59
USB_EXTA	USB_85D	USB	USB_EXTA_P	14 59
USB_EXTA	USB_85D	USB	USB_EXTA_N	14 59
USB_EXTB	DEFAULT	DEFAULT	SMC_DEBUGPRT_RX_L	14 59 37
USB_EXTB	DEFAULT	DEFAULT	SMC_DEBUGPRT_TX_L	14 59 37
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_P	14 59
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_N	14 59
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_F_P	14 59
USB_EXTA	USB_85D	USB	USB2_EXTA_MUXED_F_N	14 59
USB_EXTA	USB_85D	USB	USB_LTI_P	14 59
USB_EXTA	USB_85D	USB	USB_LTI_N	14 59
USB_EXTB	USB_85D	USB	USB_EXTB_P	14 59
USB_EXTB	USB_85D	USB	USB_EXTB_N	14 59
USB_TPAD	USB_85D	USB	USB_TPAD_P	14 59
USB_TPAD	USB_85D	USB	USB_TPAD_N	14 59
USB_TPAD	USB_85D	USB	USB_TPAD_R_P	14 59
USB_TPAD	USB_85D	USB	USB_TPAD_R_N	14 59
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3_EXTA_D2R_P	14 59 08
USB3_EXTA_D2R	USB_85D	USB3_RX	USB3_EXTA_D2R_N	14 59 08
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_P	14 59 08
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_N	14 59 08
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_C_P	14 59 08
USB3_EXTA_R2D	USB_85D	USB3_TX	USB3_EXTA_R2D_C_N	14 59 08
USB3_EXTB_D2R	USB_85D	USB3_RX	USB3_EXTB_D2R_P	14 59 08
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3_EXTB_R2D_C_P	14 59 08
USB3_EXTB_R2D	USB_85D	USB3_TX	USB3_EXTB_R2D_C_N	14 59 08
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RECIE_SD_D2R_P	14 59 08
USB3_SD_D2R	USB3_85D	USB3_RX	USB3RECIE_SD_D2R_N	14 59 08
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RECIE_SD_R2D_C_P	14 59
USB3_SD_R2D	USB3_85D	USB3_TX	USB3RECIE_SD_R2D_C_N	14 59
NC	USB_85D	USB	NC_USB_IRP	14 59
NC	USB_85D	USB	NC_USB_IRN	14 59
NC	USB_85D	USB	TP_USB_5P	14 59
NC	USB_85D	USB	TP_USB_5N	14 59
NC	USB_85D	USB	NC_USB_SDP	14 59
NC	USB_85D	USB	NC_USB_SDN	14 59
NC	USB_85D	USB	NC_USB_CAMERAP	14 59
NC	USB_85D	USB	NC_USB_CAMERAN	14 59
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	14 59
	SATA_85D	SATA_RX	DUMMY SATA_D2R_P	
	SATA_85D	SATA_RX	DUMMY SATA_D2R_N	
	SATA_85D	SATA_TX	DUMMY SATA_R2D_P	
	SATA_85D	SATA_TX	DUMMY SATA_R2D_N	
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	17 59
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	17 59
SYSCLK_CLK25M	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	17 59
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	17 59
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKP	17 59
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	17 59
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_P	17 59
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	17 59
SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	17 59
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	17 59
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	17 59

Notes:
This is here to keep the SATA rules.

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USB Constraints

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_QDS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTL	*	=2x_DIELECTRIC	?
MEM_CTL2CTL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_20THERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_20THER	*	=6x_DIELECTRIC	?
MEM_CMD2CMD_RM	*	=2x_DIELECTRIC	?
MEM_CMD2CTL_RM	*	=2x_DIELECTRIC	?
MEM_CTL2CTL_RM	*	=2x_DIELECTRIC	?
MEM_12MIL	*	0.305 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_QDS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTL2CTL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_20THERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_20THER	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_CMD2CMD_RM	TOP,BOTTOM	=3x_DIELECTRIC	?
MEM_CMD2CTL_RM	TOP,BOTTOM	=3x_DIELECTRIC	?
MEM_CTL2CTL_RM	TOP,BOTTOM	=3x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE*	*	*	MEM_20THER
MEM_*_DQS*	*	*	MEM_20THER
MEM_CMD	*	*	MEM_20THER
MEM_CTL	*	*	MEM_20THER
MEM_CLK	*	*	MEM_20THER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTL	*	MEM_CMD2CTL
MEM_CTL	MEM_CTL	*	MEM_CTL2CTL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_20THERMEM
MEM_CMD	MEM_CMD	BGA_MEM	MEM_CMD2CMD_RM
MEM_CMD	MEM_CTL	BGA_MEM	MEM_CMD2CTL_RM
MEM_CTL	MEM_CTL	BGA_MEM	MEM_CTL2CTL_RM

Haswell ULT Memory Down DDR3L 1x8 Length Matching

DDR3 Signal Group	Unit	Min Length	Max Length
CTLmax - CTLmin	mils	0	100
CTL to CLK	mils	CLK - 500	CLK + 500
CMD1 to CMDj	mils	CMDj - 100	CMDj + 100
CMD to CLK	mils	CLK - 500	CLK + 500
(DQmax - DQmin) per byte	mils	0	250
(DQS - DQmax) per byte	mils	-100	150
DQS to DQS#	mils	-5	5
DQS to CLK (Rule 1)	mils	CLK - 6500	CLK + 500
Max (CLK-DQS) - Min (CLK-DQS)	mils	0	5500
CLK to CLK#	mils	-5	5

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<0>	7 20 22
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<0>	7 20 22
MEM_A_CTL	MEM_40S	MEM_CTL	MEM_A_CKR<0>	7 20 22
MEM_A_CTL	MEM_40S	MEM_CTL	MEM_A_CS_L<0>	7 20 22
MEM_A_ODT0	MEM_40S	MEM_CTL	MEM_A_ODT<0>	20 22
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RA<3..1>	7 20 22 66
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	7 20 22 66
MEM_A_DQBYTE0	MEM_45S	MEM_A_DQBYTE_0	MEM_A_WE_L	7 20 22 66
MEM_A_DQBYTE1	MEM_45S	MEM_A_DQBYTE_1	MEM_A_DO<7..0>	7 47 66
MEM_A_DQBYTE2	MEM_45S	MEM_A_DQBYTE_2	MEM_A_DO<13..8>	7 47 66
MEM_A_DQBYTE3	MEM_45S	MEM_A_DQBYTE_3	MEM_A_DO<23..16>	7 47 66
MEM_A_DQBYTE4	MEM_45S	MEM_A_DQBYTE_4	MEM_A_DO<31..24>	7 47 66
MEM_A_DQBYTE5	MEM_45S	MEM_A_DQBYTE_5	MEM_A_DO<39..32>	7 20 47 66
MEM_A_DQBYTE6	MEM_45S	MEM_A_DQBYTE_6	MEM_A_DO<47..40>	7 47 66
MEM_A_DQBYTE7	MEM_45S	MEM_A_DQBYTE_7	MEM_A_DO<55..48>	7 47 66
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DO<63..56>	7 47 66
MEM_A_DQS0	MEM_80D	MEM_A_DQS_0	MEM_A_DQS_P<0>	7 47
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_N<0>	7 47
MEM_A_DQS1	MEM_80D	MEM_A_DQS_1	MEM_A_DQS_P<1>	7 47
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_N<1>	7 47
MEM_A_DQS2	MEM_80D	MEM_A_DQS_2	MEM_A_DQS_P<2>	7 47
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_N<2>	7 47
MEM_A_DQS3	MEM_80D	MEM_A_DQS_3	MEM_A_DQS_P<3>	7 47
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_N<3>	7 47
MEM_A_DQS4	MEM_80D	MEM_A_DQS_4	MEM_A_DQS_P<4>	7 47
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_N<4>	7 47
MEM_A_DQS5	MEM_80D	MEM_A_DQS_5	MEM_A_DQS_P<5>	7 47
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_N<5>	7 47
MEM_A_DQS6	MEM_80D	MEM_A_DQS_6	MEM_A_DQS_P<6>	7 20 47
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_N<6>	7 47
MEM_A_DQS7	MEM_80D	MEM_A_DQS_7	MEM_A_DQS_P<7>	7 47
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<0>	7 20 22
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<0>	7 20 22
MEM_B_CTL	MEM_40S	MEM_CTL	MEM_B_CKR<0>	7 20 22
MEM_B_CTL	MEM_40S	MEM_CTL	MEM_B_CS_L<0>	7 20 22
MEM_B_ODT0	MEM_40S	MEM_CTL	MEM_B_ODT<0>	20 22
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	7 20 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	7 20 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RA<3..1>	7 20 22 66
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	7 20 22 66
MEM_B_DQBYTE0	MEM_45S	MEM_B_DQBYTE_0	MEM_B_WE_L	7 20 22 66
MEM_B_DQBYTE1	MEM_45S	MEM_B_DQBYTE_1	MEM_B_DO<7..0>	7 47 66
MEM_B_DQBYTE2	MEM_45S	MEM_B_DQBYTE_2	MEM_B_DO<13..8>	7 47 66
MEM_B_DQBYTE3	MEM_45S	MEM_B_DQBYTE_3	MEM_B_DO<23..16>	7 47 66
MEM_B_DQBYTE4	MEM_45S	MEM_B_DQBYTE_4	MEM_B_DO<31..24>	7 47 66
MEM_B_DQBYTE5	MEM_45S	MEM_B_DQBYTE_5	MEM_B_DO<39..32>	7 20 47 66
MEM_B_DQBYTE6	MEM_45S	MEM_B_DQBYTE_6	MEM_B_DO<47..40>	7 47 66
MEM_B_DQBYTE7	MEM_45S	MEM_B_DQBYTE_7	MEM_B_DO<55..48>	7 47 66
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DO<63..56>	7 47 66
MEM_B_DQS0	MEM_80D	MEM_B_DQS_0	MEM_B_DQS_P<0>	7 47
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_N<0>	7 47
MEM_B_DQS1	MEM_80D	MEM_B_DQS_1	MEM_B_DQS_P<1>	7 47
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_N<1>	7 47
MEM_B_DQS2	MEM_80D	MEM_B_DQS_2	MEM_B_DQS_P<2>	7 47
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_N<2>	7 47
MEM_B_DQS3	MEM_80D	MEM_B_DQS_3	MEM_B_DQS_P<3>	7 47
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_N<3>	7 47
MEM_B_DQS4	MEM_80D	MEM_B_DQS_4	MEM_B_DQS_P<4>	7 47
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_N<4>	7 47
MEM_B_DQS5	MEM_80D	MEM_B_DQS_5	MEM_B_DQS_P<5>	7 47
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_N<5>	7 47
MEM_B_DQS6	MEM_80D	MEM_B_DQS_6	MEM_B_DQS_P<6>	7 20 47
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_N<6>	7 47
MEM_B_DQS7	MEM_80D	MEM_B_DQS_7	MEM_B_DQS_P<7>	7 47
	MEM_PWR		PE1V35_S3	17 19 20 21 22 41 55 65
	MEM_PWR		PE1V35_S3_CPUDDR	8 12 41 43
	MEM_PWR		PE1V675_S3_DDRVTT	20 41 43 66
	MEM_PWR		PE1VTTDDR_S3	44 45 66
	MEM_12MIL		CPU DIMMA_VREFDQ	7 19
	MEM_12MIL		CPU DIMMA_VREFDQ_A_ISOL	19
	MEM_12MIL		CPU DIMMA_VREFDQ	7 19
	MEM_12MIL		CPU DIMMB_VREFDQ_B_ISOL	19
	MEM_12MIL		CPU DIMM_VREFCA	7 19
	MEM_12MIL		CPU DIMM_VREFCA_A_ISOL	19
	MEM_12MIL		CPU DIMM_VREFCA_B_ISOL	19
	MEM_12MIL		PP0V675_S3_MEM_VREFDQ_A	19 20 65
	MEM_12MIL		PP0V675_S3_MEM_VREFDQ_B	19 20 65
	MEM_12MIL		PP0V675_S3_MEM_VREFCA_A	19 20 65
	MEM_12MIL		PP0V675_S3_MEM_VREFCA_B	19 20 65

Memory Constraints

SYNCH MASTER-144

SYNCH DATE-01/03/2011

NAME TITLE

Memory Constraints

REVISED

DATE

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2X_DIELECTRIC	?
S2_DQ82OWNDATA	*	=2X_DIELECTRIC	?
S2_CMD2CMD	*	=2X_DIELECTRIC	?
S2_CMD2CTRL	*	=2X_DIELECTRIC	?
S2_CTRL2CTRL	*	=2X_DIELECTRIC	?
S2_2OTHERMEM	*	=4X_DIELECTRIC	?
S2MEM_2PWR	*	=2X_DIELECTRIC	?
S2MEM_2GND	*	=2X_DIELECTRIC	?
S2MEM_2OTHER	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_DQ82OWNDATA	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6X_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4X_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4X_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM*	S2_MEM*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQ82OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQ82OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONST SET	NET TYPE			
	PHYSICAL	SPACING		
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P	31 32
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N	31 32
S2_MEM_CKE	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE	31 32
S2_MEM_CS	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT	32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_BAS_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BAC0>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BAC1>	31 32
S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BAC2>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>	31 32
S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>	31 32
S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>	31 32
S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>	31 32
S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>	31 32
S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>	31 32
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P	31 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N	31 32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P	32 68
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N	32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P	31 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N	31 32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P	32 68
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N	32 68
		S2_MEM_PWR	PPIV35_CAM	31 32
		S2_MEM_PWR	PFOV675_CAM_VREF	31 32
		S2_MEM_PWR	PFOV675_MEM_CAM_VREFCA	32
		S2_MEM_PWR	PFOV675_MEM_CAM_VREFDO	32

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SMC SMBus & Charger Net Properties									
ELECTRICAL CONST SET		NET TYPE							
		PHYSICAL	SPACING						
<div></div>	smbus_smc_2	smc_45R	smc	SMBUS_SMC_2_S3_SCL	34	36	38	40	
<div></div>	SMBUS_SMC_2	smc_45R	smc	SMBUS_SMC_2_S3_SDA	34	38	39	40	
<div></div>	SMBUS_SMC_1	smc_45R	smc	SMBUS_SMC_1_S0_SCL	14	30	34	39	43
<div></div>	SMBUS_SMC_1	smc_45R	smc	SMBUS_SMC_1_S0_SDA	14	30	34	39	43
<div></div>	SMBUS_SMC_0	smc_45R	smc	SMBUS_SMC_0_S0_SCL	30	39	42	46	
<div></div>	SMBUS_SMC_0	smc_45R	smc	SMBUS_SMC_0_S0_SDA	30	39	42	46	
<div></div>	SMBUS_SMC_5	smc_45R	smc	SMBUS_SMC_5_G3_SCL	30	39	43	44	46
<div></div>	SMBUS_SMC_5	smc_45R	smc	SMBUS_SMC_5_G3_SDA	30	39	43	44	46
<div></div>	SMBUS_SMC_3	smc_45R	smc	SMBUS_SMC_3_SCL	30	39	43	44	
<div></div>	SMBUS_SMC_3	smc_45R	smc	SMBUS_SMC_3_SDA	30	39	43	44	

8		7			6		
PHYSICAL_NDLE_SE	LAYER	ALLOW ROUTE ON LAYERS	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFRAIR PRIMARY GAP	DIFFRAIR NECK GAP
SENSE_45S	*	=101_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
THERM_45S	*	=101_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
DIG_AUDIO	*		=101_DIFFPAIR	=101_DIFFPAIR	=101_DIFFPAIR	0.1 MM	0.1 MM
ANL_AUDIO	*	=101_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
ANL_AUDIO_WIDE	*	=101_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X DIELECTRIC	?
THERM	*	=2X DIELECTRIC	?
AUDIO	*	=2X DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	=STANDARD	?	CLK PCIE	GND	*	GND P2MM
				GND	PCIE *	*	GND P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE *	*	GND_P2MM

GND	SATA *	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA *	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFRACTION PRIMARY GAP	DIFFRACTION NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.070 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.100 MM	500 MIL		
CPU_27P4S	BOTTOM			0.230 MM	100 MIL		
USB3_85D	TOP			0.100 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DDR3 Loaded Segment Constraint Relaxations

Alternate single ended and differential impedances between devices.

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_40S	BGA MEM	MEM_45S
MEM_72D	BGA MEM	MEM_85D

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.100 MM	6.35 MM		

DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	P65_BGA
PCIE_85D	BGA	P65_BGA
CLK_PCIE_85D	BGA	P65_BGA
HDMI_85D	BGA	P65_BGA


NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SENSE_45S	*	SENSE_45S
THERM_45S	*	THERM_45S
DIG_AUDIO	*	DIG_AUDIO
ANL_AUDIO	*	ANL_AUDIO
1T01_DIFFPAIR	*	1T01_DIFFPAIR


J44 Specific Net Properties

ELECTRICAL CONST SET		NET TYPE		
		PHYSICAL	SPACING	
	THERM_DP_TBT_D1	THERM_45G	THERM	TBTTHMSNS D1 P
0000	THERM_DP_TBT_D1	THERM_45G	THERM	TBTTHMSNS D1 N
	THERM_DP_CEU_D1	THERM_45G	THERM	CPUTHMSNS D1 P
	THERM_DP_CEU_D1	THERM_45G	THERM	CPUTHMSNS D1 N
0000	THERM_DP_CEU_D2	THERM_45G	THERM	CPUTHMSNS D2 P
	THERM_DP_CEU_D2	THERM_45G	THERM	CPUTHMSNS D2 N
0000		SENSE_45G	SENSE	NC ISNS CAMERAP
	SENSE_DP	SENSE_45G	SENSE	NC ISNS CAMERAN
	SENSE_DP	SENSE_45G	SENSE	ISNS_CPUDDR P
	SENSE_DP	SENSE_45G	SENSE	ISNS_CPUDDR N
00000000	SENSE_DP_LCDBKLT	SENSE_45G	SENSE	ISNS LCDBKLT P
	SENSE_DP_LCDBKLT	SENSE_45G	SENSE	ISNS LCDBKLT N
	SENSE_DP_TBT	SENSE_45G	SENSE	ISNS TBT P
00000000	SENSE_DP_TBT	SENSE_45G	SENSE	ISNS TBT_N
	SENSE_DP	SENSE_45G	SENSE	ISNS_LCDBANEL_P
	SENSE_DP	SENSE_45G	SENSE	ISNS_LCDBANEL_N
0000	SENSE_DP	SENSE_45G	SENSE	ISNS_HS_COMPUTING P
	SENSE_DP	SENSE_45G	SENSE	ISNS_HS_COMPUTING N
00000000	SENSE_DP	SENSE_45G	SENSE	ISNS_HS_OTHERSV P
	SENSE_DP	SENSE_45G	SENSE	ISNS_HS_OTHERSV_N
	SENSE_DP	SENSE_45G	SENSE	ISNS_HS_OTHERSV3 P
00000000	SENSE_DP	SENSE_45G	SENSE	ISNS_HS_OTHERSV3_N
	SENSE_DP_CPUIVR	SENSE_45G	SENSE	CPUIVR ISNS P
	SENSE_DP_CPUIVR	SENSE_45G	SENSE	CPUIVR ISNS_N
00000000	SENSE_DP_CPUIVR	SENSE_45G	SENSE	CPUIVR ISNS_R P
	SENSE_DP_CPUIVR	SENSE_45G	SENSE	CPUIVR ISNS_R N
00000000		SENSE_45G	SENSE	CPUIVR ISNS1 P
		SENSE_45G	SENSE	CPUIVR ISNS1_N
		SENSE_45G	SENSE	CPUIVR ISNS2 P
00000000		SENSE_45G	SENSE	CPUIVR ISNS2_N
	SENSE_DP	SENSE_45G	SENSE	ISNS_IV05_S0 P
00000000	SENSE_DP	SENSE_45G	SENSE	ISNS_IV05_S0_N
	SENSE_DP	SENSE_45G	SENSE	ISNS_SSD P
	SENSE_DP	SENSE_45G	SENSE	ISNS_SSD_N
00000000	SENSE_DP	SENSE_45G	SENSE	ISNS_TP4D P
	SENSE_DP	SENSE_45G	SENSE	ISNS_TP4D_N
0000		SENSE_45G	SENSE	NC ISNS_DDR_S3P
	SENSE_DP	SENSE_45G	SENSE	NC ISNS_DDR_S3N
	SENSE_DP	SENSE_45G	SENSE	ISNS_PP3V3S0 P
	SENSE_DP	SENSE_45G	SENSE	ISNS_PP3V3S0_N
00000000	SENSE_DP	SENSE_45G	SENSE	ISNS_PP5V0 P
	SENSE_DP	SENSE_45G	SENSE	ISNS_PP5V0_N
0000	SENSE_DP_CPHUGAIN	SENSE_45G	SENSE	ISNS_CPHUGAIN P
	SENSE_DP_CPHUGAIN	SENSE_45G	SENSE	ISNS_CPHUGAIN_N
00000000	SENSE_DP_CPHUGAIN	SENSE_45G	SENSE	ISNS_CPHUGAIN_R P
	SENSE_DP_CPHUGAIN	SENSE_45G	SENSE	ISNS_CPHUGAIN_R_N
00000000	SENSE_DP_CHGR_CS1	SENSE_45G	SENSE	CHGR_CS1 P
	SENSE_DP_CHGR_CS1	SENSE_45G	SENSE	CHGR_CS1_N
00000000	SENSE_DP_CHGR_CS1	SENSE_45G	SENSE	CHGR_CS1_R P
	SENSE_DP_CHGR_CS1	SENSE_45G	SENSE	CHGR_CS1_R_N
	SENSE_DP_CHGR_C50	SENSE_45G	SENSE	CHGR_C50 P
00000000	SENSE_DP_CHGR_C50	SENSE_45G	SENSE	CHGR_C50_N
	SENSE_DP_CHGR_C50	SENSE_45G	SENSE	CHGR_C50_R P
	SENSE_DP_CHGR_C50	SENSE_45G	SENSE	CHGR_C50_R_N

J44 Specific Net Properties

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