

Compal LA-L973P

HH514(50) MB Schematic Document

Rev : 1.0

2021.10.26

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Int. DMIC

- On CCD Module

Int. Speaker

- ON M/B > L
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Audio Jack

- On IO/B

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Vcc	3.3V +/- 5%	EC Board ID Table for AD channel				
Ra	100K +/- 1%					
Board ID	Rb	Vmin	Vtyp	Vmax	EC AD	
0	0		0.000 V	0.300 V	0x00 - 0x13	
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76	
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87	
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96	
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4	
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF	
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7	
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF	
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9	
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4	
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD	
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0	
19	NC	3.000 V	3.000 V		0xF1 - 0xFF	

	*PCB Version
	*Key board type
Board ID	PCB Revision
0	50 Rev0.1
1	50 Rev0.2
2	50 Rev1.0
3	
4	50 Rev0.1+RGB
5	50 Rev0.2+RGB
6	50 Rev1.0+RGB
7	
8	60 Rev0.1
9	60 Rev0.2
10	60 Rev1.0
11	
12	60 Rev0.1+RGB
13	60 Rev0.2+RGB
14	60 Rev1.0+RGB
15	
16	
17	
18	
19	

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_1	TM-P3393-003 (Touch Pad)			
SOC_SMBCLK	DIMM1	0xA0	0xA1	0xA0
	DIMM2	0xA3	0xA4	0xA3
EC_CK/DA (Port0)	BQ24800 (Charger IC)	0x12	0001_0010	
(+3VLP)	BATTERY PACK	0x16		
EC_CK/DA (Port1)	TGL-U / PCH LP	TBD		
(+3VS)	GN20 E3/E5/E7 (VGA)	0x9E		
SOC_SML1CK/DA	Thermal Sensor (NCT7718W)	0x98	1001_1001b	1001_1000b
(+3VALW)	Thermal Sensor (G781)	0x9A	1001_1011b	1001_1010b
EC_CK/DA (Port2)	LED Driver (59116F)	0xC0		
	eDP Mux(P58461E)	0x10-0x2F		
	LightBar	0x5B		
EC_CK/DA (Port3)	Realtek RTS5452E	0x62		0100_0110b
EC_CK/DA (Port5)	KC3810	TBD		

PCB Version *Key board type			
43 Level	Description	BOM Structure	
431AU8BOL01	HH514 N18P QXZR BRL	QXZR8/N18P61A8/N18P48/EVTGR8/LB8/LED14P8/LOGOBL8/PERKEY8/X76SAM8/X76UP1GEN18/PCB8/GLITCH8/CMC8/SLC8555448/CHG8/HDD8/TMS8/EDP8/DP8/GN20P8/DDR48/KC38108/CNV18/DEBUC8/12VFAN8/TypeC8/FP8/VGA8/OVRM8/GEN28/X4E8/20128/PB8/DR8/COST8	
431AU8BOL02	HH514 N18P QXZR B3L	QXZR8/N18P61A8/N18P48/EVTGR8/LB8/LED14P8/LOGOBL8/PERKEY8/X76HYN8/X76UP1GEN18/PCB8/GLITCH8/CMC8/SLC8555448/CHG8/HDD8/TMS8/EDP8/DP8/GN20P8/DDR48/KC38108/CNV18/DEBUC8/12VFAN8/TypeC8/FP8/VGA8/OVRM8/GEN28/X4E8/20128/PB8/DR8/COST8	
431AU8BOL03	HH514 N20P QXQZ BRL	QYQZ8/GN20P08/N20P8/EVT18/LB8/LED14P8/LOGOBL8/PERKEY8/X76SAM8/X76UP1GEN28/PCB8/GLITCH8/CMC8/SLC8555448/CHG8/HDD8/TMS8/EDP8/DP8/GN20P8/DDR48/KC38108/CNV18/DEBUC8/12VFAN8/TypeC8/FP8/VGA8/OVRM8/GEN28/X4E8/20128/PB8/DR8/COST8	
431AU8BOL04	HH514 N20P QXQZ B3L	QYQZ8/GN20P08/N20P8/EVT18/LB8/LED14P8/LOGOBL8/PERKEY8/X76HYN8/X76UP1GEN28/PCB8/GLITCH8/CMC8/SLC8555448/CHG8/HDD8/TMS8/EDP8/DP8/GN20P8/DDR48/KC38108/CNV18/DEBUC8/12VFAN8/TypeC8/FP8/VGA8/OVRM8/GEN28/X4E8/20128/PB8/DR8/COST8	
431AU8BOL05	HH514 N20P1 QXZH BRL	QXZH8/GN20P18/N20P8/EVT18/LB8/LED14P8/LOGOBL8/PERKEY8/X76SAM8/X76UP1GEN28/PCB8/GLITCH8/CMC8/SLC8555448/CHG8/HDD8/TMS8/EDP8/DP8/GN20P8/DDR48/KC38108/CNV18/DEBUC8/12VFAN8/TypeC8/FP8/VGA8/OVRM8/GEN28/X4E8/20128/PB8/DR8/COST8	
431AU8BOL06	HH514 N20P1 QXZH B3L	QXZH8/GN20P18/N20P8/EVT18/LB8/LED14P8/LOGOBL8/PERKEY8/X76HYN8/X76UP1GEN28/PCB8/GLITCH8/CMC8/SLC8555448/CHG8/HDD8/TMS8/EDP8/DP8/GN20P8/DDR48/KC38108/CNV18/DEBUC8/12VFAN8/TypeC8/FP8/VGA8/OVRM8/GEN28/X4E8/20128/PB8/DR8/COST8	
431AU8BOL07	HH514 PWR N-CHIP	N20P8/EVT18/LB8/LED14P8/LOGOBL8/PERKEY8/X76UP1GEN28/PCB8/GLITCH8/CMC8/SLC8555448/CHG8/HDD8/TMS8/EDP8/DP8/GN20P8/DDR48/KC38108/CNV18/DEBUC8/12VFAN8/TypeC8/FP8/VGA8/OVRM8/GEN28/X4E8/20128/PB8/DR8/COST8	

V : Must		V : Options	
Item (X43 / X76)	BOM Structure	Item (X43 / X76)	BOM Structure
Unpop	@	eDP W/O retimer	EDP@ V
Connector	CONN@	eDP retimer	EDPRT@
PCB	PCB@ V	mDP	DP@ V
CPU ADL-P		Intel CNVi	CNVi@ V
FJ8071504587820 QXZH	QXZH@ V	FOR UART debug	UART@
FJ8071504587817 QXZR	QXZR@ V	FOR EVT EC debug	DEBUG@ V
FJ8071504587821 QY0Z	QY0Z@ V	Finger Print	FP@ V
		PERKEY	PERKEY@ V
		Thermal sensor	TMS@ V
		GLITCH	GLITCH@ V
		XDP	CMC@ V
N18P-G61-A-A1 GPU	N18PG61A@ V	Vpro function	VPRO@
dGPU circuit	VGA@ V	TypeC Port	TypeC@ V
N18PG-61-A GPU&Part	N18PA@ V	HDD	HDD@ V
GN20 Part	N20P@ V	USB Changer	CHG@ V
GN20P0 GPU	GN20P0@ V	USB Changer(SLG)	SLGC55544@ V
GN20P1 GPU	GN20P1@ V	USB Changer(CW)	CW3046@ V
GPU OVRM	OVRM@ V	KC3810	KC3810@ V
GPU OVRM Gen1	GEN1@ V	12V FAN	12VFAN@ V
GPU OVRM Gen2	GEN2@ V		
PROJECT ID(DDR4/DDR5)	DDR4@ V	EC Board ID	
PROJECT ID(50/60)	GN20P@ V	50 Rev0.1	EVT@
XTAL package	2012@ V	50 Rev0.1+ RGB	EVTRGB@
XTAL package	3215@		


Item Backlight	BOM Structure
KB LED driver	LED14P@
LOGO backlight	LOGOBL@
Lightbar	LB@

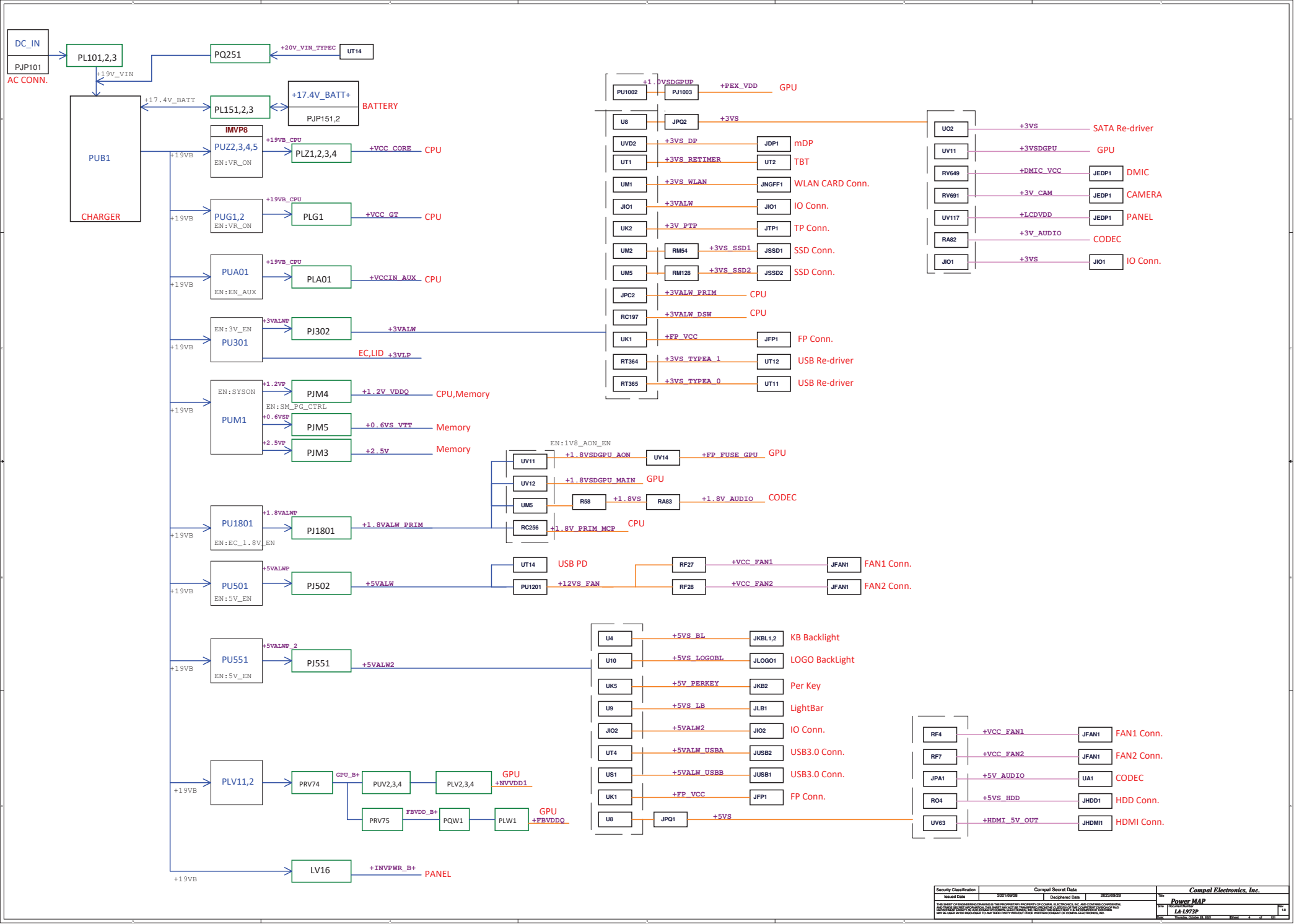
Item(X4E) un-pop	BOM Structure
EMI require reserve	XEMI@
EMC require reserve	XEMC@
ESD require reserve	XESD@
RF require reserve	@RF@

Item (X4E) pop	BOM Structure
EMI requirement	EMI@ V
EMC requirement	EMC@ V
ESD requirement	ESD@ V
RF requirement	RF@ V
FP EMC requirement	FP EMC@ V
FP ESD requirement	FPESD@ V
TBT ESD requirement	BL ESD@ V
TBT EMC requirement	BL EMC@ V
X4EAQTBOLO1	HH514 50

Item (X76)	BOM Structure
OVRM-uPI Gen1	X76UPIGEN1@
OVRM-ON Gen1	X76ONGEN1@
OVRM-uPI Gen2	X76UPIGEN2@
OVRM-ON Gen2	X76ONGEN2@
VRAM-SAMSUNG	X76SAM@
VRAM-HYNIX	X76HYN@

```
X76869BOLC7 - UPI OVRM GEN1
X76869BOLC8 - ON OVRM GEN1
X76869BOLC9 - UPI OVRM GEN2
X76869BOLCA - ON OVRM GEN2
X76869BOLC1 - SAMSUNG
X76869BOLC2 - HYNIX
```

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G3->S0

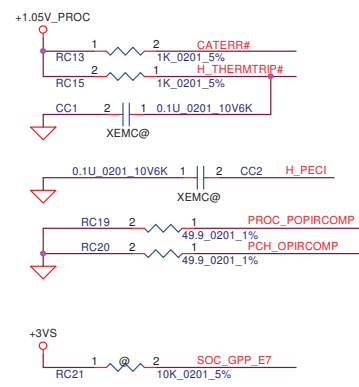
S0-> S3

S3 ->S0

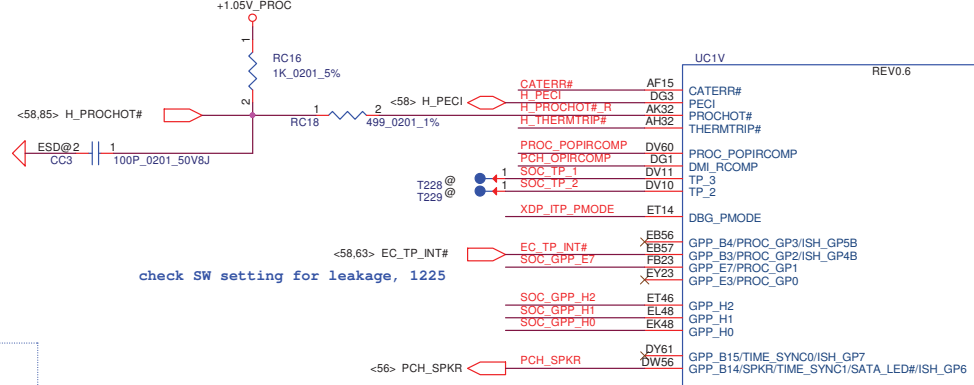
S0->S5



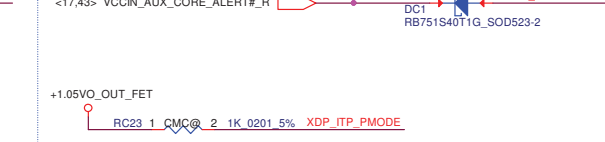




CHECK power net name, 05/17

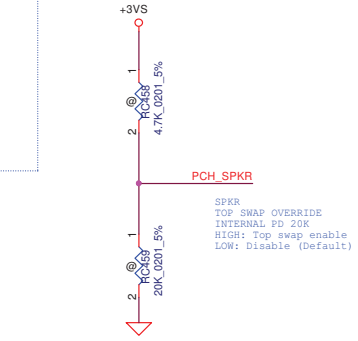


check SW setting, 1225

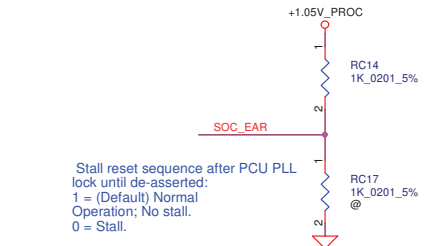
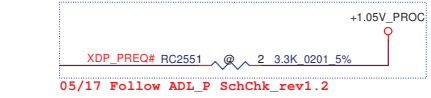
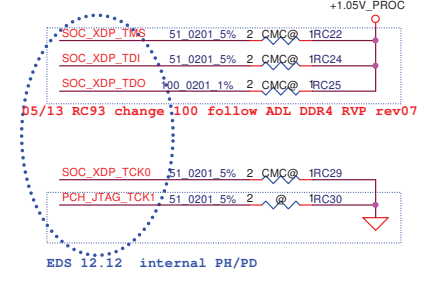
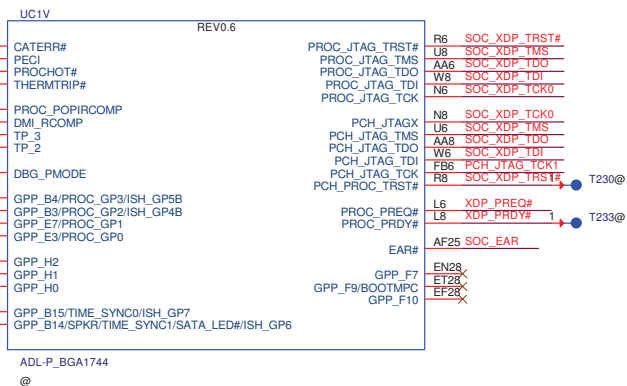


XDP_ITP_PMODE
DFX_TEST_MODE
INTERNAL_PU_20K
This strap should sample high. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Strap Pin



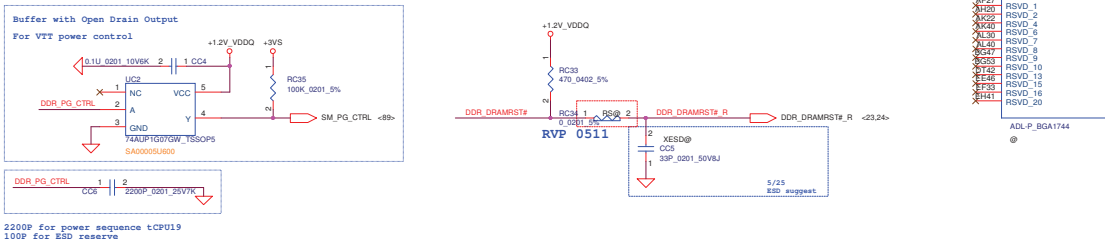
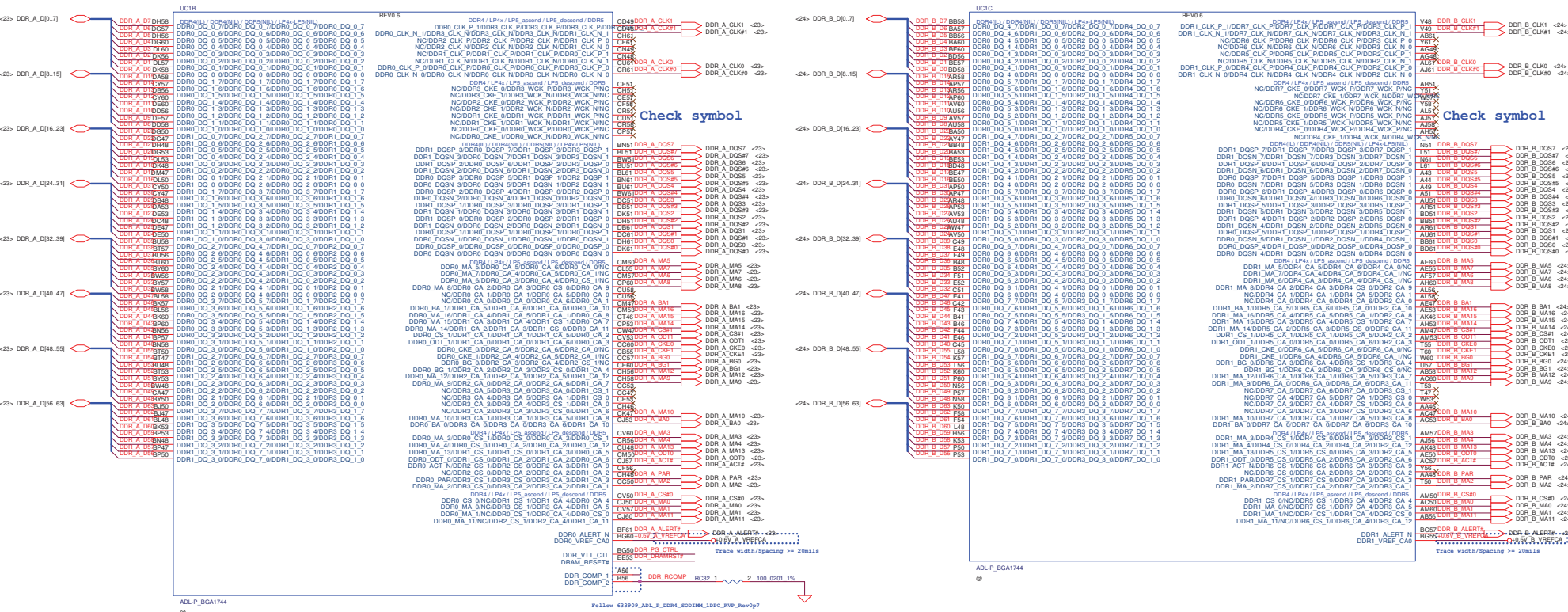
SPKR
TOP SWAP OVERRIDE
INTERNAL_PD_20K
HIGH: Top swap enable
LOW: Disable (Default)

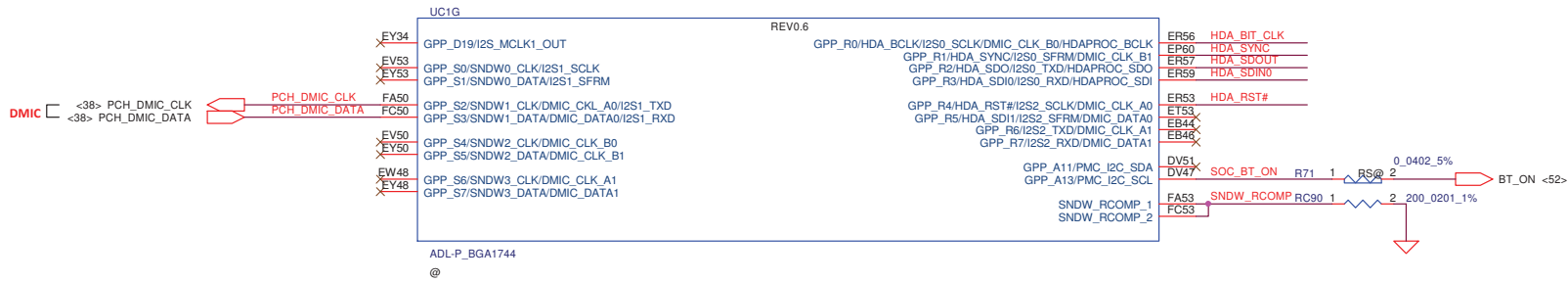


Stall reset sequence after PCU PLL lock until de-asserted:
1 = (Default) Normal Operation; No stall.
0 = Stall.

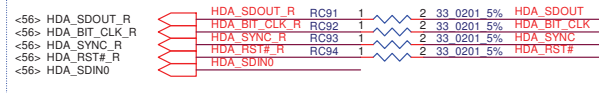
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DDR4: Refer to ADL_P_DDR4_SODIMM_1DPC_RVP_Rev0p7

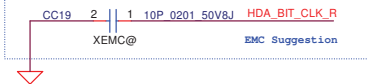




HDA for AUDIO



Follow
627205_ADL_P_PDG for Glitch



To Enable ME Override



572631_ICL_PCH_IP_EDS_Vol_1_Rev_0p7

VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V

Need to sync with codec VDDIO

HDA_SDOOUT

FLASH_DESCRIPTOR SECURITY OVERRIDE

INTERNAL PD 20K

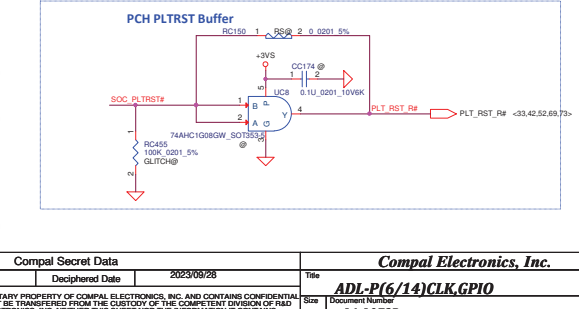
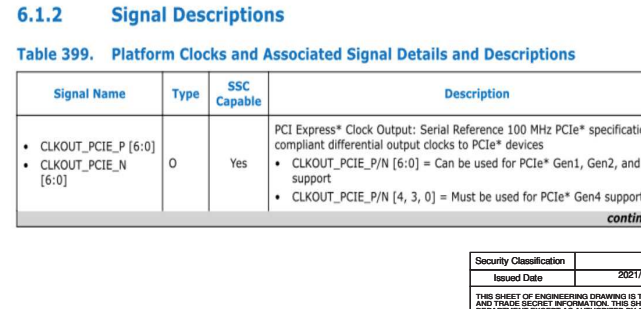
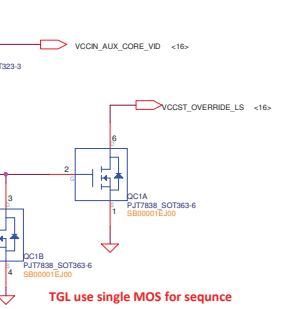
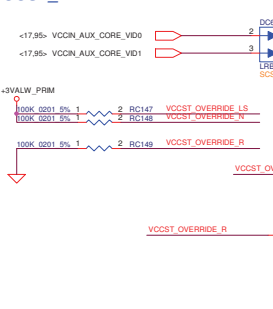
HIGH: OVERRIDEN

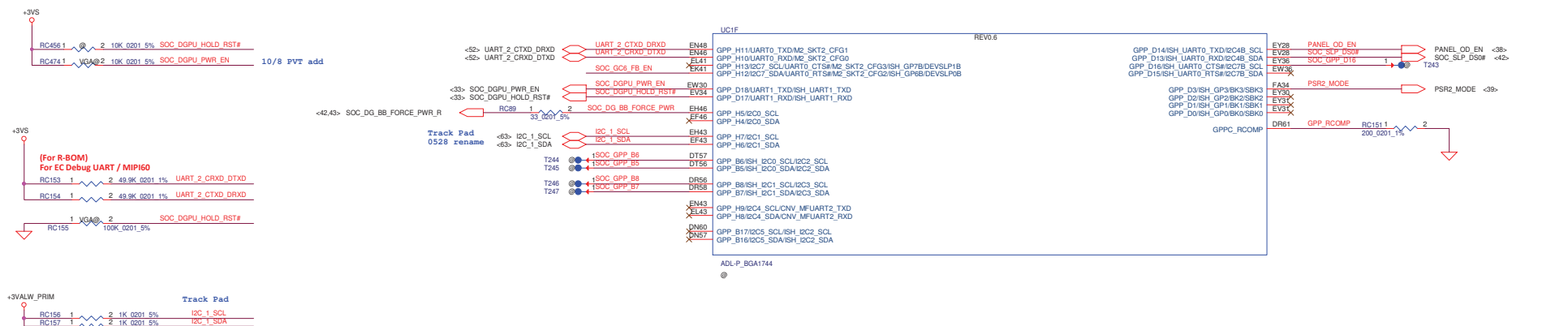
LOW: SECURITY MEASURES NOT OVERRIDEN (DEFAULT)

HDA_SYNC	CC12	@RF@1	2	22P	0201	25V8
HDA_BIT_CLK	CC13	@RF@1	2	22P	0201	25V8
HDA_SDOOUT	CC14	@RF@1	2	22P	0201	25V8
HDA_SDI0	CC15	@RF@1	2	22P	0201	25V8
HDA_RST#	CC16	@RF@1	2	22P	0201	25V8
PCH_DMIC_CLK	CC17	@RF@1	2	22P	0201	25V8
PCH_DMIC_DATA	CC18	@RF@1	2	22P	0201	25V8

Close SOC

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16.2.1 Configurable GPIO Voltage

Except for all pads in GPIO S, GPIO R, and GPD groups, all other GPIO groups support per-pad configurable voltage, which allows control selection of 1.8 V or 3.3 V for each pad. The configuration is done via soft straps.

Before soft straps are loaded, the default voltage of each pin depends on its default as input or output.

- Input: 1.8 V level with 3.3 V tolerant.
- Output: the pin drives 3.3 V via a ~20 K pull-up. With this, any 1.8 V device must be capable of taking 20 K pull-up to 3.3 V.

WARNING

GPIO pad voltage configuration must be set correctly depending on device connected to it; otherwise, damage to the PCH or the device may occur.

NOTES

1. GPIO S group supports 1.8 V only.
2. GPIO R group supports per-group voltage configuration (3.3 V or 1.8 V) only.
3. GPD group supports 3.3 V only.

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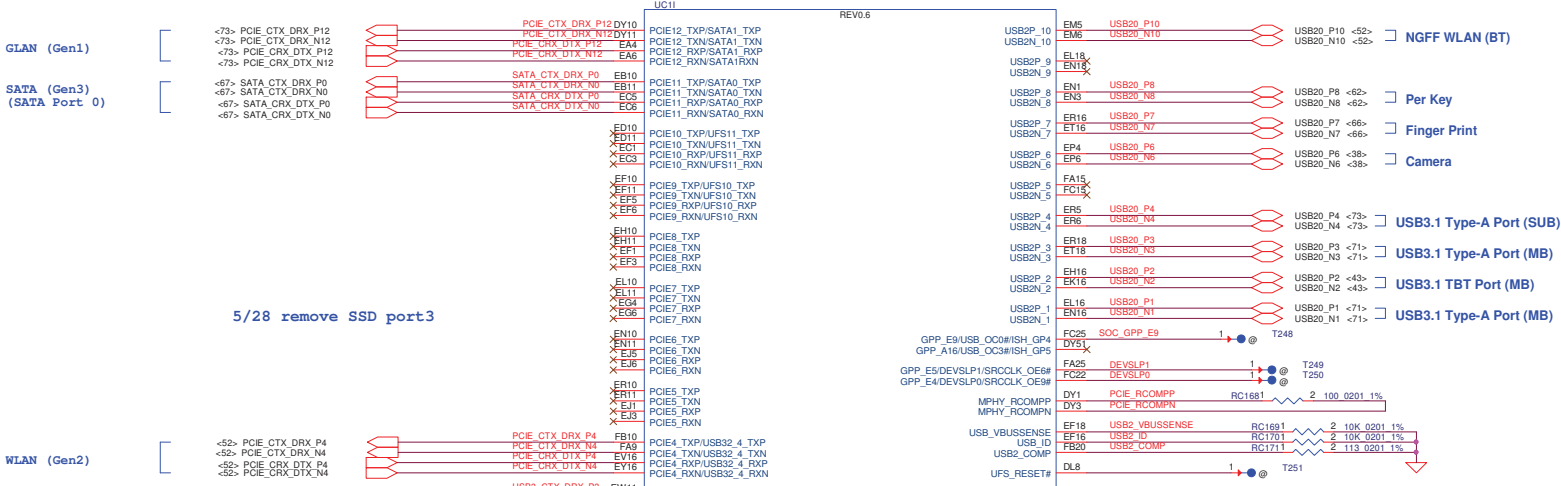
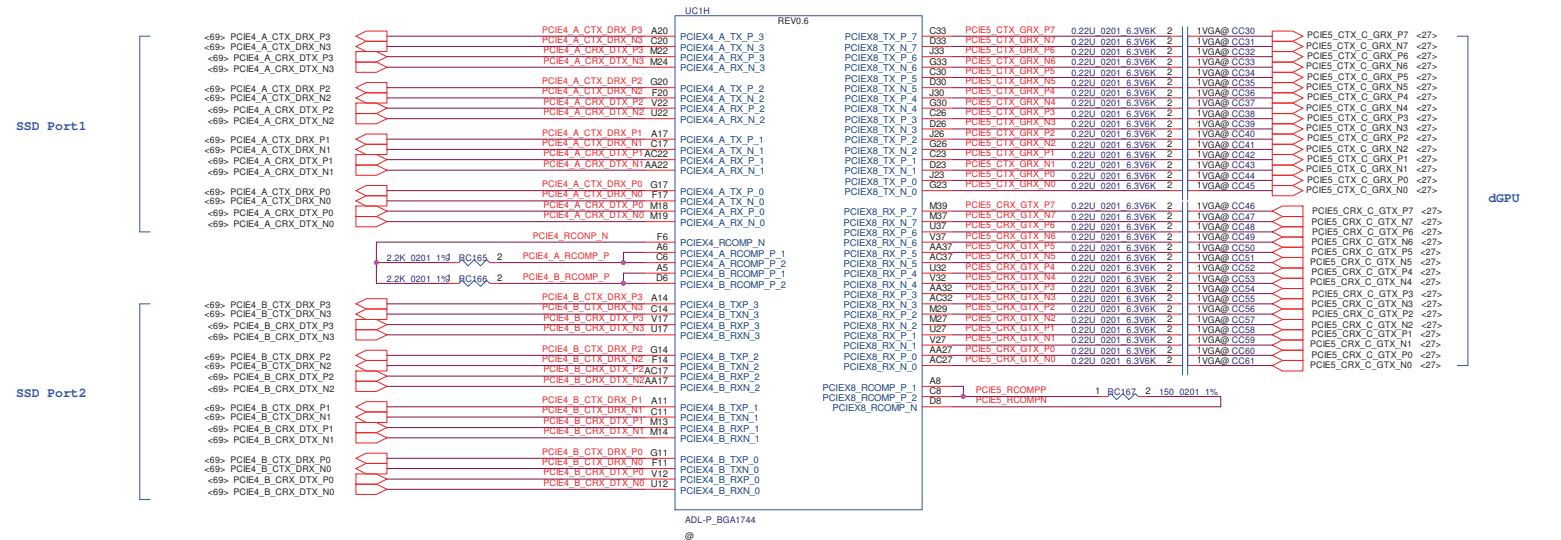
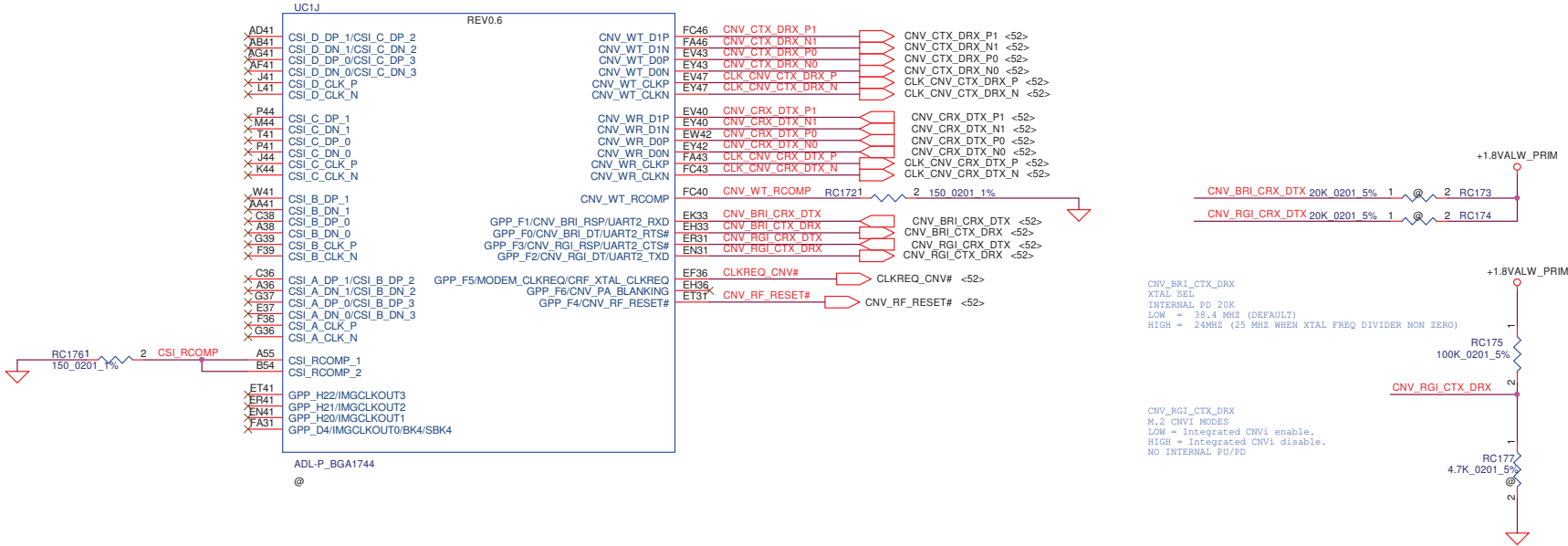
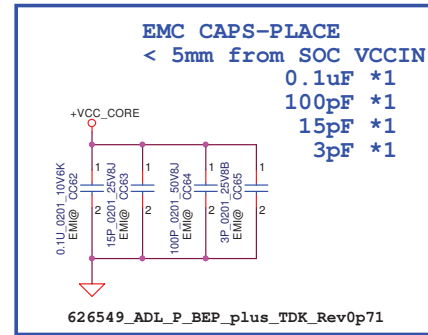
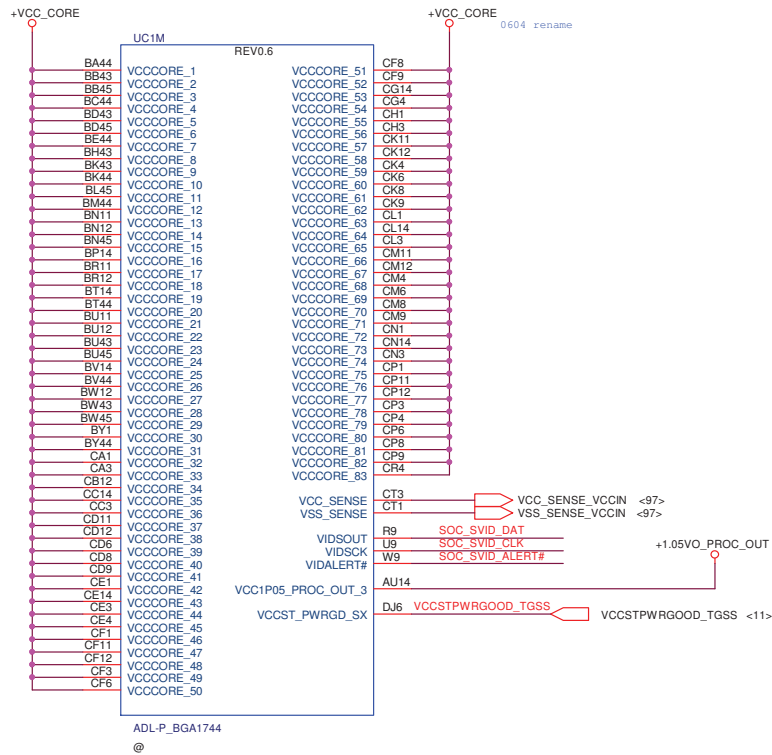


Table 180. USB3/USB2 Port Pairing for USB-C* Connectors

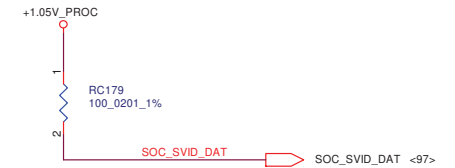
	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

To make split xDCI controller working functionally for different USB-C* connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C* connectors, but it is not strictly required.





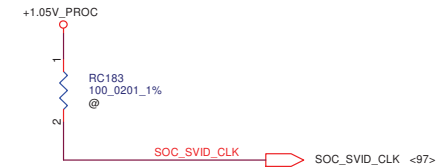
SVID DATA



SVID ALERT



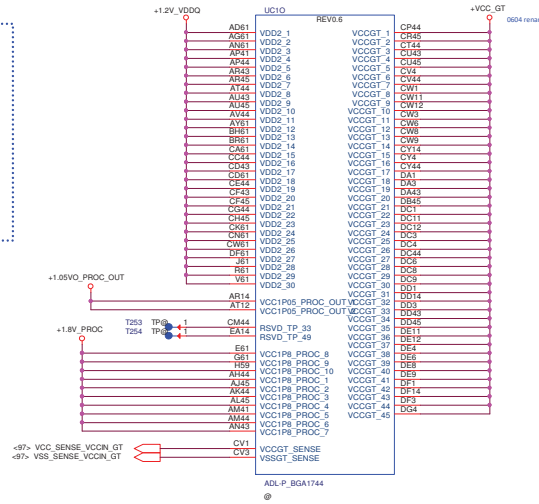
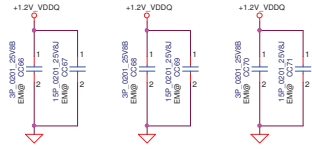
SVID CLOCK



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EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
15pF* 3 (EMI@)
3pF* 3 (EMI@)

627333_ADL_P_DDR4_RVP_TDK_Rev0p7



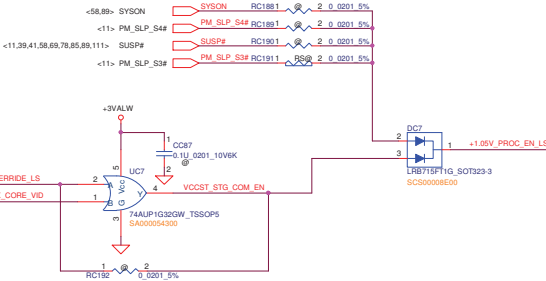
627205_ADL_P_PDG_Rev1.2



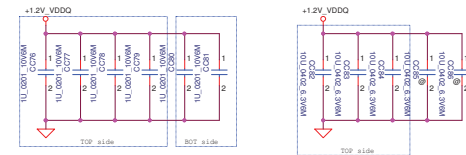
NOTE

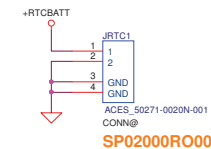
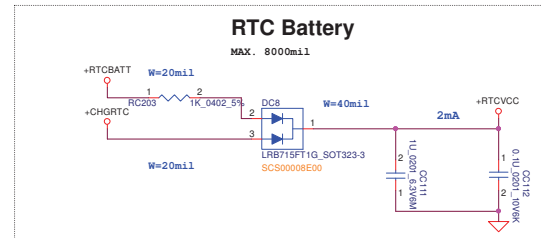
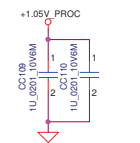
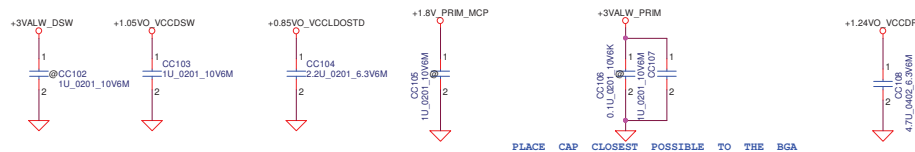
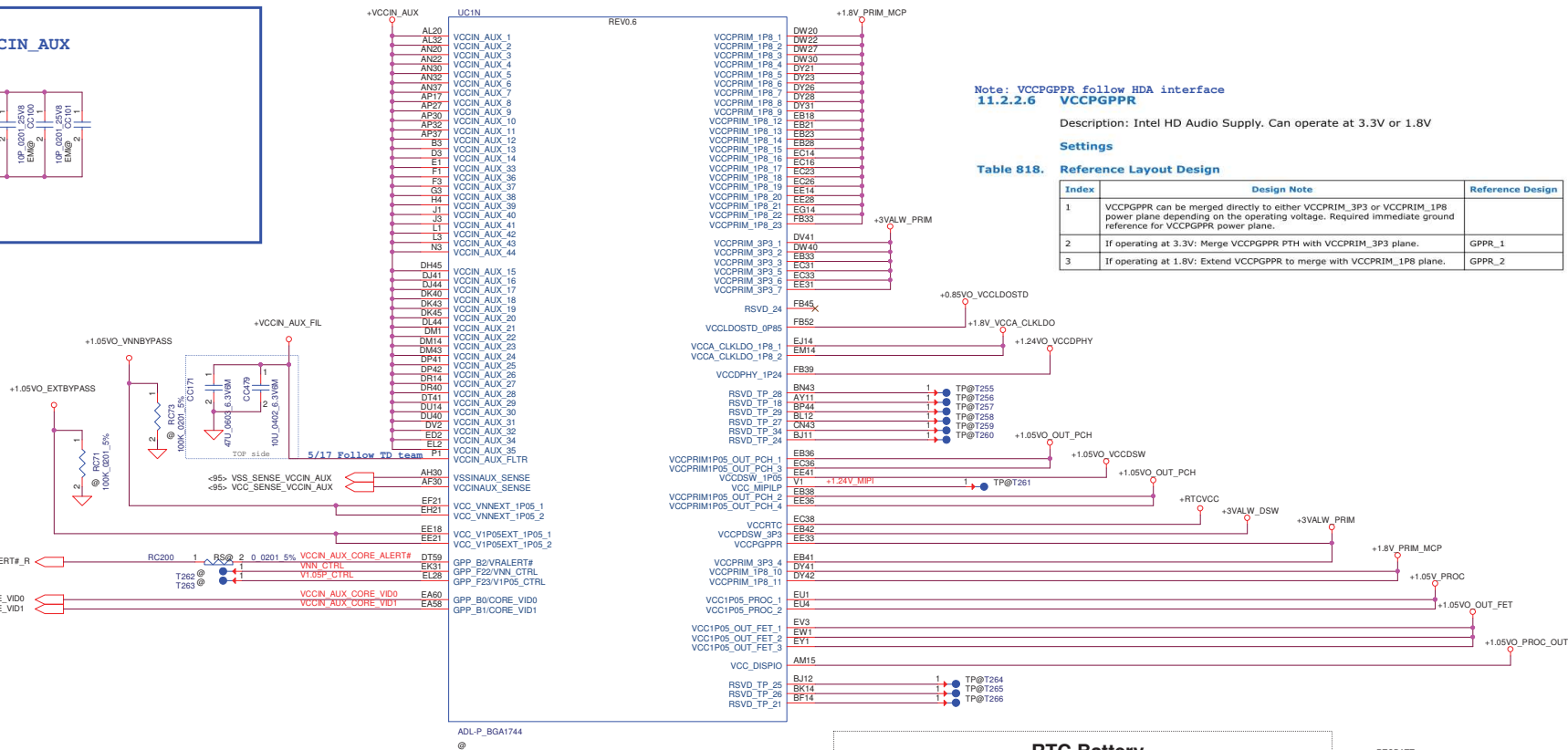
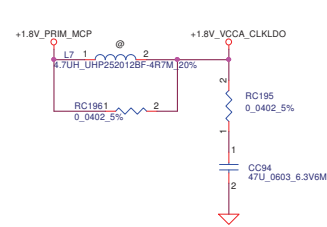
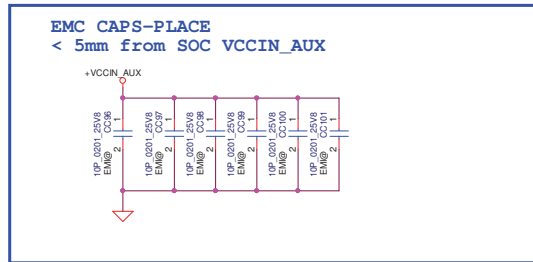
Sideband signals(PECI,THERMTRIP,PROCHOT,VCCST_PWRGD,SVID) should be connected to **VCC1P05_PROC** rail when there is Power Gate or to **VCC1P05_OUT_FET** (which should be shorted to VCC1P05_OUT_FET)rail when there is no Power Gate.

+1.05V_PROC Enable

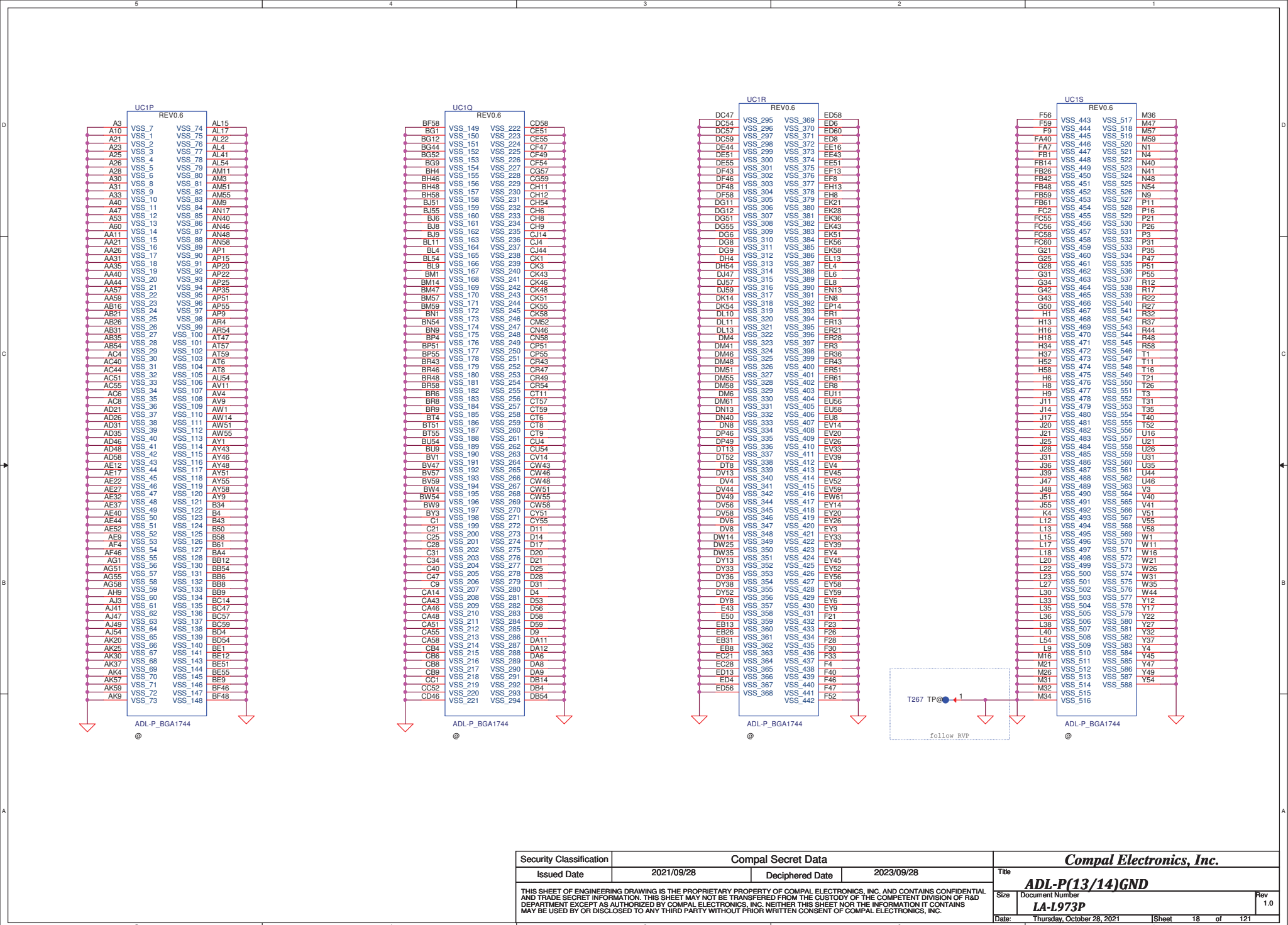


1uF* 6
10uF * 3
uF * 2
Layout Follow 627205_ADL_P_PDG_Rev0p7





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CHANNEL-A (Interleaved Memory)

> BOT : Reverse type (4mm)

> Non-ECC SO-DIMM

SPD ADDRESS FOR CHANNEL A :

WRITE ADDRESS: 0XA0

READ ADDRESS: 0XA1

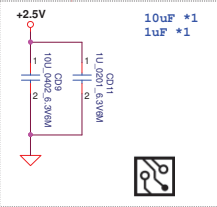
SA0 = 0; SA1 = 0; SA2 = 0.

DDR4 POR OPERATING SPEED: 1867 MT/S

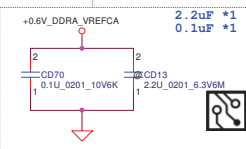
STRETCH GOAL IS 2133 MT/S

Decoupling Cap._Channel A

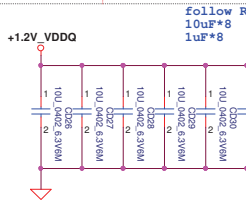
Layout Note:
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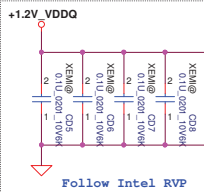
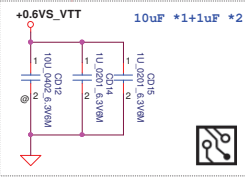
Layout Note:
PLACE THE CAP near JDIMM1B. 164



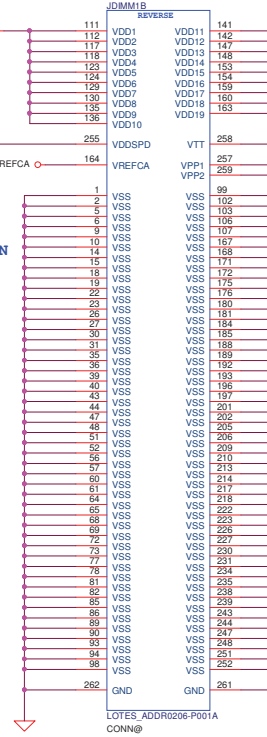
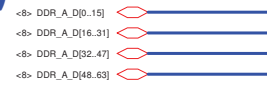
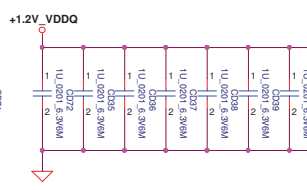
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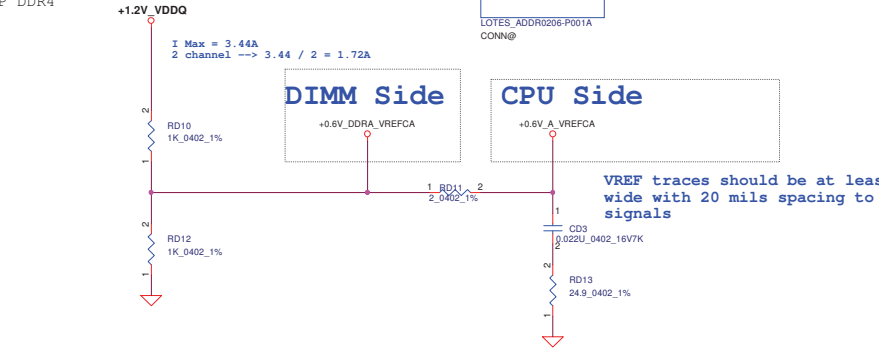
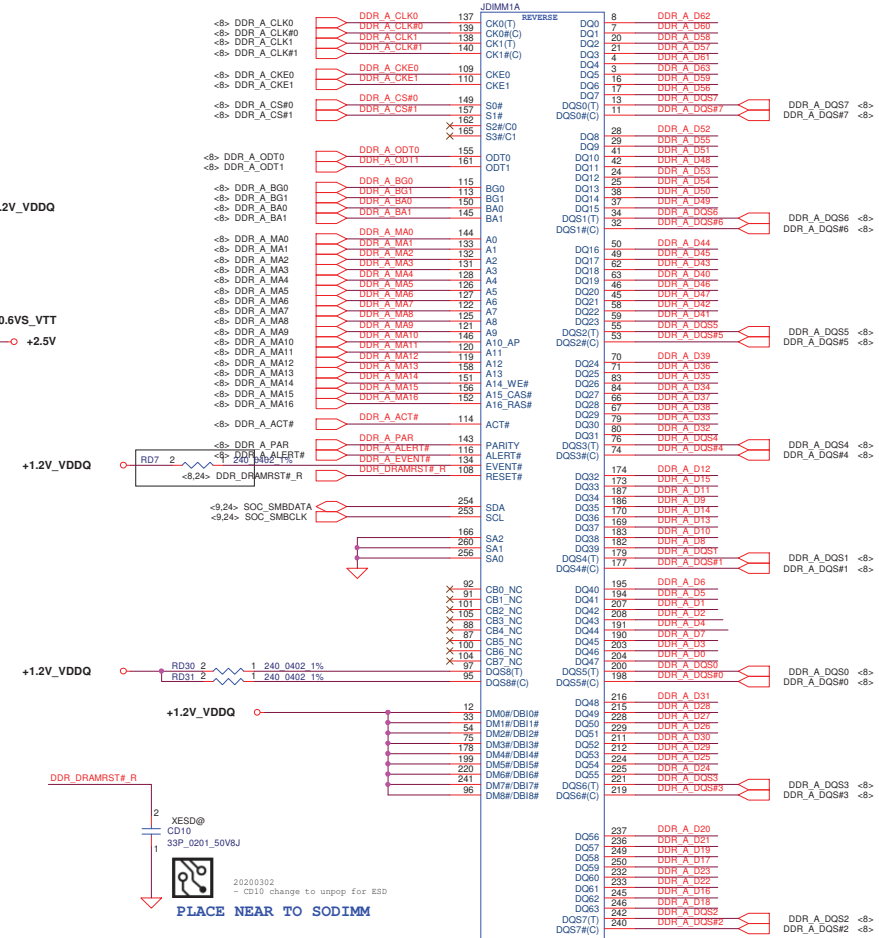
Layout Note:
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Follow Intel RVP



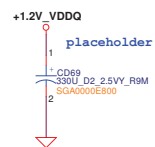
Part Number: SP07001CY00
Part Value: S SOCKET LOTES ADDR0206-P001A 260P DDR4



> Non-ECC SO-DIMM



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals



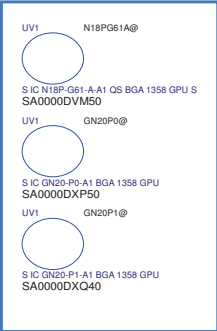
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Issued Date	2021/09/28	Deciphered Date	2023/09/28	Title	DDRIV CHB: DIMM0	
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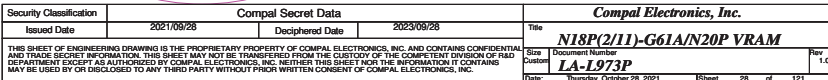
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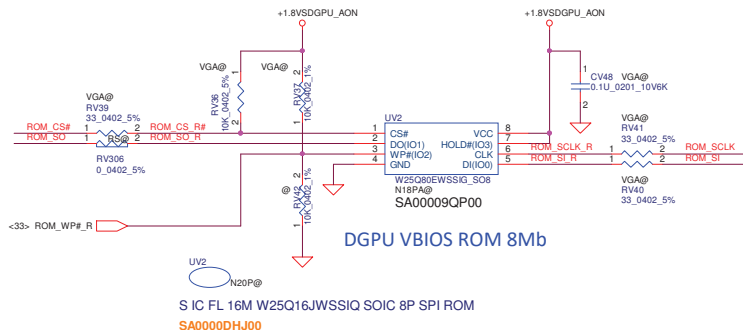
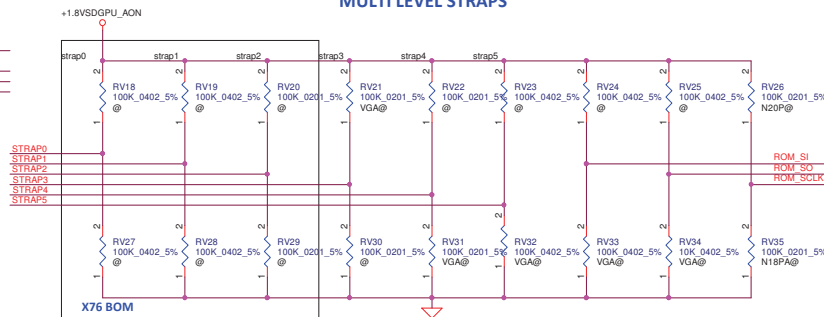
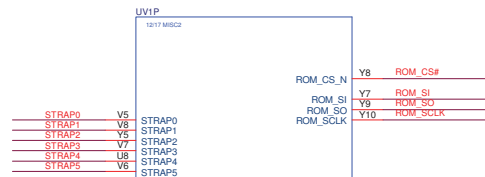
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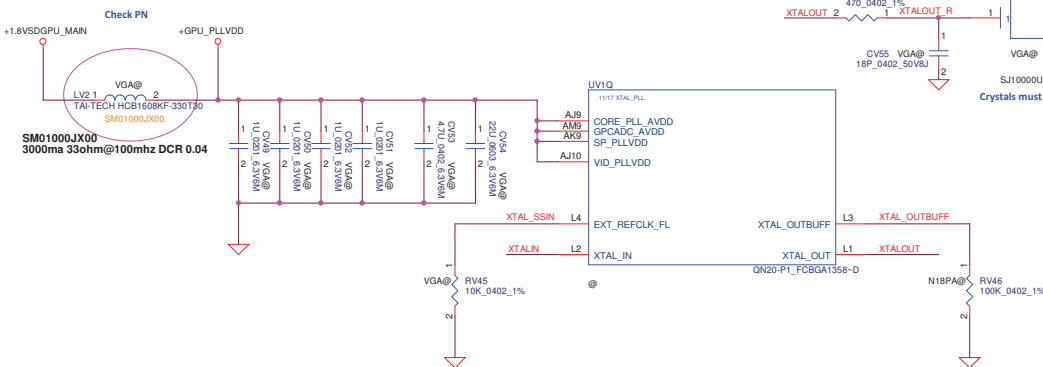


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ZZZ X76UPGEN1@
ALT. GROUP PARTS OVRM N20P UPI G1 HH514
X76869BOLCU
ZZZ X76ONGEN1@
ALT. GROUP PARTS OVRM N20P ON G1 HH514
X76869BOLCV
ZZZ X76UPGEN2@
ALT. GROUP PARTS OVRM N20P UPI G2 HH514
X76869BOLC9
ZZZ X76ONGEN2@
ALT. GROUP PARTS OVRM N20P ON G2 HH514
X76869BOLCA



N18PA

Table 11.3 RAMCFG

Strap Pins See Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	
L	L	H	1 (0x0001)	
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	

Table 11.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1

ROM_SO (10K)	ROM_SI	ROM_SCLK	Strap5	Strap4	Strap3	Strap2	Strap1	Strap0
L	L	L	L	L	H	RVL	RVL	RVL

SAMSUNG (000)	RV27 100K_0402_5% SD028100380	RV28 100K_0402_5% SD028100380	RV29 100K_0402_5% SD043100380	RV30 100K_0402_5% SD043100380	ZZZ X76SAM@ ALT. GROUP PARTS VRAM SAM 4G HH514 X76869BOLC1
MICRON (001)	RV18 100K_0402_5% SD028100380	RV28 100K_0402_5% SD028100380	RV29 100K_0402_5% SD043100380	RV30 100K_0402_5% SD043100380	ZZZ X76MIC@ ALT. GROUP PARTS VRAM MICRON 4G HH514 X76869BOLC2
HYNIX (010)	RV27 100K_0402_5% SD028100380	RV28 100K_0402_5% SD028100380	RV29 100K_0402_5% SD043100380	RV30 100K_0402_5% SD043100380	ZZZ X76HYN@ ALT. GROUP PARTS VRAM HYN 4G HH514 X76869BOLC2

N20P

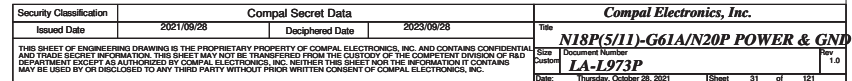
Table 9.3 RAMCFG

Strap Pins See Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	
L	L	H	1 (0x0001)	
L	H	L	2 (0x0002)	
L	H	H	3 (0x0003)	

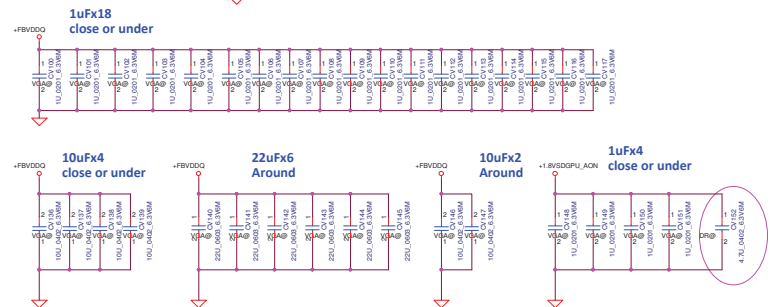
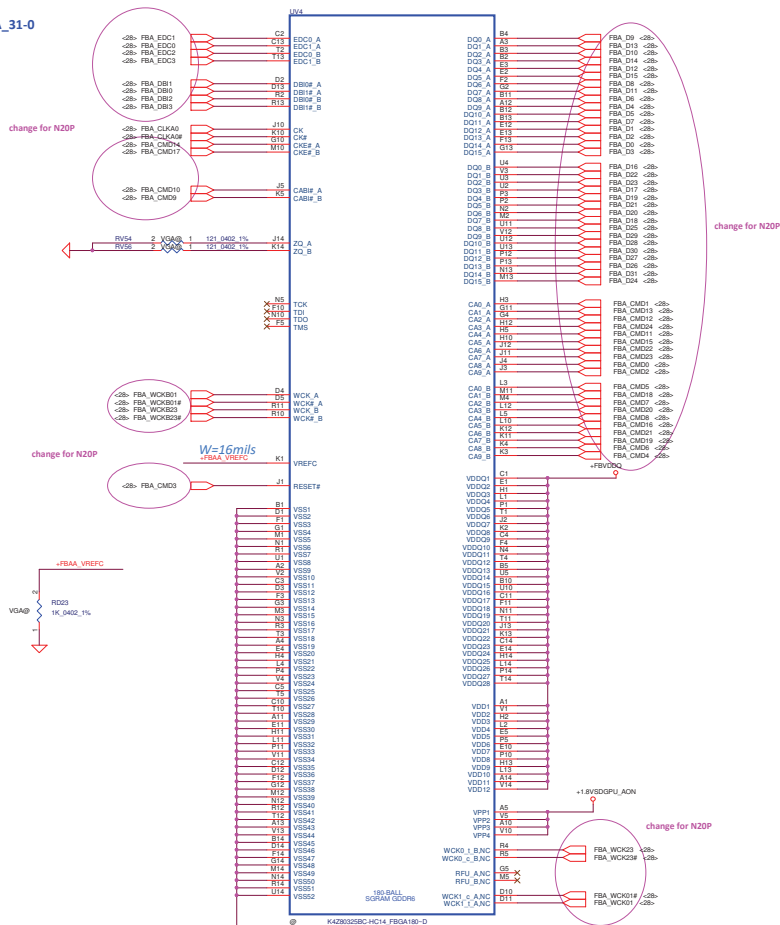
Table 9.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1

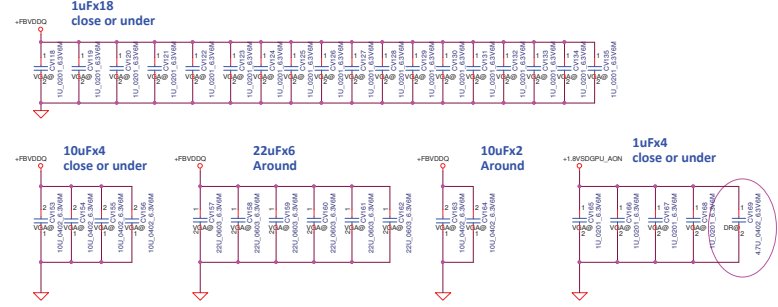
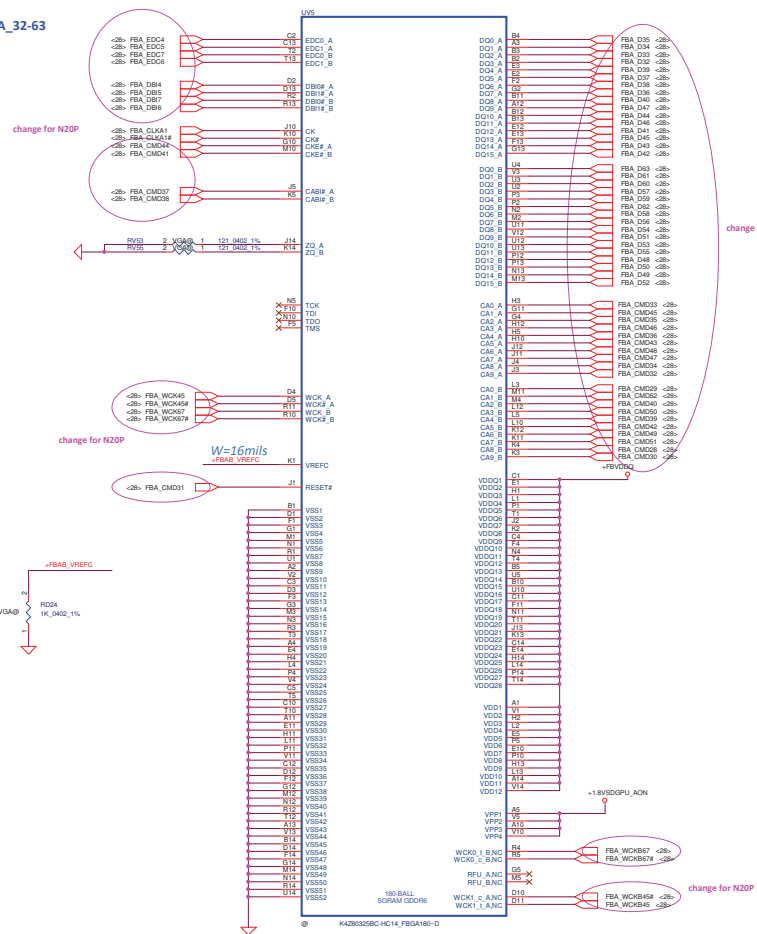
ROM_SO (10K)	ROM_SI	ROM_SCLK	Strap5	Strap4	Strap3	Strap2	Strap1	Strap0
L	L	H	L	L	H	RVL	RVL	RVL



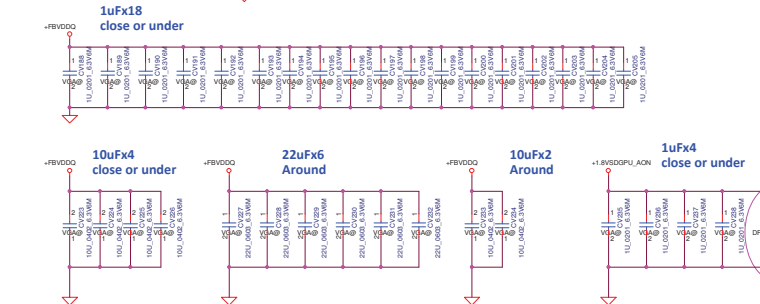
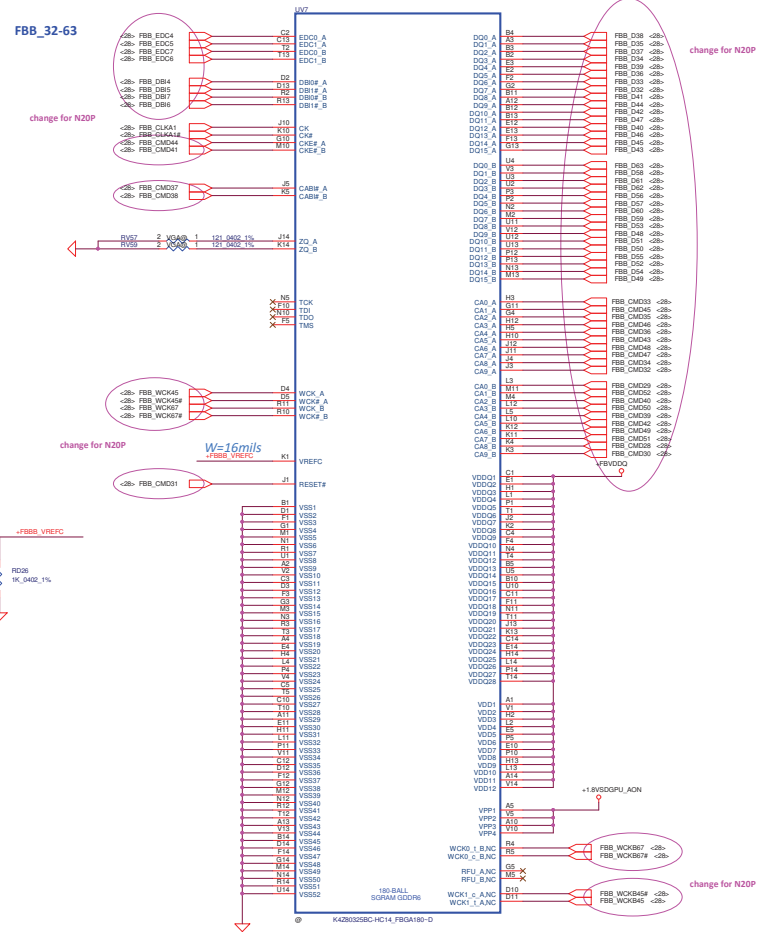
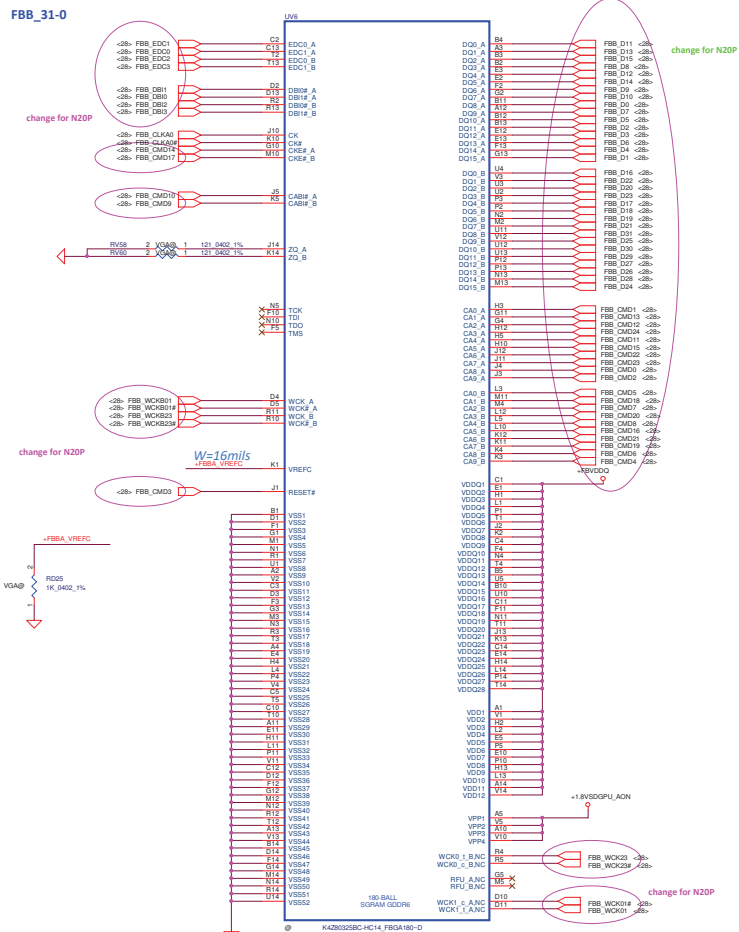
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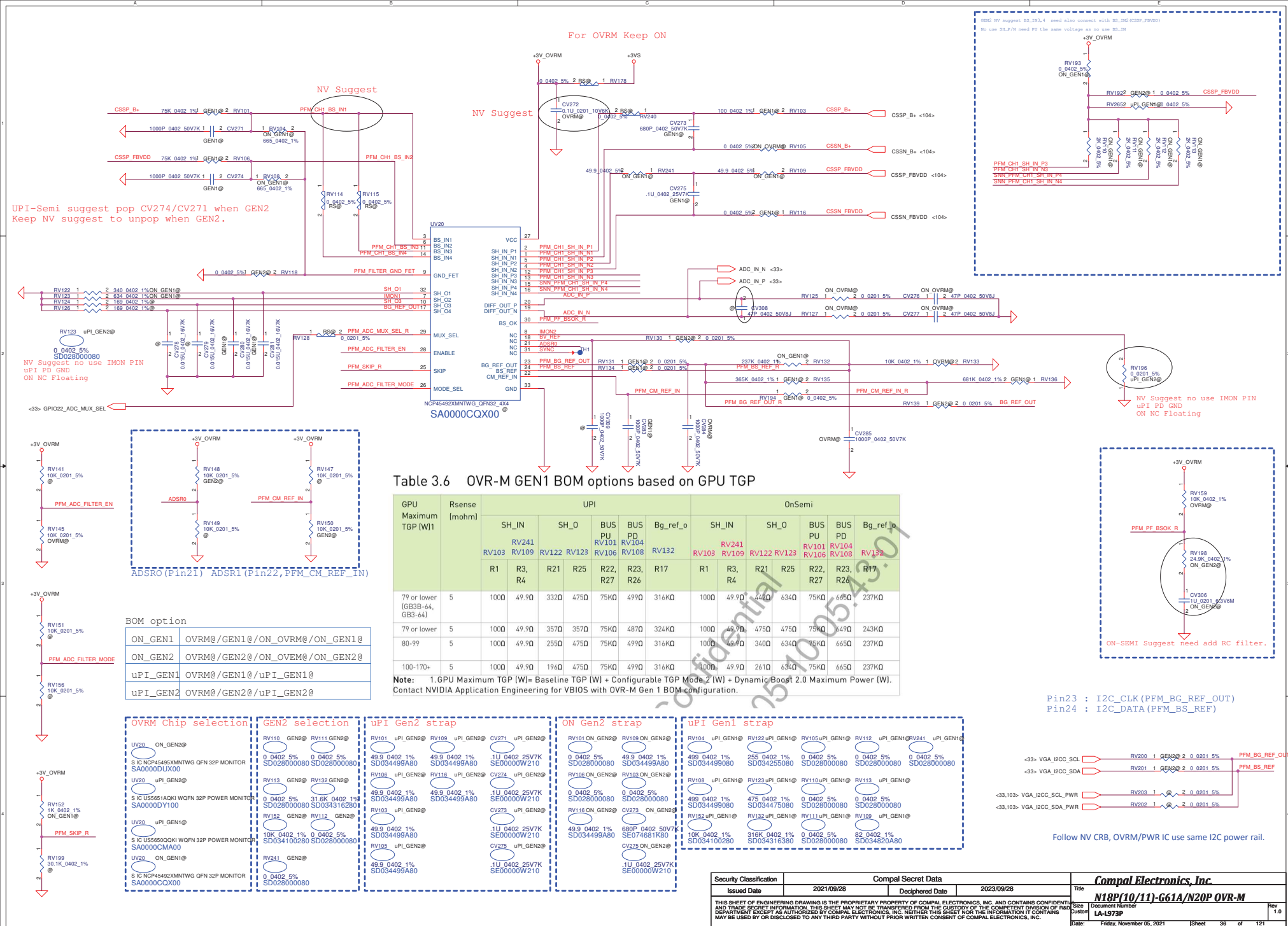


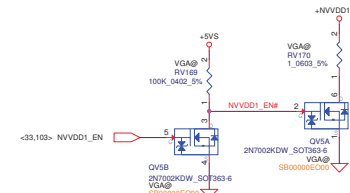
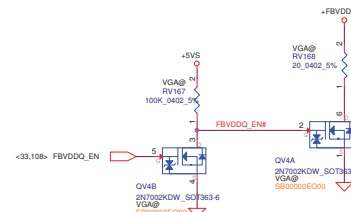
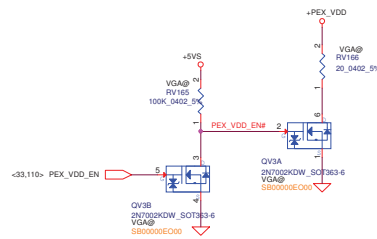
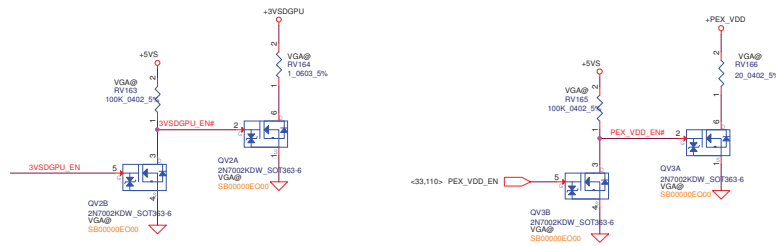
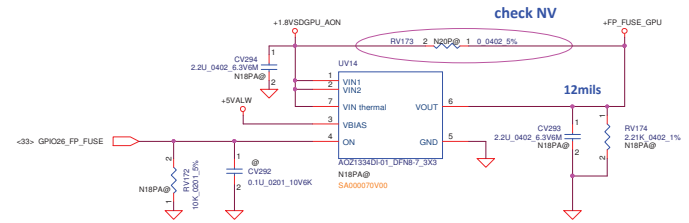
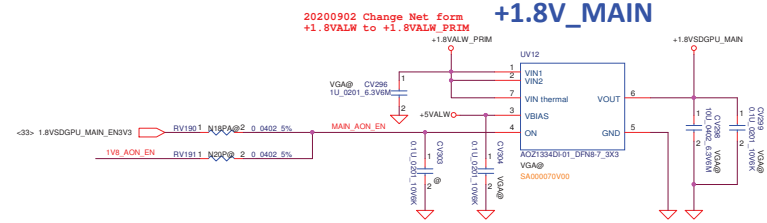
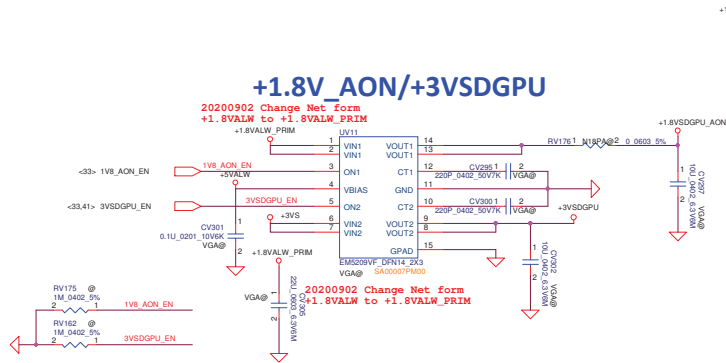
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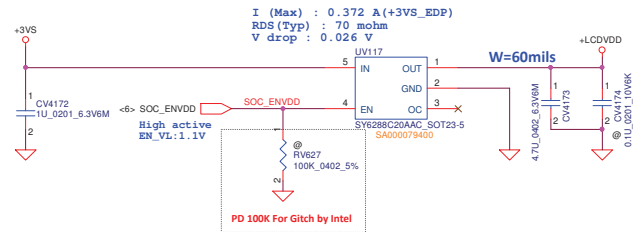
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Issued Date	2021/09/26	Deciphered Date	2023/08/28	
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			Sheet	34 of 121



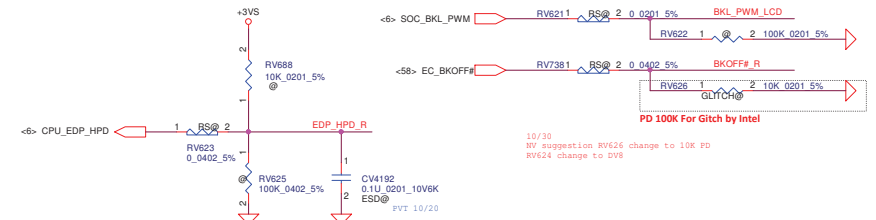




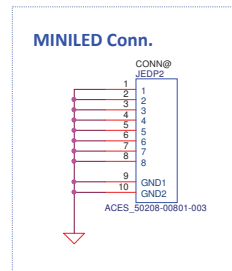
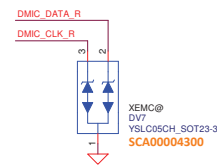
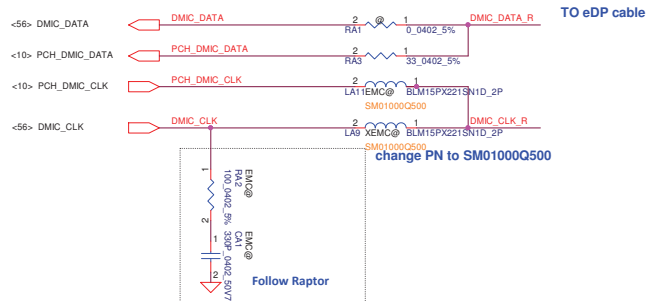
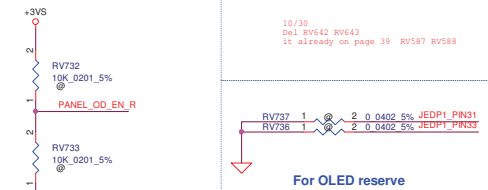
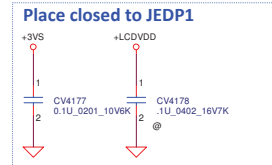
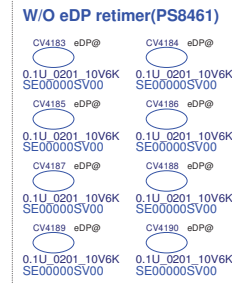
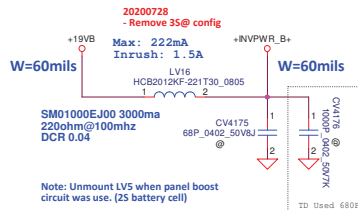
LCD POWER CIRCUIT



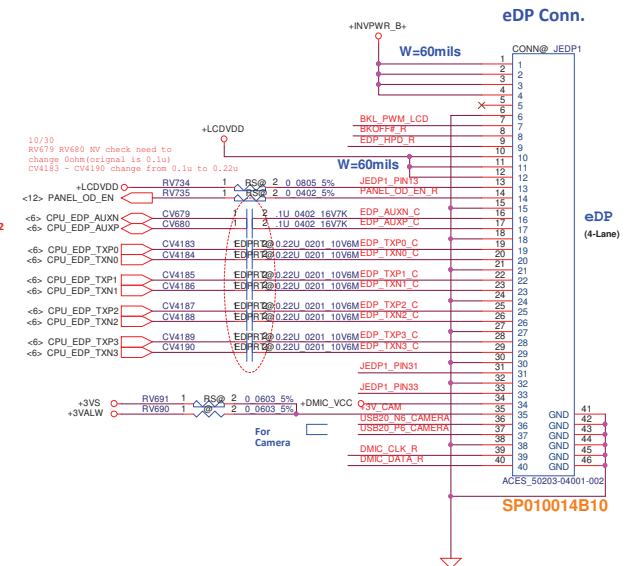
LCD enable signal



Camera



2021/4/27 RV679 and RV680 change from 0ohm to 0.1u 0.0402

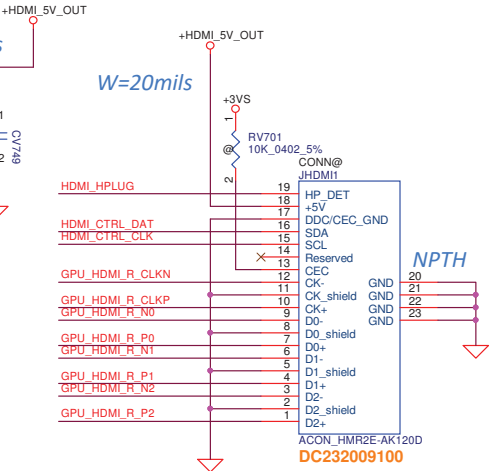
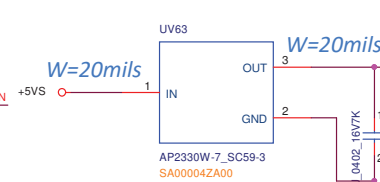
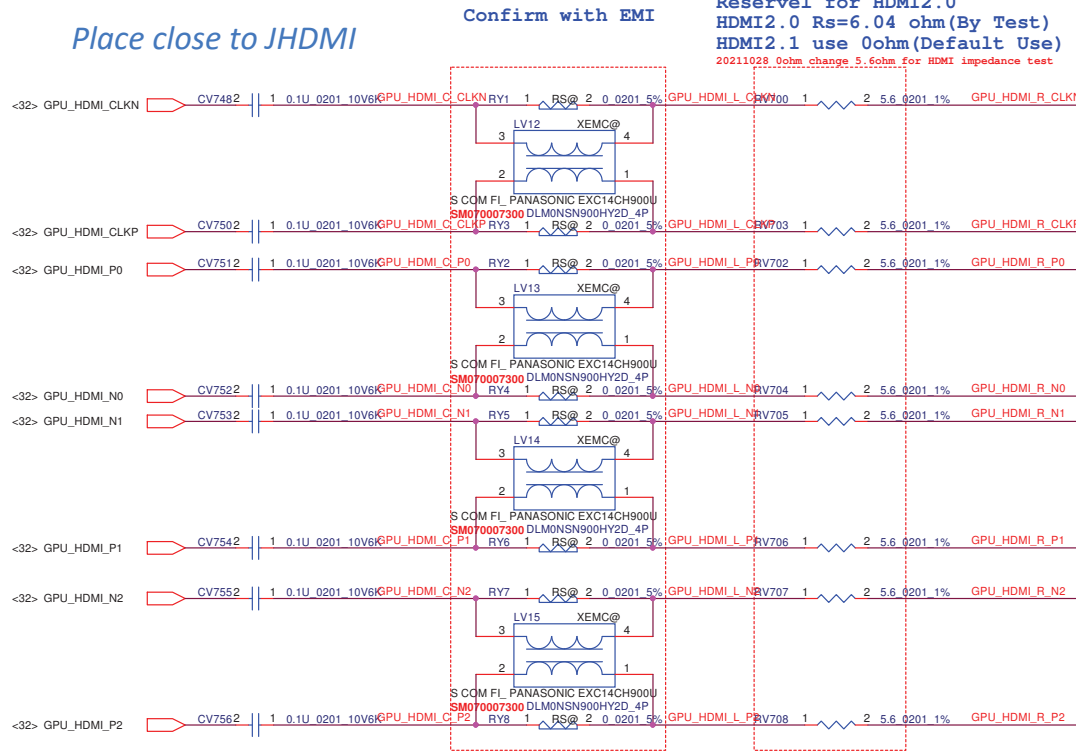


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								Size		Document Number		Rev	
										LA-L973P		1.0	
								Date:		Thursday, October 26, 2021		Sheet 38 of 121	

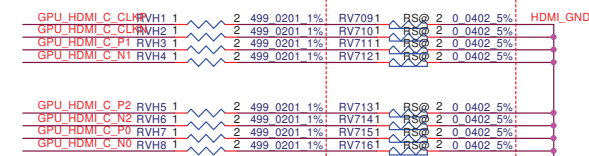
Place close to JHDMI

Confirm with EMI

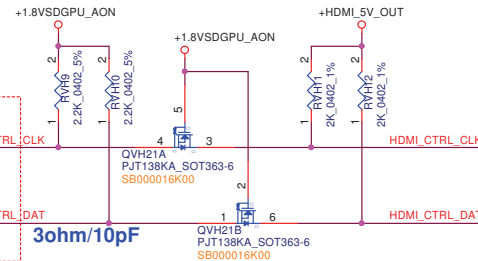
Reservel for HDMI2.0
HDMI2.0 Rs=6.04 ohm(By Test)
HDMI2.1 use 0ohm(Default Use)
20211028 0ohm change 5.6ohm for HDMI impedance test



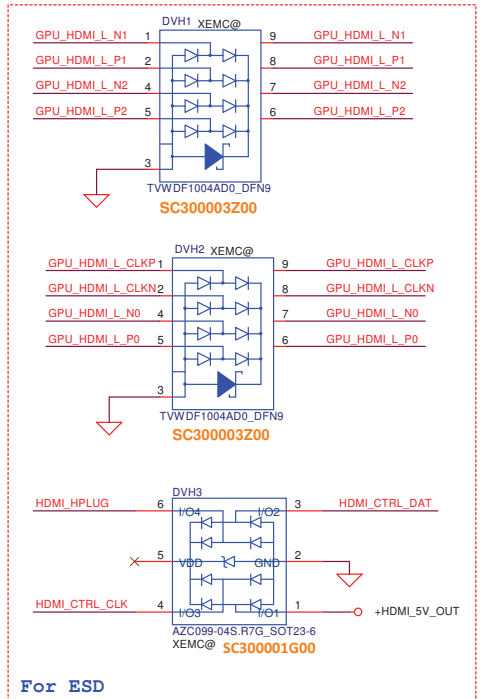
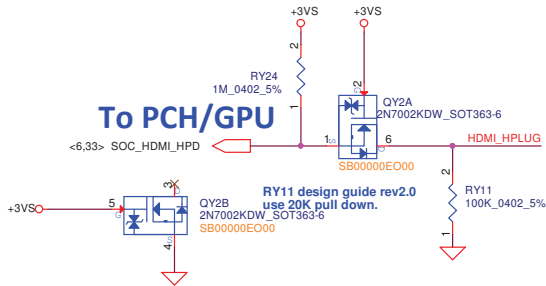
Reservel for HDMI2.0 bead SM01000LP00



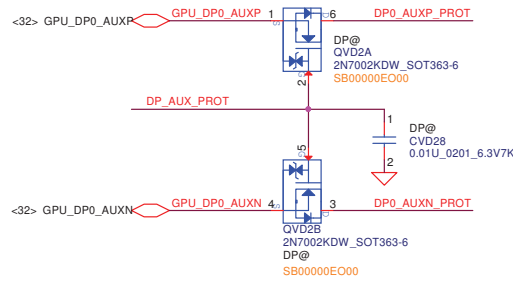
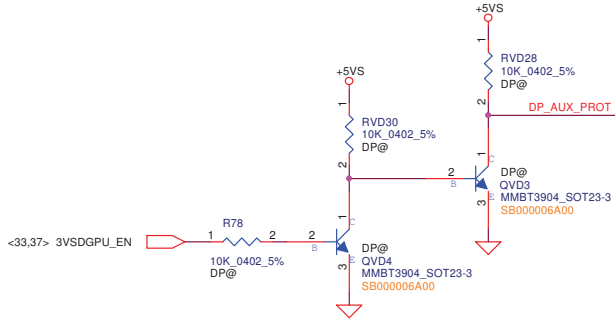
DDC



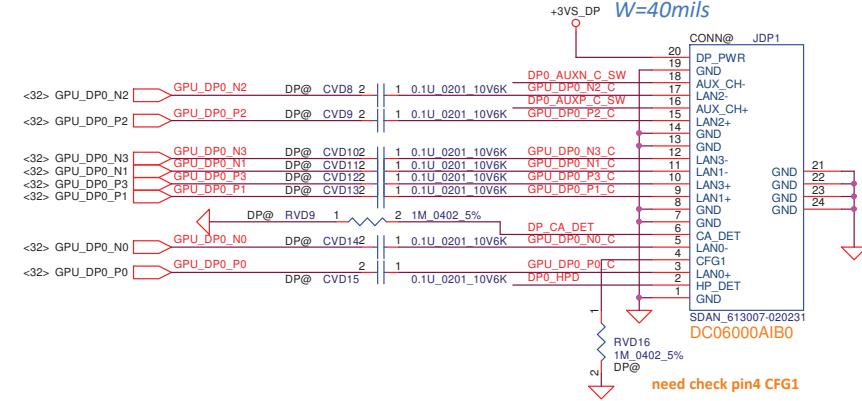
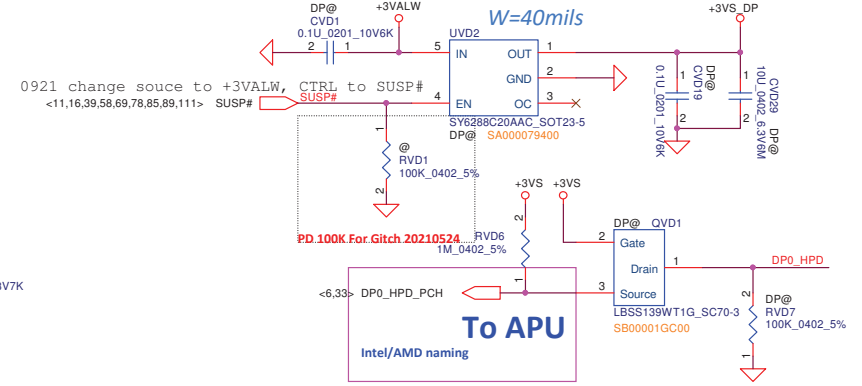
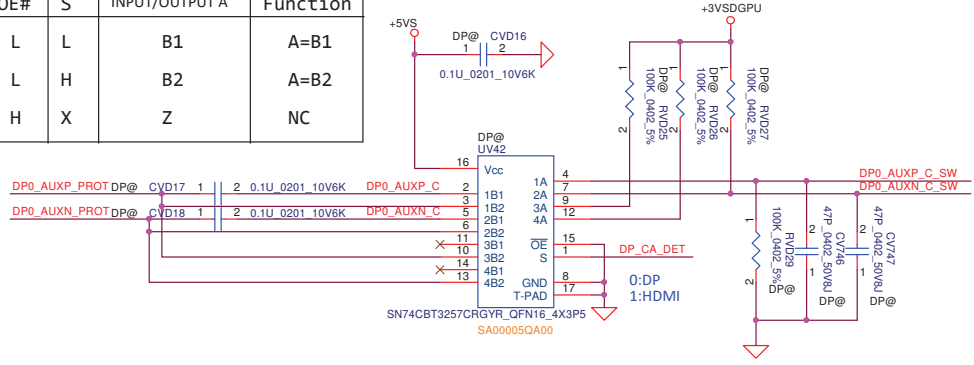
To PCH/GPU



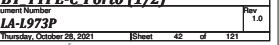
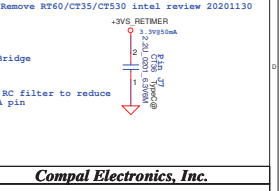
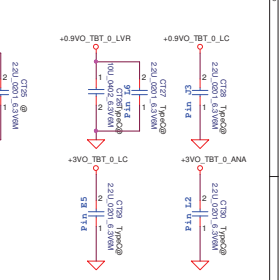
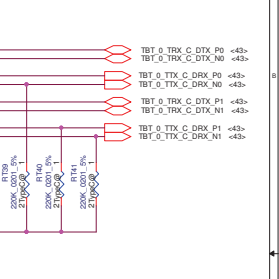
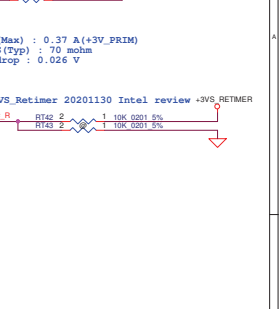
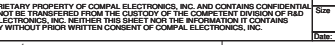
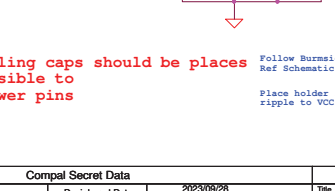
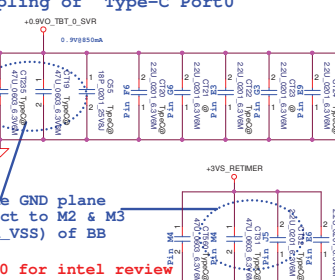
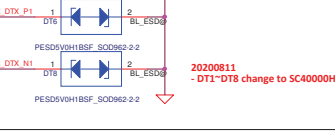
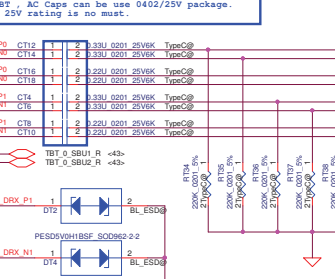
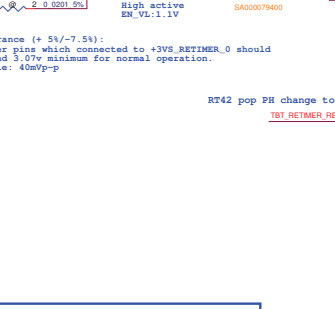
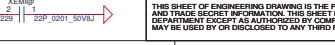
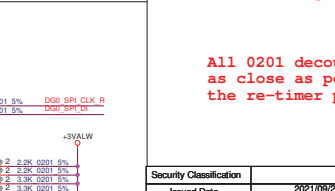
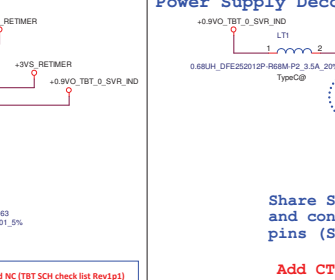
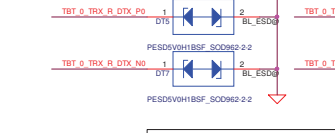
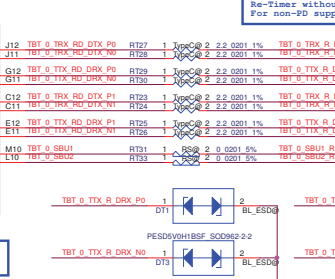
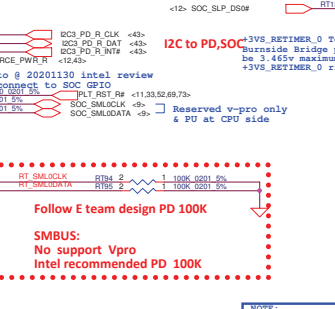
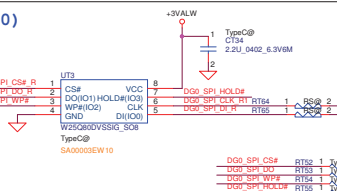
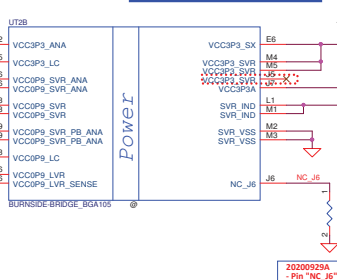
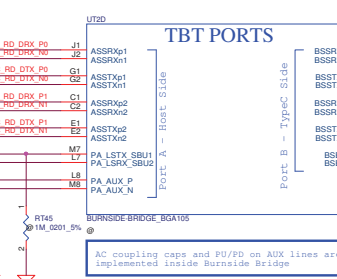
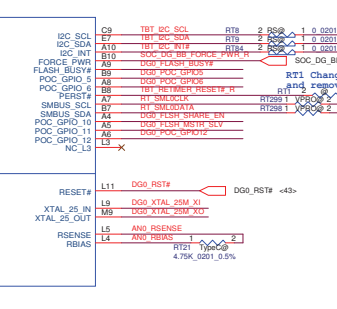
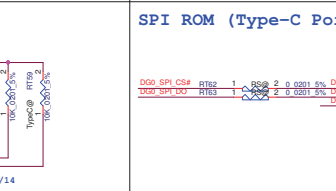
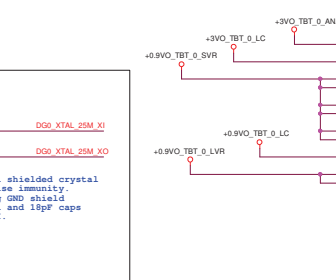
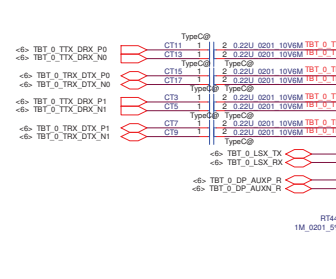
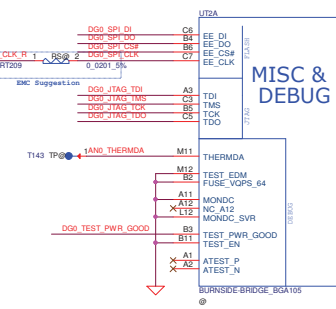
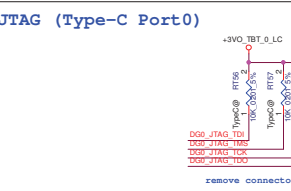
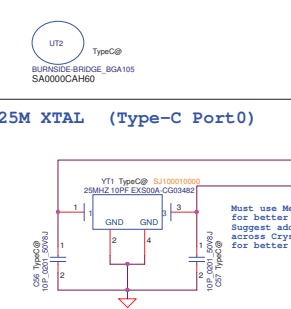
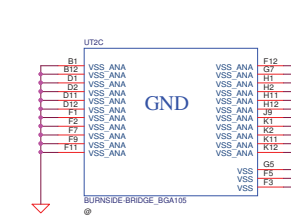
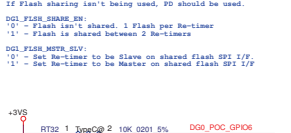
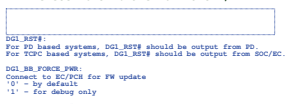
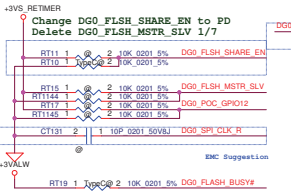
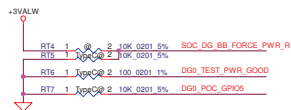
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								HDMI LS & Conn.	
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						Date:	Monday, November 08, 2021	Sheet	40



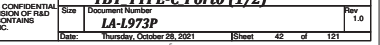
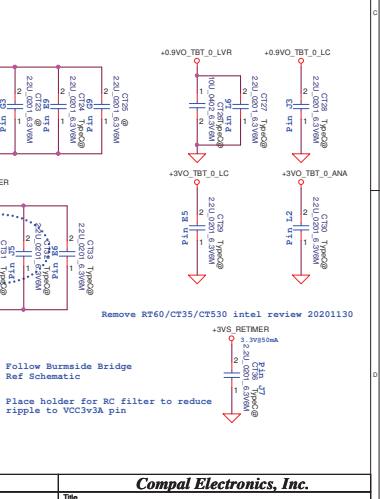
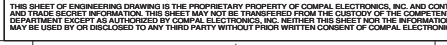
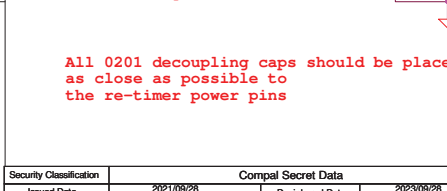
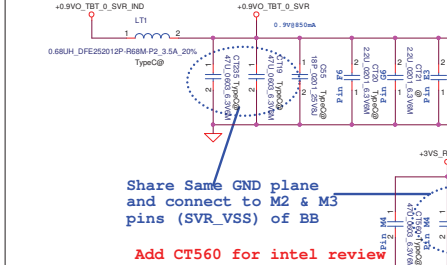
OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1
L	H	B2	A=B2
H	X	Z	NC



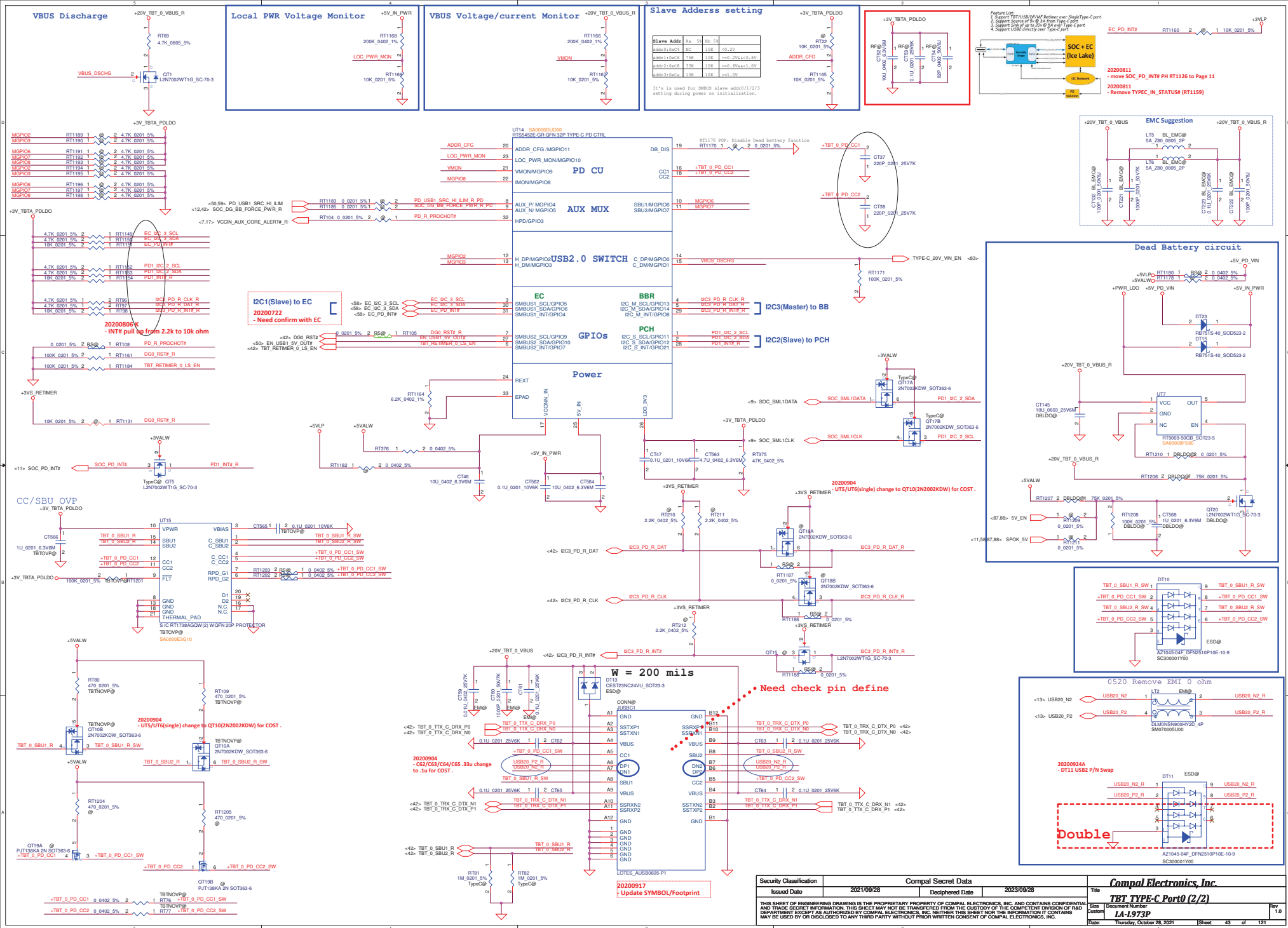
MB_USB3.1 TypeC Conn. (Port 0/ Re-Timer Master)



Power Supply Decoupling of Type-C Port0



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				Date:	Thursday, October 28, 2021	Sheet 47 of 121

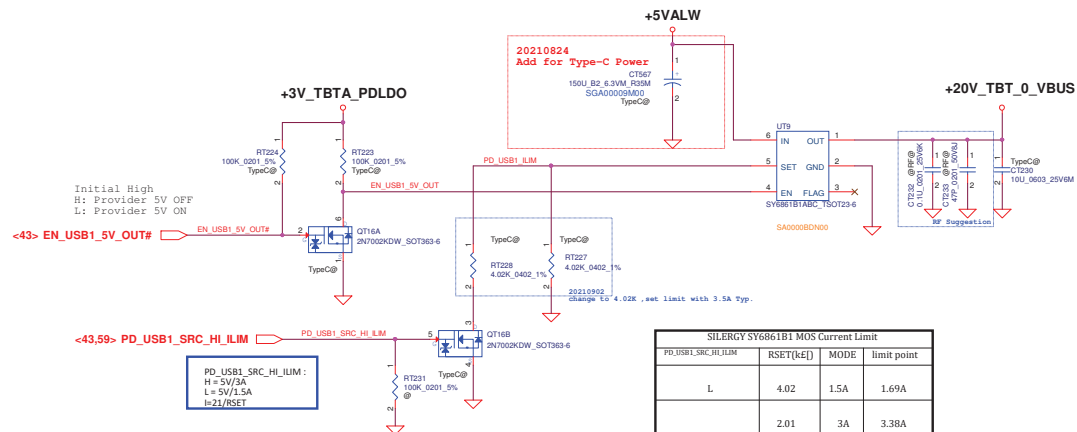
Reserve Page

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MB_USB3.1 TypeC Conn. (Power Path) - For Realtek 5452E

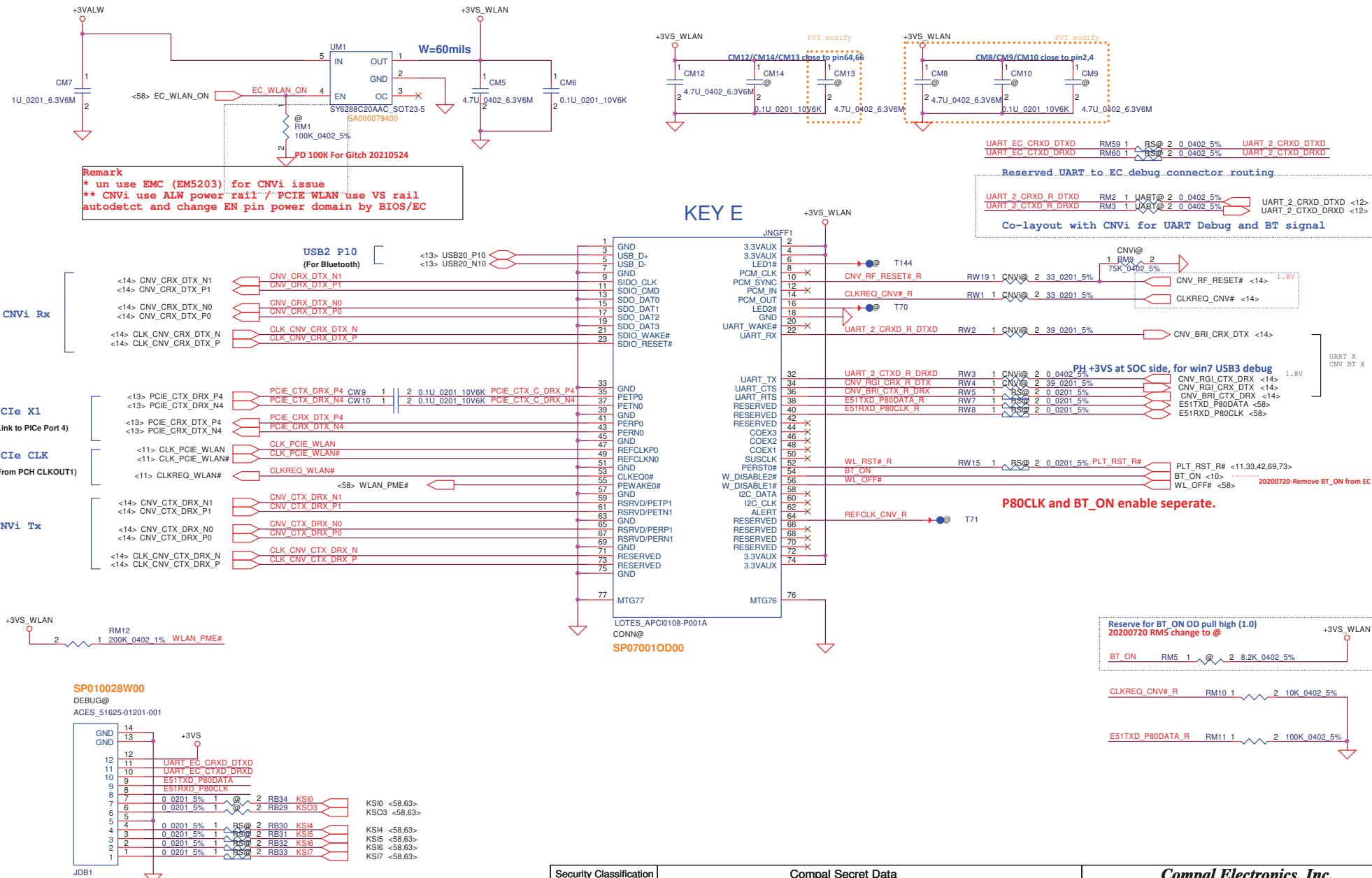


SILERGY SY6861B1 MOS Current Limit			
PD_USB1_SRC_HI_LIM	RSET(k Ω)	MODE	limit point
L	4.02	1.5A	1.69A
	2.01	3A	3.38A

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				Date:	Thursday, October 28, 2021	Sheet 51 of 121

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]



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				Document Number	1.0
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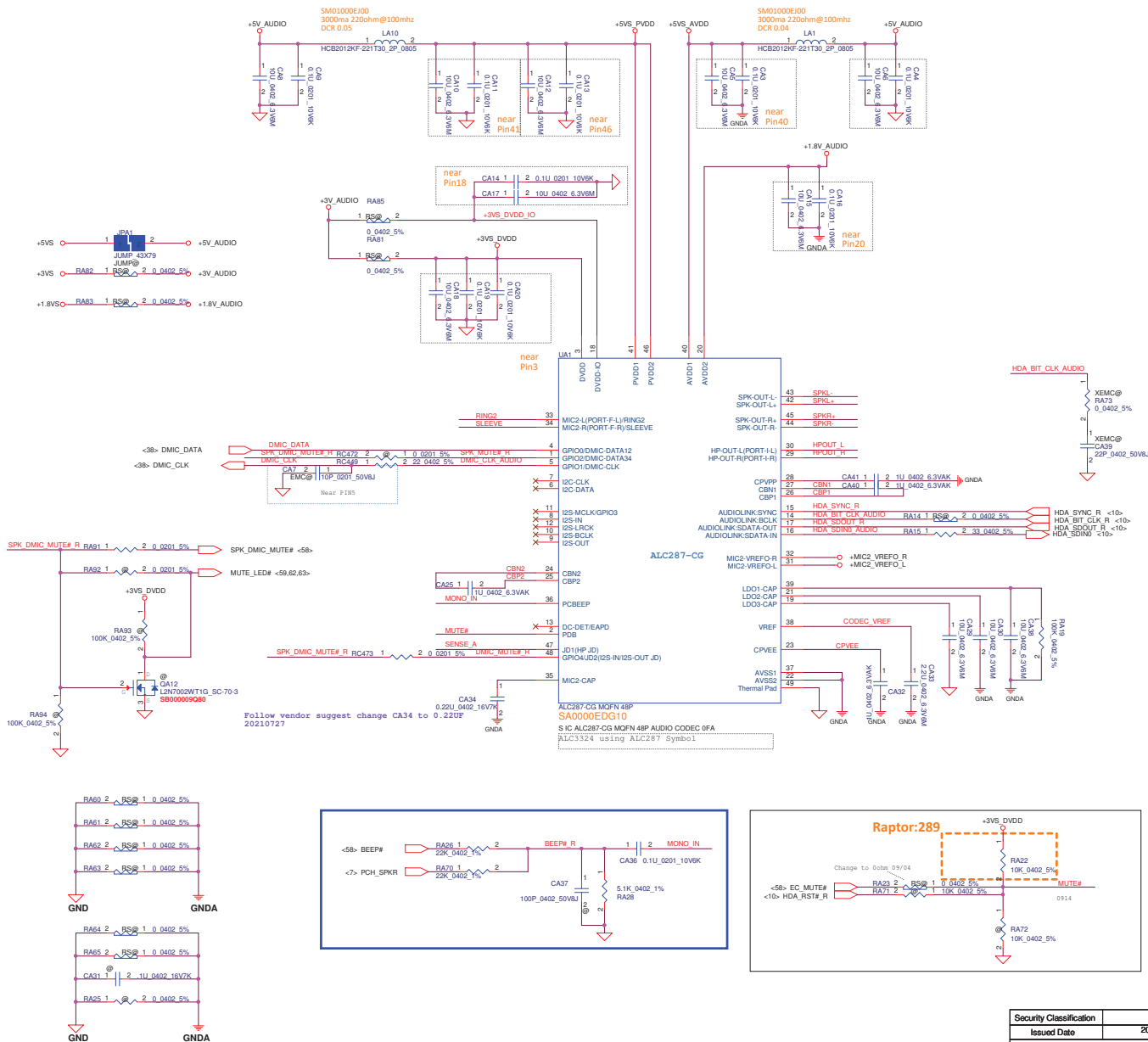
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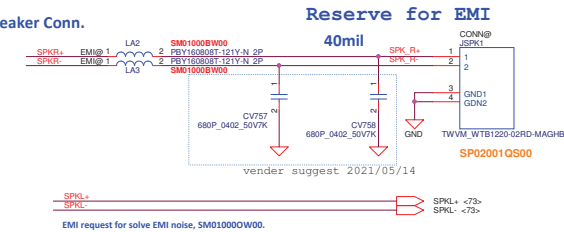
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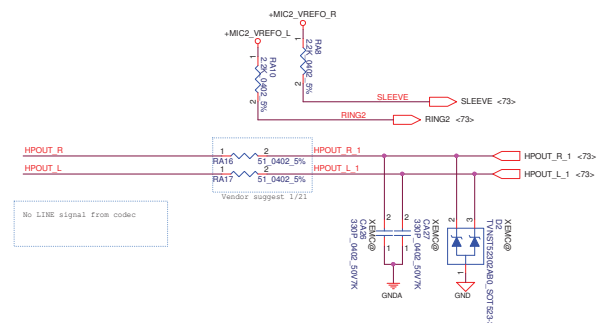
HD Audio Codec



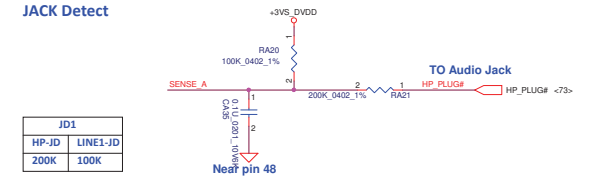
Int. Speaker Conn.



Headphone Out

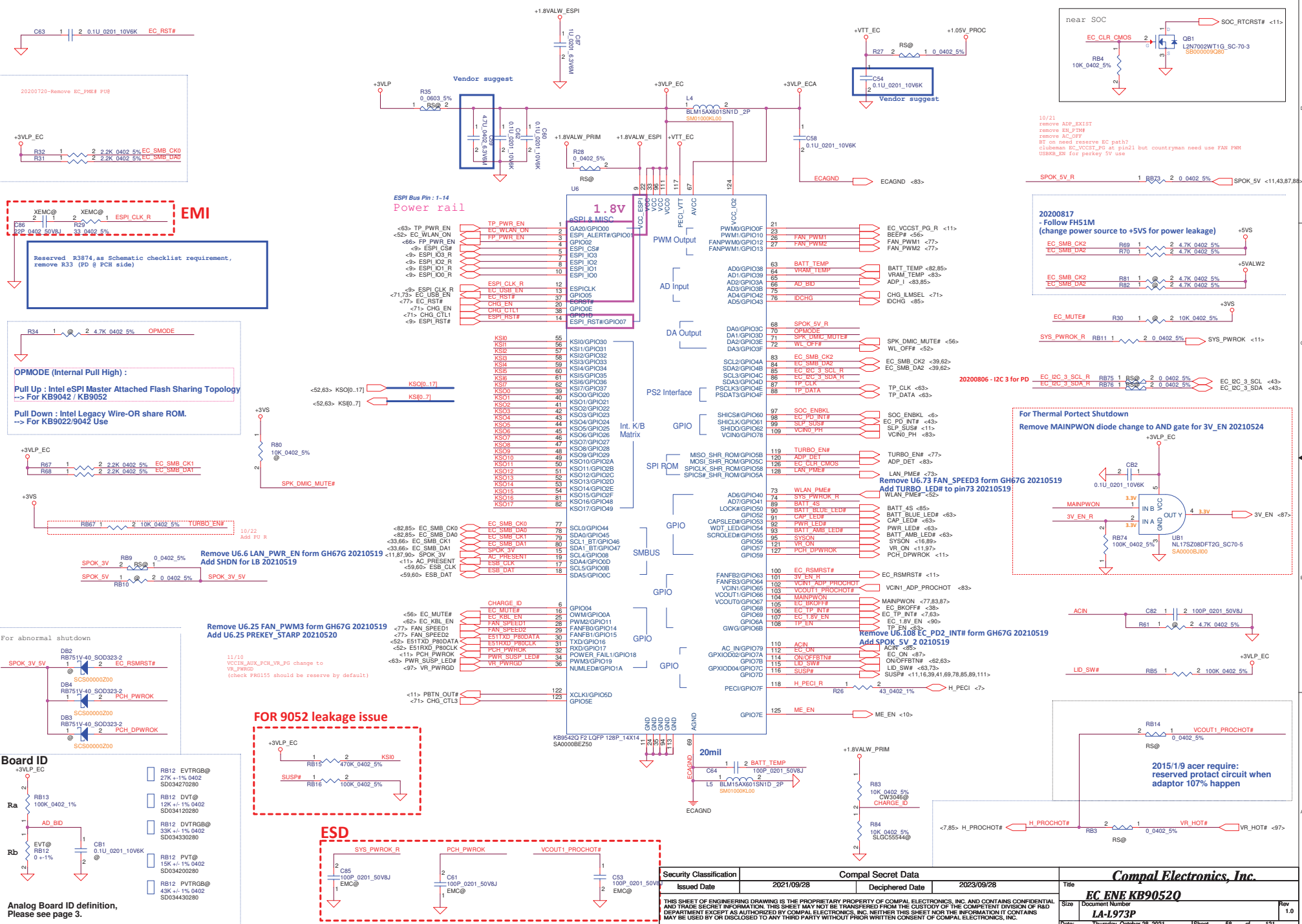


JACK Detect



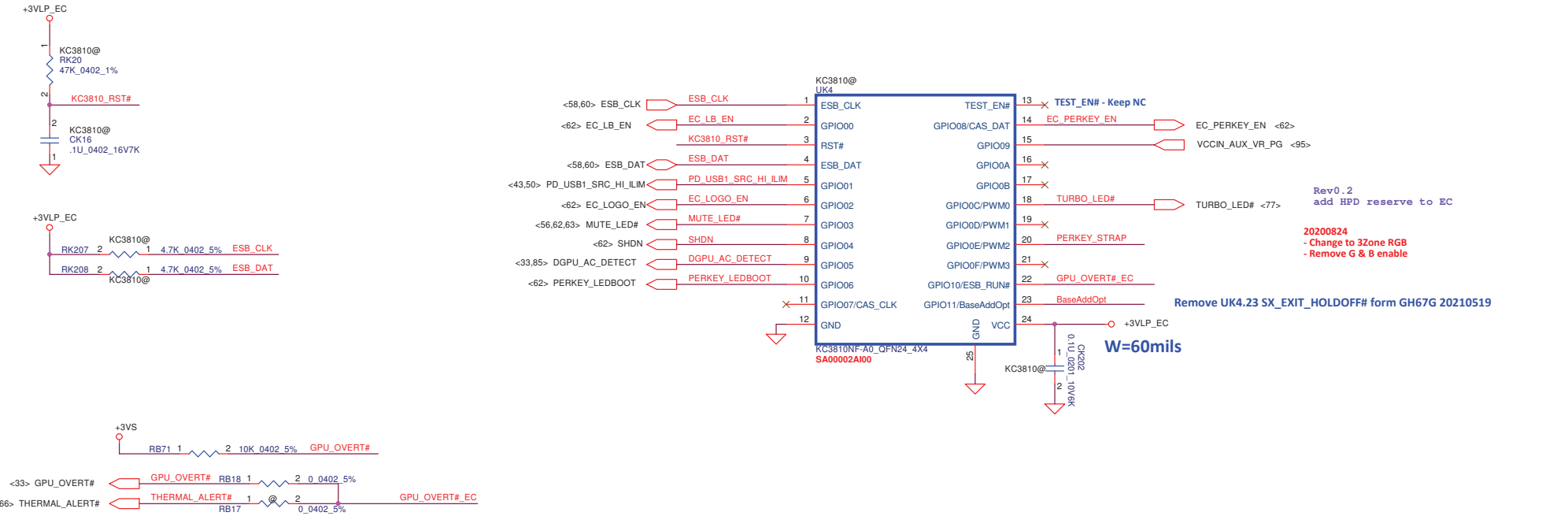
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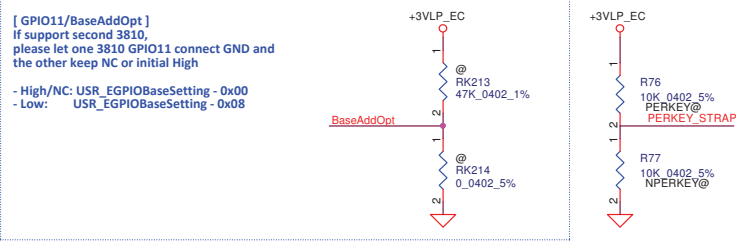


OMEN New ESB CLK&DAT for Extend I/O

*NMI_DBG#: is a debug pin for EC to
infrom BIOS after press hot key.

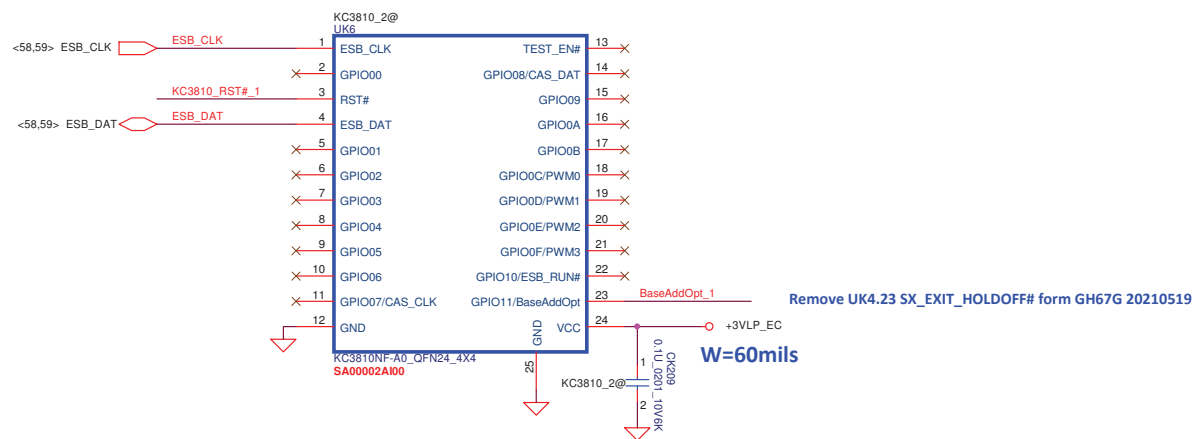
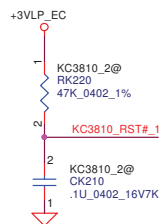


Need EC confirm



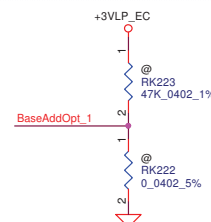
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*NMI_DBG#: is a debug pin for EC to inform BIOS after press hot key.



[GPIO11/BaseAddOpt]
If support second 3810,
please let one 3810 GPIO11 connect GND and
the other keep NC or initial High

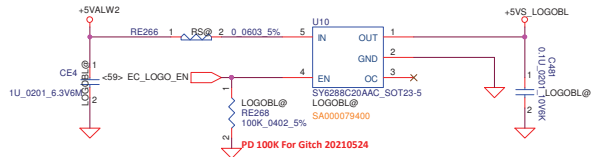
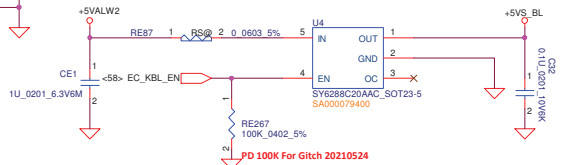
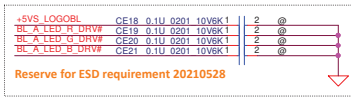
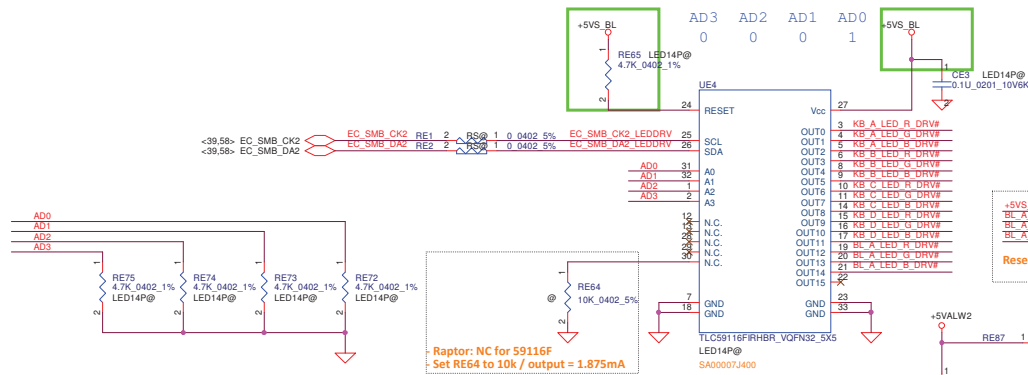
- High/NC: USR_EGPIOBaseSetting - 0x00
- Low: USR_EGPIOBaseSetting - 0x08



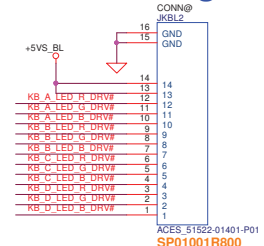
Security Classification		Compal Secret Data		Compal Electronics, Inc. Reserve for Secure & Reset IC		
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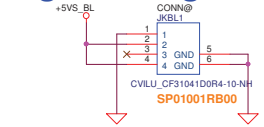
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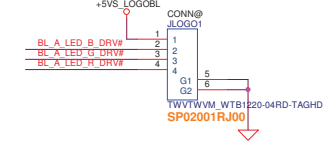
RGB KB Backlight Conn



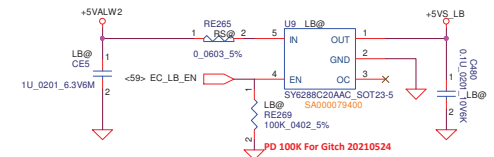
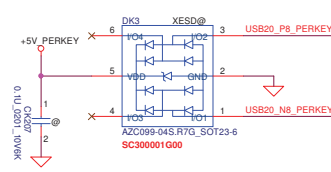
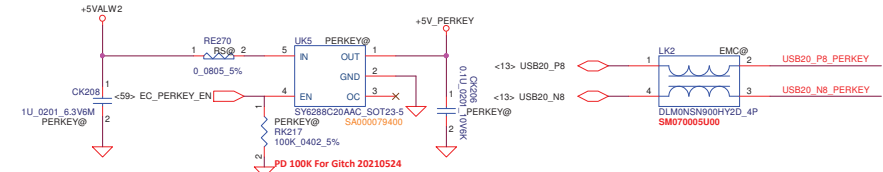
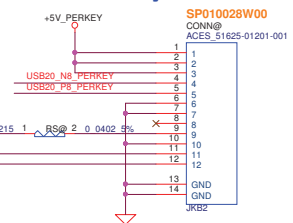
Single BackLight Conn



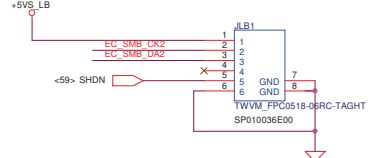
LOGO BackLight Conn



Per Key Conn.



LightBar Conn



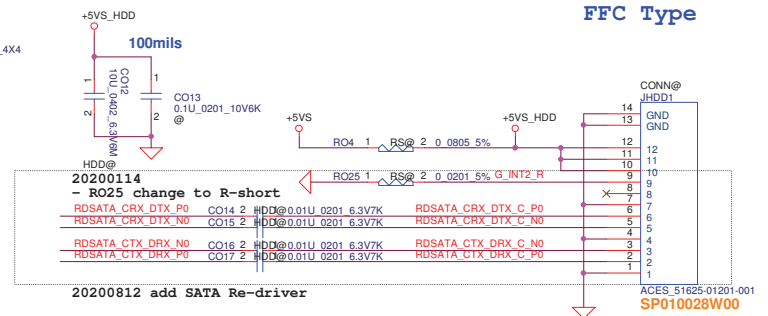
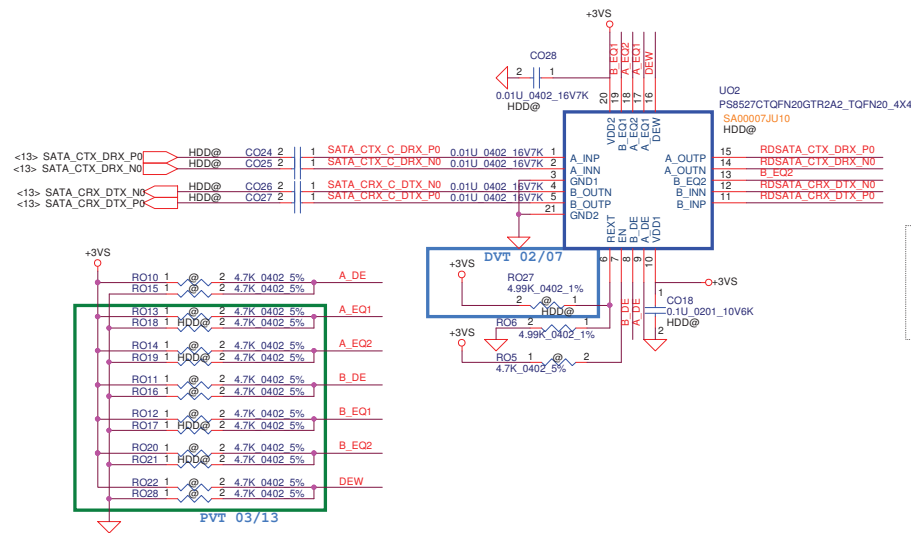
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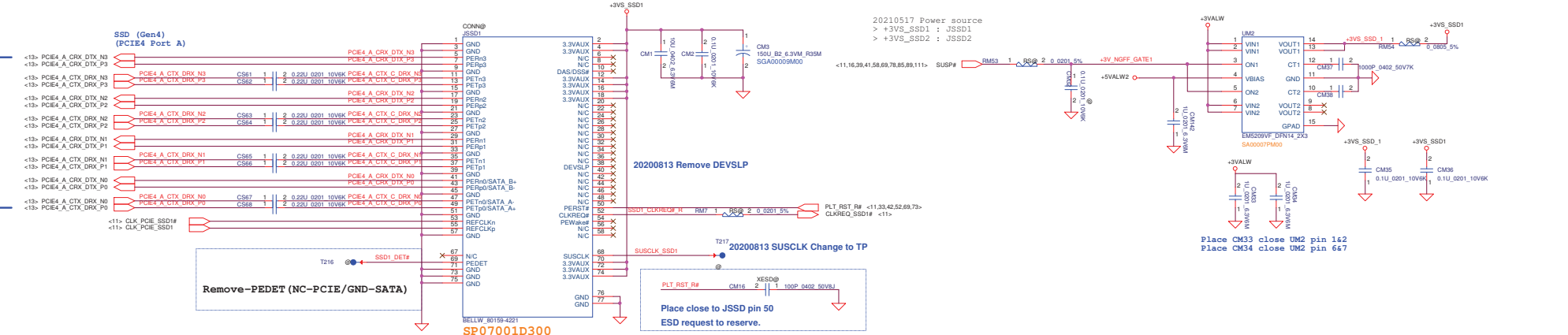
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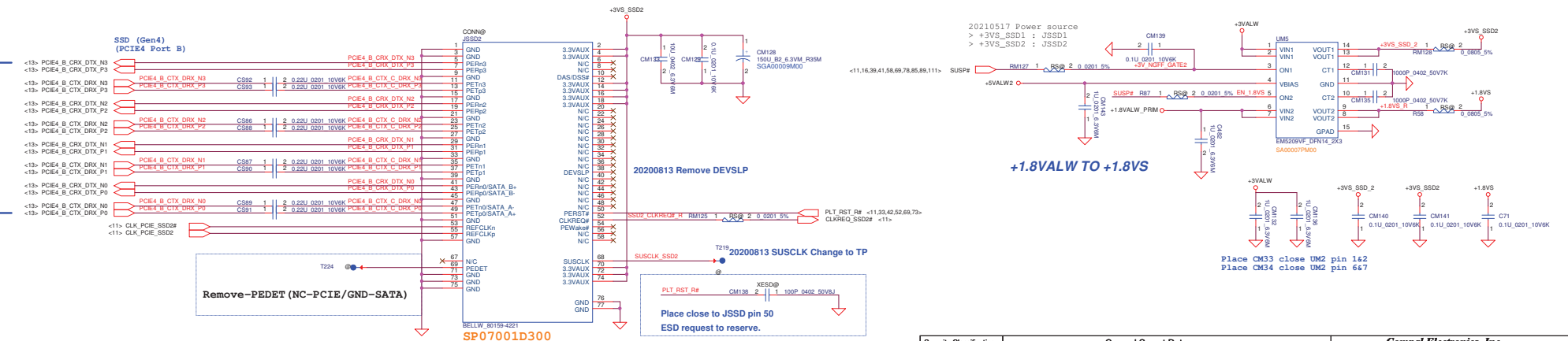


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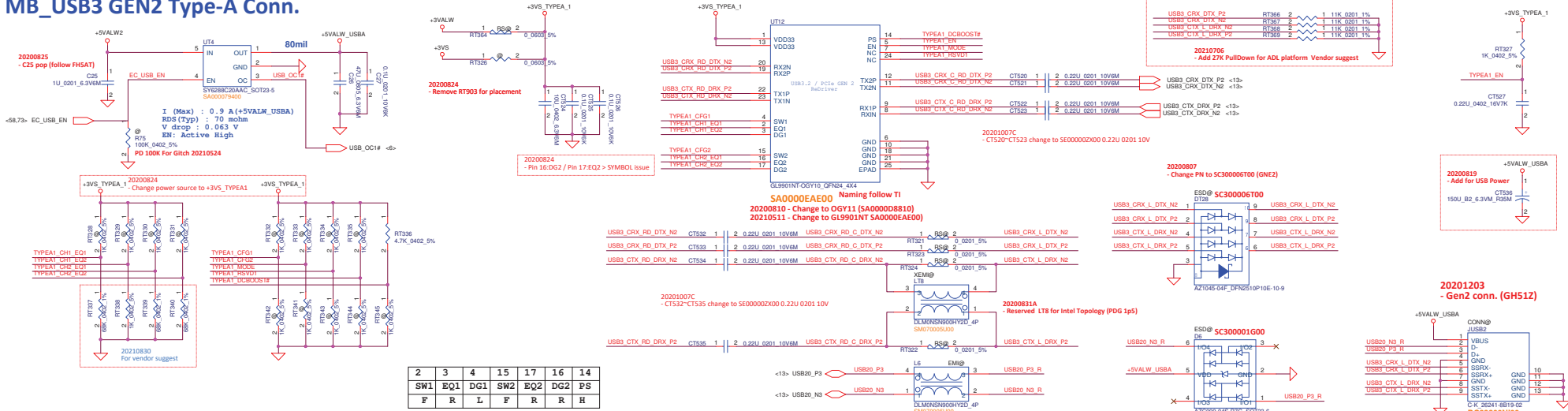
5/28 remove SSD port3



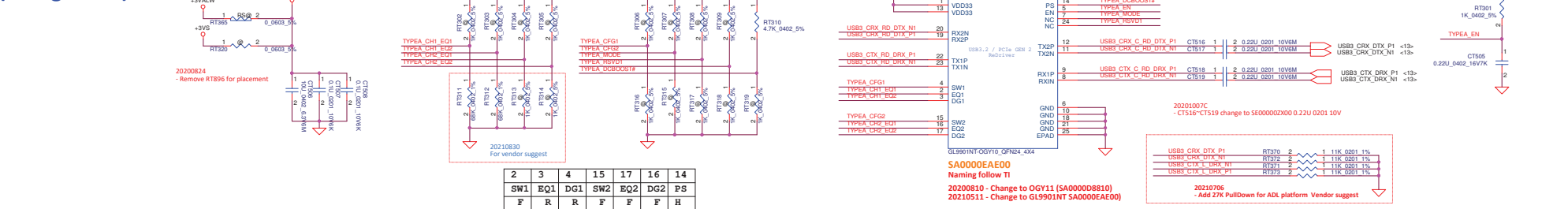
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				Date: Thursday, October 28, 2021	Sheet 70 of 121

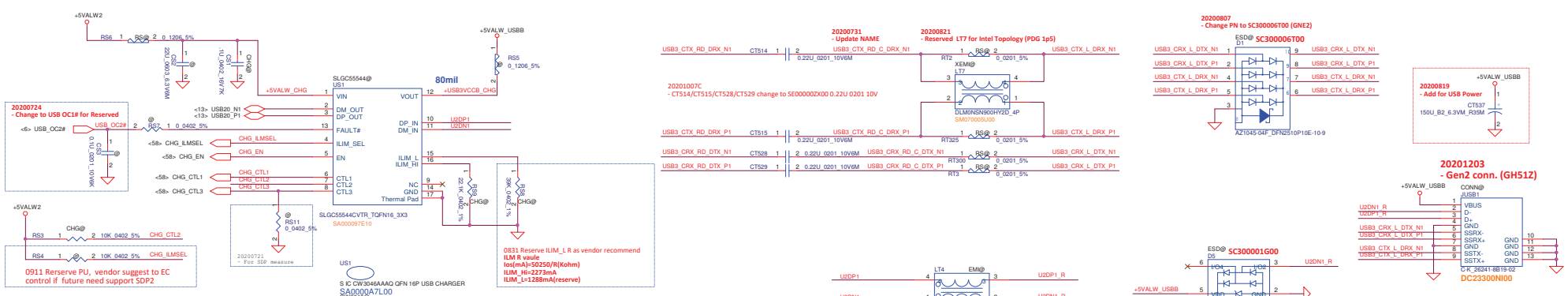
MB_USB3 GEN2 Type-A Conn.



MB_USB3 GEN2(W Re-verter) Type-A Conn. (Charge Port)



USB Host Charger



USB Host Charger Truth Table

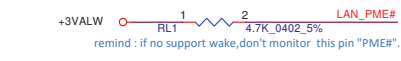
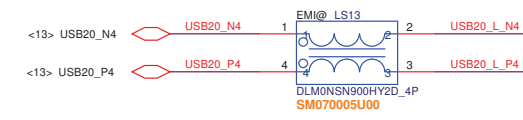
CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

22Z X76CW@
ALT. GROUP PARTS B1 C1 30346 HS14
X76869BOLCJ
22Z X76LSQG@
ALT. GROUP PARTS B1 C1 30346 HS14
X76869BOLCK

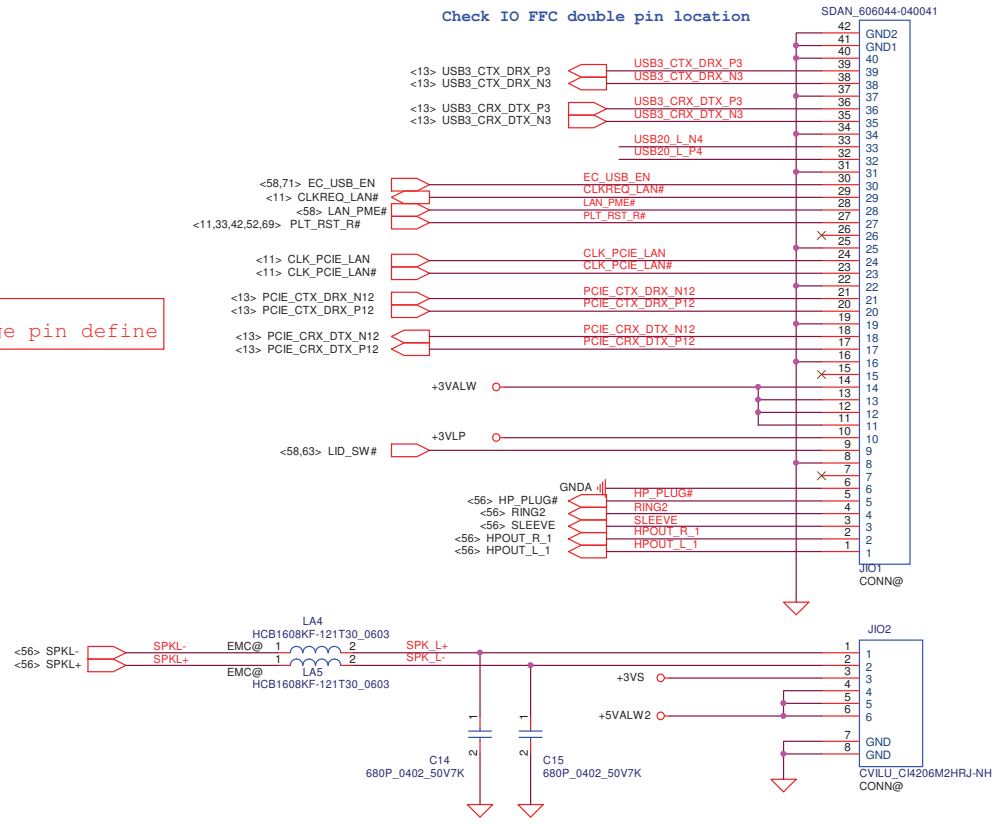
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IO/B CONN



0603
- IO_B change pin define



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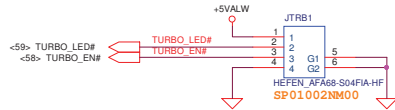
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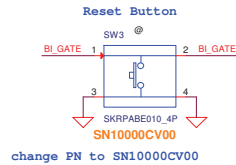
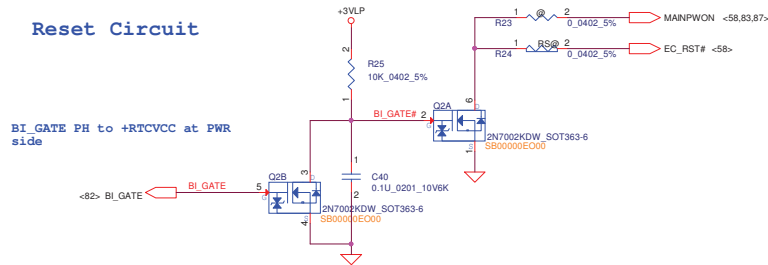
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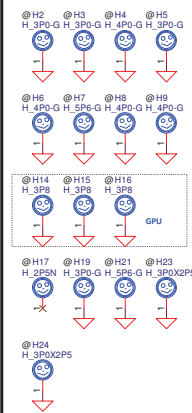
Turbo Key



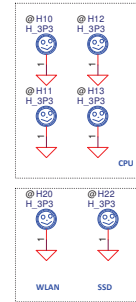
Reset Circuit



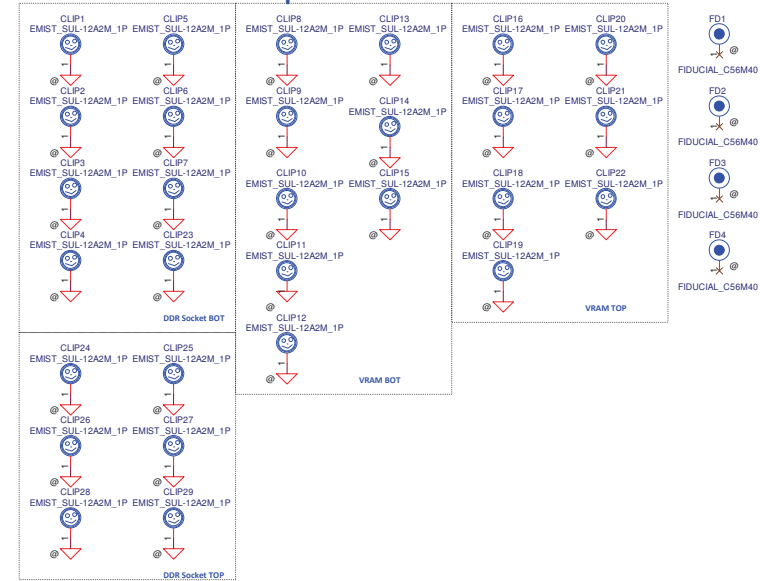
Screw Hole



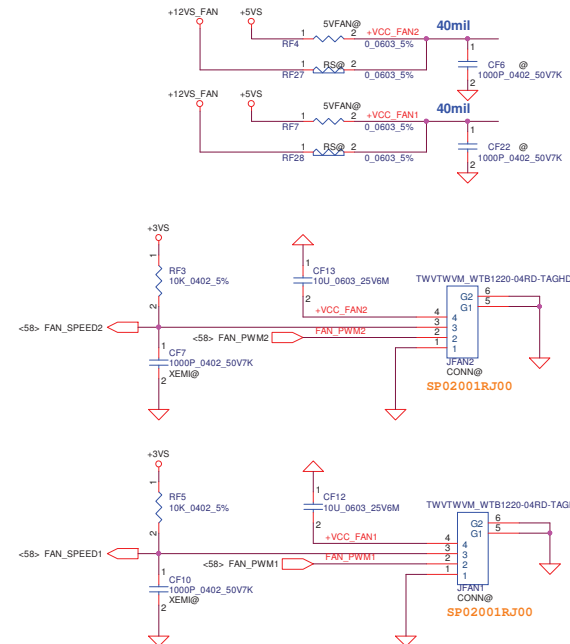
Stand OFF



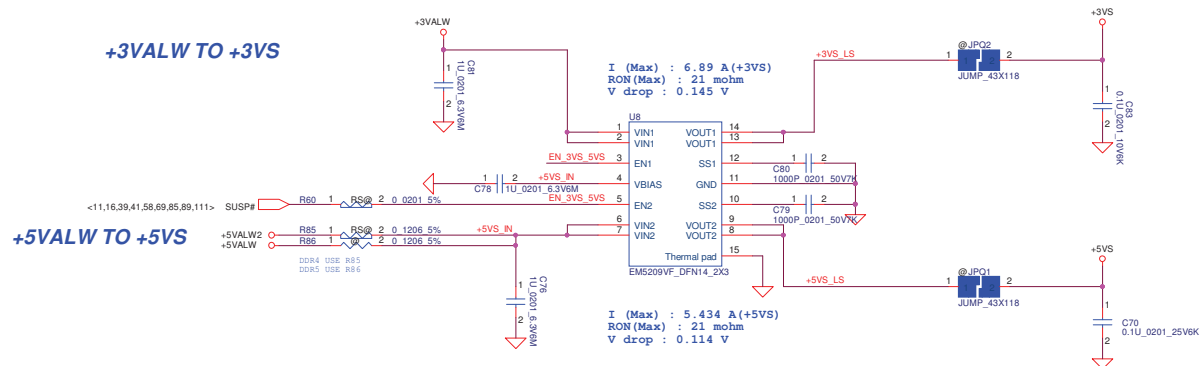
Clips



FAN Conn



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20210610
- Move +1.8VALW to +1.8VS to page 69

20200717
- Remove VGA Power sequence

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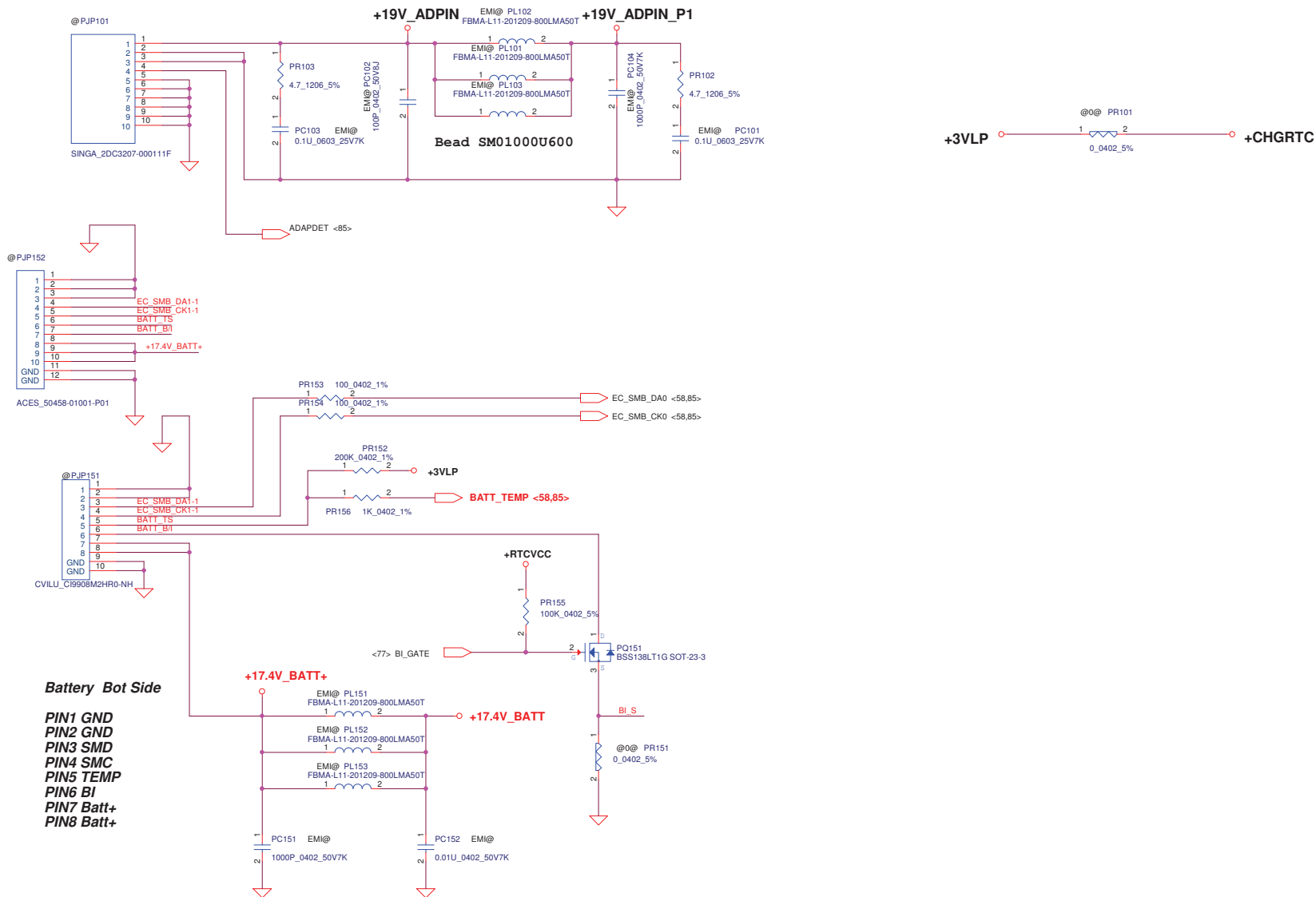
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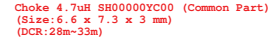
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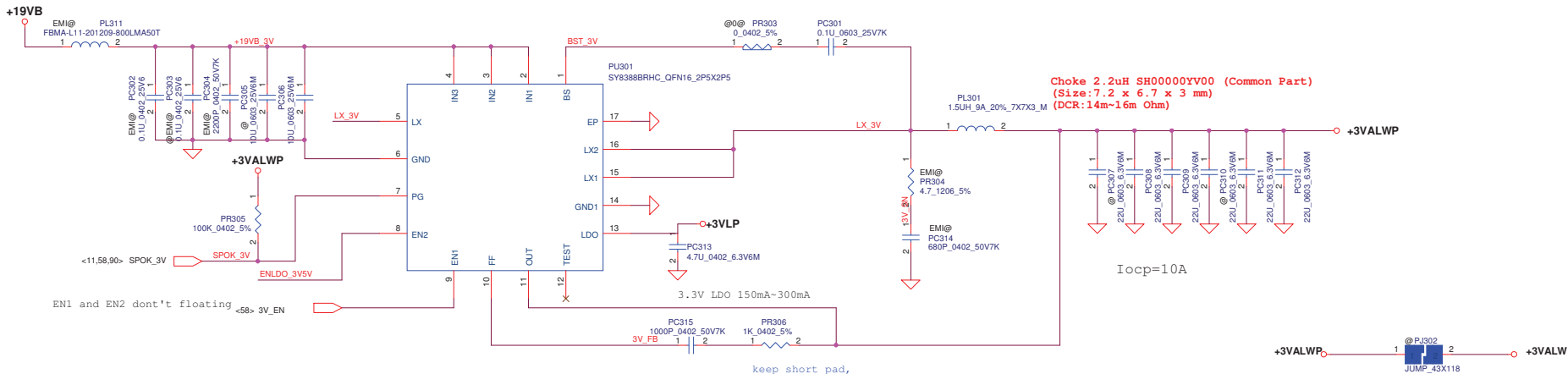
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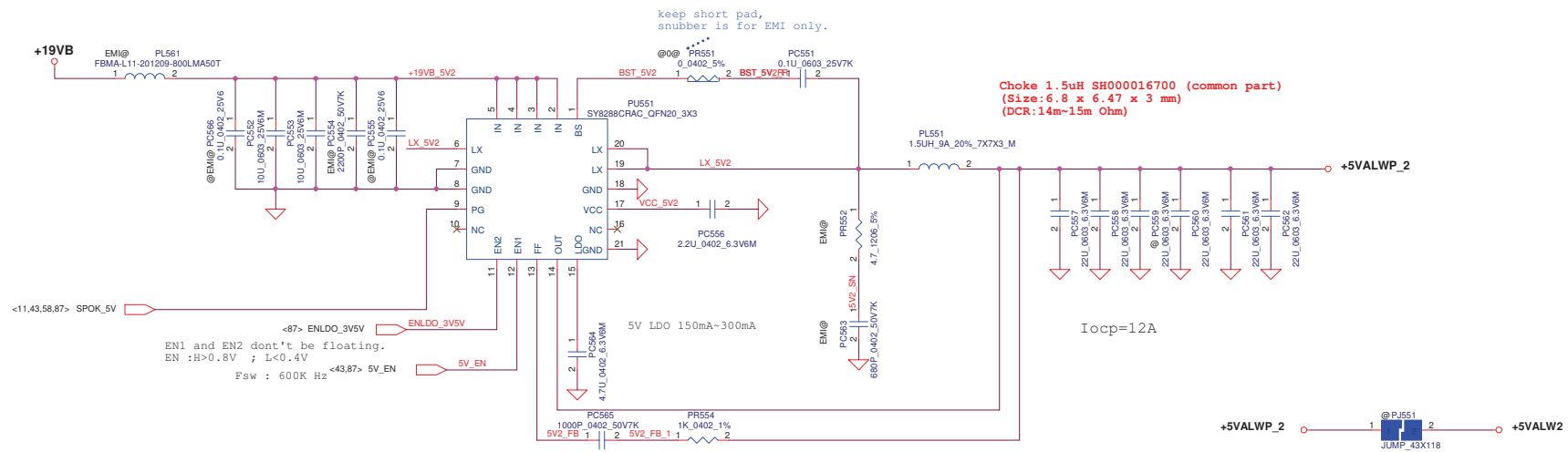


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Module model information
TPS51486_V1.mdd
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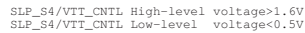


Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

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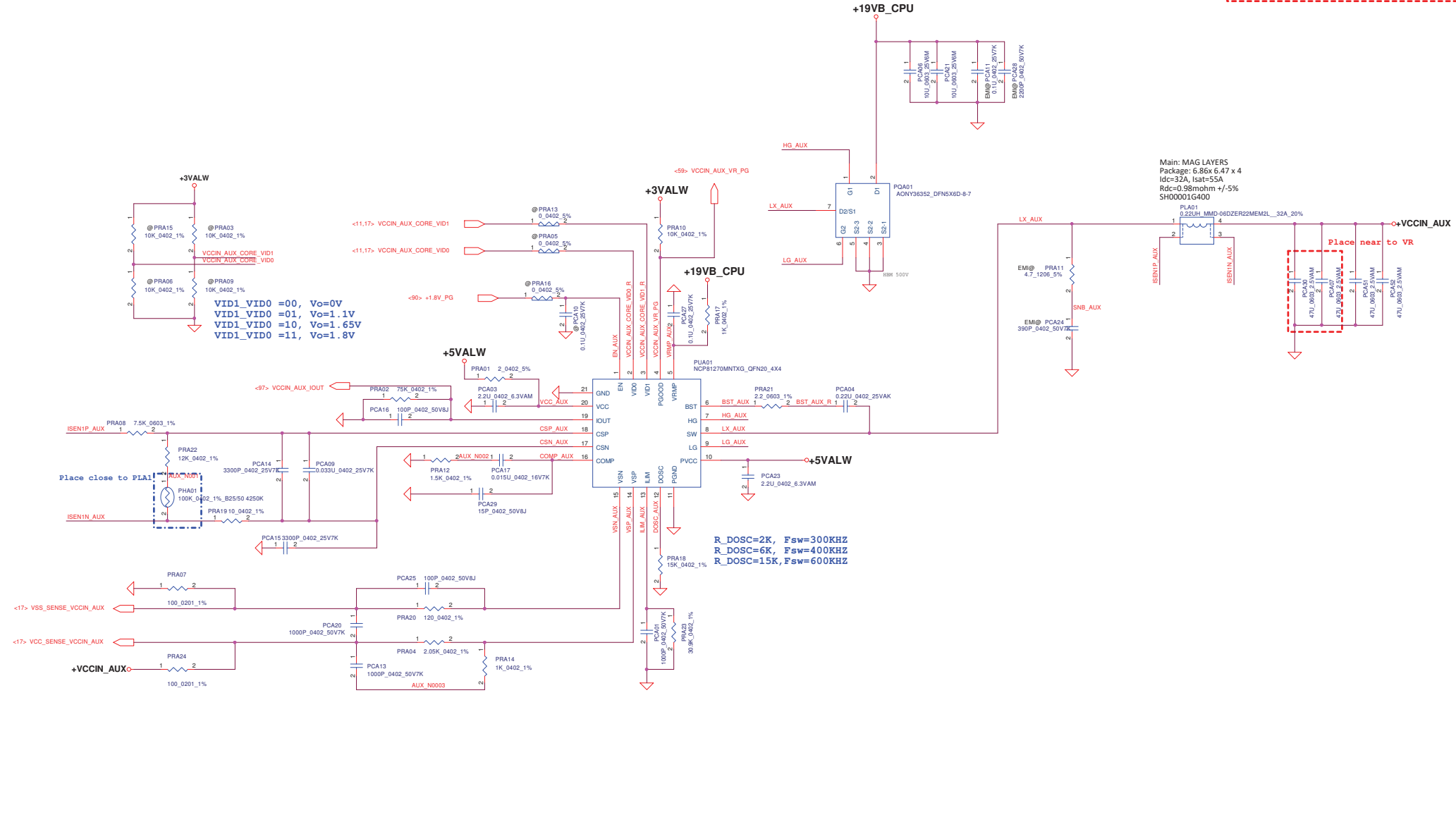
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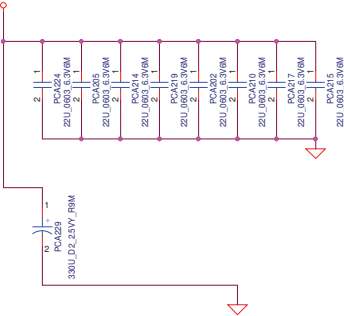
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Main Func = +VCCIN_AUX

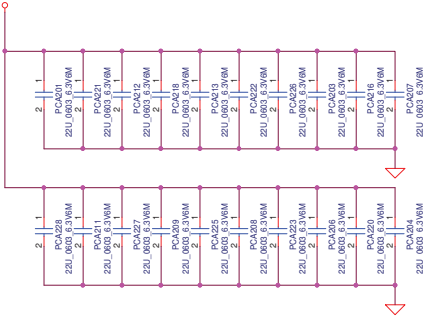
+VCCIN_AUX
Vout 1.8V
IPL2 (TDC) = 17A
Peak Current = 34.2A (ICCMAX)
OCP: 44.6 A
OVP: VID+0.36V (max 2V)
FSW= 600KHz



CPU Primary Side
+VCCIN_AUX



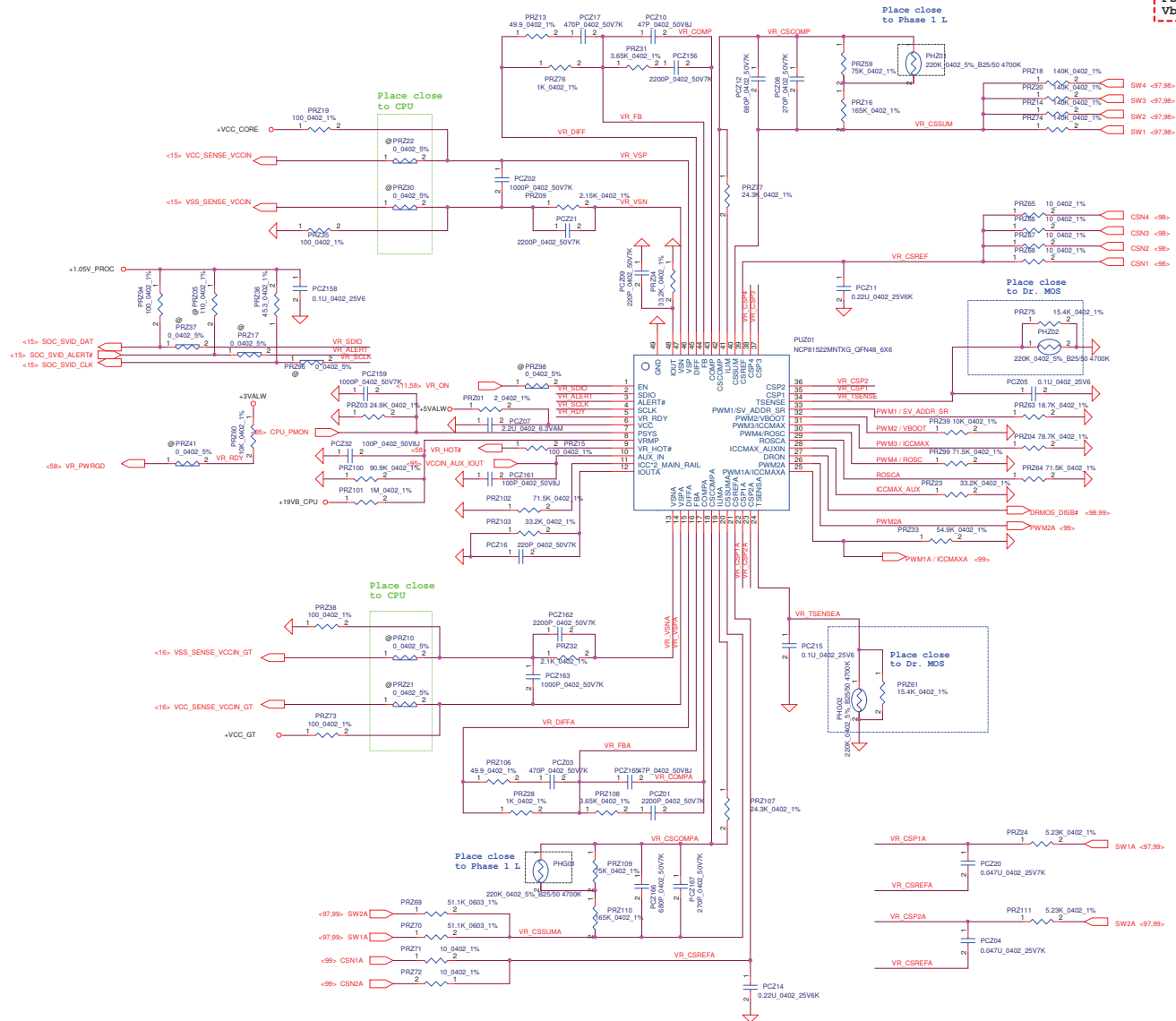
CPU Secondary side
+VCCIN_AUX



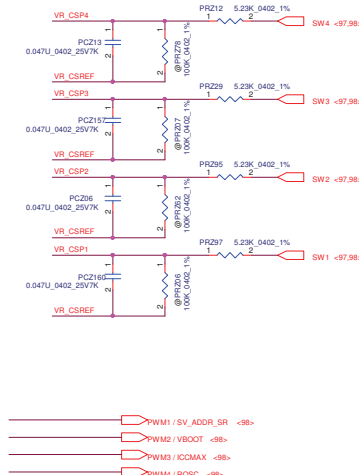
Main Func = CPU (IA/GT)

```
+VCC_CORE
IPL2 = 93A
Peak Current = 160A(ICCmax)
DC Load line: 2.1mohm
AC Load line: 2.1mohm
Current limit =200A(OCp)
OVP: VID+0.36V
FSW= 540K Hz
Vboot: 0V
```

```
+VCC_GT
IPL2 = 30A
Peak Current = 50A(ICCmax)
DC Load line: 3.1mohm
AC Load line: 3.1ohm
Current limit =65A(OCP)
OVP: VID+0.36V
FSW= 540K Hz
Vboot: 0V
```

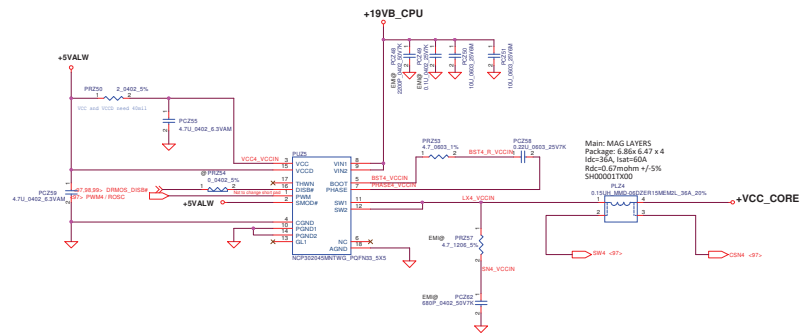
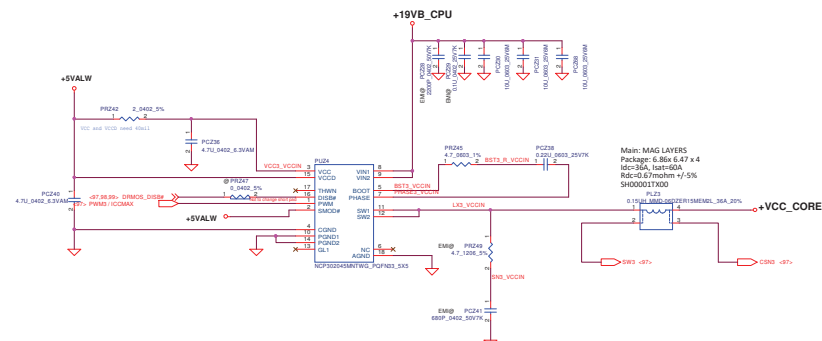


PHASE DETECTION



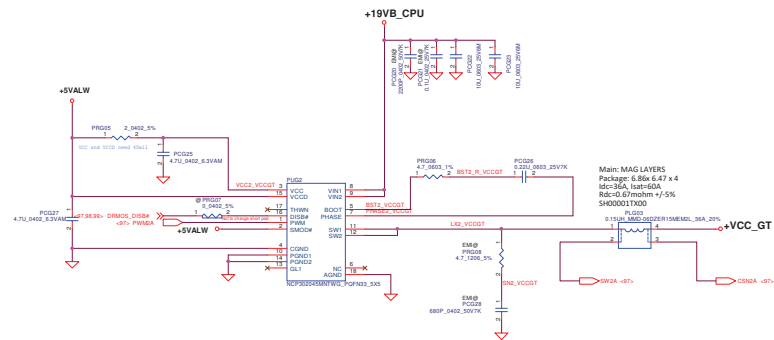
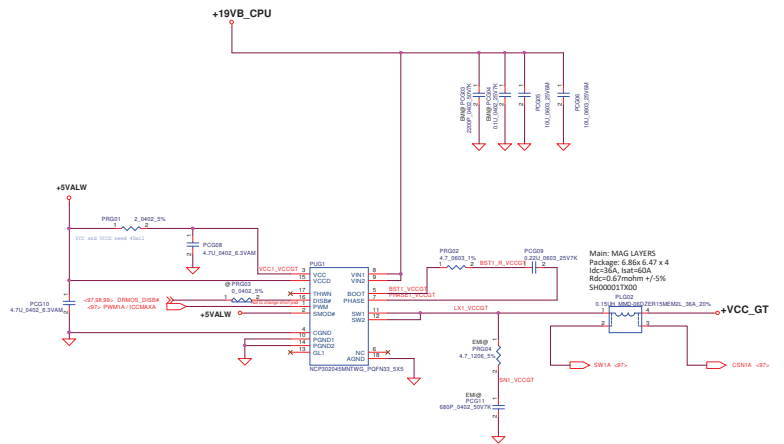
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```
+VCCORE
IPL2 = 93A
Peak Curren = 160A(ICCmax)
DC Load line: 2.1mohm
AC Load line: 2.1mohm
Current limit =A(OCP)
FSW= K Hz
```



Main Func = +VCCGT

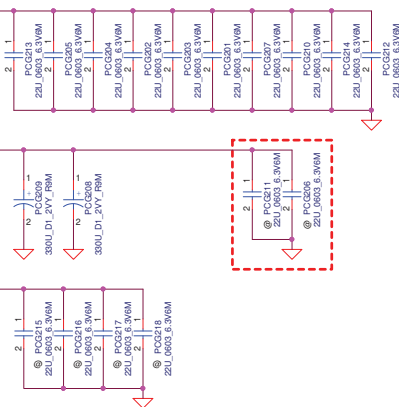
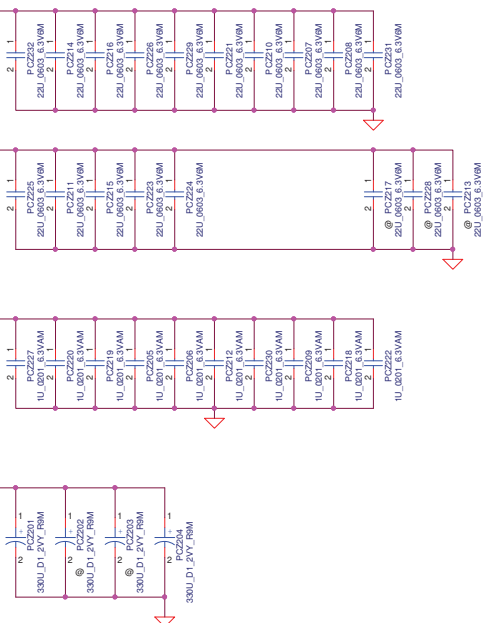
+VCCGT
IPL2 = 30A
Peak Current = 50A (ICmax)
DC Load line: 3.1mohm
AC Load line: 3.1ohm
Current limit =A (CCP)
FSW= K Hz



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Main Func = +VCCIN DECOUPLING



Compal
+VCCGT Output CAP :

CPU primary side:
330uF_B2 *3pcs
22uF_0603_low-noise *16pcs

CPU Secondary side:
22uF 0603 low-noise *7pcs

Compal(follow PDG)
+VCC_GT Output CAP :

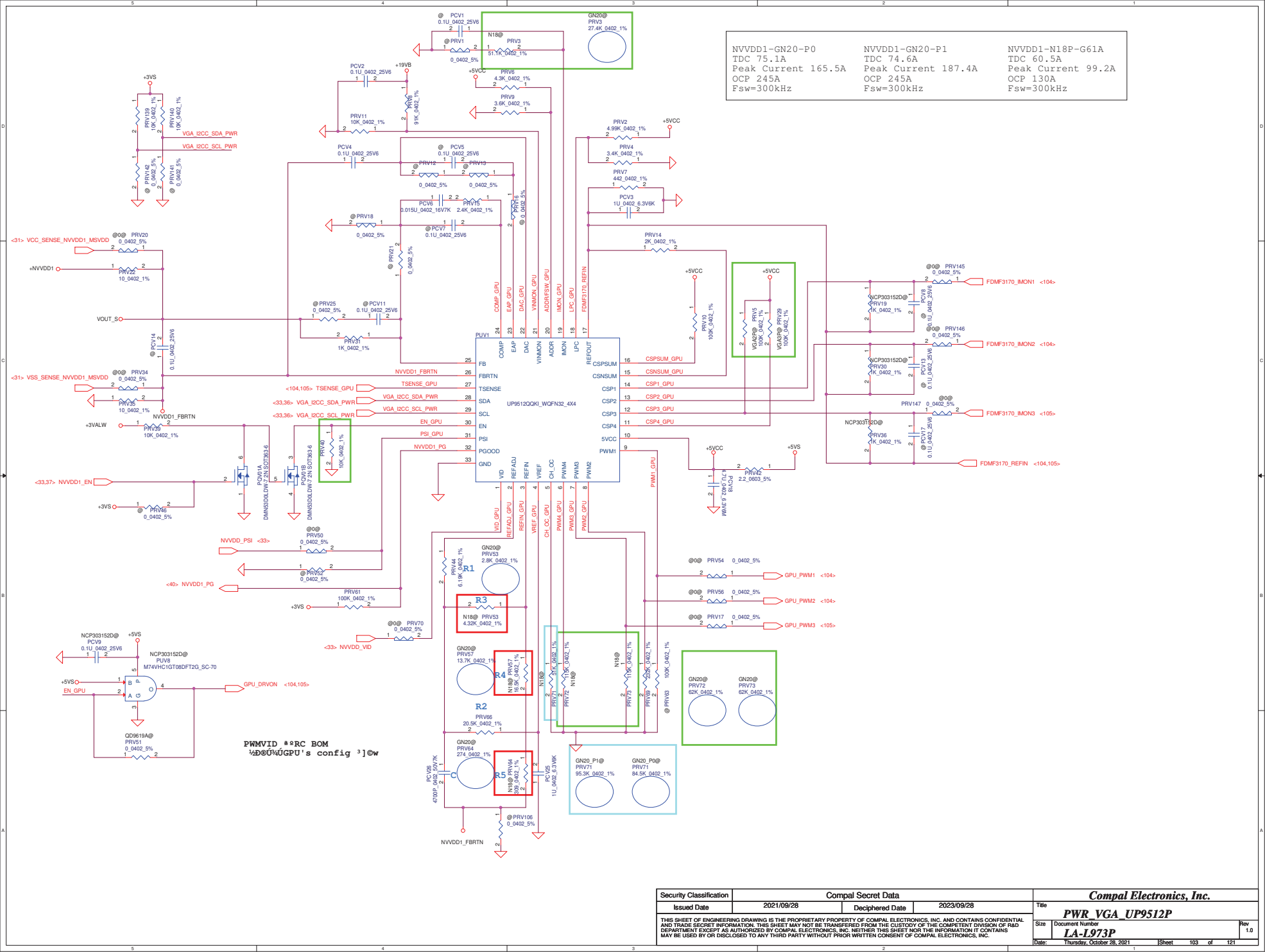
```
CPU Primary Side:
330uF_B2 *3pcs
47uF_0603_low-noise *7 pcs
22uF_0603_low-noise *2 pcs
```

```
CPU Secondary side:
22uF_0603_low-noise *6 pcs
10uF_0603_low-noise *2 pcs
```

Security Classification	Compal Secret Data			Compal Electronics, Inc. PWR CPU Decoupling CAP		
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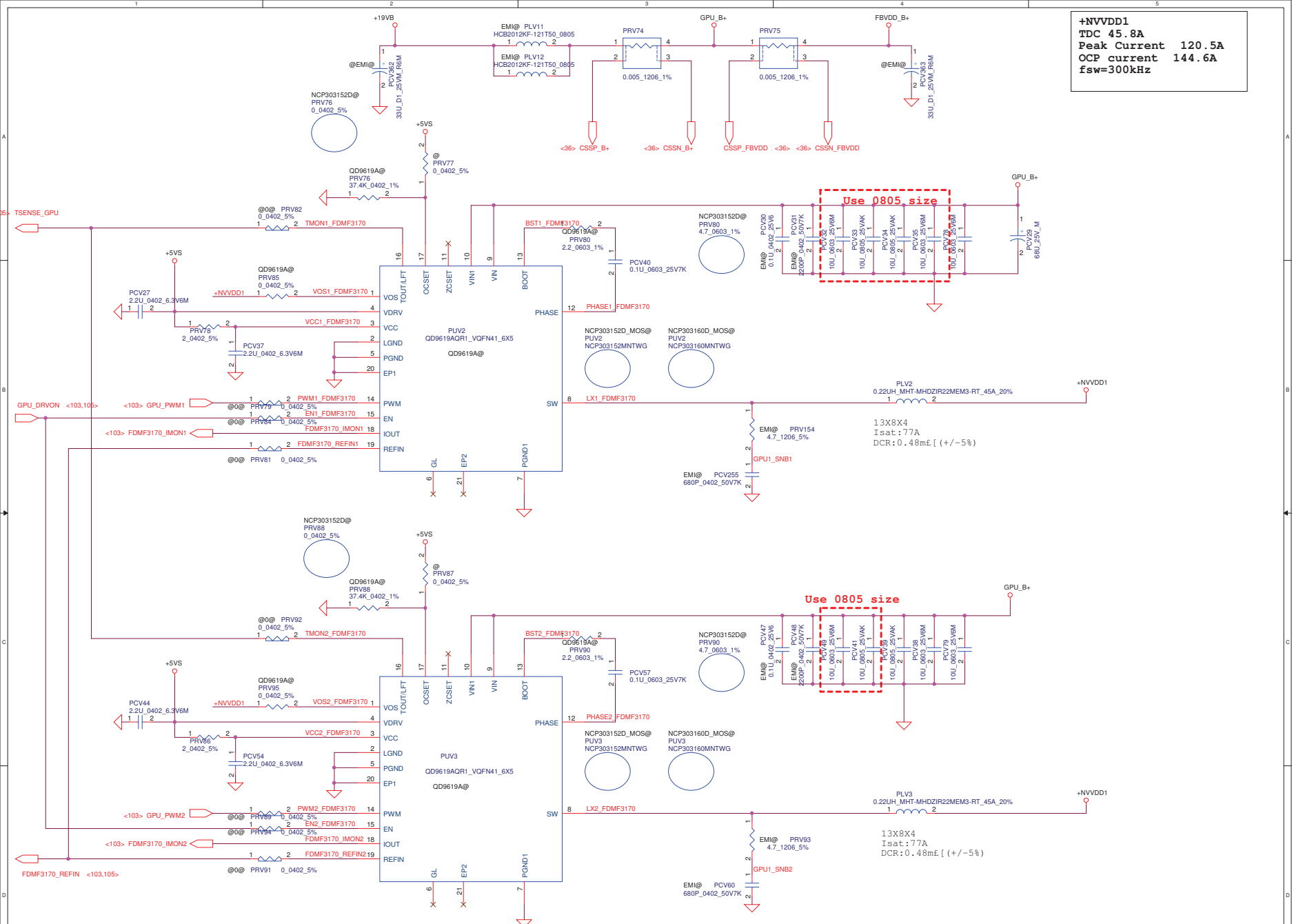
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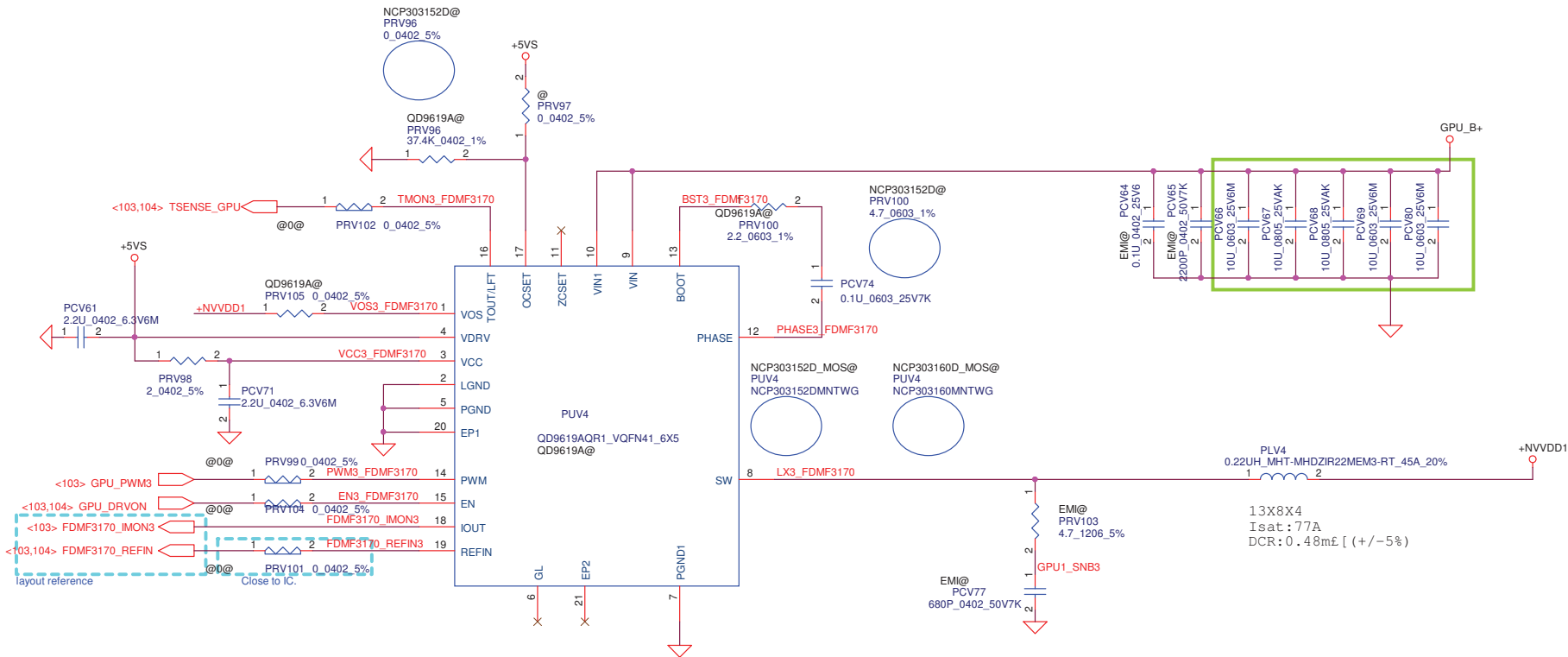
NVVDD1-GN20-P0	NVVDD1-GN20-P1	NVVDD1-N18P-G61A
TDC 75.1A	TDC 74.6A	TDC 60.5A
Peak Current 165.5A	Peak Current 187.4A	Peak Current 99.2A
OCV 245A	OCV 245A	OCV 130A
Fsw=300kHz	Fsw=300kHz	Fsw=300kHz

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+NVVDD1
TDC 45.8A
Peak Current 120.5A
OCP current 144.6A
fsw=300kHz



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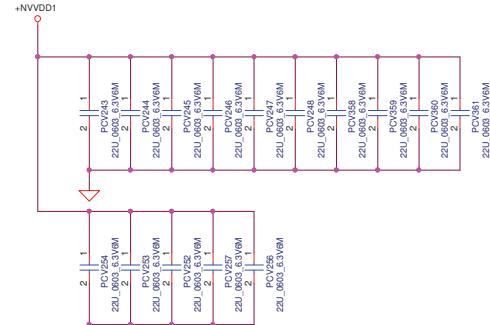
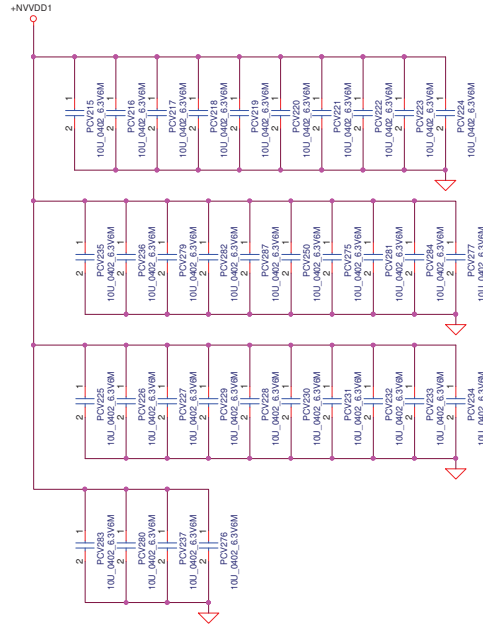
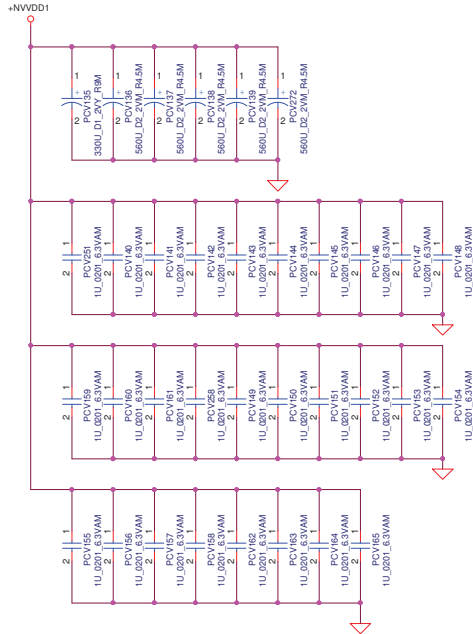


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```
+NVVDD
560uF X 6
22uF_0603 X 15
10uF_0402X 34
1uF_0201 X 28
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