

HuaQin Confidential


NB8511/12_M/B Schematics Document

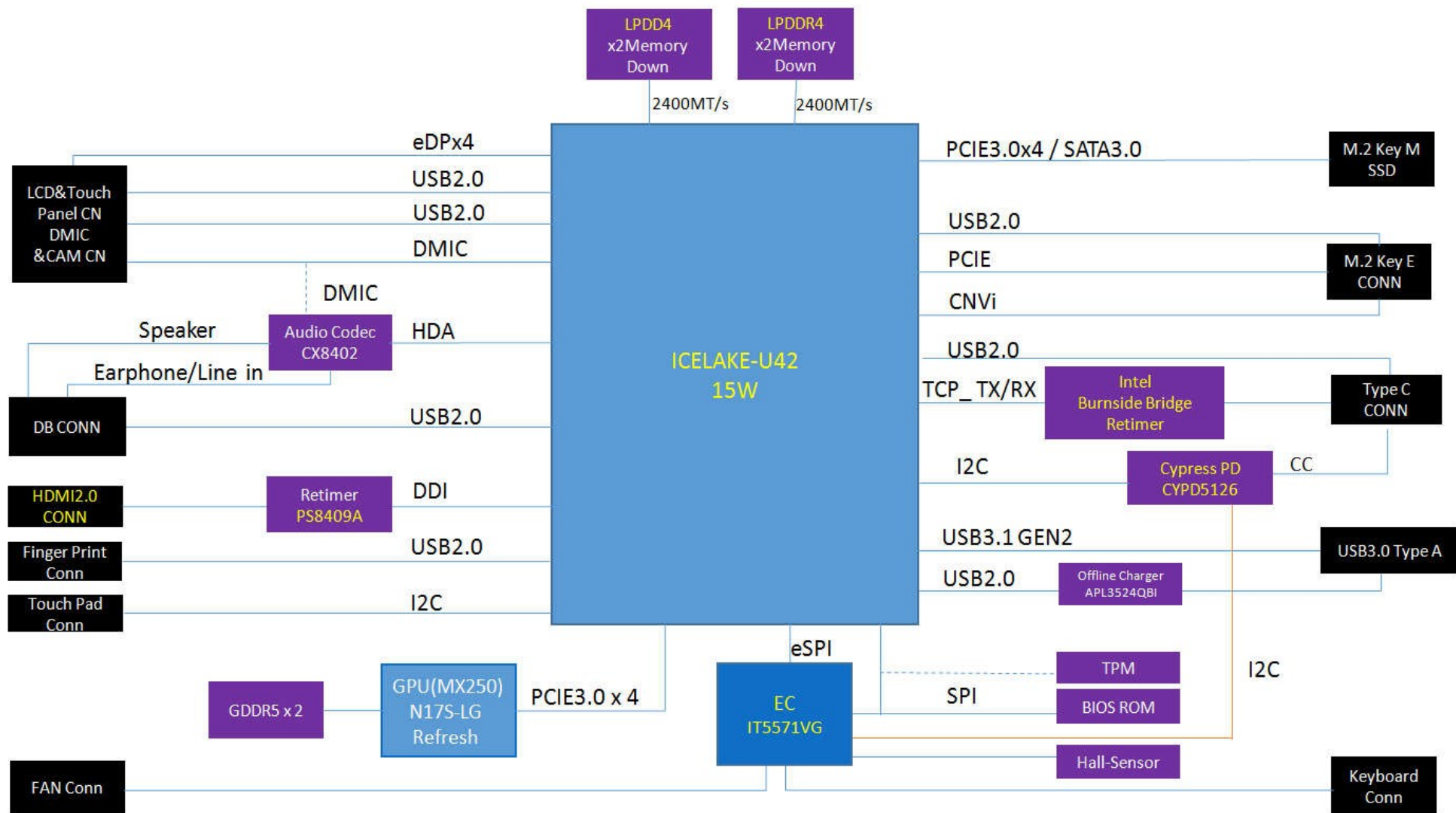
Intel ICL Lake U-Processor with LPDDR4

REV1.0

2019-02-01

<http://www.repair1.ru/>

Author	Leo.Liu & Payne.Zhang	 Huaqin Telecom Technology Com.,Ltd.		
Reviewer	Nelosn.Hai & Nemo.Jiang	Page name: Cover page		
Approver	Lobo_Fan	Size: A4	Project Name: NB8511	REV: V1.0
		Date: Monday, July 15, 2019	Sheet: 1	of 72



<http://www.repair1.ru/>

MEM ID

HW_ID3	HW_ID2	HW_ID1	HW_ID0	Description	Total
0	0	0	0	SAMSUNG LPDDR4 3733 1GB K4F8E304HB-MGCJ LF+HF D20	4GB
0	0	0	1	HYNIX LPDDR4 3733 1GB H9HCNNN8KUMLHR-NME LF+HF DDP	4GB
0	0	1	0	MICRON LPDDR4 4266 2GB MT53E512M32D2NP-046 WT:E LF+HF Z11N	8GB
0	1	0	0	HYNIX LPDDR4 3733 2GB H9HCNNNBPUMLHR-NME LF+HF DE	8GB
0	1	0	0		16GB
1	0	0	0	HYNIX LPDDR4X 4266 4GB H9HCNNNCPMALHR-NEE LF+HF QDP	
				4x 16Gb(reserve)	

GPU ID

HW_ID5	HW_ID4	Description	
		N17-LG-Refresh	N17-LG
0	0	NC	NC
1	0	Mount	
1	1		Mount

KB BL ID

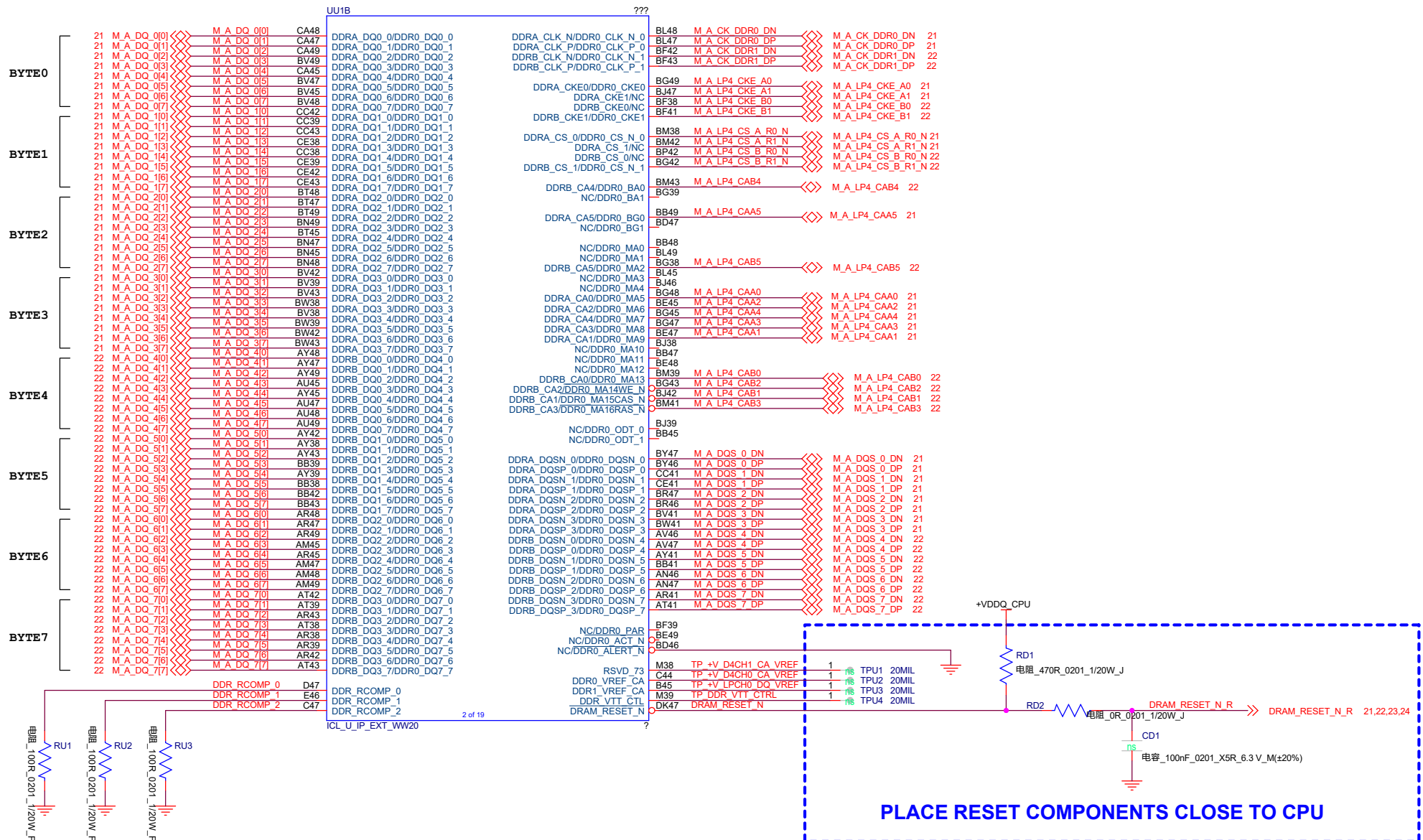
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1	Keyboard Backlight

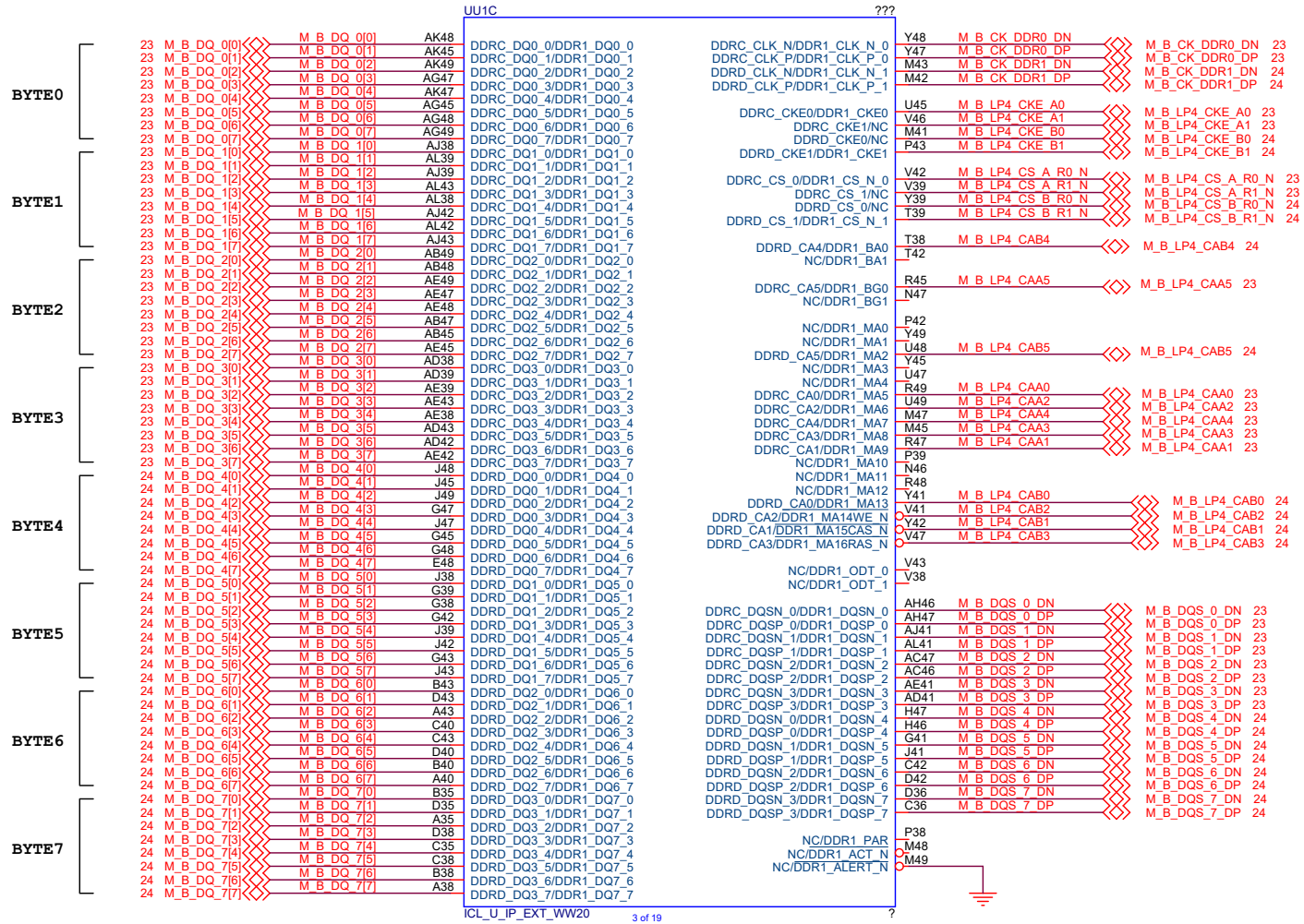
Reserve ID

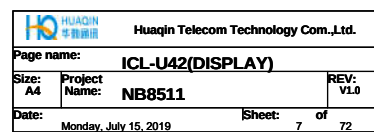
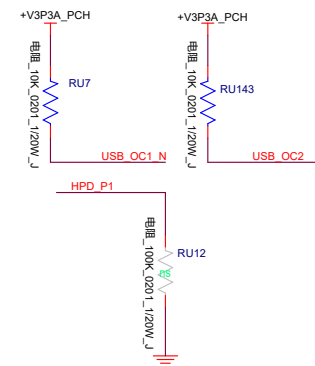
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1	Reserve

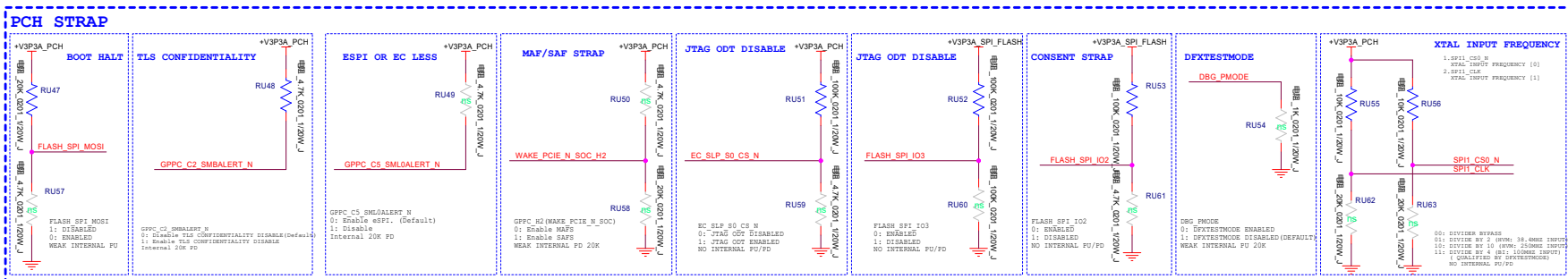
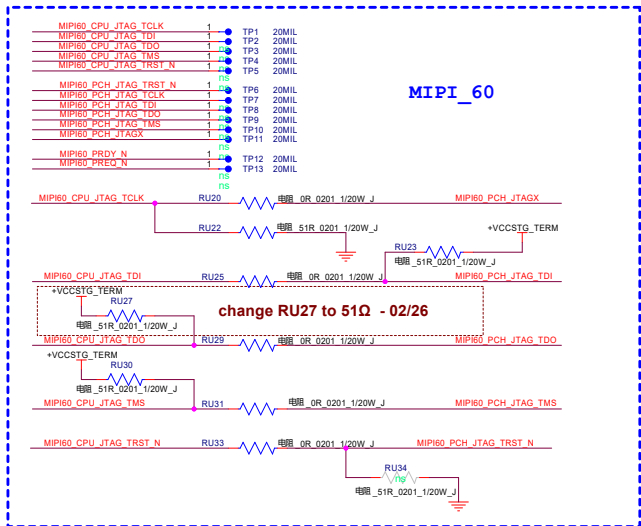
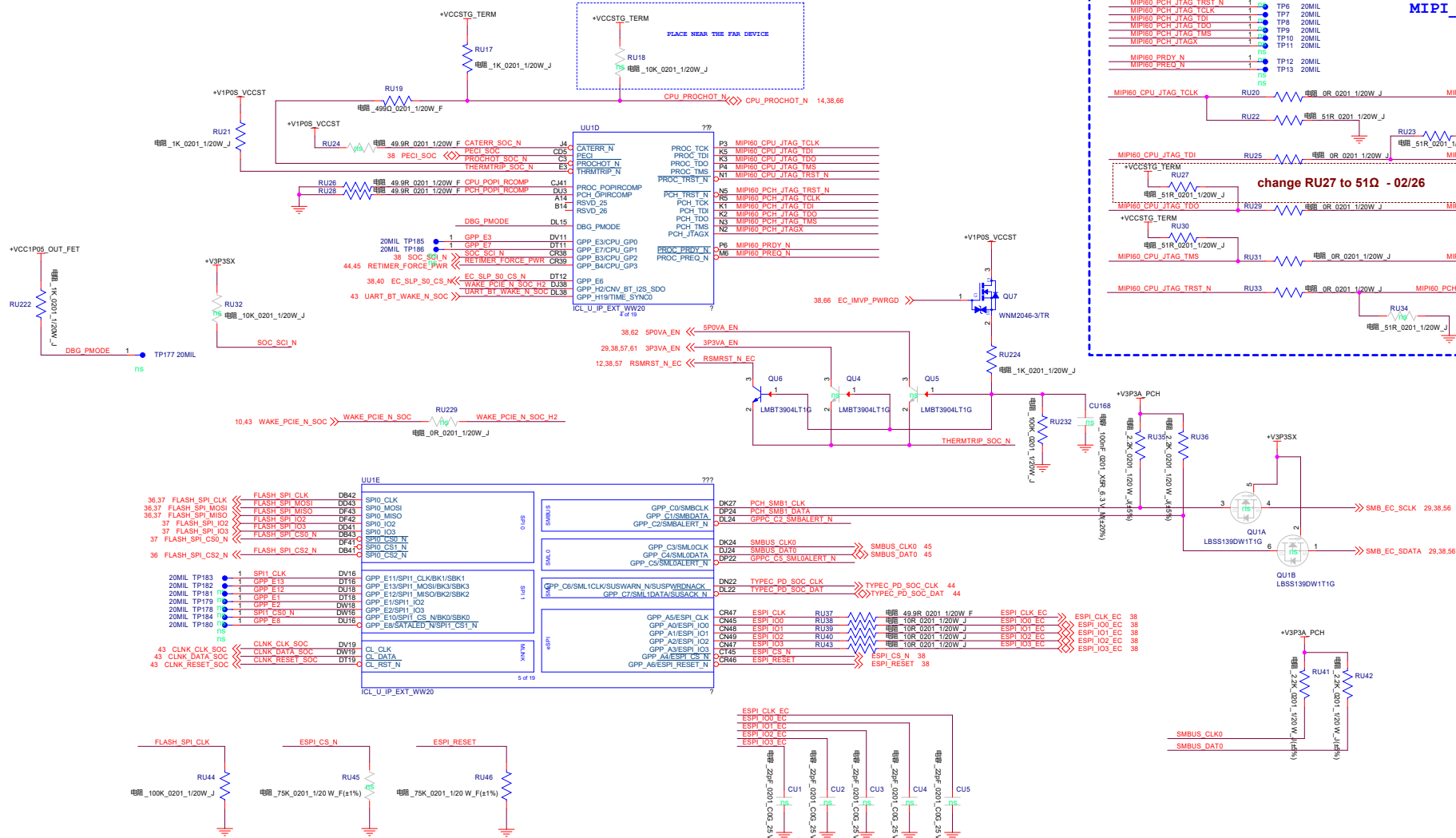
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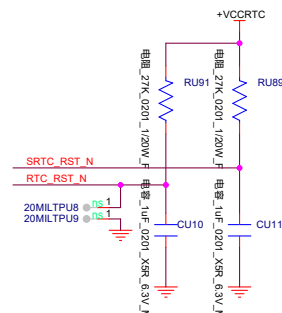
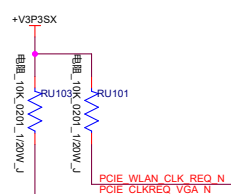
CHA



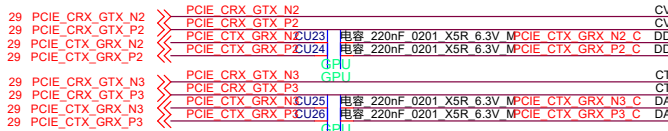






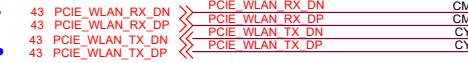


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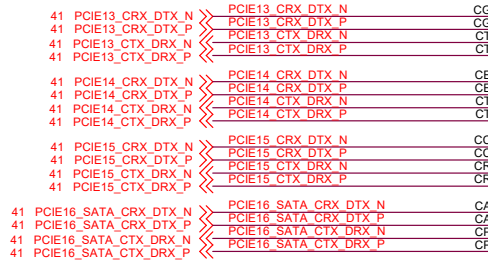


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WLAN



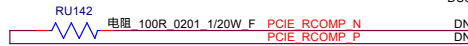
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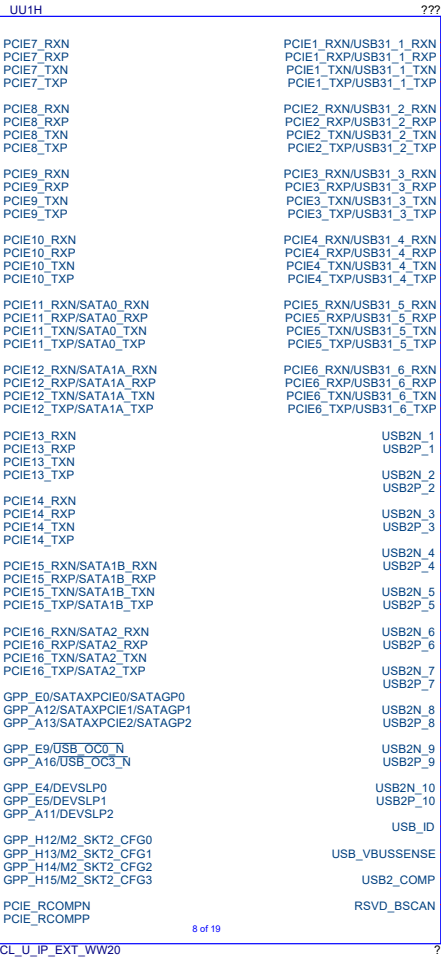
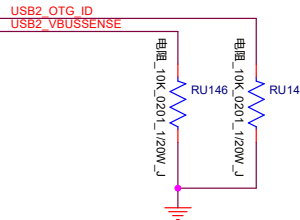
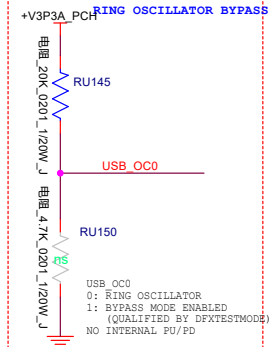
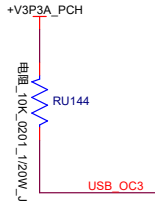
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49 USB_OC0 >> USB_OC0 DW14
54 USB_OC3 >> USB_OC3 CT43

41 SATA1_DEVS_LP << SATA1_DEVS_LP



PCH STRAP



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USB3.0 TypeA 1 AUO

NA

NA

NA

USB3.0 Type-A 1 AUO

GPU

USB3.0 Type-A 1 AUO

NA

Type-C

DB USB2.0 Type-A

Finger Print

Camera

NA

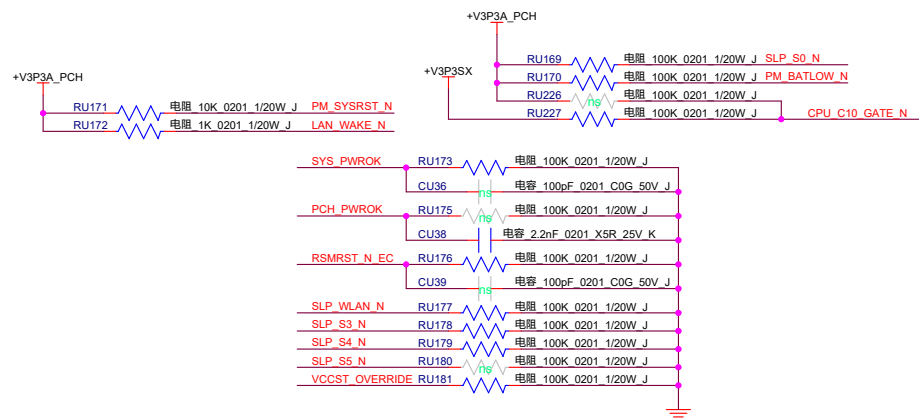
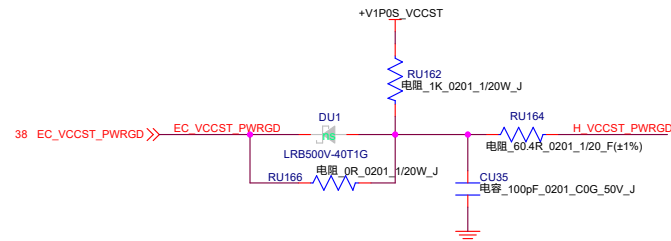
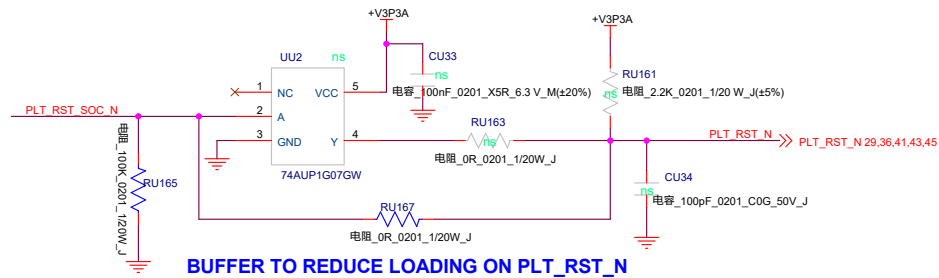
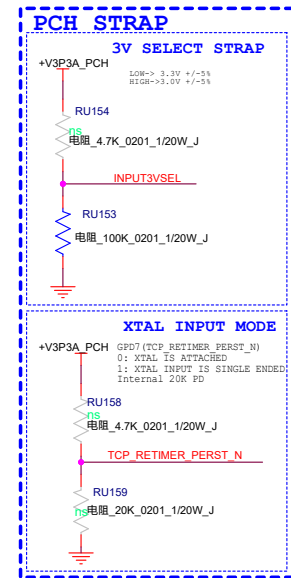
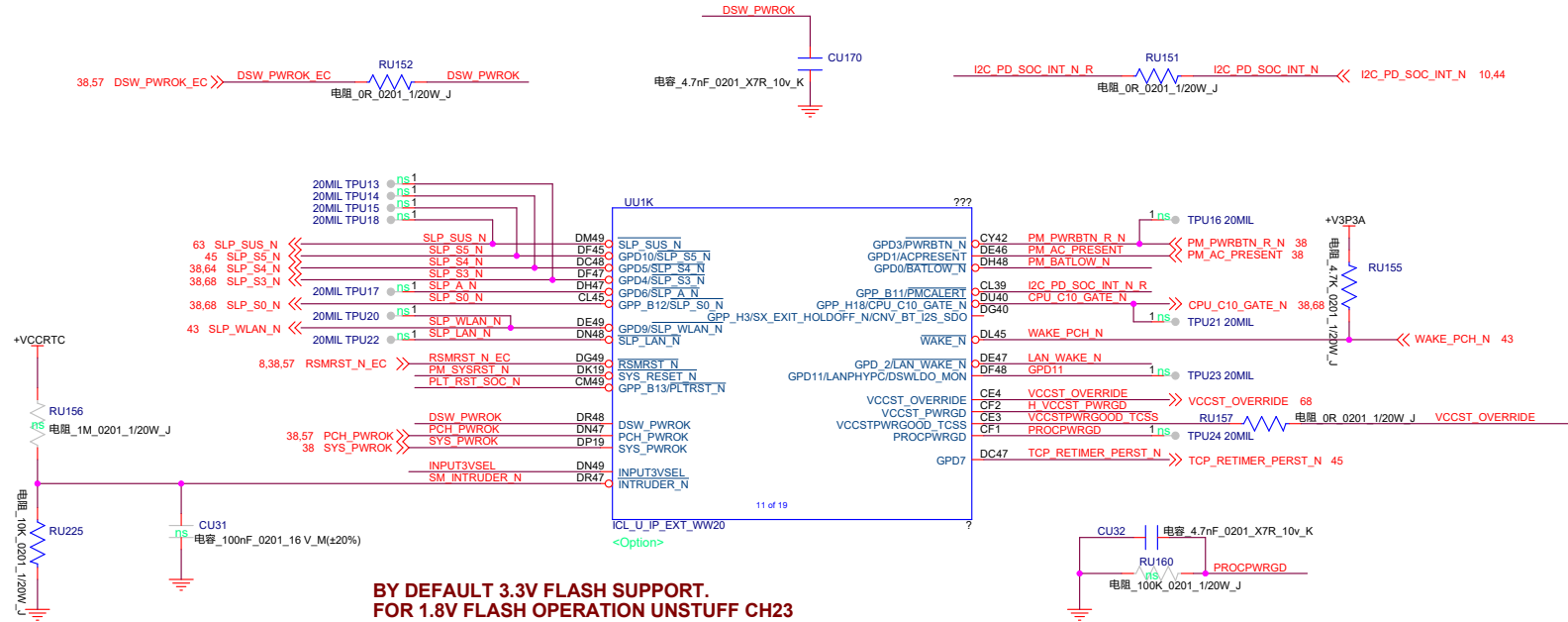
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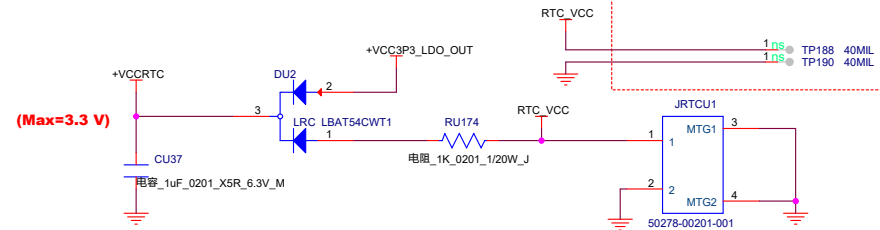
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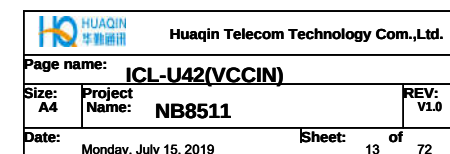
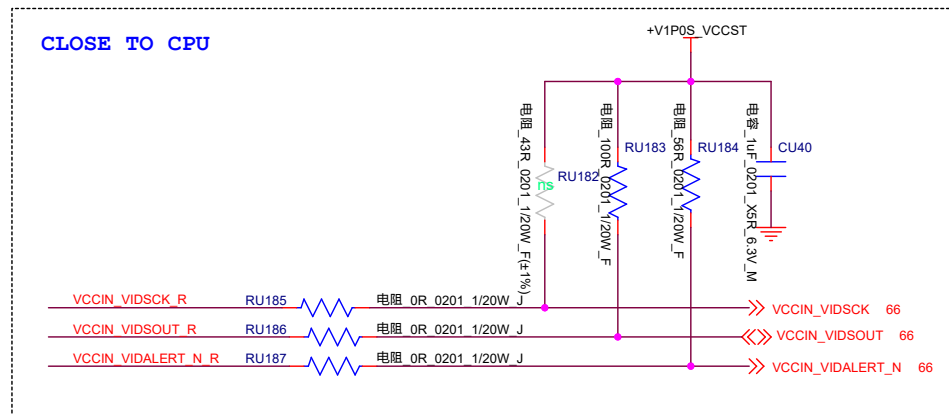
电阻 113R 0201 1/20 W_F(±1%)
USB2_COMP2 RESISTOR SHOULD
BE PLACED NEAR TO THE PIN
LENGHT <450 MILS

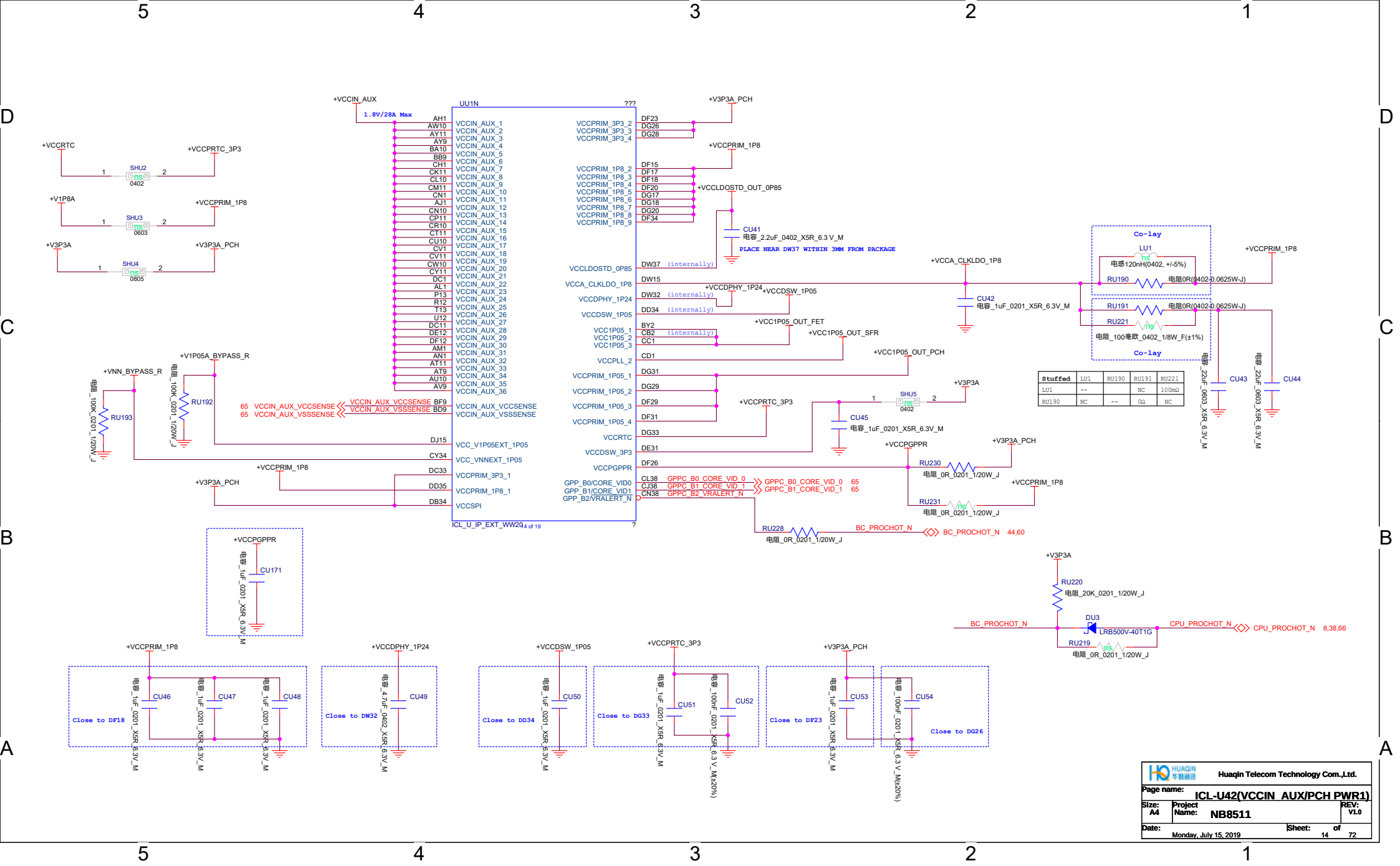
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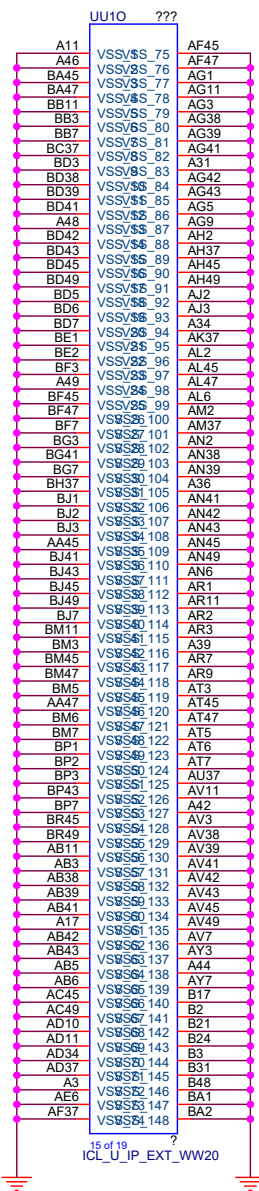


RTC

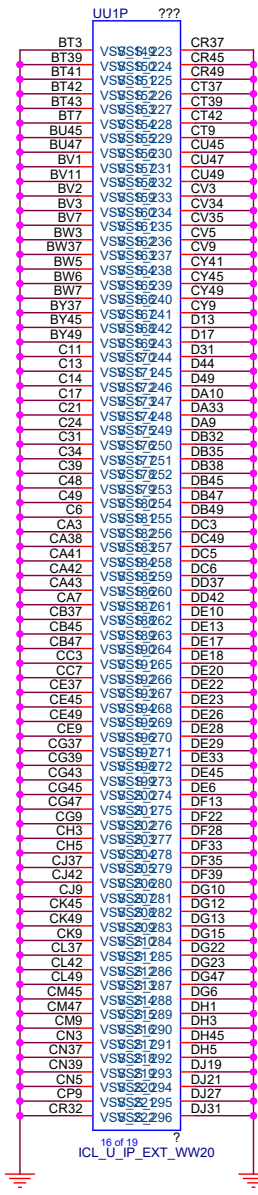




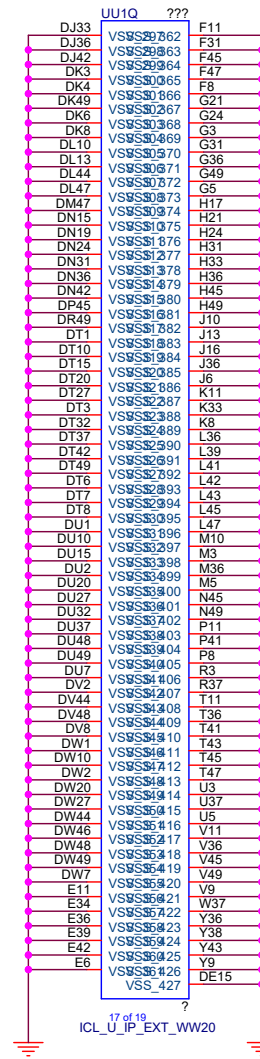




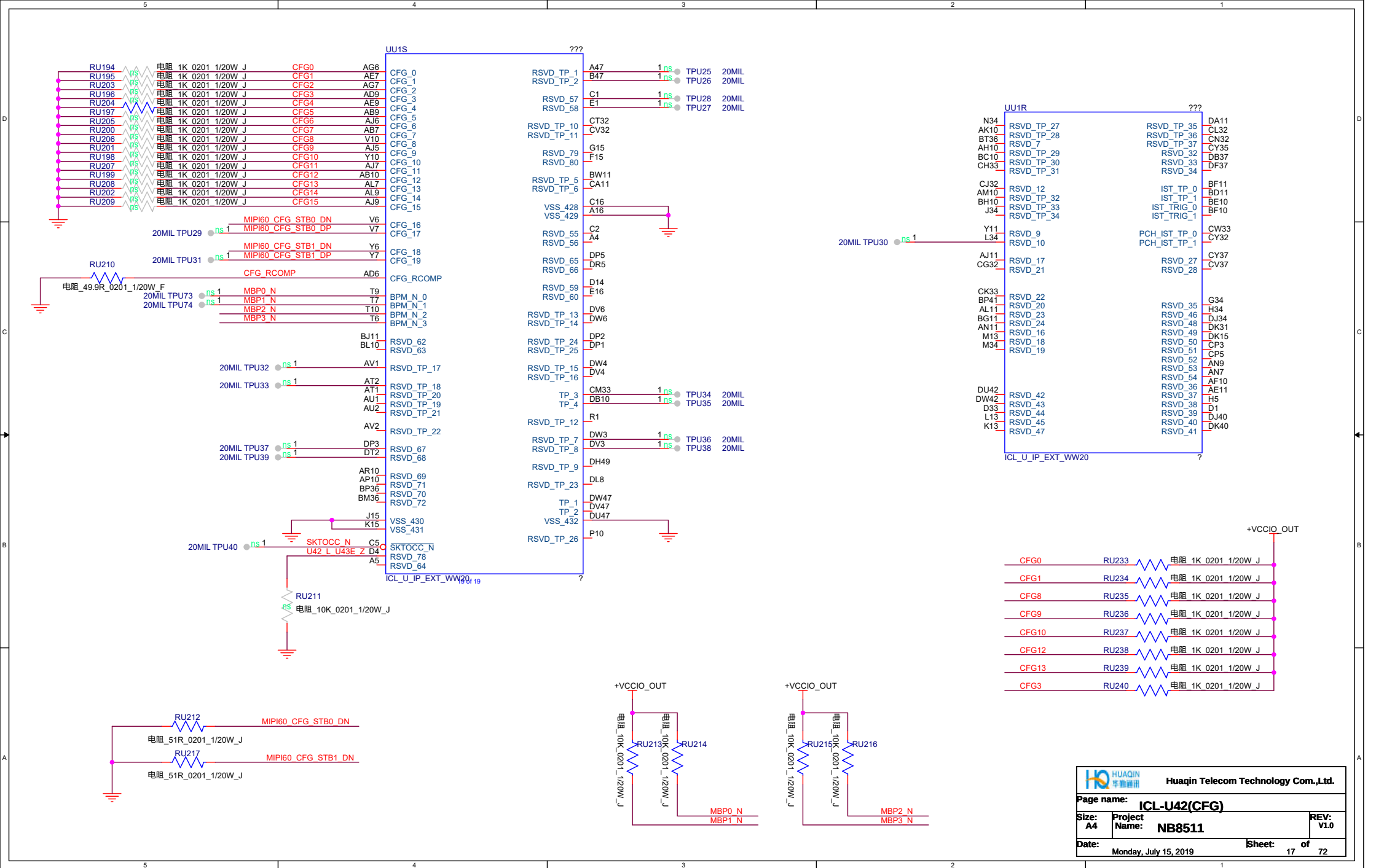
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ICL_U_IP_EXT_WW20

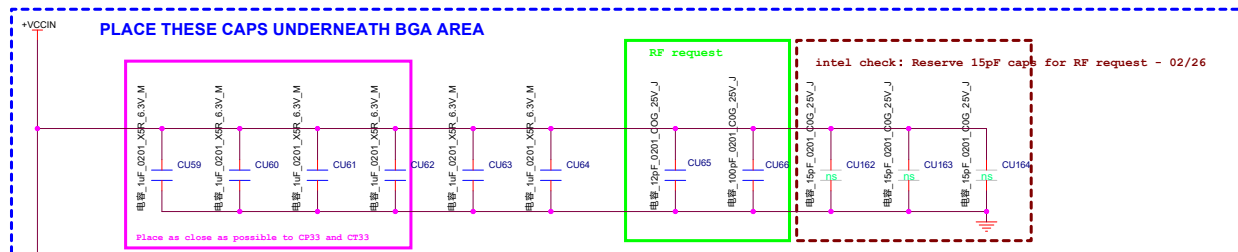


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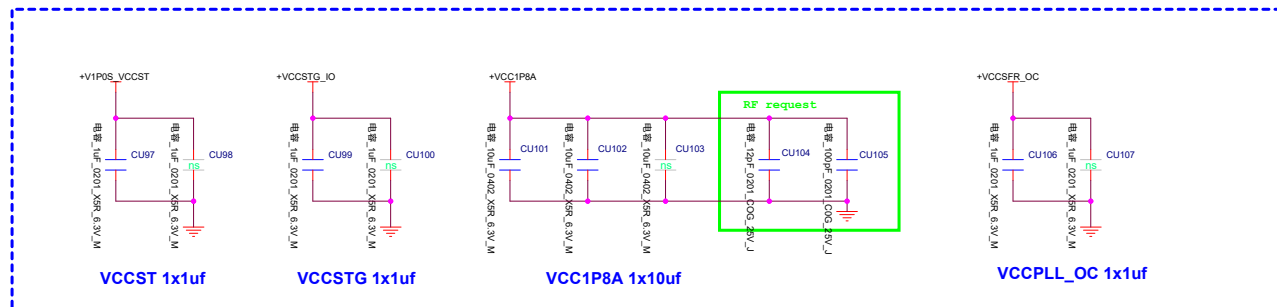
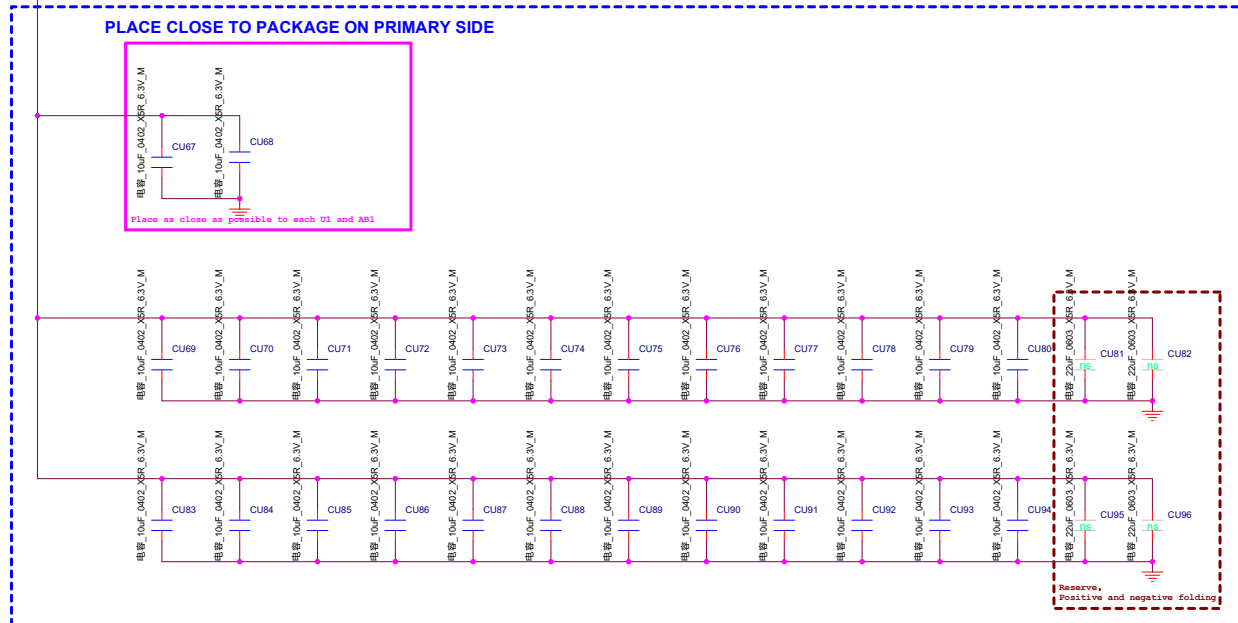
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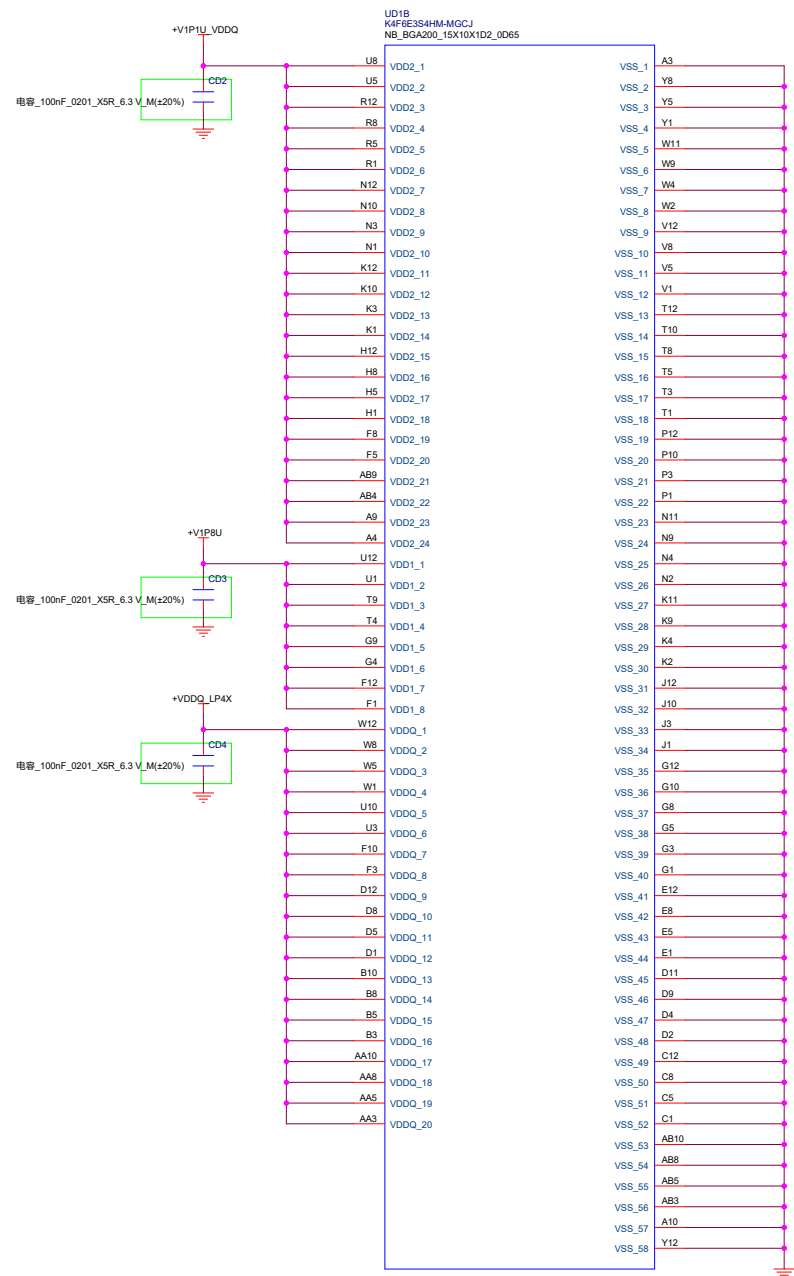
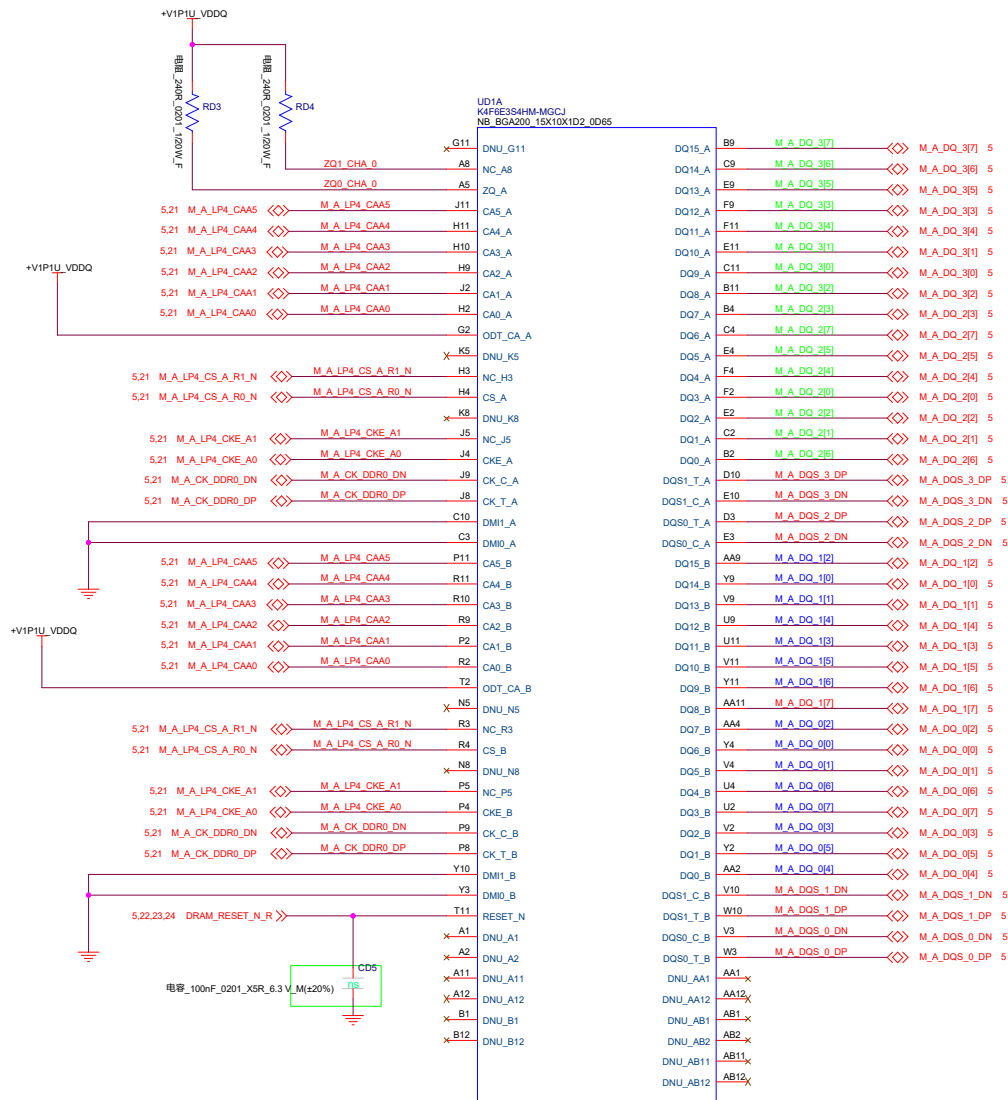


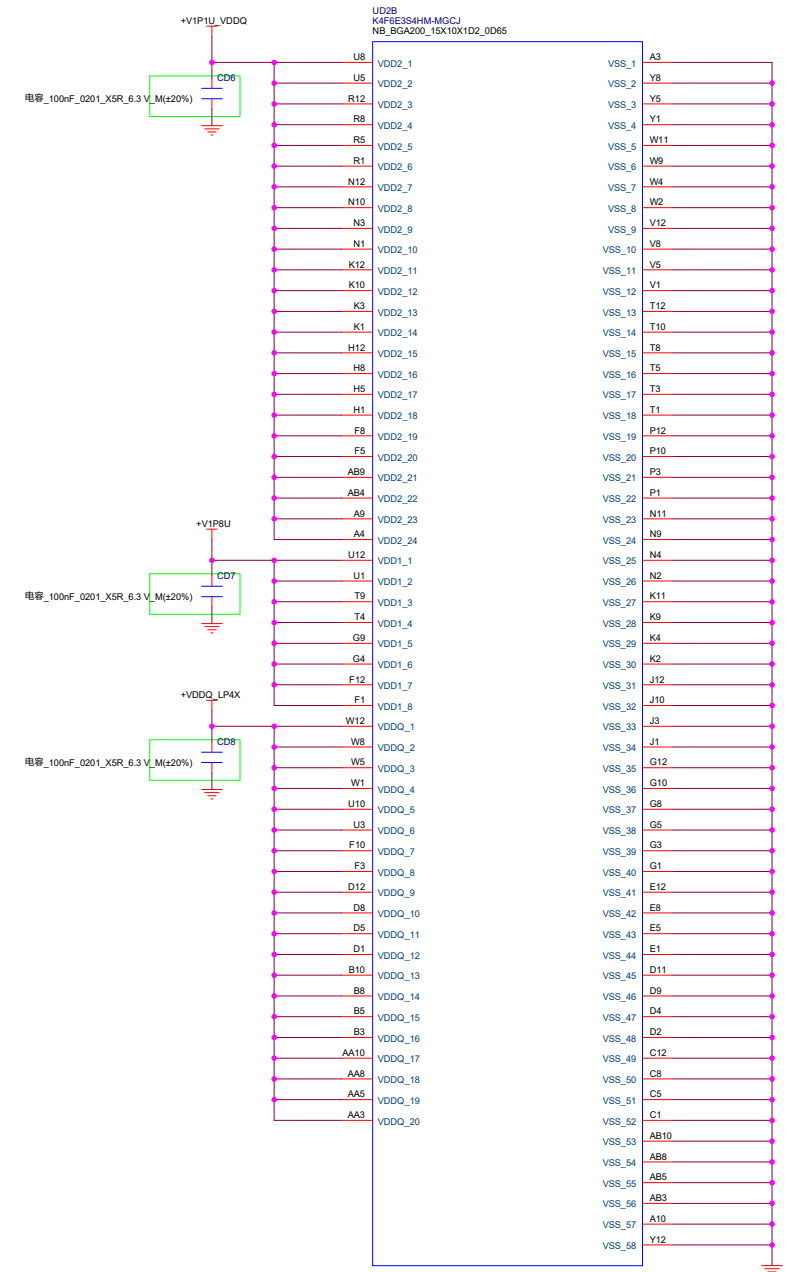
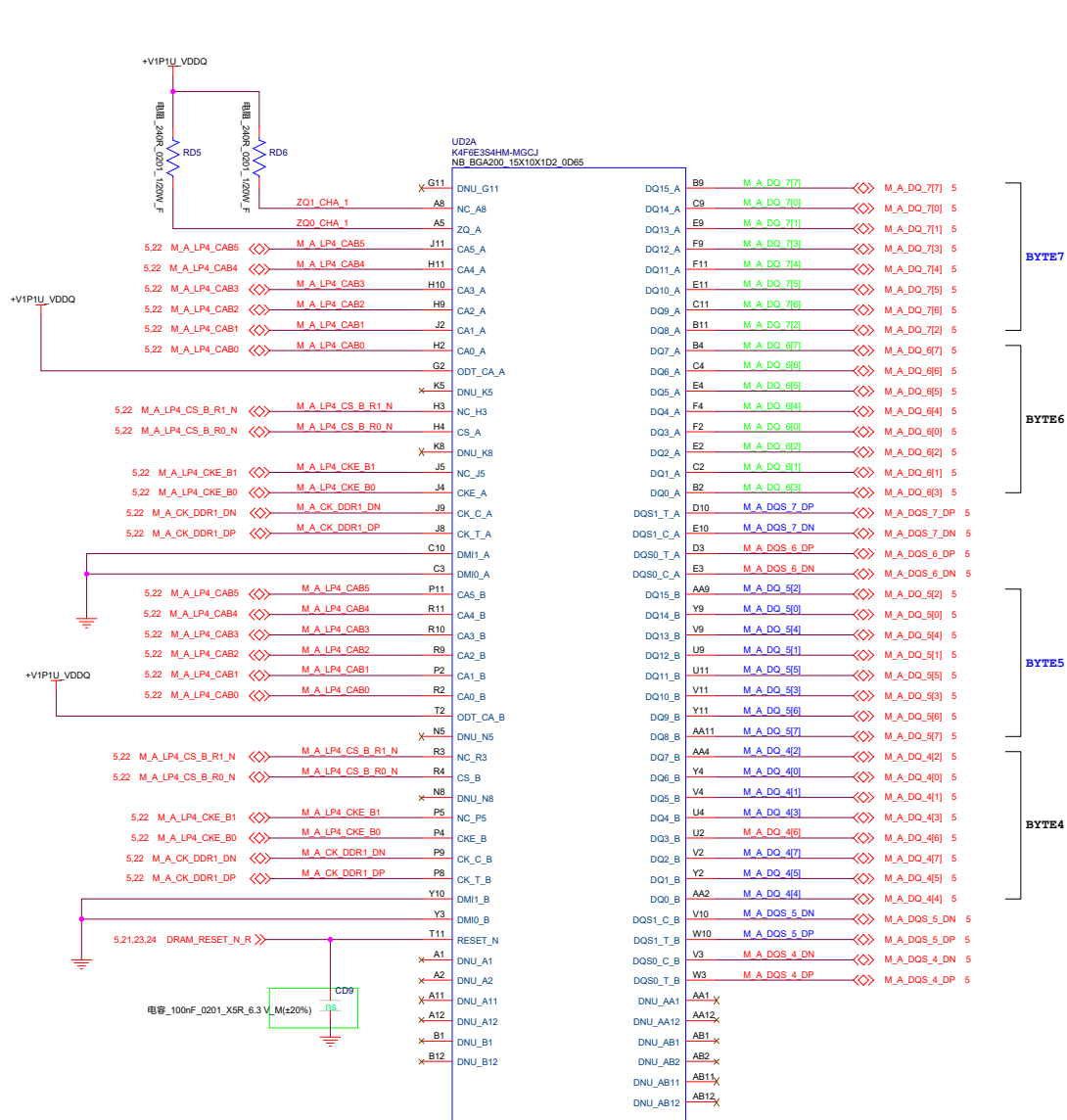
+VCCIN

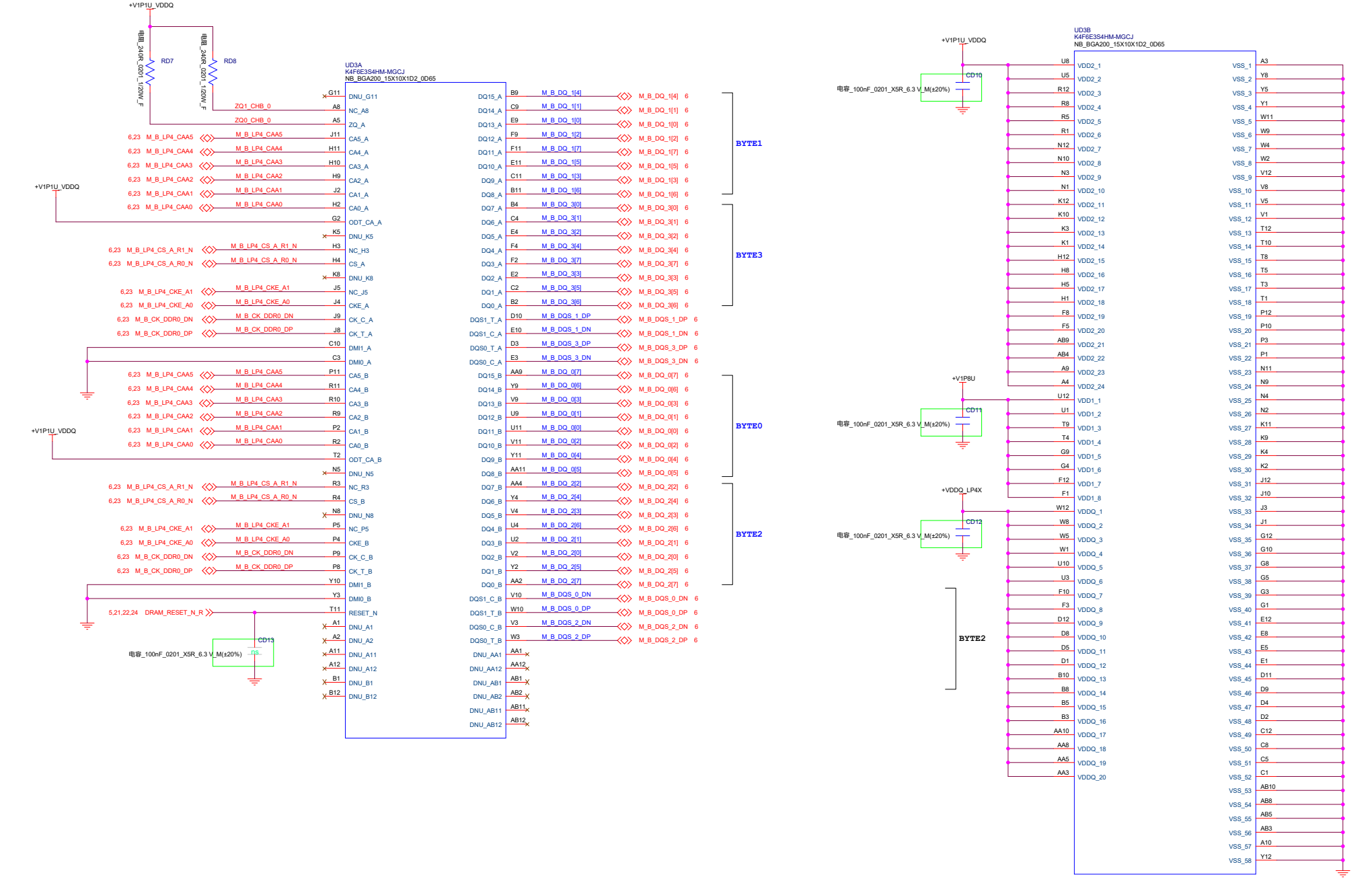
PDG:4 x 1uF
2 x 10uF
10x 22uF
3x 47uF

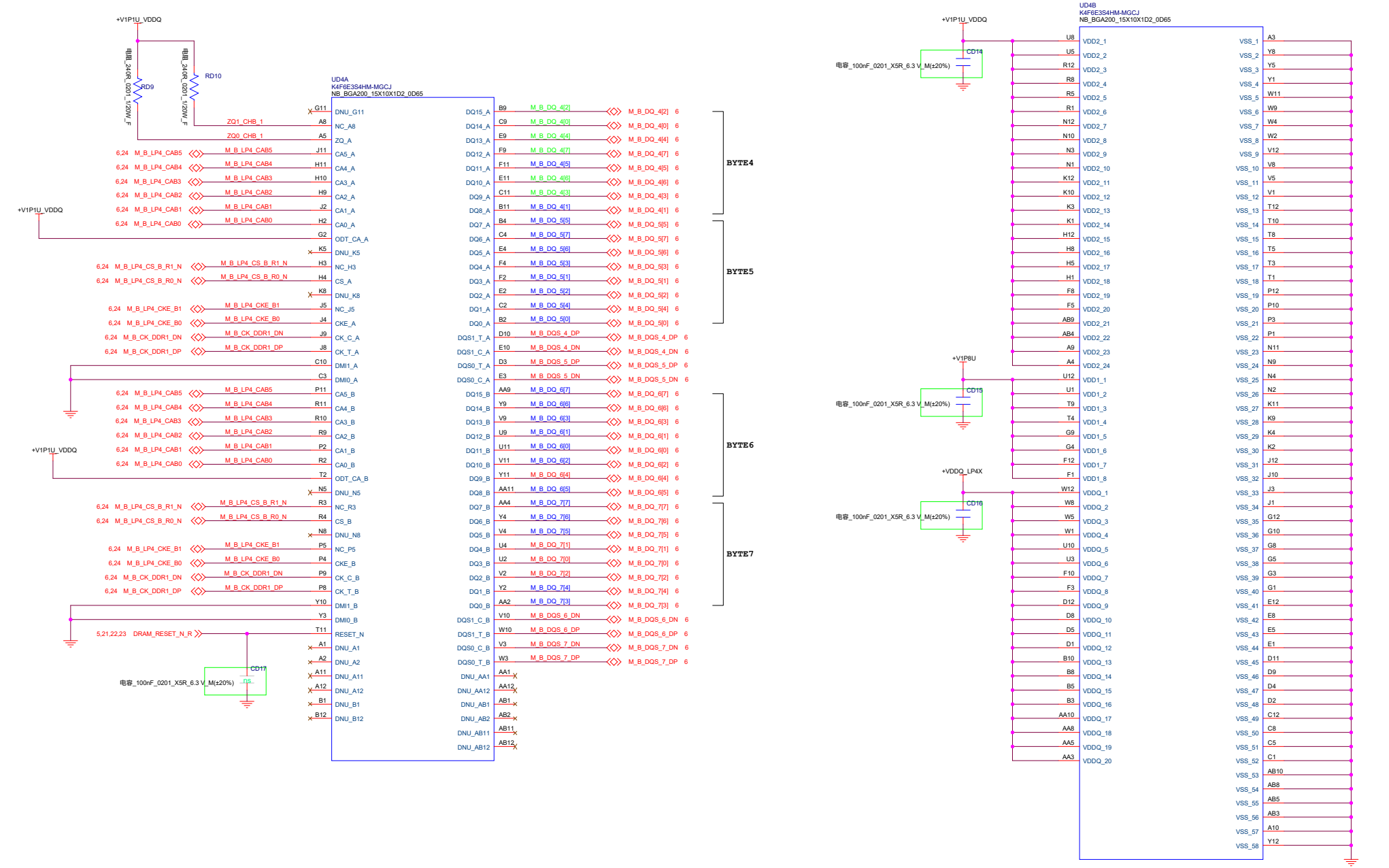


CHA-1



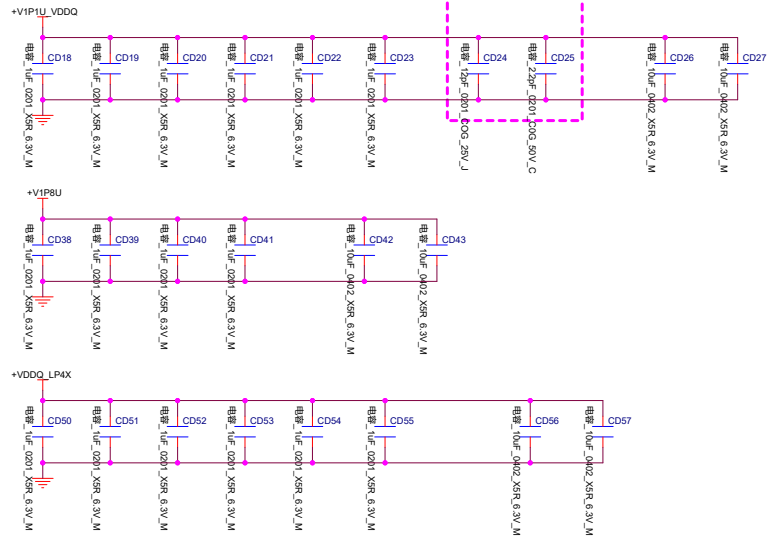




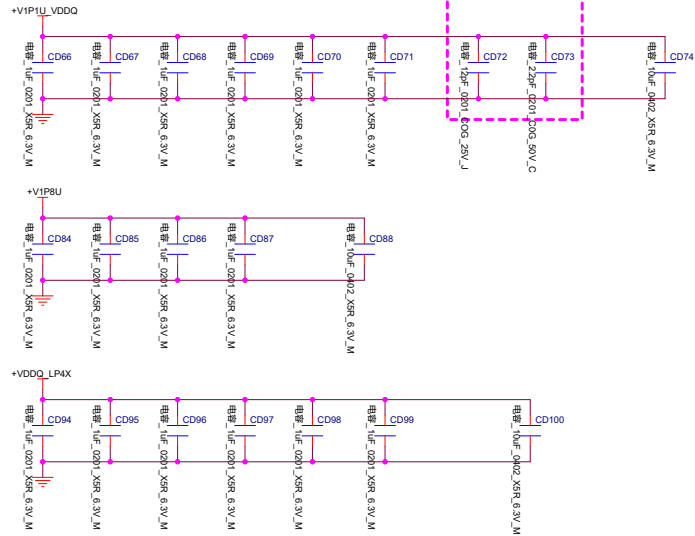


DECOUPLING CAPACITORS FOR LPDDR4 CHANNEL A

Place as close as possible to UD?

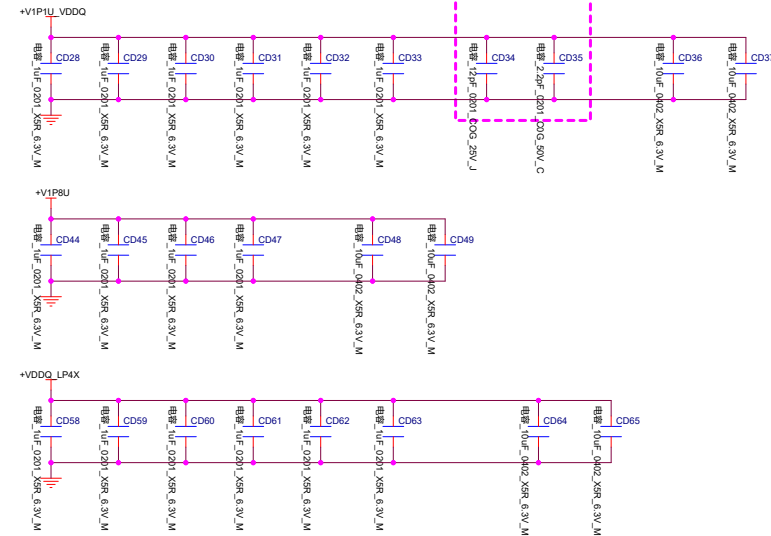


Place as close as possible to UD?

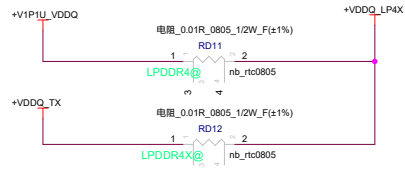
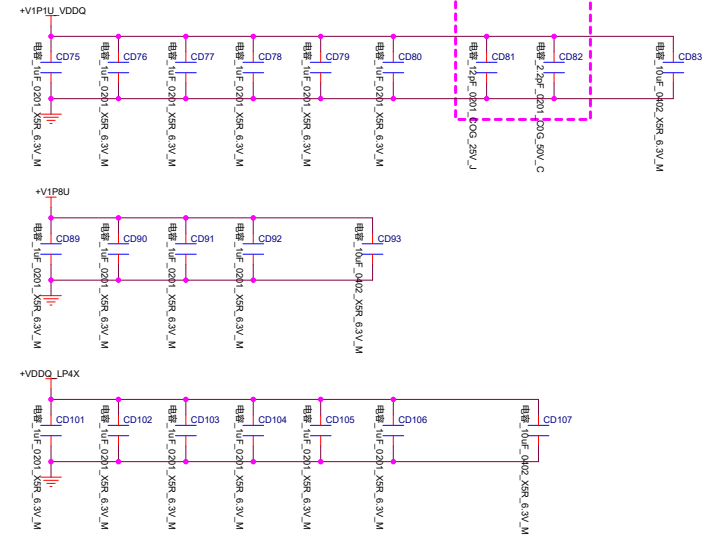


DECOUPLING CAPACITORS FOR LPDDR4 CHANNEL B


Place as close as possible to UD?




Place as close as possible to UD?

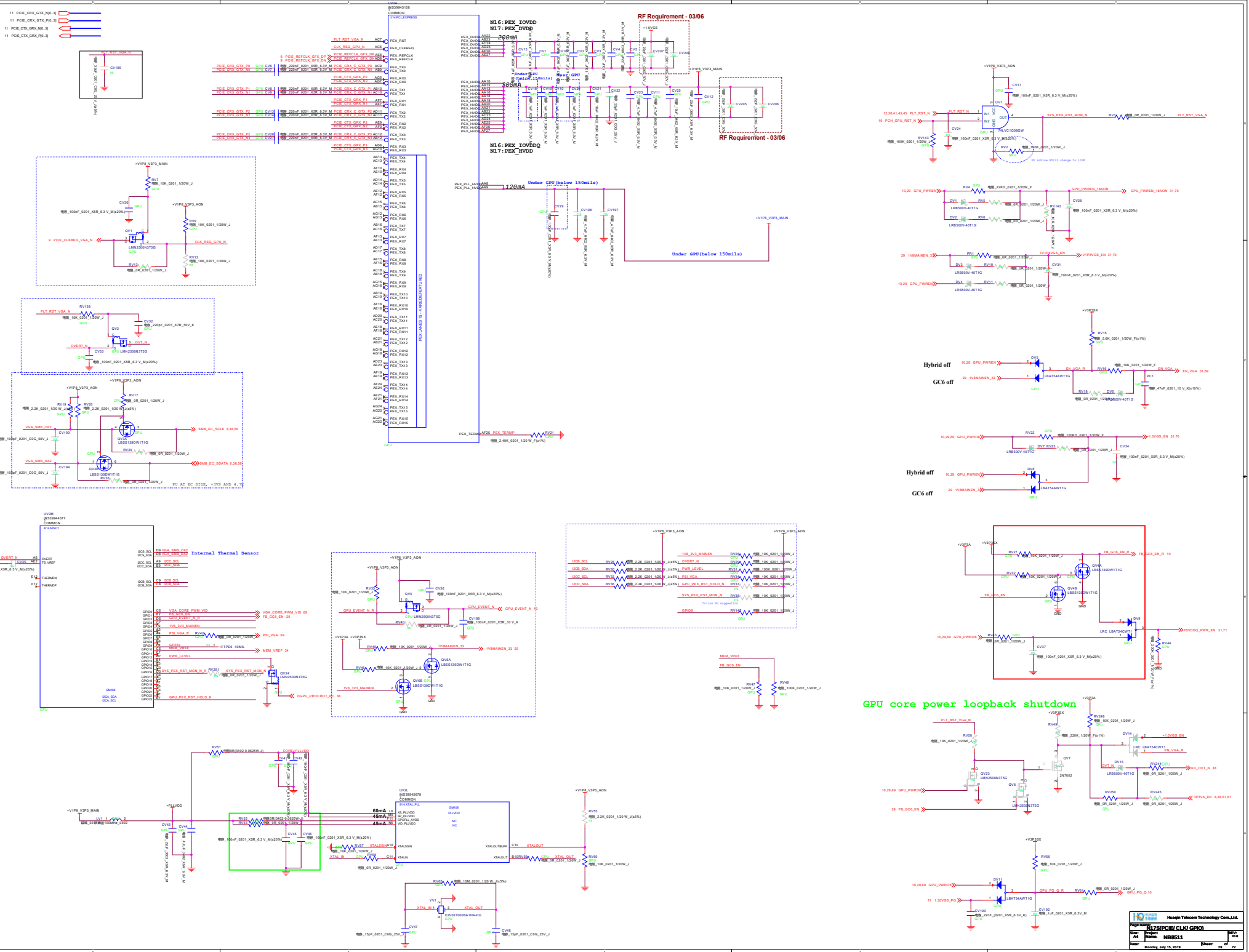


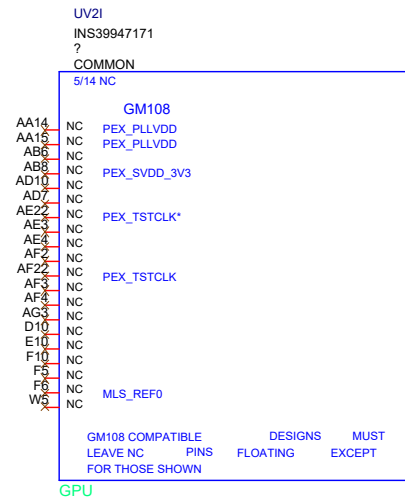
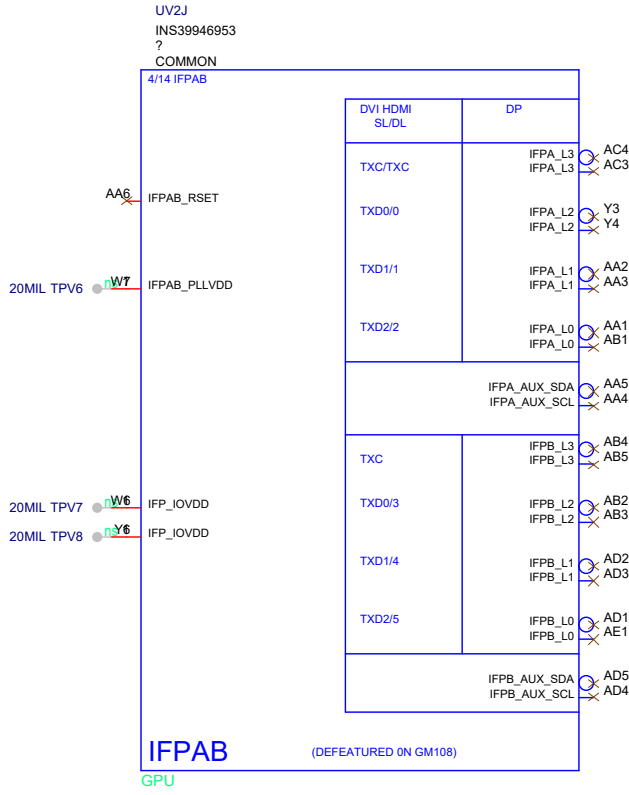
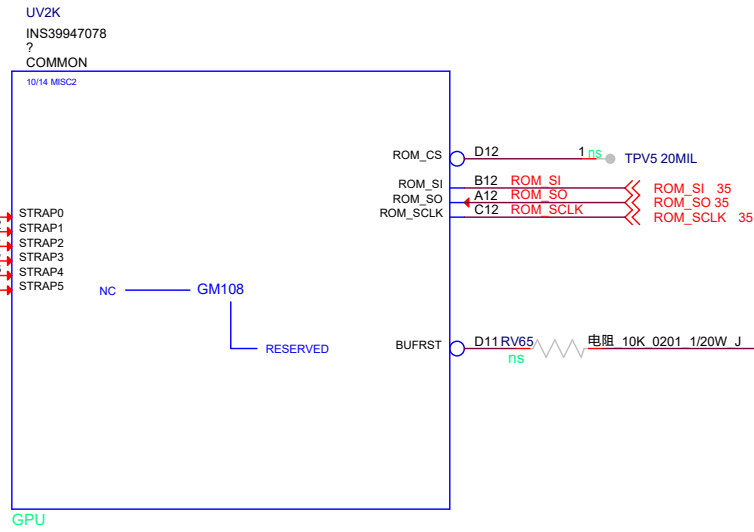
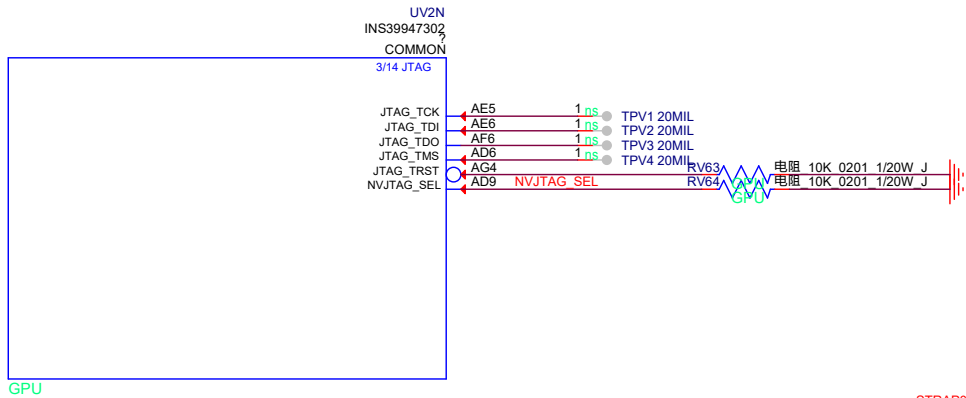
	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

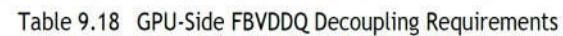
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Size: A4	Project Name: NB8511	REV: V1.0
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5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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Size: A4		Project Name: NB8511			REV: V1.0
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FBVDDQ Decoupling Requirements		
Recommended Quantity and Placement (for all supported partitions combined)		
Size	Quantity	Placement
2C-64 (preliminary)		
6S [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
6S [0603]	2	
6S [0603]	1	Near GPU device
6S [0603]	3	
4C-128 (preliminary)		
6S [0402]	12	Under GPU FBVDDQ ball (equally distributed across partitions)
6S [0603]	4	
6S [0603]	2	Near GPU device
6S [0603]	5	
B4-256		
6S [0402]	24	Under GPU FBVDDQ ball (equally distributed across partitions)
6S [0603]	5	
6S [0603]	7	Near GPU device
6S [0603]	9	

Move to Power Page 2018/06/07

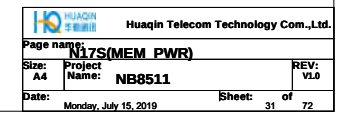


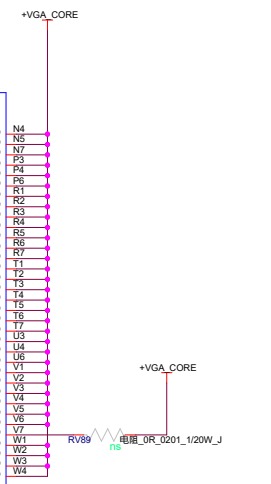
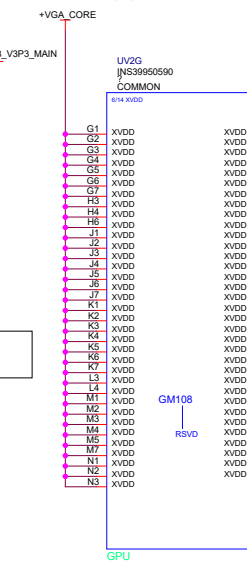
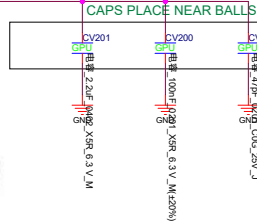
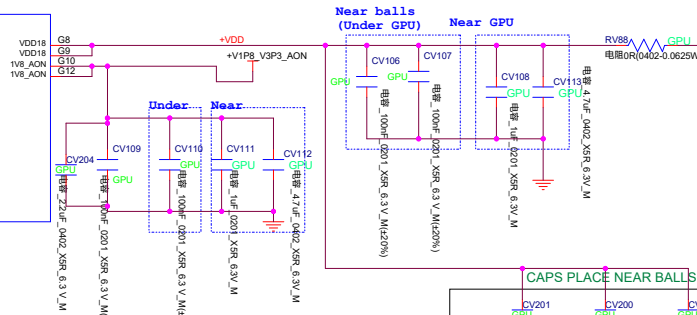
Table 7.18 GB2C-64 Package: Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage: Current	Filtering under GPU	Filtering Near GPU
NVVDD	31	Varies	3 X 1uF (0402) 8 X 4.7uF (0603)	1 X 4.7uF (0805) 4 X 10uF (0305) 3 X 22uF (0805) 1 X 330uF (Pocscap)
NVVDD_S	10	Varies	2 X 1uF (0402) 4 X 4.7uF (0603)	Near VR: 2 X 10uF (0805) 7 X 10uF (0805) 1 X 22uF (0805) 1 X 330uF (Pocscap)
FBVDDQ (GPU side) ¹	27	1.35V 1.5V 1.55V	8 X 1uF (0402) 2 X 10uF (0603)	10uF (0603) 3 X 22uF (0603)
FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (0402 X7R)	1 X 300 bead (0603 max<ESR 10 mΩ)
FBB_PLL_AVDD	1	1.8V	0.1uF (0402 X5R)	1 X 22uF (0805)
FB_REFPLL_AVDD	1	1.8V	1 X 0.1uF (0402 X5R)	1 X 300 bead (0603 max<ESR 0.01 Ω)
IFPAB_PLLVDD	1	1.8V	2 X 0.1uF (0402 X5R)	1 X 22uF (0805)
GPCPLL_AVDD	2	1.8V	1 X 0.1uF (0402 X5R)	1 X 4.7uF (0603)
XS_PLLVDD	1	1.8V	1 X 0.1uF (0402 X5R)	1 X 4.7uF (0603)
SP_PLLVDD	1	1.8V	1 X 0.1uF (0402 X5R)	1 X 4.7uF (0603)
WD_PLLVDD	1	1.8V	1 X 0.1uF (0402 X5R)	1 X 4.7uF (0603)
IFP_OVDD	2	1.0V	2 X 0.1uF (0402 X6S)	1 X 1uF (0402)

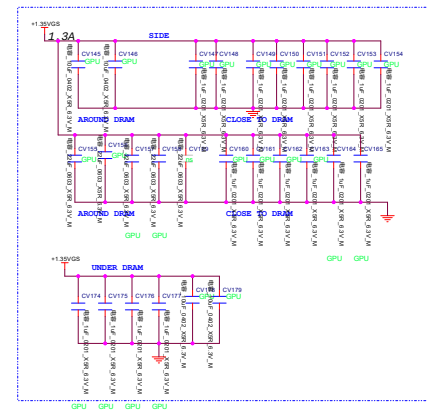
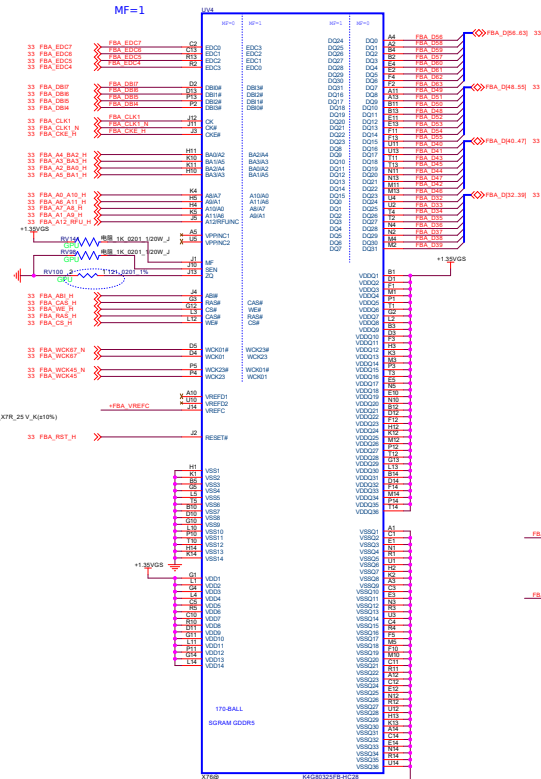
Table 7.18 GB2C-64 Package: Power Rail Filtering (Continued)


Rail (GPU Ball) Name	Balls	Voltage: Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway bet GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_HVDD	2	1.8V	1 X 0.1uF (0402)	Near GPU: 2 X 4.7uF (0603) Midway bet GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	1 X 4.7uF (0603)
1VB_MAIN	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402)
1VB_AON	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402)

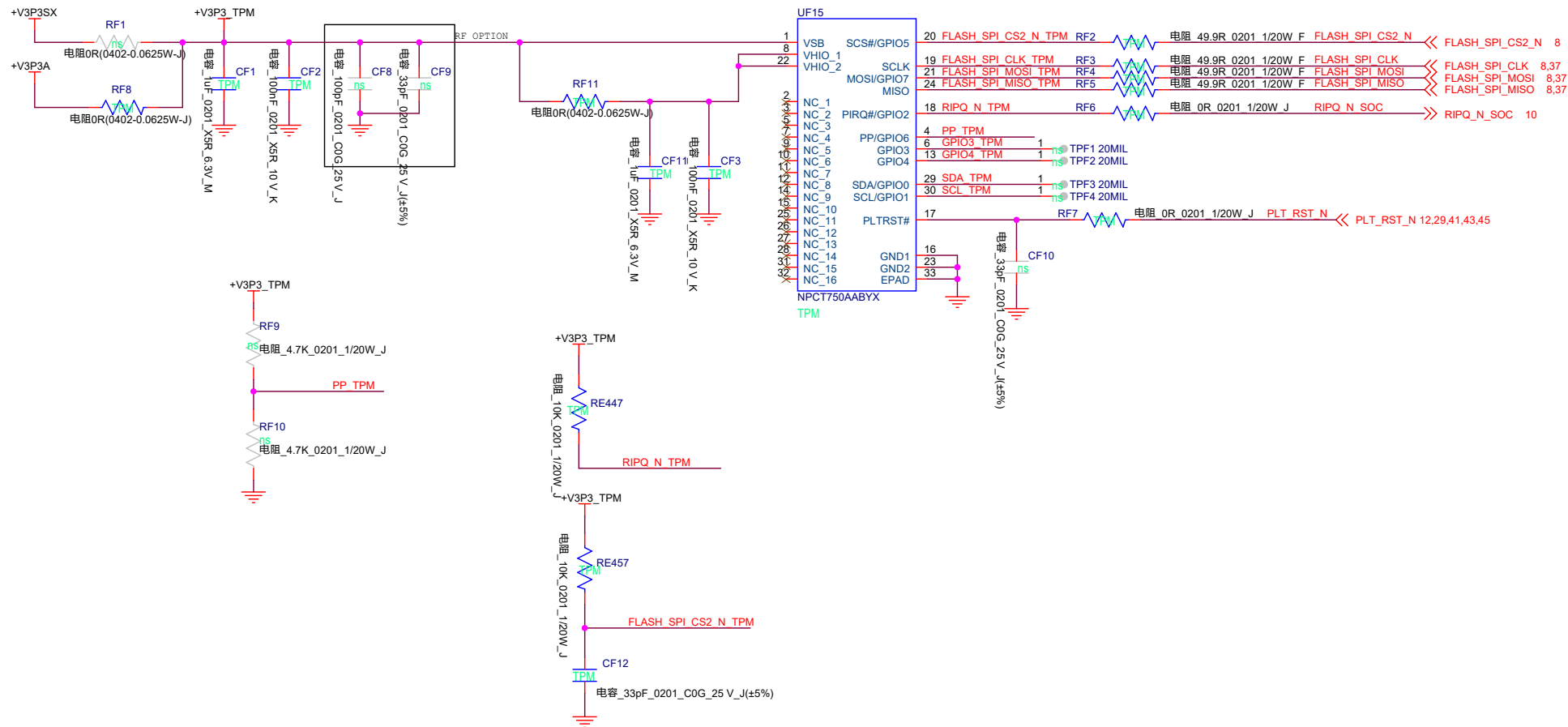
Note:
1. Also see Section 9.2.2.1.10.1

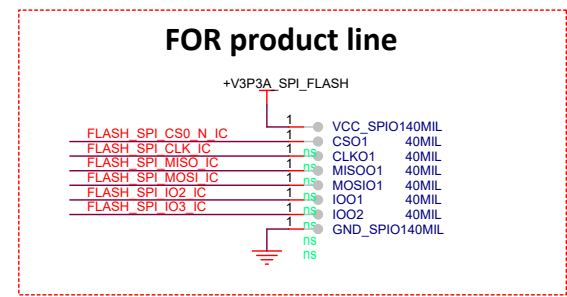
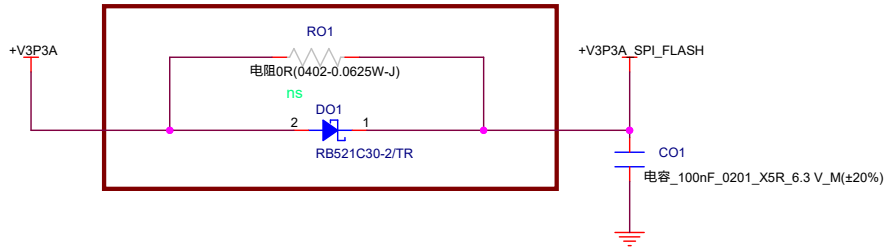


Memory - Upper 32 bits

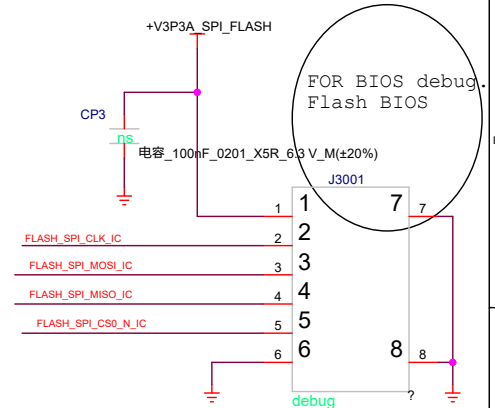
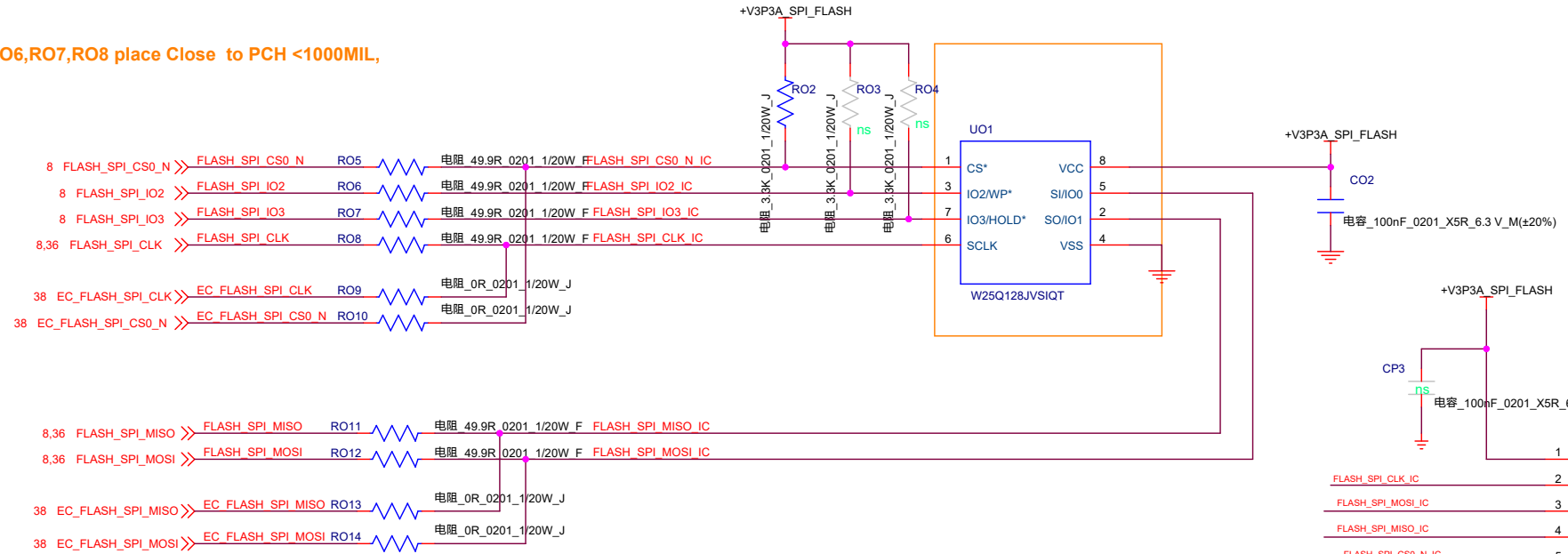
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Size: A4	Project Name: NB8511	REV: V1.8	
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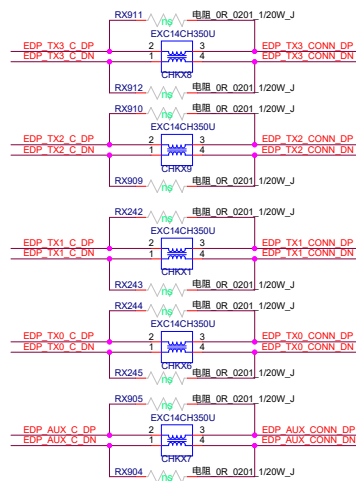
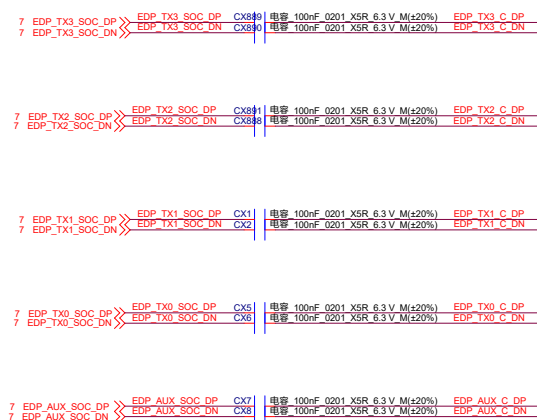




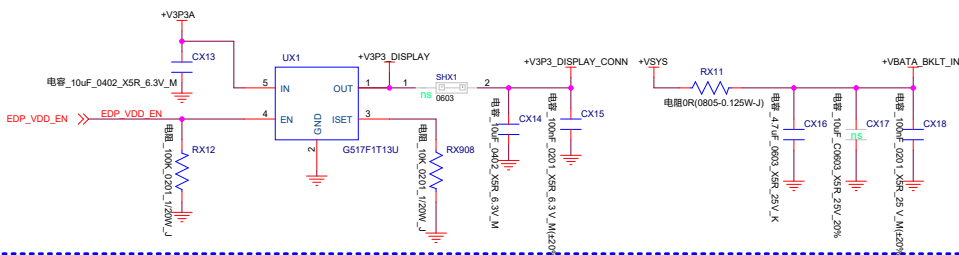
Series RO5,RO6,RO7,RO8 place Close to PCH <1000MIL,



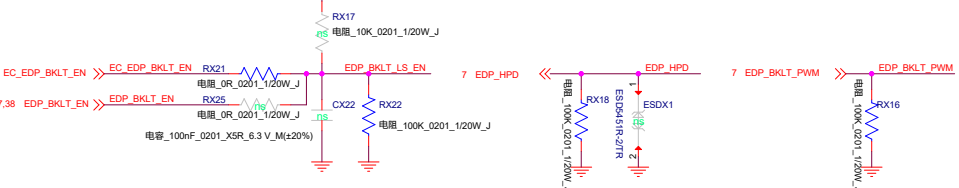
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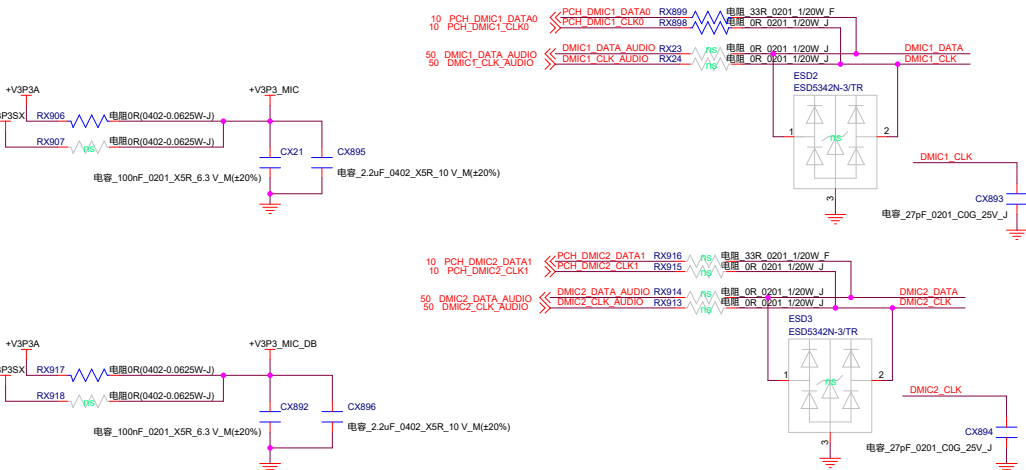
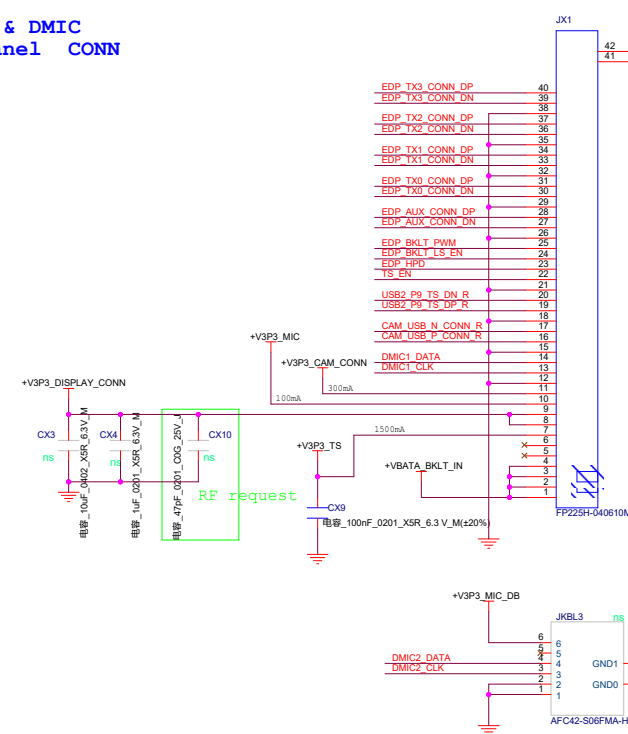
eDP VCC & BL Power



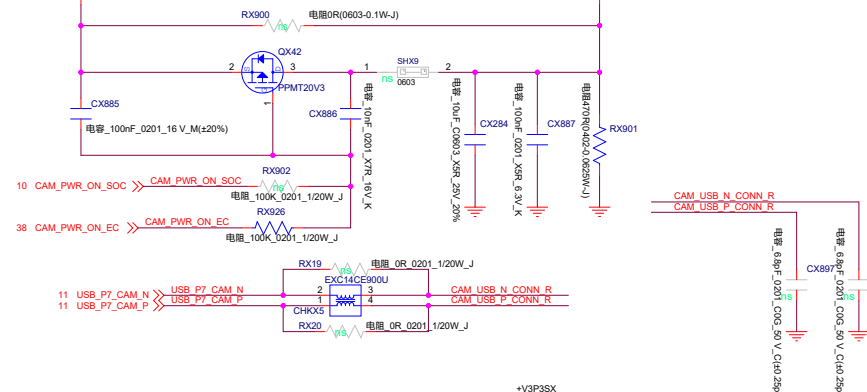
eDP Control



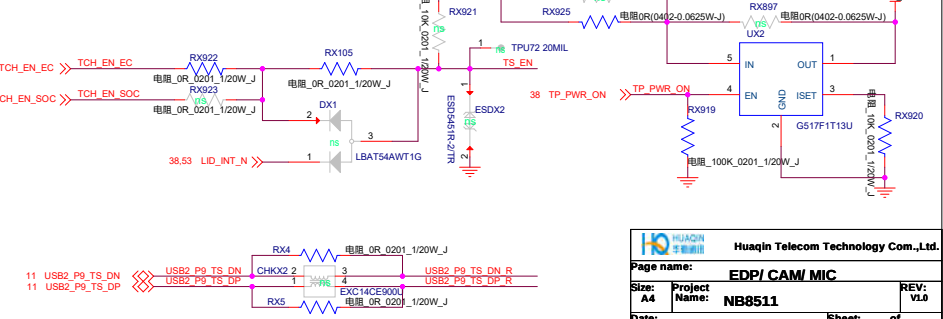
MIC

eDP & CAM & DMIC
& Touch Panel CONN

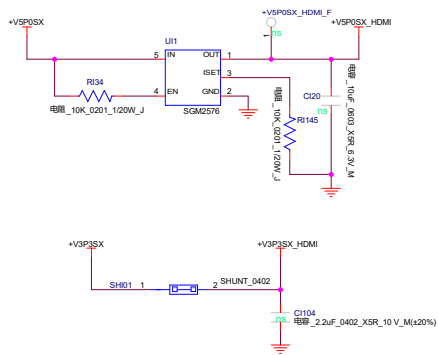
ex CAM Power



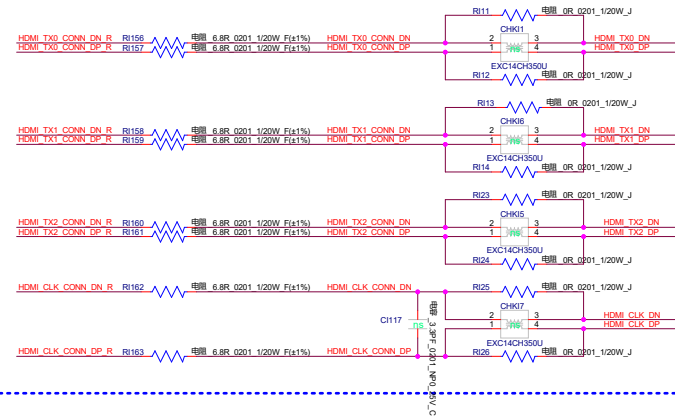
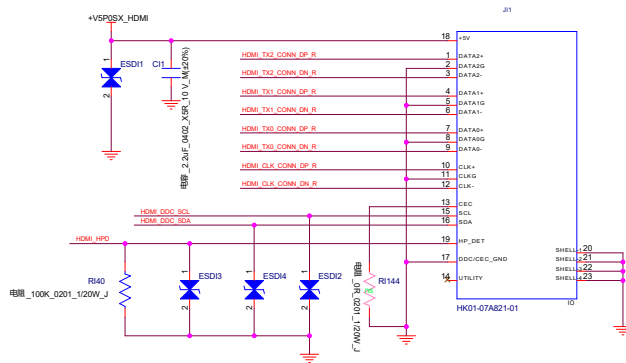
Touch Panel



Power 1



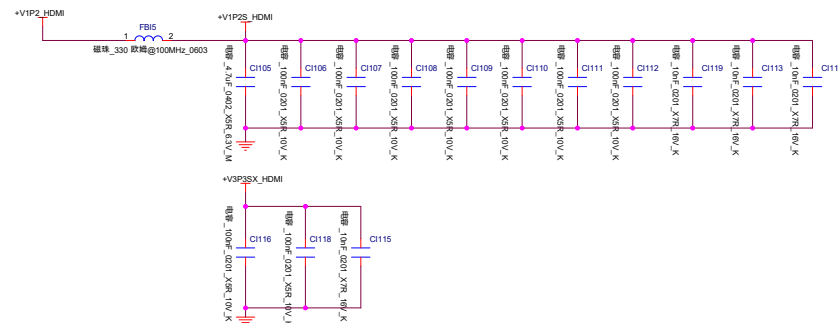
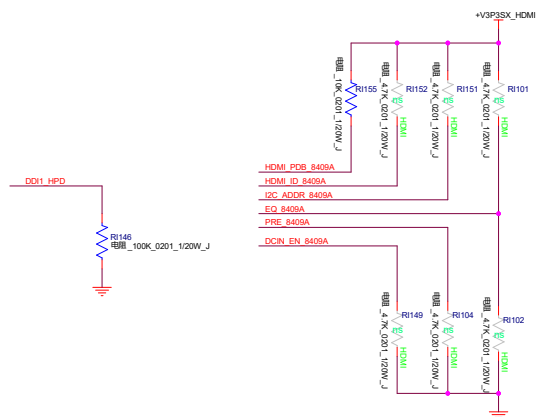
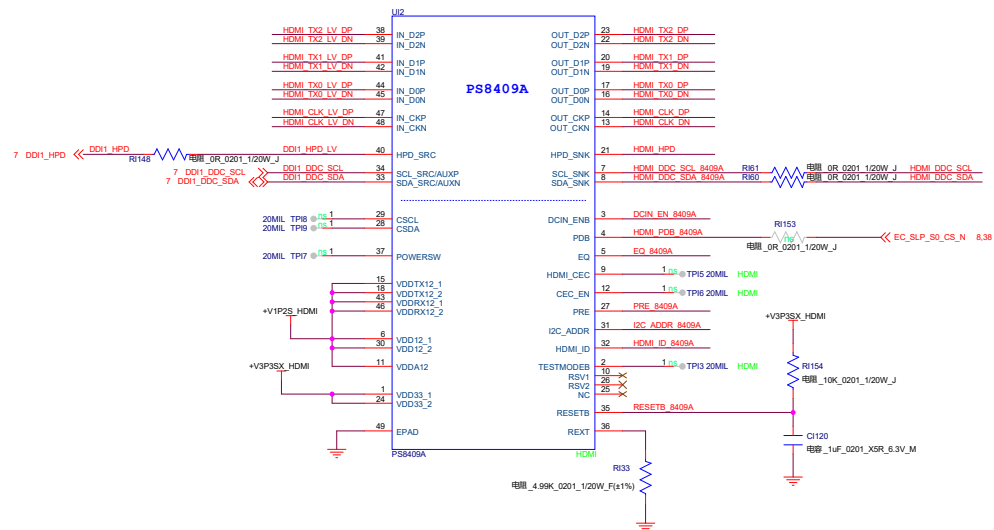
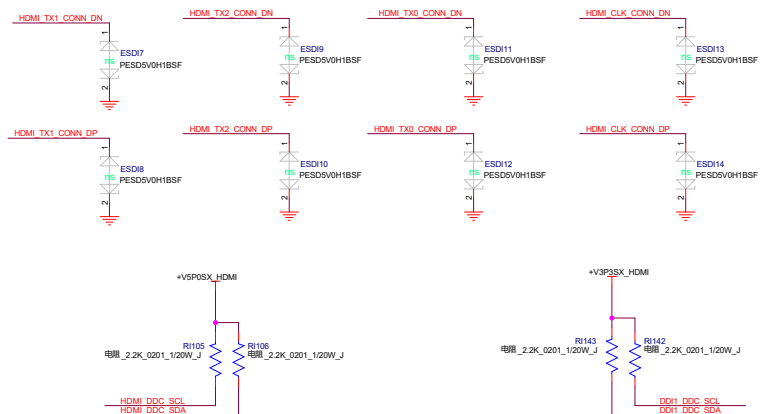
HDMI CONN



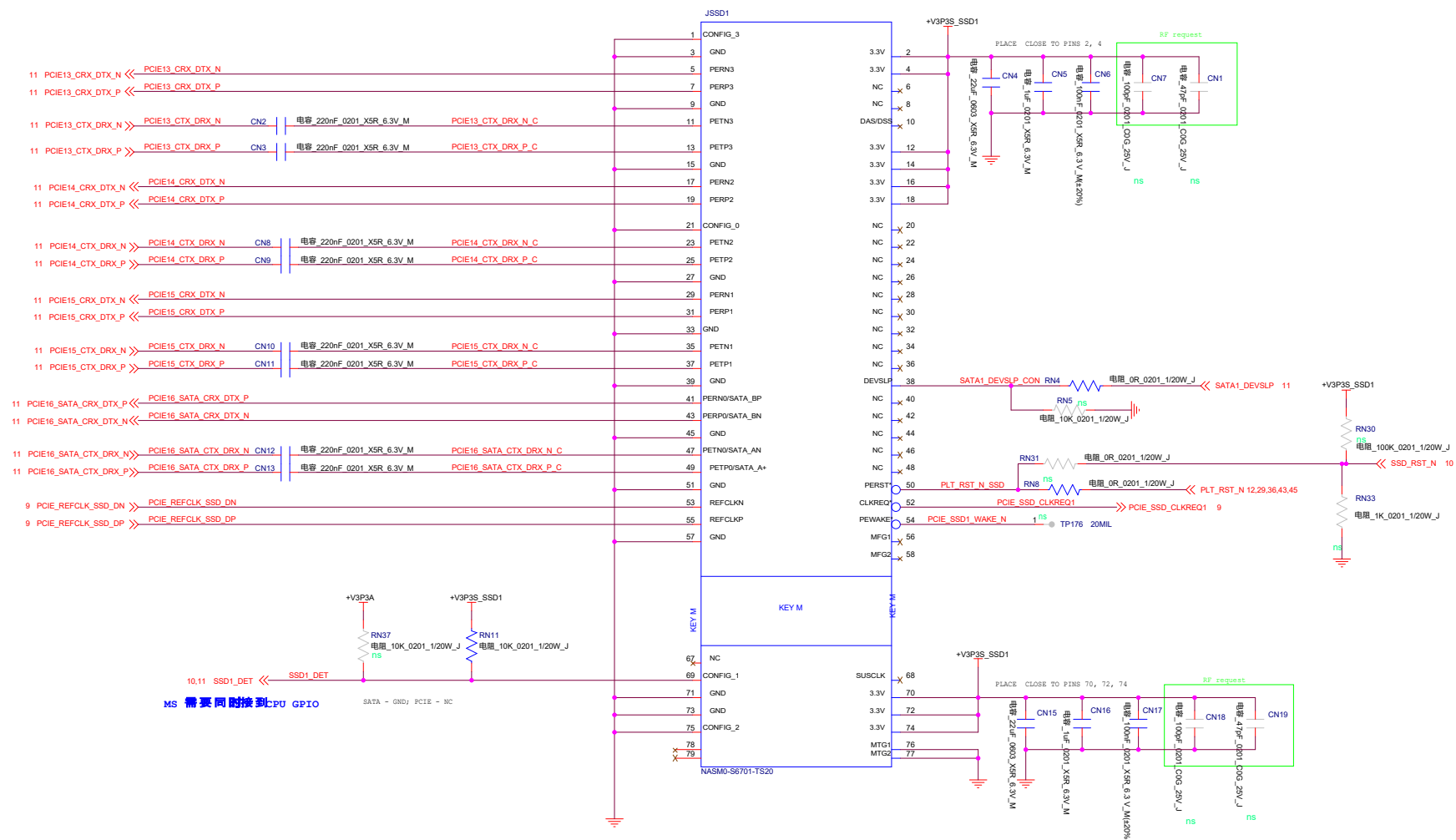
Signal

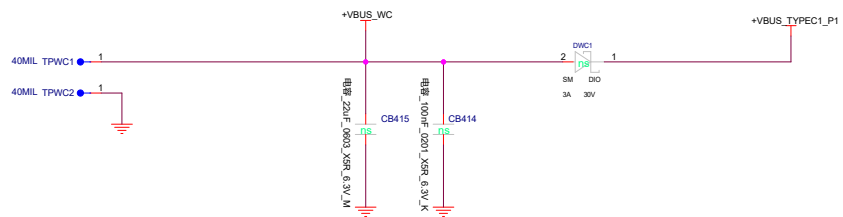


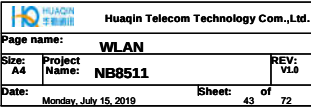
ESD

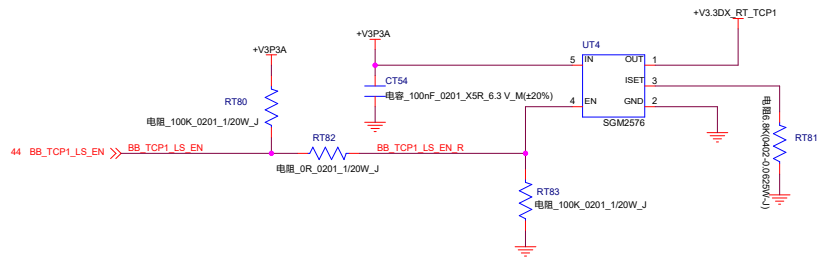
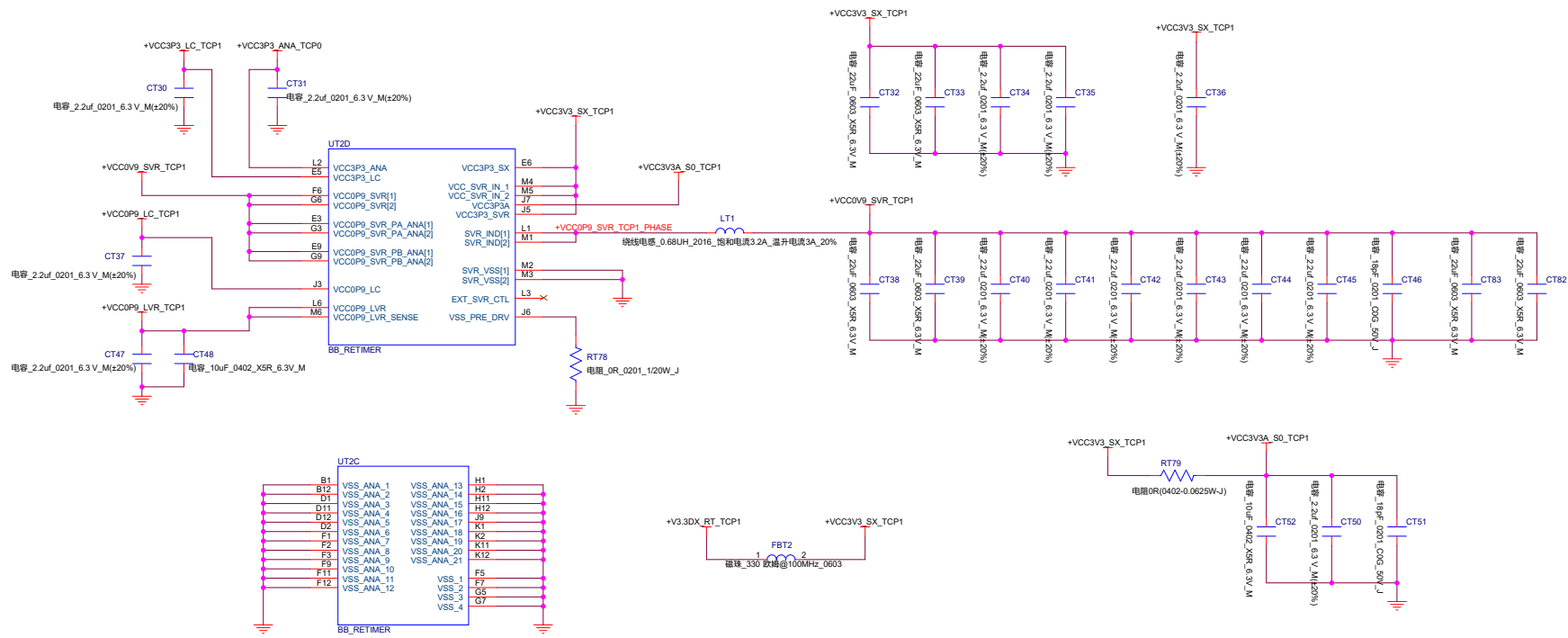


SSD

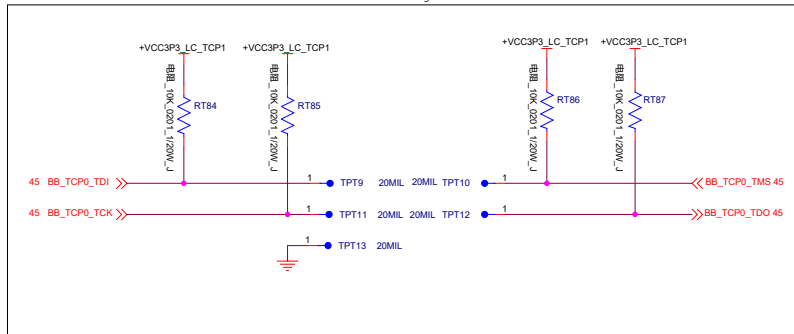




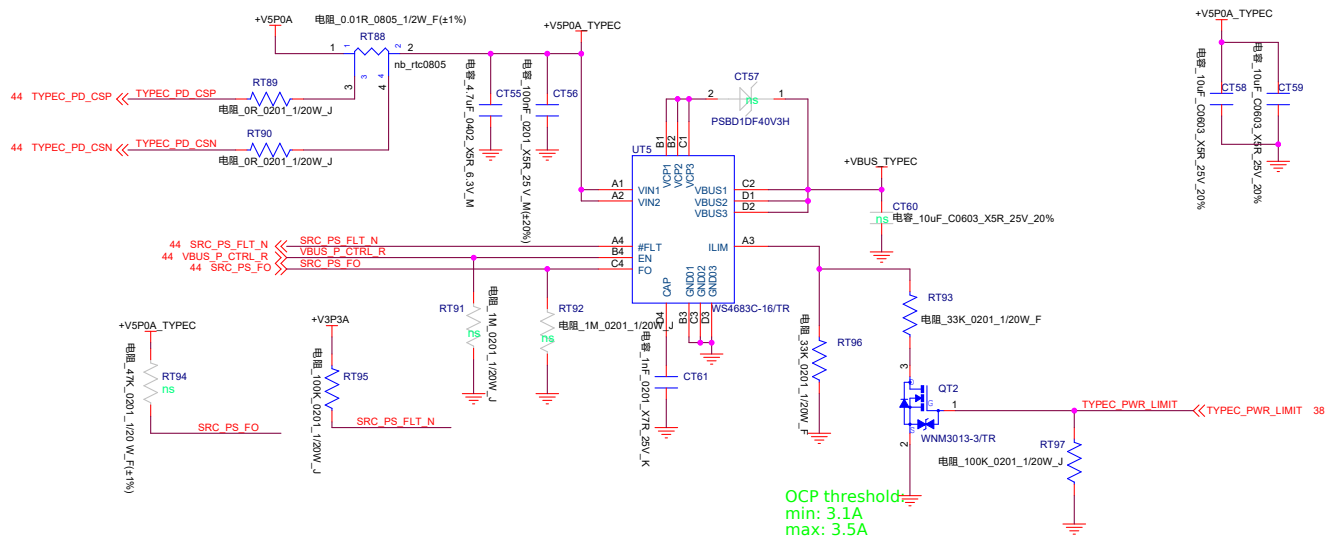




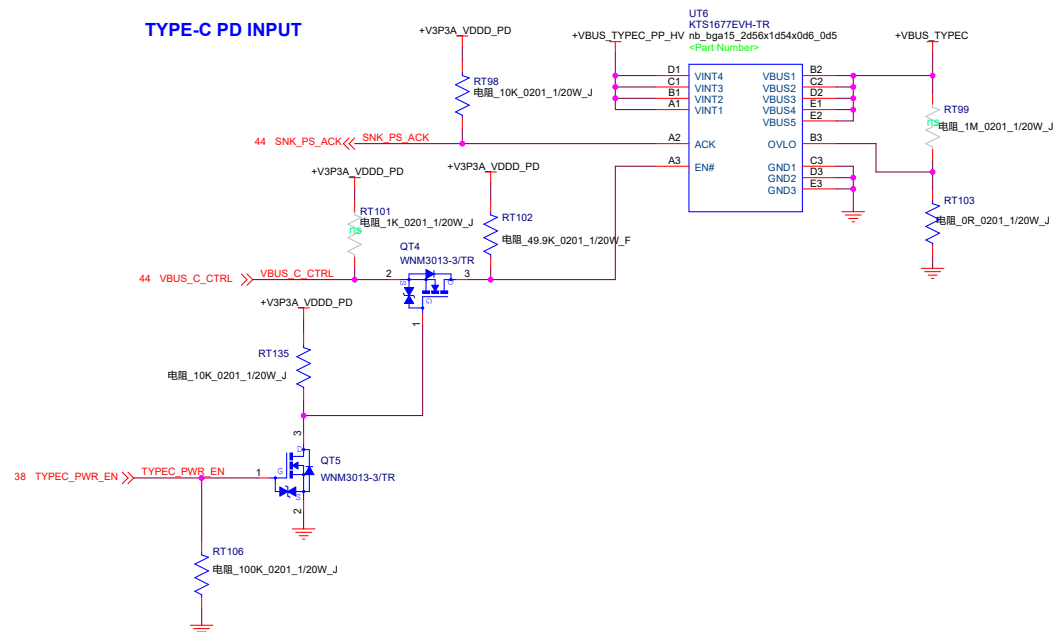
Place together



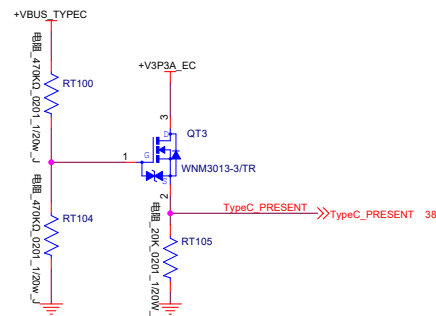
TYPE-C PD OUTPUT



TYPE-C PD INPUT

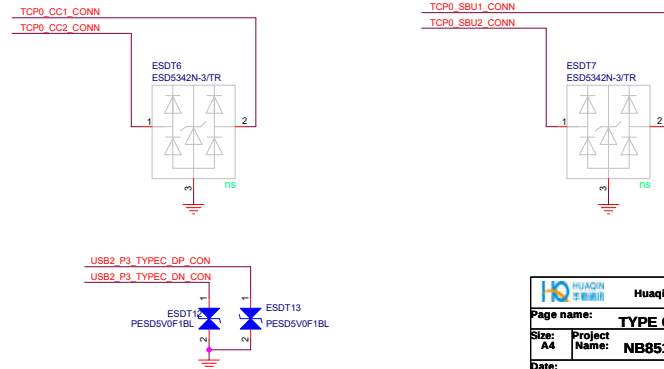
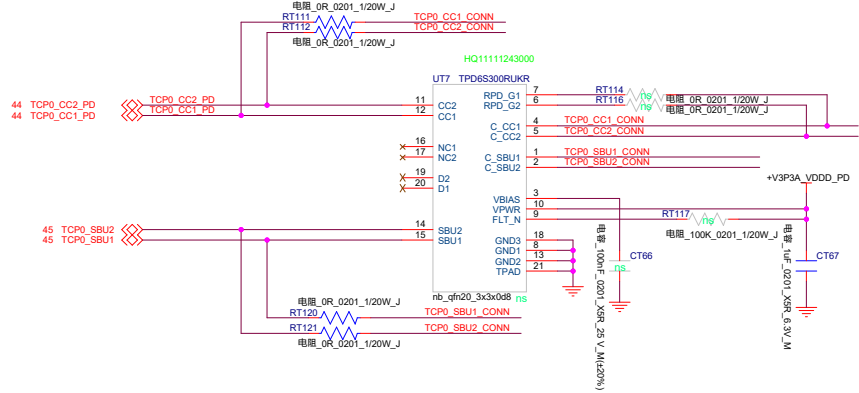
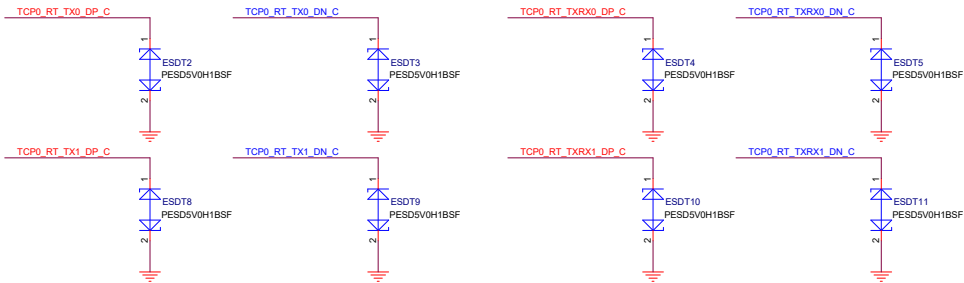
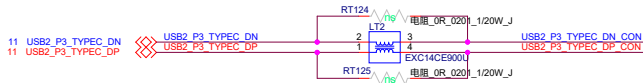
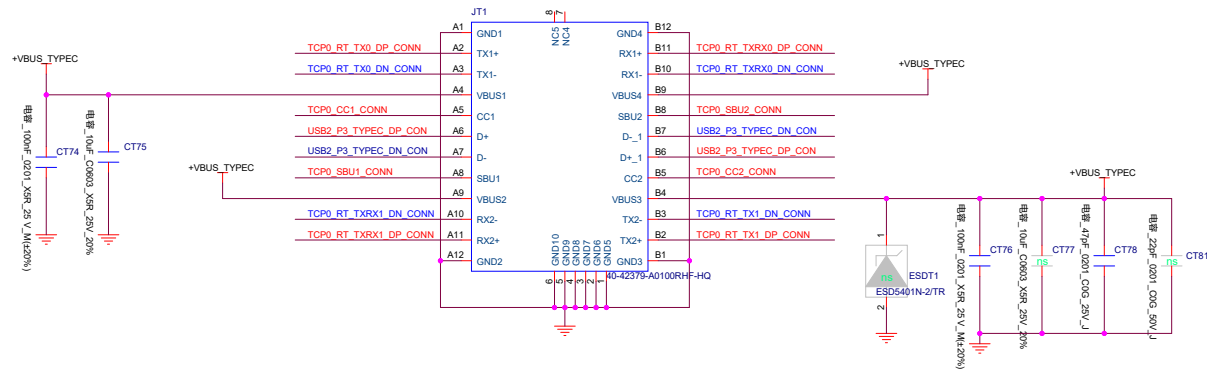
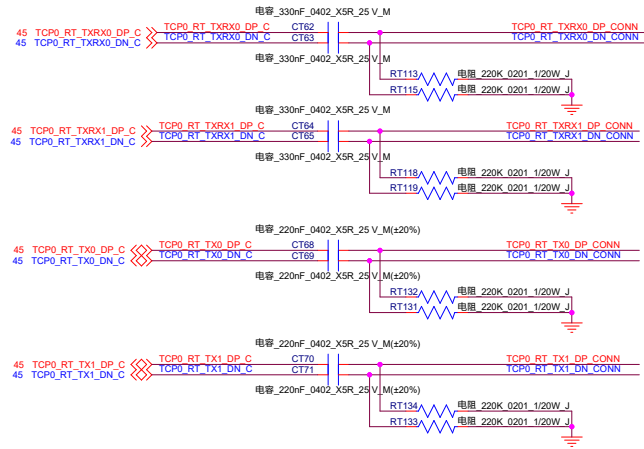


TYPEC-IN detect

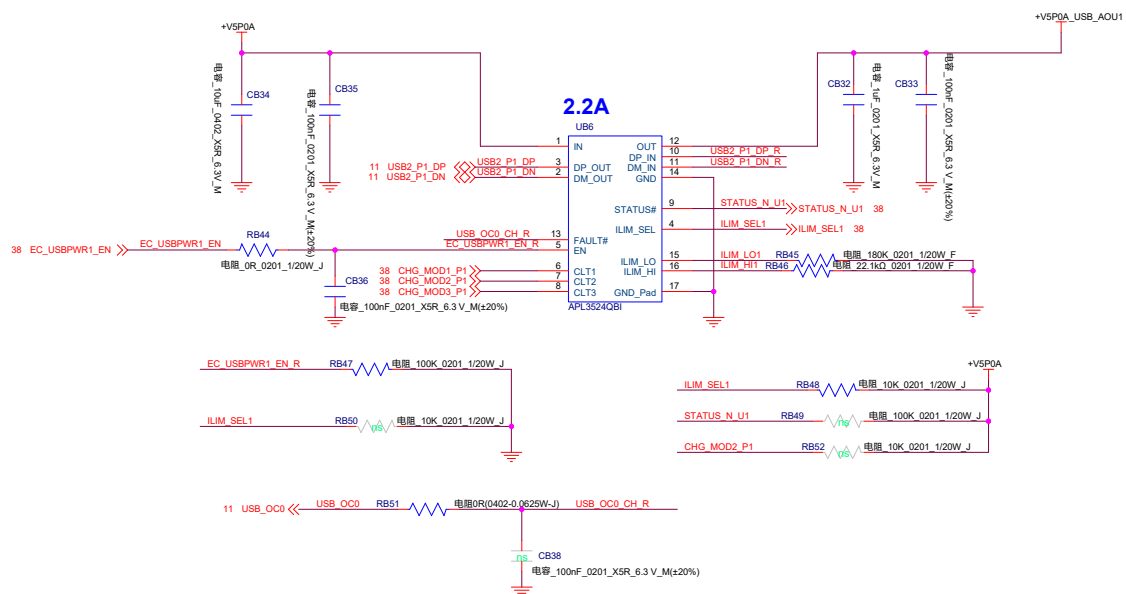


dead battery power on logic

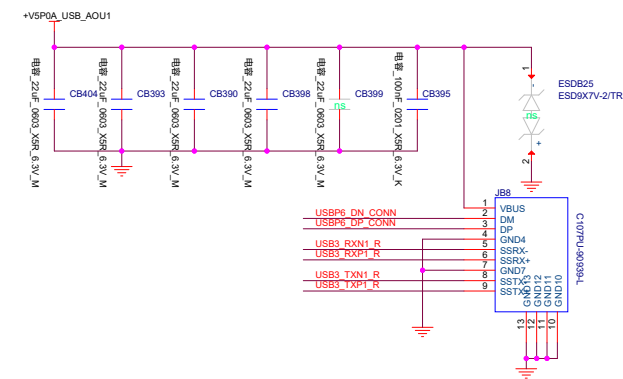
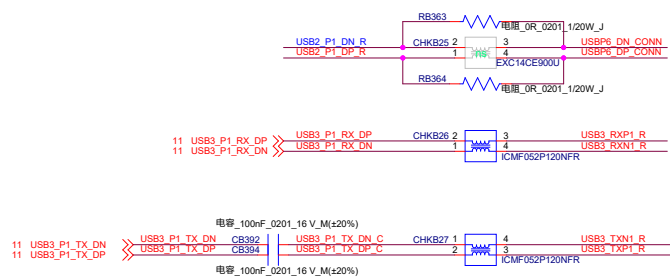
Discharge



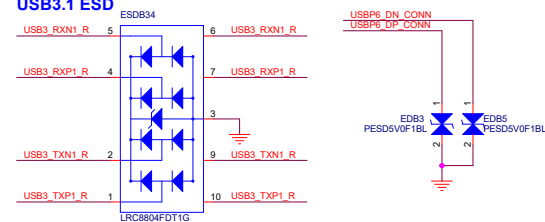
USB3.1 POWER Port1

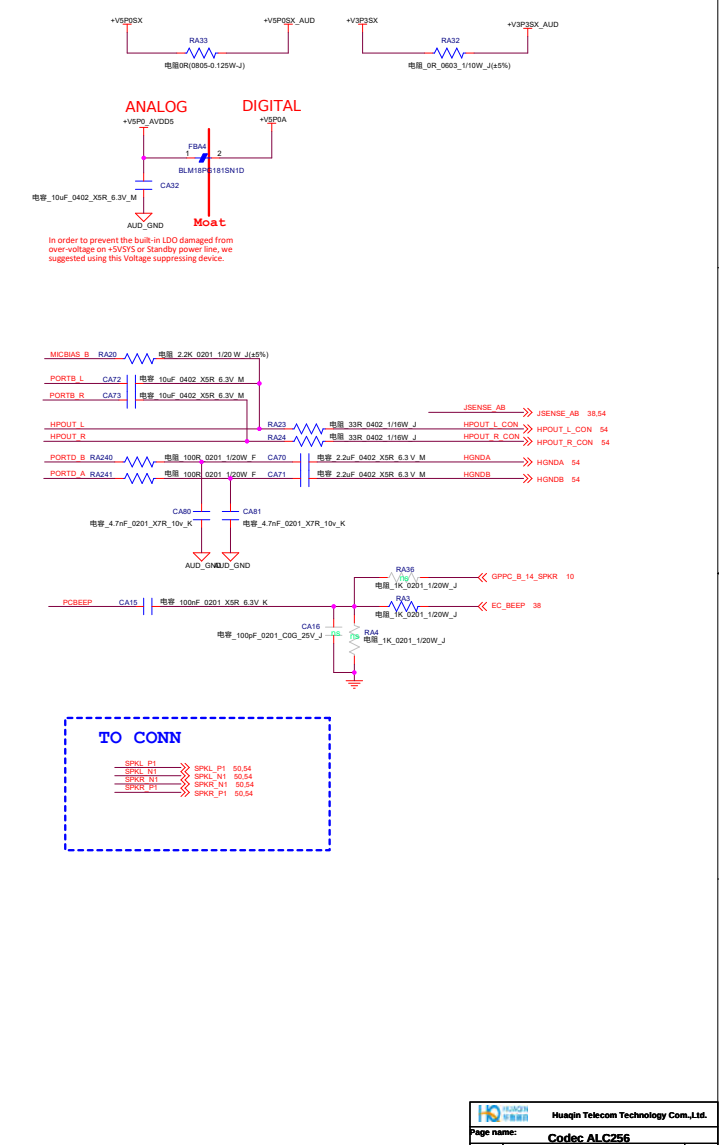
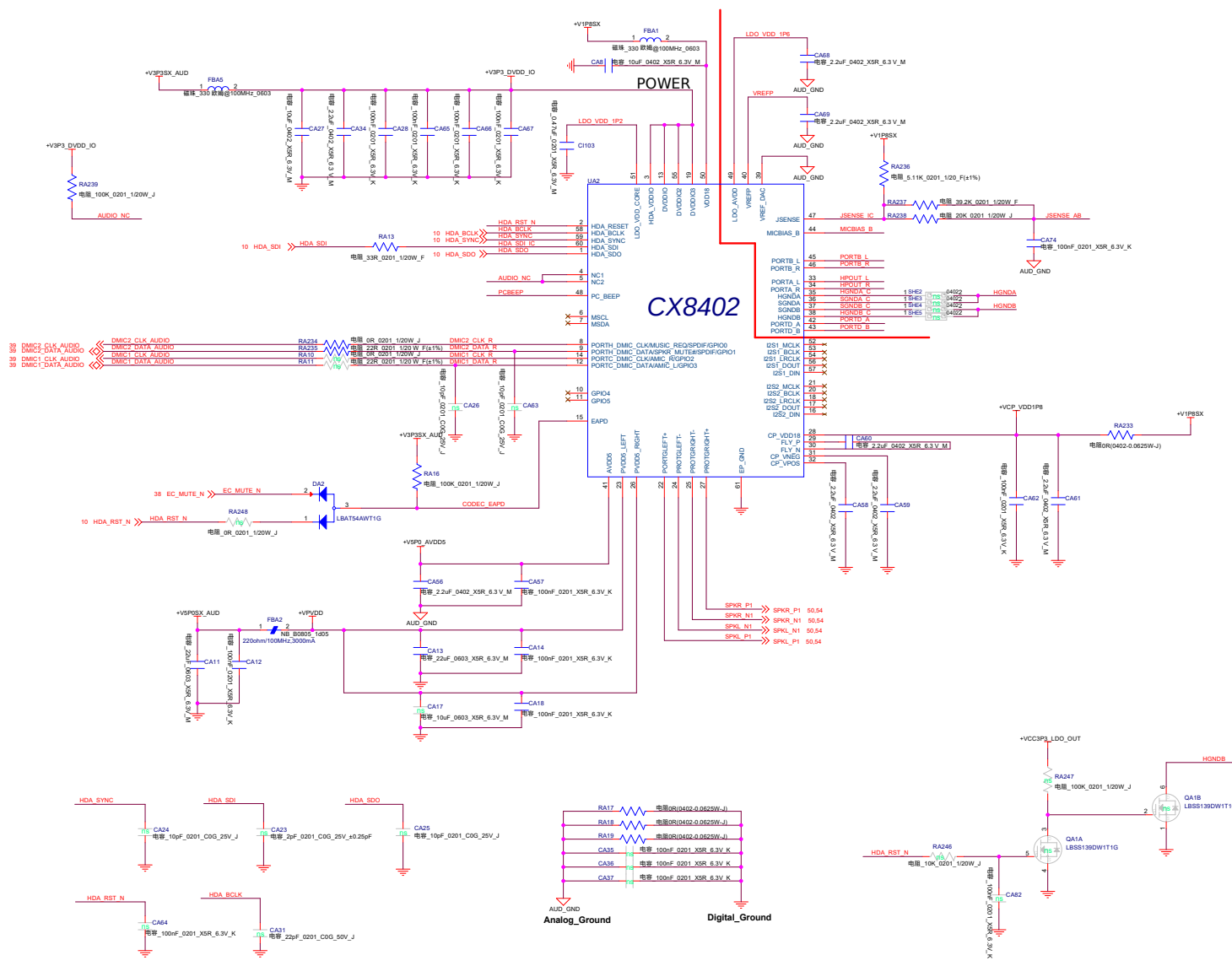


USB3.1 Signal

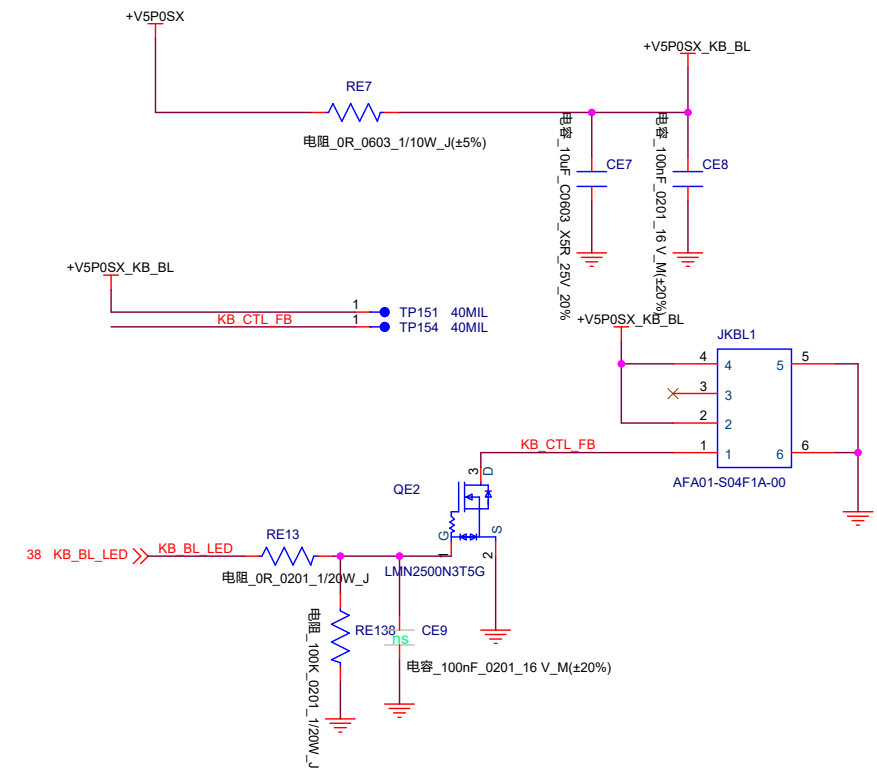


USB3.1 ESD

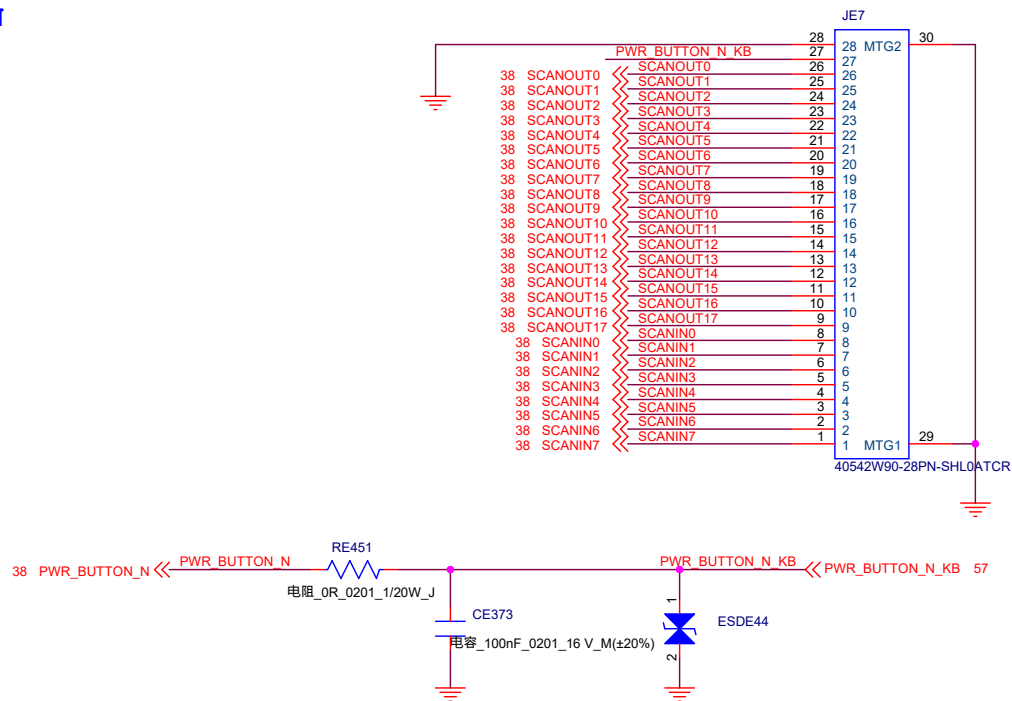




KB Backlight



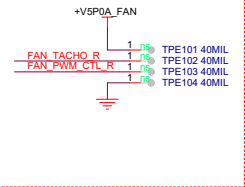
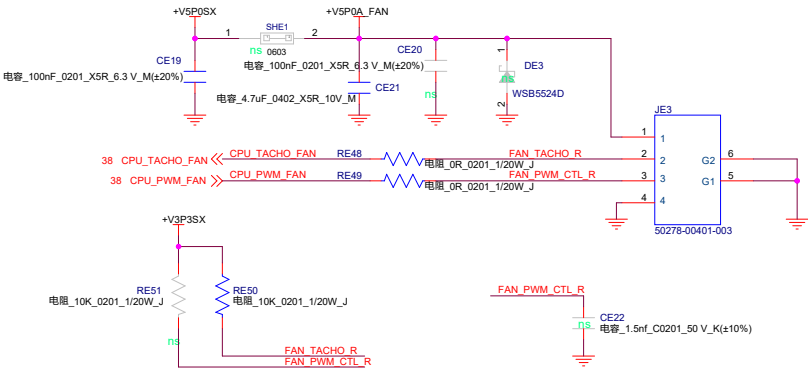
KB CONN



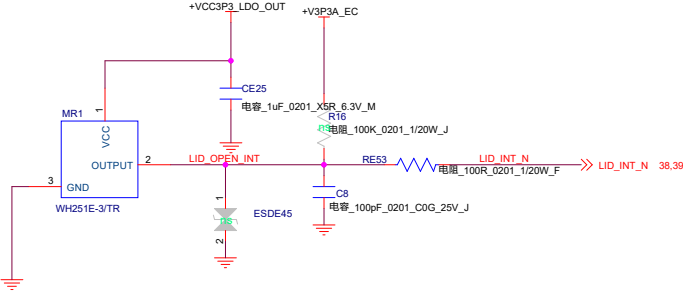
Voice input with LED-NC

FAN CONN

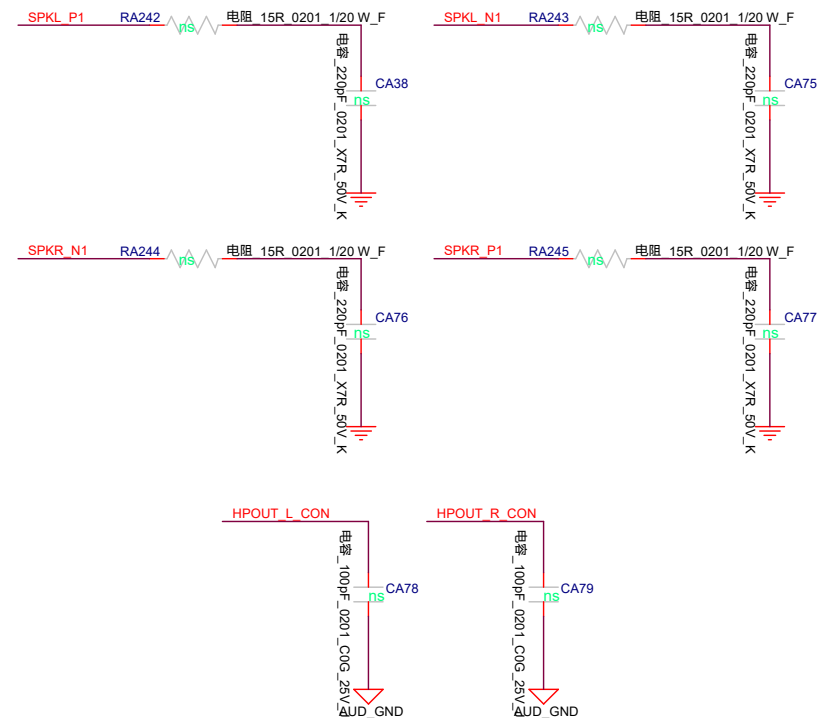
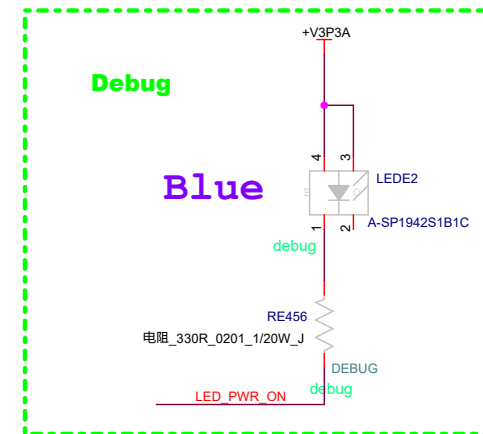
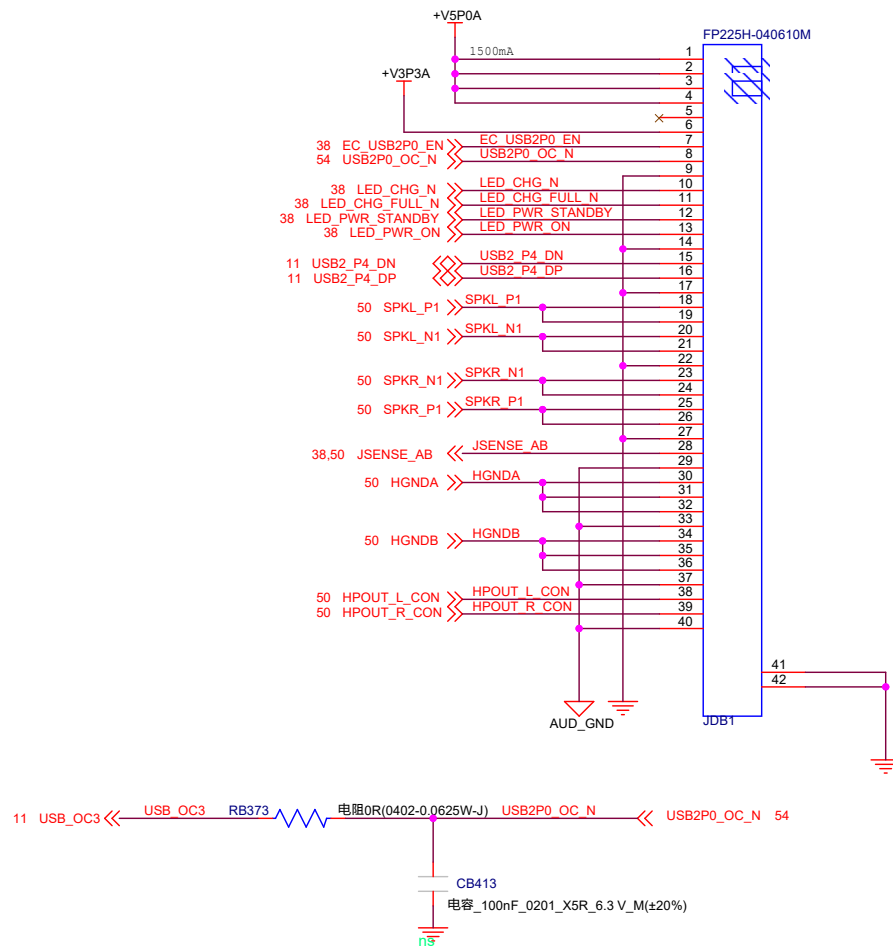
FOR product line




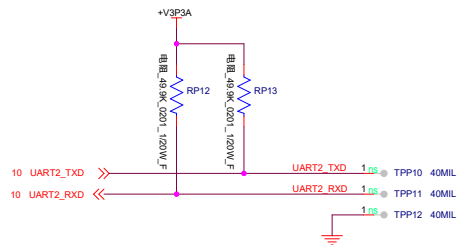
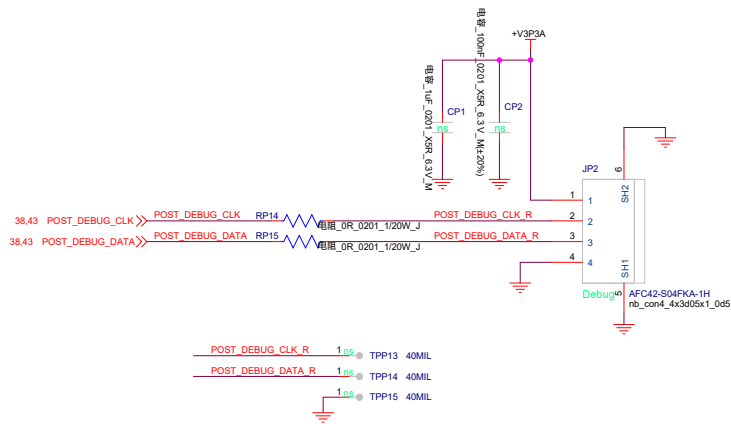
HALL



Huaqin Telecom Technology Com.,Ltd.			
Page name:	G-SENSOR/FAN/LED/Hall		
Size: A4	Project Name: NB8511	REV: V1.0	
Date: Monday, July 15, 2019	Sheet: 53	of 72	

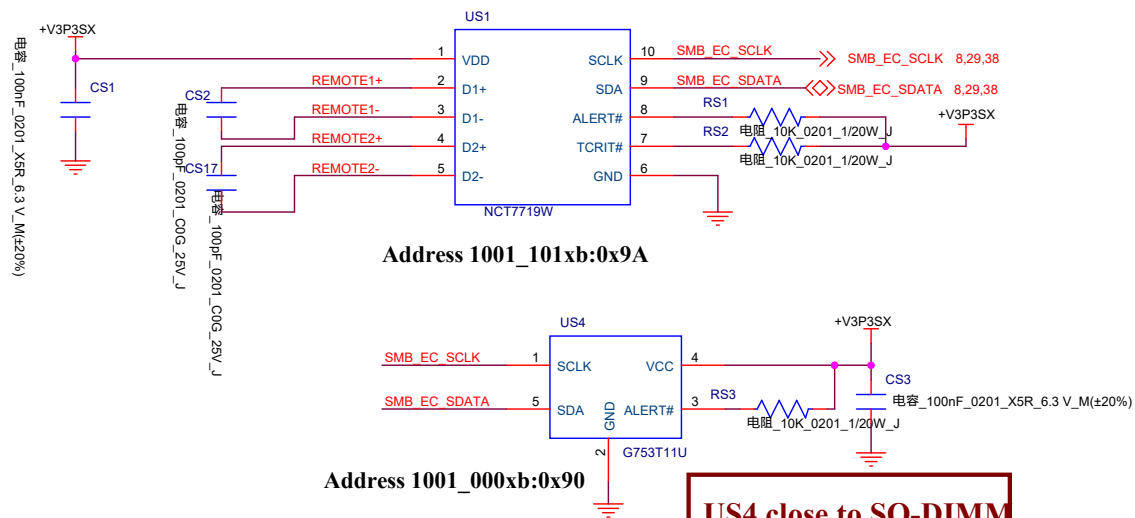


		Huaqin Telecom Technology Com.,Ltd.	
Page name: DB CONNECTOR			
Size: A4	Project Name: NB8511	REV: V1.0	
Date: Monday, July 15, 2019	Sheet: 54	of 72	




REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"
Connect guard traces to GND on either side of the
DXP-DXN traces

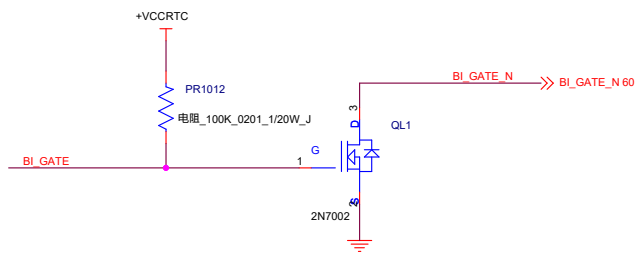
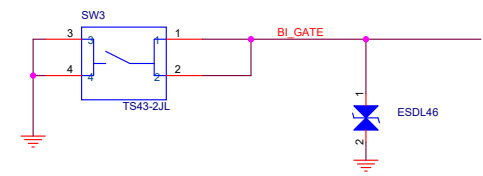
Close to charger



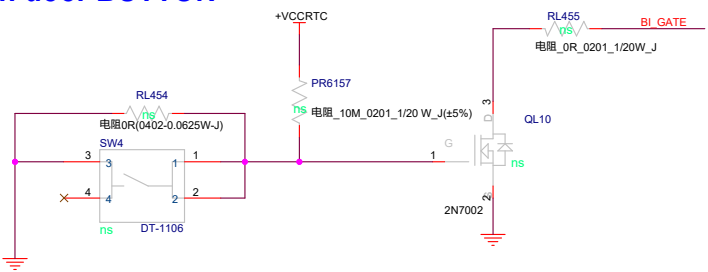
Between CPU and GPU

		Huaqin Telecom Technology Com.,Ltd.	
Page name: Thermal sensor			
Size: A4	Project Name: NB8511		REV: V1.0
Date: Monday, July 15, 2019	Sheet: 56		of 72

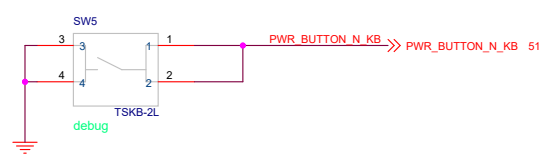
Reset BUTTON



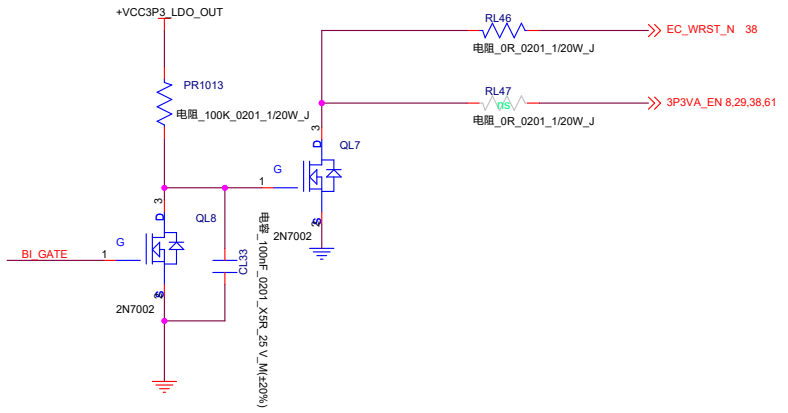
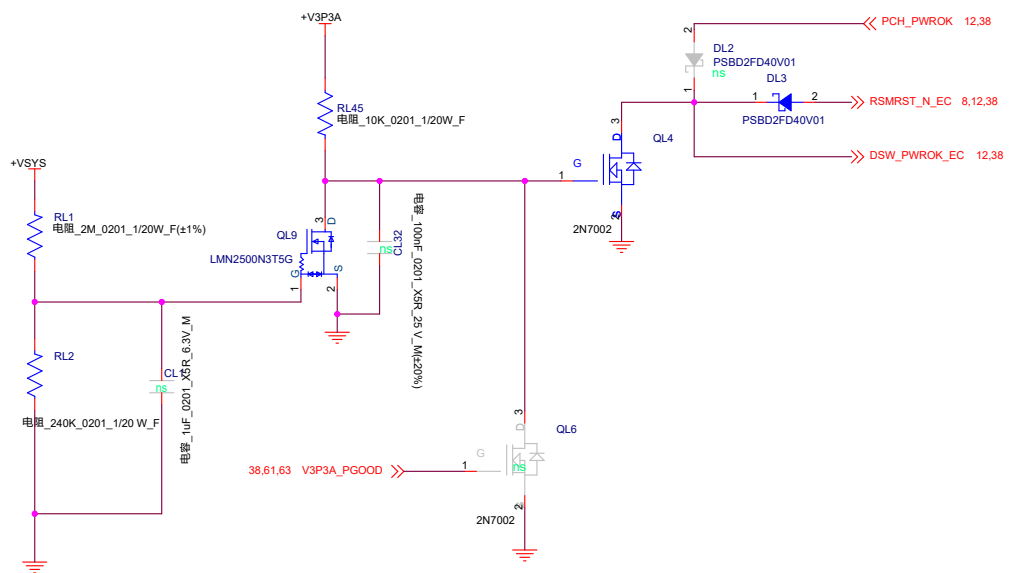
Open door BUTTON



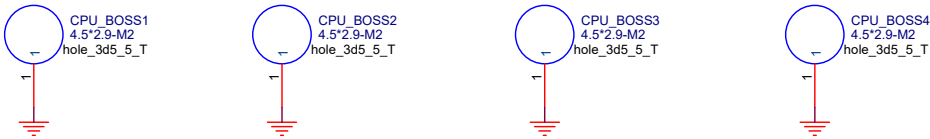
Debug BUTTON



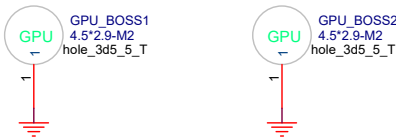
Abnormal PD logic



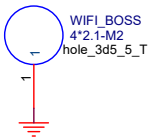
CPU螺母元件 *4



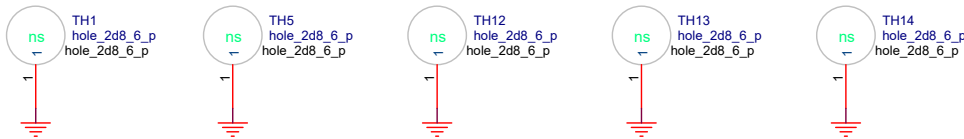
GPU螺母元件 *2



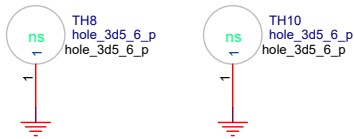
WIFI螺母元件 *1




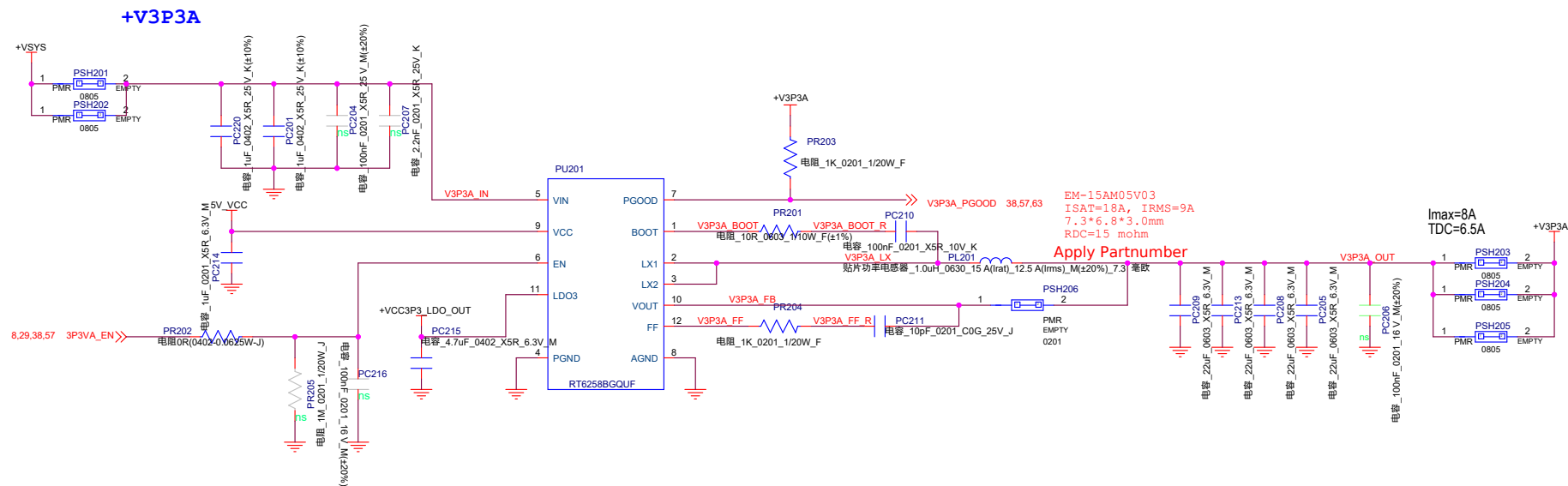
HOLE *5

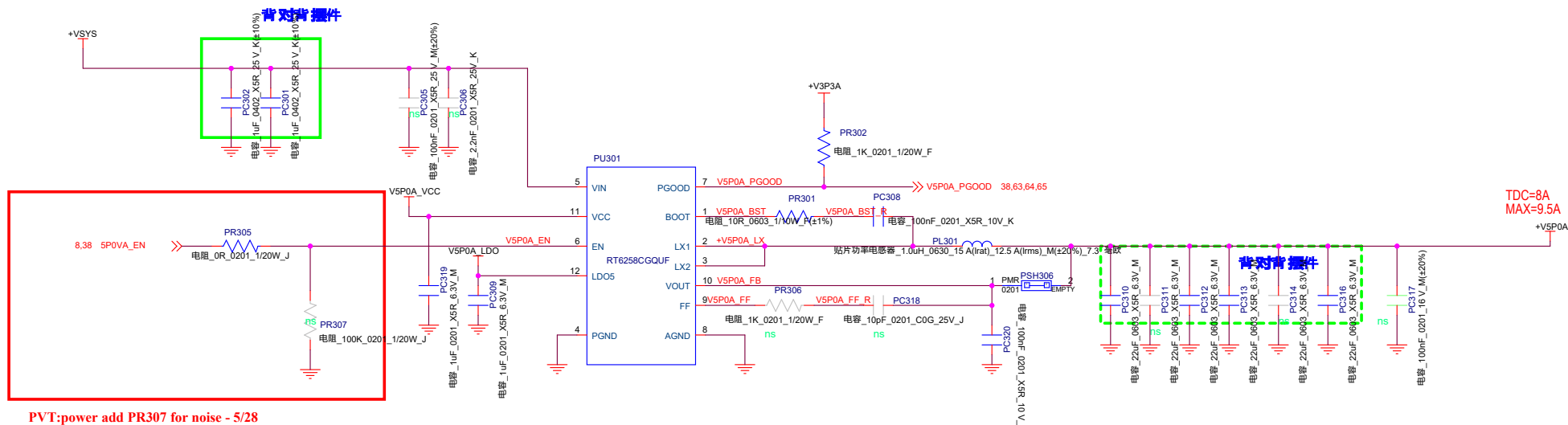


HOLE *2

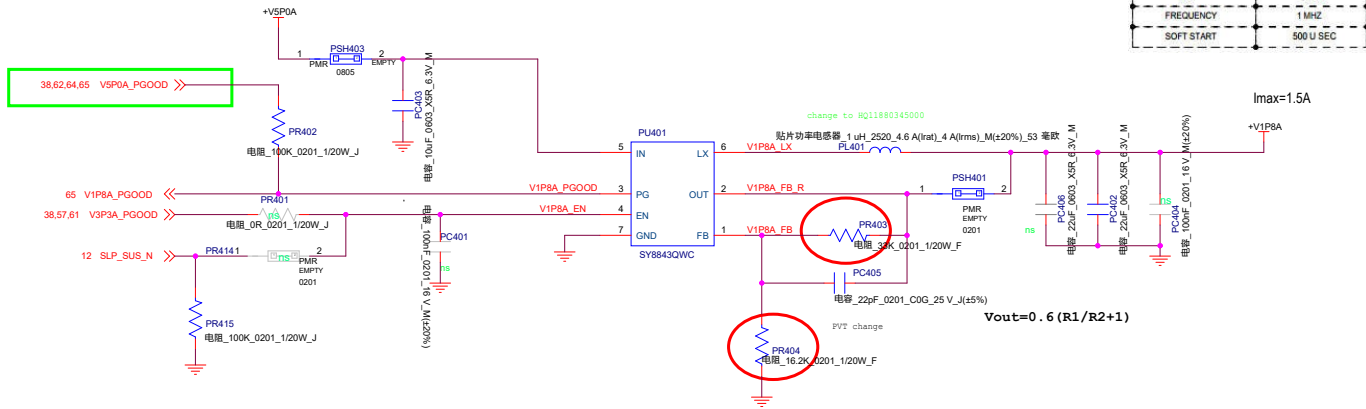


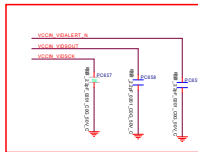
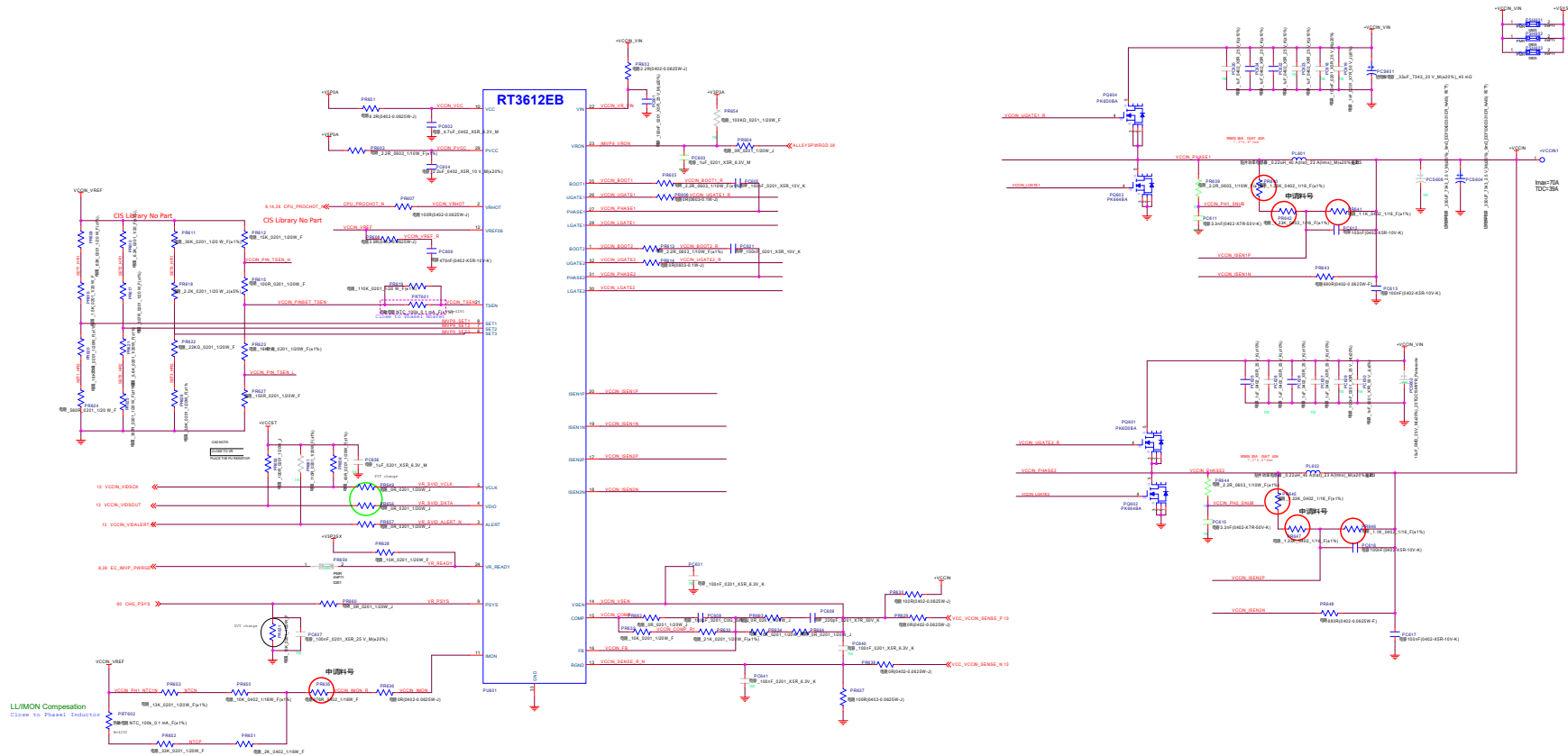
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Page name: BLANK			
Size: A4	Project Name: NB8511		REV: V1.0
Date: Monday, July 15, 2019	Sheet: 58		of 72



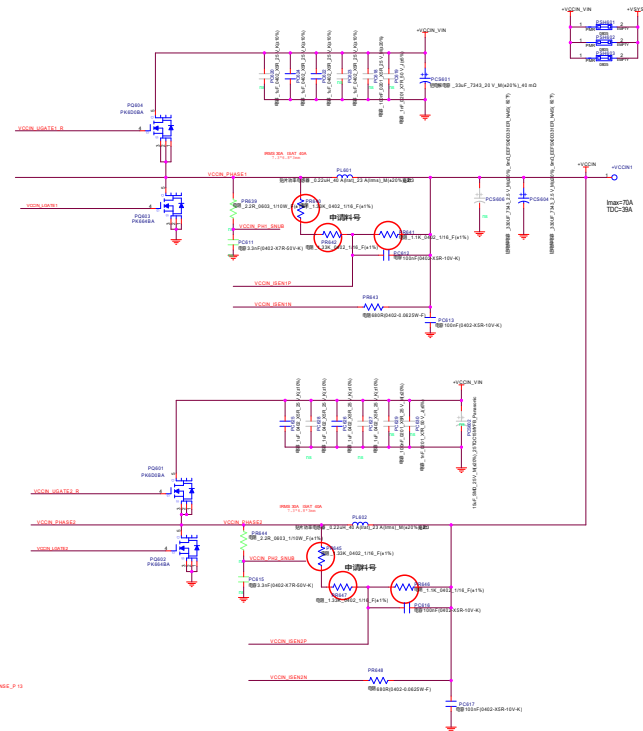


+V1P8A

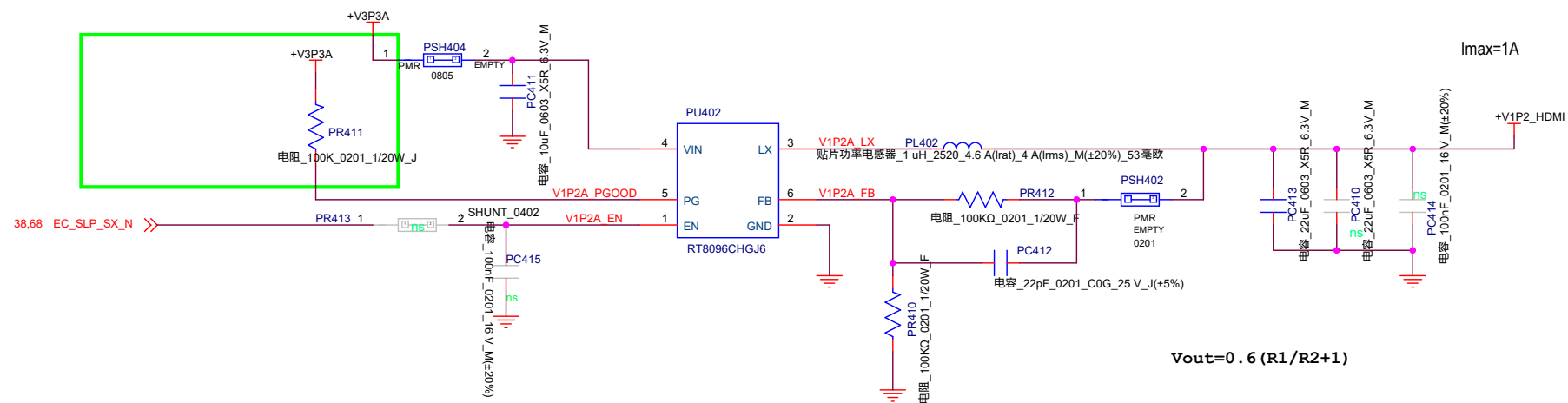


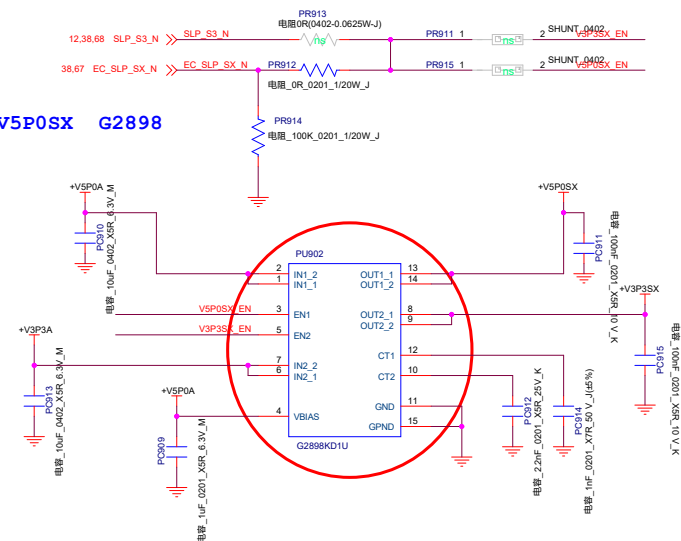
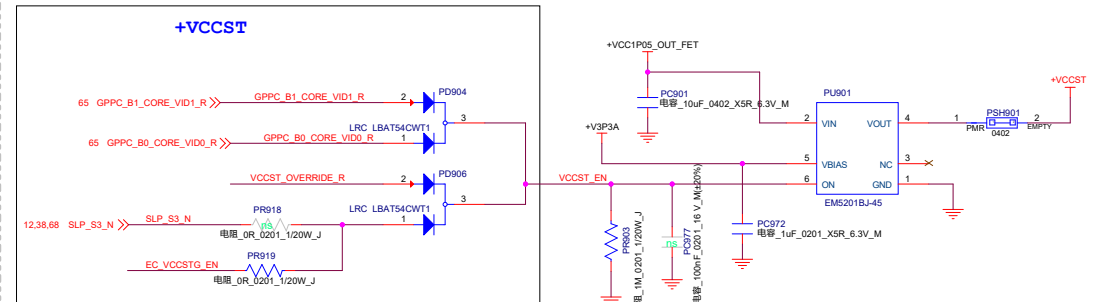


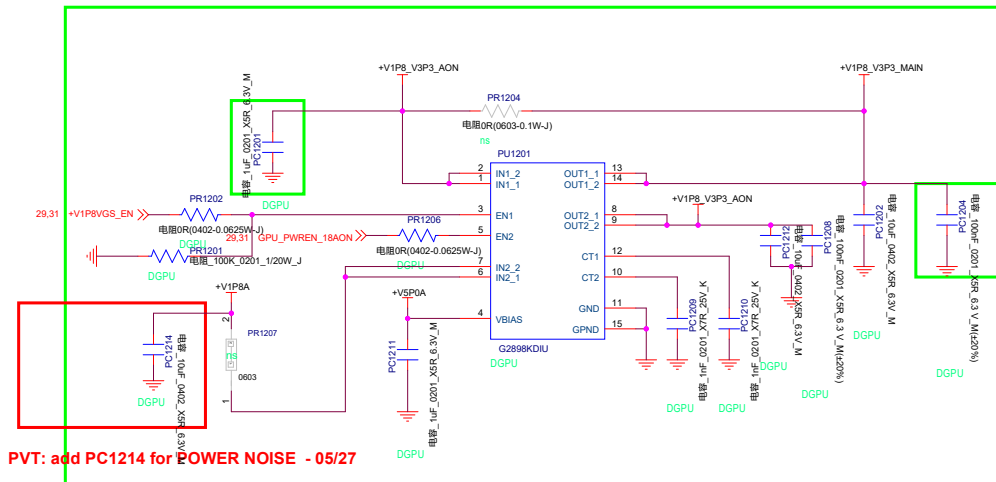
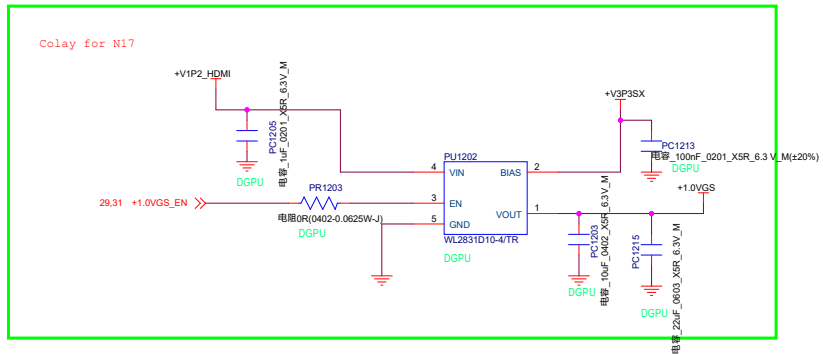
PVT/SVID signal add 2.2pf cap - 5/27

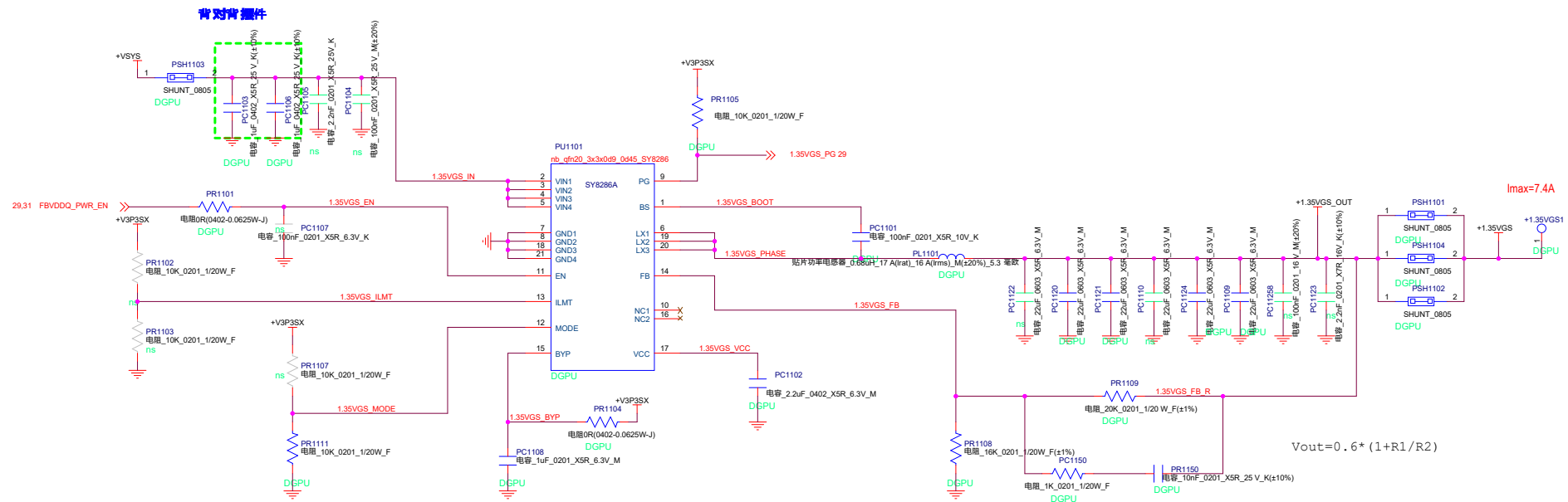


Pin Setting	FUNCTION1	FUNCTION2	FUNCTION3
SET1	EN_LV_WDRG	VDDIO1	ECBANK
SET2	ANTIDIV_TH	ALGAP	NA
SET3	Q10N	NA	NA
SET4	DISABLE	DRIVE_LPH	VH_HOT
SET5	DISABLE	DRIVE_LPH	DRIVE_LPH









stuff reduce S0 power consumption 11/5

PR1150:0Ω-10kΩ
PC1150:100pF-1nF 11/5

ILMT=Low	6.7	7.8	8.9	A
ILMT=Floating	9.3	10.6	11.9	A
ILMT=High	12	13.3	14.8	A

