

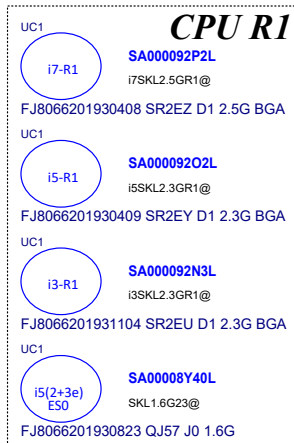
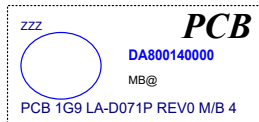
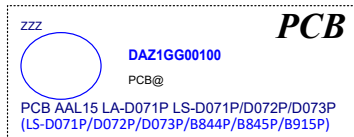
COMPAL CONFIDENTIAL

MODEL NAME : AAL15
PCB NO : DA800140000
BOM P/N :
GPIO MAP:

SKL-U+MEC1404 VC board

2015-07-09

REV : 1.0 (A00)



@ : Nopop Component

i3SKL2.3GR1@/i5SKL2.3GR1@/i7SKL2.5GR1@/SKL1.6G23R1@:CPU R1
i3SKL2.3GR3@/i5SKL2.3GR3@/i7SKL2.5GR3@/SKL1.6G23R3@:CPU R3
UMA@/DIS@ : UMA & DIS Type

DSX@/N_DSX@: DSX Mode

EMI@/ESD@/HDMI@EMI@/RF@ : EMI, ESD and RF Component

@EMI@/@ESD@/@RF@ : EMI, ESD and RF Nopop Component

CMC@ : XDP Component

CONN@ : Connector Component

100@/1000@/LAN_SW@ : LAN type

3234@/3246@ : CODEC type

CRT@/HDMI@ : CRT/HDMI

TP_WAKE@/NOTP_WAKE@ : TouchPad wake

ODD@/NOZPODD@/ZPODD@ : ODD and Zero Power

EXOR1@/MESOR1@ : GPU R1

EXOR3@/MESOR3@ : GPU R3

EXO@/MESO@ : GPU relative component

2G_H@/2G_S@/2G_M@/4G_H@/4G_S@/4G_M@ : VRAM type

V_4G@ : 4G VRAM Support component

Layout Dell logo



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REV: X00
PWB: 9HTP8

<http://www.repair1.ru/>

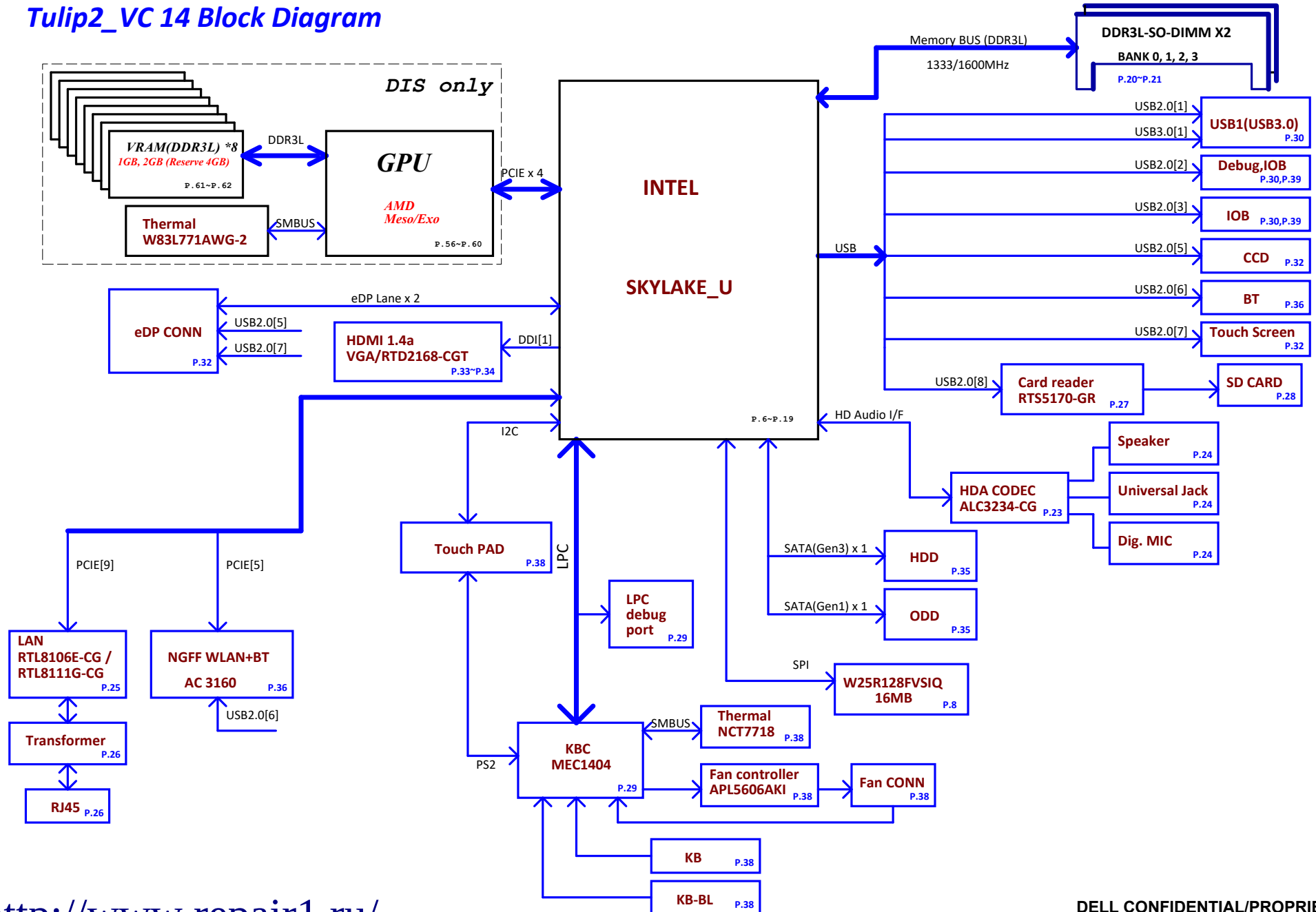
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Tulip2_VC 14 Block Diagram



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Block diagram		
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

State \ power plane	+1.0V_PRIM +RTC_CELL +1.8V_EDRAM +1.8V_PRIM +5VALWP +3VALWP +5VALW +3VALW +1.0V_MPHYGT +1.0V_PRIM_CORE +3.3V_ALW_DSW	+3VALW_PCH +1.0V_VCCST	+1.35V_MEM +1.0V_VCCSTG +VCC_CORE +VCC_GT +1.0VS_VCCIO +VCC_SA +VCC_EDRAM +VCC_EOPIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Board ID & Model ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10.0	3.000	Pre-EVT
2	100	13.7	2.902	EVT
3	100	17.8	2.801	DVT1
4	100	22.1	2.703	DVT2
5	100	27.0	2.598	
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	
15	100	120.0	1.500	
16	100	137.0	1.392	
17	100	154.0	1.299	
18	100	200.0	1.100	
19	100	232.0	0.994	

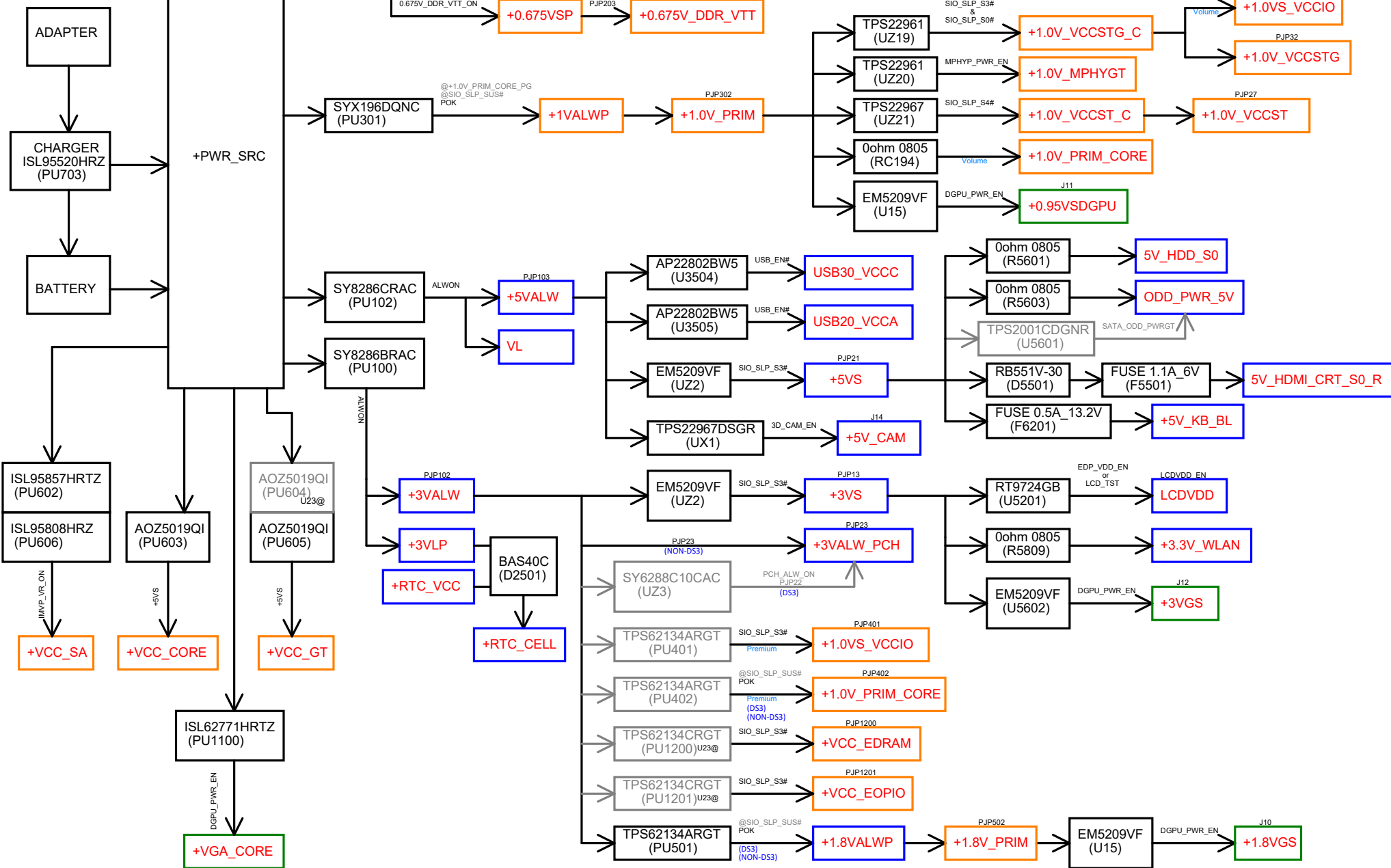
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USB3.0-2	SSIC-1			N/A
USB3.0-3	SSIC-2			N/A
USB3.0-4				N/A
USB3.0-5		PCIE-1		GPU
USB3.0-6		PCIE-2		GPU
		PCIE-3		GPU
		PCIE-4		GPU
		PCIE-5		WLAN
		PCIE-6		LAN/GLAN
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	SATA ODD
		PCIE-9		N/A
		PCIE-10		N/A
		PCIE-11	SATA-1*	N/A
		PCIE-12	SATA-2	N/A

USB PORT#	DESTINATION
1	USB3.0 Port1
2	IO/DB
3	IO/DB
4	N/A
5	CCD
6	Card Reader
7	Touch Screen
8	BT
9	N/A
10	N/A


COMPRESSED
IMAGE

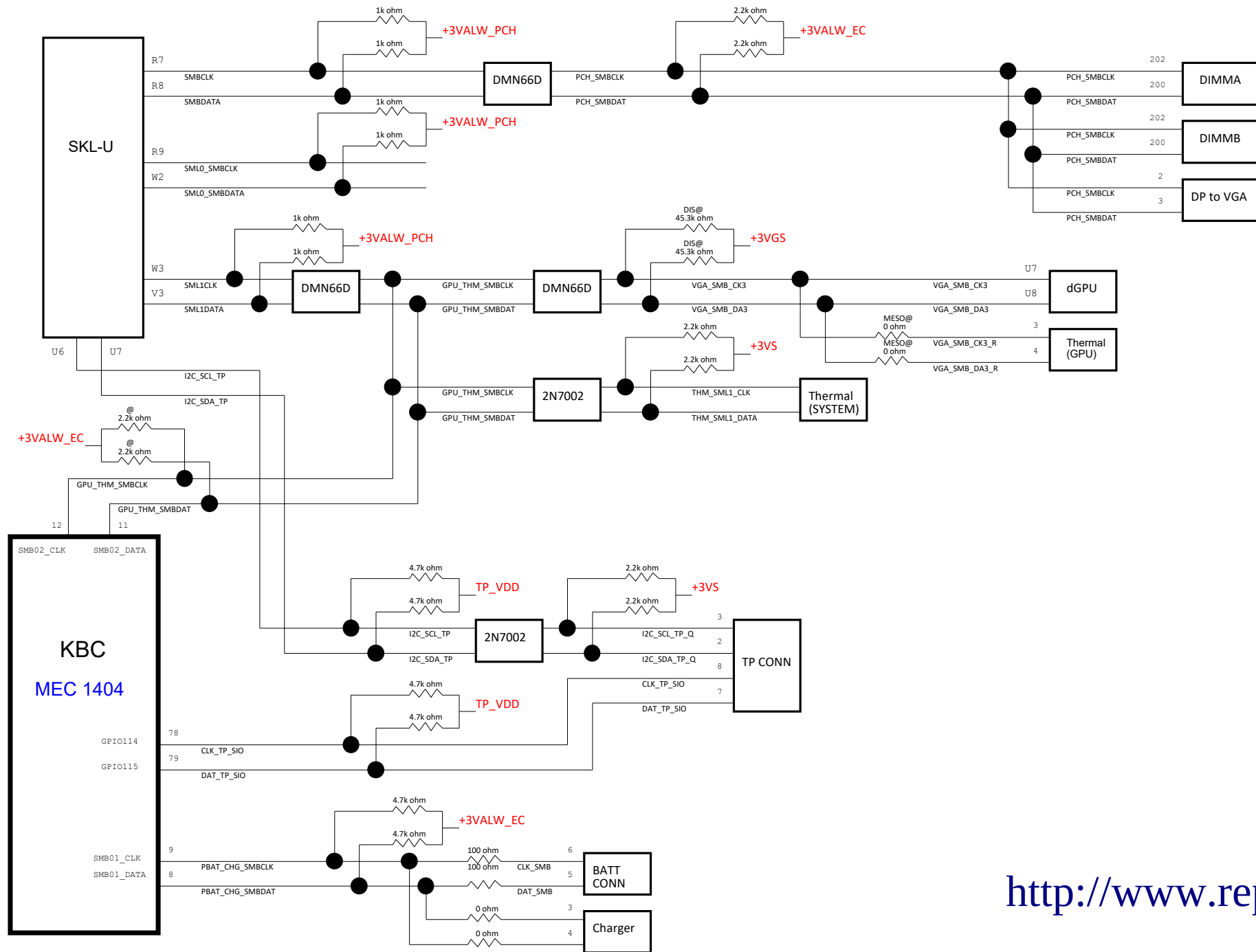
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	Power rails		
	Size	Document Number	Rev
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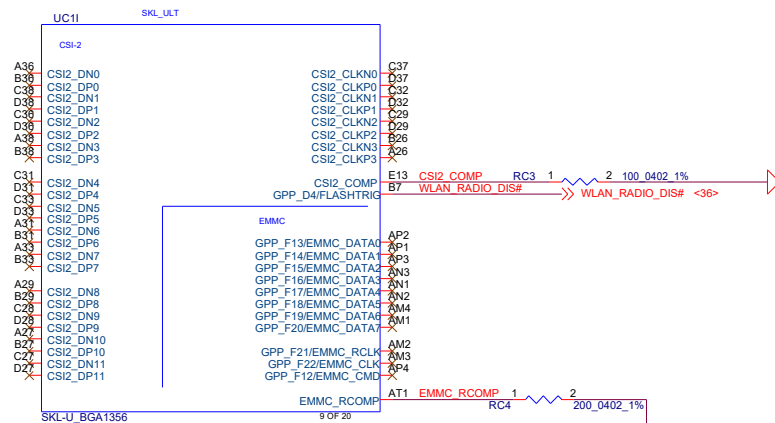
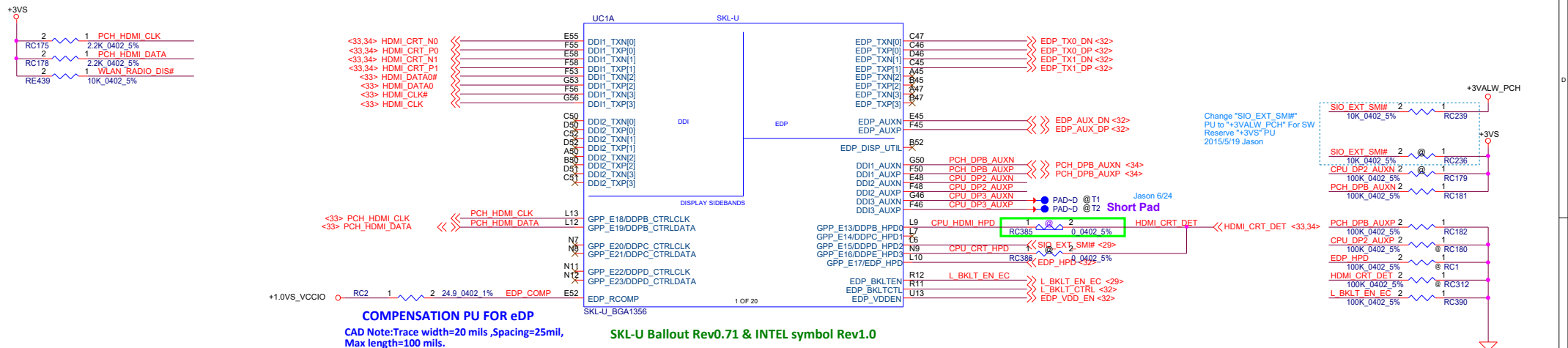
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Computer Electronics, Inc.			
Title			
SMBus Block diagram			
Size	Document Number		Rev
	LA-D071P		1.0(400)
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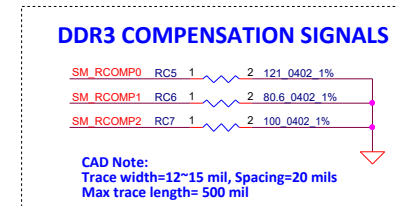
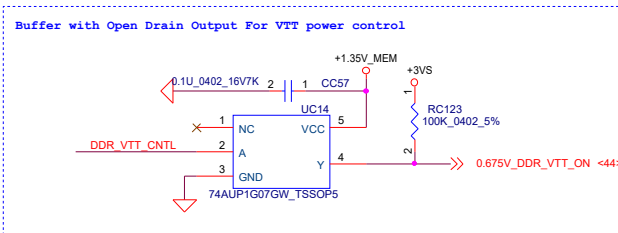
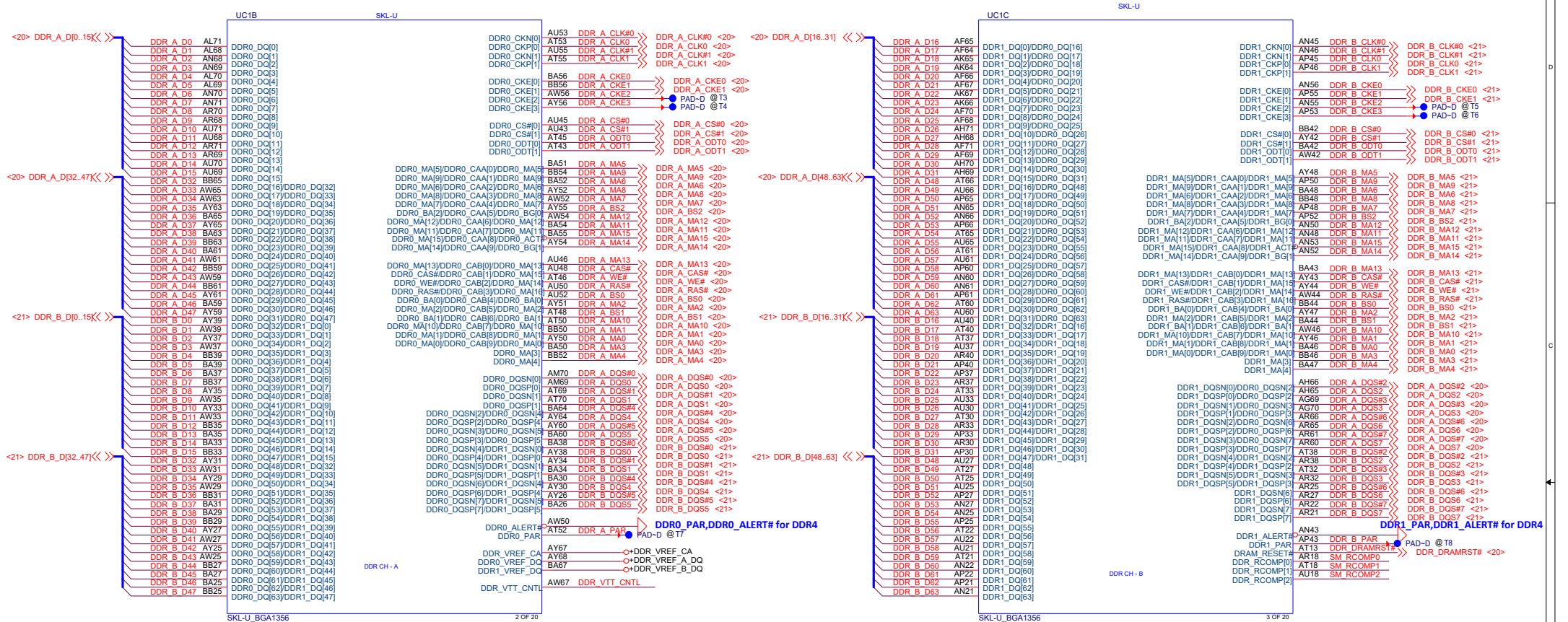
CPU (1/14)

LA-D071P

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DDR3L, Ballout for side by side(Non-Interleave)



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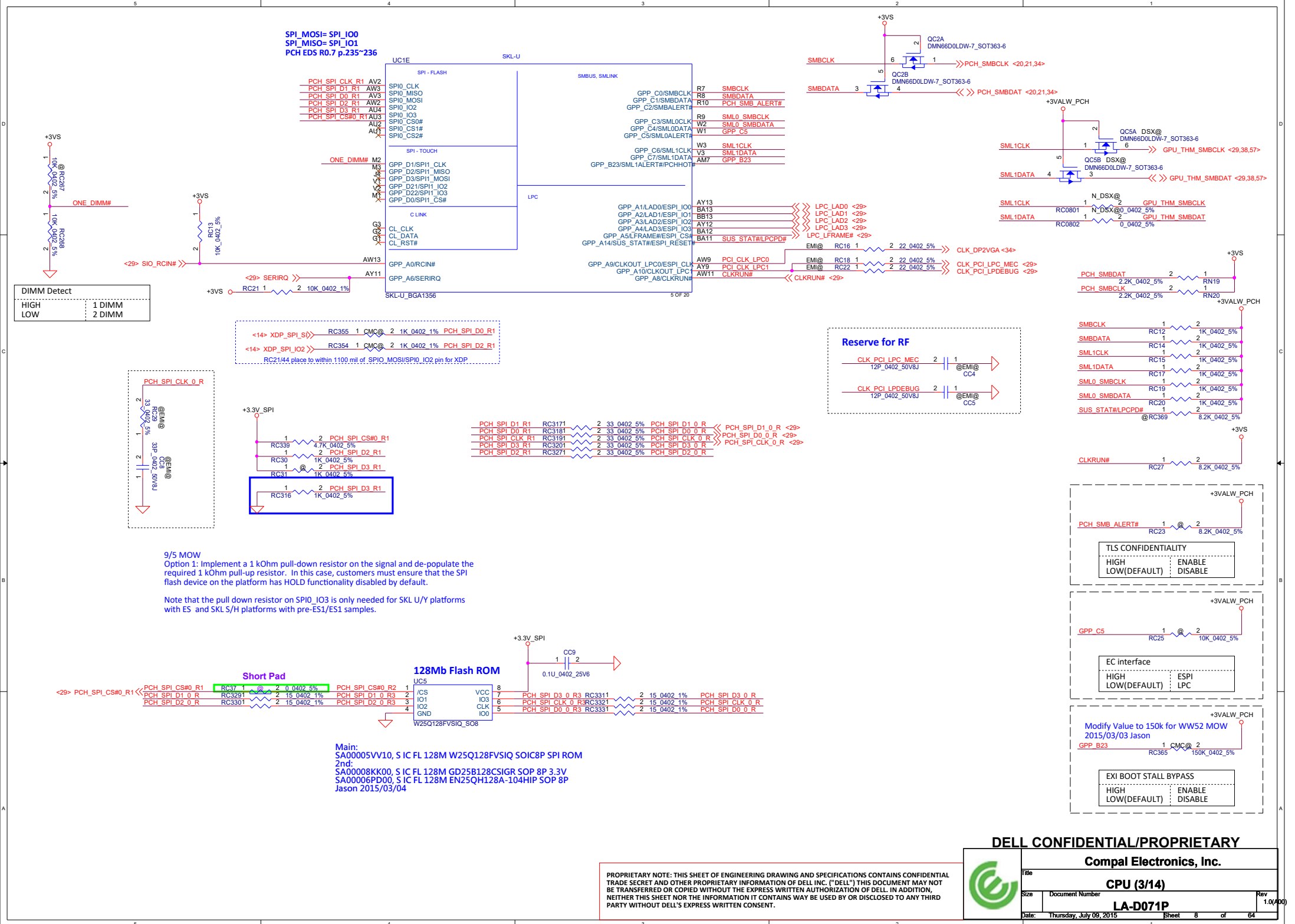
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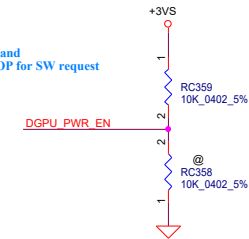
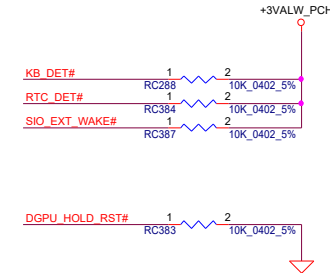
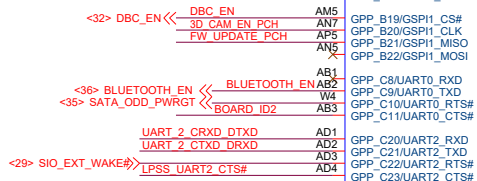
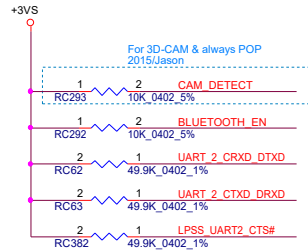
CPU (2/14)

LA-D071P

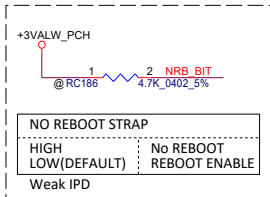
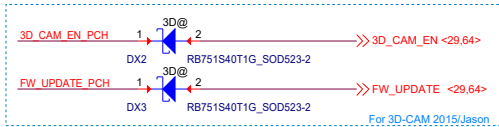
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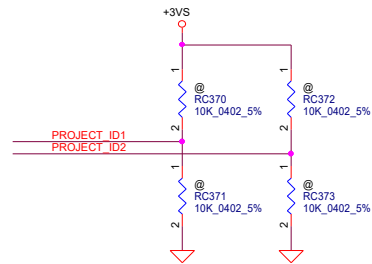
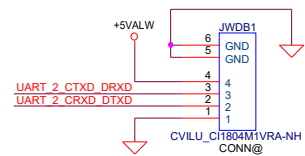


Add RC359 10kOhm PU and Change RC358 to UN-POP for SW request 2015/04/28 Jason

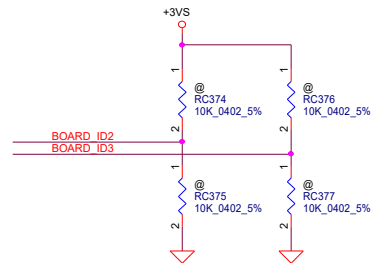


Win7 Debug solution

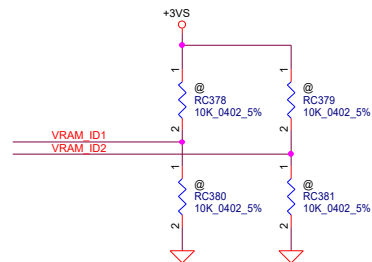
Option 2 : For Open Chassis Platforms



Reserve for TULIP/VanGogh MB switch



Reserve for MB Platform(SKL) switch



Reserve for VRAM Type switch

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CPU (4/14)

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GPU ---->

WLAN ---->

GLAN ---->

SATA HDD ---->

SATA ODD ---->

+3VS

RC245

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2

10K_0402_5%

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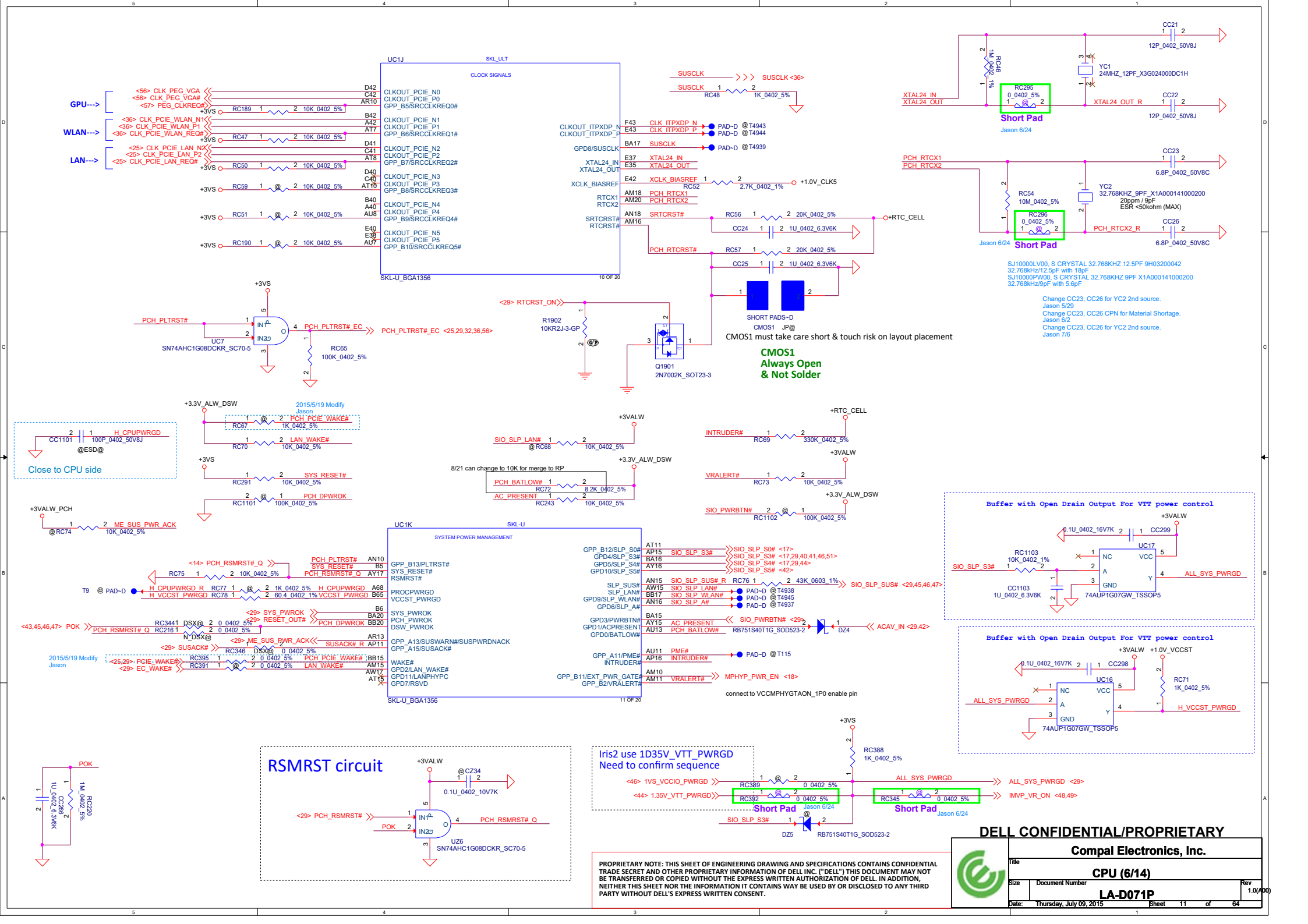
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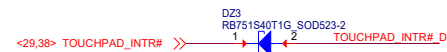
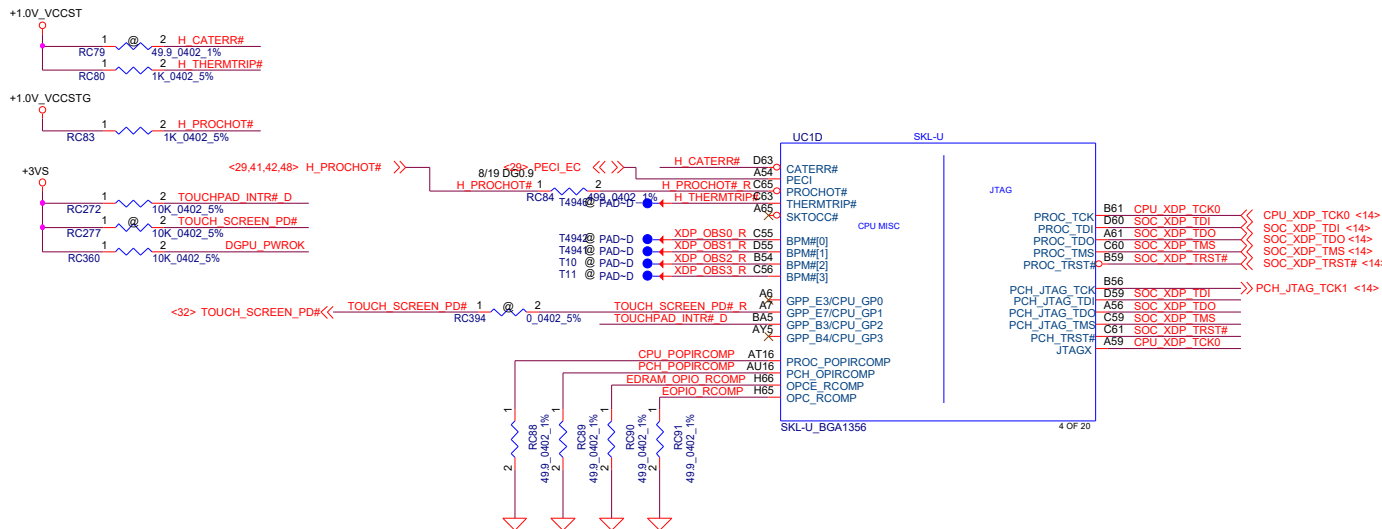
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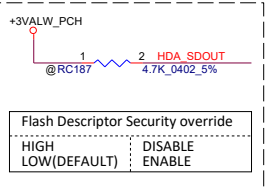
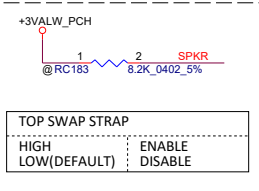
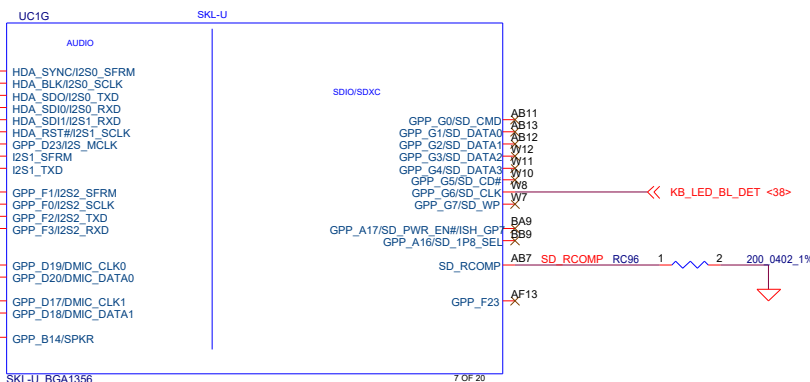
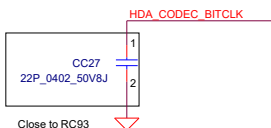
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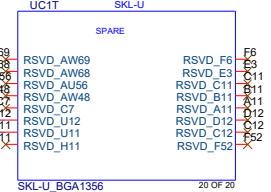
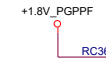
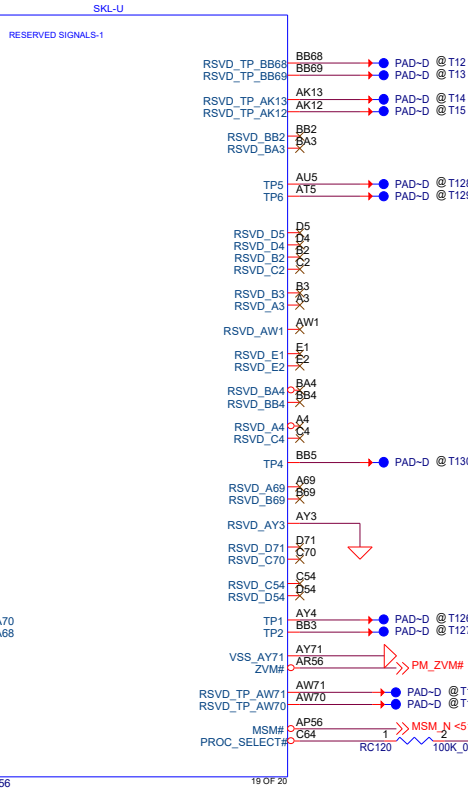
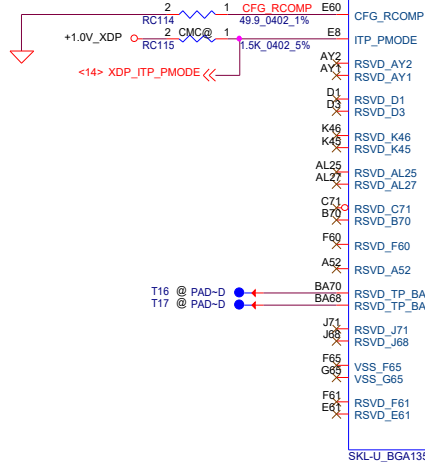
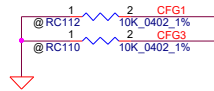
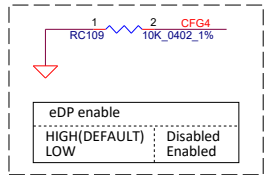
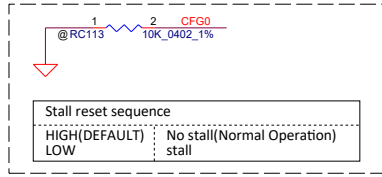


ME_FWP_EC

- LOW = ENABLE --> ME lock, can't update ME
- HIGH = DISABLE --> ME un-lock, can update ME



CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin



ZVMM for SKYLAKE-U 2+3e
MSM6 for SKYLAKE-U 2+3e

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CPU (8/14)

LA-D071P

File

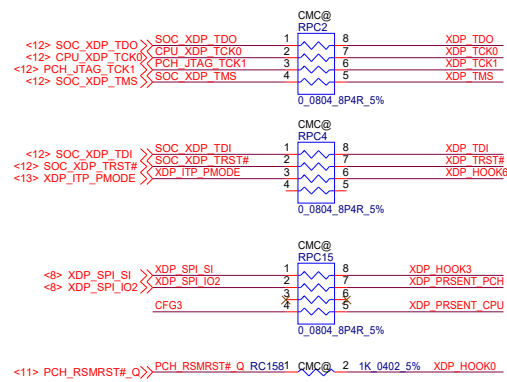
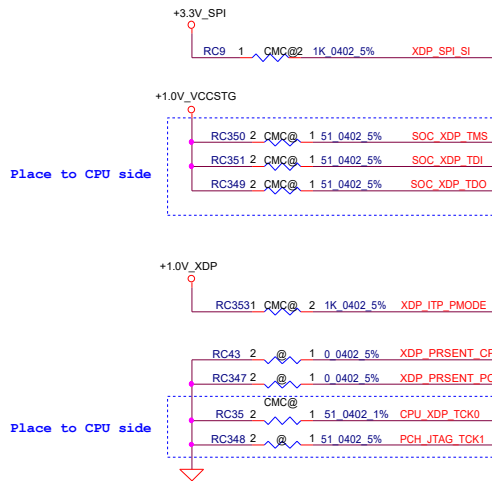
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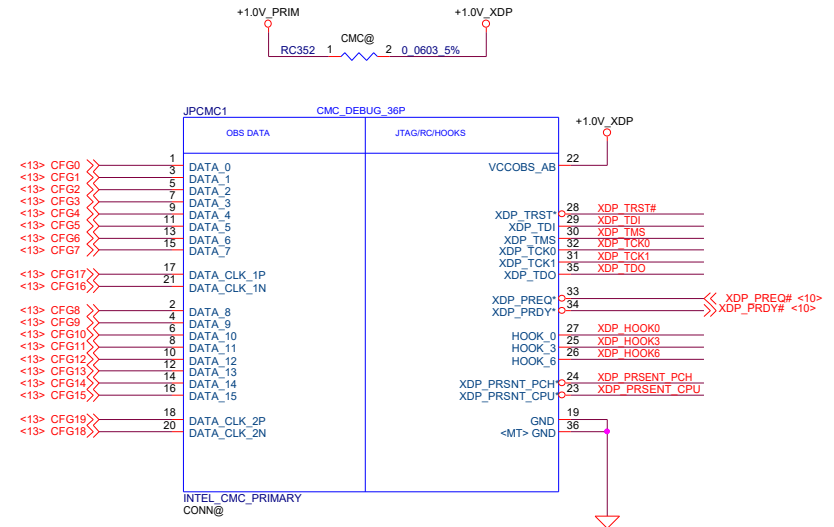
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PRIMARY CMC CONN



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Compal Electronics, Inc.

CPU (9/14)

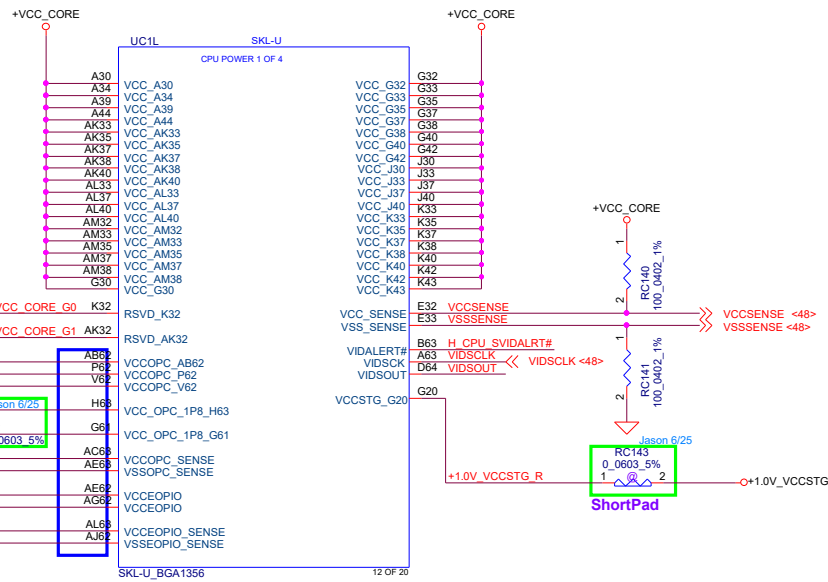
LA-D071P

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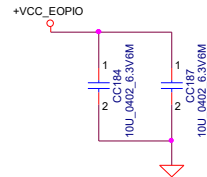
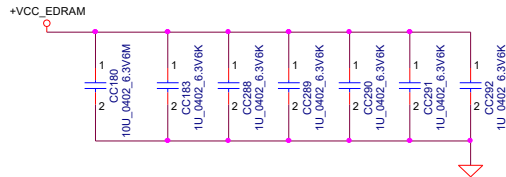


Title		Rev	
Size	Document Number	1.0	400
Date:	Thursday, July 09, 2015	Sheet	14 of 64

+VCC_CORE: 0.3~1.35V



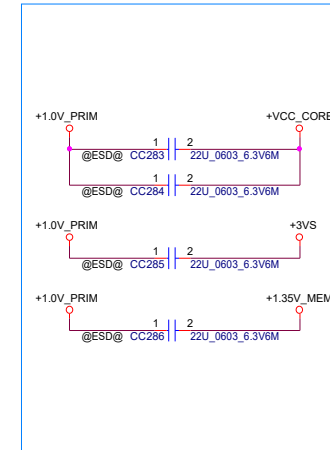
VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e
(w/ on package cache)



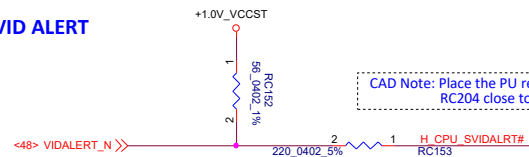
PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

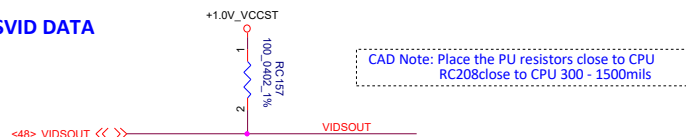
ESD Request



SVID ALERT



SVID DATA



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DELL CONFIDENTIAL/PROPRIETARY



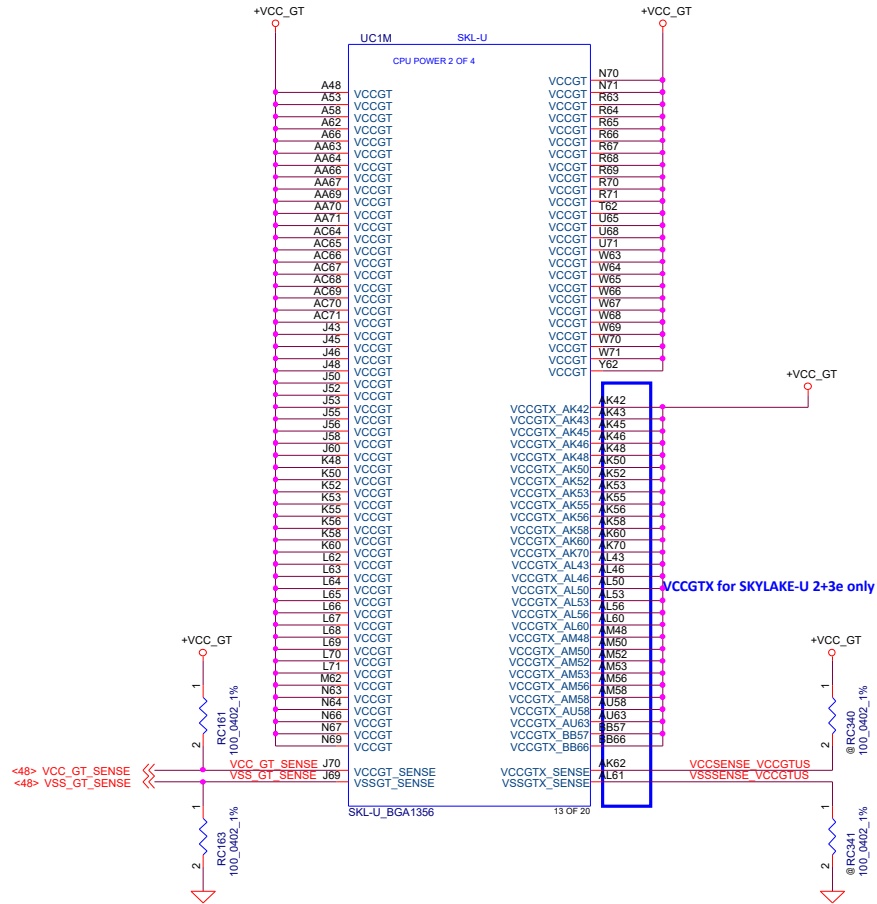
Compal Electronics, Inc.

CPU (10/14)

LA-D071P

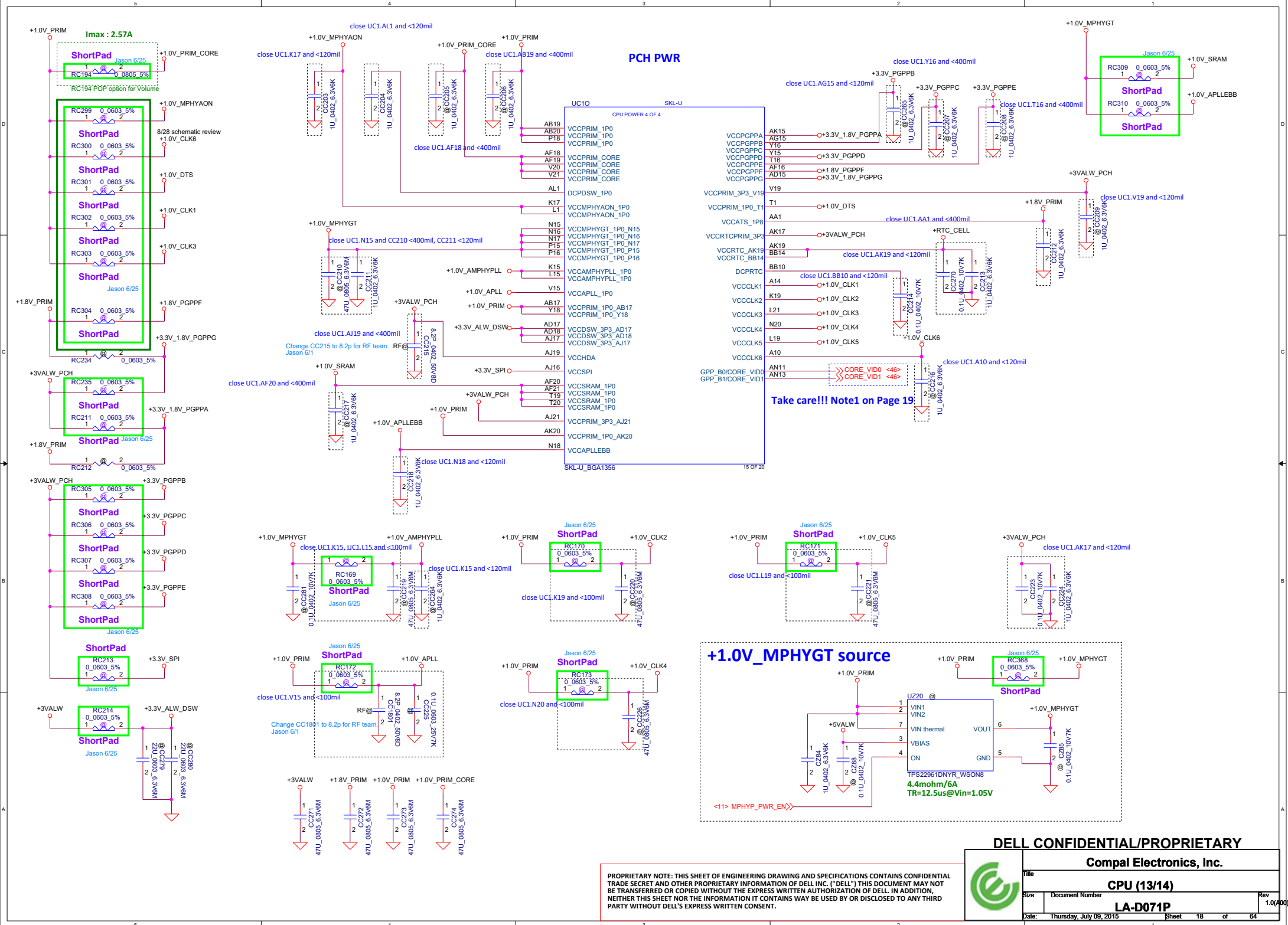
Title		Document Number		Rev
Size		Date		1.0(400)
Thursday, July 08, 2015		Sheet 15 of 64		

+VCCGT: 0.3~1.35V
+VCCGTx : 0.3~1.35V

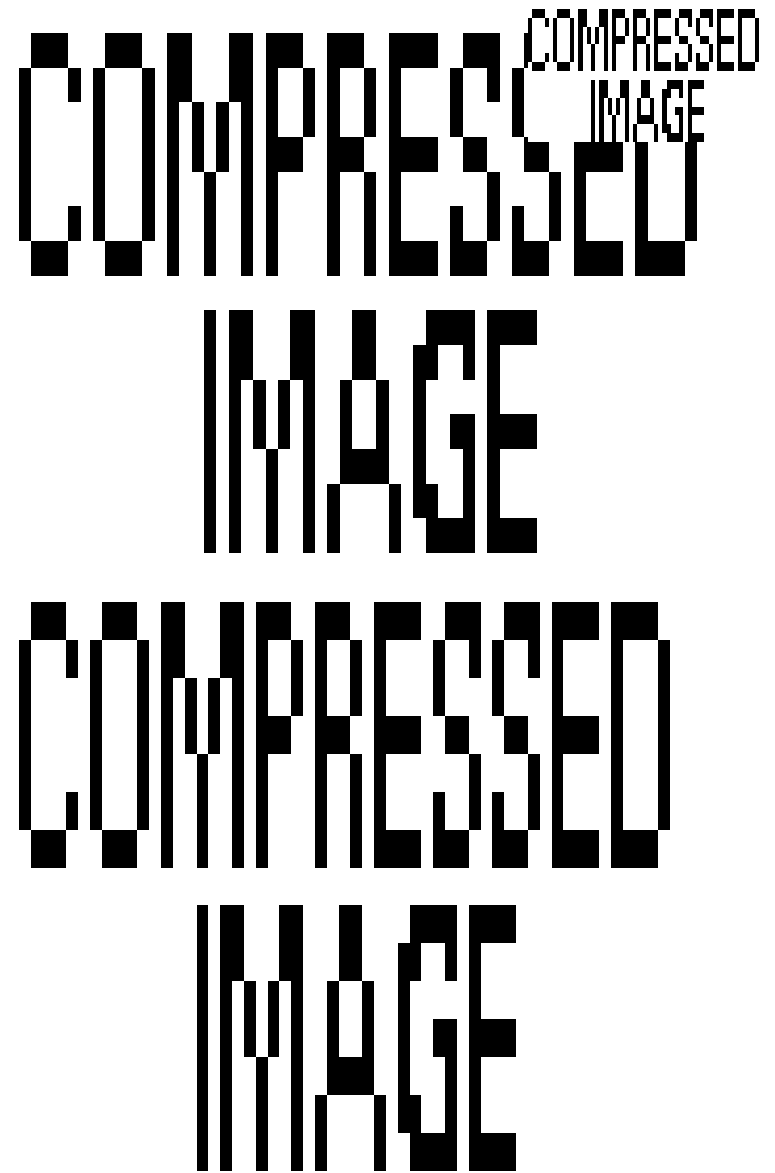



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Compal Electronics, Inc.			
Title CPU (11/14)			
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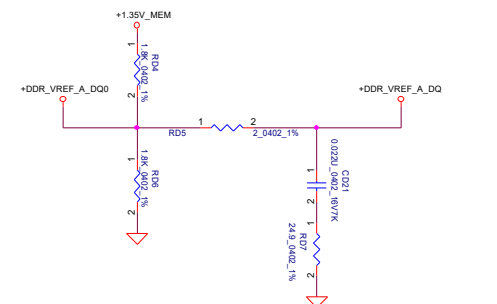
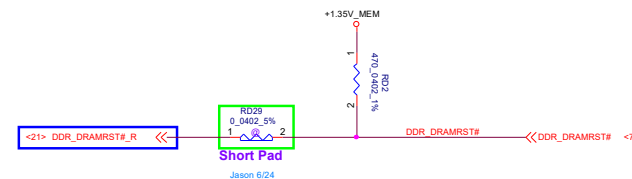
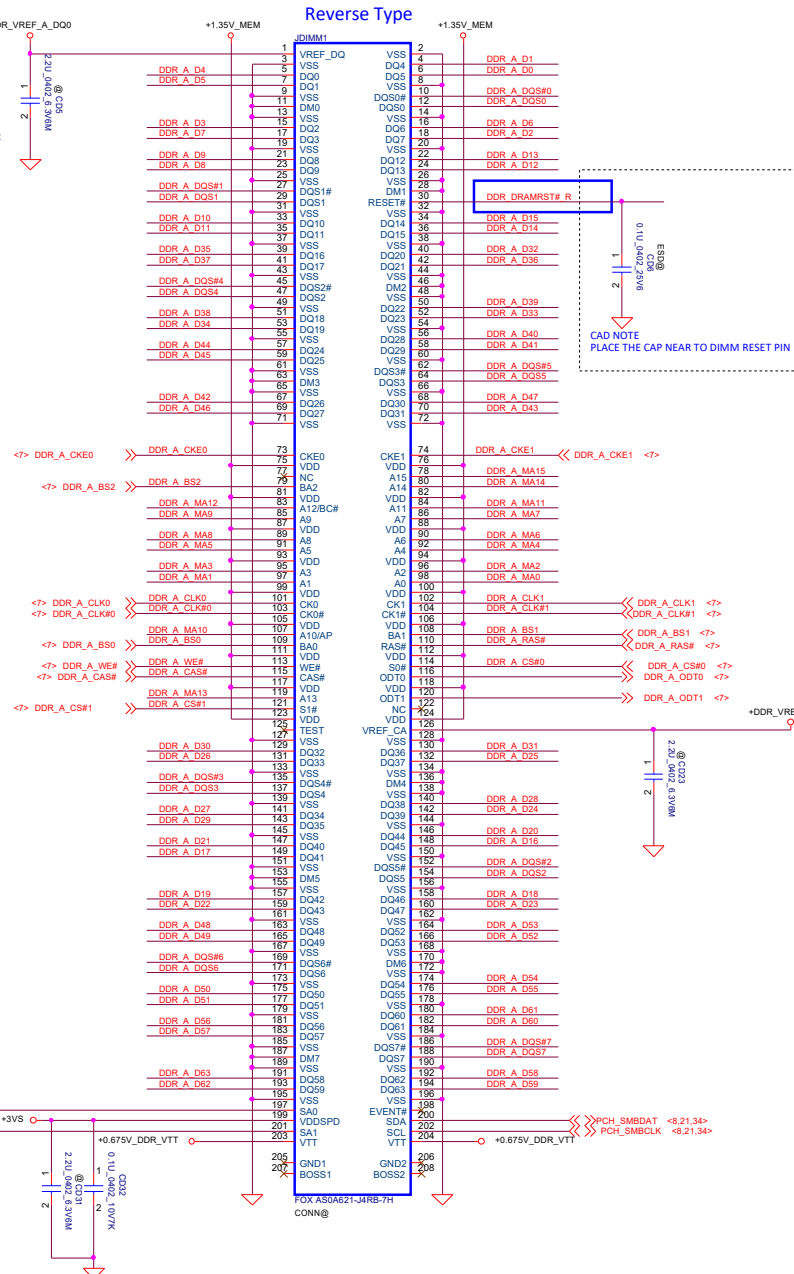
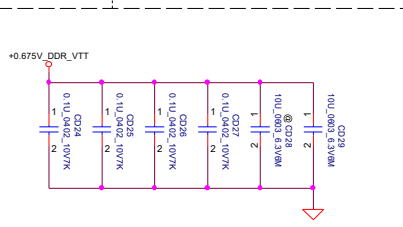
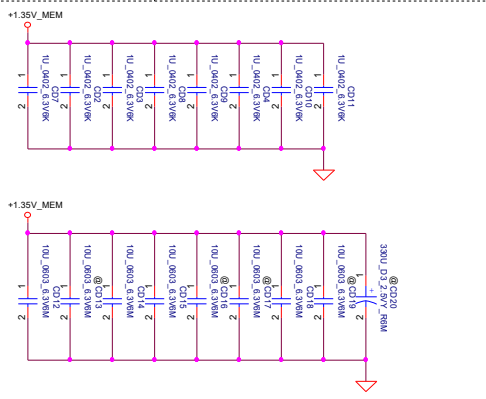


R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424

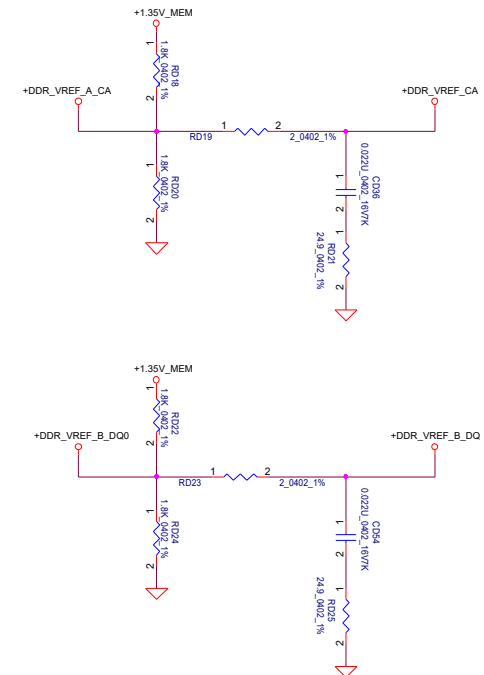
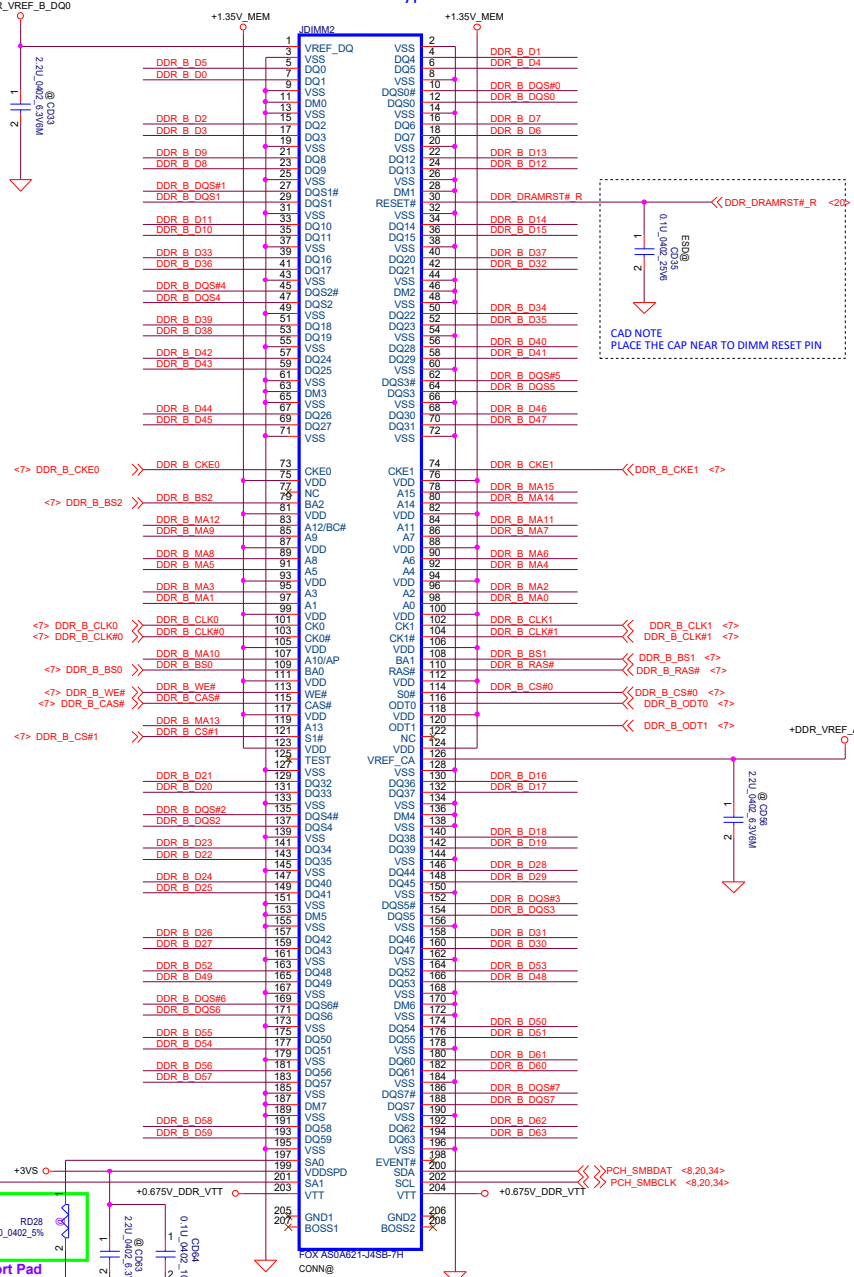


	Compal Electronics, Inc.		
	Title		
	CPU (14/14)		
	Size	Document Number	Rev
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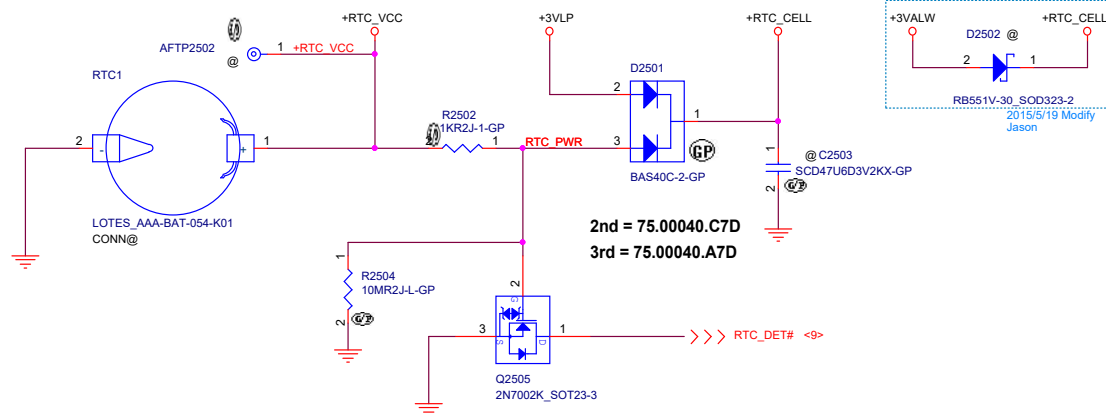
9/17 delete ODT Genertation, connect directly to CPU
refer 546765 2014WW37 SkylakeU Y_MOW Rev 1.0

[illegible]

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Main Func = RTC

Mind the voltage rating of the caps.



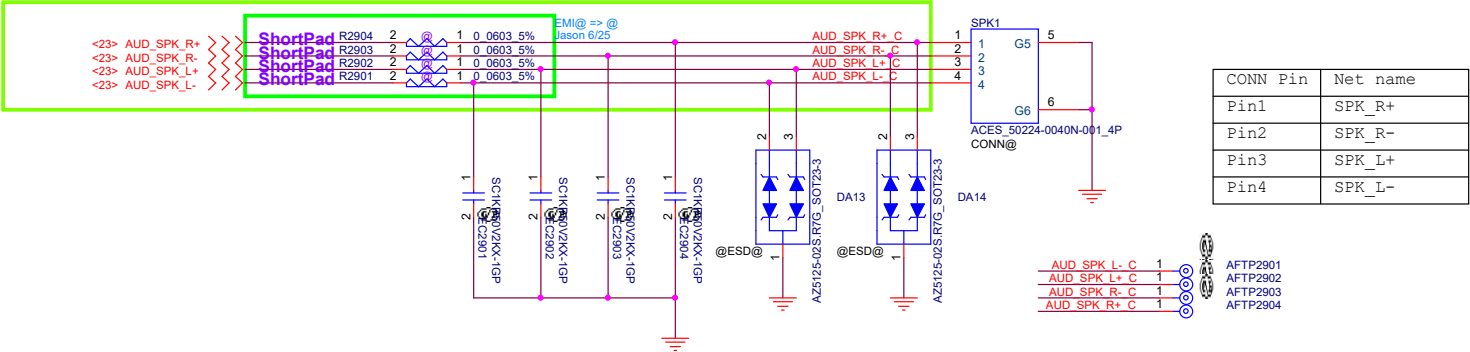
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2015/07/09	Deciphered Date	2016/07/31	Title		
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				Size	Document Number	Rev
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Main Func = Audio

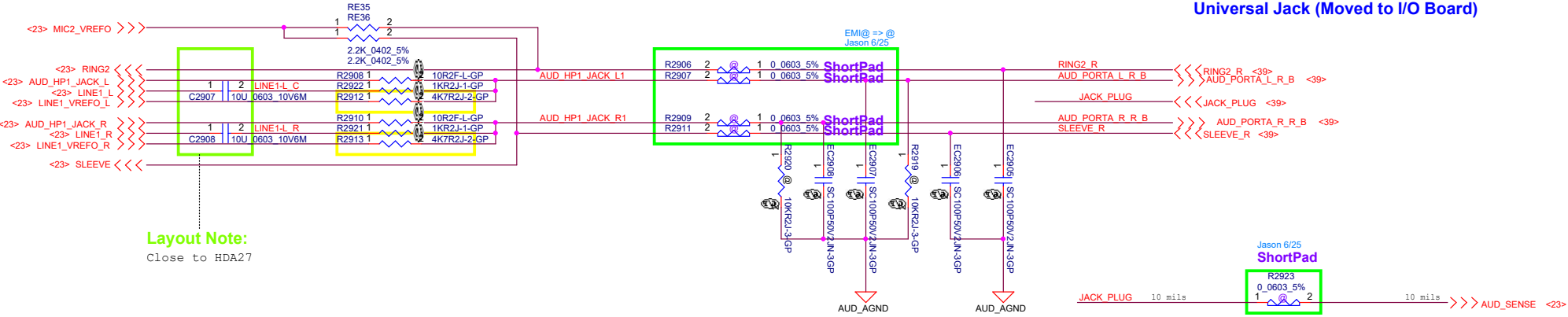
Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

Speaker



Universal Jack (Moved to I/O Board)

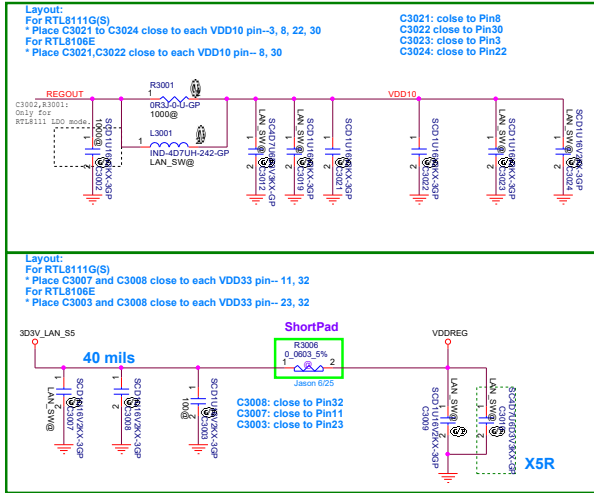


Layout Note:

Close to HDA27

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					LA-D071P
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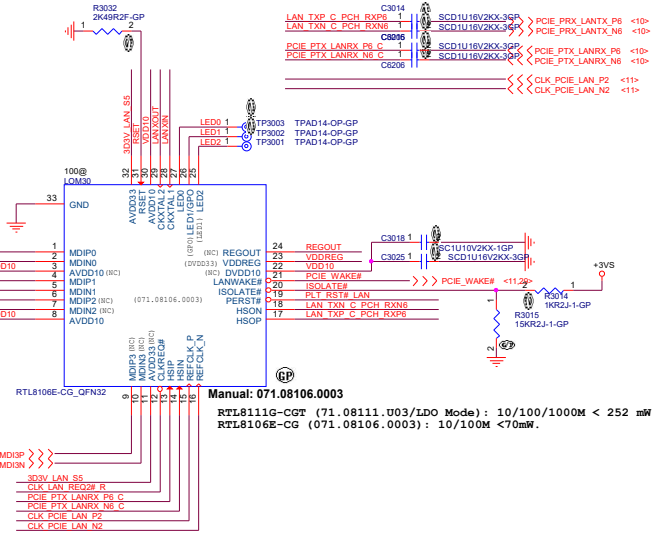
LAN CHIP (10/100/1000M & 10/100M co-lay)



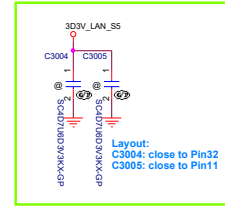
RTL811100B-CG	RTL8111G-CGT	RTL810600B-CG	RTL8106E-CGT
71.08111.W03	71.08111.U03	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M

LOM30 1000@
RTL8111G-CG QFN 32P E-LAN CTRL
SA00005V700

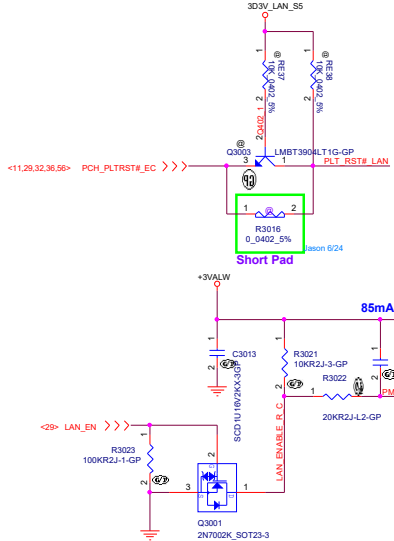
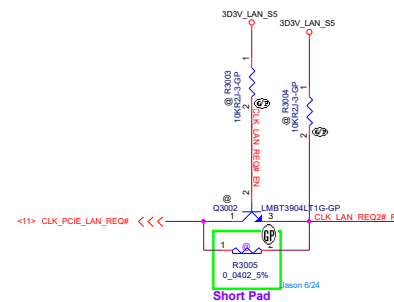
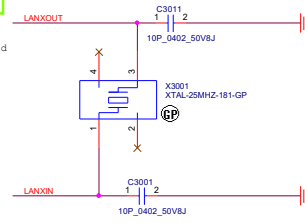
<26> LAN_MDIP
<26> LAN_MDIN
<26> LAN_MDIP
<26> LAN_MDIP
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<26> LAN_MDIN
<26> LAN_MDIN



Manual: 071.08106.0003
RTL8111G-CGT (71.08111.U03/LDO Mode): 10/100/1000M < 252 mW.
RTL8106E-CG (071.08106.0003): 10/100M < 70mW.

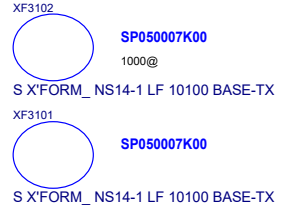
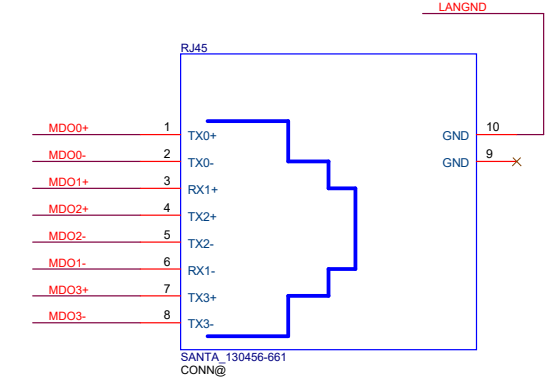
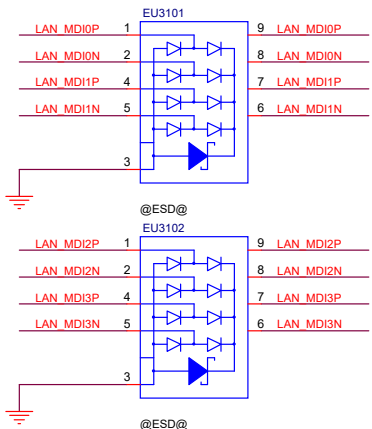
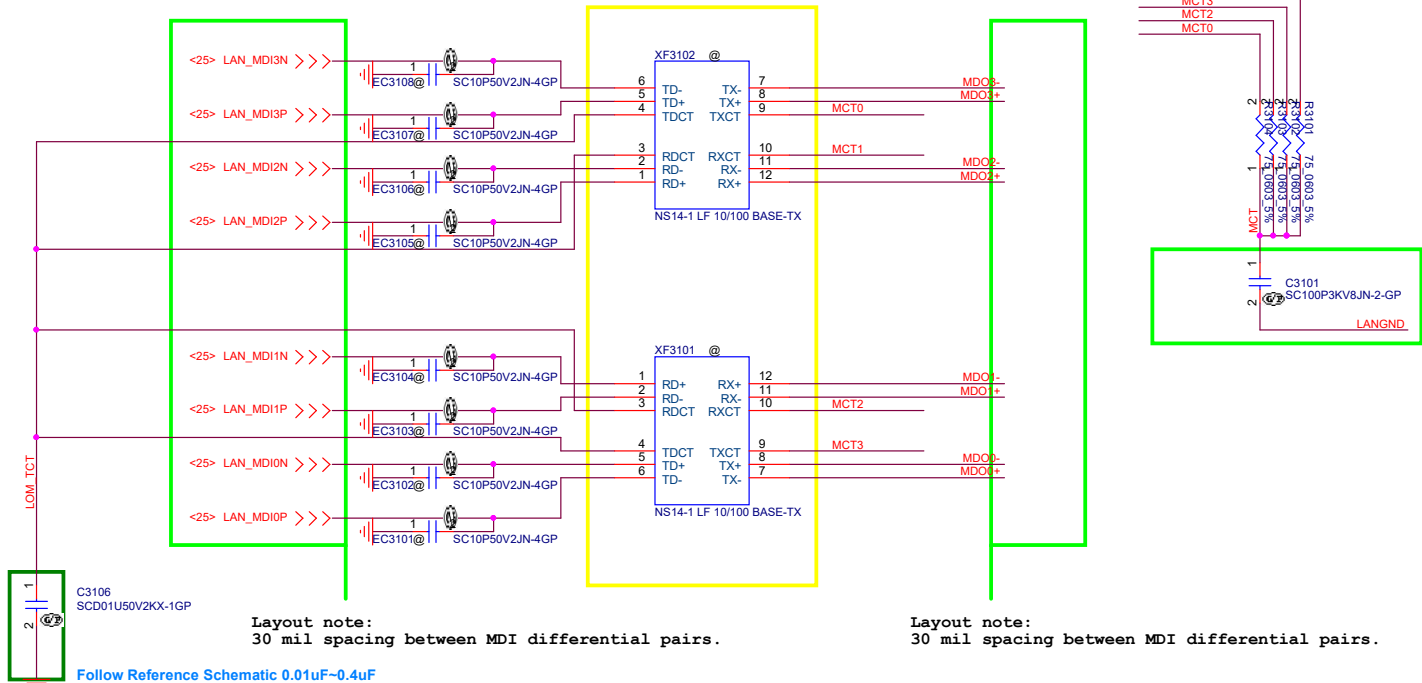


3D3V_LAN_S5 rise time must be controlled between 0.5 ms and 100 ms.



	1.0V Source	R3001	C3002	C3023	C3024	C3007	L3001	C3012	C3019	C3009	C3010	C3003
RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X	X	X	X	X	X
RTL8111GUS-CG (71.08111.W03) / RTL8106EUS-CG (71.08106.003)	SWR	X	X	O	O	O	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	X	X	X	X	X	O

LAN Transformer (10/100/1000M & 10/100M co-lay)

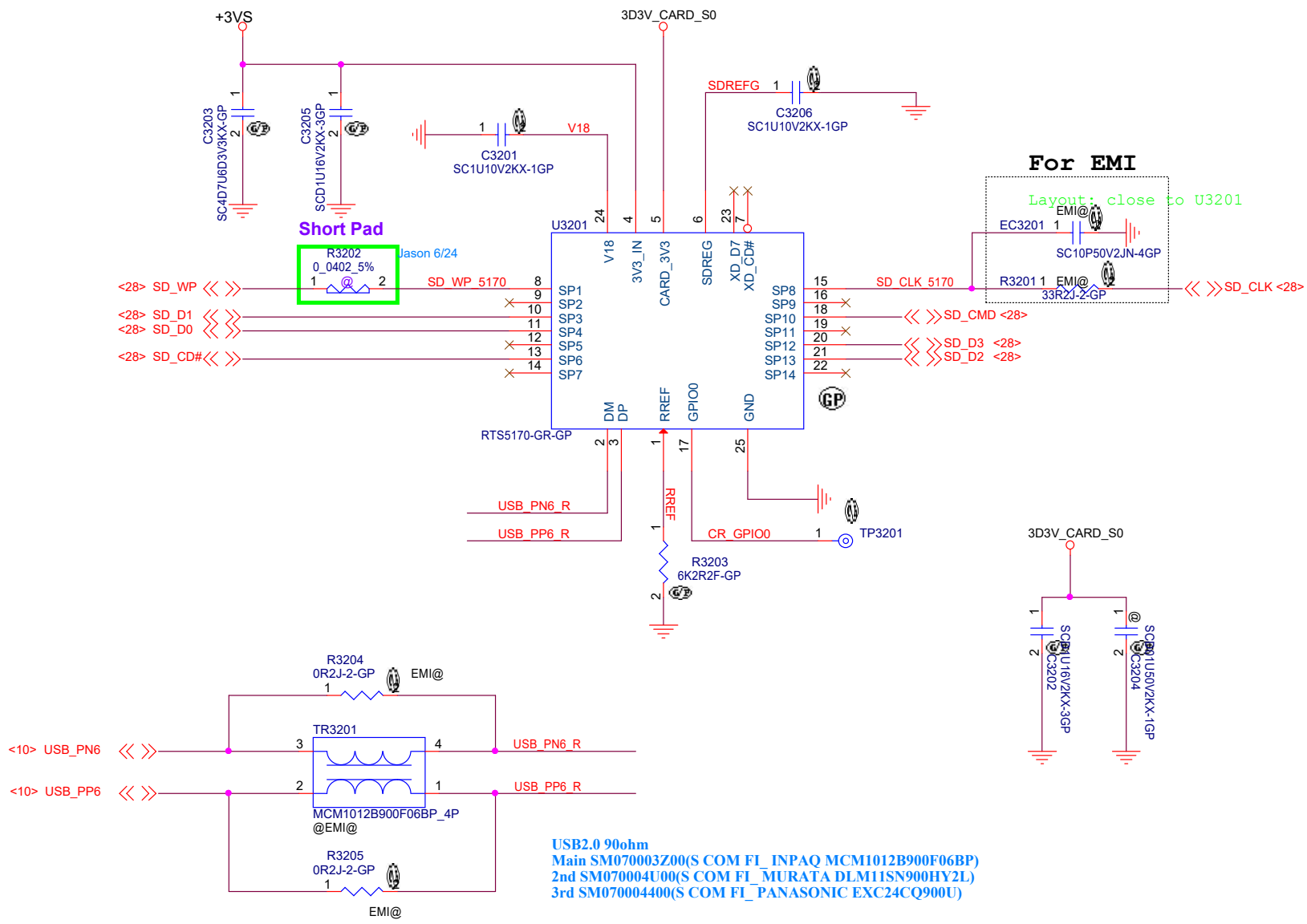


Main:
SP050007K00, S X'FORM_HD-081-A LAN
2nd:
SP050008L00, S X'FORM_NS681677 LAN
Jason 2015/04/27

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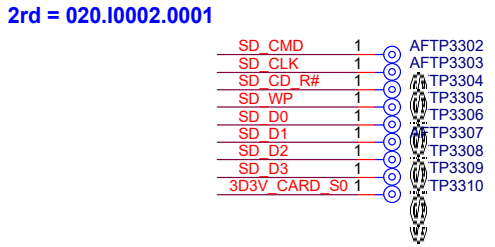
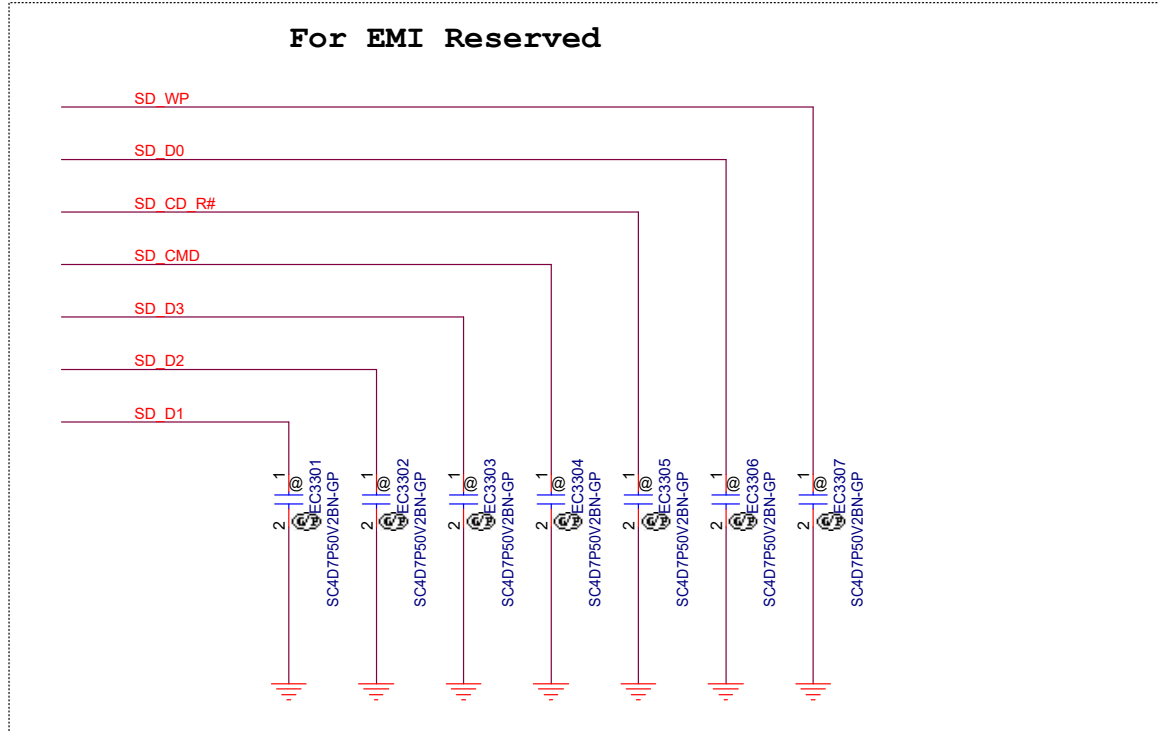
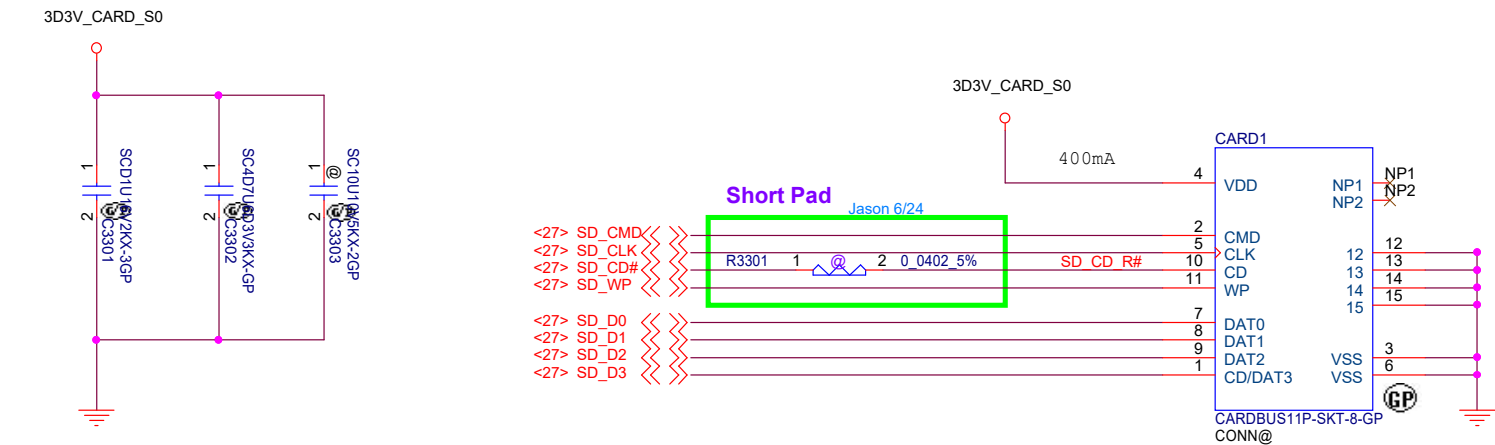
Main Func = Card Reader

The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA

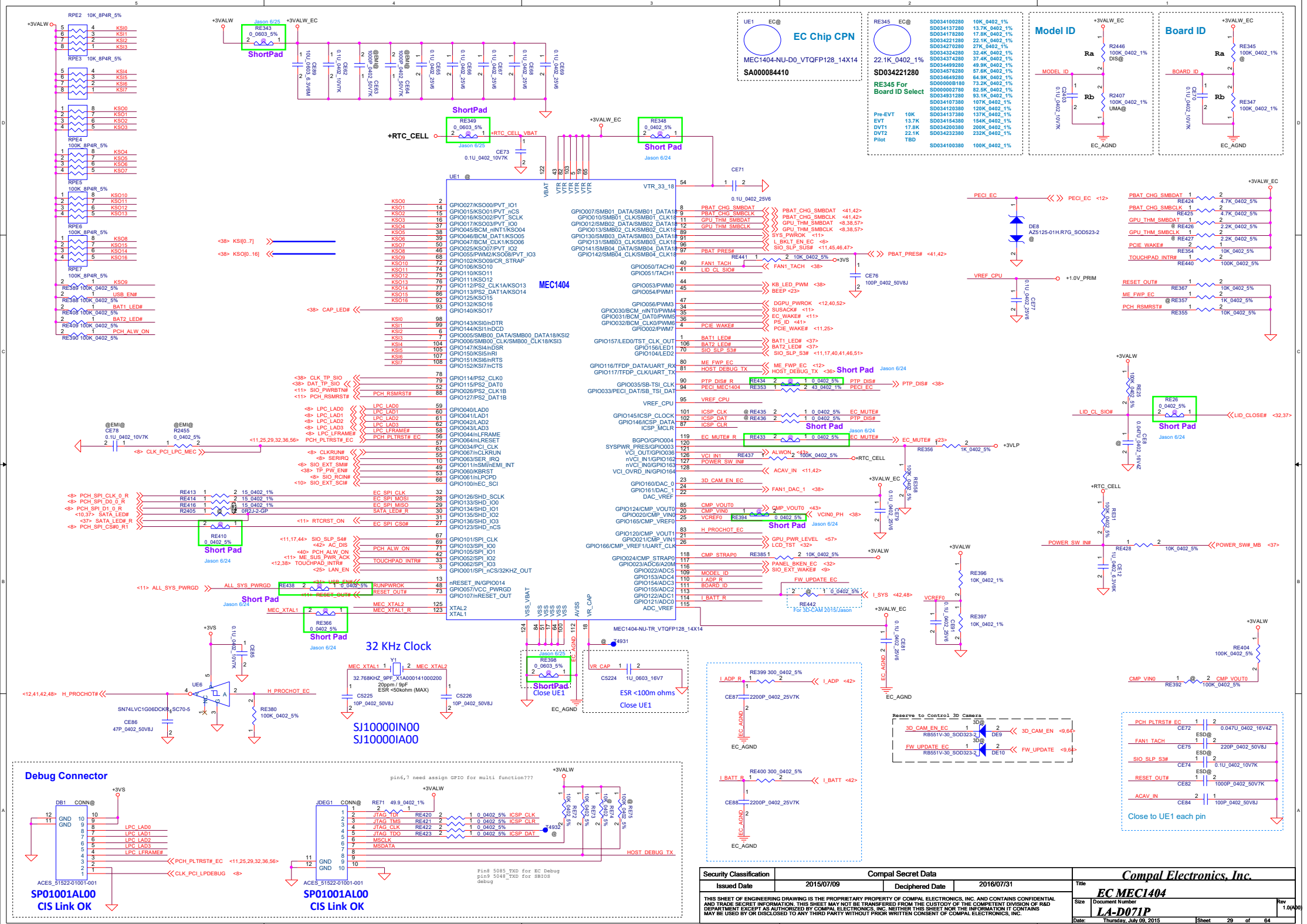


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				Size	Document Number
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Date: Thursday, July 09, 2015		Sheet 27 of 64		Rev 1.0(A00)	

Main Func = Card Reader

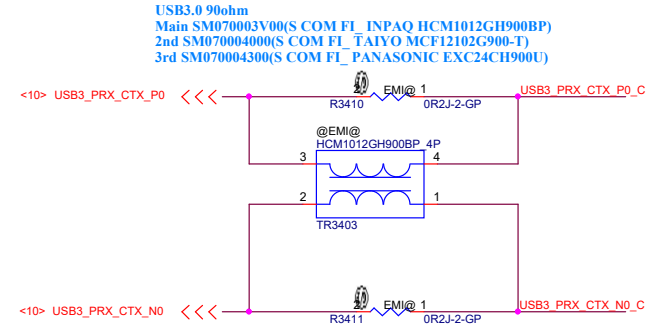
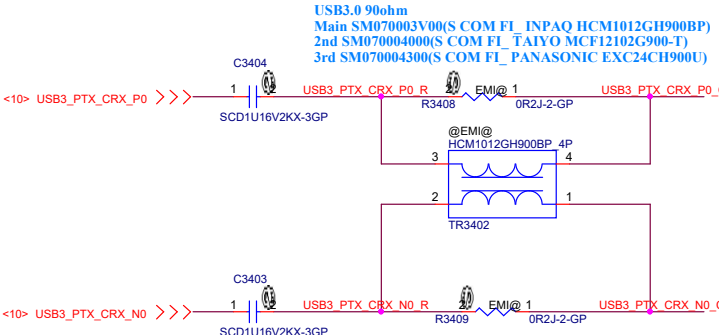
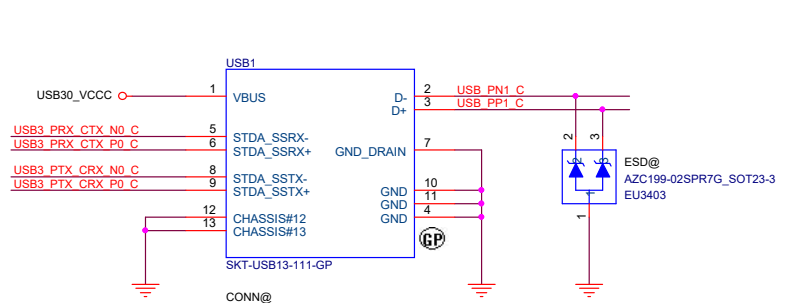
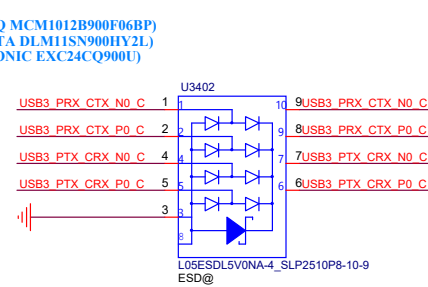
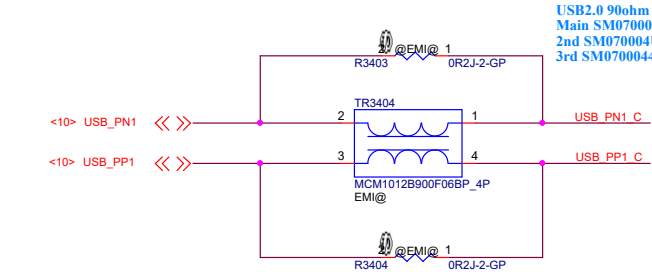


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				Size	Document Number
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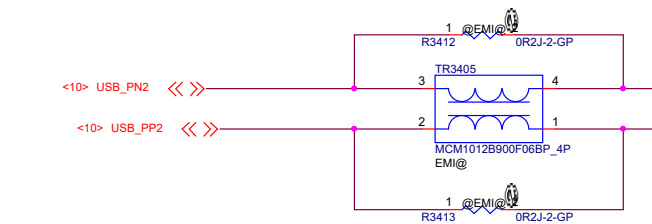


Main Func = USB3.0 Port1

USB2.0 Port2 and USB2.0 Port3 are on IOBD

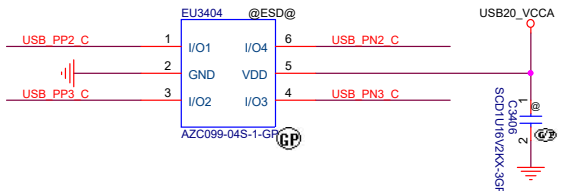


USB2 (USB2.0) CMC

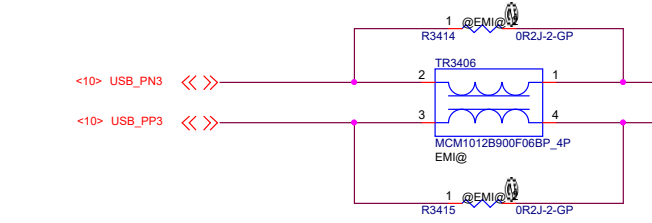


USB2.0 90ohm
Main SM070003Z00(S COM FL_INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FL_MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FL_PANASONIC EXC24CQ900U)

USB ESD Diode



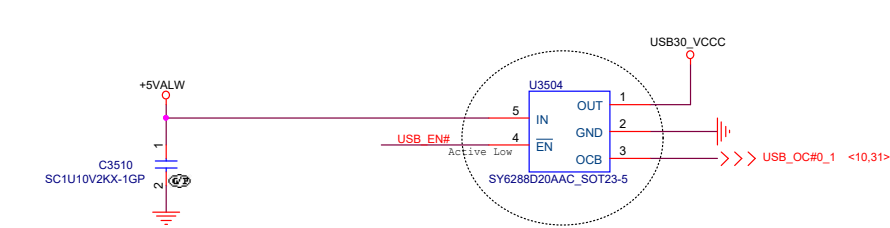
USB3 (USB2.0) CMC



USB2.0 90ohm
Main SM070003Z00(S COM FL_INPAQ MCM1012B900F06BP)
2nd SM070004U00(S COM FL_MURATA DLM11SN900HY2L)
3rd SM070004400(S COM FL_PANASONIC EXC24CQ900U)

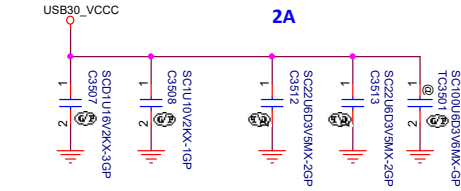
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Size		Document Number		Rev	
		LA-D071P		1.0(A00)	
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Main Func = USB3.0 Port1

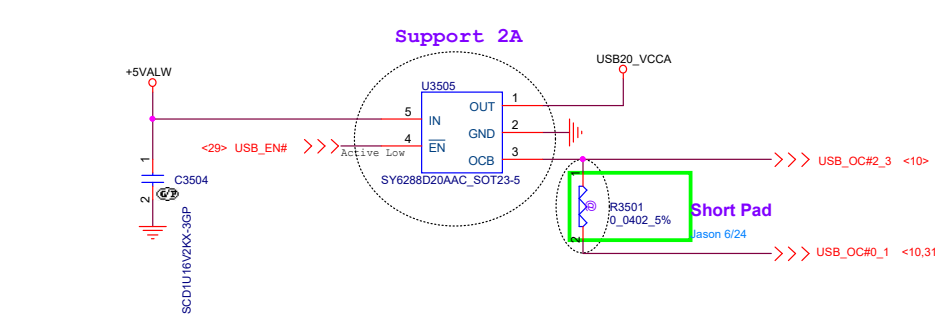


USB3.0 Port1

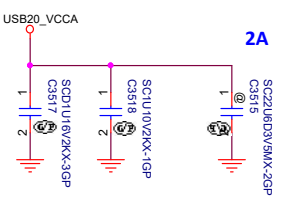
Layout Note: Close USB1



Main Func = USB2.0 Port3



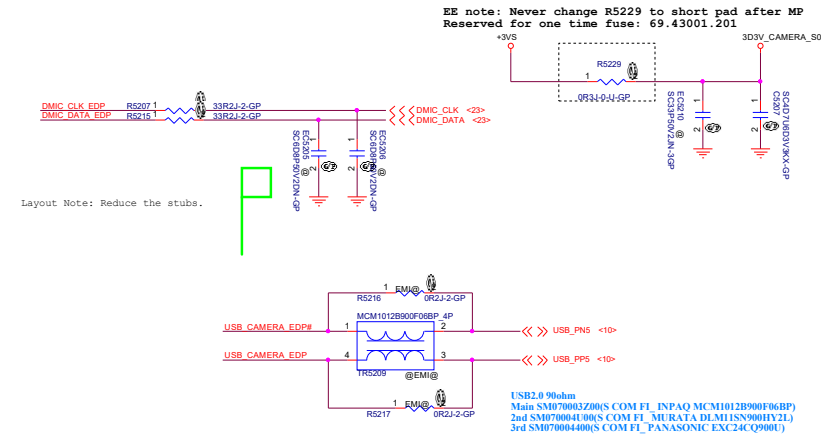
USB2.0 Port3 (IO Board)



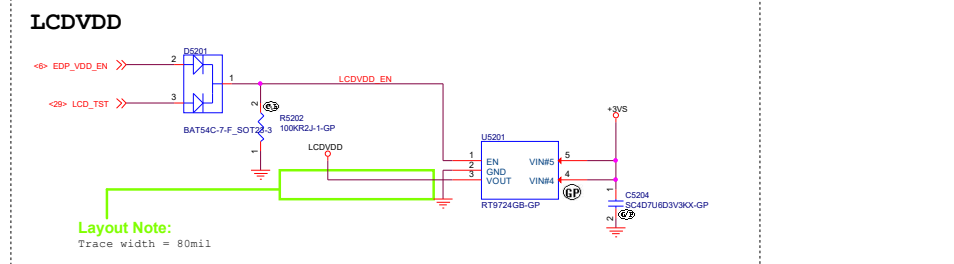
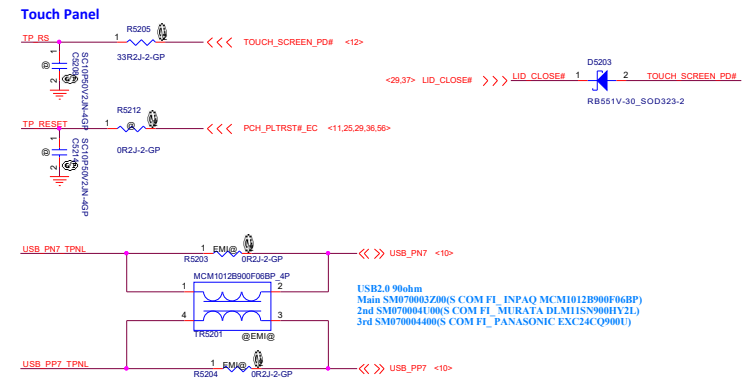
Main Func =

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/07/09	Deciphered Date	2016/07/31	Title	USB Power SW
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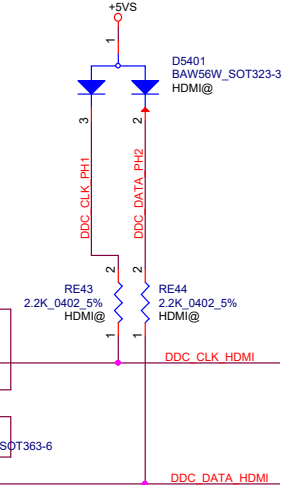
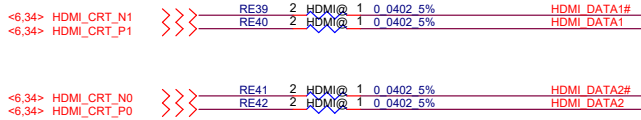
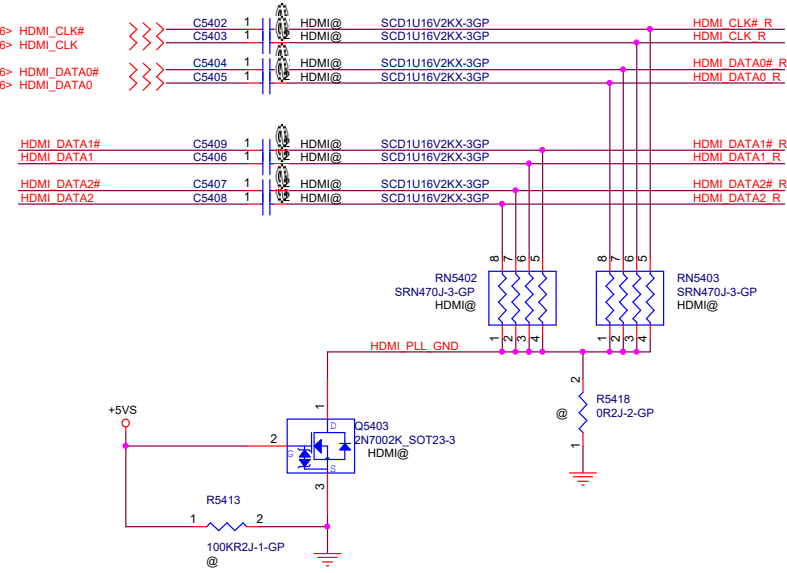
Main Func = CAM



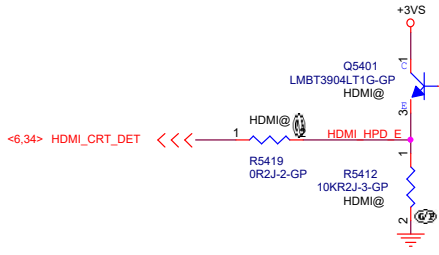
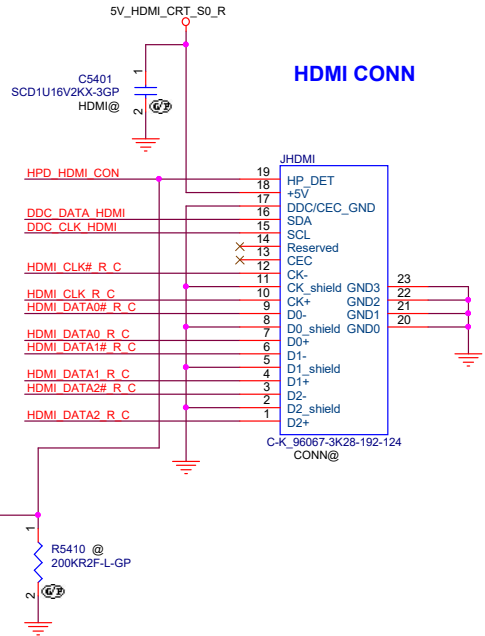
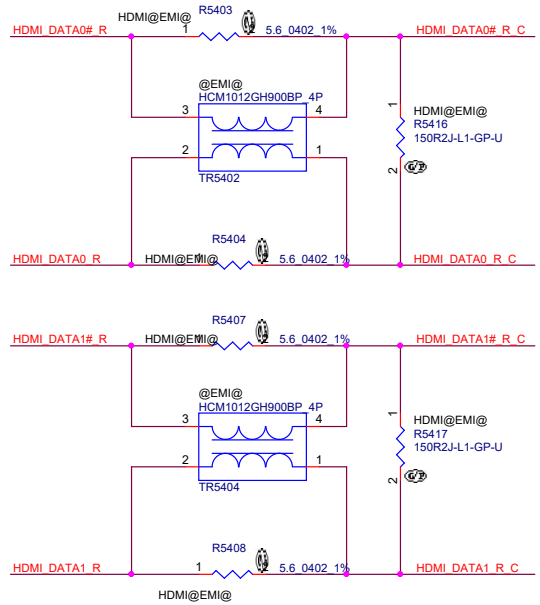
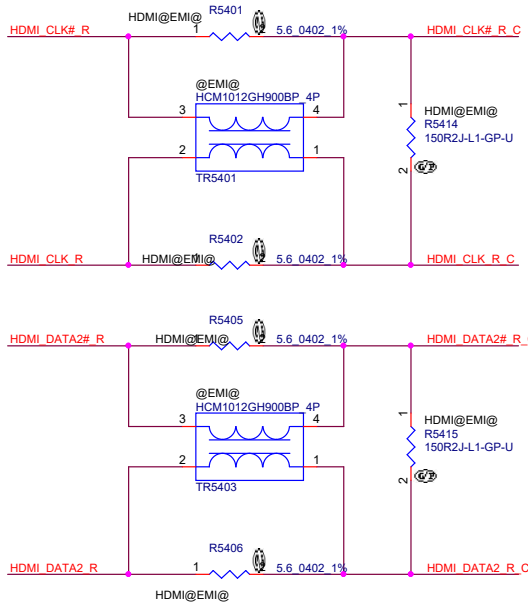
Touch Panel



Main Func = HDMI

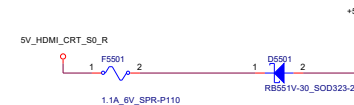
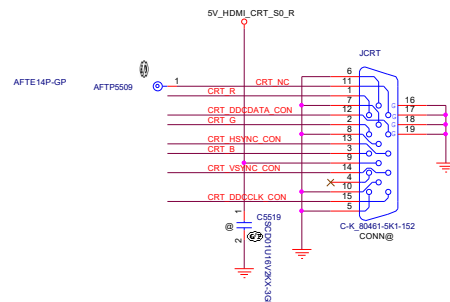
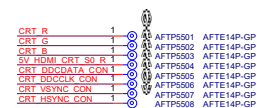


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3rd = 75.00601.07C
4th = 84.DMN66.03F

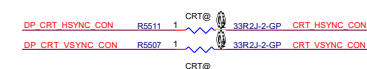
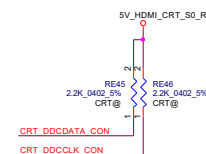
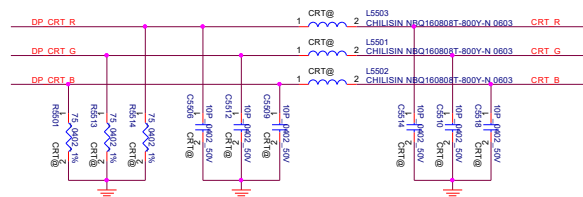
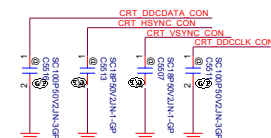


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LA-D071P		Date:		Thursday, July 09, 2015	Sheet 33 of 64

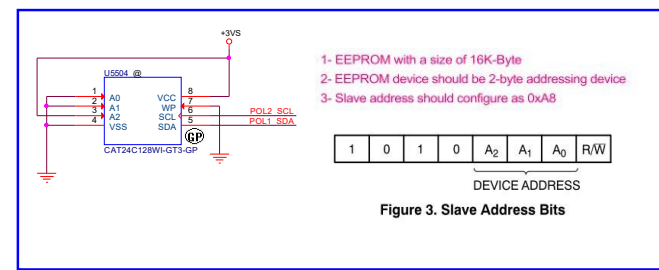
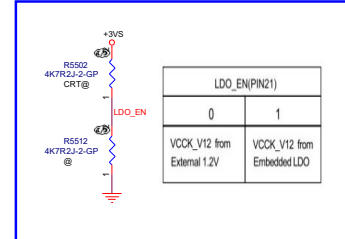
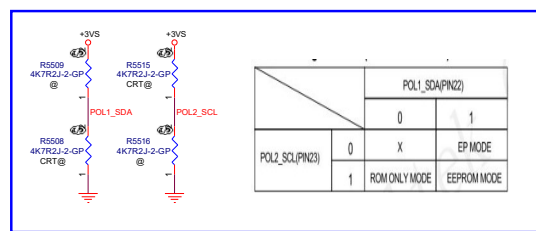
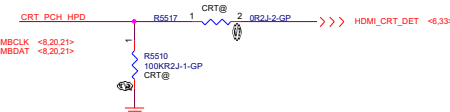
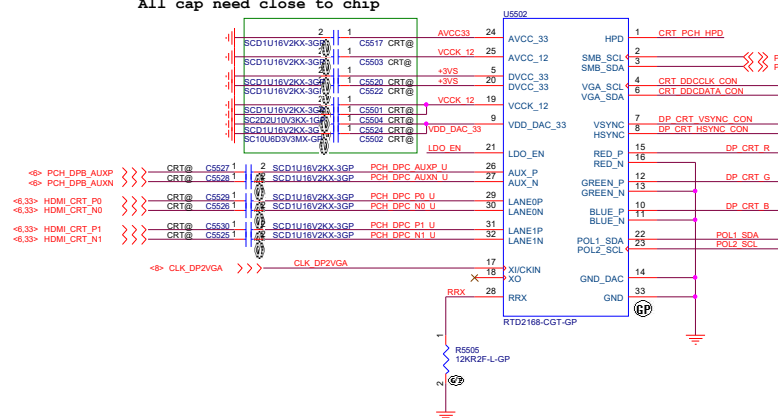
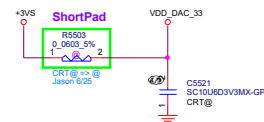
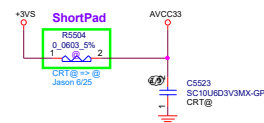
- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8



CRT RGB
CRT HVSYN
CRT SMBUS



Layout note:
All cap need close to chip

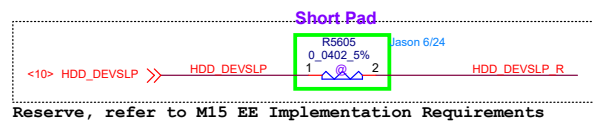
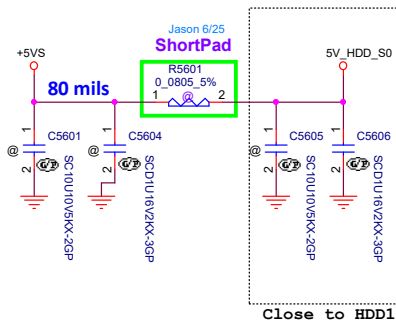


- 1- EEPROM with a size of 16K-Byte
- 2- EEPROM device should be 2-byte addressing device
- 3- Slave address should configure as 0xA8

1	0	1	0	A ₂	A ₁	A ₀	R/W
---	---	---	---	----------------	----------------	----------------	-----

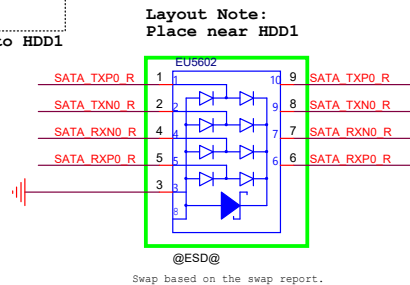
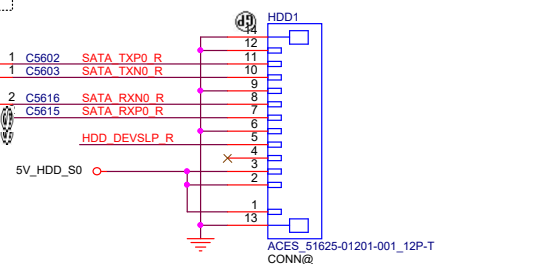
Figure 3. Slave Address Bits

SATA HDD Connector



```
<10> SATA3_PTX_HDDR_X_P0
<10> SATA3_PTX_HDDR_X_N0

<10> SATA3_PRX_HDDTX_N0
<10> SATA3_PRX_HDDTX_P0
```



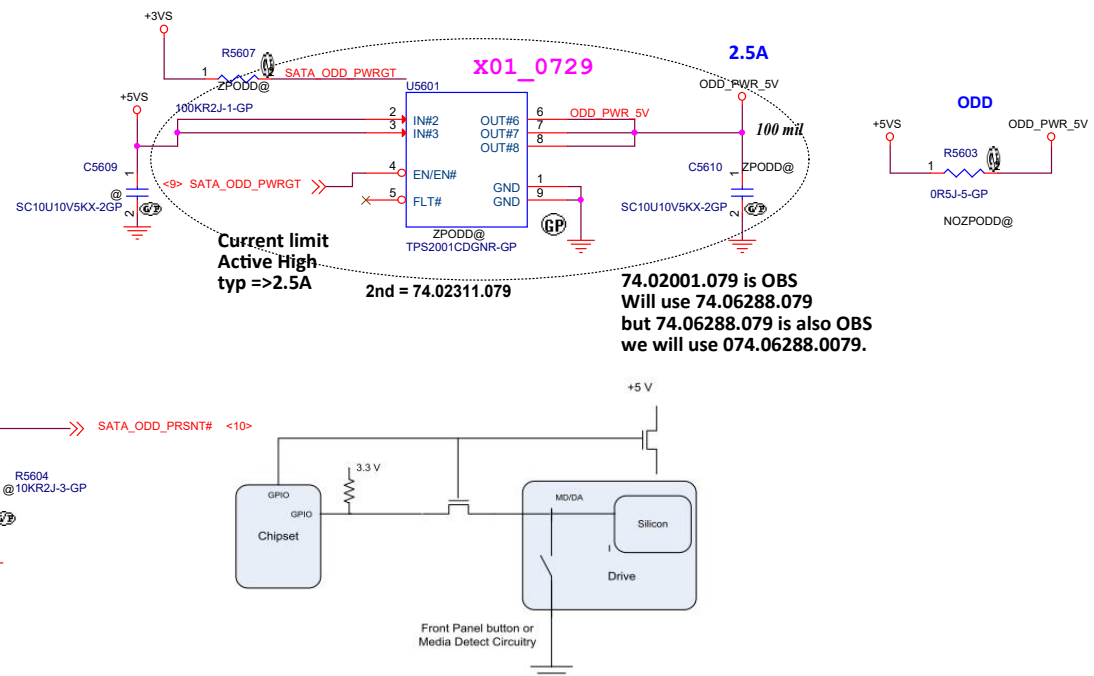
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

ODD Connector

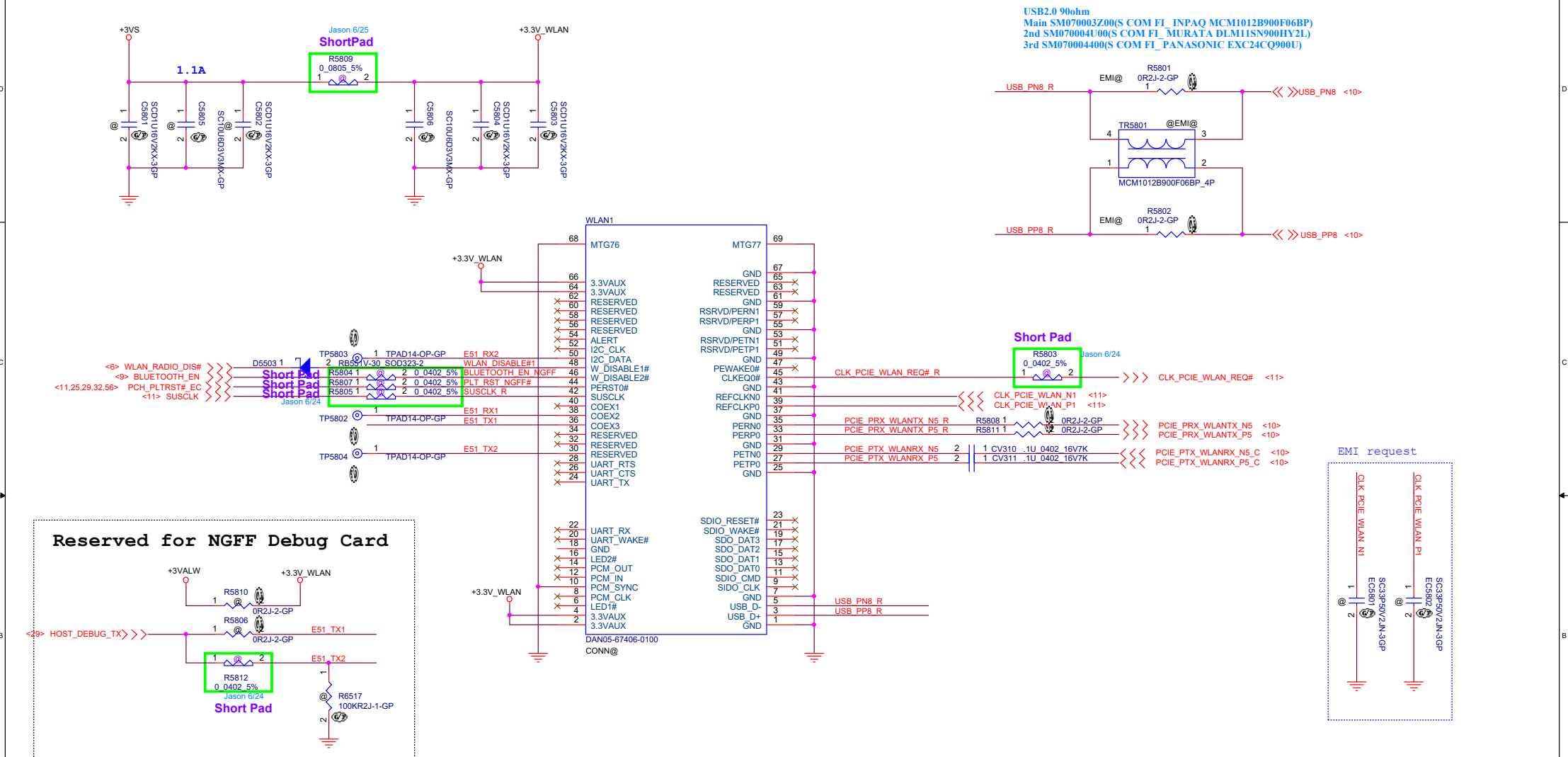


SATA Zero Power ODD



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				Size	Document Number
				LA-D071P	
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				Rev	1.0 (ADD)

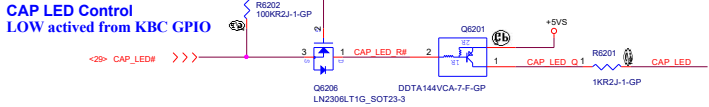
Main Func = WLAN



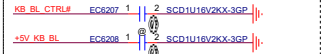
Support: Intel Dual Band Wireless-AC 3160

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				Size	Document Number	Rev
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Main Func = KB



Keyboard Backlight (Reserved)

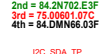


Main Func = Thermal

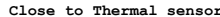


TEMPERATURE (°C)		T_CRIT#				
		2KQ	7.5KQ	10.5KQ	14KQ	18.7KQ
ALERT#	2KQ	77	87	97	107	117
	7.5KQ	79	89	99	109	119
	10.5KQ	81	91	101	111	121
	14KQ	83	93	103	113	123
	18.7KQ	85	95	105	115	125

Main Func = TPAI



Fan controller1



Close to KBC
VD IN1 for system thermal sensor

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<p>DATE: Thursday, July 9, 2015</p>			<p>Sheet 38 of 64</p>	

Main Func = IO Connector

I/O Board Connector

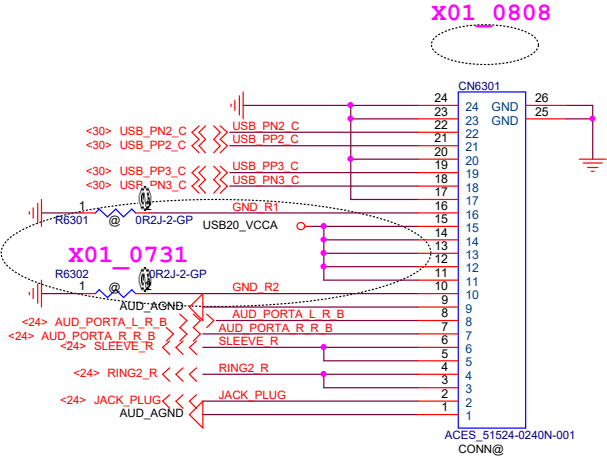
USB2 (USB2.0)

USB3 (USB2.0)

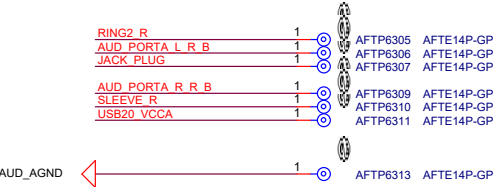
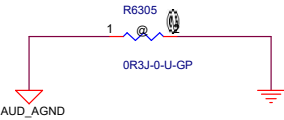
USB2 (USB2.0)

USB3 (USB2.0)

Universal Jack

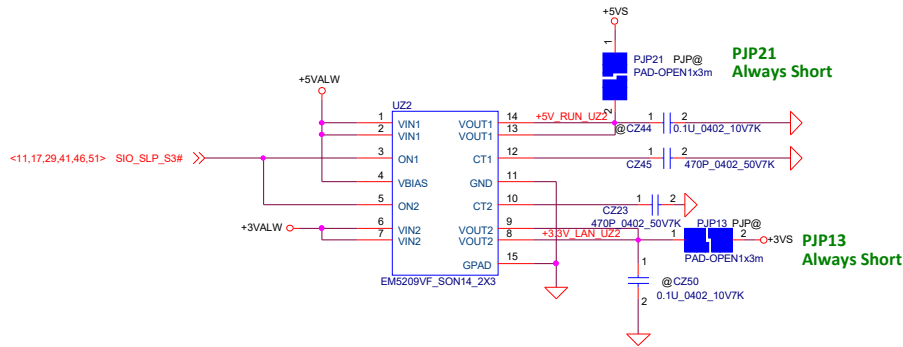


Pitch: 1mm
Power: 5 pins
GND: 4 pins
AGND: 2 Pins

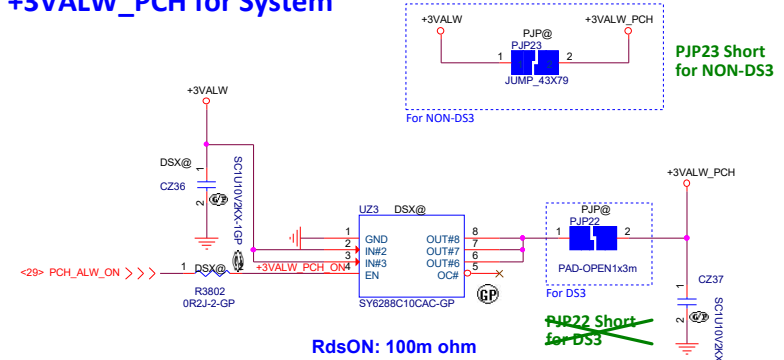


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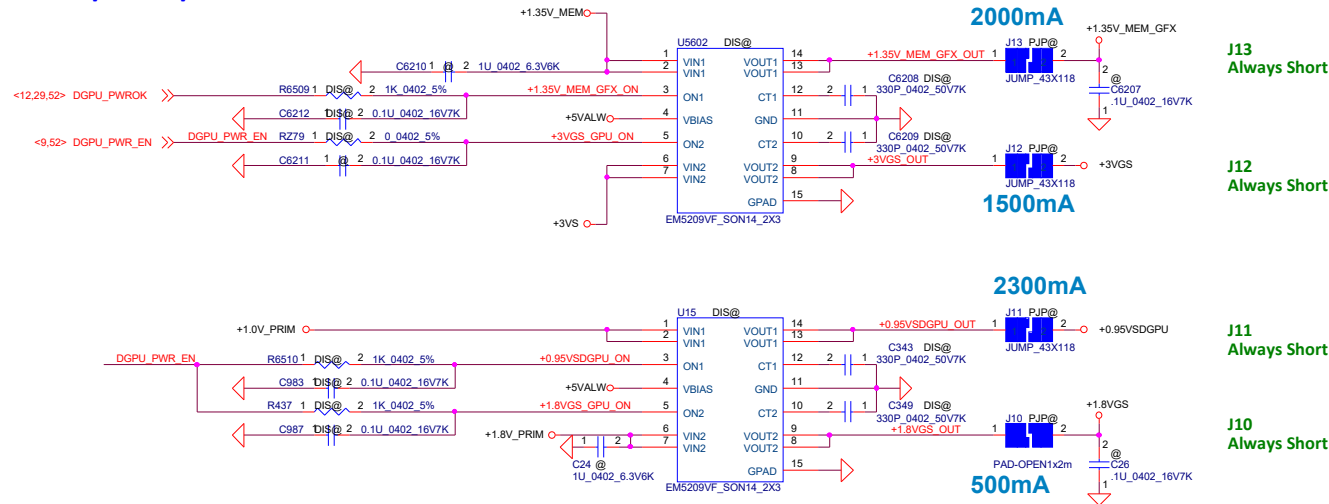
+5V_RUN/+3.3V_RUN for System



+3VALW_PCH for System



+3V/+0.95V/+1.8V/+1.35V for GPU



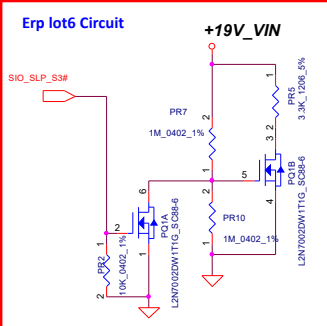
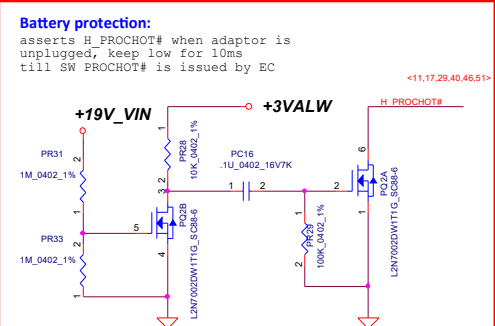
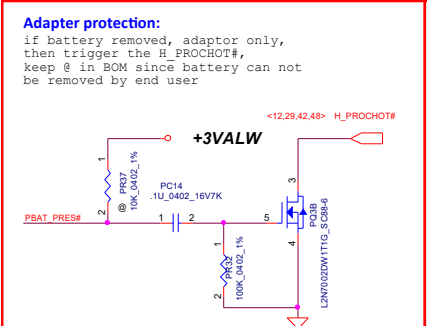
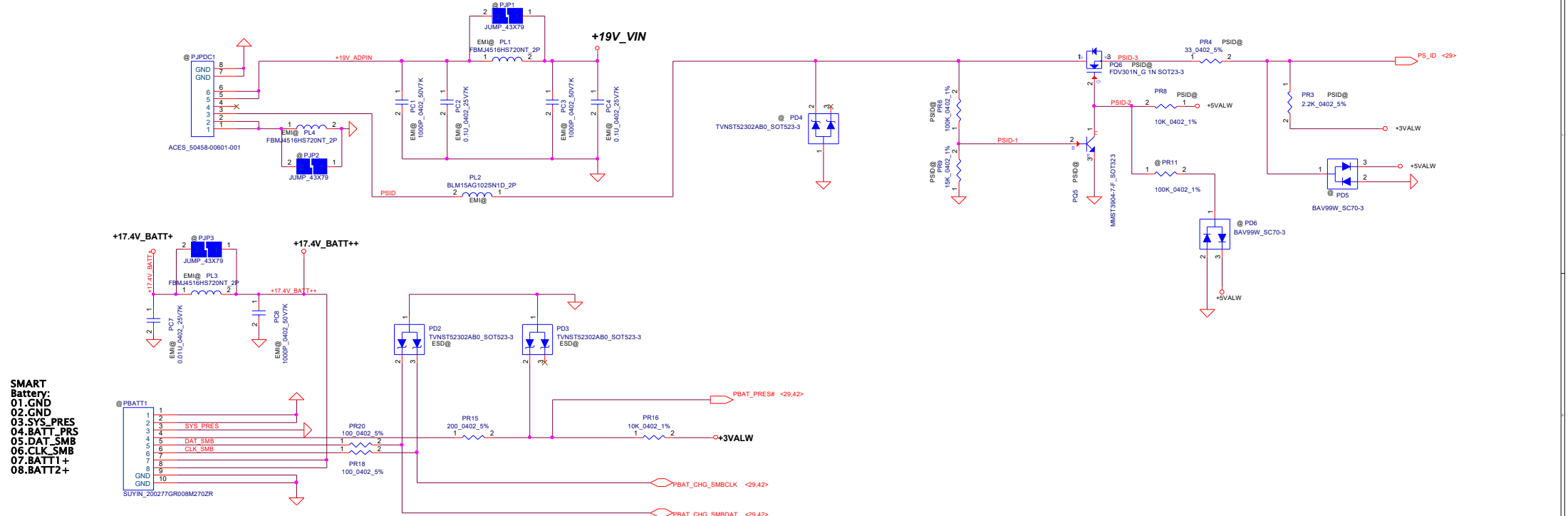
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Power control			
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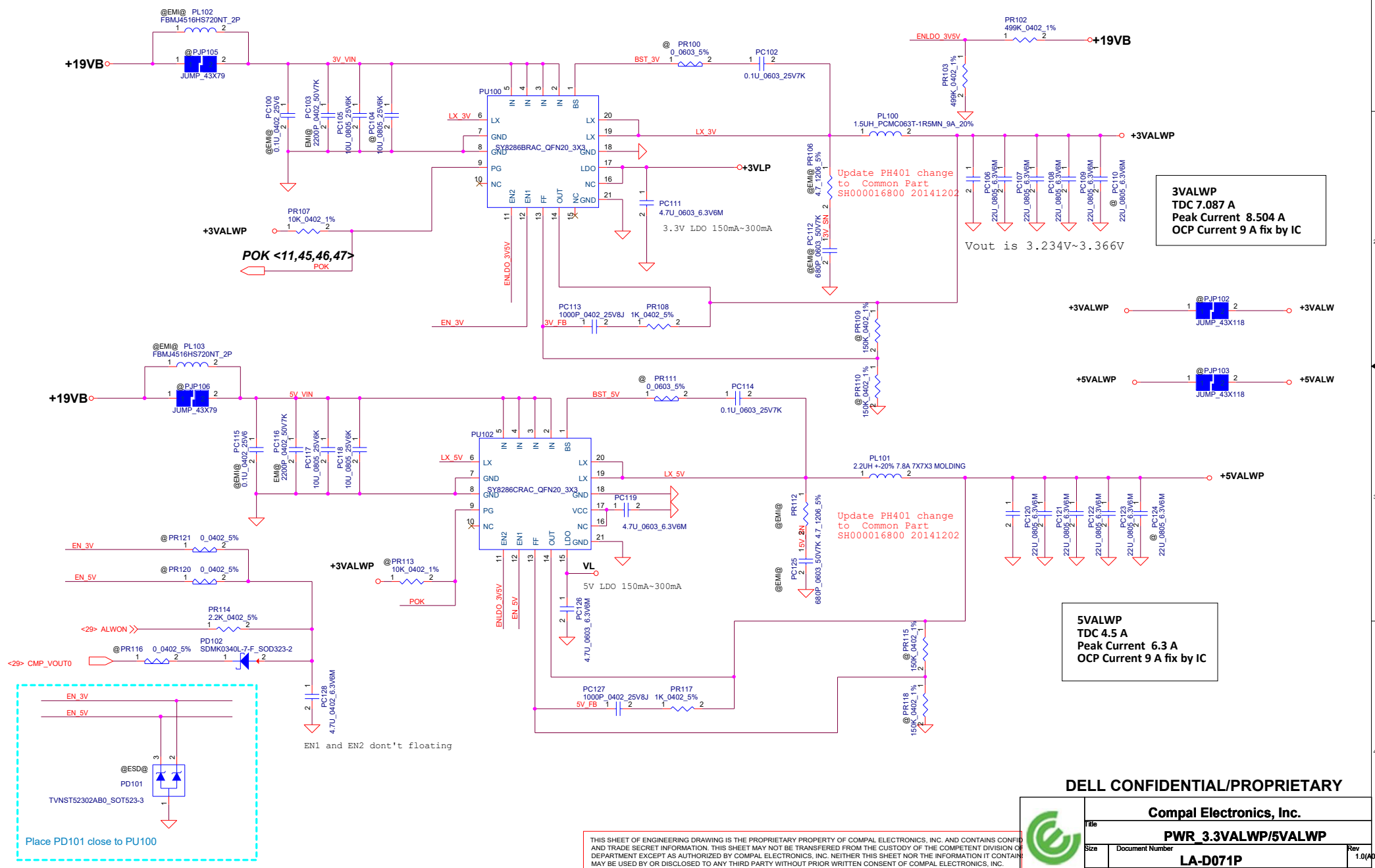
I_{ada}=0~2.30A(45W)

$$ADP_I = 32 * I_{\text{adapter}} * R_{\text{sense}}$$

4S1P: CV = 17.7V CC: 1.6A

4S1P: CV = 17.7V CC: 1.6A

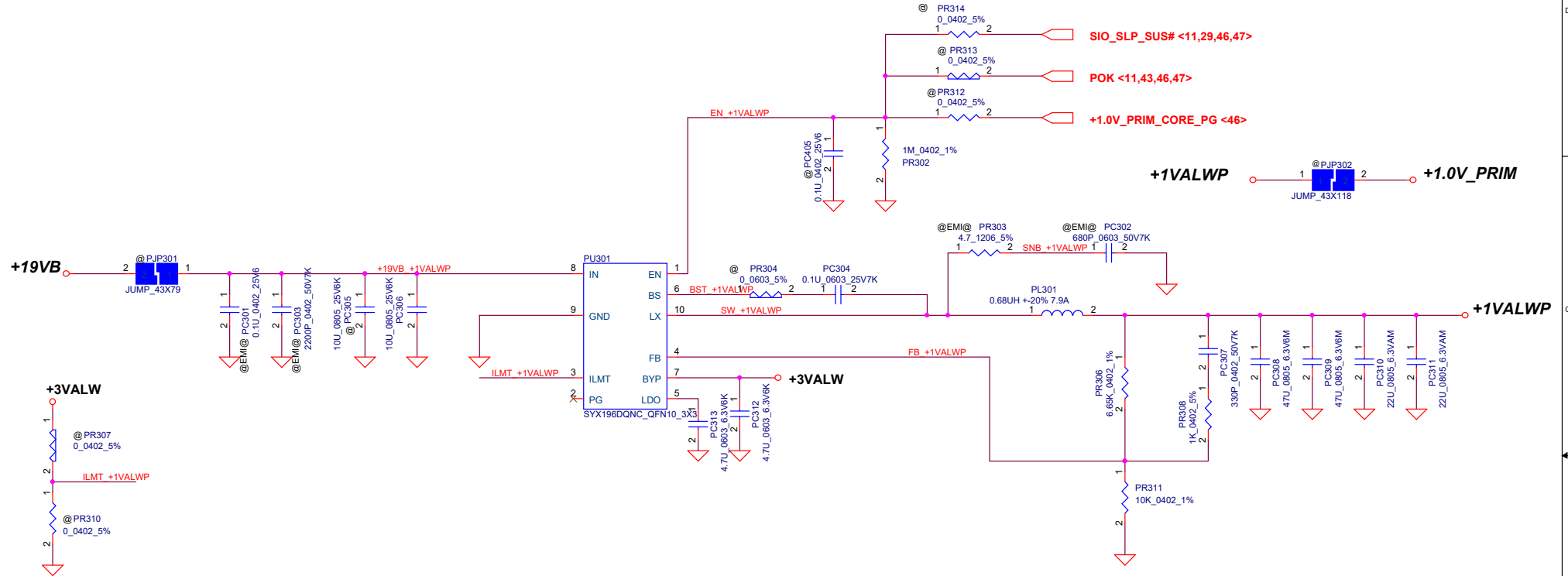
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PWR_3.3VALWP/5VALWP			
Size	Document Number	Rev	
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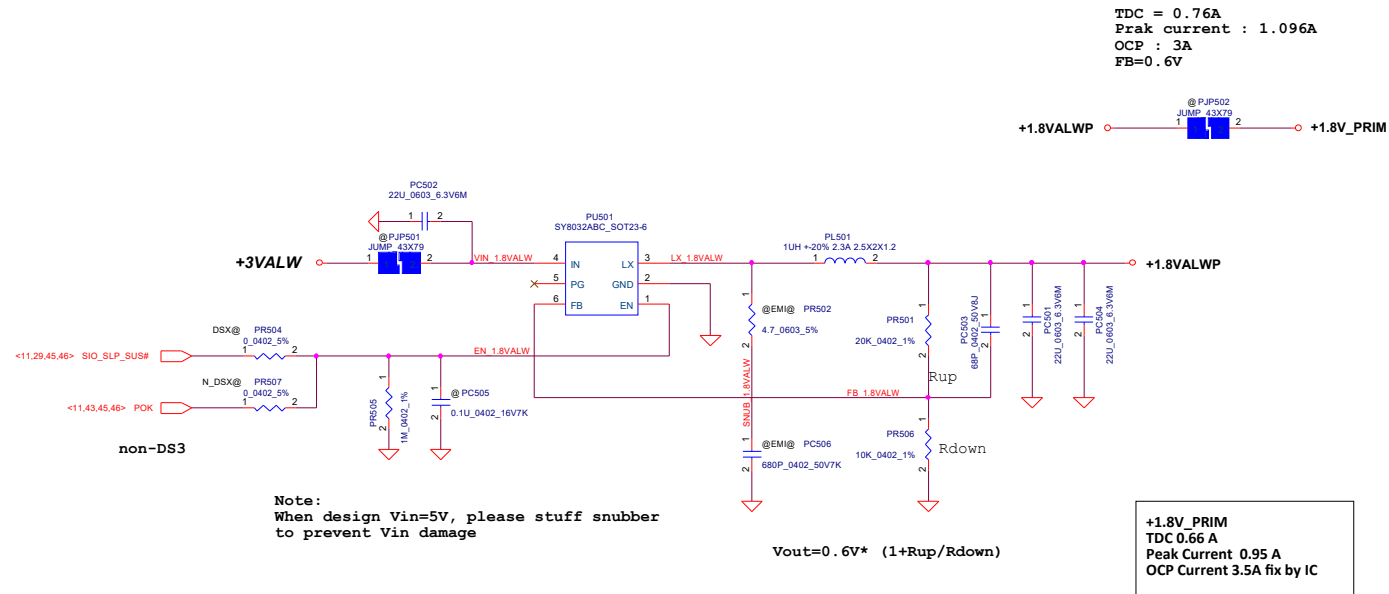
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+1.0V_PRIM
TDC 2.63 A
Peak Current 3.748 A
OCP Current 6.0 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm

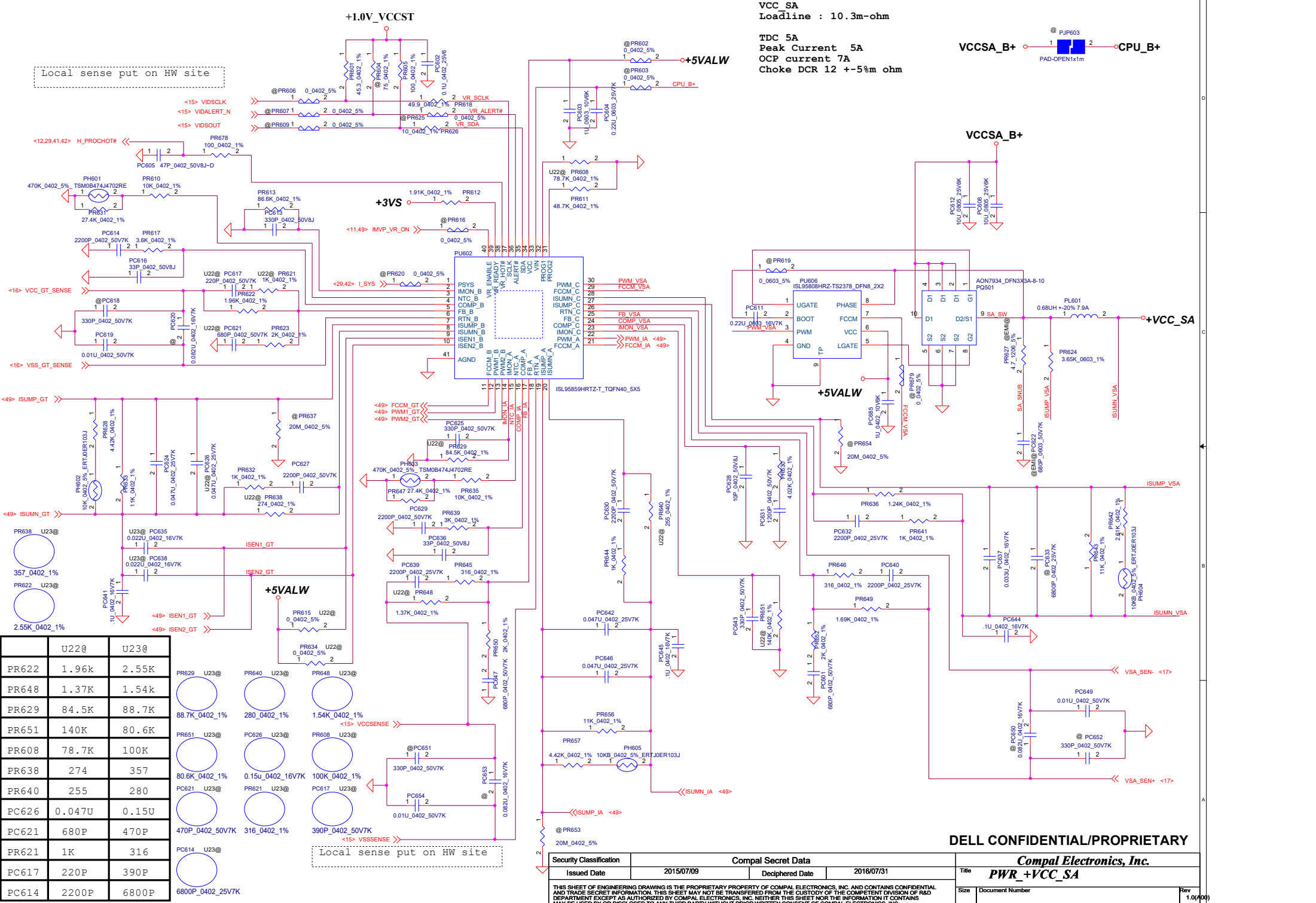
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Document Number				Rev
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	U22@	U23@
PR622	1.96k	2.55K
PR648	1.37K	1.54k
PR629	84.5K	88.7K
PR651	140K	80.6K
PR608	78.7K	100K
PR638	274	357
PR640	255	280
PC626	0.047U	0.15U
PC621	680P	470P
PR621	1K	316
PC617	220P	390P
PC614	2200P	6800P

PR629	U23@	PR640	U23@	PR648	U23@
					
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PR651	U23@	PC626	U23@	PR608	U23@
					
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PC614	U23@				
					
6800P_0402_25V7K					

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Size		Document Number			
		Rev 1.0(
Date:		Thursday, July 09, 2015		Sheet 48 of 64	

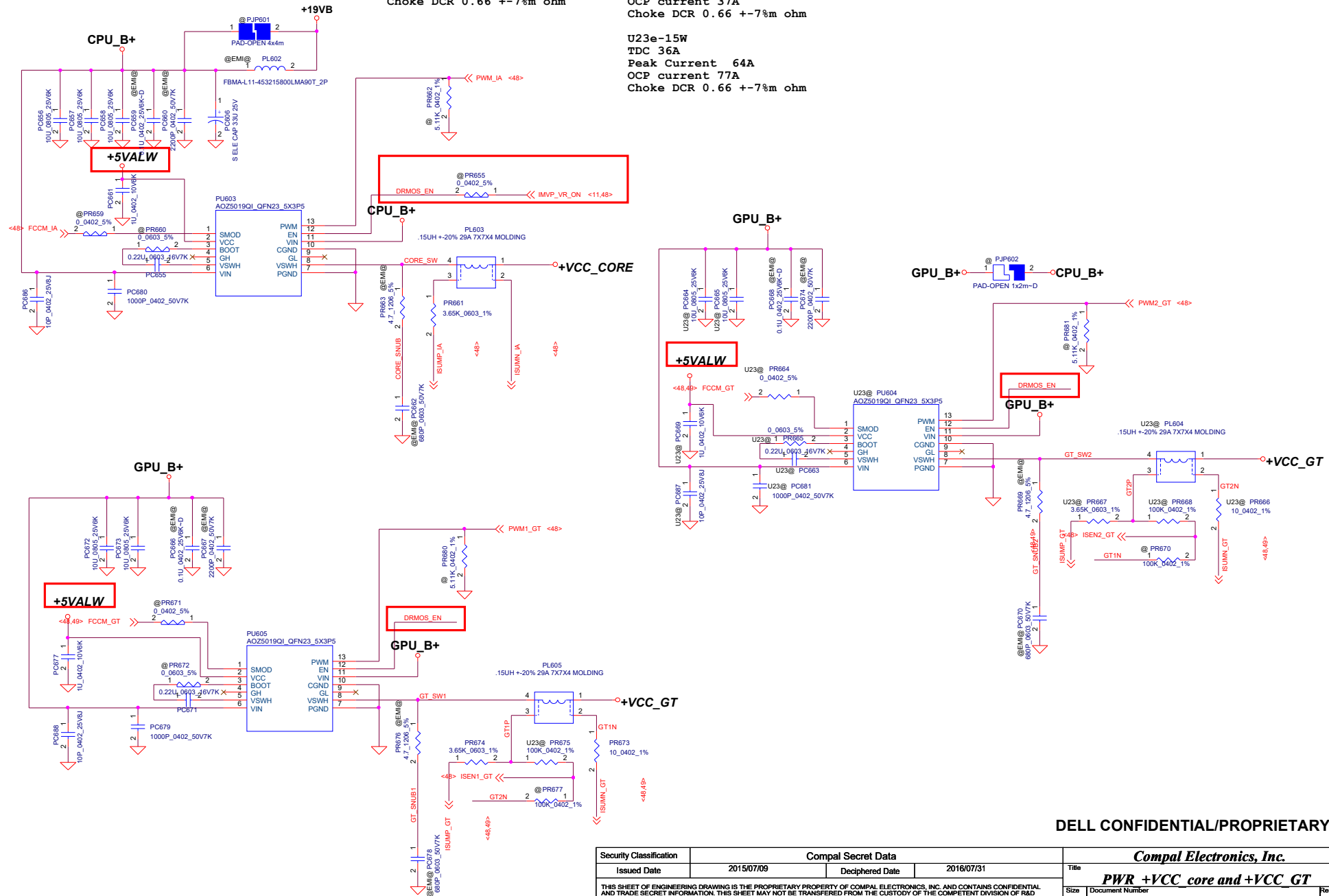
VCC_core
U22 - 15W
Loadline : 2.4m-ohm
U23e - 15W
Loadline : 2.4m-ohm

TDC 21A
Peak Current 29A
OCP current 34A
Choke DCR 0.66 +-7% ohm

VCC_GT
U22 - 15W
Loadline : 3.1m-ohm
U23e - 15W
Loadline : 2m-ohm

U22-15W
TDC 18A
Peak Current 31A
OCP current 37A
Choke DCR 0.66 +-7% ohm

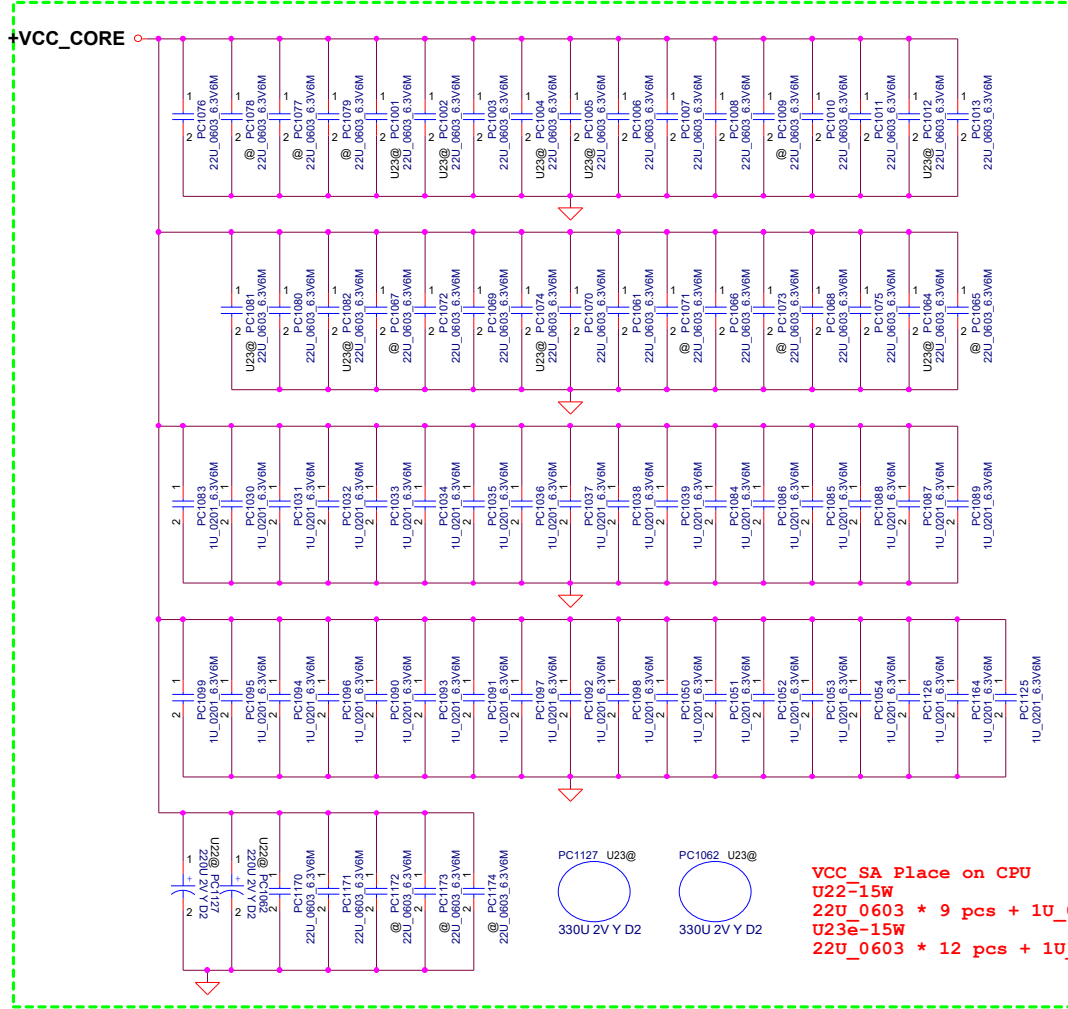
U23e-15W
TDC 36A
Peak Current 64A
OCP current 77A
Choke DCR 0.66 +-7% ohm



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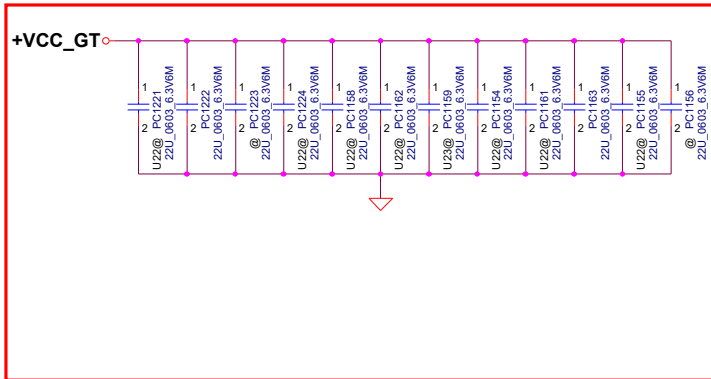
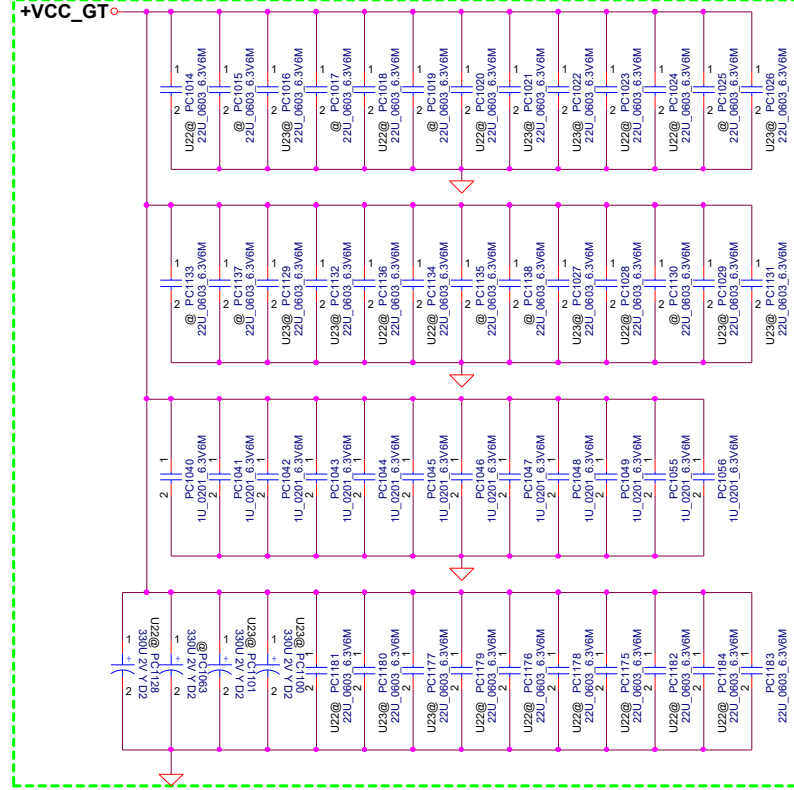
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Issued Date	2015/07/09	Deciphered Date	2016/07/31	Title	PWR +VCC_core and +VCC_GT
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VCC_CORE Place on CPU
 U22-15W
 22U_0603 * 18 pcs +1U_0201*35 pcs+220u_D2*2 pcs
 U23e-15W
 22U_0603 * 27 pcs +1U_0201*35 pcs+330u_D2*2 pcs

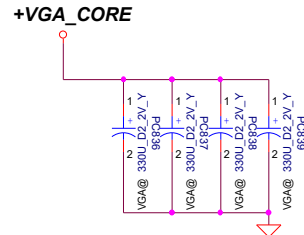


VCC_SA Place on CPU
 U22-15W
 22U_0603 * 9 pcs + 1U_0201*7 pcs
 U23e-15W
 22U_0603 * 12 pcs + 1U_0201*7 pcs

VCC_GT Place on CPU
 U22-15W
 22U_0603 * 25 pcs +1U_0201*12 pcs+330u_D2*1 pcs
 U23e-15W
 22U_0603 * 48 pcs +1U_0201*12 pcs+330u_D2*4 pcs



For GTX

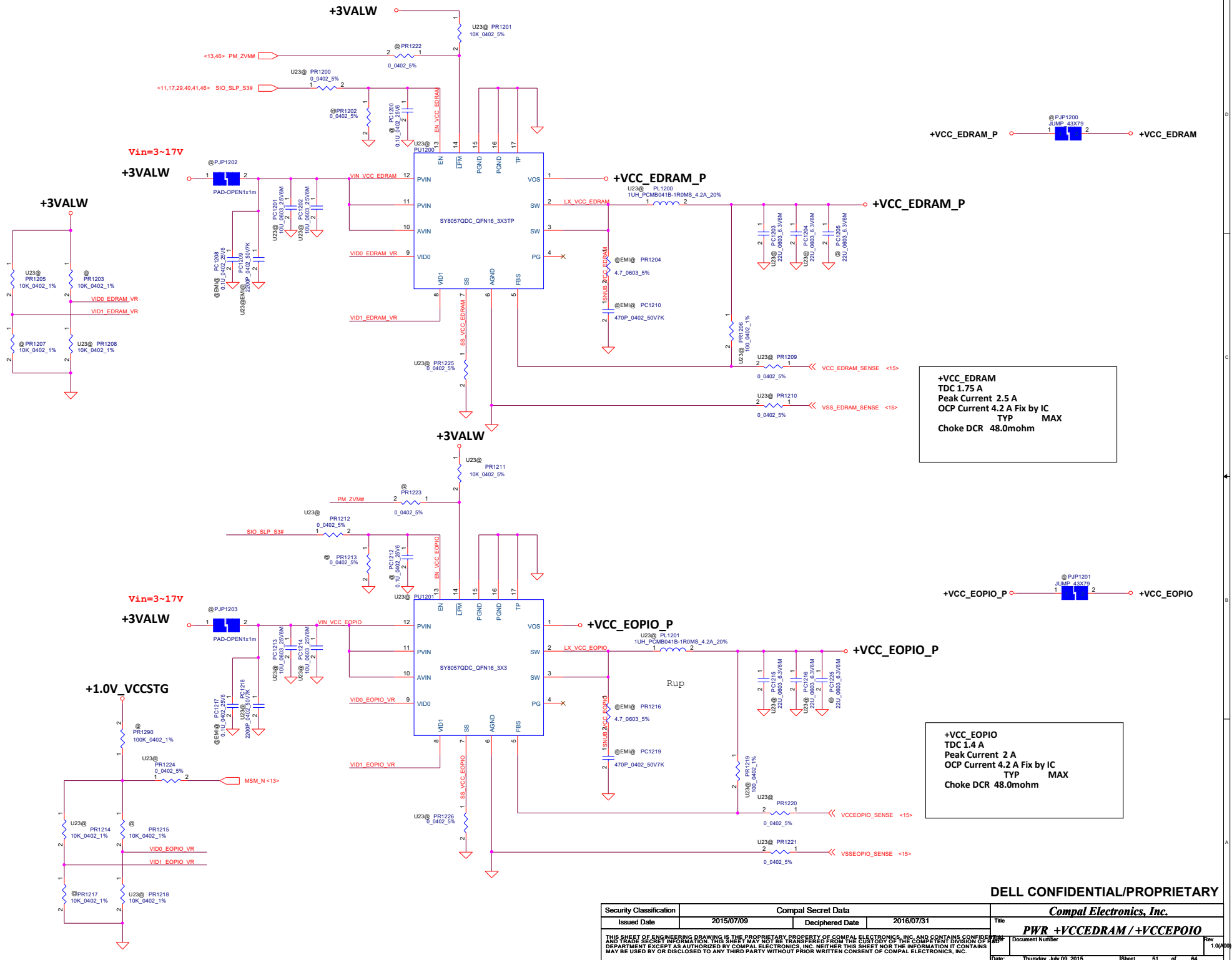


For VGACORE

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PWR_CPU&VGA bulk and MLCC



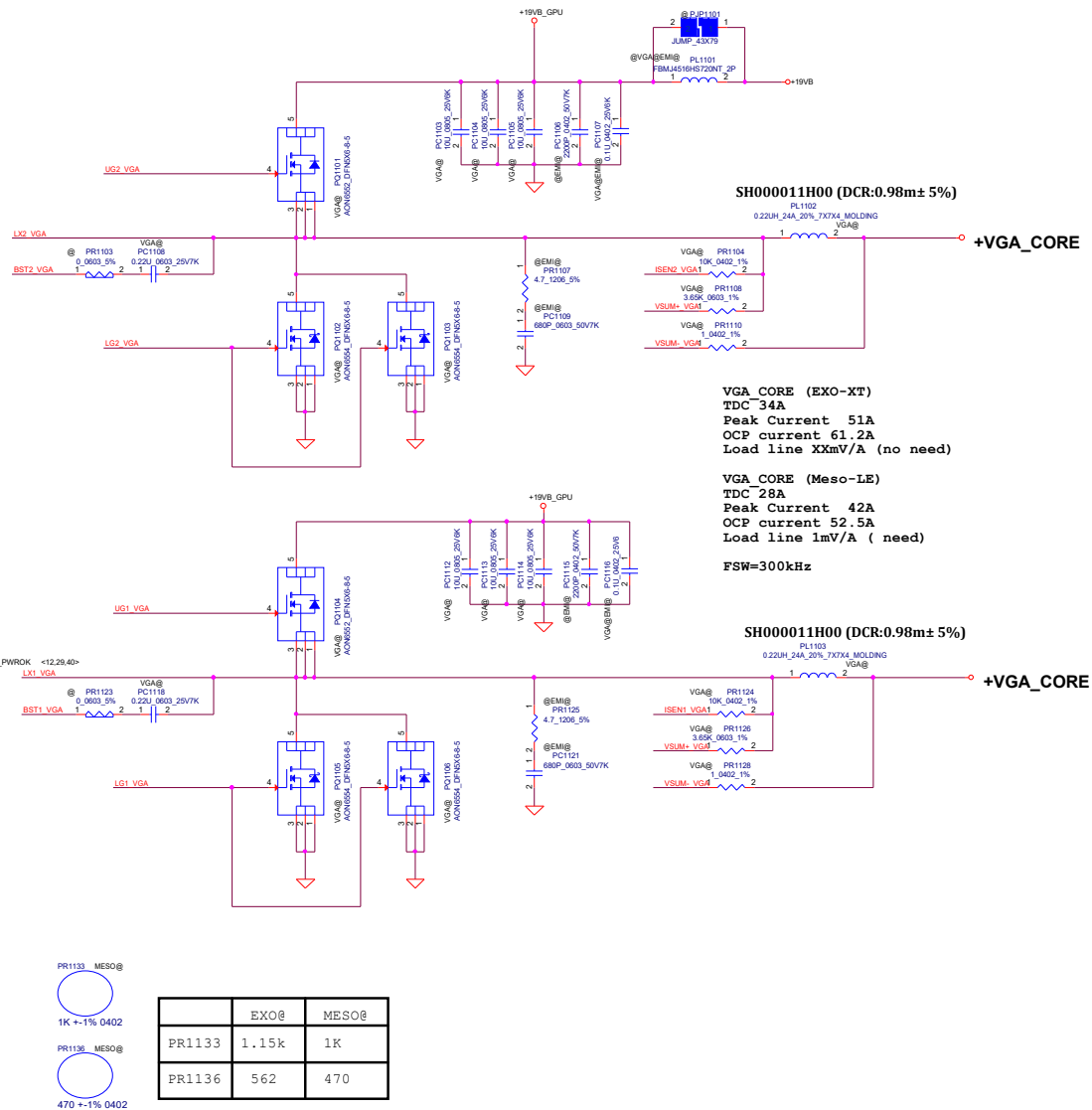
+VCC_EDRAM
TDC 1.75 A
Peak Current 2.5 A
OCP Current 4.2 A Fix by IC
TYP MAX
Choke DCR 48.0mohm

+VCC_EOPIO_P

+VCC_EOPIO
TDC 1.4 A
Peak Current 2 A
OCP Current 4.2 A Fix by IC
TYP MAX
Choke DCR 48.0mohm

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Date: Thursday, July 09, 2015				Sheet 51 of 64



	EXO@	MESO@
PR1133	1.15k	1K
PR1136	562	470

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	NA	HW or PWR	NA	COMPAL	NA	NA	NA
2				COMPAL			
3				COMPAL			
4				COMPAL			
5				COMPAL			
6				COMPAL			
7				COMPAL			
8				COMPAL			
9				COMPAL			
10				COMPAL			
11				COMPAL			0.2 (X01)
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Size		Document Number					Rev 1.0/40
Date:		Thursday, July 09, 2015		Sheet		53 of 64	

Version Change List (P. I. R. List)							
Item	Page #	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1		HW	20141124	GENERAL	Power sequence	1. Add RC344 for BCM SWPWRG reserved 2. Add UC13, RC343, RC345, RC429 for IMVP_VR_ON	0.1 (X000)
2		HW	20141124	GENERAL	Debug conn	1. Delete JABE1, JBP11	0.1 (X000)
3		HW	20141125	GENERAL	Correct XDP conn and GPIO check	1. Change XDP conn 2. Add RC430 for GPIO21 reserve 3. Add RC336, RC337, RC338 for GPIO pull-up 4. Delete RC27, RC330, UC11, RC24	0.1 (X000)
4		HW	20141126	GENERAL	Circuit double	1. Delete R22, R23 for double circuit.	0.1 (X000)
5		HW	20141128	GENERAL	GPIO modify	1. Add RC360 for PWRED_VGA 2. Delete RC383, RC374, RC447, RC603, RC604, RC26, RC337, Q2505, RC604 C265, C821, R74 3. Add U84, Q2504, U5602	0.1 (X000)
6		HW	20141203	GENERAL	GPIO modify	1. Add RC437 2. Delete R84	0.1 (X000)
7		HW	20141204	GENERAL	Follow M16 EE implementation guide modify	1. Delete C810, RC620, RC620, RC621, RC621, Q2402, C810, RC621, RC622, RC627 2. Add C814, C815, RC612, RC614, RC615, RC381	0.1 (X000)
8		HW	20141210	GENERAL	PCB Strap modify	1. Add D5503, RC439	0.1 (X000)
9		HW	20141212	GENERAL	PCB Strap modify	1. Add RC360 2. Change VCCIO, ROPD, EDORAM power enable by R38 3. Delete RC362, RC363 4. VCCP_PWRD control by RC	0.1 (X000)
10		HW	20141216	GENERAL	1. COR_VTT_CTRL 2. CORRC 3. LFC connector 4. VCCPWR control	1. Add UC14, C257, RC123 for COR_VTT_CTRL buffer 2. Delete R24 3. Change R23 to 1K and move to D701 pin1 4. Change R27 to 1K 5. Move C255 to ADJ_JB24 and change to 0.1uF 6. Move RC391-RC394 to R201-RC204 pin1 7. Move RC391, RC392, RC393 and RC394 to R209, R297, R299, R291 pin1 8. Change C297, C298 to 10uF/10V/5603 9. Change D82 location to D8 10. Add UC15 for VCCPWR control, delete R25	0.1 (X000)
11		HW	20141217	GENERAL	1. DMSX power rail 2. FRCWRD 3. DMSD_ID 4. CORRC 5. Touch pad 6. USB power	1. pop RC15, RC17, de-pop RC426, RC427 2. RC17 de-pop 3. Change VREF CPU to +1.0V_VCCPWR 4. Delete RC338, connect VCC_CPU_LPS to +1.0V_VREF 5. Change C238-C239 pin1 to +1.0V_VREF 6. Add C238-C239 for VREF_EDORAM 7. Add C238-C239 for VREF 8. Add C239 for VREF 9. Add C237 for VREF,DC 10. Change D82 VIN from +1.0V_VREF to +1.0V_VREF 11. Add RC338 for +1.0V_VREF to +1.0V_VREF 12. Delete R409 for HMC power config 13. Change DMSD pin 2, 10 from 30V_20 to +VPS 14. Change DMSD pin 2, 10 from 30V_20 to +VPS	0.1 (X000)
12		HW	20141218	GENERAL	1. GPIO 2. RC 3. CPU 4. DSI to VGA	1. Add RC367, delete R240, R254, R255 for MISO VIA CORE power 2. RC 3. Change VREF CPU to +1.0V_VCCPWR 4. Delete RC338, connect VCC_CPU_LPS to +1.0V_VREF 5. Change C238-C239 pin1 to +1.0V_VREF 6. Add C238-C239 for VREF_EDORAM 7. Add C238-C239 for VREF 8. Add C239 for VREF 9. Add C237 for VREF,DC 10. Change D82 VIN from +1.0V_VREF to +1.0V_VREF 11. Add RC338 for +1.0V_VREF to +1.0V_VREF 12. Delete R409 for HMC power config 13. Change DMSD pin 2, 10 from 30V_20 to +VPS 14. Change DMSD pin 2, 10 from 30V_20 to +VPS	0.1 (X000)
13		HW	20141219	GENERAL	1. GPIO 2. CORRC	1. Add RC15, RC17, de-pop RC426, RC427 2. RC17 de-pop 3. Change +3V_1.0V_VCCPWR to DMSD	0.1 (X000)
14		HW	20141222	GENERAL	1. Power rail 2. Debug solution	1. Change VREF CPU to +1.0V_VREF 2. Delete R27, R28 3. Add R27, RC369 for debug port 4. Swap R2 pin for layout routing smoothly	0.1 (X000)
15		HW	20141223	GENERAL	1. Power rail 2. Debug solution	1. Change +1.0V_VCCPWR to +1.0V_VCCPWR 2. Delete RC338 3. Add R27, RC369, RC370, R4702, R4703, R4704, R4706, C4701, U4701 -R4701 for debug port 4. Change R27, R28 5. Delete R27, R28, +VREF	0.1 (X000)
16		HW	20141224	GENERAL	1. Debug solution	1. Delete R421, R422, RC27, R4702, R4703, R4704, R4706, C4701 R4701, R27 for debug port 2. Add RC32, RC33 for debug port	0.1 (X000)
17		HW	20141226	GENERAL	1. RMT CAP	1. Delete C284, C287, C284 for placement	0.1 (X000)
18		HW	20141228	GENERAL	1. GPIO	1. Change C14, RC1, LFC, MFC to RC1, C14, LFC 2. Delete R407, Add R208-R210 for RMT_RMT_ID 3. Add RC339 for RMT_RMT_ID 4. Add RC337-RC370 for RMT_RMT_ID, RMT_RMT_ID 5. Add RC374-RC377 for RMT_RMT_ID, RMT_RMT_ID 6. Add RC378-RC381 for RMT_RMT_ID, RMT_RMT_ID 7. Swap R20, R21, R22 to R20, R21 8. Swap R20, R21, R22 to R20, R21 9. Swap R20, R21, R22 to R20, R21 10. Swap R20, R21, R22 to R20, R21 11. Add RC337 for RMT_RMT_ID, RMT_RMT_ID 12. Swap RMT_RMT_ID to RMT_RMT_ID 13. Add RC337 for RMT_RMT_ID, RMT_RMT_ID 14. Change R20, R21, R22 to R20, R21, R22 15. Add R20, R21, R22 to R20, R21, R22 16. Swap R20, R21, R22 to R20, R21, R22 17. Swap R20, R21, R22 to R20, R21, R22 18. Add RC337, RC338 for RMT_RMT_ID, RMT_RMT_ID 19. Replace R20, R21, R22 to RMT_RMT_ID, RMT_RMT_ID 20. Add RC337 for RMT_RMT_ID, RMT_RMT_ID 21. Add R20 for RMT_RMT_ID 22. Add R20, delete R21 23. Delete R20, R21, R22 to RMT_RMT_ID, RMT_RMT_ID 24. Add R20, R21, R22 to RMT_RMT_ID, RMT_RMT_ID 25. Delete UC13, RC2, R27, R28, Add RC339 for ALL_VREF_PWRD 26. Add RC339, R27 for VCCP_PWRD 27. Delete R27, R28, R29 28. Add RC339 for L_PWR, R27, R28, delete D5503, R4304 29. Change VREF CPU to +1.0V_VREF 30. Swap R20, R21, R22 to RMT_RMT_ID, RMT_RMT_ID 31. Swap R20, R21, R22 to RMT_RMT_ID, RMT_RMT_ID 32. Swap R20, R21, R22 to RMT_RMT_ID, RMT_RMT_ID 33. Swap R20, R21, R22 to RMT_RMT_ID, RMT_RMT_ID	0.1 (X000)
19		HW	20141229	GENERAL	1. GPIO	1. Add Q150, R150 for RMT_RMT_ID	0.1 (X000)
20		HW	20141230	GENERAL	1. Change CPU part number 2. Change capacitor part number 3. Change USB Load switch symbol and part number 4. Add CPU dummy symbol, modify PCB dummy symbol	1. Change part number R41145071 to R41145071-UC1A-UC17 2. Change part number R41145071 to R41145071-UC1A-UC17 3. Change USB Load switch symbol and part number 4. Add CPU dummy symbol, modify PCB dummy symbol 5. Change symbol and part number from R41145071 to R41145071-UC1A-UC17 6. Change symbol and part number from R41145071 to R41145071-UC1A-UC17	0.1 (X000)
21		HW	20150108	GENERAL	1. Change CPU part number 2. Change capacitor part number 3. Change USB Load switch symbol and part number 4. Add CPU dummy symbol, modify PCB dummy symbol	1. Change part number R41145071 to R41145071-UC1A-UC17 2. Change part number R41145071 to R41145071-UC1A-UC17 3. Change USB Load switch symbol and part number 4. Add CPU dummy symbol, modify PCB dummy symbol 5. Change symbol and part number from R41145071 to R41145071-UC1A-UC17 6. Change symbol and part number from R41145071 to R41145071-UC1A-UC17	0.1 (X000)

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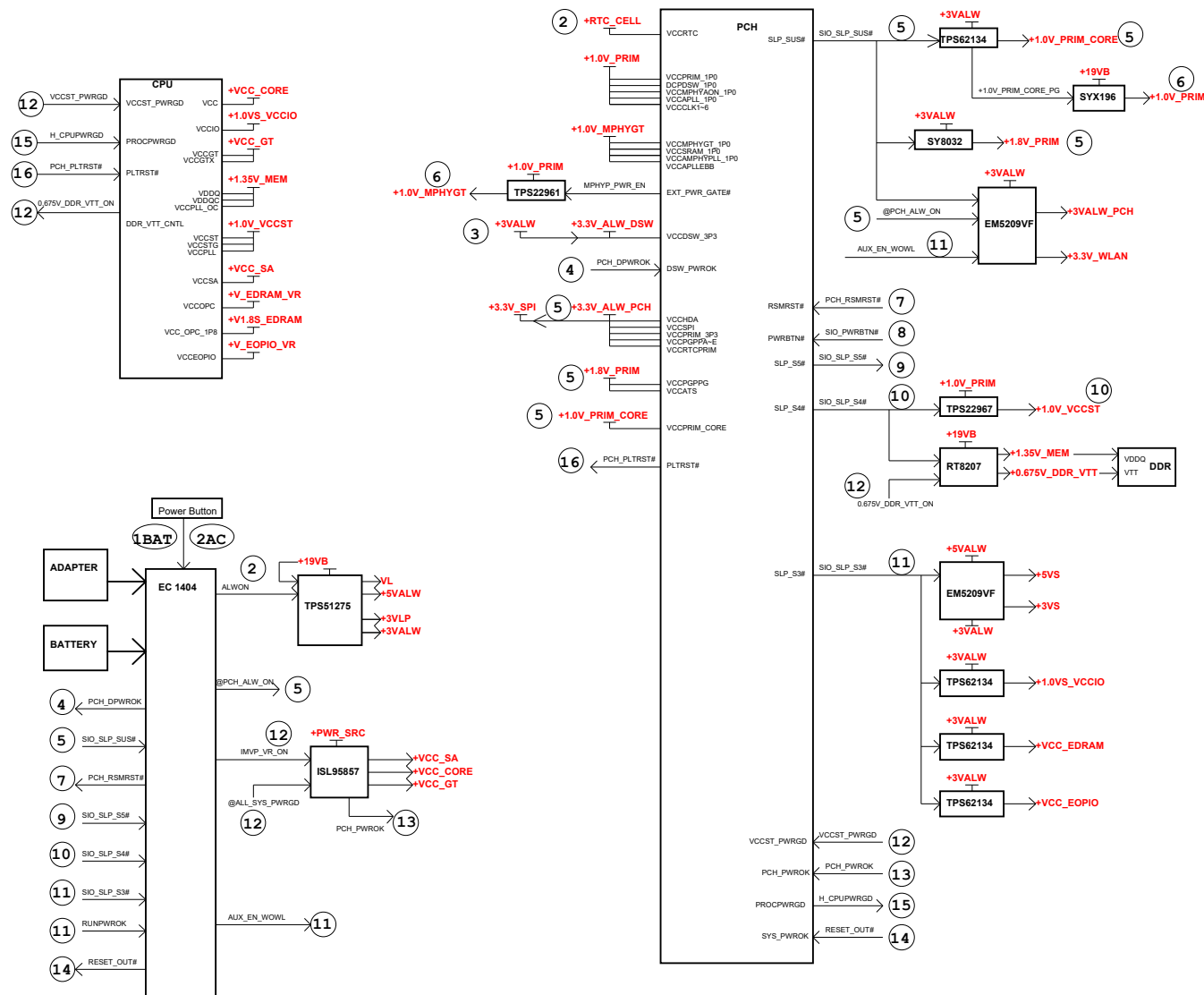
EE Change list

L-0071P

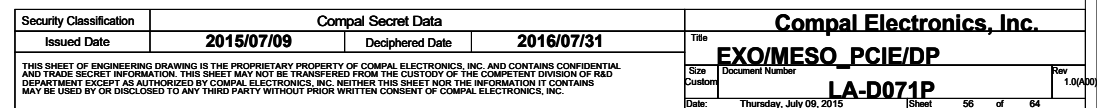
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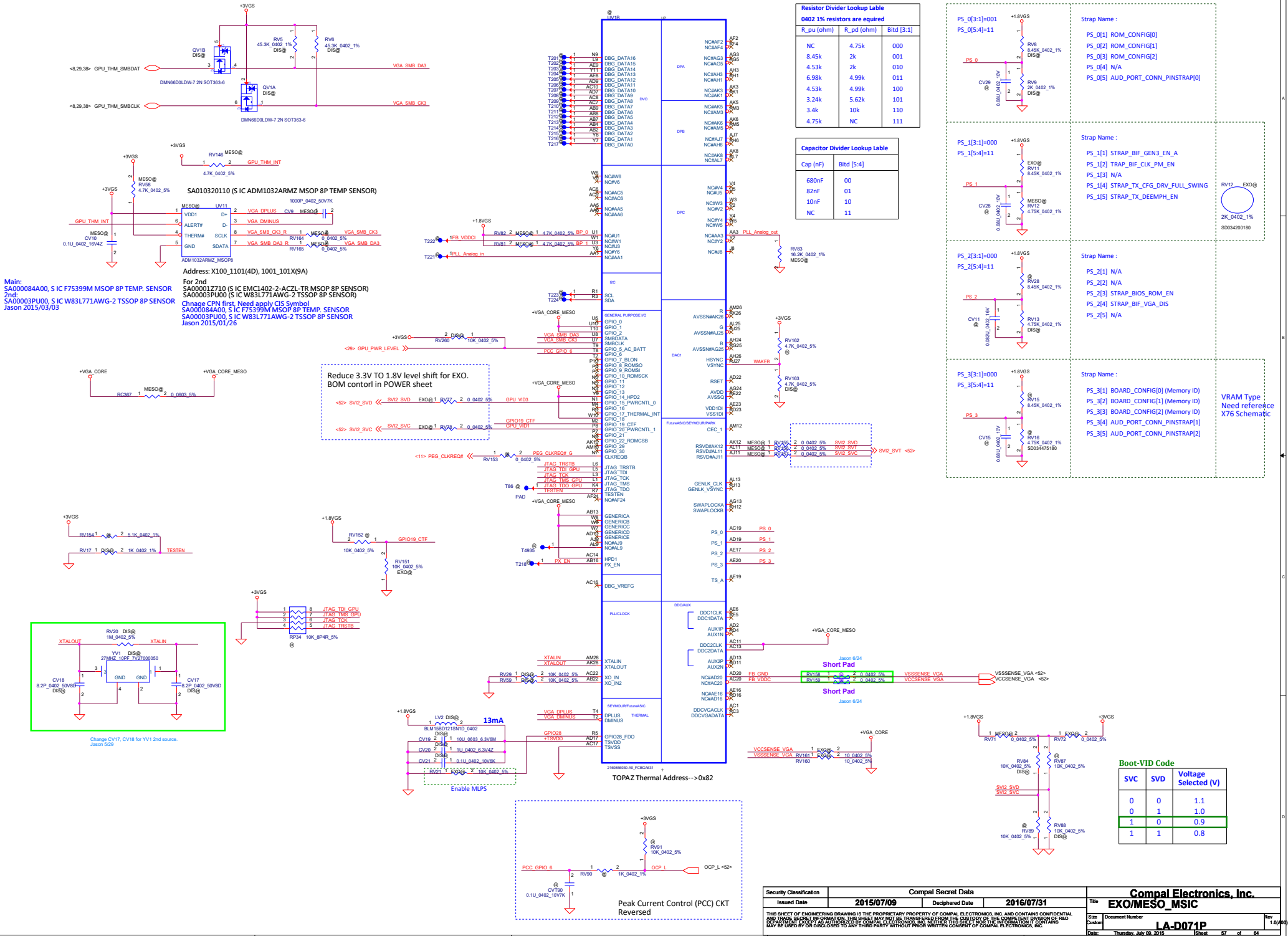


Timing Diagram for S5 to S0 mode



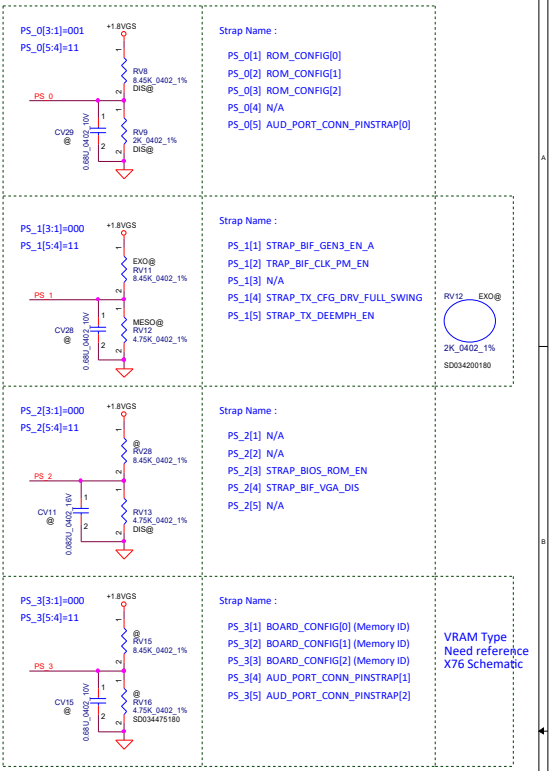
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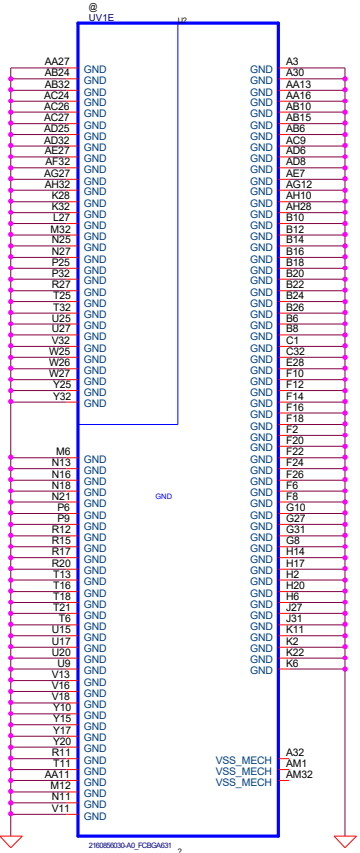
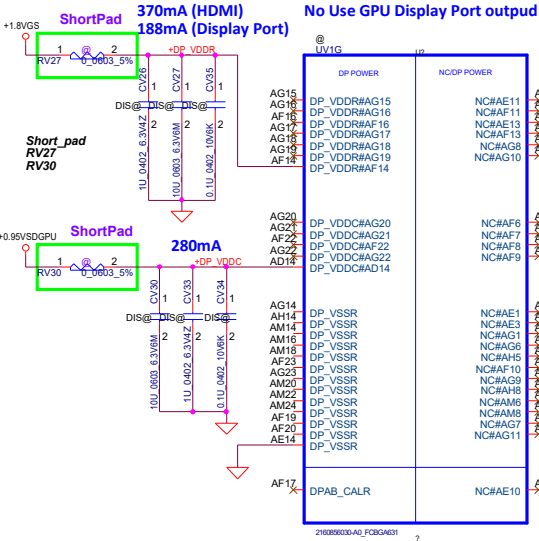
Resistor Divider Lookup Table			
0402 1% resistors are required			
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]	
NC	4.75k	000	
8.45k	2k	001	
4.53k	2k	010	
6.98k	4.99k	011	
4.53k	4.99k	100	
3.24k	5.62k	101	
3.4k	10k	110	
4.75k	NC	111	

Capacitor Divider Lookup Table	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



Boot-VID Code		
SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

+1.35VS_VGA TO +1.35V_MEM_GFX
JP9 DEFAULT SHORT



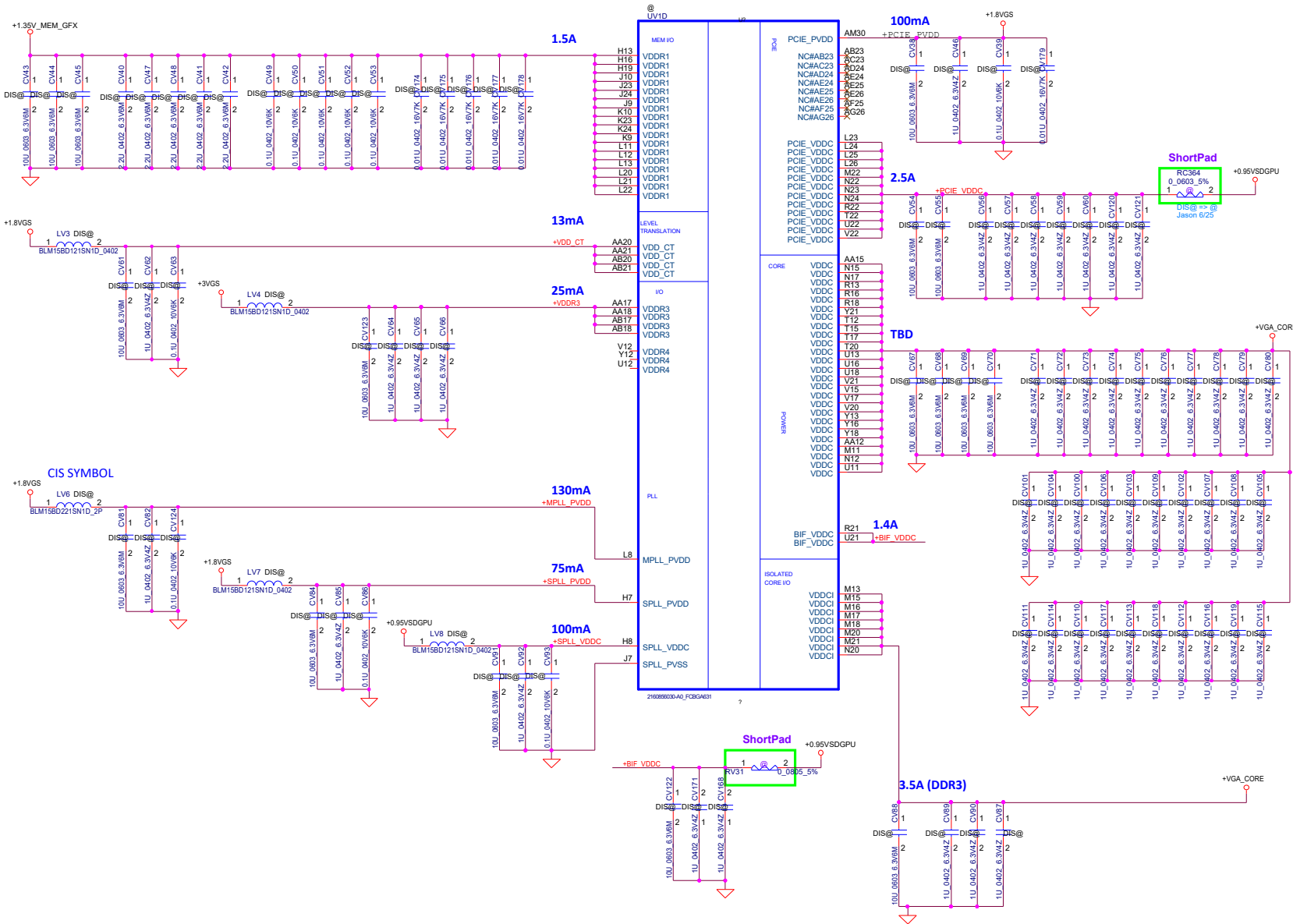
+VGA_CORE	10uF	1uF	0.1uF
VDDC	TBD	5 (1@)	10 (2@)
VDDCI	3.5A	1	3

+0.95VSDGPU	10uF	1uF	0.1uF
PCIE_VDDC	2.5A	2 (1@)	5 (1@)
BIF_VDDC	1.4A	0	1
SPLL_VDDC	100mA	1	1

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1 1.5A	3	5	5	5

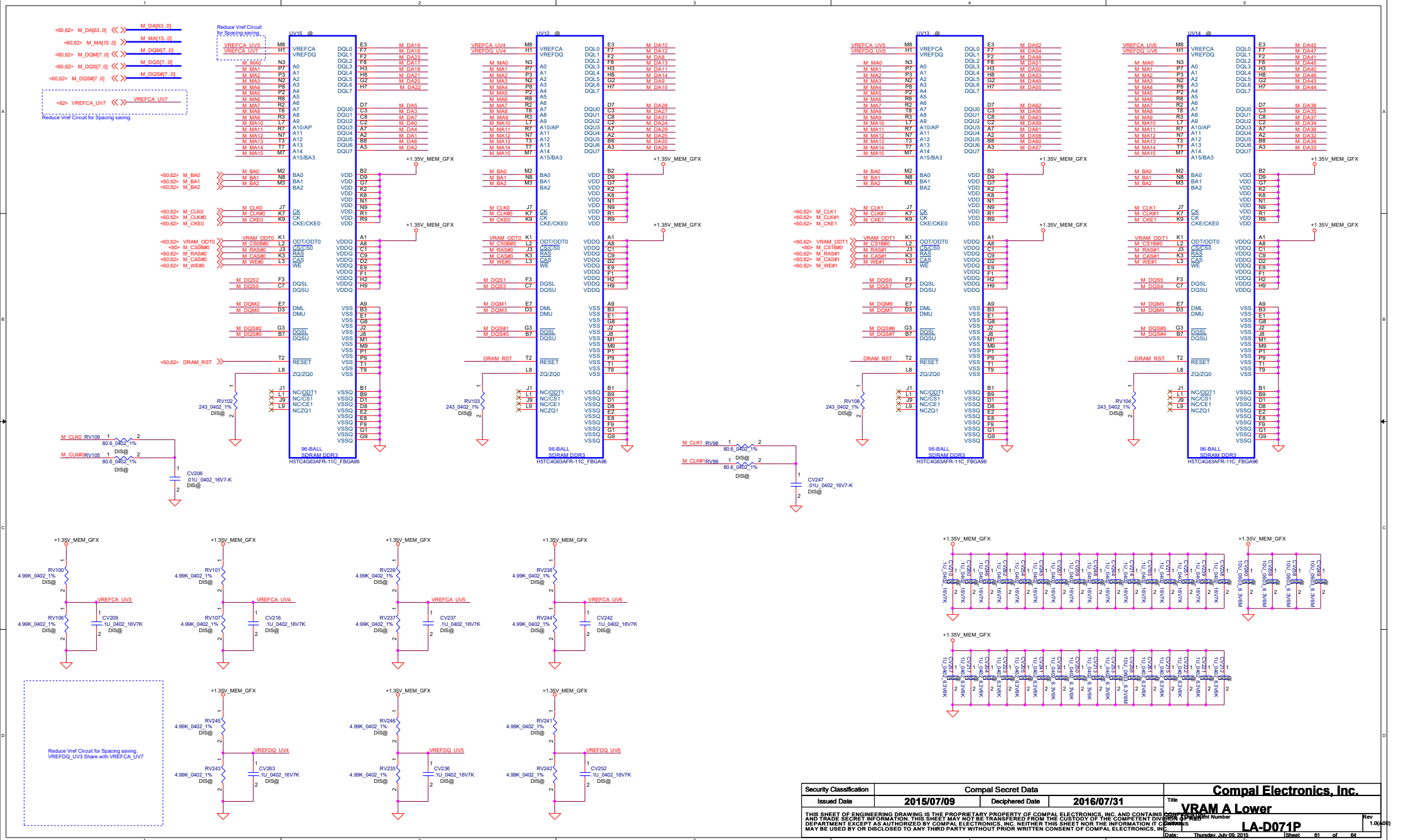
+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	1
MPLL_PVDD	130mA	1	1	1
SPLL_PVDD	75mA	1	1	1
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	1	1	1
+TSVDD	13mA	1	1	1
+DP_VDDR		0	0	0
+DP_VDDC		0	0	0

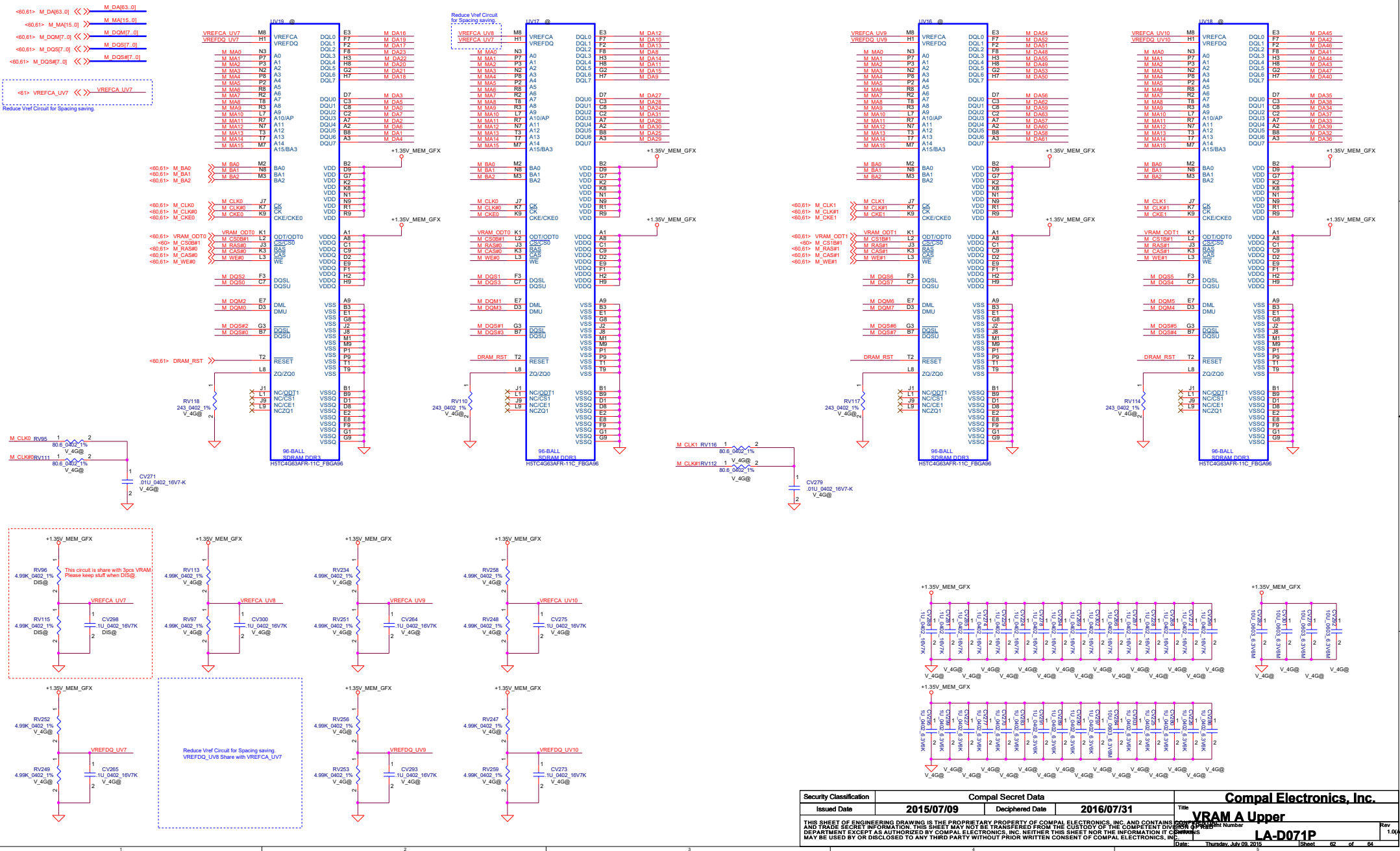
+3VGS	10uF	1uF	0.1uF
VDDR325mA	0	2 (1@)	1



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Power-Up/Down Sequence

- 1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- 2. It is recommended that the 3.3-V rail ramp up first.
- 3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
- 4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/μs).
- 5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- 6. For power down, reversing the ramp-up sequence is recommended.

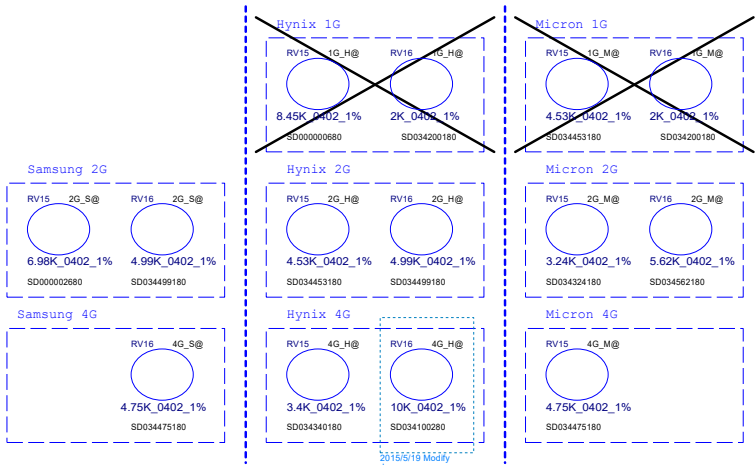
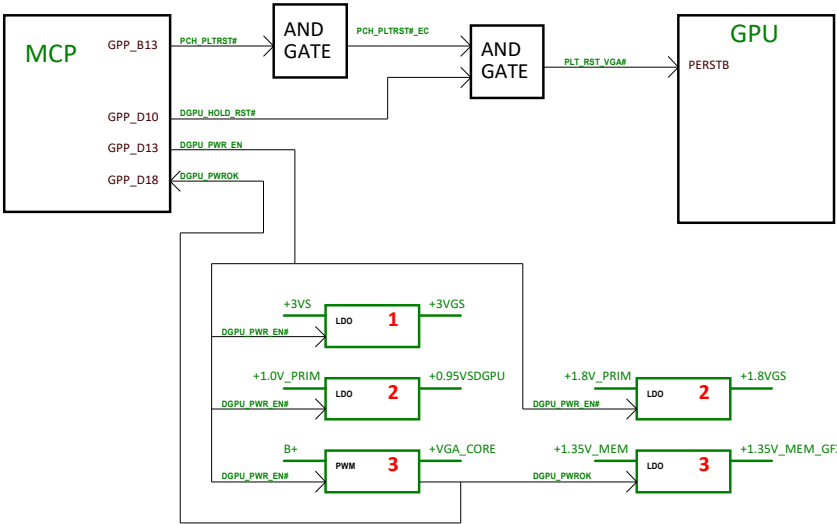
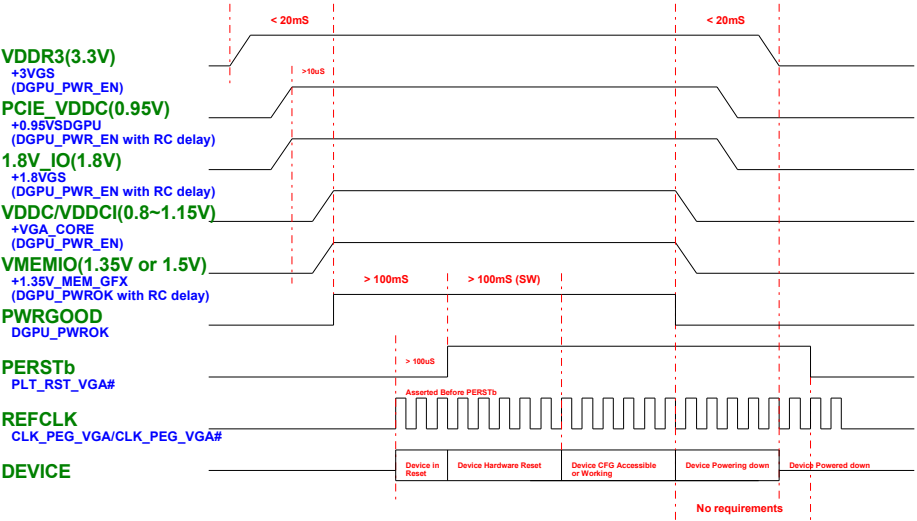


Table 3–21 Resistor Divider Lookup T

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.



For AMD EXO-XT VRAM Only

Memory ID	P/N	Vendor	Configuration	Size
000	SA000076P2L	SAMSUNG	256MX16 K4W4G1646E-BC1A FBGA 96P	4GB
110	SA00008DN0L	HYNIX	256MX16 H5TC4G63CFR-NOC FBGA 96P	4GB
111	SA000077K0L	Micron	256M16 MT41J256M16HA-093G:E FBGA	4GB
011	SA000076P2L	SAMSUNG	256MX16 K4W4G1646E-BC1A FBGA 96P	2GB
100	SA00008DN0L	HYNIX	256MX16 H5TC4G63CFR-NOC FBGA 96P	2GB
101	SA000077K0L	Micron	256M16 MT41J256M16HA-093G:E FBGA	2GB

For AMD MESO-LE VRAM Only

Memory ID	P/N	Vendor	Configuration	Size
011	SA000076P2L	SAMSUNG	256MX16 K4W4G1646E-BC1A FBGA 96P	2GB
100	SA00008DN0L	HYNIX	256MX16 H5TC4G63CFR-NOC FBGA 96P	2GB
101	SA000077K0L	Micron	256M16 MT41J256M16HA-093G:E FBGA	2GB

