

# Compal LA-K701P

## GH5JJ/GH7JJ MB Schematic Document

Rev: 1C

2020.11.10

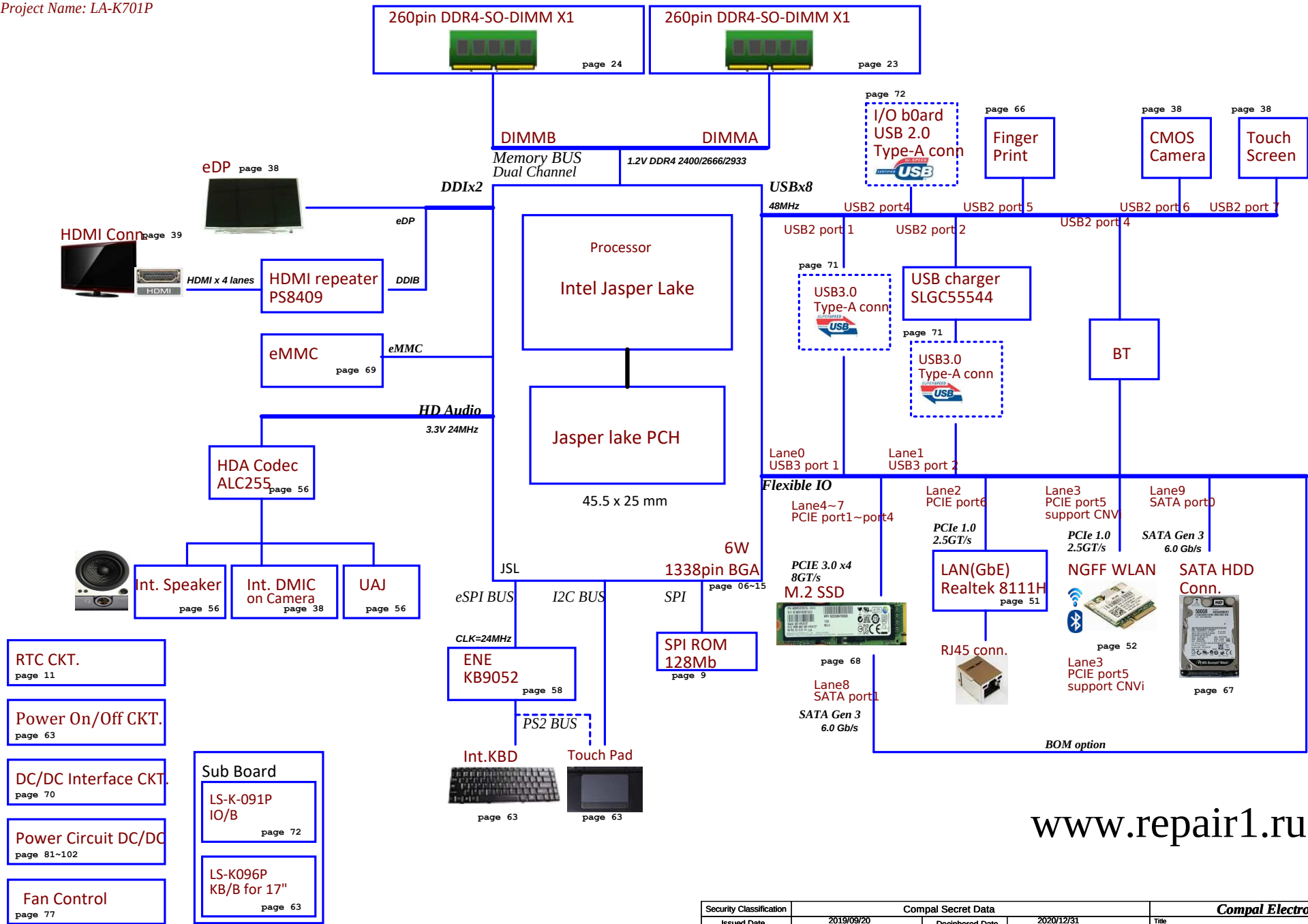
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Compal Confidential

Model Name: Jasper Lake

Project Name: LA-K701P



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Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V <sub>BIAS</sub> min	V <sub>BIAS</sub> typ	V <sub>BIAS</sub> max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xBF
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xC8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xFF
19	NC	3.000 V	3.000 V		0xFF1 - 0xFF

HSIO Port	Capable	Port Allocation	PCIE CLK	NOTE
0	USB3.1 Gen2 #1	USB3.1 Type A	NA	USB3.1 interface
1	USB3.1 Gen2 #2	USB3.1 Type A (with charger)	NA	USB3.1 interface
2	USB3.1 #2 / PCIe #5	WLAN	CLK0 & CLKREQ#0	PCIe interface
3	USB3.1 #1 / PCIe #6	GLAN	CLK2 & CLKREQ#2	PCIe interface
4	USB3.1 #3/PCIe #4 PCIe #3 PCIe #2 PCIe #1	SSD (NGFF Key M)	CLK1 & CLKREQ#1	PCIe interface
5				
6				
7				
8	USB3.1 #4 / PCIe #8 /SATA1	SSD (NGFF Key M)	NA	SATA interface
9	PCIe #7 /SATA1	HDD	NA	SATA interface
10				
11				

43#	GH5JJ/ GH7JJ	Load BOM Option
431AMXBOL01	431AMXBOL51	GSEN@/FP@/255@/CHG@/TPM@/PREM@/DVT@/MEM@/CNVi@/CMC@/GLITCH@/UMA@/3S@/ES2_i3@/FP3V@/USBT
431AMXBOL04	431AMXBOL52	GSEN@/FP@/255@/CHG@/TPM@/PREM@/DVT@/MEM@/CNVi@/CMC@/GLITCH@/UMA@/3S@/ES2_i5@/FP3V@/USBT
431AMXBOL03	431AMXBOL53	GSEN@/FP@/255@/CHG@/TPM@/PREM@/DVT@/MEM@/CNVi@/CMC@/GLITCH@/UMA@/3S@/ES2_i7@/FP3V@/USBT

HW Function	BOM Structure
EMI / EMC / ESD	EMC@XEMC@
RF Components	@RF@
Premium/Volumentary	PREM@ VOL@
CNVi	CNVi@
UART	UART@
CPU	
Finger Print	FP@ FPEMC@FP3V@ FP5V@
GLITCH	GLITCH@
Touch screen	I2CTS@USBSTS@
I2C/USB	EVT@ PVT_6W@ PVT2_6W@ EVT2@ PVT_10W@PVT2_10W@
Board ID	
TPM	TPM@
Gsensor	GSEN@
Charger	CHG@ NCHG@
over 3 cell battery	B@
NC Components	@
ME Cnncetor	CONN@
Audio	255@ 256@ 255M@
EMMC	EMMC@ NEMMC@
SSD	M2PCIE@ M2SATA@
PCB	PCB@
EMMC sku	SD64@ SD128@ KS64@ KS128@

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SOC_SMBCLK SOC_SMBDATA	+3V_PRIM level shift to +3VS	DIMM0/1	TBC	TBC	TBC
		G-sensor	TBC	TBC	TBC
SOC_SML0CLK SOC_SML0DATA	+3V_PRIM	NC	TBC	TBC	TBC

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
EC_SMB_CK1 EC_SMB_DA1	+3VLP_EC	BAT	TBC	TBC	TBC
		CHGR	TBC	TBC	TBC
EC_SMLCLK EC_SML0DATA	NC	NC	TBC	TBC	TBC

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
I2C 0	NC	NA	TBC	TBC	TBC
I2C 1	NC	NA	TBC	TBC	TBC
I2C 2	NC	NA	TBC	TBC	TBC
I2C 3	+3VALW_PRIM	Touch Pad	0x2CH	TBC	TBC
I2C 4	NC	NA	0FH	TBC	TBC
I2C 5	+3VS	Touch Screen ( I2C interface )	TBC	TBC	TBC
ISH_I2C 0	NC	NA	TBC	TBC	TBC
ISH_I2C 1	NC	NA	TBC	TBC	TBC

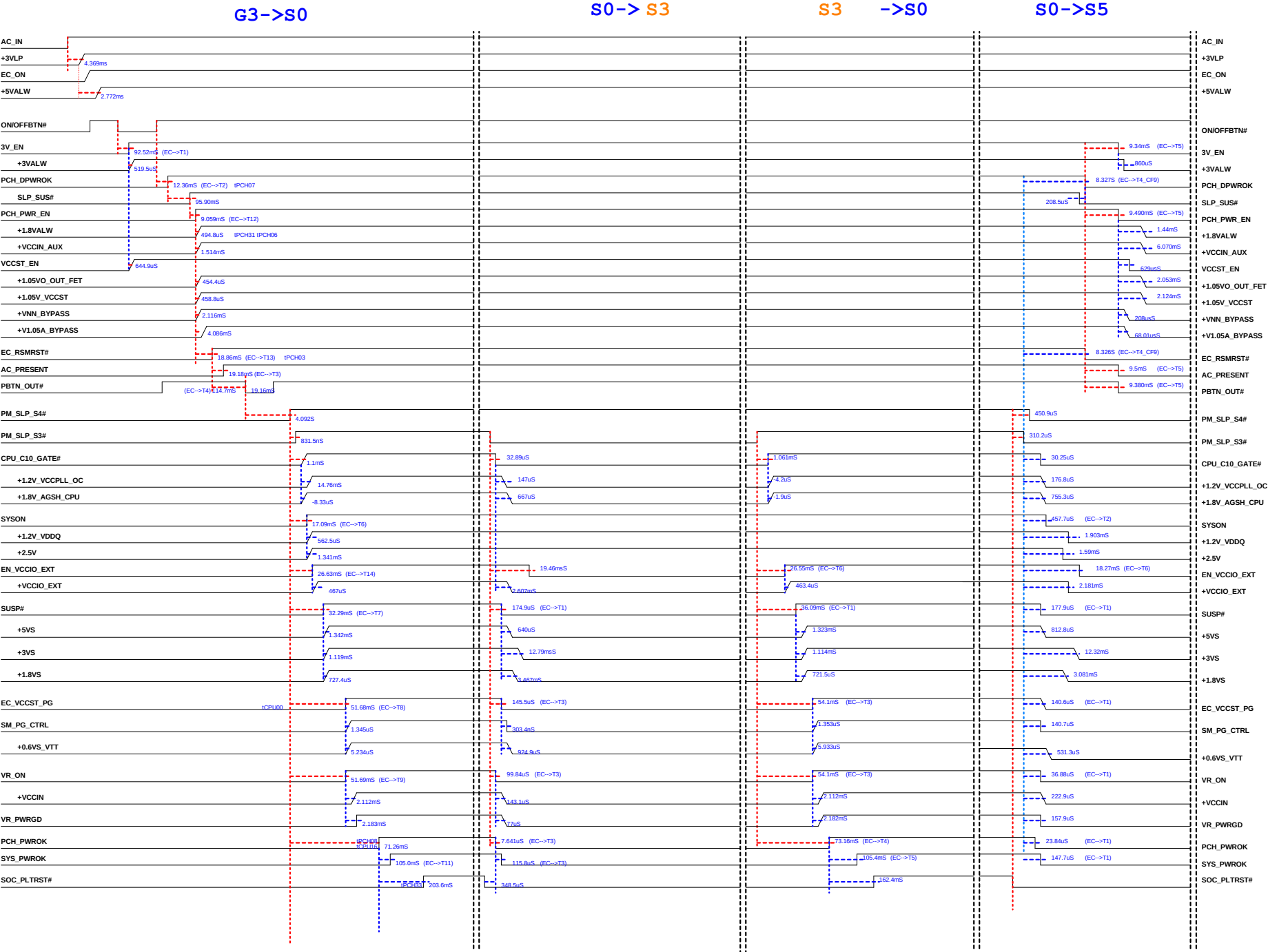
Power Plane	Description	S0	S0ix	S3	S4/S5
+19V ADPIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V BATT+	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+VCCIN	Processor FIVR input power supply	ON	OFF	OFF	OFF
+VCCIN_AUX	PCH FIVR input power supply	ON	OFF	OFF	OFF
+VCCIO_EXT	Supply for PCH and Processor VCCIO_EXT	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR termination	ON	OFF	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby mode	ON	ON	ON	OFF
+1.05VS_VCCST	Gated version of VCCST	ON	OFF	OFF	OFF
+1.2V_VDDQ	DDR4/L-RS +1.2V power rail and CPU digital PLL	ON	ON	ON	OFF
+2.5V	DDR4/L-RS +2.5V power rail	ON	ON	ON	OFF
+1.8VALW_PRIM	PCSS/AGSH TypeC sub system / CPU analog power supply	ON	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+3VALW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*
+3V PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF

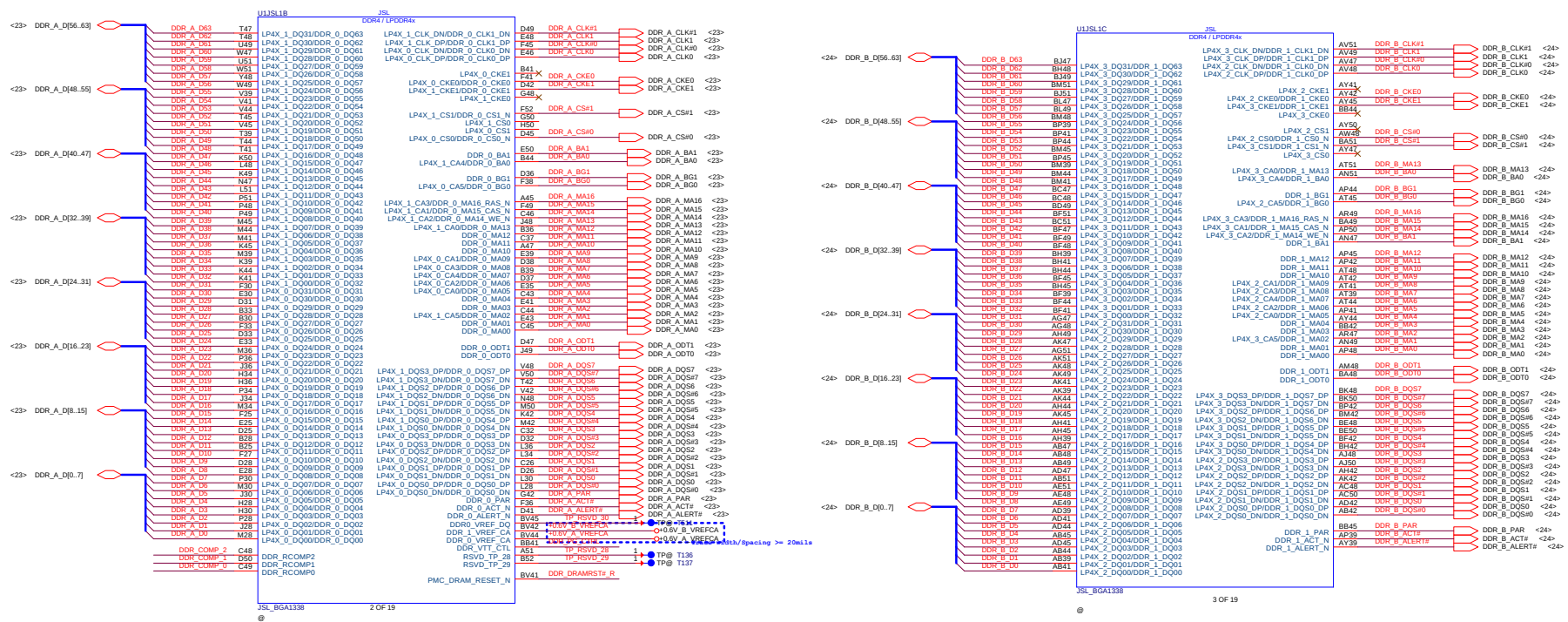
Adaptor	45W@ 65W@
TEMP. protect	OTP@
4 cell battery	4S_BATT@
EMI	EMI@ @EMI@
RF Components	@RF@

USB2.0 Port	Device
1	USB Type-A ( MB )
2	USB Type-A ( MB )
3	NA
4	USB Type-A ( IO Board
5	FP
6	Camera
7	TS
8	BT

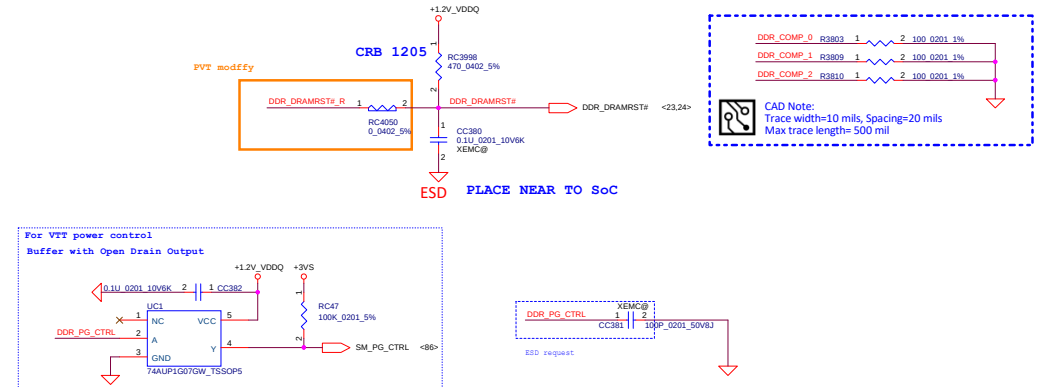
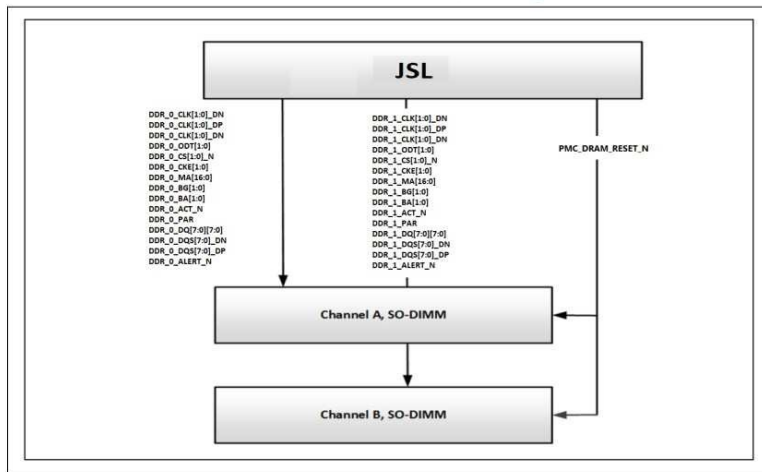




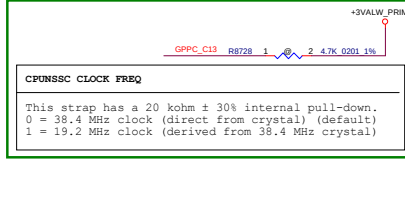
@ = Un-Stuff



**Figure 46. DDR4 SODIMM Back-to-Back Placement and Block Diagram**



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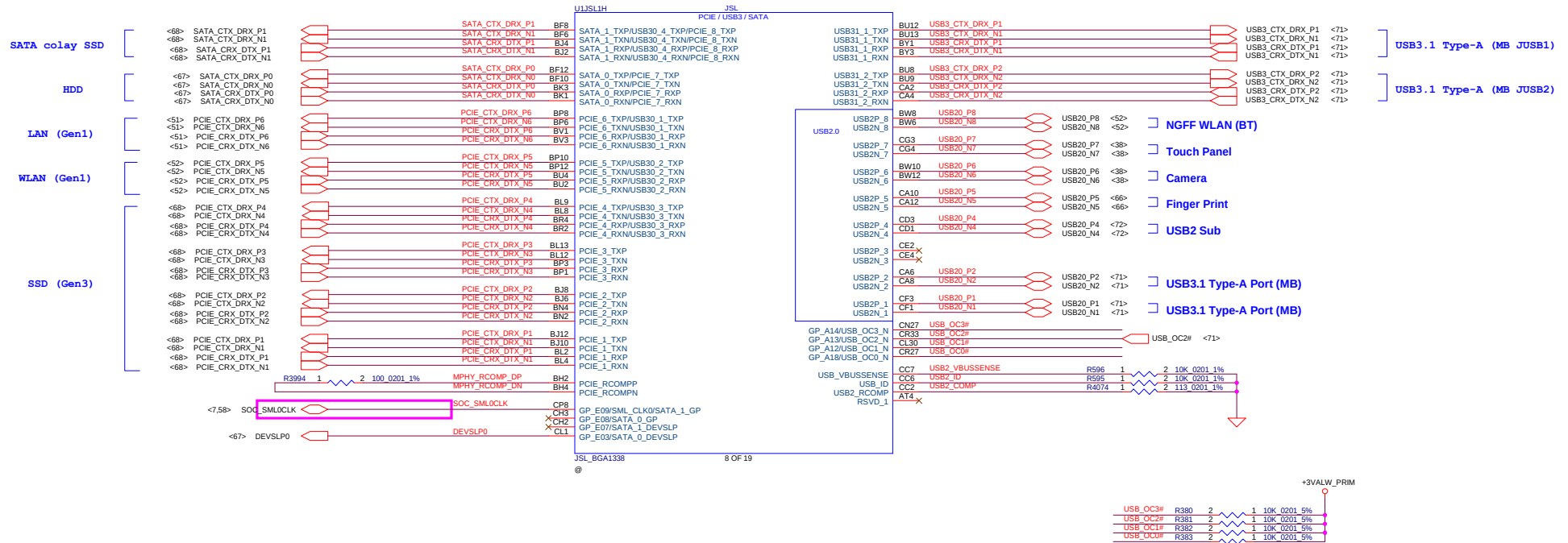
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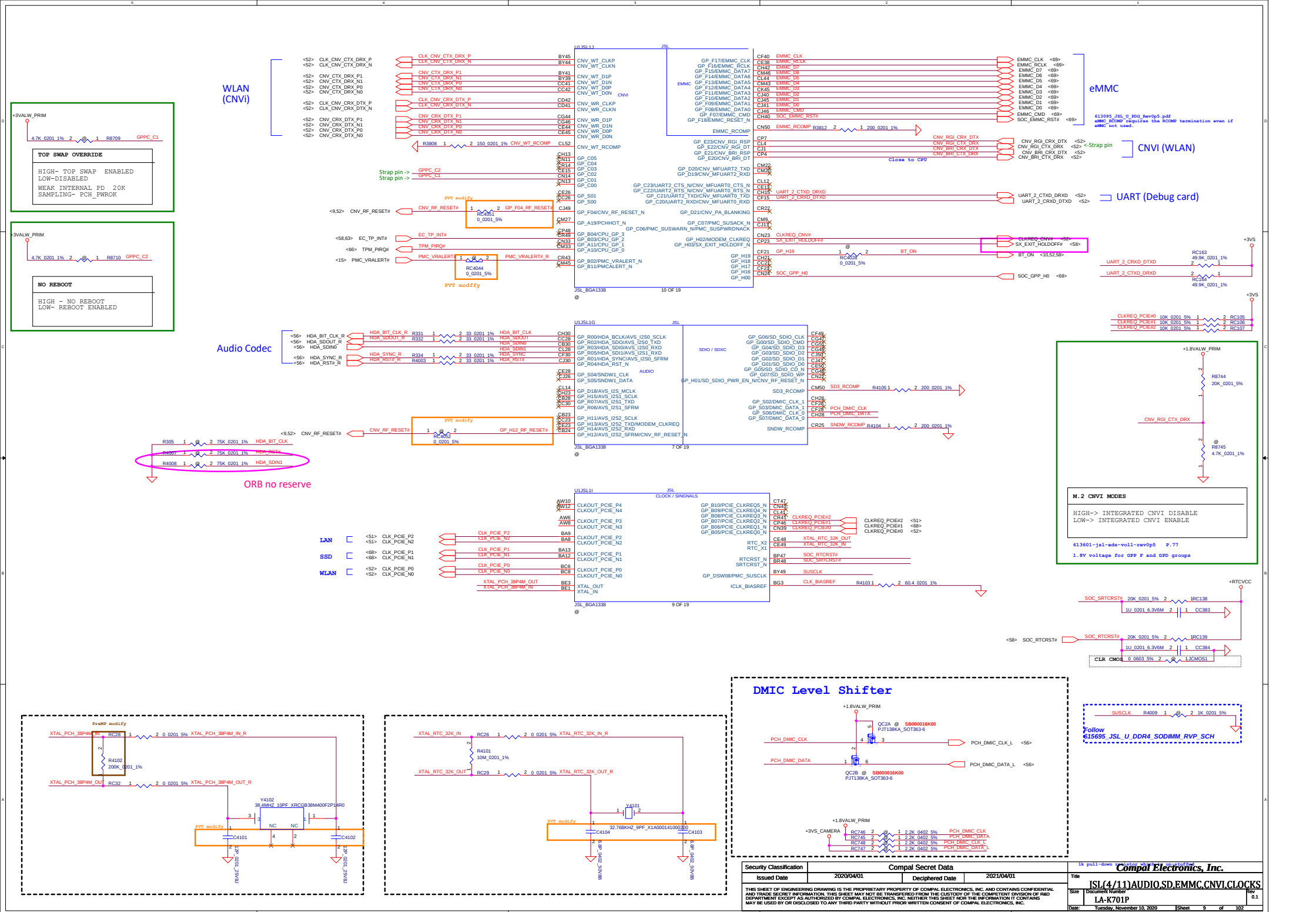
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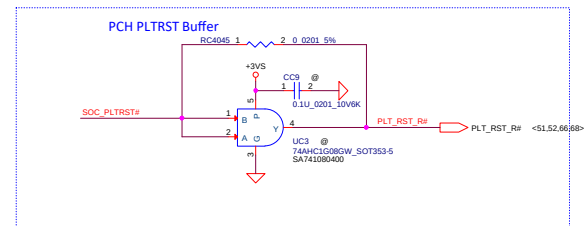
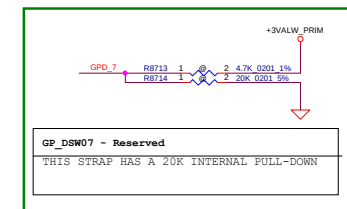
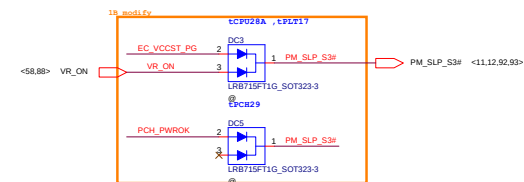
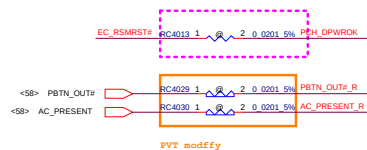
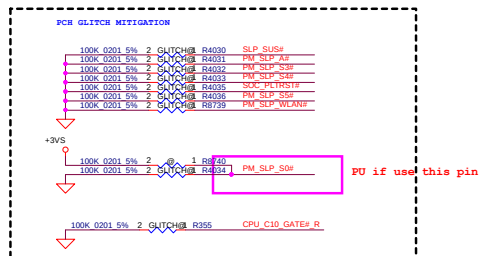




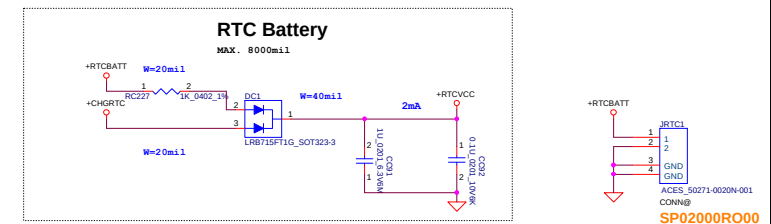
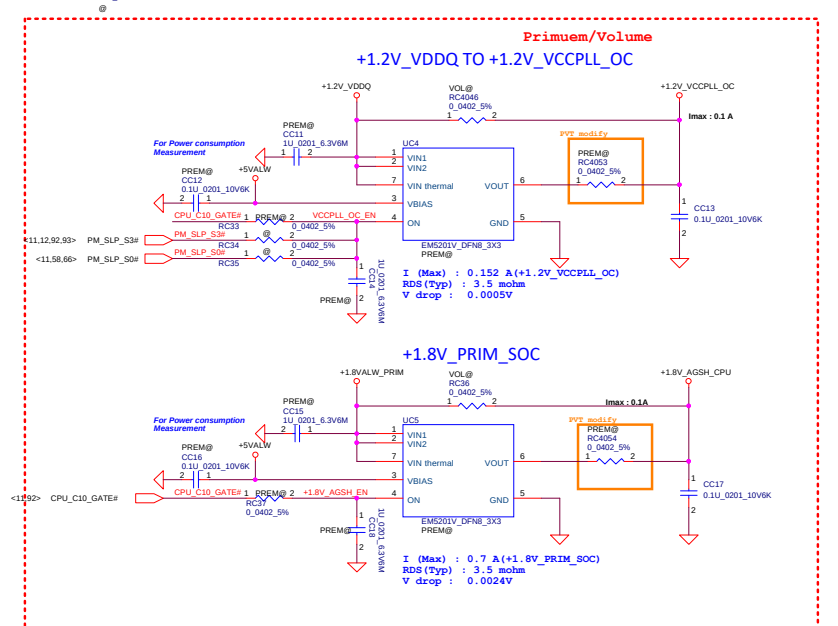
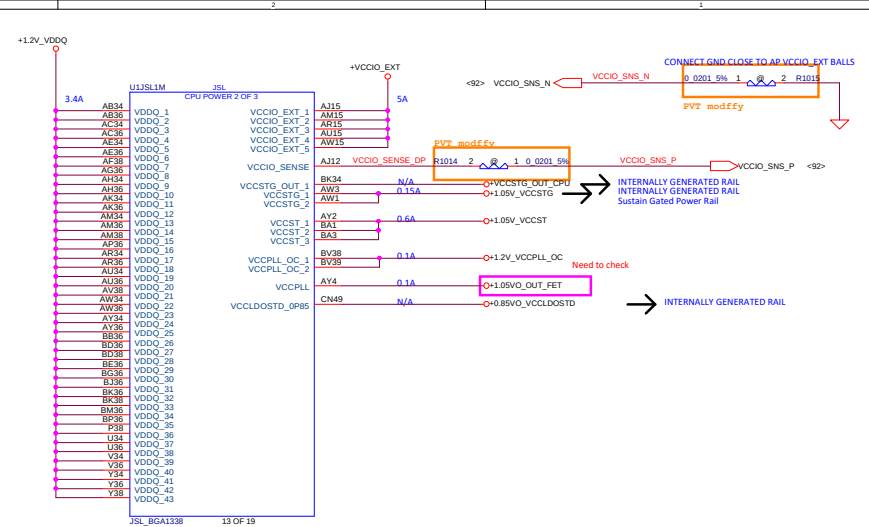






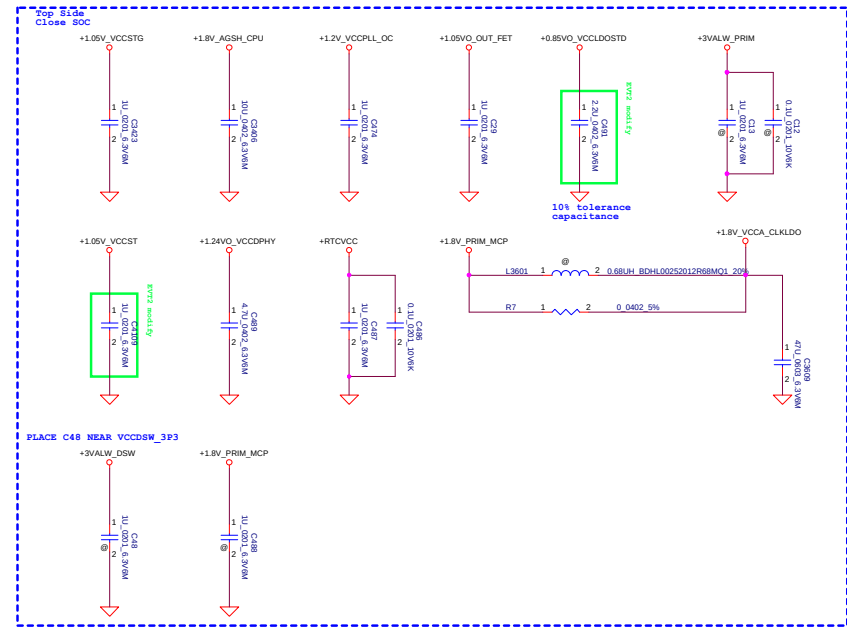


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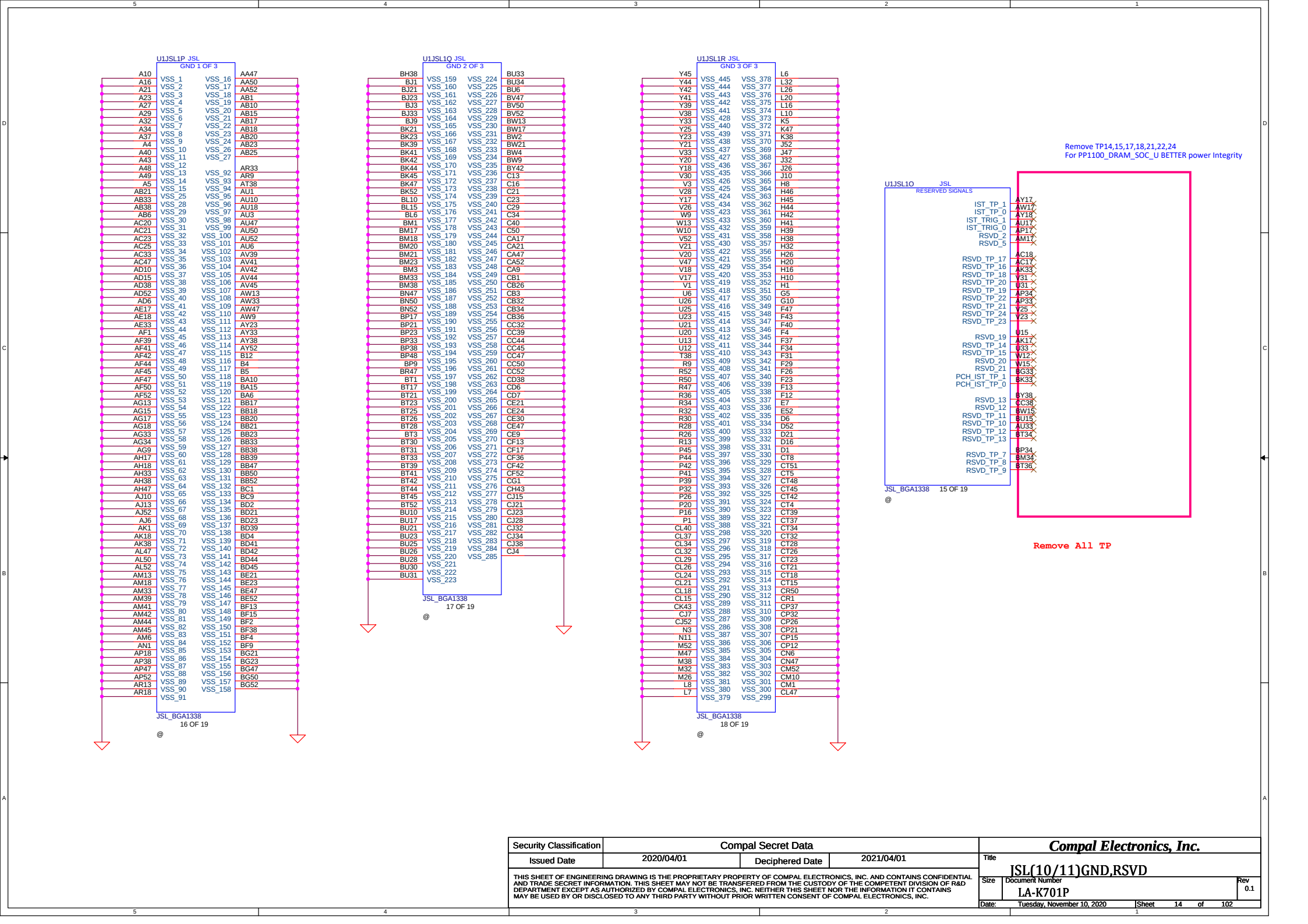


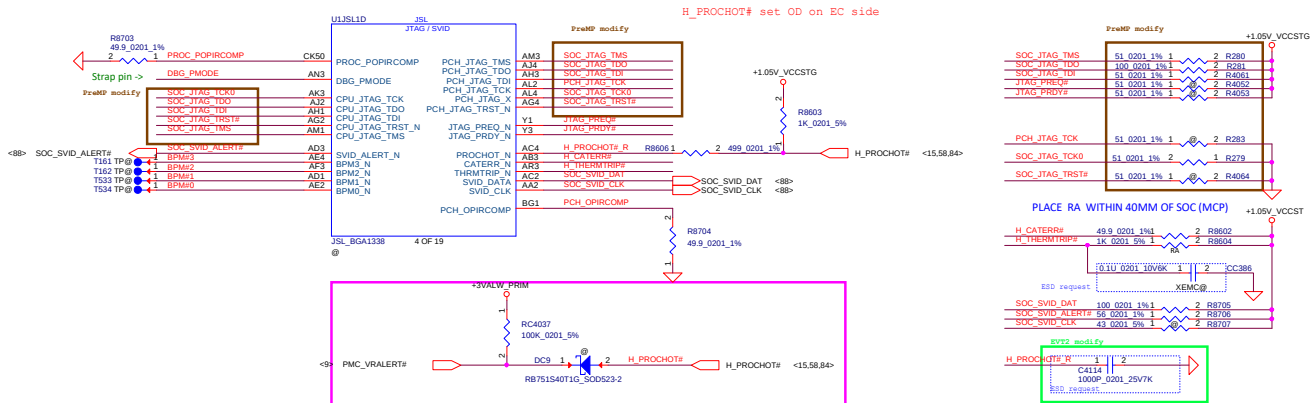
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Decoupling Requirements for VDDQ			
Domain	Primary Side Cap	Secondary Side Cap	Placement Guideline
VDDQ	3 x 0603_22uF	2 x 0201_0.1uF 2 x 0402_4.7uF 2 x 0402_10uF  <u>Place holders:</u> 2 x 0201 2 x 0402 1 x 0402	<u>Secondary Side Cap:</u> Place the secondary caps on the bottom power plane and equally distribute, with the highest cap values closer to the VR. Also place the caps beside or as close as possible to the PTHs that connects to the VDDQ BGAs.



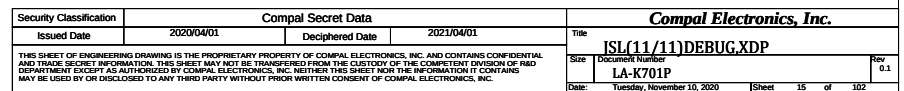
Domain	Primary Side Cap	Secondary Side Cap	Placement Guideline
VCCIO_EXT	12 x 0402_10uF 4 x 0603_22uF	4 x 0402_10uF	<p>Primary Side Place primary caps on the top power plane such that the caps also of distance &lt; 8mm from the package edge. Punch as many PTHs as possible connecting the top side and bottom side power planes, and place the PTHs beside the primary caps' pads to optimise the loop-inductance between caps to the BGAs. Punching too many PTHs may break any power plane and GND plane underneath. To avoid breaking the planes, punch at least 1 PTHs for every 2 cap pads within &lt; 1mm radius.</p> <p>Back Side: Place underneath specific power rail's BGAs. If not doable, place as close as possible.</p>





CFG	Description	Termination	Resistor
CFG0	CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall.	Pull Up to VCCIO_EXT	1K Ohm
CFG1,8,9,10,12,13	RSVD	Pull Up to VCCIO_EXT	1K Ohm
CFG2,3,5,6,7,11,14,15	RSVD	No termination	N/A
CFG4	CFG[4]: eDP enable: — 1 = Disabled. — 0 = Enabled.	Pull Down	1K Ohm

**Note:**  
Refer [Platform Debug and Test Architecture](#) on page 522 for debug connectivity guidelines.





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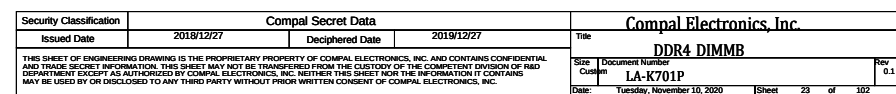
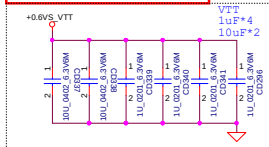


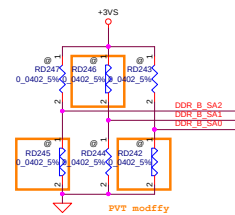
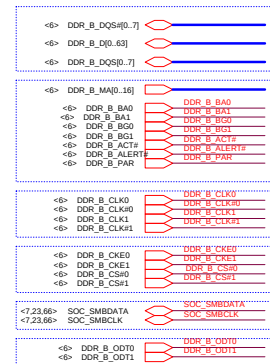
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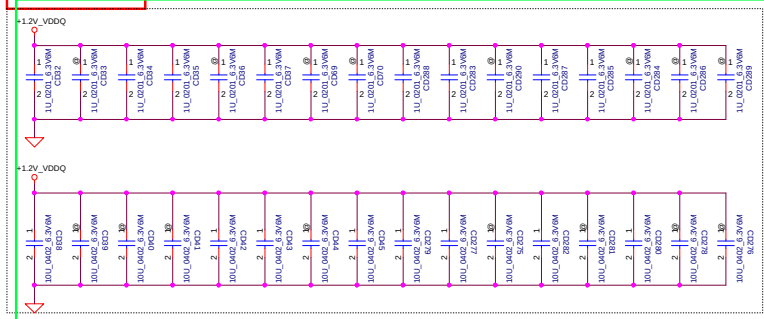
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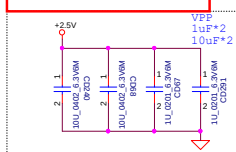




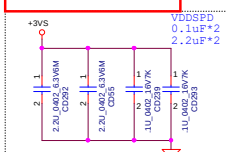
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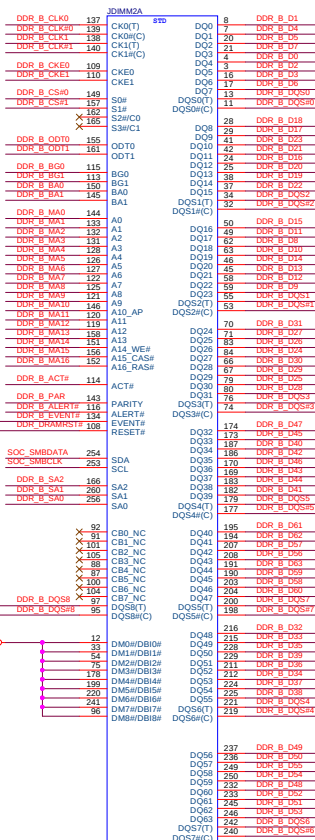
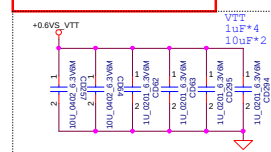
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Layout Note:  
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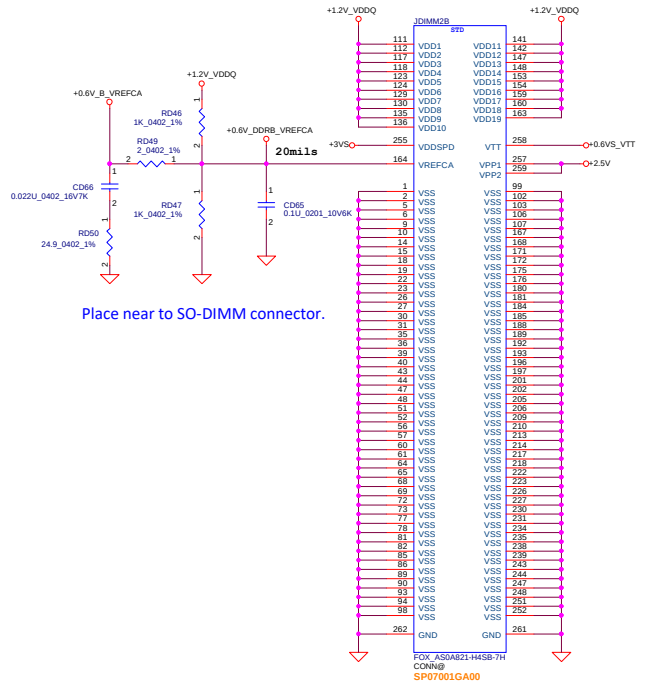


Layout Note:  
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FOX A50A821-H5B-7H  
CON#B  
SP07001GA00  
Compatible with SP07001HW00

Standard Type  
2-3A to 1 DIMMs/channel



Non Interleaved Memory

Refer for DDR4 SO-DIMM Decoupling Caps  
613095\_JSL\_R00\_Rev1p0

Table 21. DDR4 Memory Power Plane Decoupling (Config-1: 1DPC, 2 SODIMMs)

Power Domain	Qty x $\mu$ F (size)	Decoupling Location
VDDQ/VDD	16x 1uF (0402)	4 caps near each side of DIMM connector close to VDD pins
	16x 10uF (0603)	4 caps near each side of DIMM connector close to VDD pins
	1x 330uF (7343)	Placeholder
VPP	2x 1uF (0402)	DIMM Pin side, 1 cap per DIMM
	2x 10uF (0603)	DIMM Pin side, 1 cap per DIMM
VTT	4x 1uF (0402)	Placed on VTT plane close to DIMM
	2x 10uF (0603)	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder
VDDSPD	2x 0.1uF (0402)	1 cap per DIMM. Place close to DIMM
	2x 2.2uF (0402)	1 cap per DIMM. Place close to DIMM



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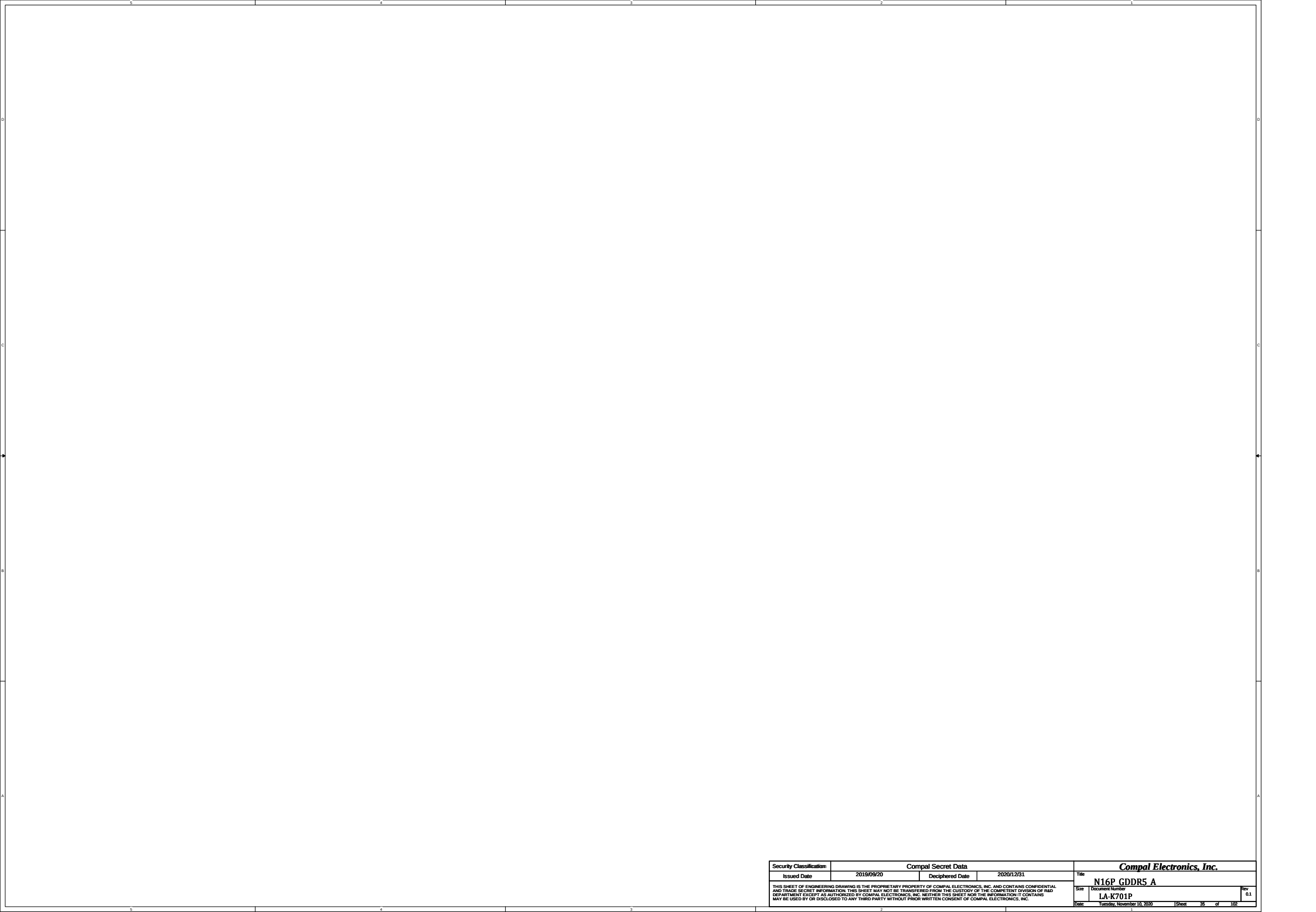
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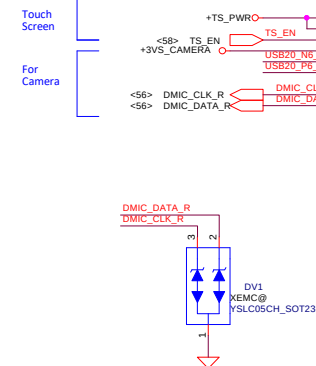
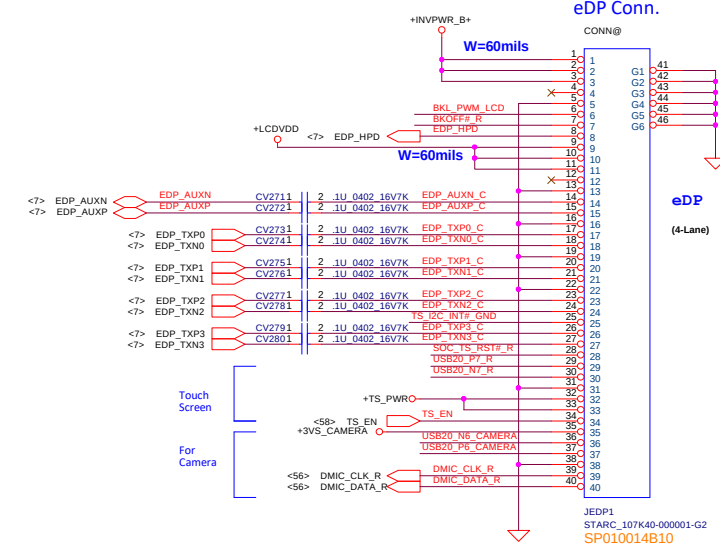
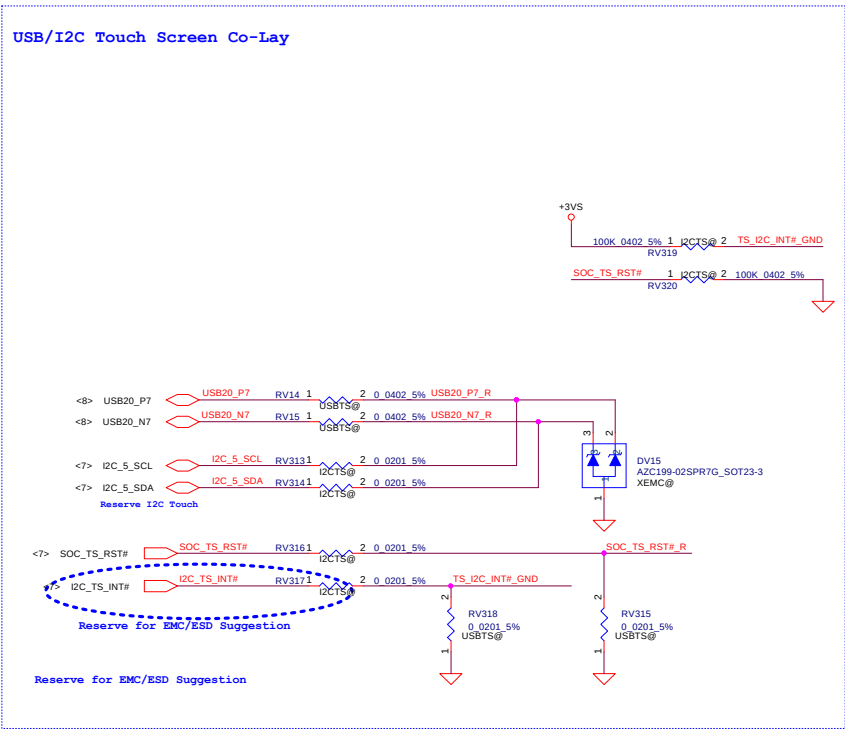
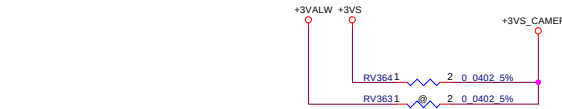
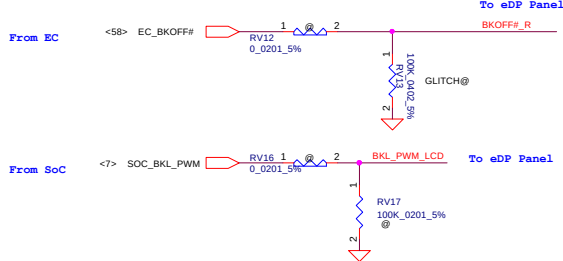
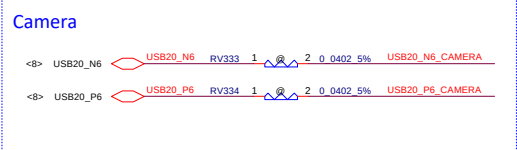
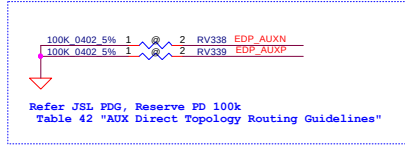
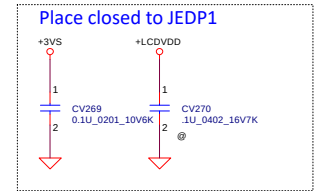
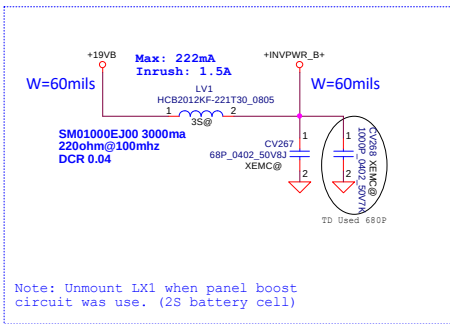
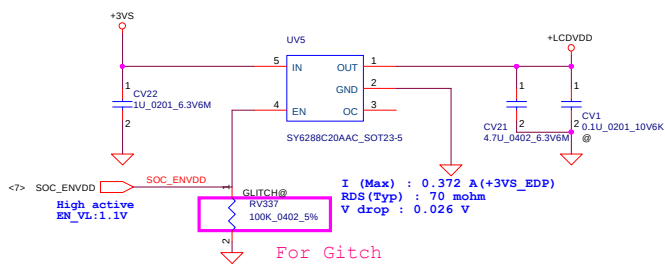
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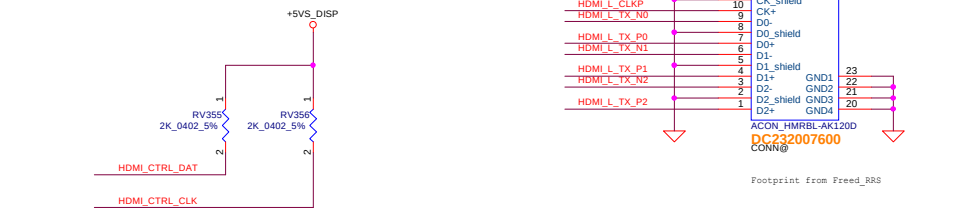
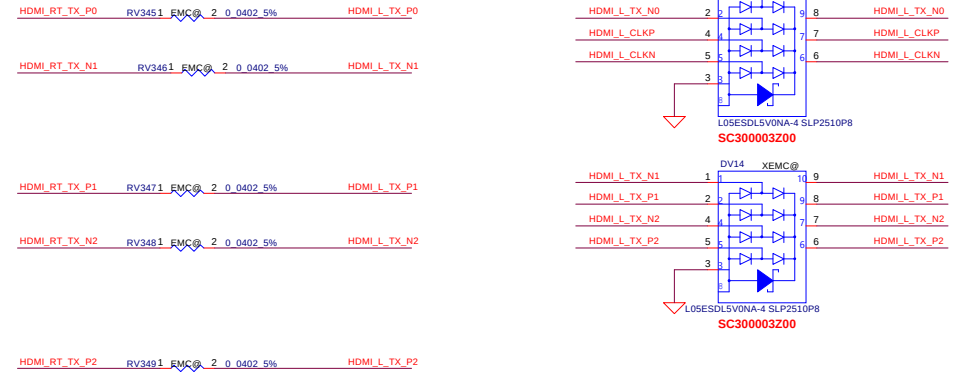
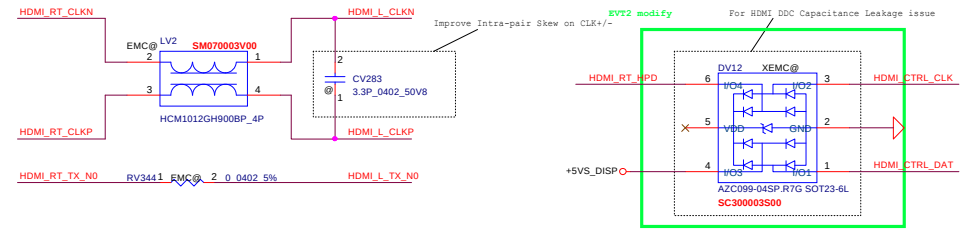
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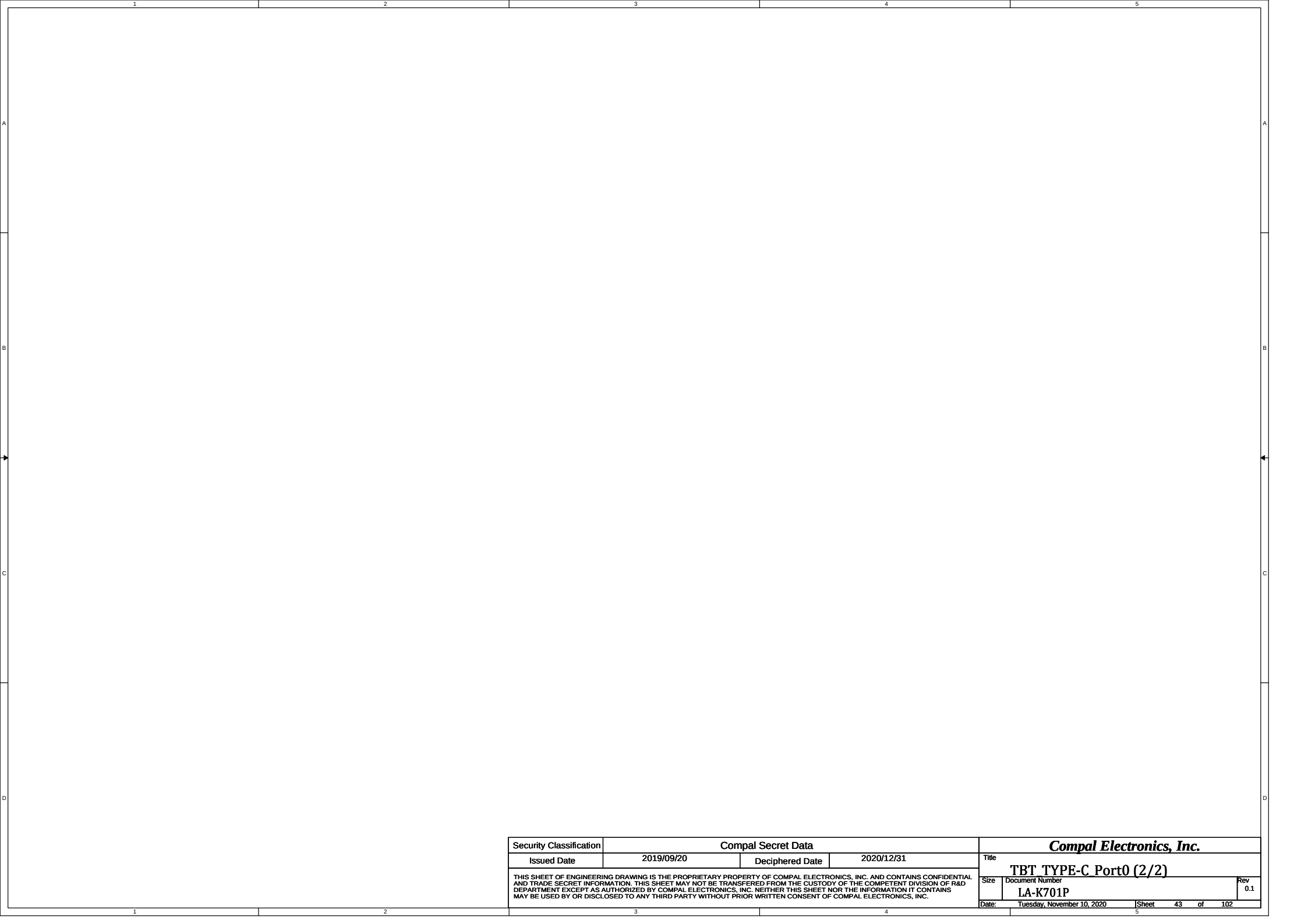


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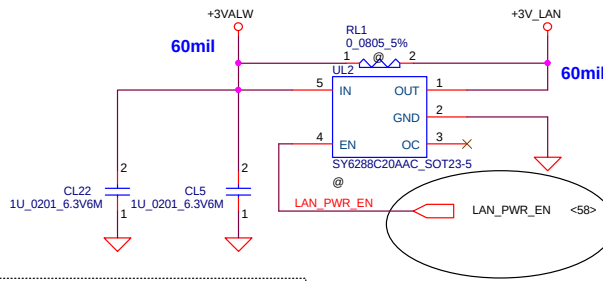




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				Document Number	
				LA-K701P	
Date: Tuesday, November 10, 2020				Sheet	50 of 102

# LAN-RTL8111H



W=60mil

IDC=1200mA

+REGOUT

RL10 1 2 0.0603 5%

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0.1u 0201\_10V6K

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W=60mil

300mA

+LAN\_VDD

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+3V\_LAN

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From EC

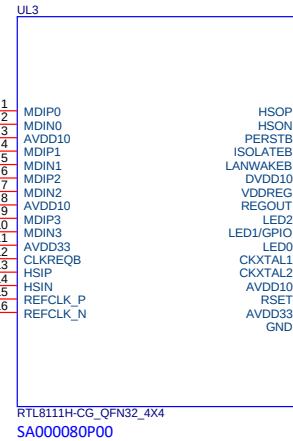
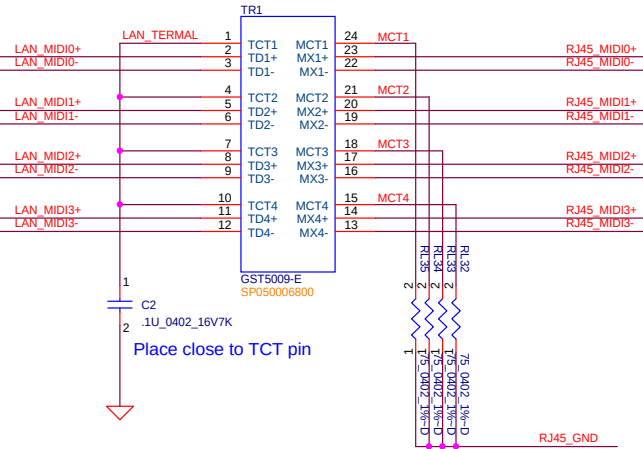
High active.  
EN threshold voltage min:1.2V typ:1.6V max:2.0V  
Current limit threshold 1.5~2.8A

reserve EC\_PME# pull high 100K to +3VALW\_EC

PCIe X1  
PU at PCH side PCIe CLK

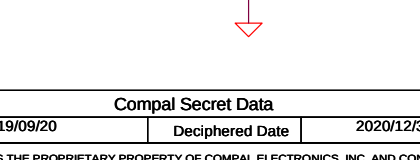
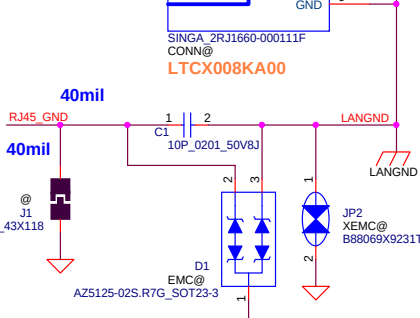
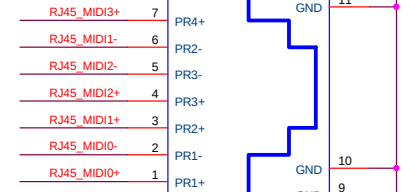
CLKREQ\_PCIE#2  
0.1u 0201\_10V6K 1 2 CL20  
0.1u 0201\_10V6K 1 2 CL21  
CLK\_PCIE\_P2  
CLK\_PCIE\_N2

LAN\_MIDI0+  
LAN\_MIDI0-  
+LAN\_VDD  
LAN\_MIDI1+  
LAN\_MIDI1-  
LAN\_MIDI2+  
LAN\_MIDI2-  
+LAN\_VDD  
VDDREG  
+LAN\_VDD  
LAN\_MIDI3+  
LAN\_MIDI3-  
+3V\_LAN  
MDIP0  
MDIN0  
AVDD10  
MDIP1  
MDIN1  
MDIP2  
MDIN2  
AVDD10  
MDIP3  
MDIN3  
AVDD33  
CLKREQB  
HSIP  
HSIN  
REFCLK\_P  
REFCLK\_N



HSOP  
HSIN  
PERSTB  
ISOLATEB  
LANWAKEB  
VDD10  
VDD2  
VDDREG  
REGOUT  
LED2  
LED1/GPIO  
LED0  
CKXTAL1  
CKXTAL2  
AVDD10  
RSET  
AVDD33  
GND

17 PCIE\_CRX\_C\_DTX\_P6  
18 PCIE\_CRX\_C\_DTX\_N6  
19 PLT\_RST\_R#  
20 ISOLATEB  
21 EC\_PME#  
22 +LAN\_VDD  
23 +3V\_LAN  
24 +REGOUT  
25  
26 GPO  
27 XTLO  
28 XTLO\_R  
29 +LAN\_VDD  
30 +LAN\_VDD  
31 LAN\_RST  
32 +3V\_LAN  
33



PCIe X1  
(link to PCIe Port 9)

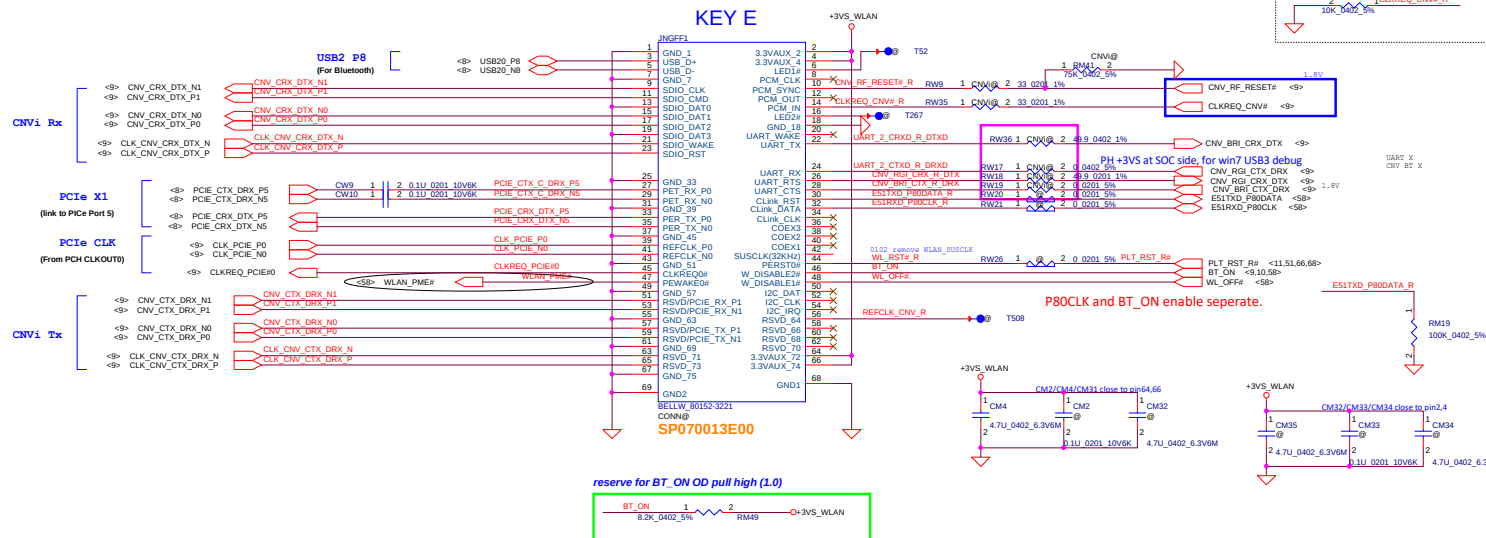
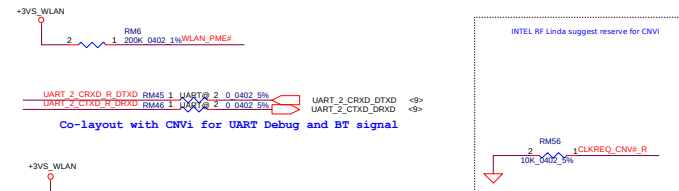
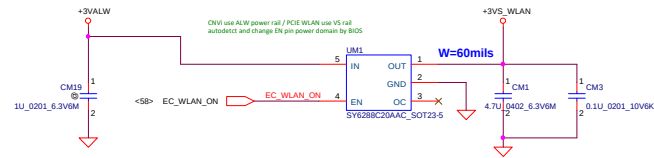
PCIE\_CRX\_C\_DTX\_P6  
PCIE\_CRX\_C\_DTX\_N6  
PCIE\_CRX\_DTX\_P6  
PCIE\_CRX\_DTX\_N6

17 PCIE\_CRX\_C\_DTX\_P6  
18 PCIE\_CRX\_C\_DTX\_N6  
19 PLT\_RST\_R#  
20 ISOLATEB  
21 EC\_PME#  
22 +LAN\_VDD  
23 +3V\_LAN  
24 +REGOUT  
25  
26 GPO  
27 XTLO  
28 XTLO\_R  
29 +LAN\_VDD  
30 +LAN\_VDD  
31 LAN\_RST  
32 +3V\_LAN  
33

17 PCIE\_CRX\_C\_DTX\_P6  
18 PCIE\_CRX\_C\_DTX\_N6  
19 PLT\_RST\_R#  
20 ISOLATEB  
21 EC\_PME#  
22 +LAN\_VDD  
23 +3V\_LAN  
24 +REGOUT  
25  
26 GPO  
27 XTLO  
28 XTLO\_R  
29 +LAN\_VDD  
30 +LAN\_VDD  
31 LAN\_RST  
32 +3V\_LAN  
33

17 PCIE\_CRX\_C\_DTX\_P6  
18 PCIE\_CRX\_C\_DTX\_N6  
19 PLT\_RST\_R#  
20 ISOLATEB  
21 EC\_PME#  
22 +LAN\_VDD  
23 +3V\_LAN  
24 +REGOUT  
25  
26 GPO  
27 XTLO  
28 XTLO\_R  
29 +LAN\_VDD  
30 +LAN\_VDD  
31 LAN\_RST  
32 +3V\_LAN  
33

17 PCIE\_CRX\_C\_DTX\_P6  
18 PCIE\_CRX\_C\_DTX\_N6  
19 PLT\_RST\_R#  
20 ISOLATEB  
21 EC\_PME#  
22 +LAN\_VDD  
23 +3V\_LAN  
24 +REGOUT  
25  
26 GPO  
27 XTLO  
28 XTLO\_R  
29 +LAN\_VDD  
30 +LAN\_VDD  
31 LAN\_RST  
32 +3V\_LAN  
33



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				Size	Document Number
				LA-K701P	
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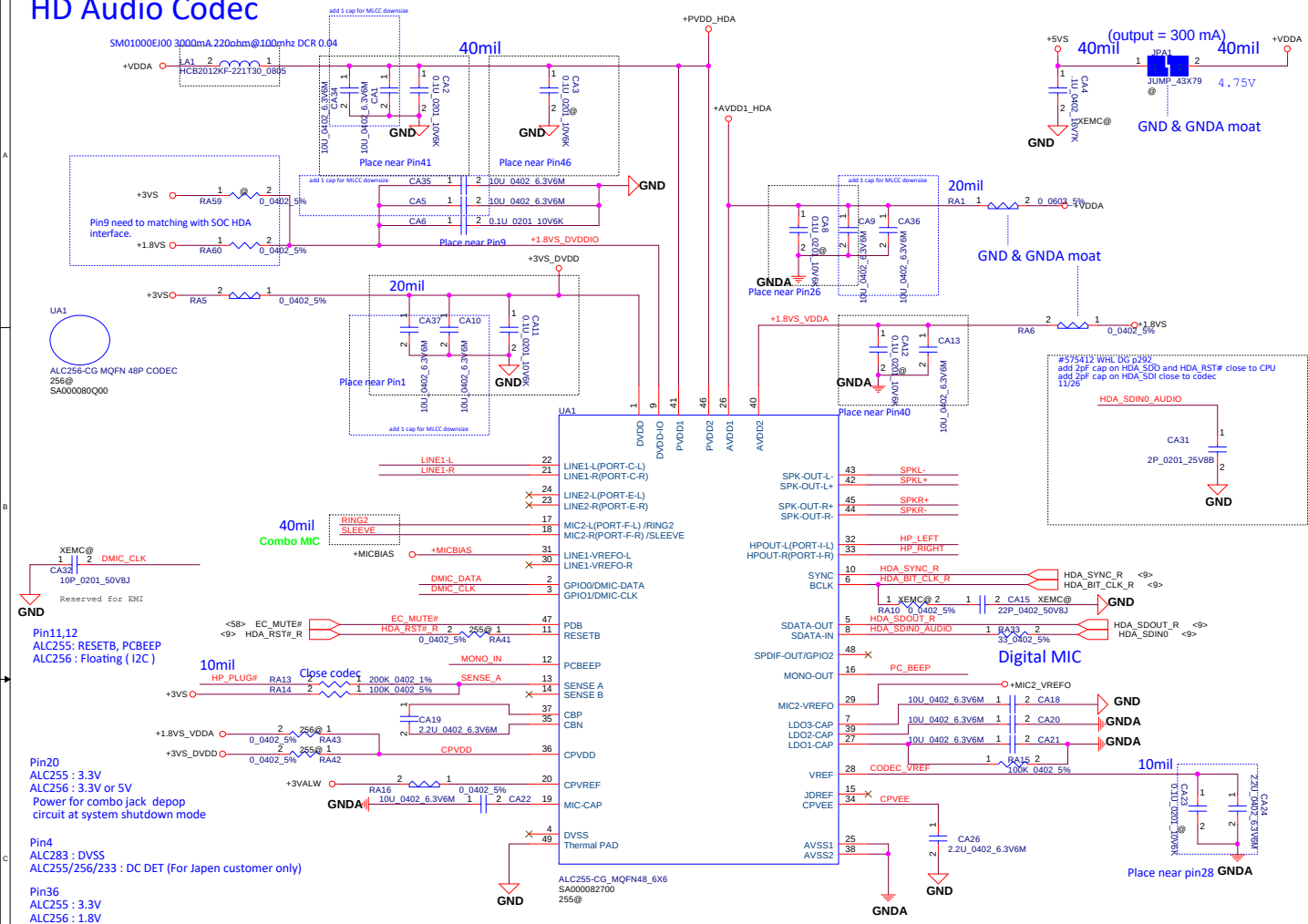


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					LA-K701P
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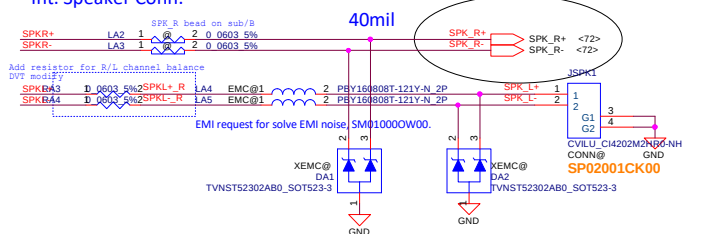


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				Size	Document Number
				LA-K701P	
Date: Tuesday, November 10, 2020		Sheet 55 of 102		Rev 0.1	

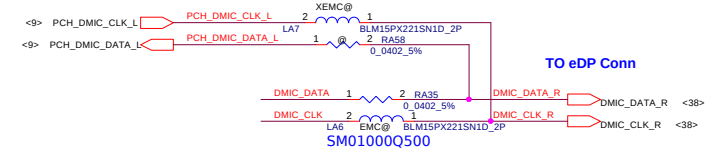
## HD Audio Codec



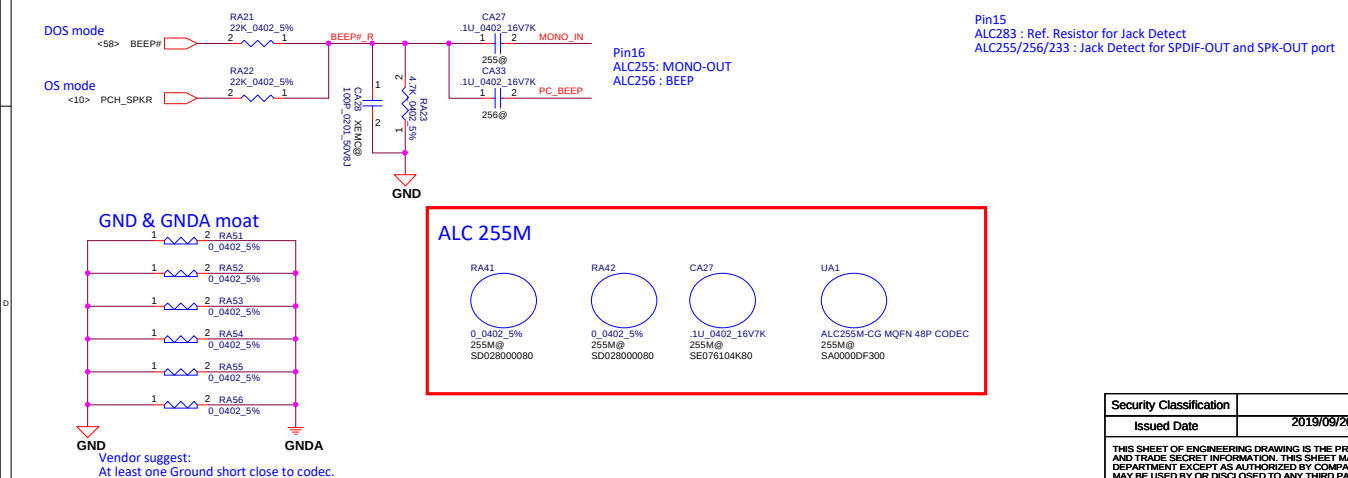
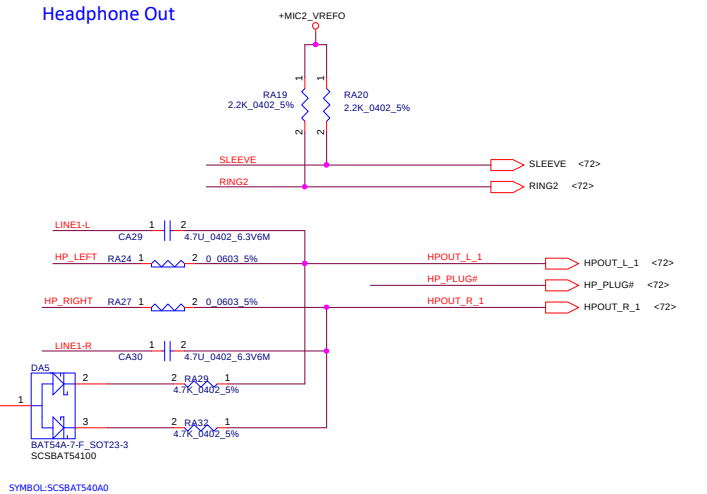
Int. Speaker Conn.



## Digital MIC



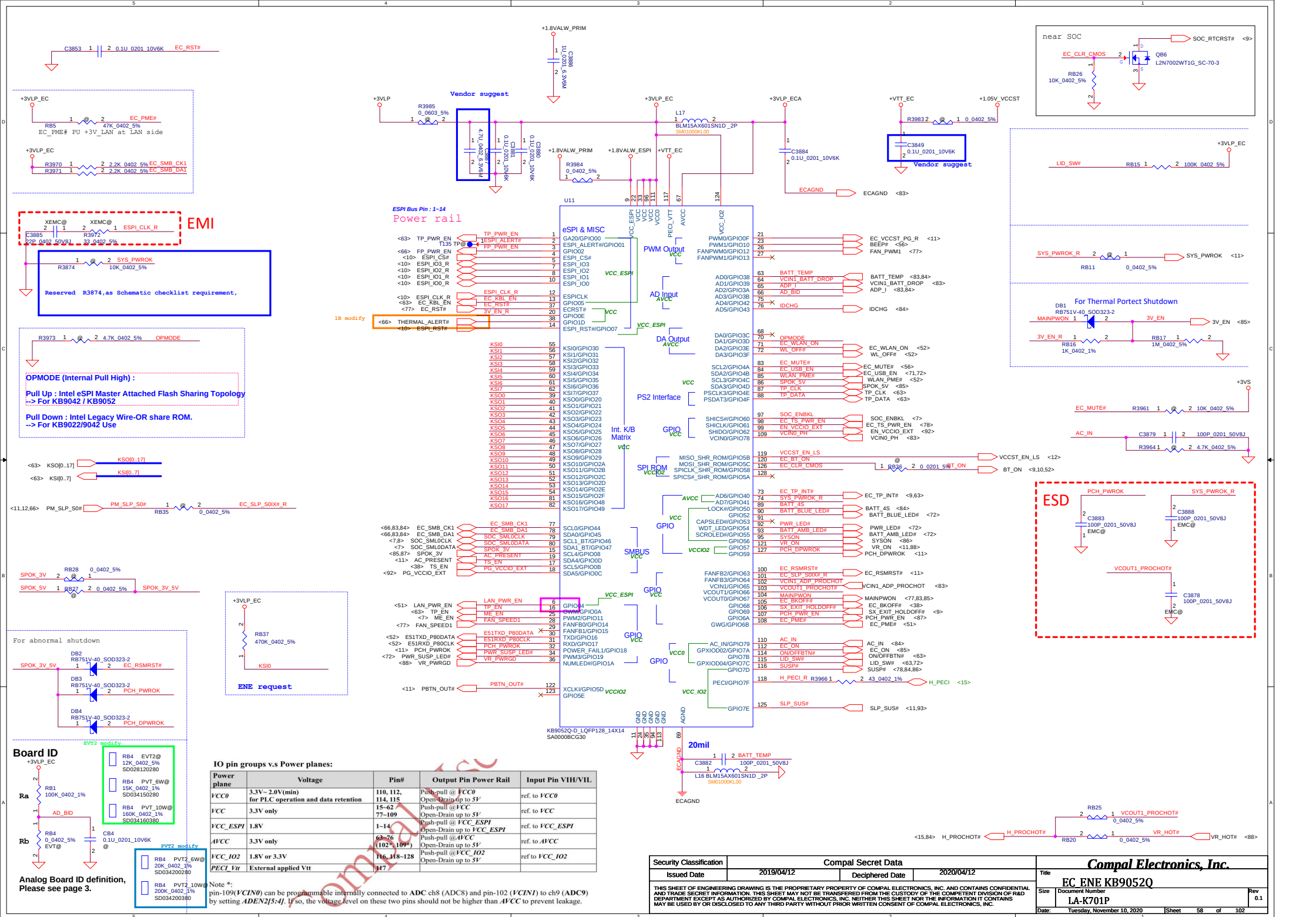
## Headphone Out



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					Size	Document Number	Rev			
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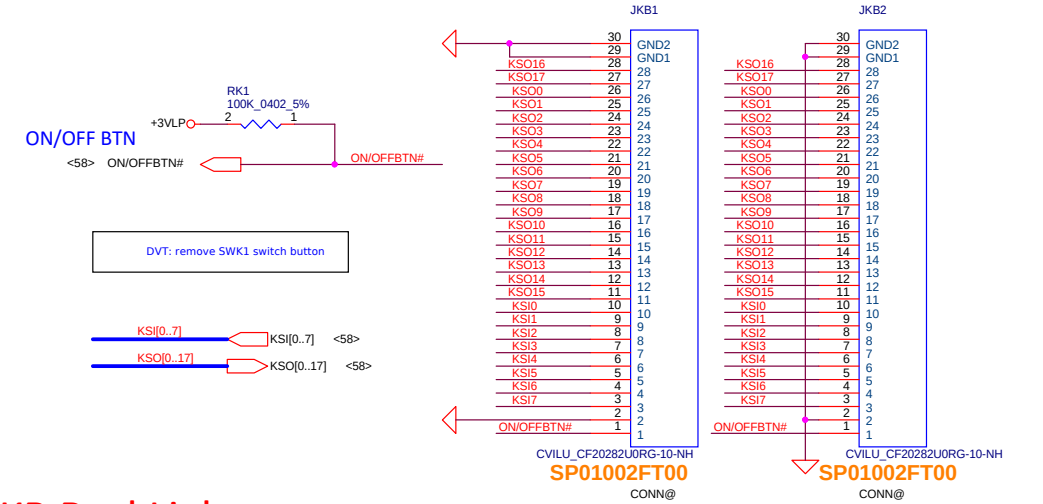


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					LA-K701P
				Date:	Tuesday, November 10, 2020
				Sheet	61 of 102
				Rev	0.1

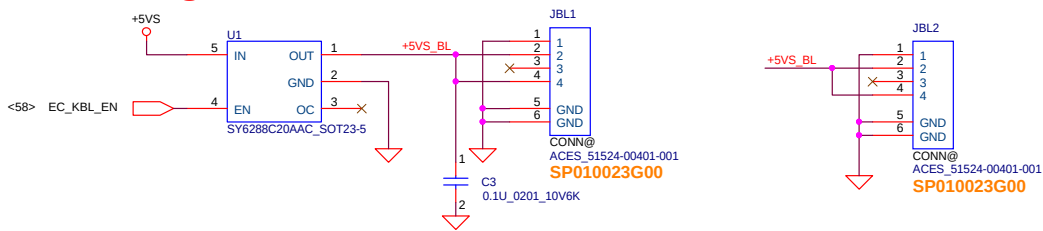


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					LA-K701P
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				Rev	0.1

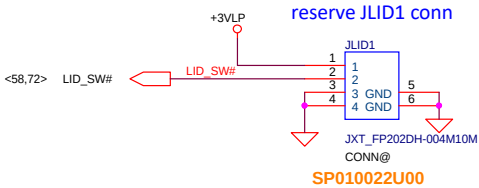
KB Conn.



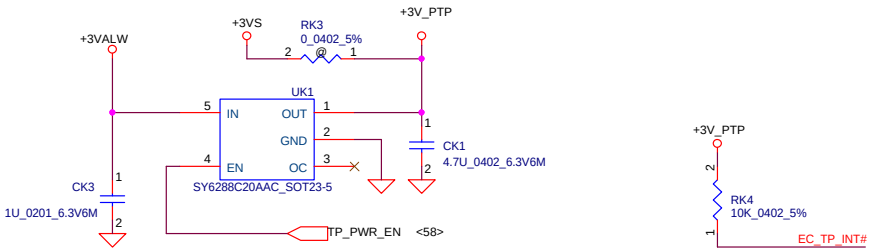
KB BackLight



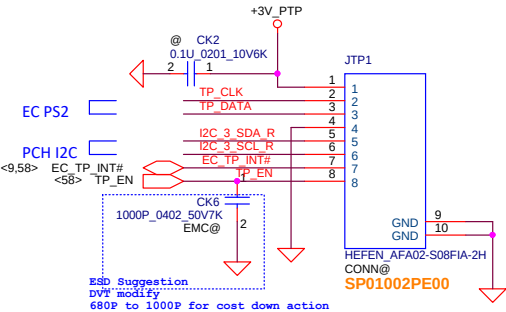
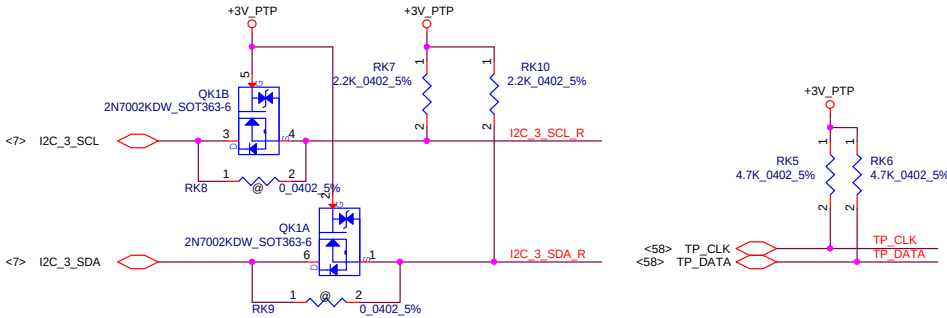
Lid Switch



TP/B Conn.



TP\_PWR\_EN follow SYSON behavior



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				Date: Tuesday, November 10, 2020	Sheet 63 of 102

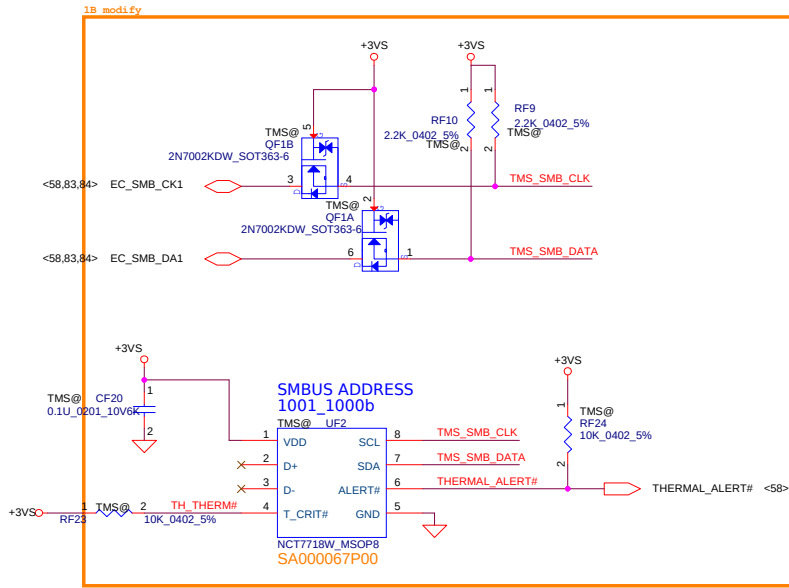


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					LA-K701P
				Date:	Tuesday, November 10, 2020
				Sheet	64 of 102
				Rev	0.1

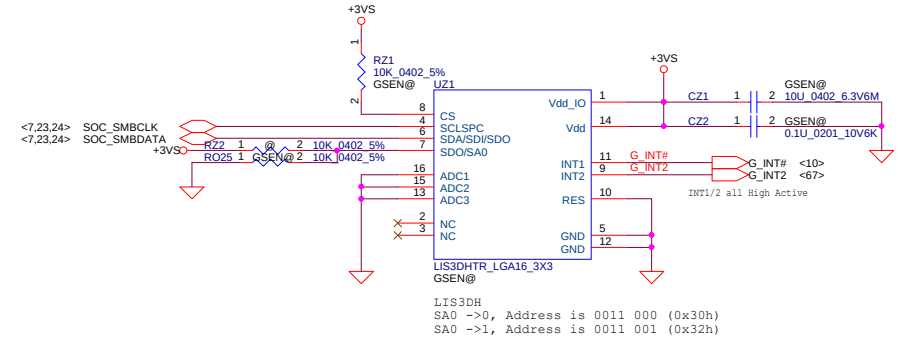


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				Size	Document Number
				LA-K701P	
Date: Tuesday, November 10, 2020		Sheet 65 of 102		Rev 0.1	

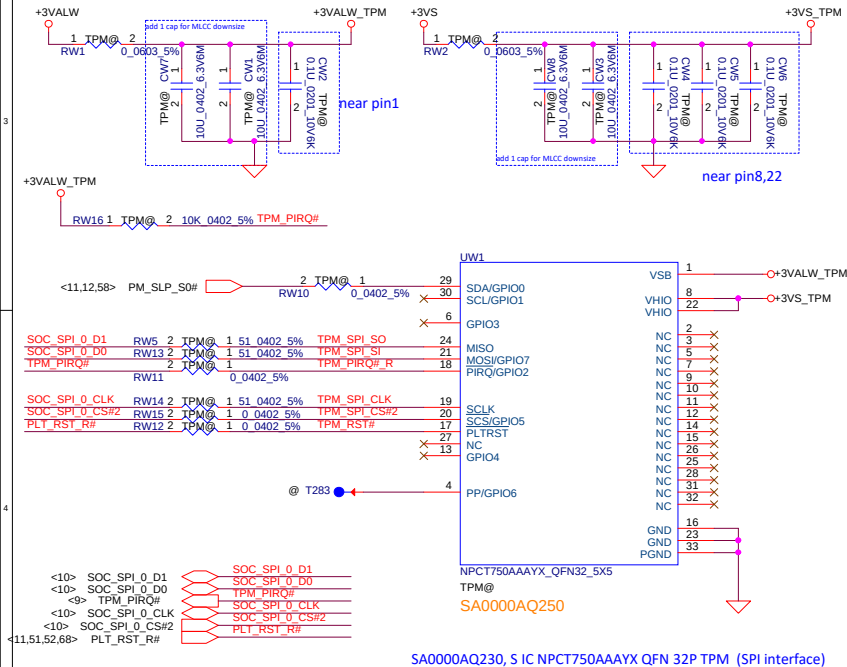
## THERMAL SENSOR



## G-Sensor reserved for BA serial

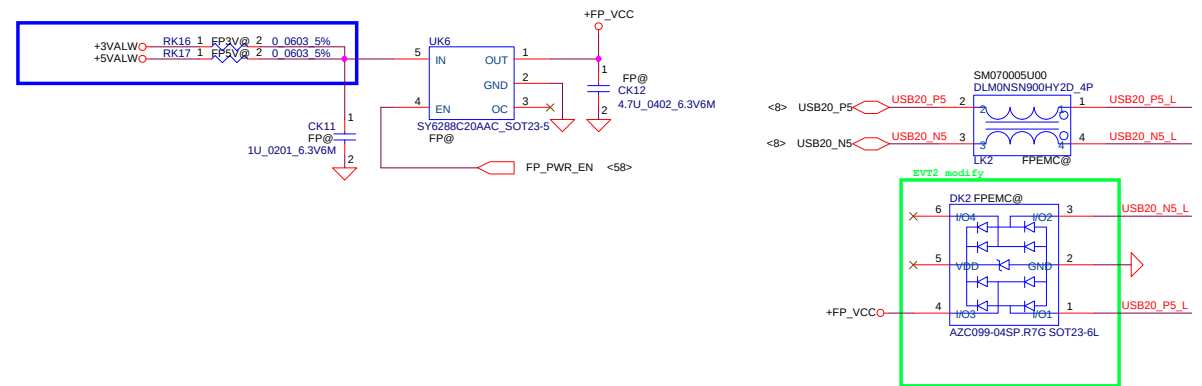


## TPM 2.0



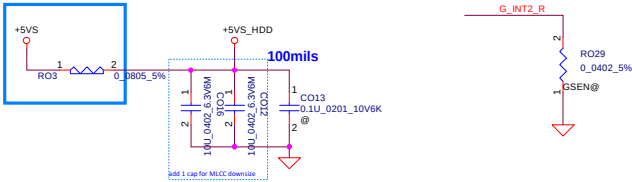
## Finger Print

Power Source Check  
EGIS ETU801 +FP VCC=5V  
ELAN SA464K-2200 +FP VCC=3.3V

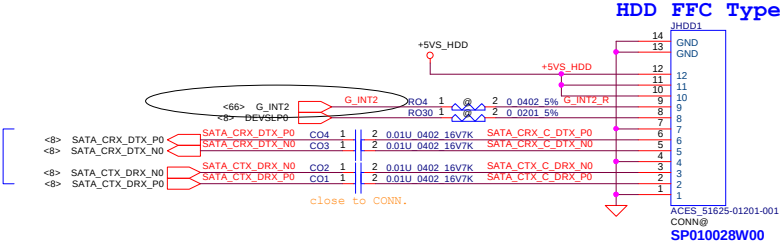


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				Size	Rev
				Custom	0.1
				LA-K701P	
				Date:	Tuesday, November 10, 2020
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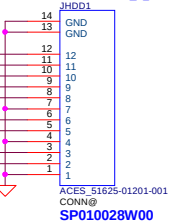
SATA HDD



SATA Port 0

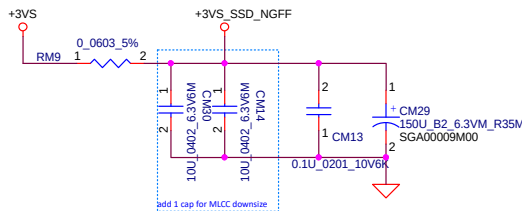


HDD FFC Type

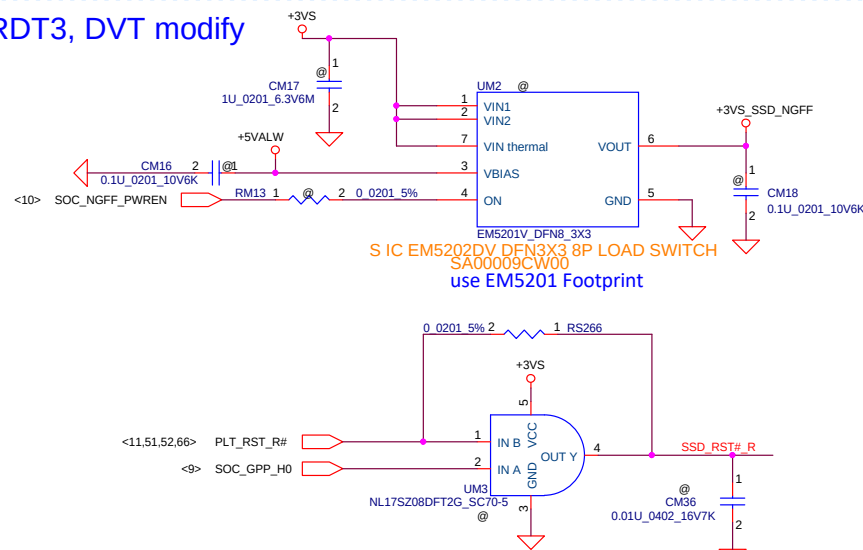


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# mSATA/SSD

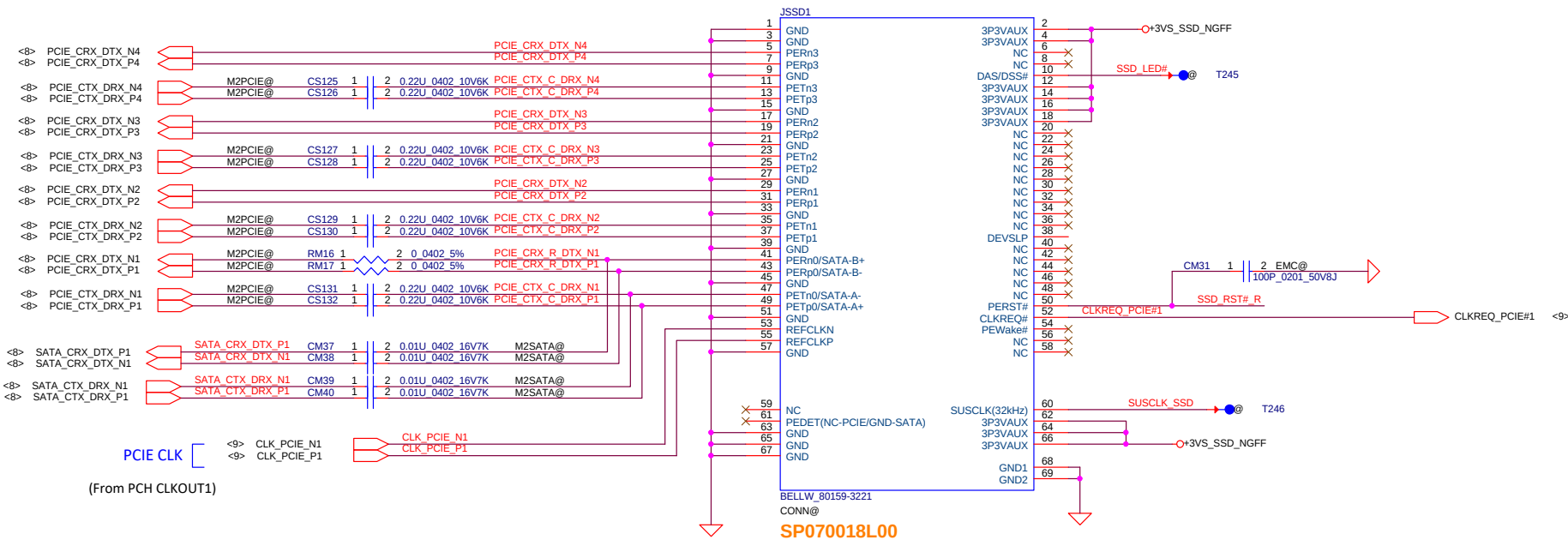


reserve for RDT3, DVT modify



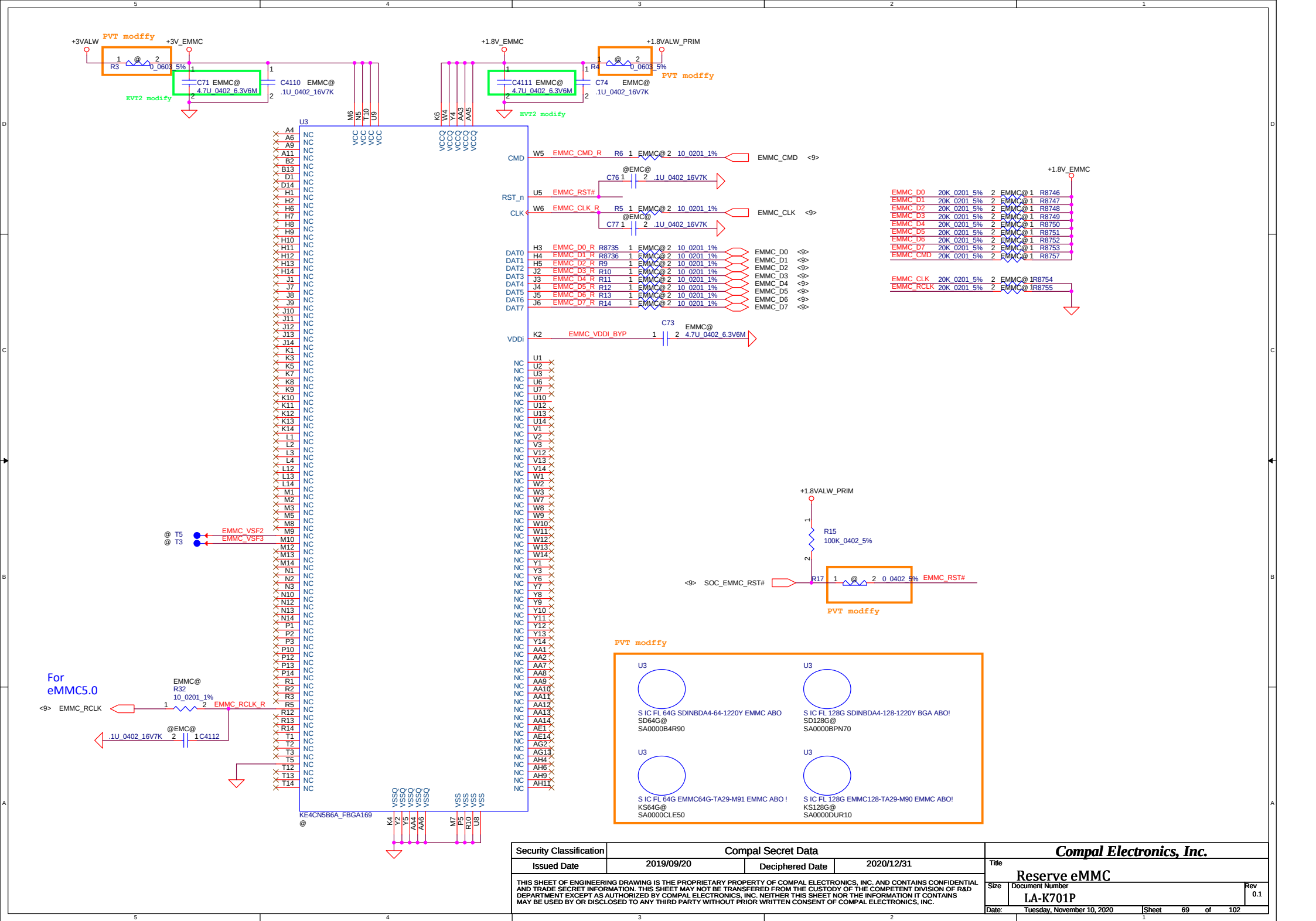
## KEY M

PCIE X4  
(link to PICE Port 1~4)



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Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title	NGFF SSD(KEY M)
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				Date	Tuesday, November 10, 2020
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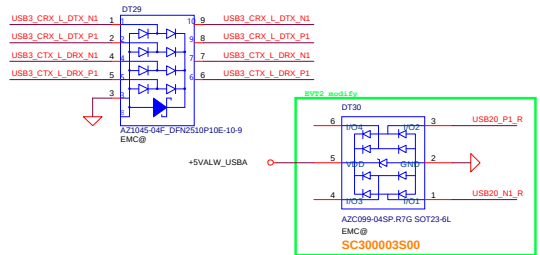
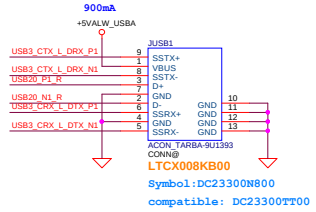
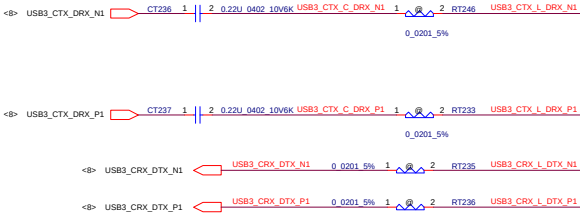
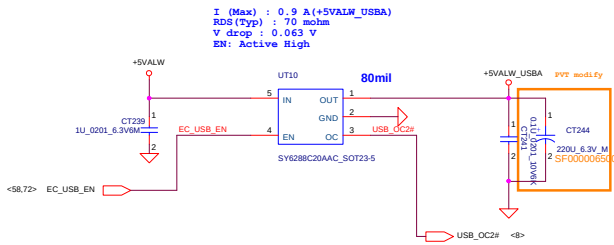




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				Date	Tuesday, November 10, 2020
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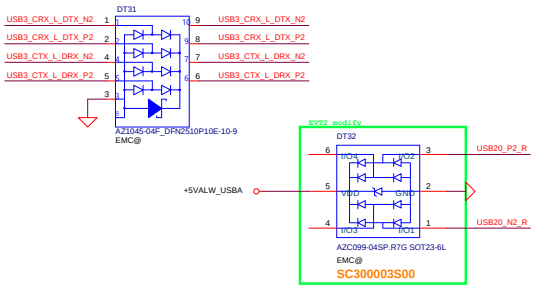
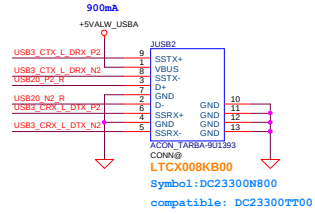
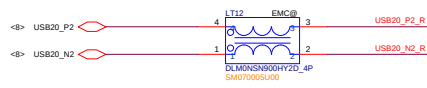
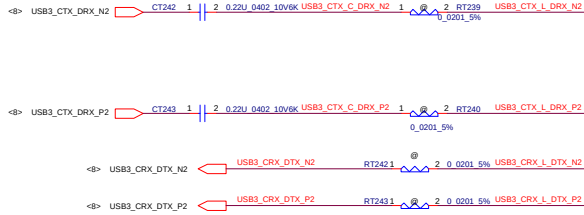
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Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title	
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MB\_USB3.1 Type-A Conn.

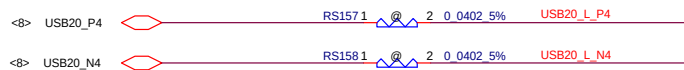


MB\_USB3.1 Type-A Conn.  
(Charge Port)

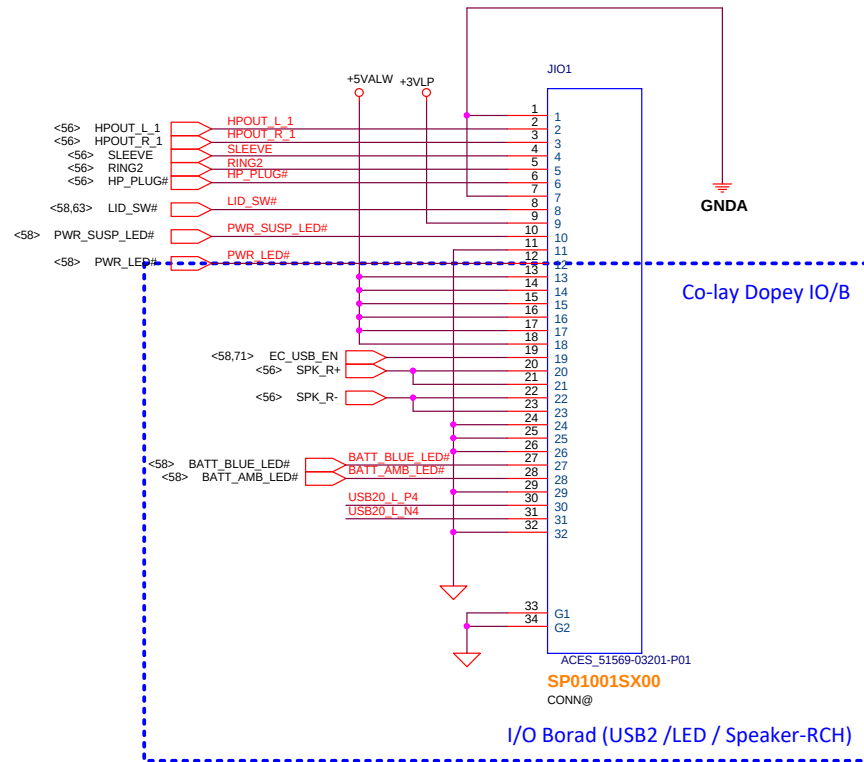
USB Host Charger



# USB2 I/O



Reserved CMC on SUB/B side



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Issued Date	2019/09/20	Deciphered Date	2020/12/31	Reserve USB2/USB3 TYPEA	
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				Size	Document Number
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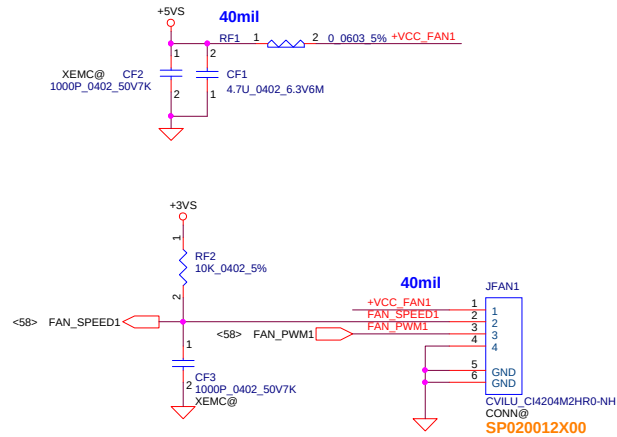
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Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title	
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				Size	Document Number
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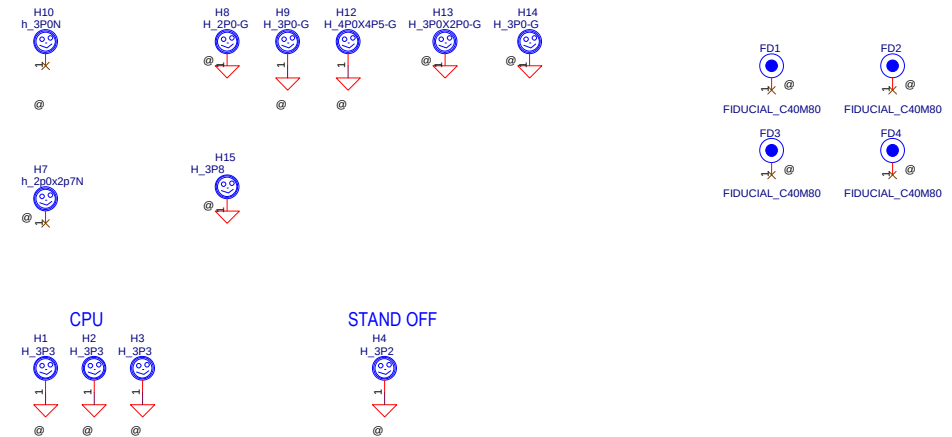
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Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title	
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				Size	Document Number
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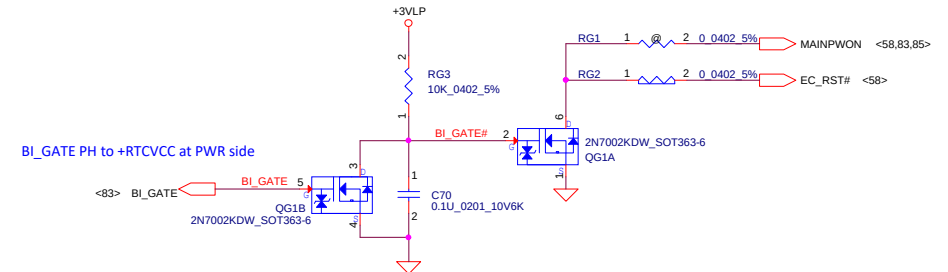
FAN1 Conn



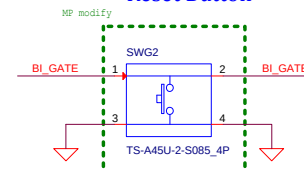
## Screw Hole



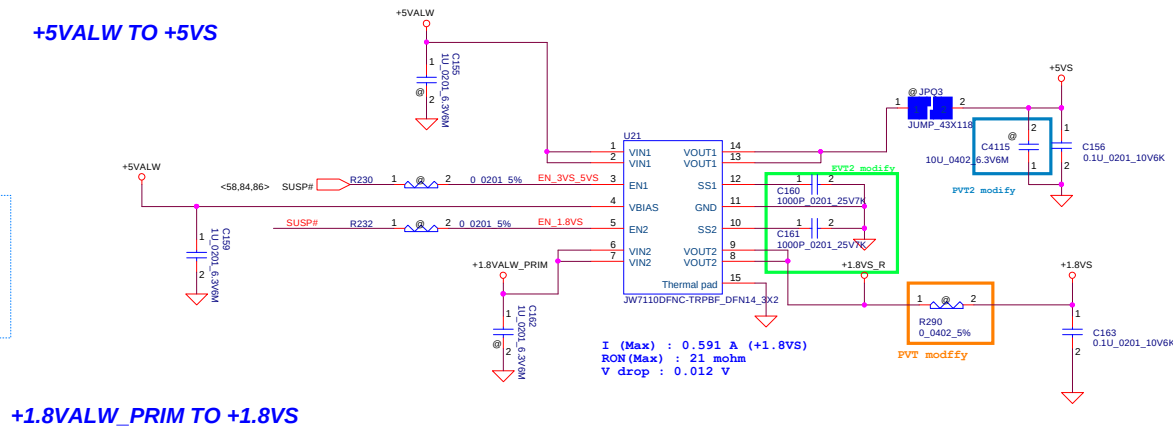
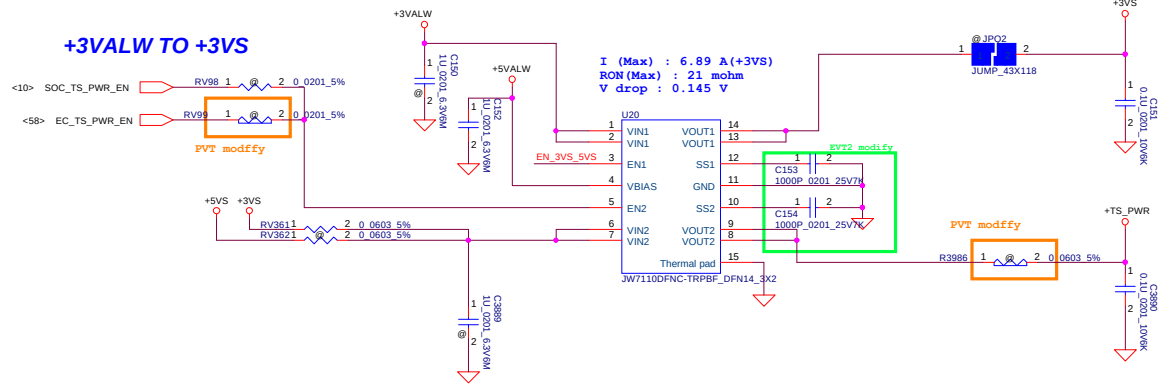
## Reset Circuit



## Reset Button



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Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title		
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**+1.8VALW\_PRIM TO +1.8VS**

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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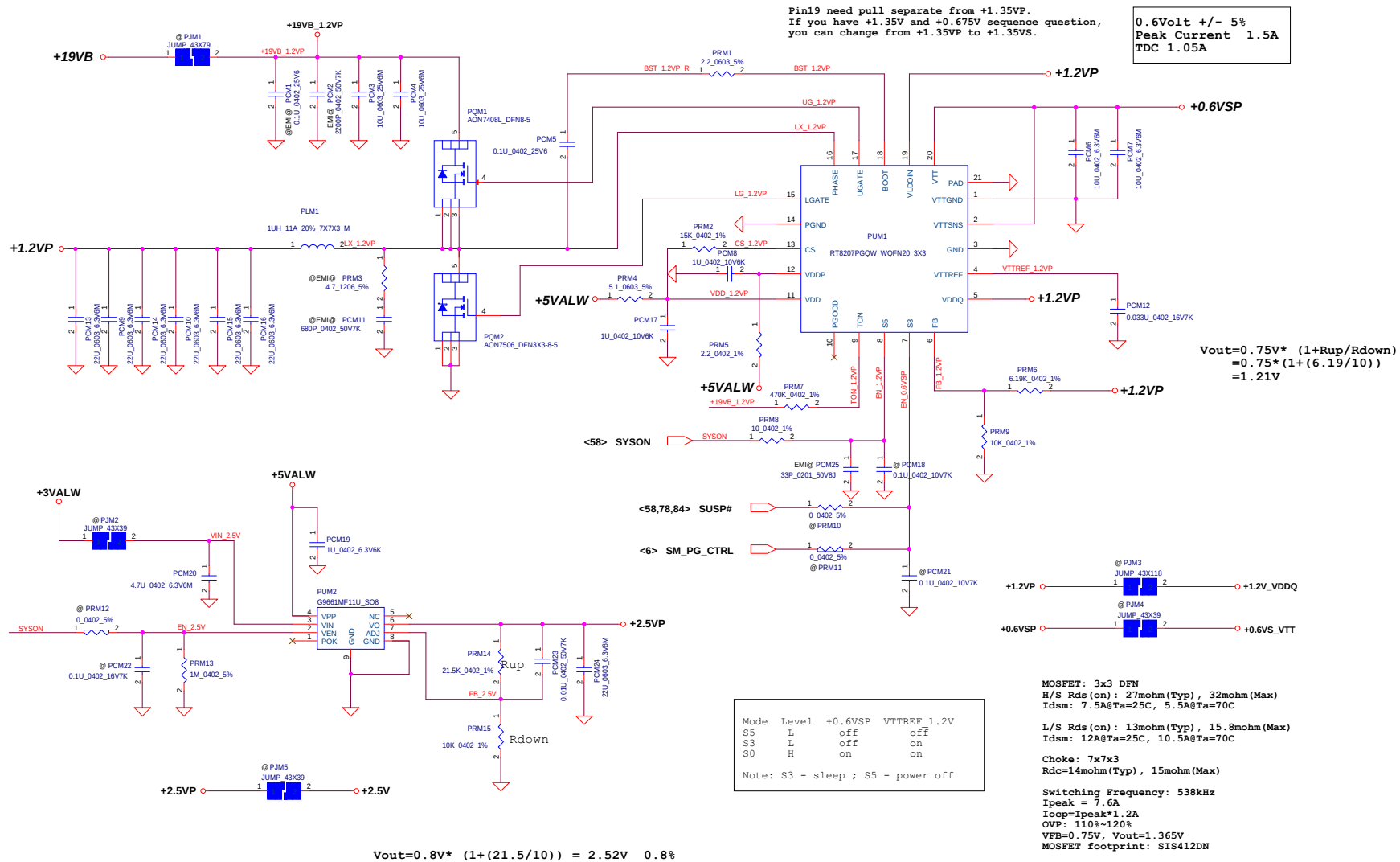


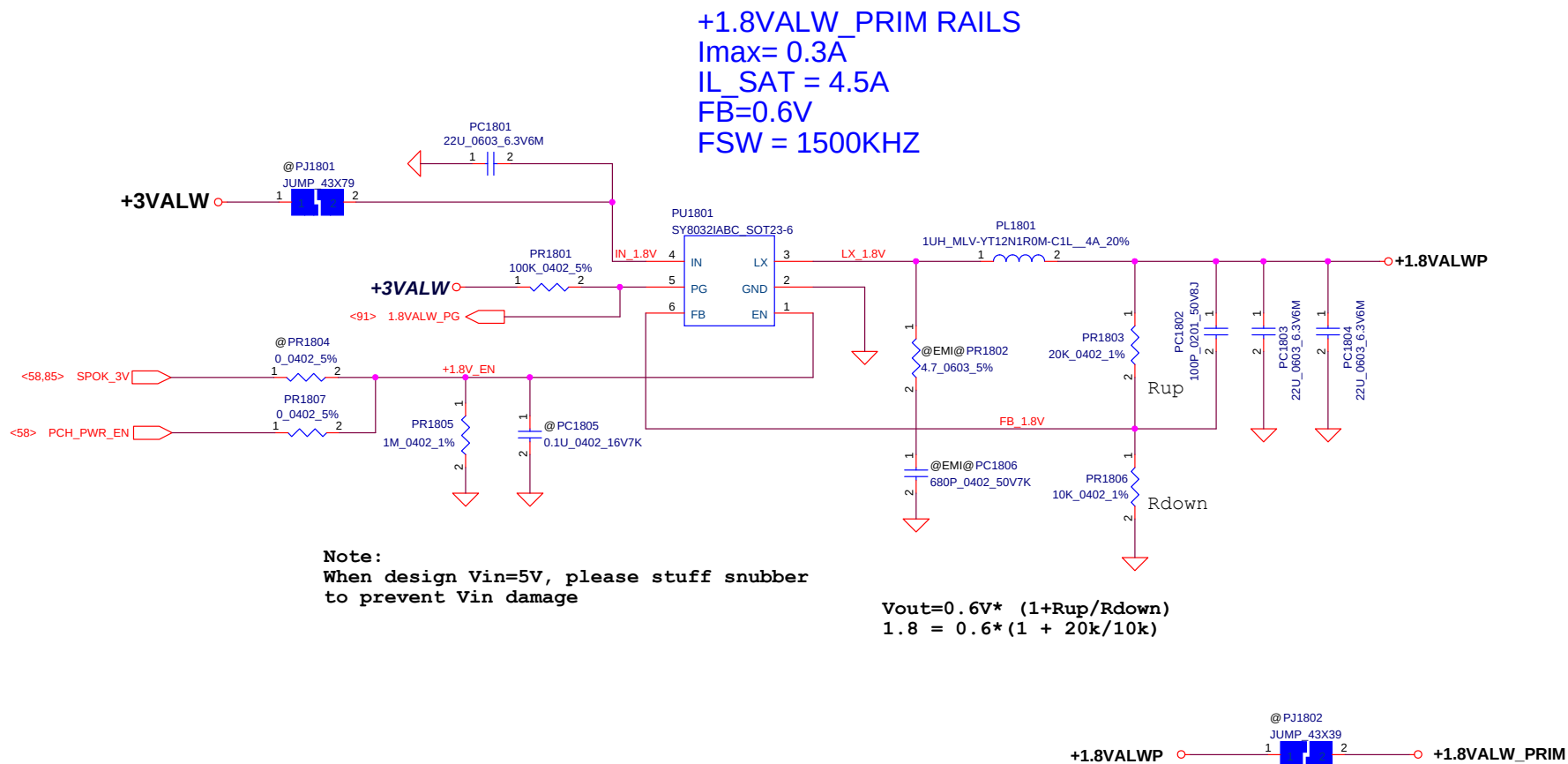










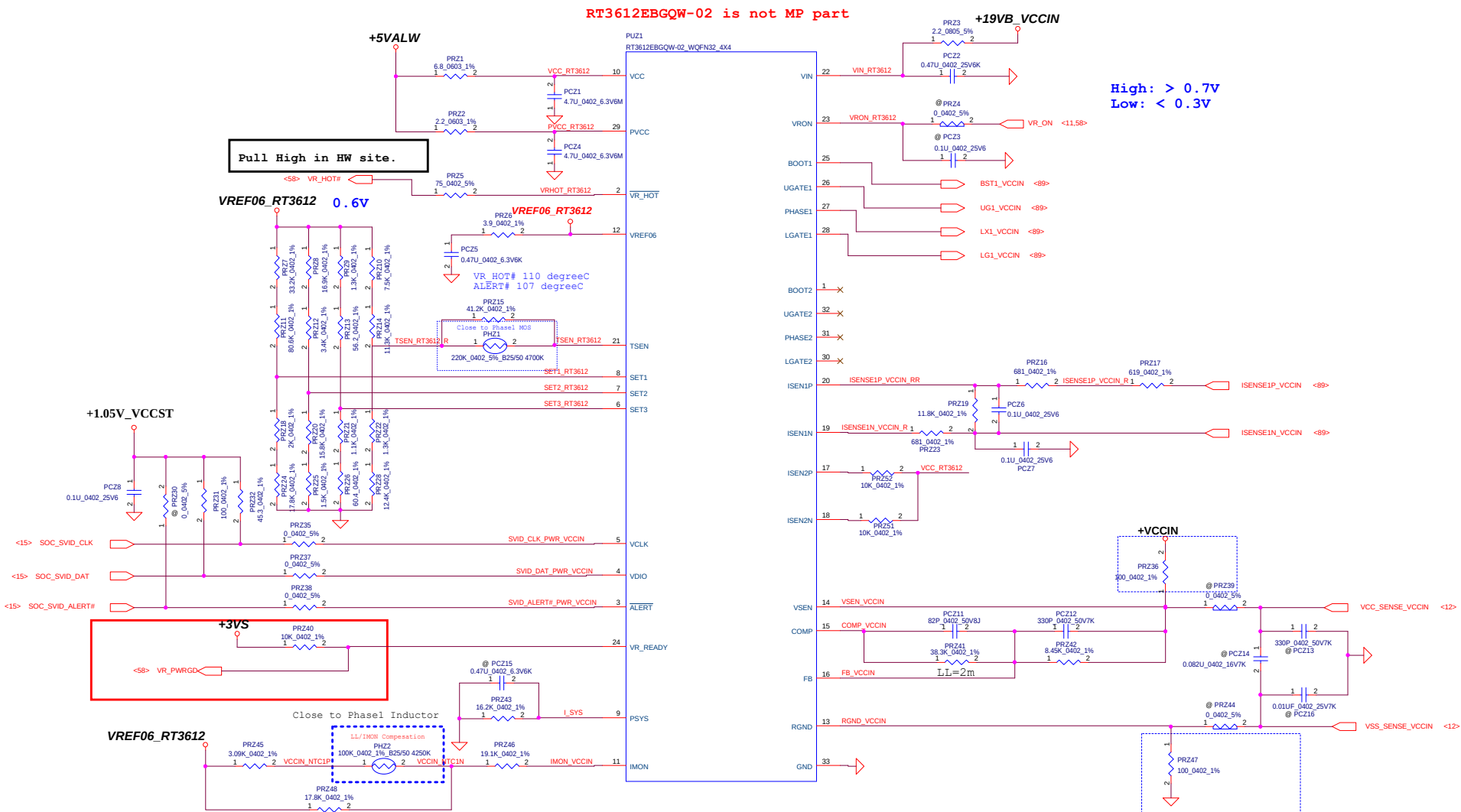


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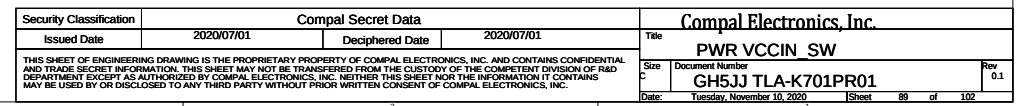
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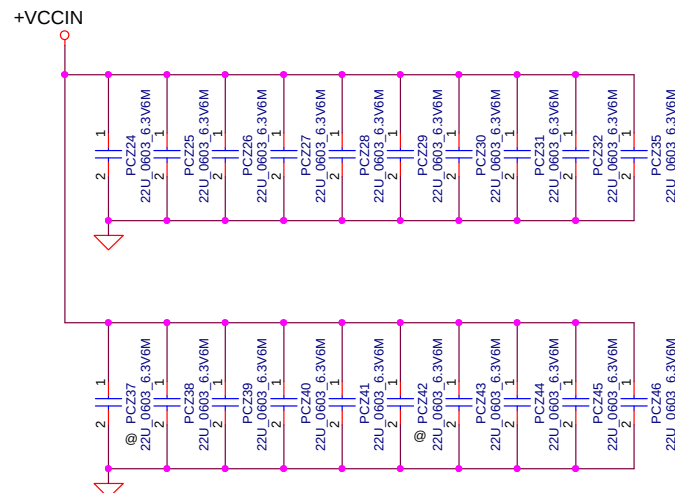
Module model information
RT3612EB_2Phase_V1A.mdd for IC portion
RT3612EB_2Phase_V1B.mdd for SW portion

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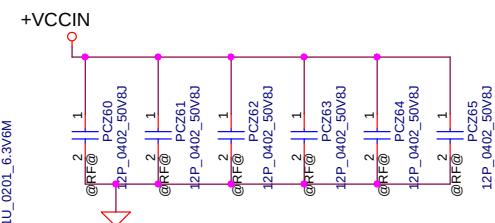
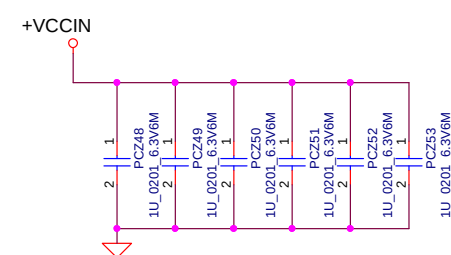


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330U R9 \*1  
22U\_0603 \*18  
1U\_0201 \*6



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Module model information  
RT6543A\_V1A.mdd for IC portion  
RT6543A\_V1B.mdd for SW portion

VCCIN\_AUX RAILS  
IPEAK = 24A  
TDC = 4A  
IL SAT = 45A  
OCP = 120% of Iccmax = 29A  
OVP = 2.2V  
FSW = 600KHZ

OCP is Lowside MOSFET Rdson sense

226K x1.2  
255K x1.4

High > 1V  
Low < 0.4V

5V: 800KHZ  
Float: 600KHZ  
GND: 400KHZ

VCCIN\_AUX VID Follow Intel PDG Rev0.71

VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

AUX input cap need place 5pcs

Rdc=0.98 mohm

330U\_R9 \*1  
22U\_0603 \*13







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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01		Cost down action		P87	Change PUB1 from BQ24800 (SA000D7R00) to BQ24781 (SA0000A6B00)	06/06	Pre-EVT
02		Add +VNN/+V1.05A circuit		P93		06/17	Pre-EVT
03		Layout		P84	Change QOB5 to SB00001IM00 Delete QOB6	06/24	Pre-EVT
04		Insufficient parts		P92 P93	Change PRH19 from 0 0402 ±1% 1/16W(SD034000080) to 0 0402 ±5% 1/16W(SD028000080) Change PRY1,PRY2,PRY3 from 0 0402 ±1% 1/8W(SD000018R00) to 0 0402 ±5%(SD028000080) Change PRY7 from 10K 0402 ±1% 1/16W(SD034000080) to 10K 0402 ±1% 1/16W(SD034100280) Change PCY12 from 10u_0603_6.3V6M% (SE000005T80) to 10K_0402 ±1% 1/16W(SE00000SU00)		
05							
06		CPU transient test					
07							
08							
09							
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