

QFKAA

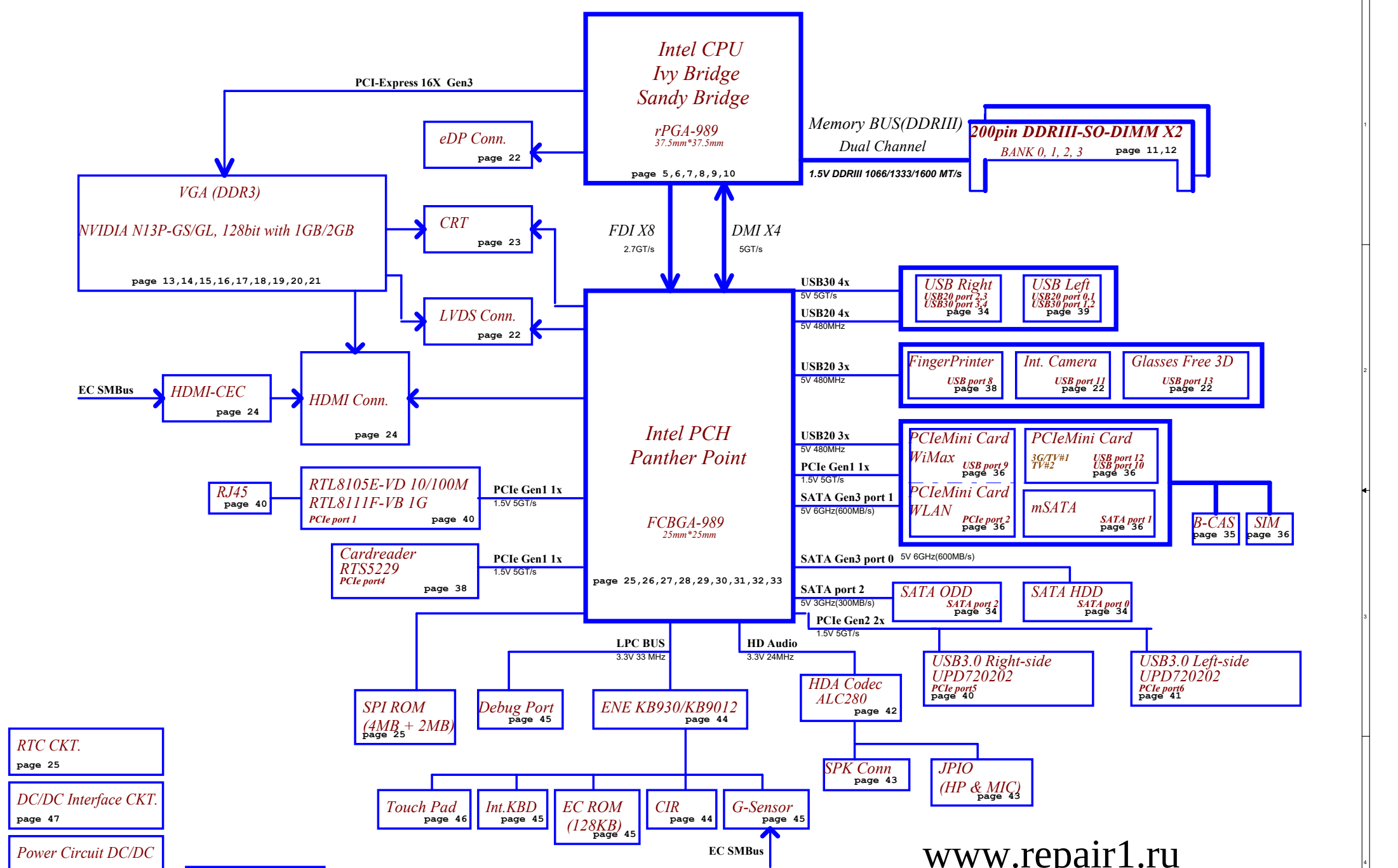
Yosemite 10FG

LA-8391P REV 1.0 Schematic

Intel Processor(Ivy Bridge / Sandy Bridge)
PCH(Panther Point)
2012-02-02 Rev 1.0

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RTC CKT.
page 25

DC/DC Interface CKT.
page 47

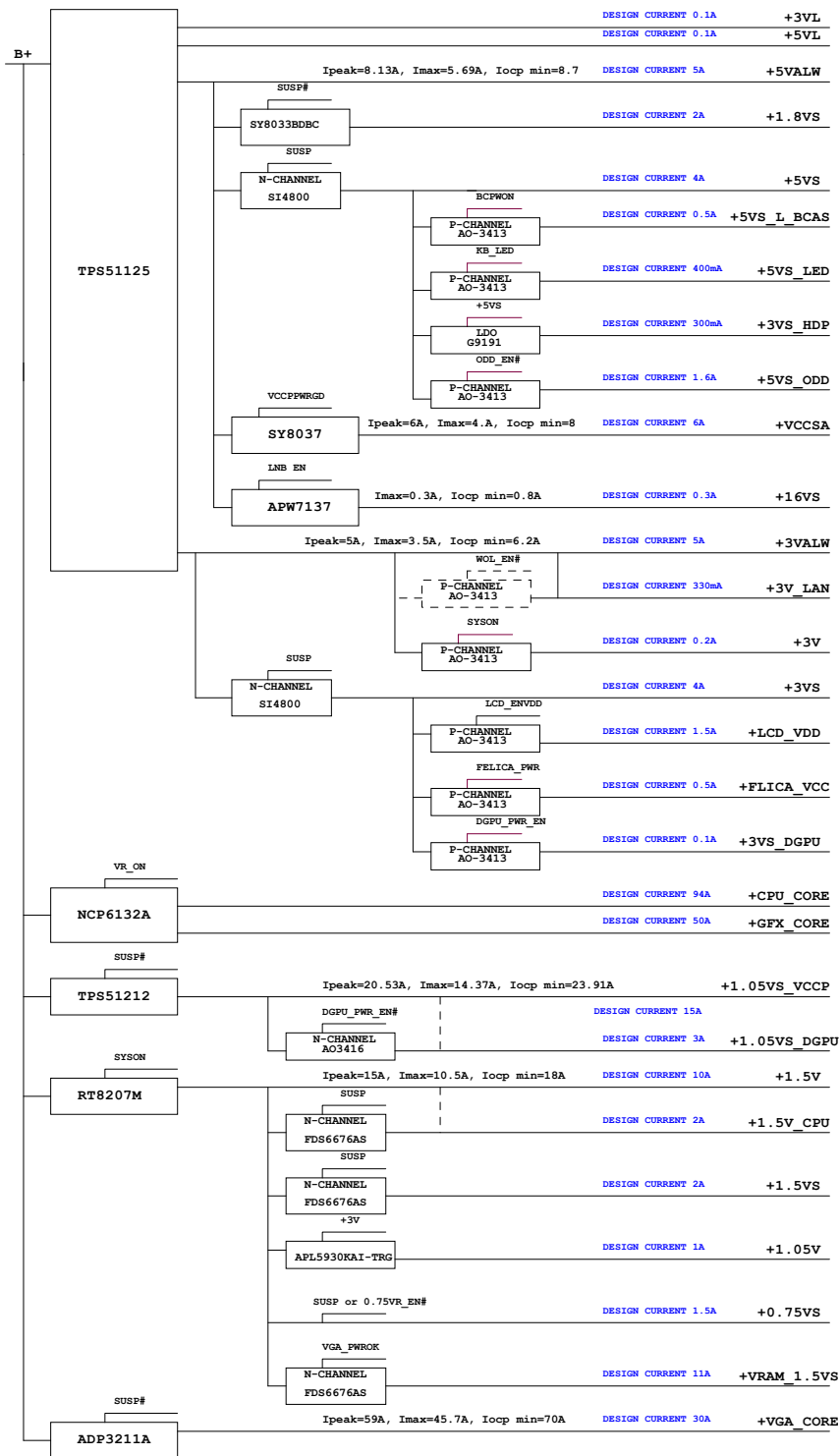
Power Circuit DC/DC
page 48,49,50,51,52,
53,54,55,56,57,58,59

Power On/Off CKT.
page 46

Finger Printer/B
page 35

Power/B
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +VSB	+1. 5V	+5VS +3VS +1. 8VS +1. 5VS +1. 05VS +0. 75VS +CPU_CORE +VGA_CORE +GFX_CORE +VTT +VRAM_1. 5VS +3VS_DGPU +1. 05VS_DGPU
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	WLAN/WIMAX		
+3VS	3G		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b
+3VL	HDMI-CEC	34 H	0011 0100 b
Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b
+3VS	NVIDIA GPU	9E H	1001 1010 b
+3VS	G-Sensor	40 H	0100 0000 b

Platform	SKU	CPU	PCH	VGA
Calpella	Discrete (DIS@)	Clarksfield/Arrandale	HM76@/HM77@	N13PGSR1@/N13PGLR1@
	Optimus (OPT@)	Arrandale	HM76@/HM77@	N13PGSR1@/N13PGLR1@

BTO Option Table

Function	HDMI				CPU		
description	HDMI				Arrandale	Clarksfield	
explain	UMA	Discrete/ Optimus	COMMON	CEC	Arrandale	Clarksfield	Clarksfield with S3 Power Saving
BTO	IHDMI@	DHDMI@	HDMI@	CEC@	M1@	M3@	PSM3@

Function	MINI PCI-E SLOT			LAN		Fingerprint	CIR	KB Light
description	SLOT2		SLOT1	LAN		Fingerprint	CIR	KB Light
explain	3G	TV Tuner	WIMAX	10/100M	Giga	Fingerprint	CIR	KB Light
BTO	3G@	TV@	WIMAX@	8105E@	8111E@	FP@	CIR@	KBL@

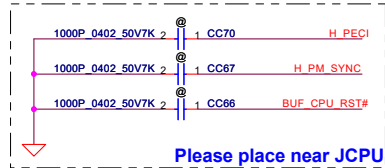
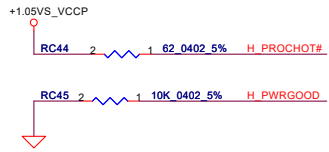
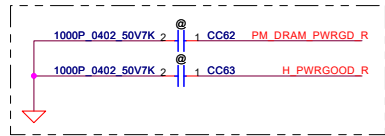
Function	G-SENSOR	SKU		LVDS			Camera & Mic	
description	G-SENSOR	SKU		2D HD/FHD Panel	2D HD eDP	3D Panel	Camera & Mic	
explain	G-SENSOR	Discrete	Optimus	Optimus	Optimus	Discrete	Camera & Mic	
BTO	GSENSOR@	DIS@	OPT@	LVDS2D@	OPTFHD@	IEDP@	3D@	CAM@

Function	GPU	
description	N13P-GS	N13P-GL
explain	N13PGS	N13PGL
BTO	N13PGSR1@	N13PGLR1@

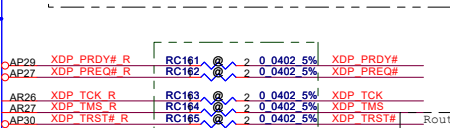
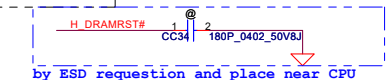
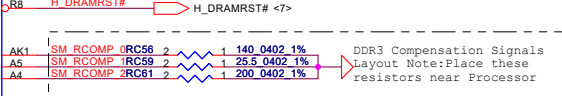
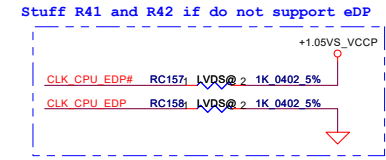
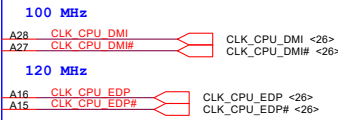
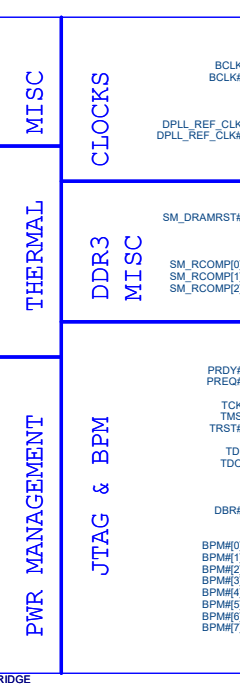
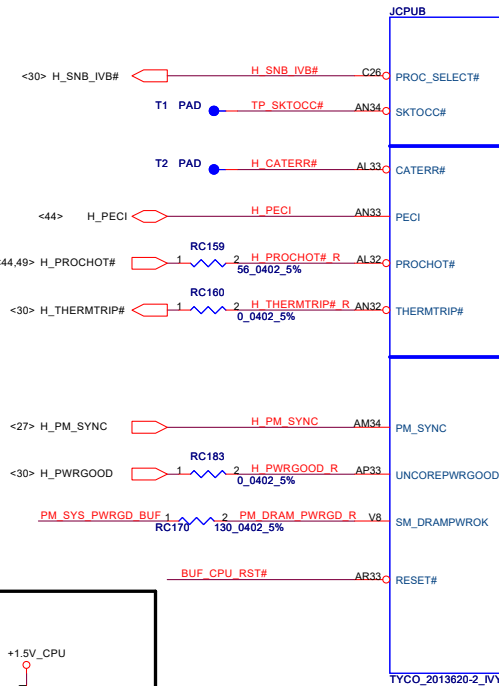
STATE	SIGNAL		
	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW

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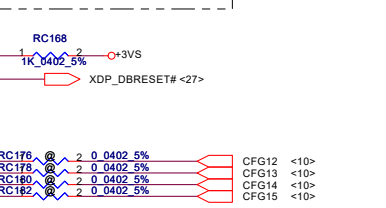
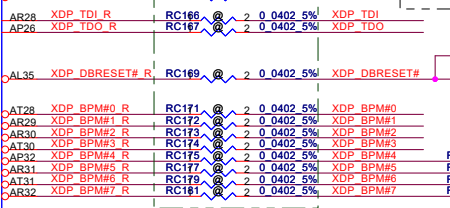
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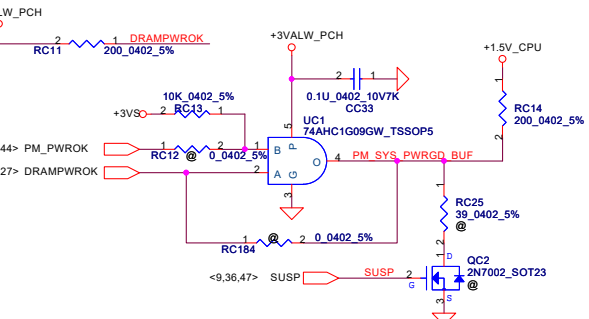
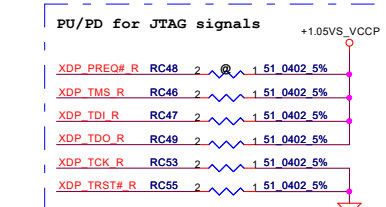
Please place near JCPU



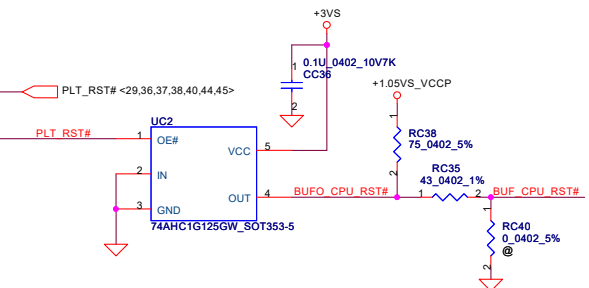
Routed as a single daisy chain



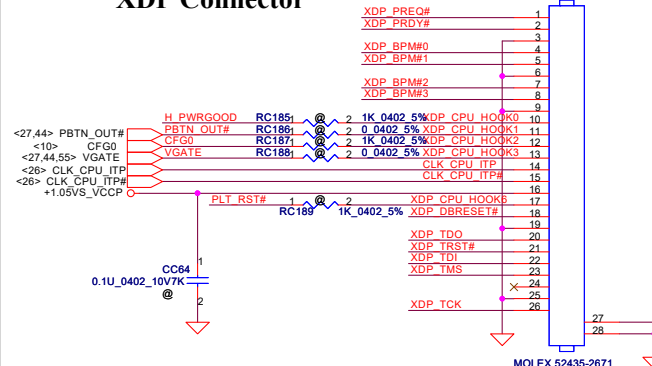
Close to CPU side



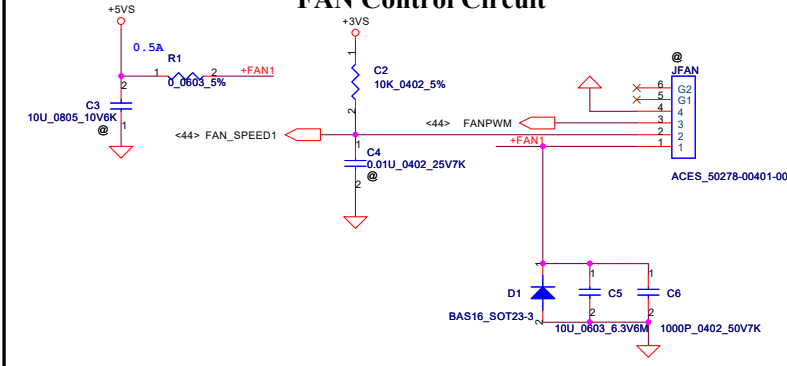
Buffered Reset to CPU



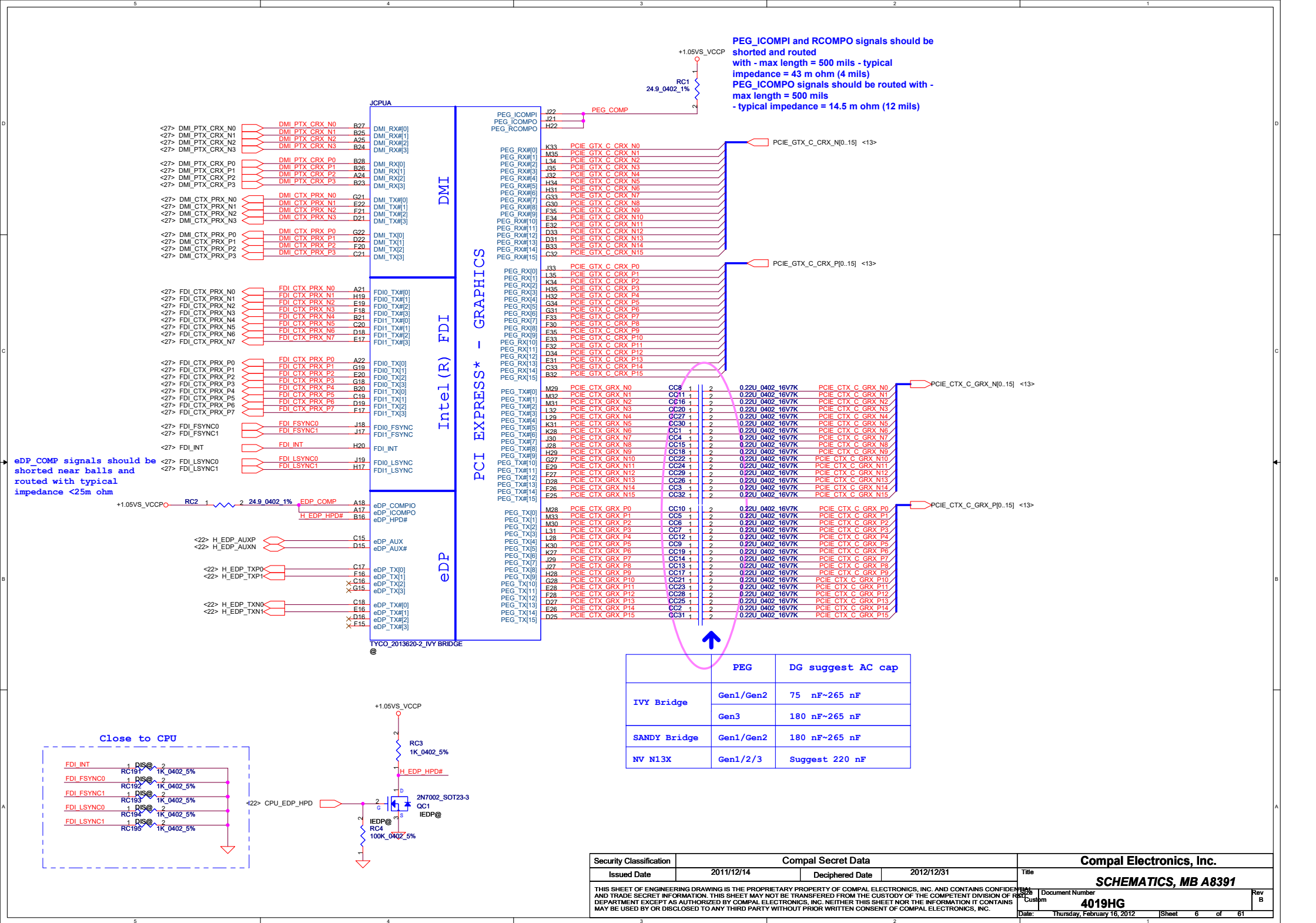
XDP Connector

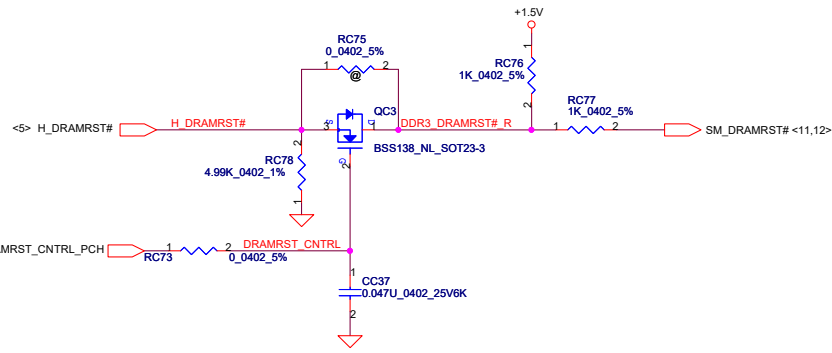
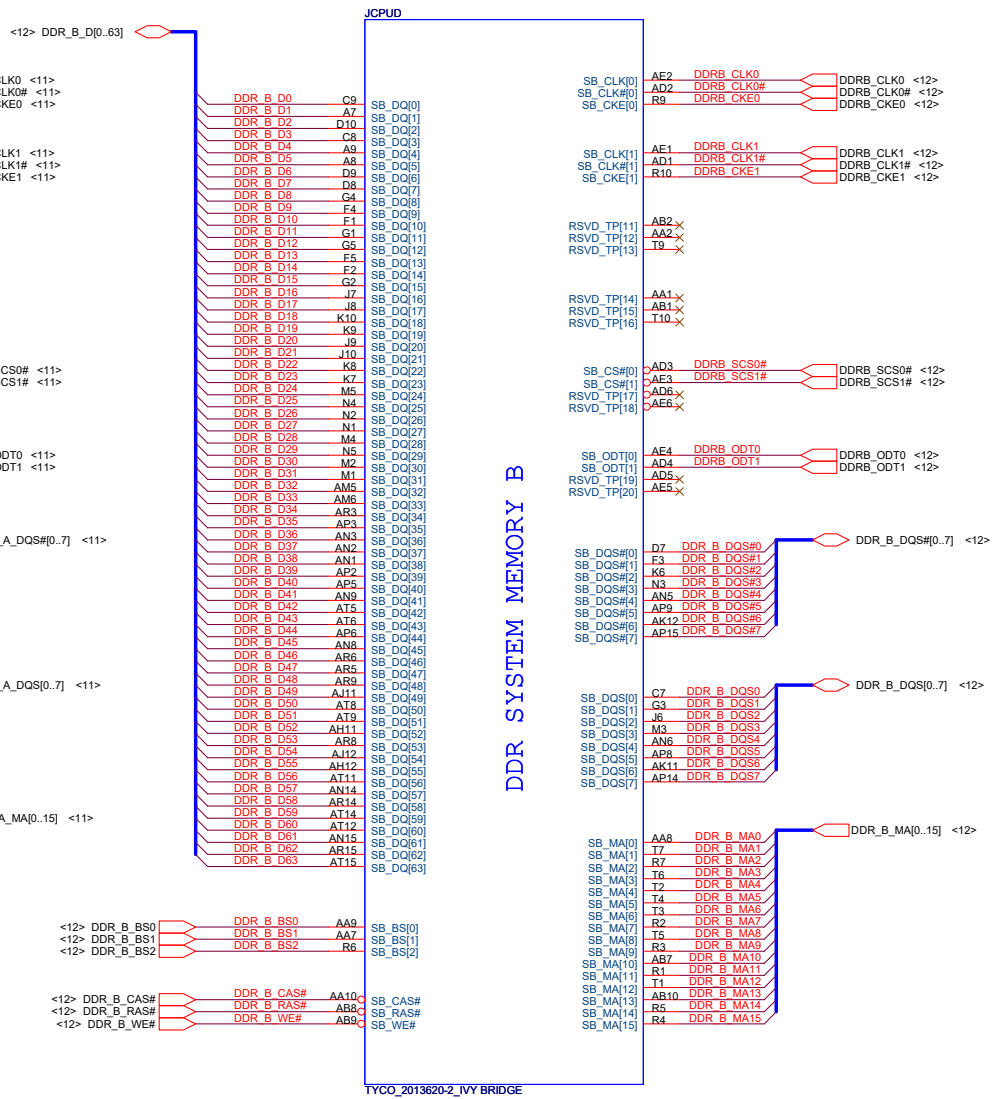
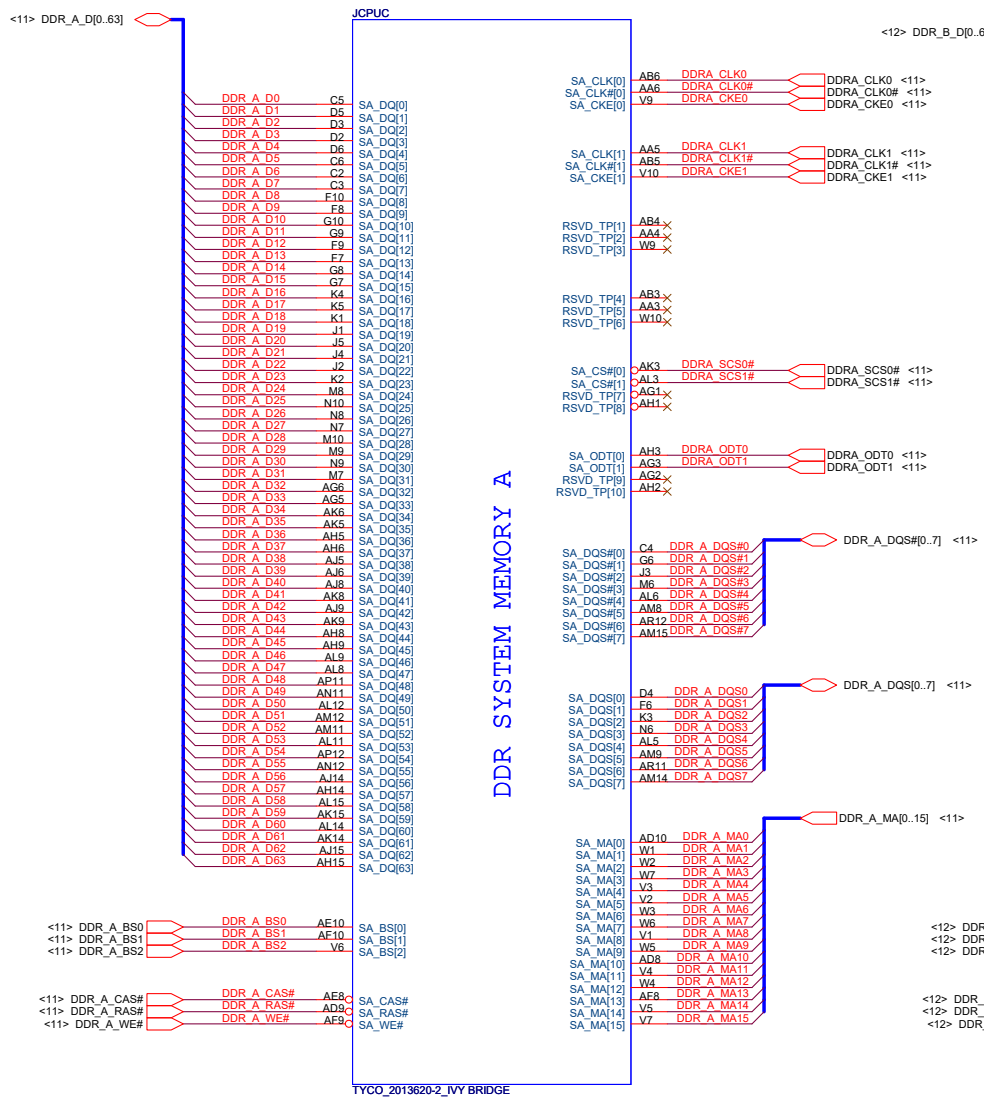


FAN Control Circuit



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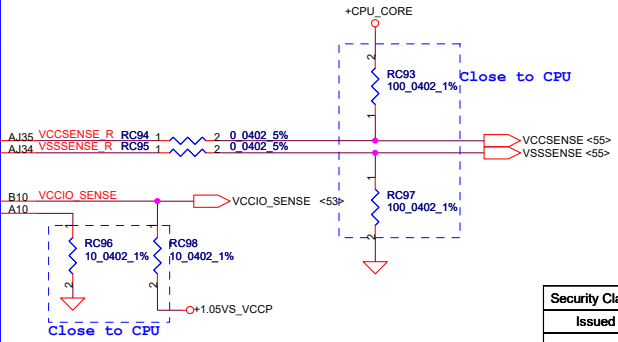
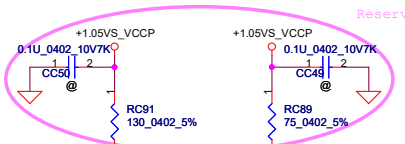
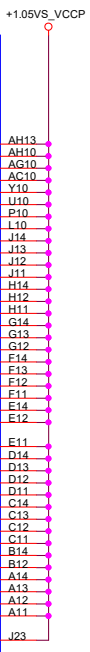
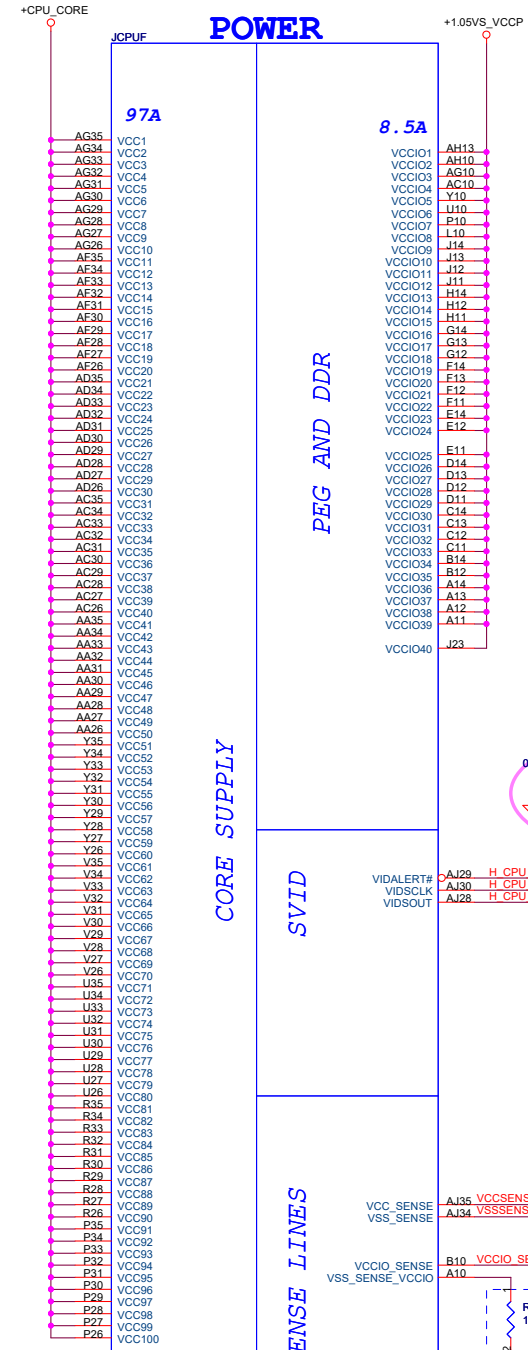
POWER

CORE SUPPLY

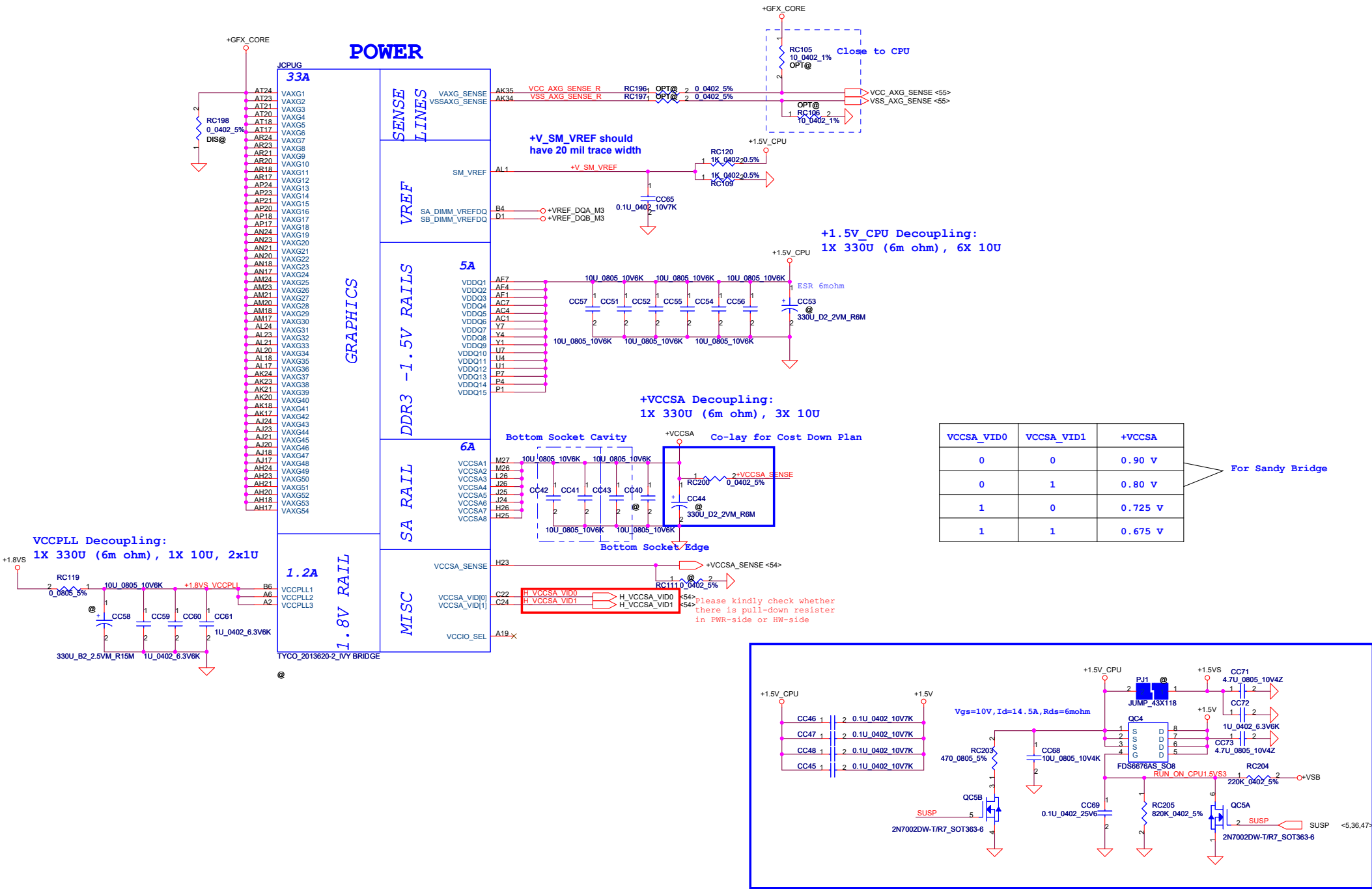
SVID

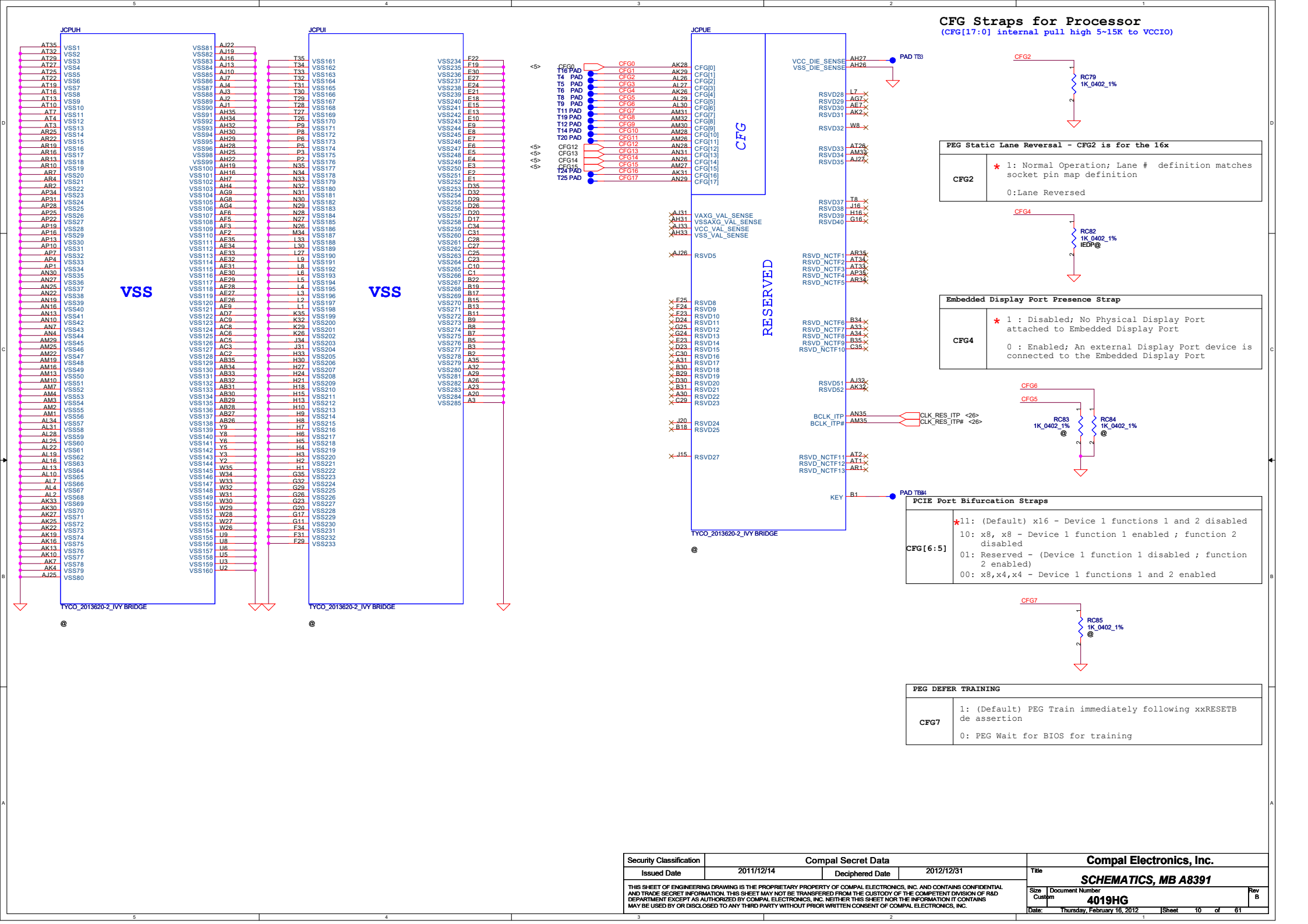
SENSE LINES

PEG AND DDR

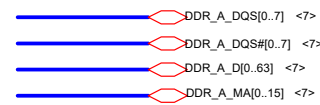
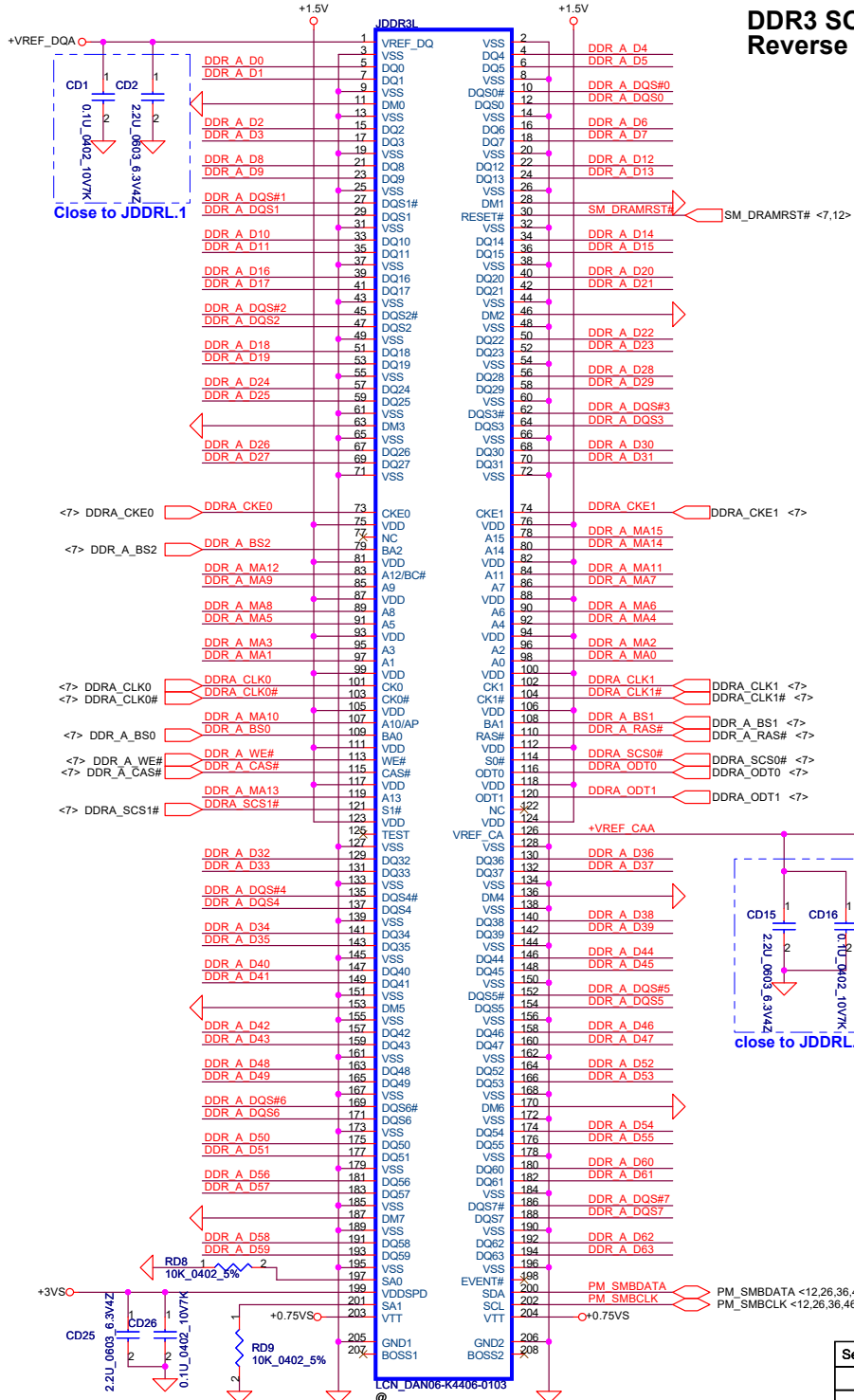


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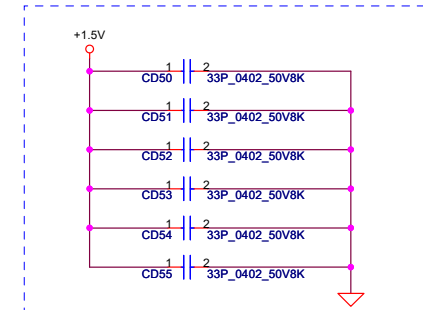
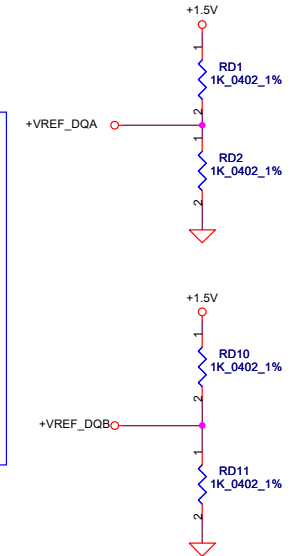
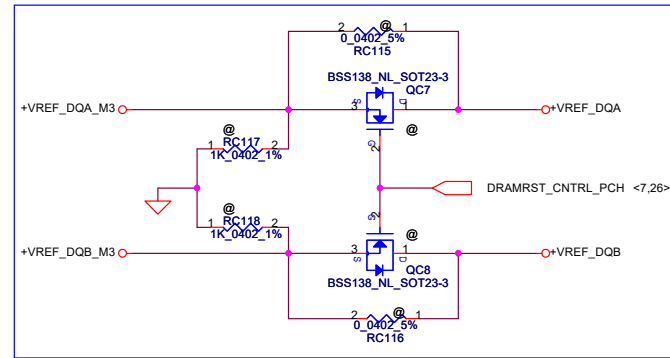




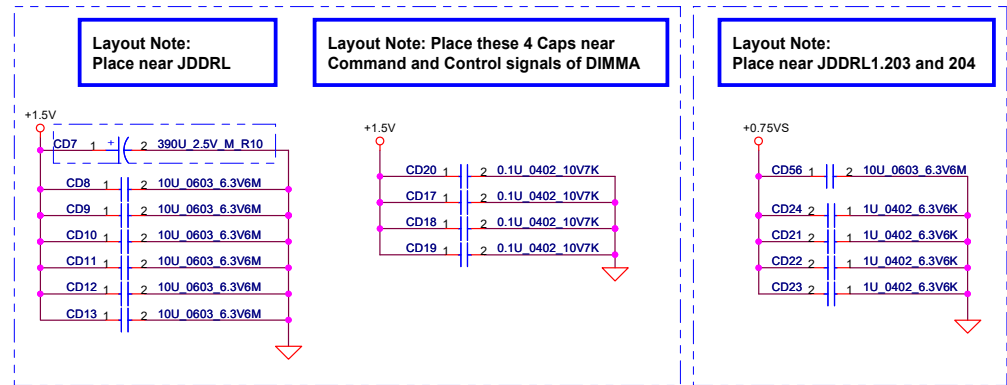
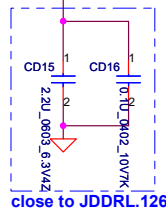
DDR3 SO-DIMM A Reverse Type



Intel DDR Vref M3

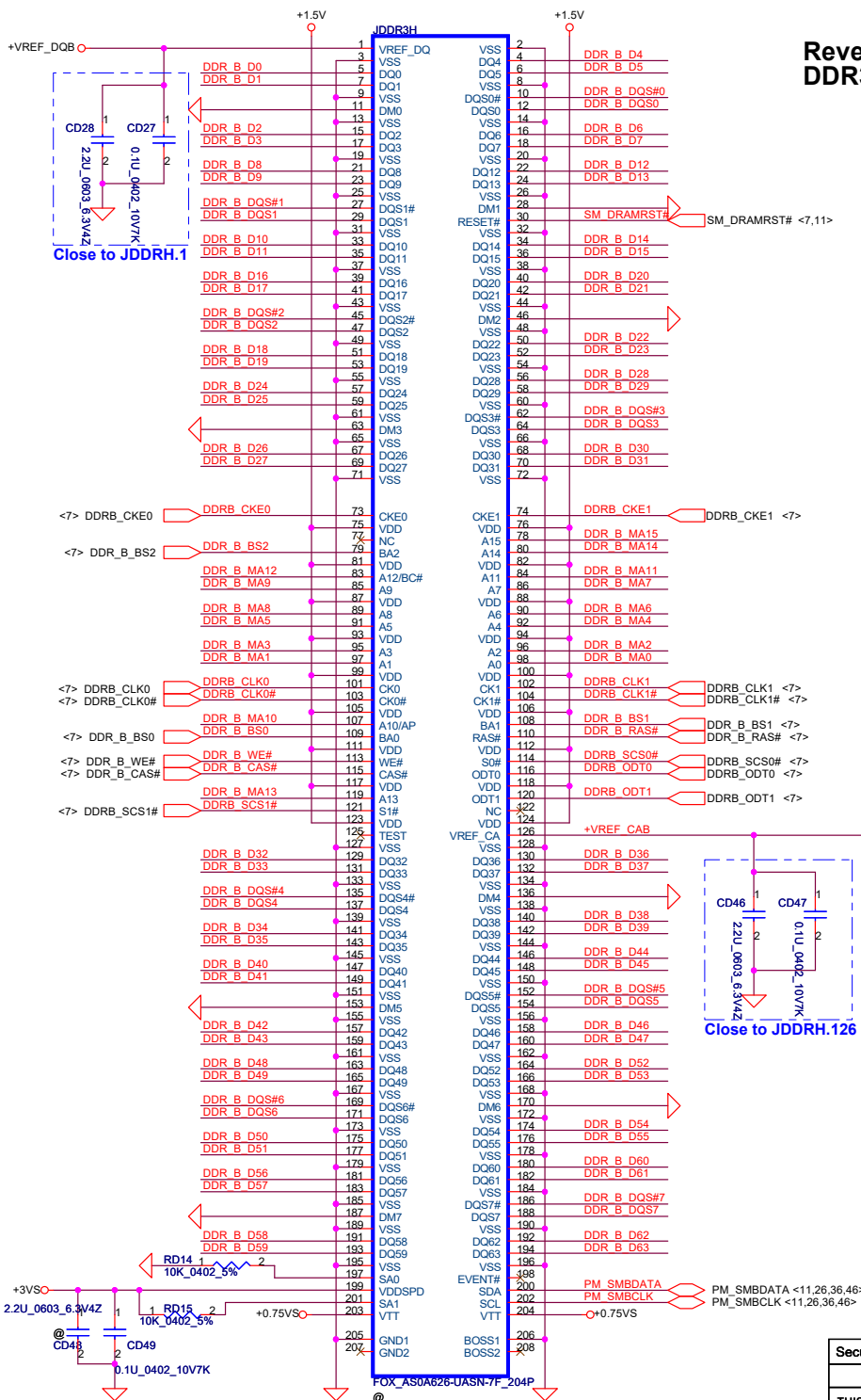


please place these caps near the
reference power plane of CMD/AD



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Reverse Type DDR3 SO-DIMM B



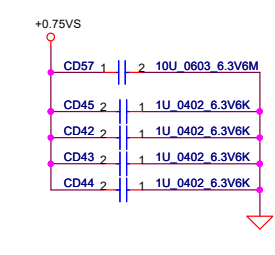
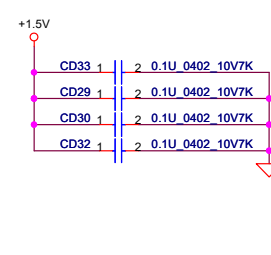
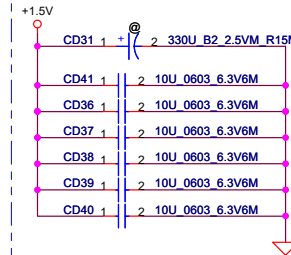
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- DDR_B_DQS#[0..7] <7>
- DDR_B_DQ[0..63] <7>
- DDR_B_MA[0..15] <7>



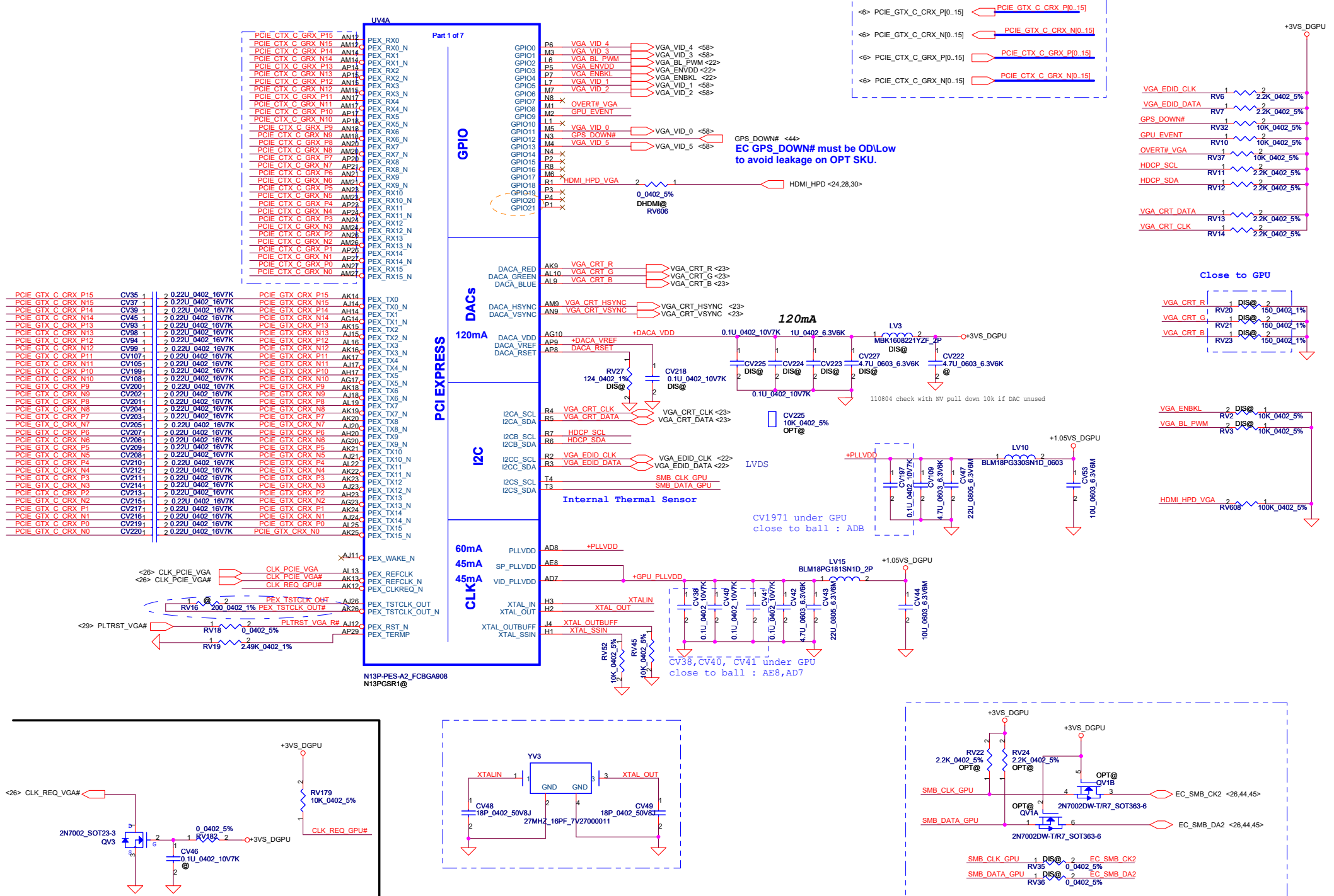
Layout Note:
Place near JDDRH

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204

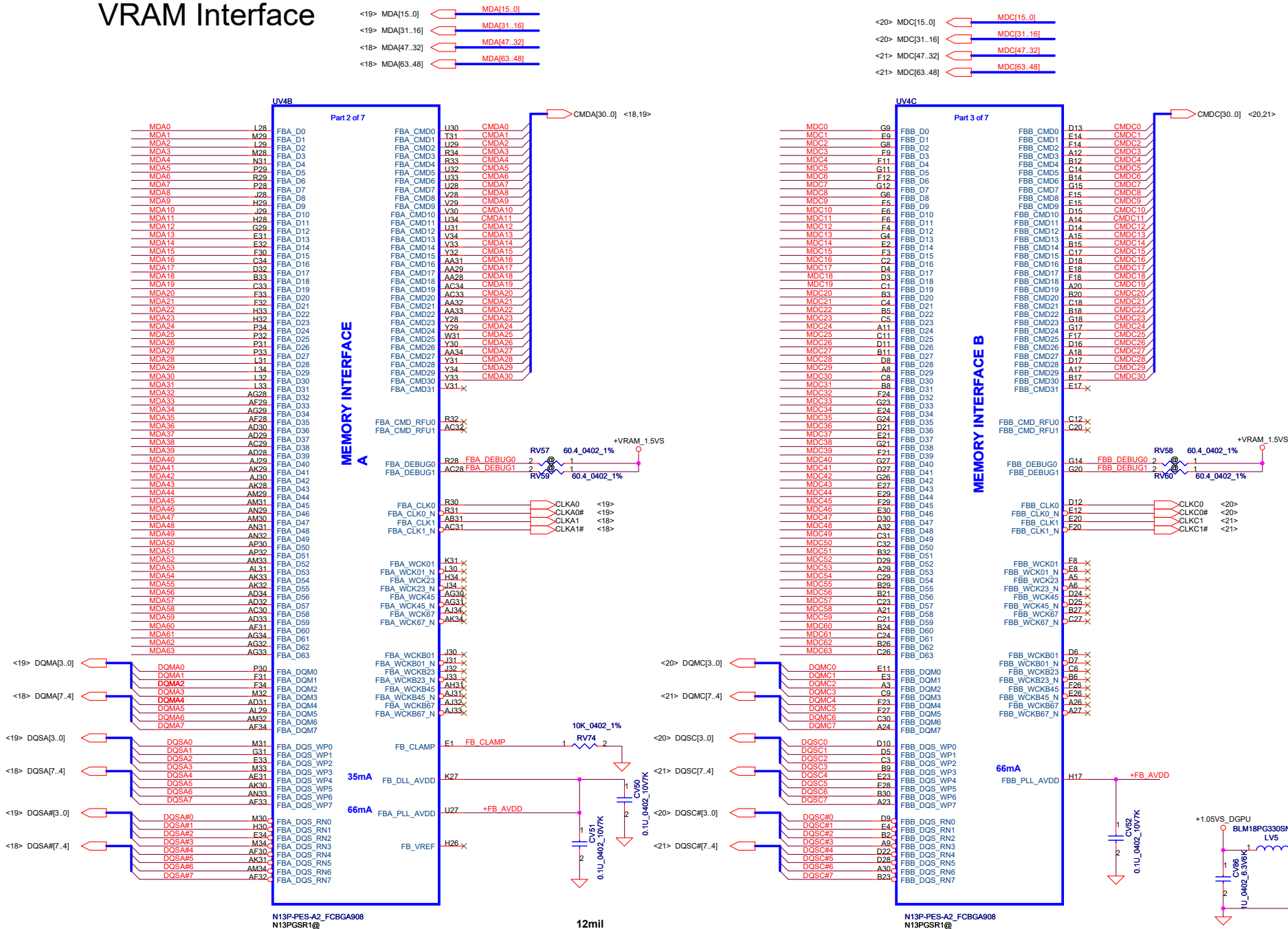


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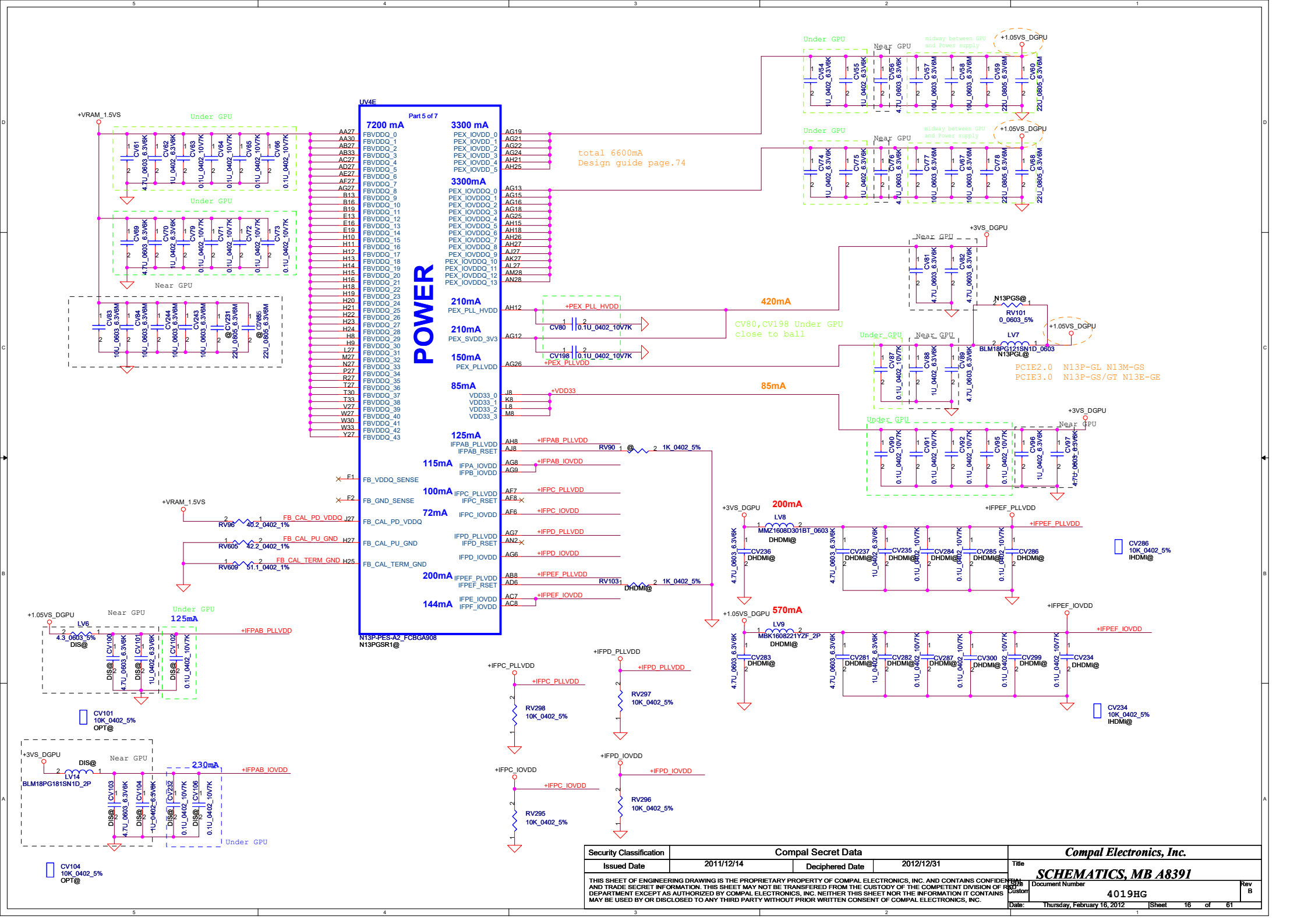


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VRAM Interface



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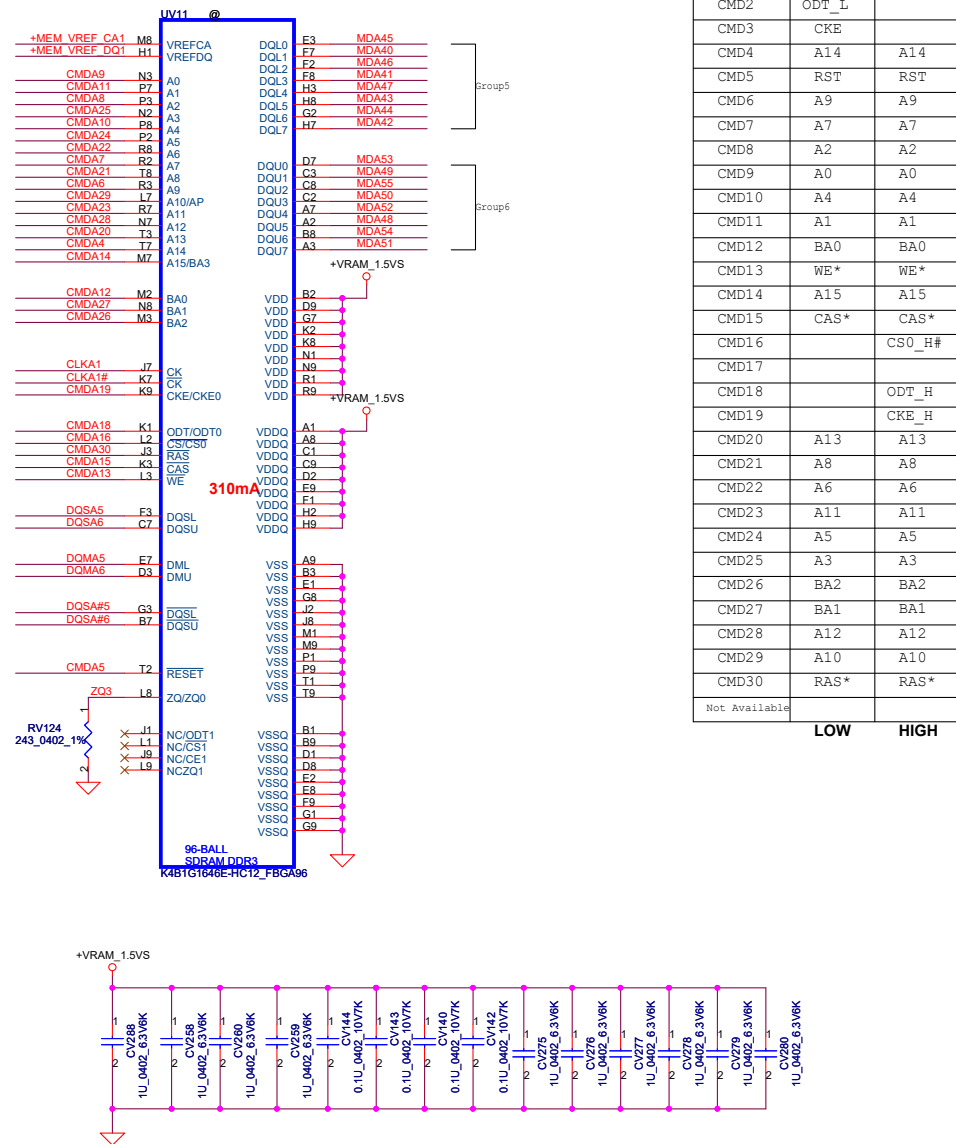


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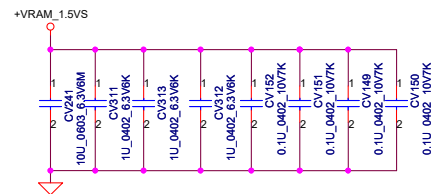
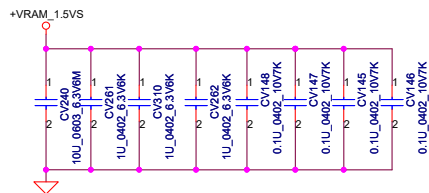
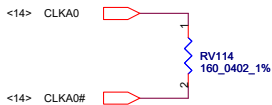
64Mx16 DDR3 *8==>1GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

64Mx16 DDR3 *8==>1GB

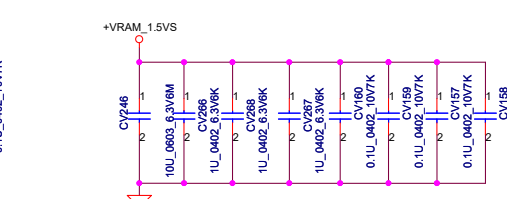
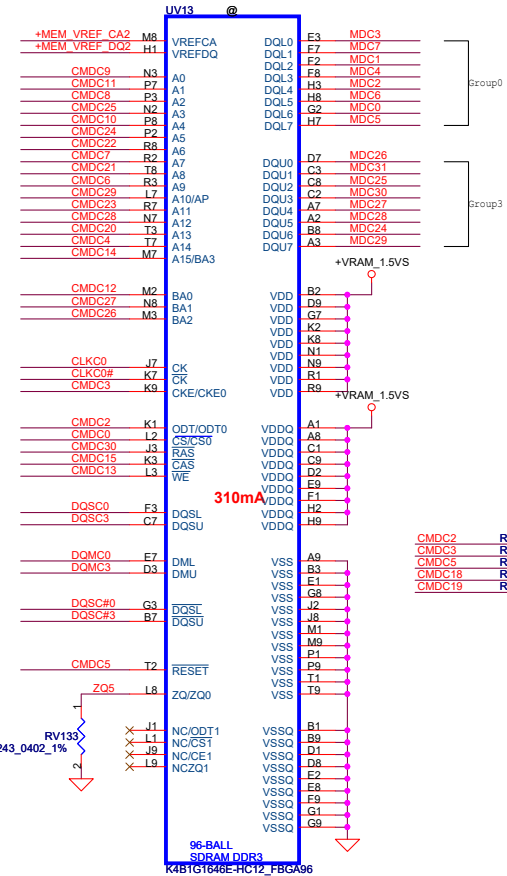
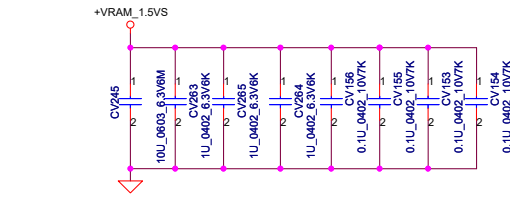
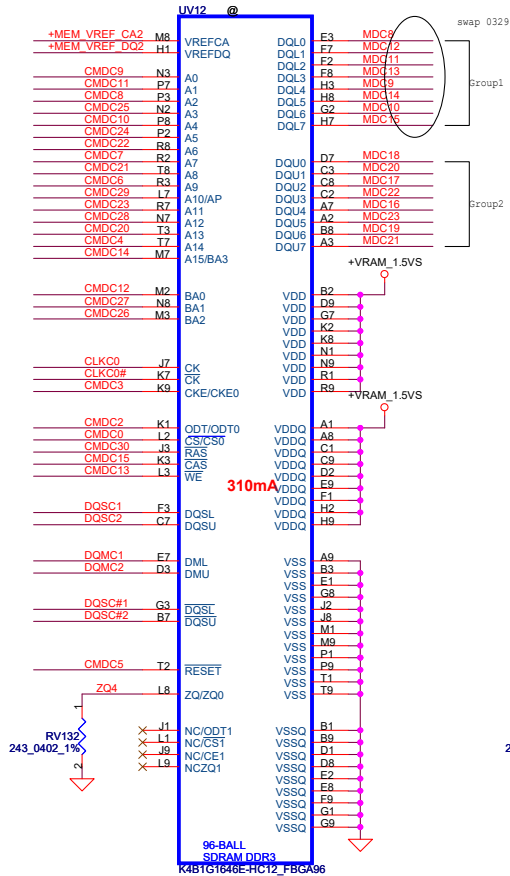
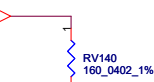
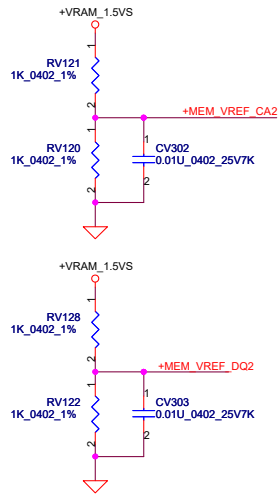


	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

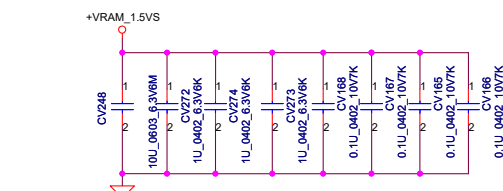
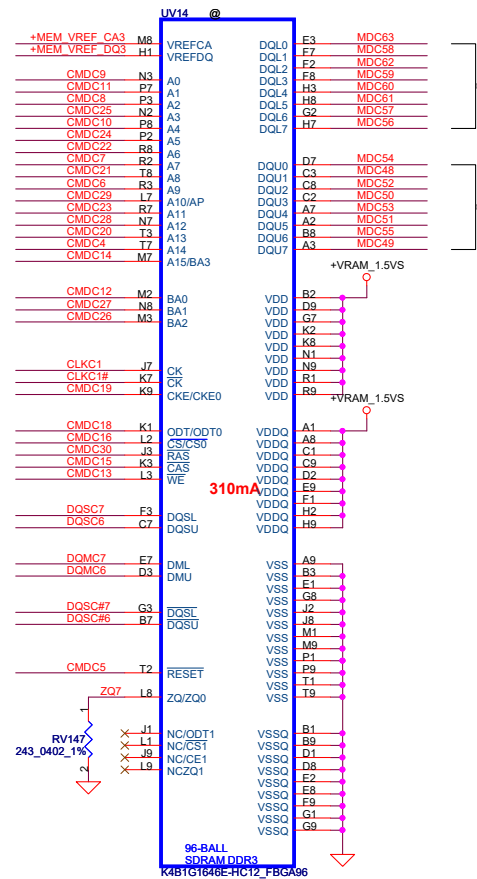
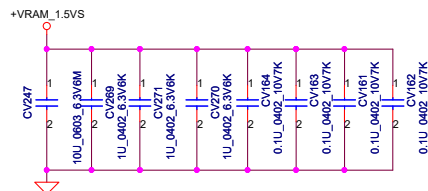
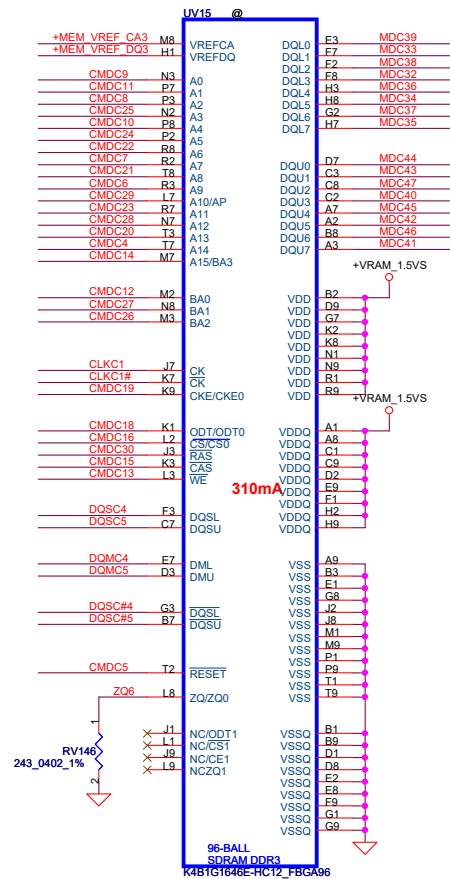
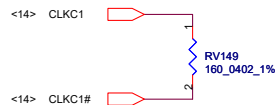
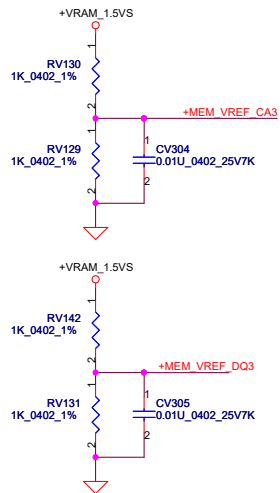
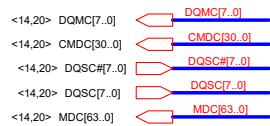
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<14,21> DQSC# [7..0] DQSC# [7..0]
<14,21> DQMC[7..0] DQMC[7..0]
<14,21> MDC[63..0] MDC[63..0]
<14,21> CMDC[30..0] CMDC[30..0]



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

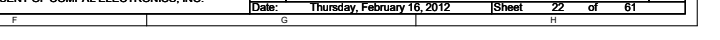
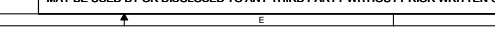
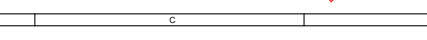
64Mx16 DDR3 *8==>1GB



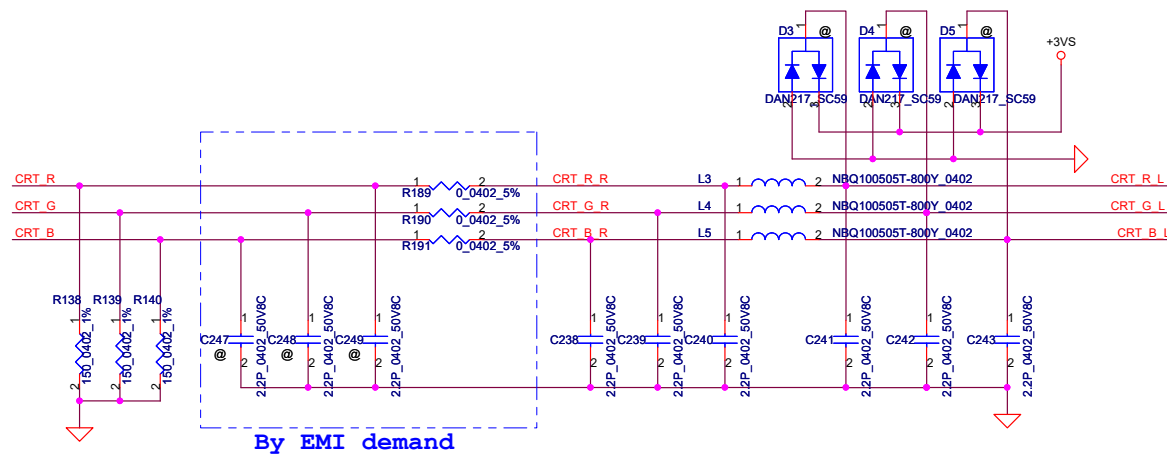
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

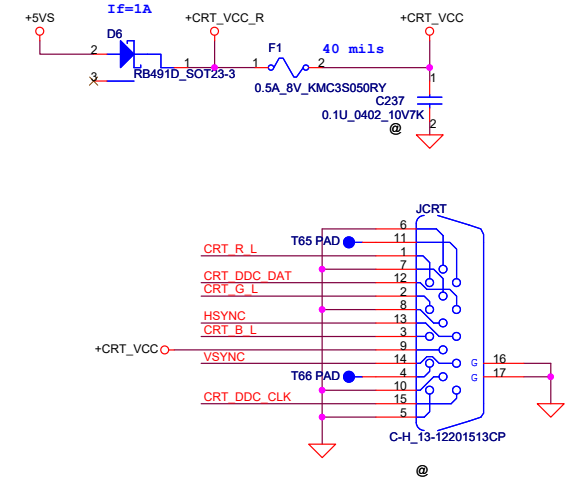
LVDS2D@ 1 2 LVDS TXOUT0+



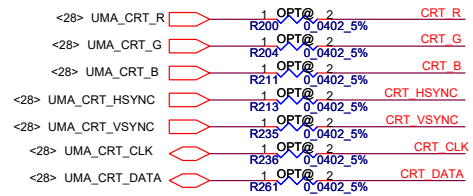
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				Customer		B	
				Date:	Thursday, February 16, 2012	Sheet	22 of 81



CRT CONNECTOR

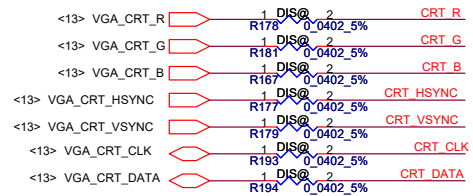


OPTIMUS

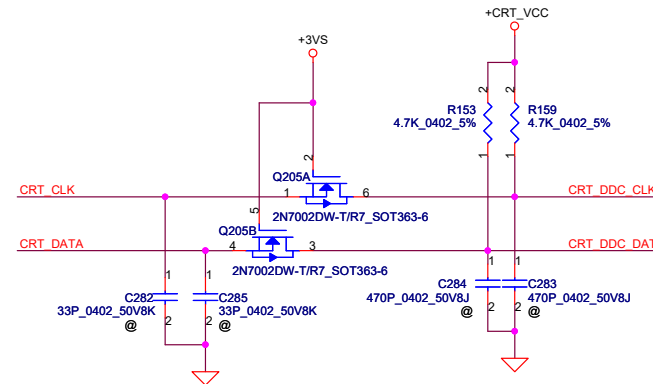
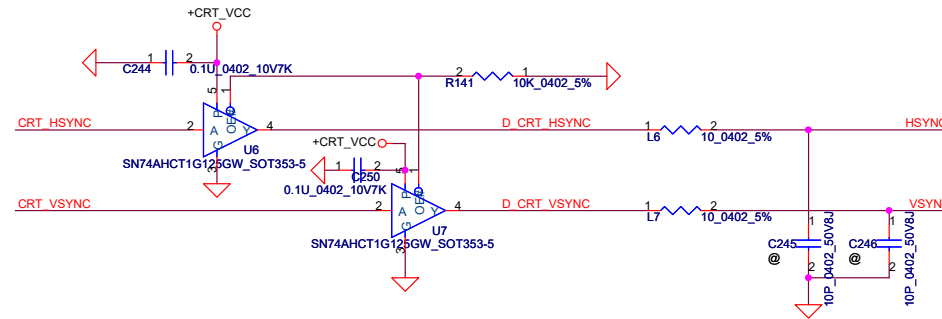


Close to CRT Connector

DISCRETE

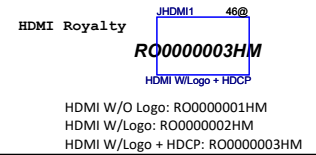
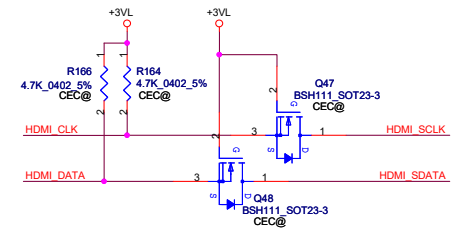
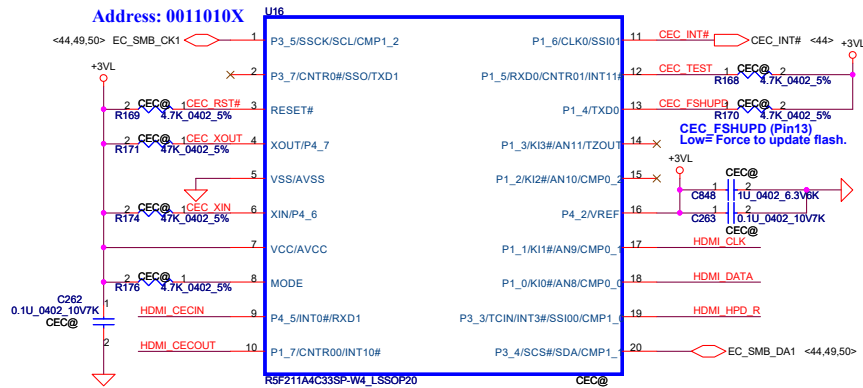
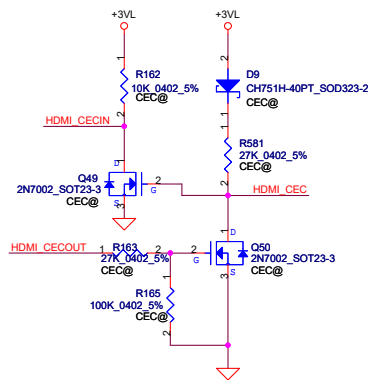


Close to CRT Connector

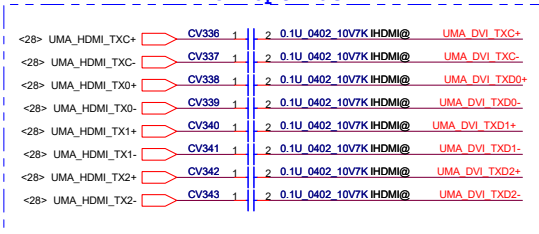


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				Date	Thursday, February 16, 2012
				Sheet	23 of 61

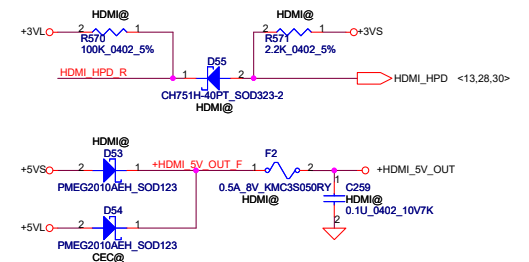
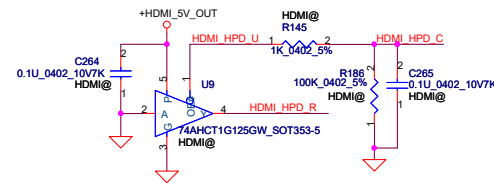
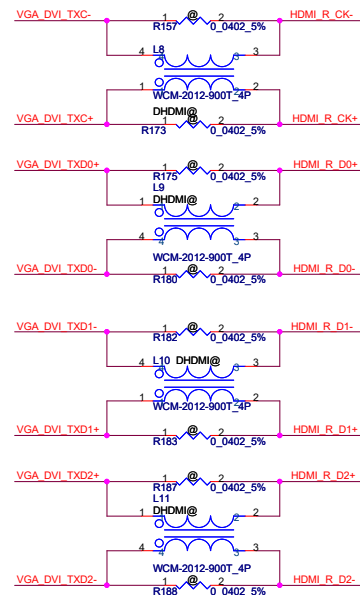
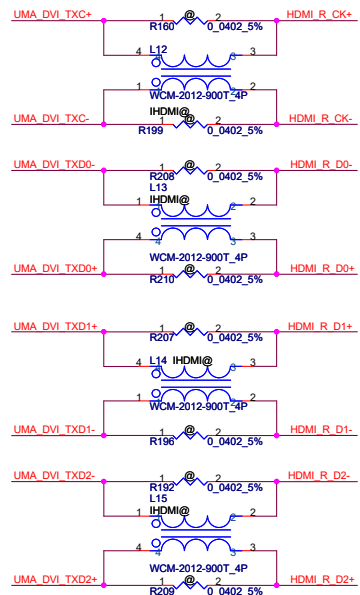
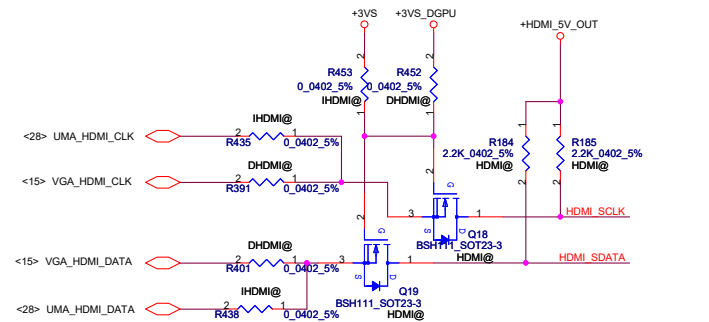
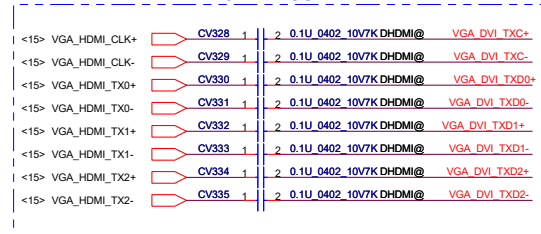
HDMI CEC Controller



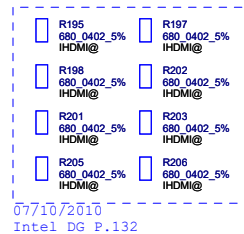
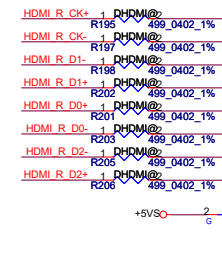
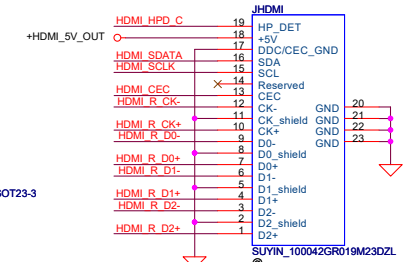
For Optimus



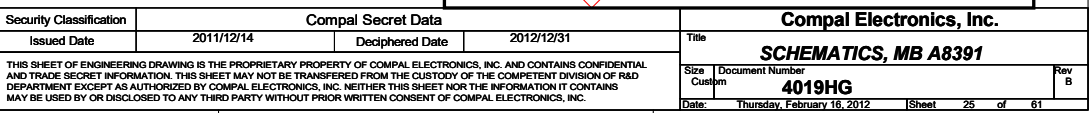
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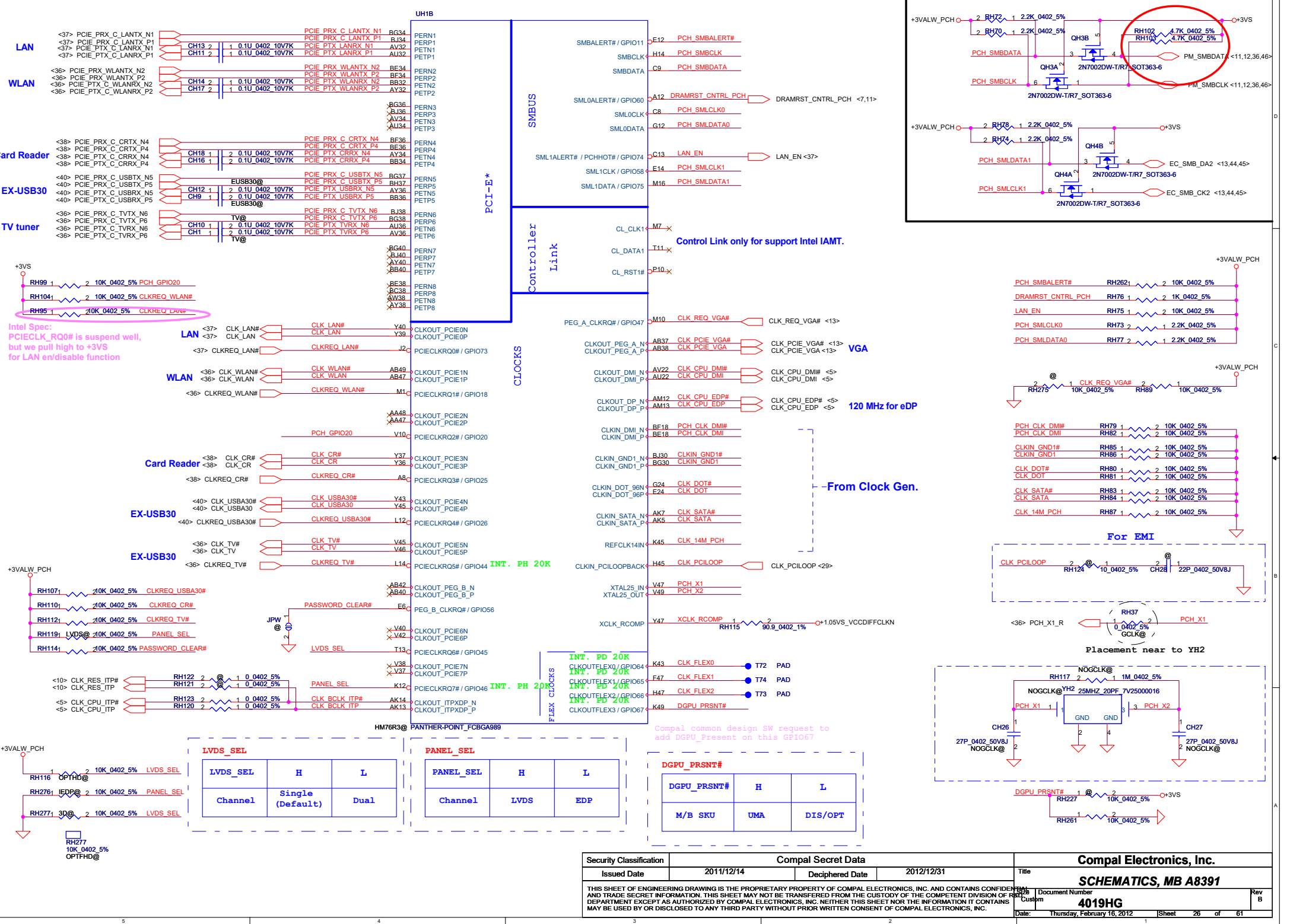


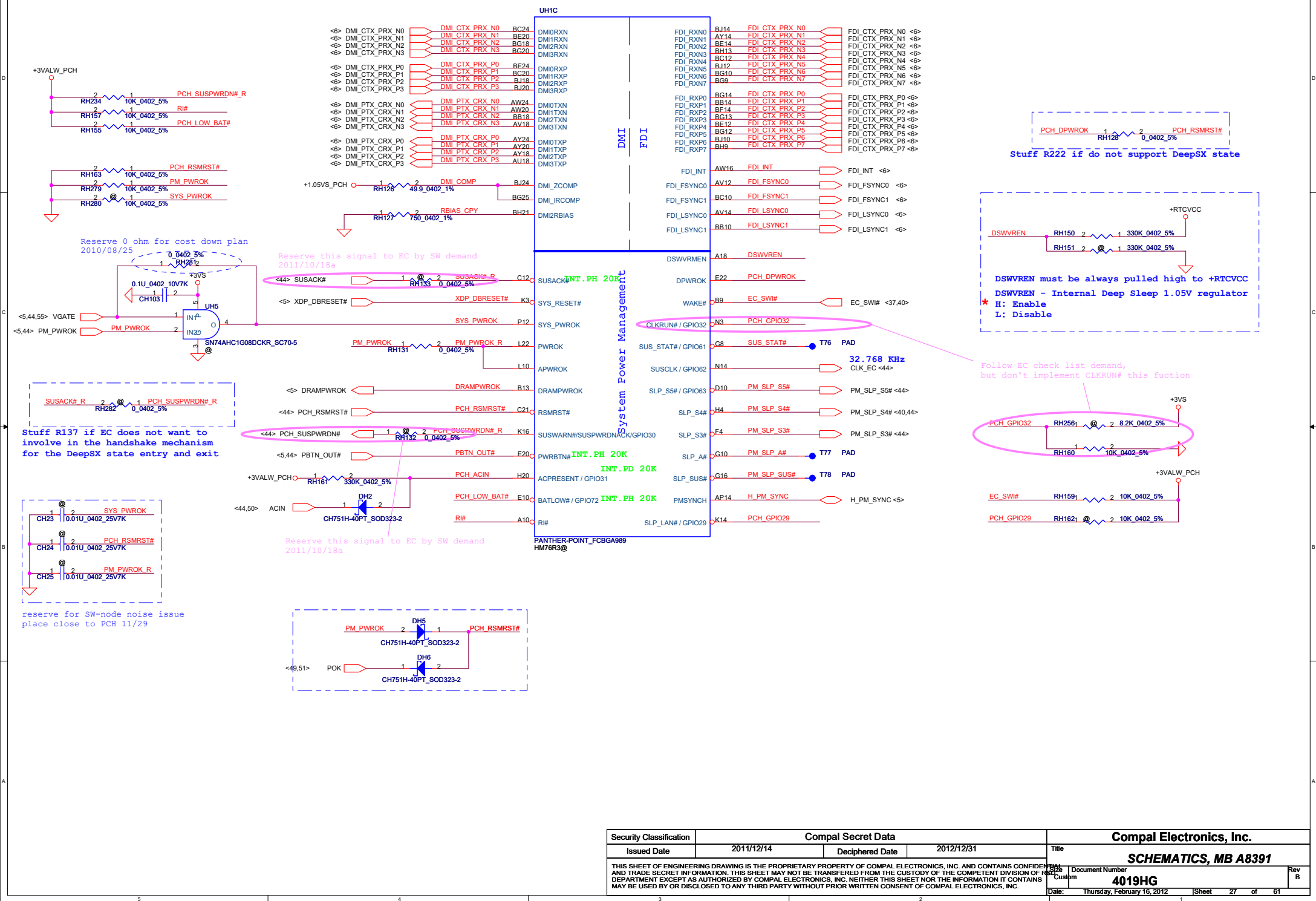
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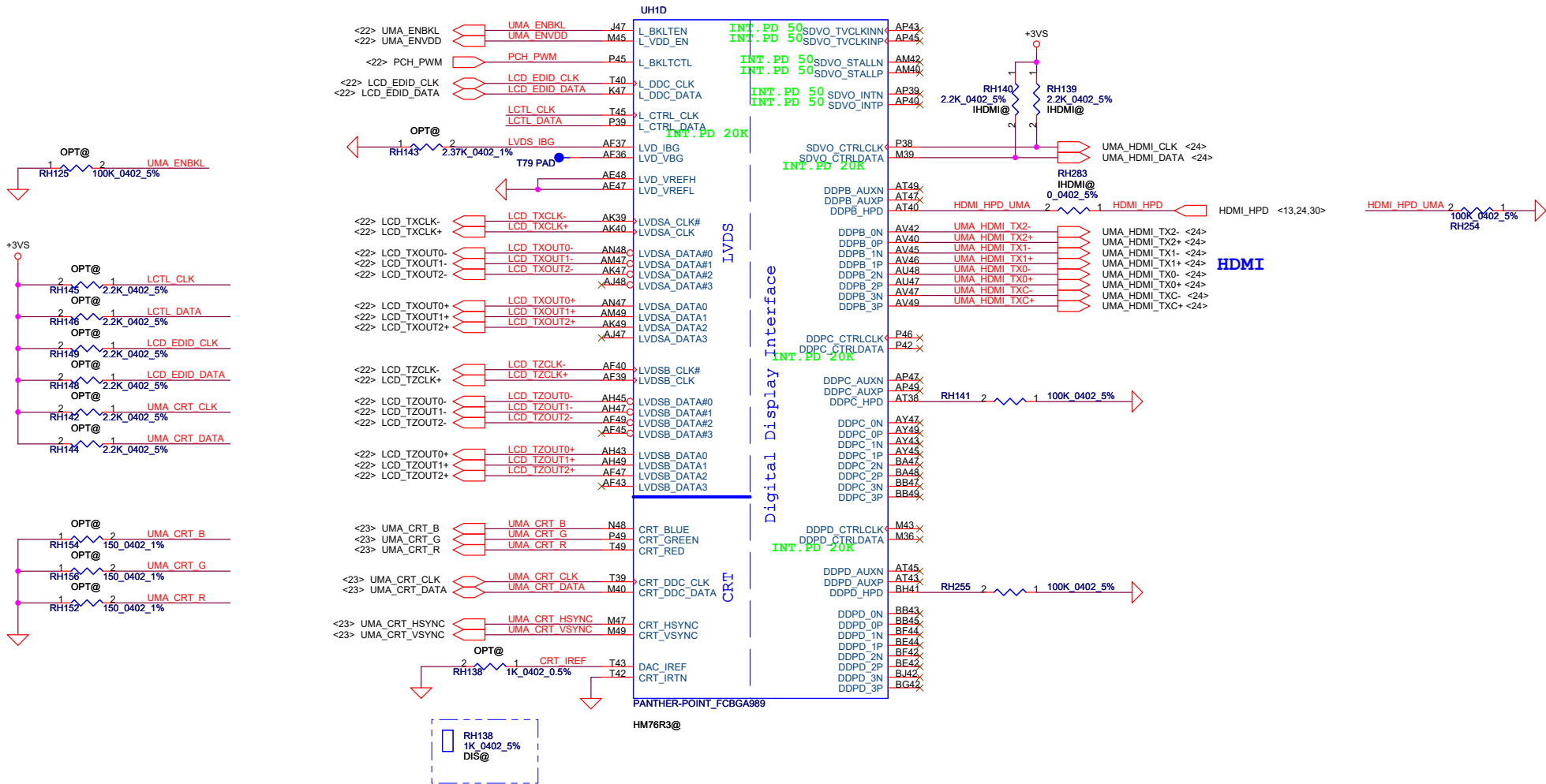


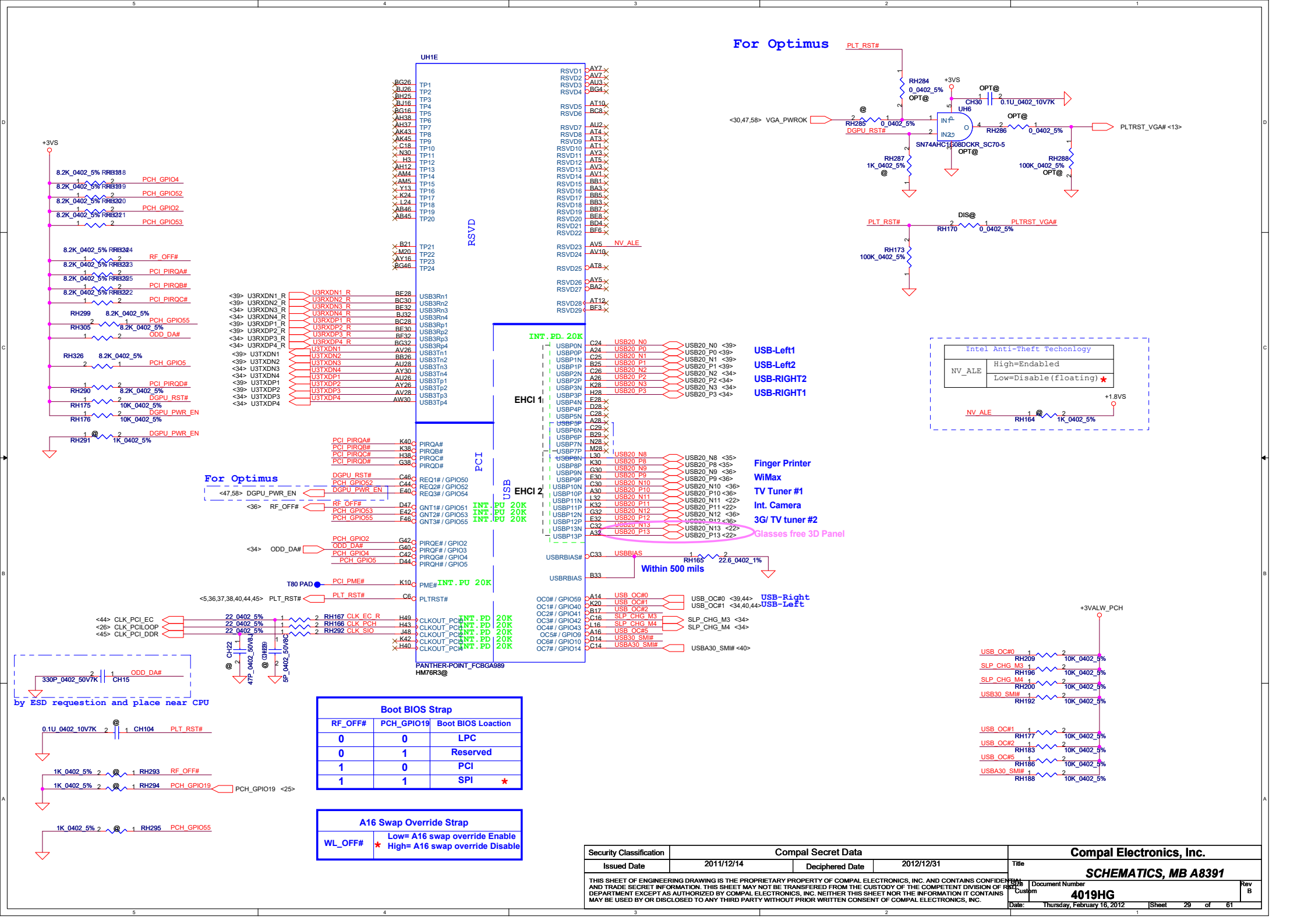
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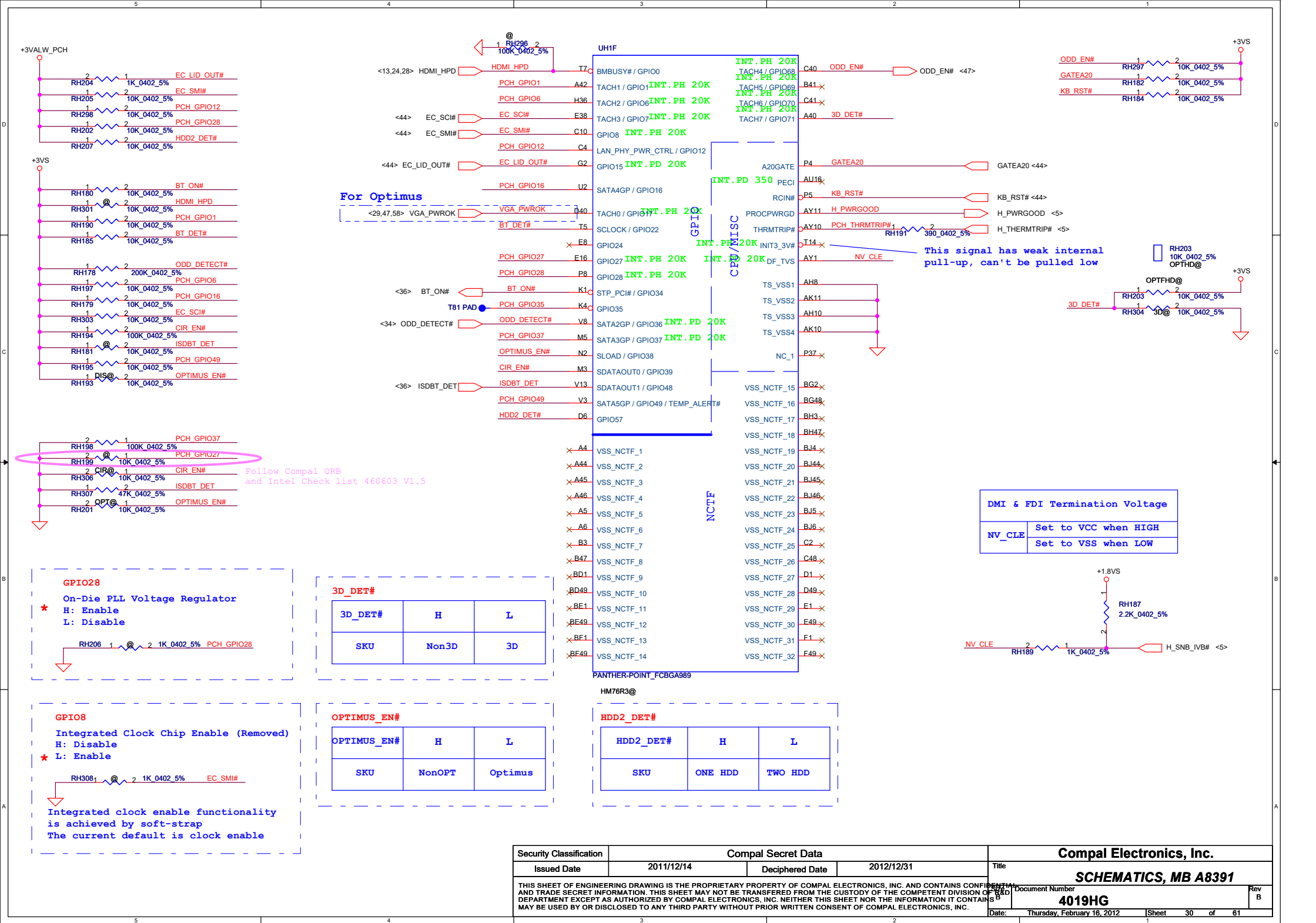


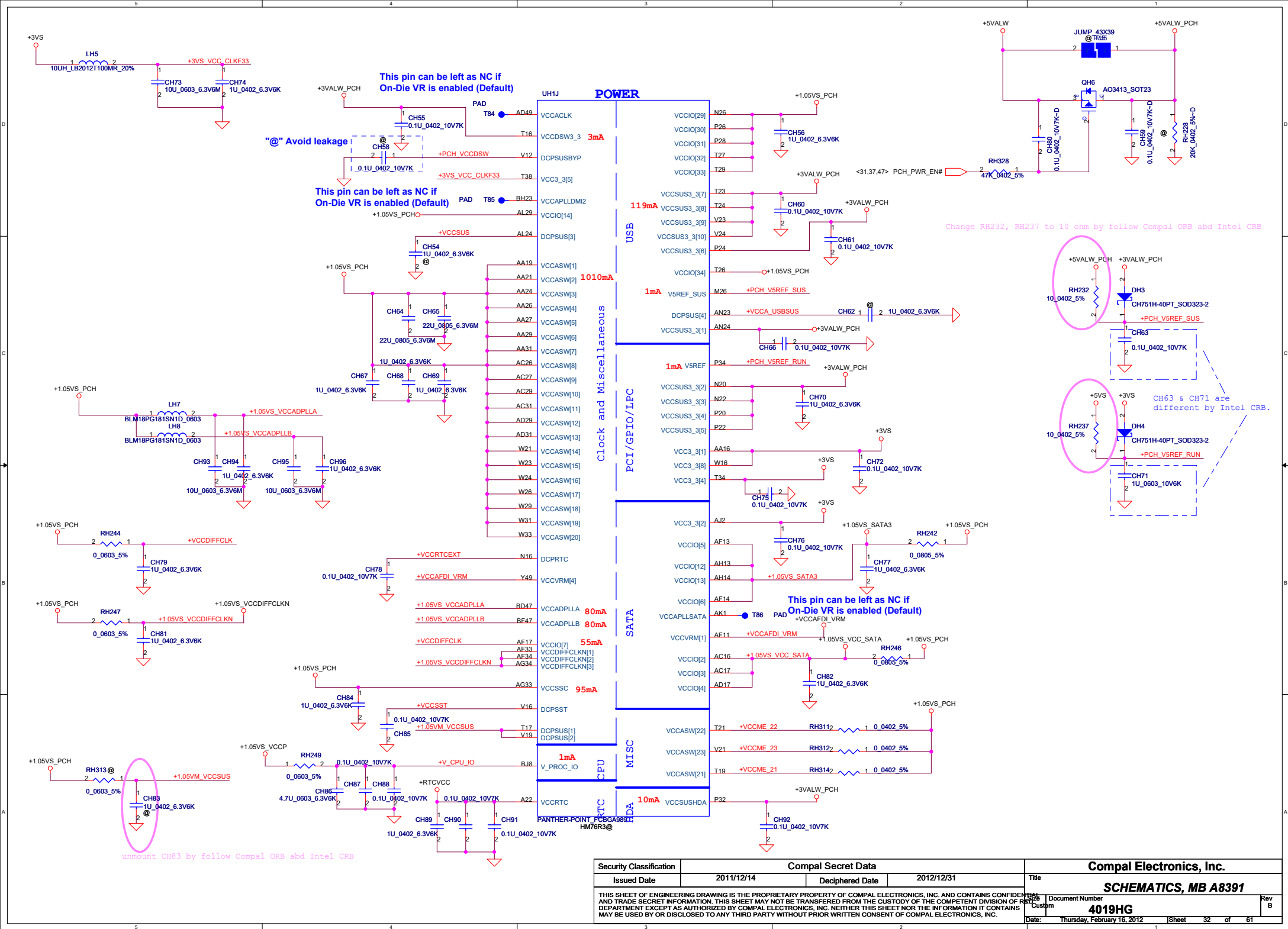




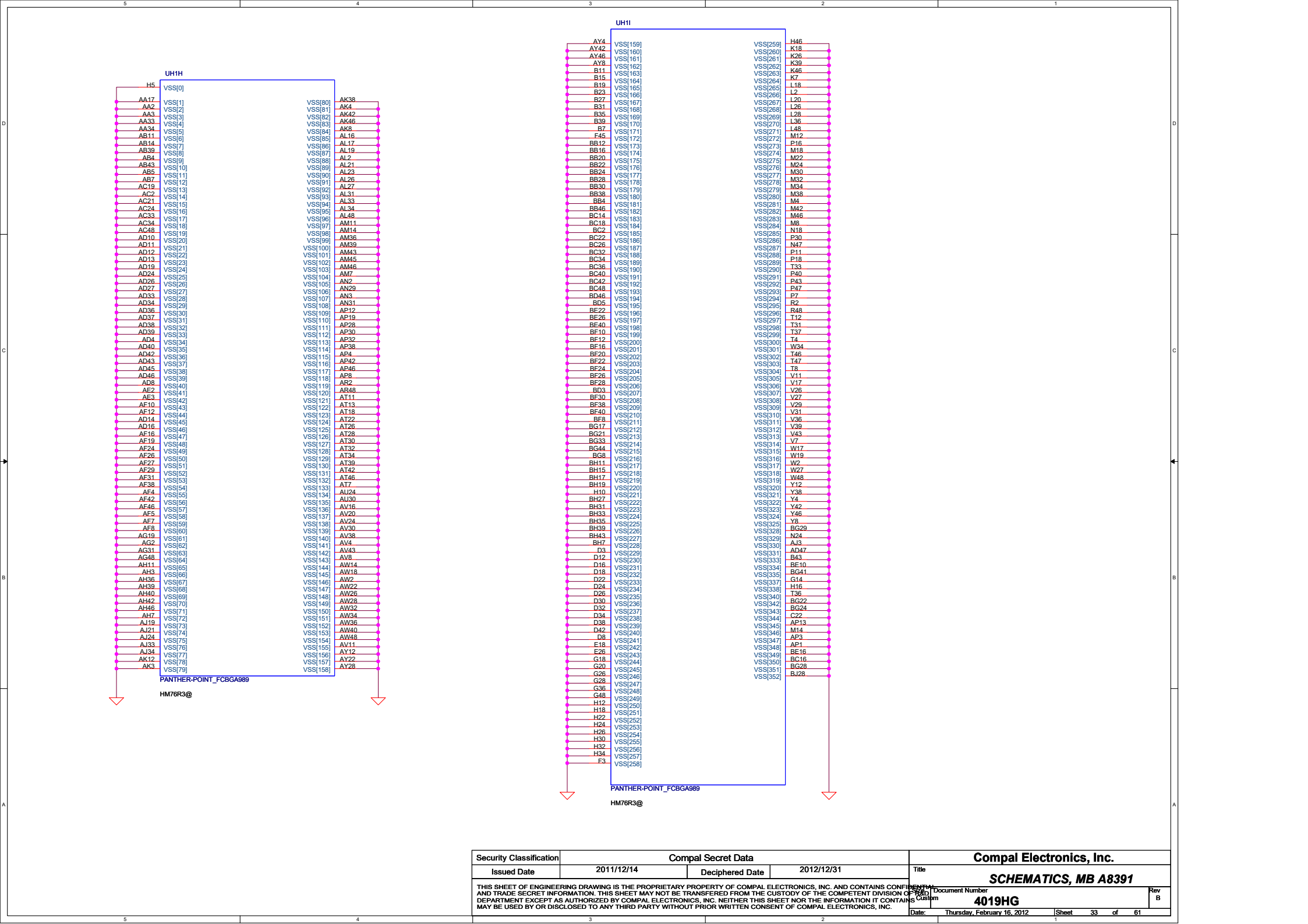






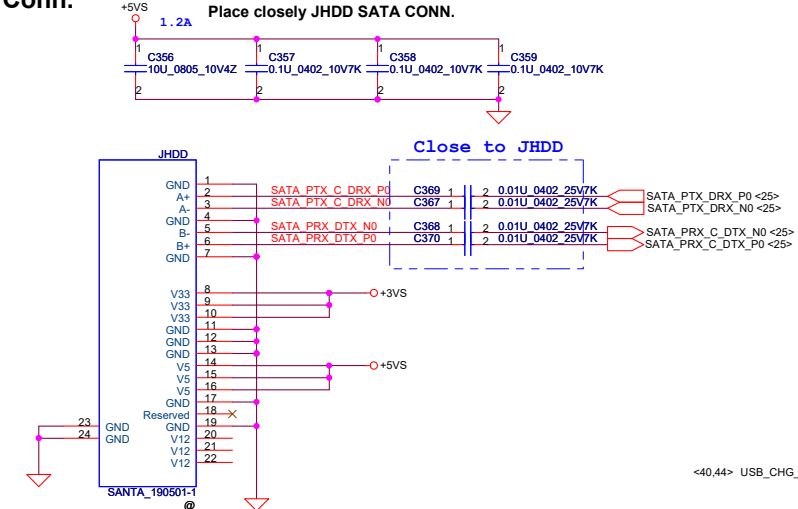


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				Document Number		4019HG	
				Date:		Thursday, February 16, 2012	
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				Rev B			

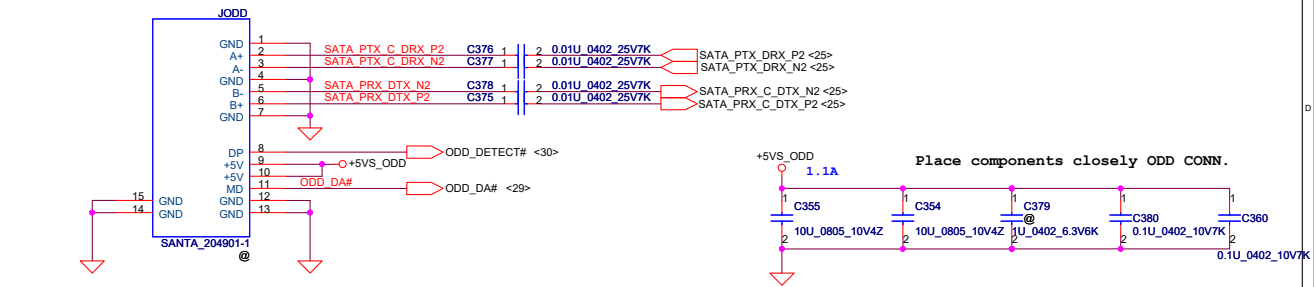


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Date:		Thursday, February 16, 2012		
		Sheet	33	of 61

SATA HDD Conn.

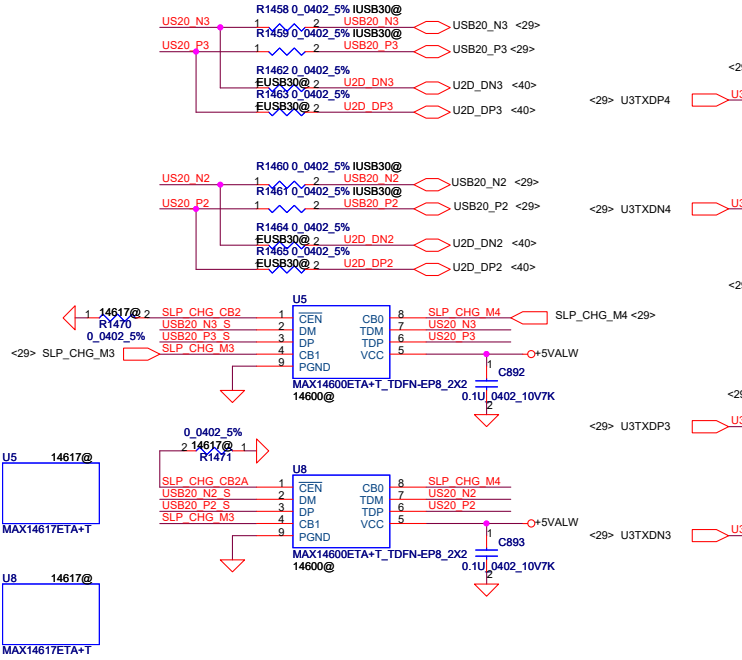


SATA ODD Conn

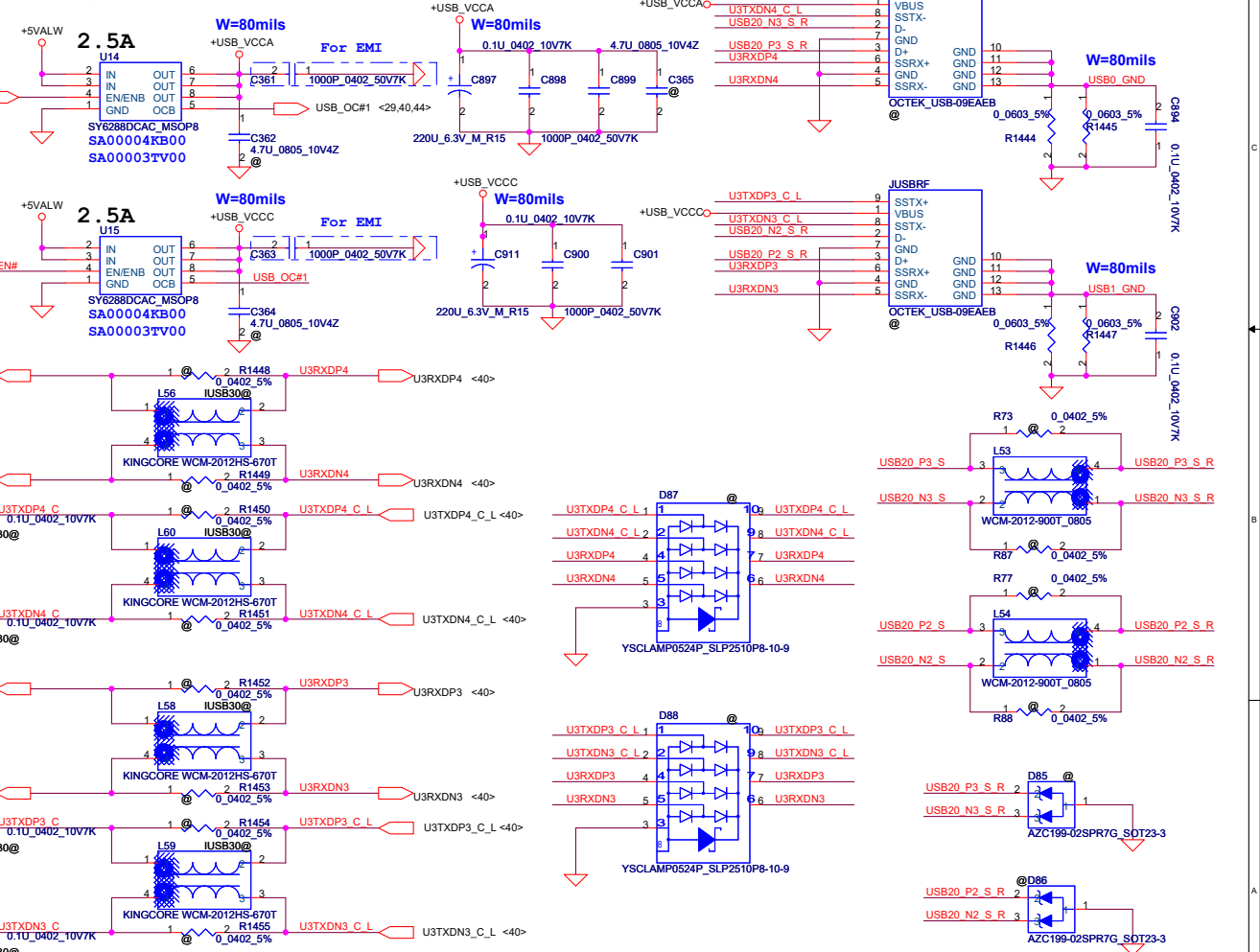


USB Sleep & Charge Auto-Mode/Mode3

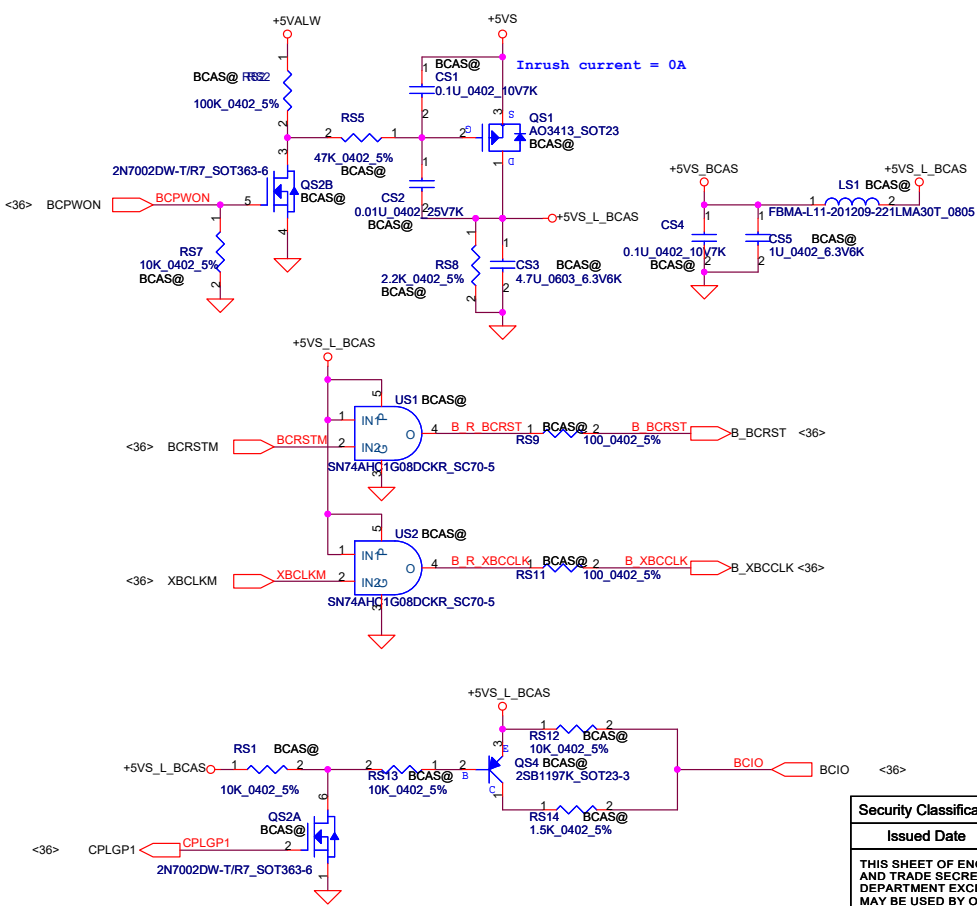
MAX14600 & MAX14617			
CB0 SLP_CHG_M4	CB1 SLP_CHG_M3	CB2 (14617 only)	STATUS
0	0	0	AUTO MODE
0	1	0	Force Dedicated charger mode (MODE3)
1	0	0	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM
1	1	0	Pass-Through (USB) Mode with CDP Emulation: Auto Connect DP/DM to TDP/TDM depending on CDP status
X	X	1	Force Apple 2A Charger Mode: Apple 2A resistor dividers



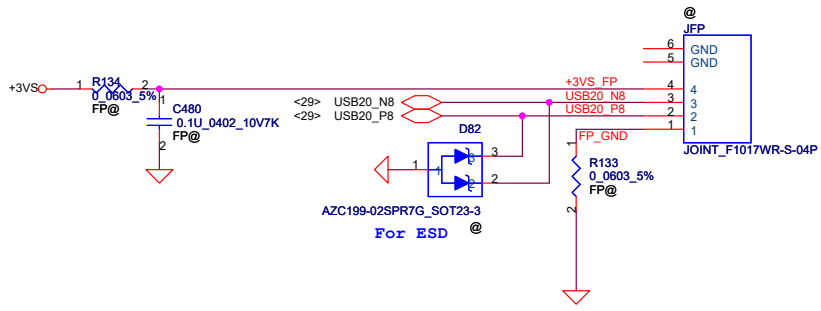
USB Right-Side



B-CAS Circuit

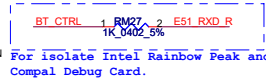
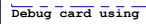


Finger printer

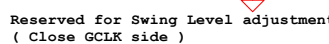


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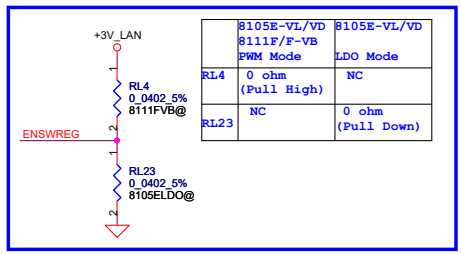
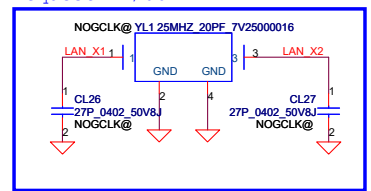
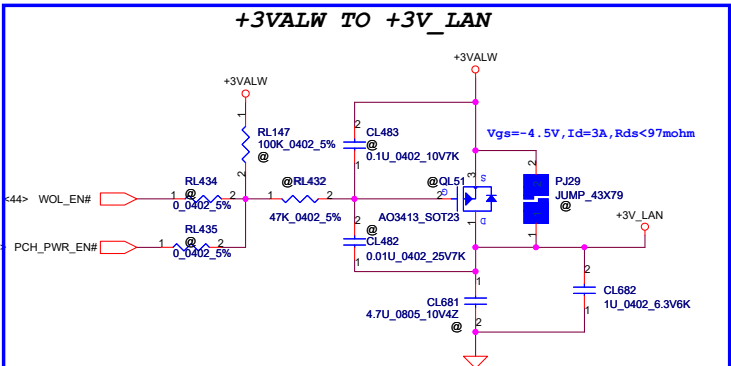
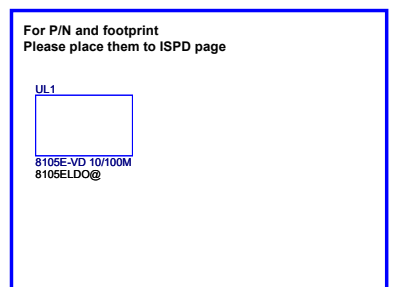
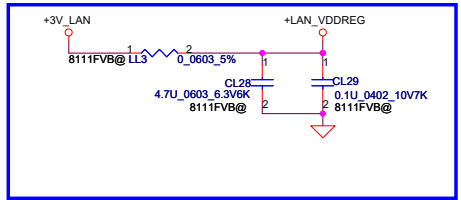
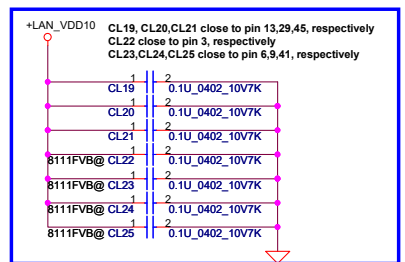
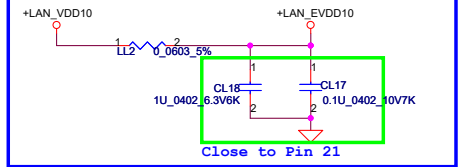
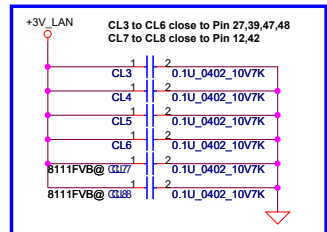
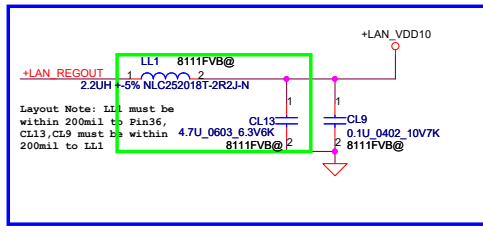
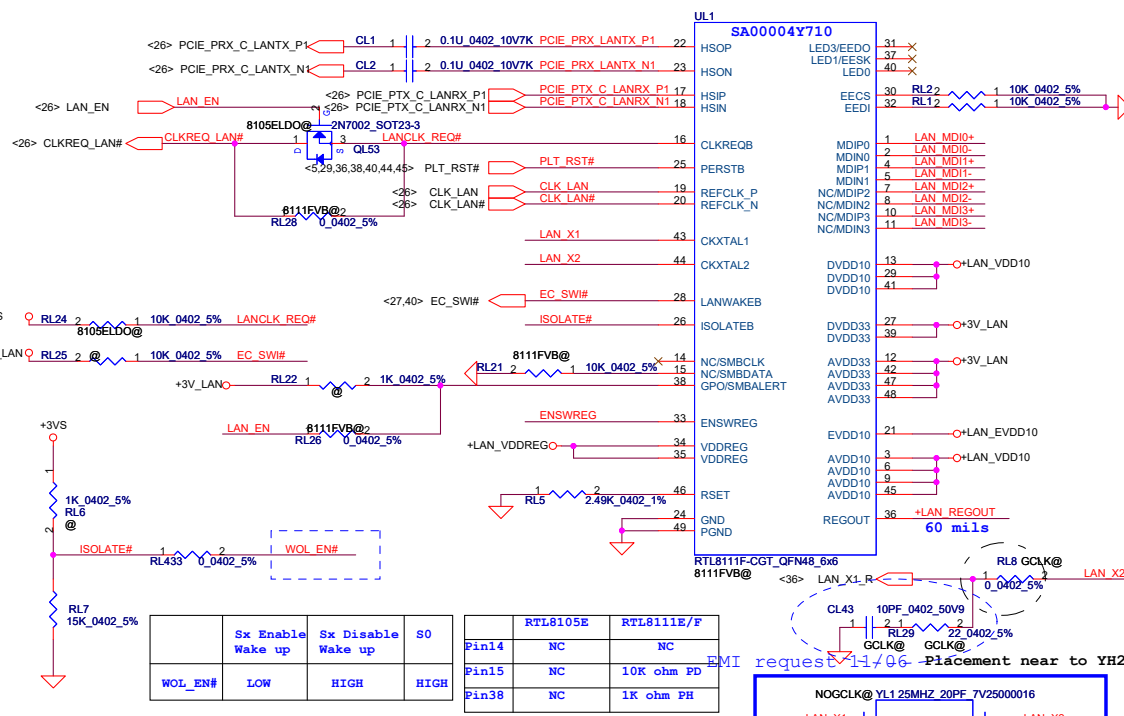
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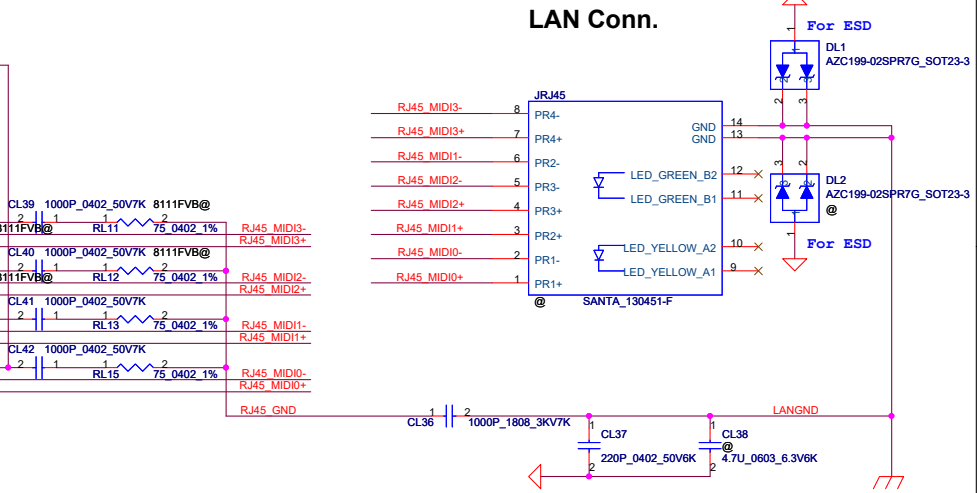
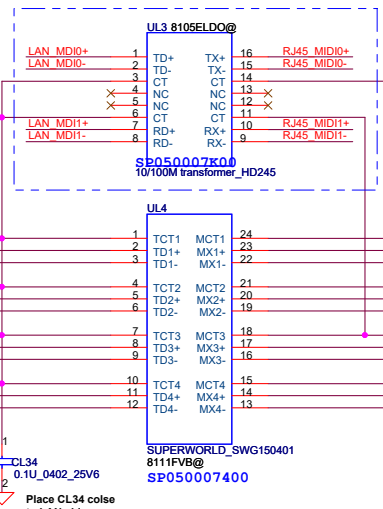


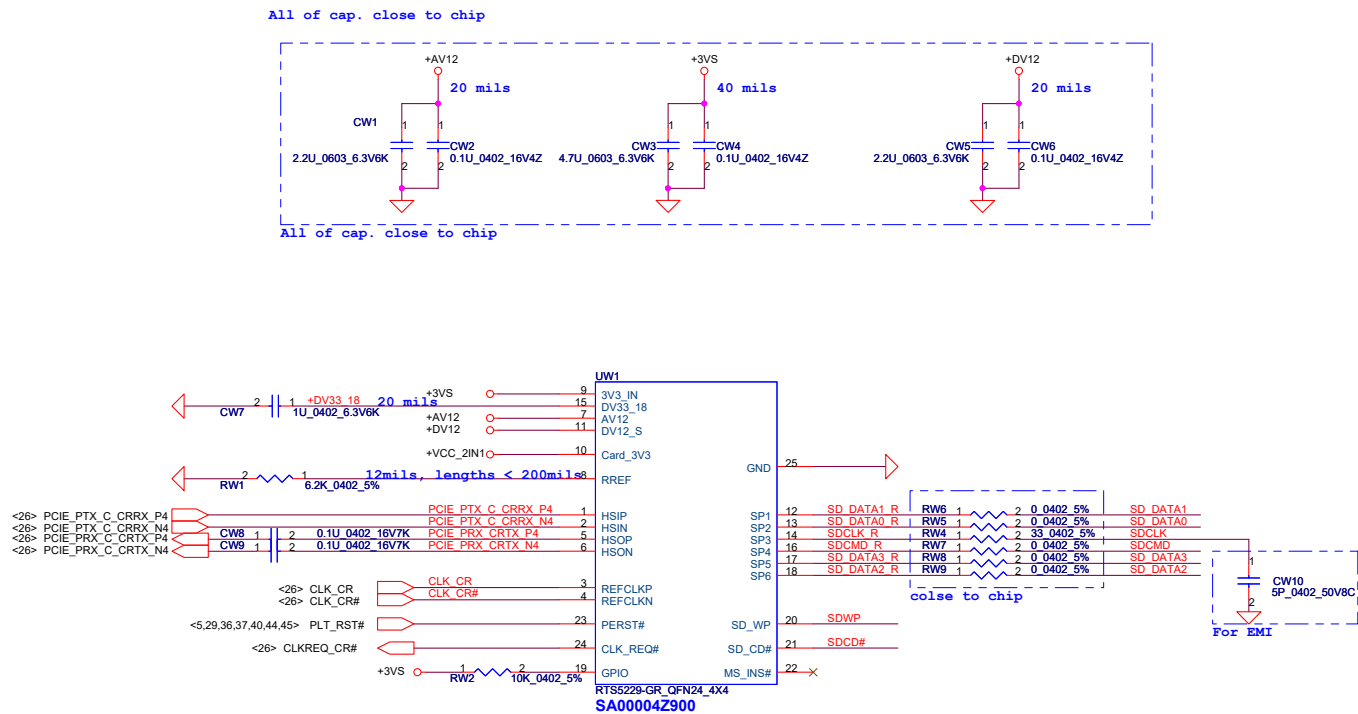
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+3V_LAN rising time (10%~90%) need > 1ms and <100ms.					
LAN	WOL	LAN_EN	ISOLATED	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

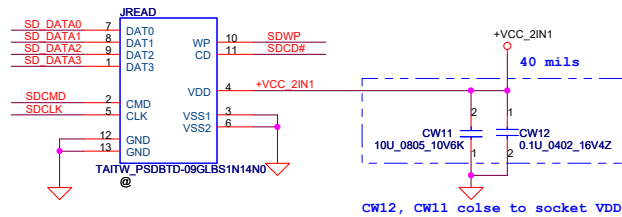
* S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms



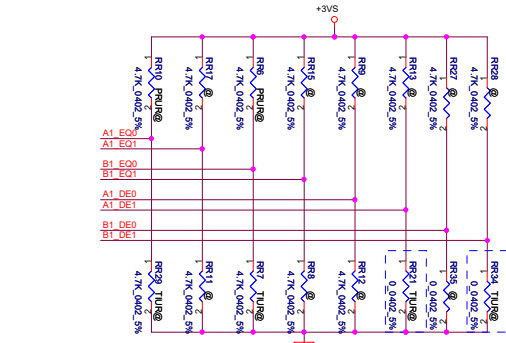


< 2 in 1 Card Reader >

Connector on bottom side



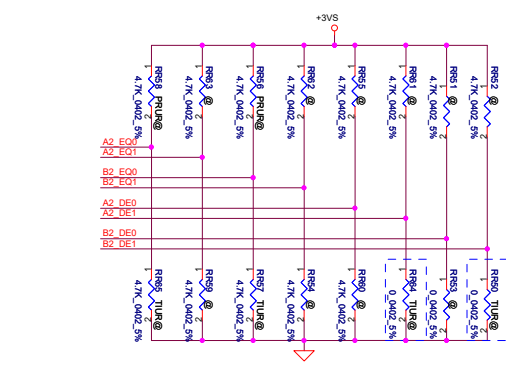
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- RR29 4.7K 0402_5% PCUR@
- RR7 4.7K 0402_5% PCUR@
- RR21 0.0402_5% PCUR@
- RR34 0.0402_5% PCUR@

Note:
 1) keep differential trace mismatch less than +/- 5mil
 2) keep USB3 impedance follow Intel SPEC
 3) Power / GND pin trace 10mil

TI: A_DE1, B_DE1 need 0ohm to GND.
 If use Parade and need control
 A_DE1 & B_DE1 please use 4.7K



- RR65 4.7K 0402_5% PCUR@
- RR57 4.7K 0402_5% PCUR@
- RR64 0.0402_5% PCUR@
- RR50 0.0402_5% PCUR@

TI: A_DE1, B_DE1 need 0ohm to GND.
 If use Parade and need control
 A_DE1 & B_DE1 please use 4.7K

REXT - swing pin(2.5K~10K)
 When test RX need add RR18

TI suggest EQ1(Pin2) & EQ2(Pin17) to pull Down use 7dB
 DE1(Pin3) & DE2(Pin16) NC use 0dB
 OS1(Pin4) & OS2(Pin15) NC use 1042mV

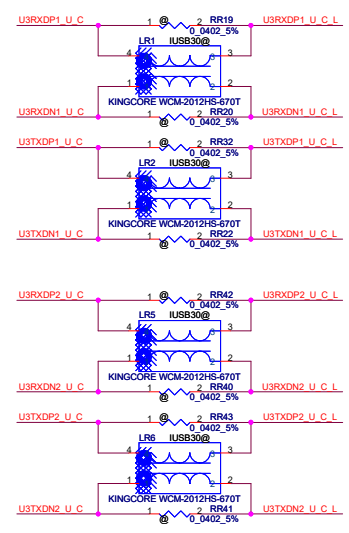
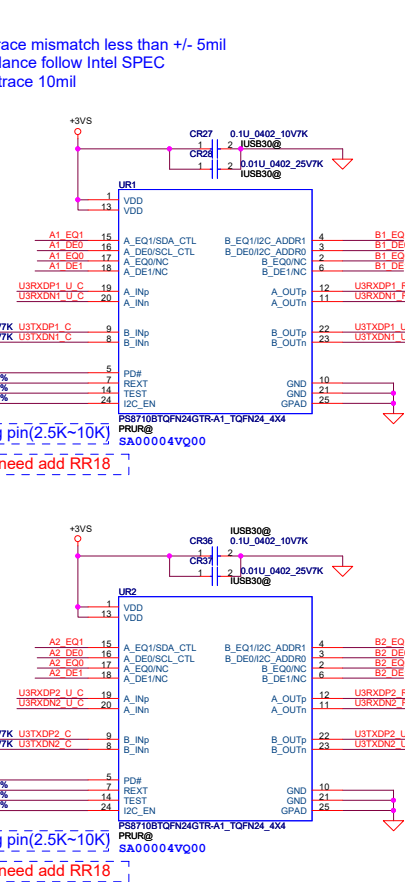
OUTPUT SWING AND EQ CONTROL (at 2.5GHz)			
OSx	TRANSISTION BIT AMPLITUDE (TVF mVpp)	EQx	EQUALIZATION (dB)
NC(default)	1042	NC(default)	0
0	908	0	7
1	1127	1	15
OUTPUT DE CONTROL (at 2.5GHz)			
DEx	OSx = NC	OSx = 0	OSx = 0
NC(default)	0 dB	0 dB	0 dB
0	-3.5 dB	-2.2 dB	-4.4 dB
1	-6.0 dB	-5.2 dB	-6.0 dB
CONTROL PINS SETTINGS			
EN_RXD	DEVICE FUNCTION	CM	DEVICE FUNCTION
1(default)	Normal Operation	0(default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode

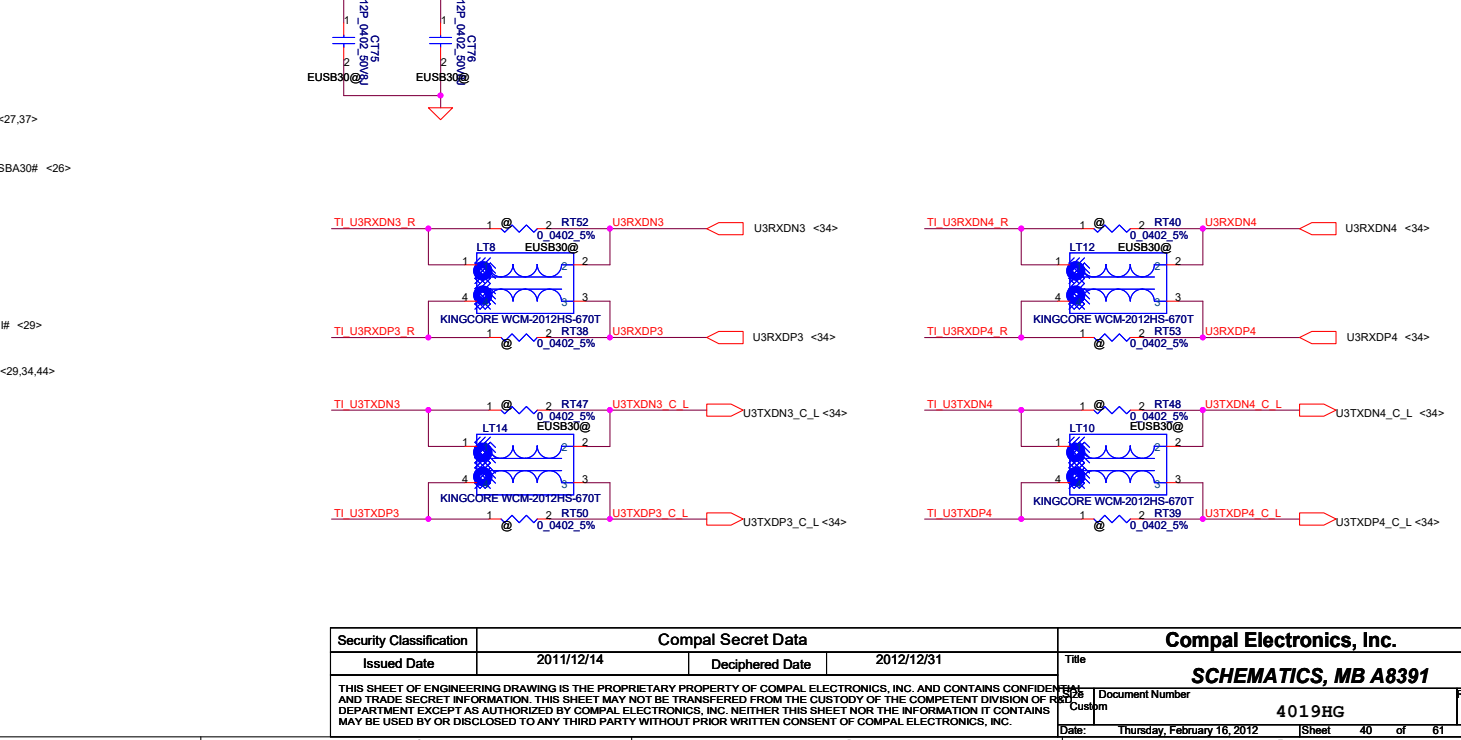
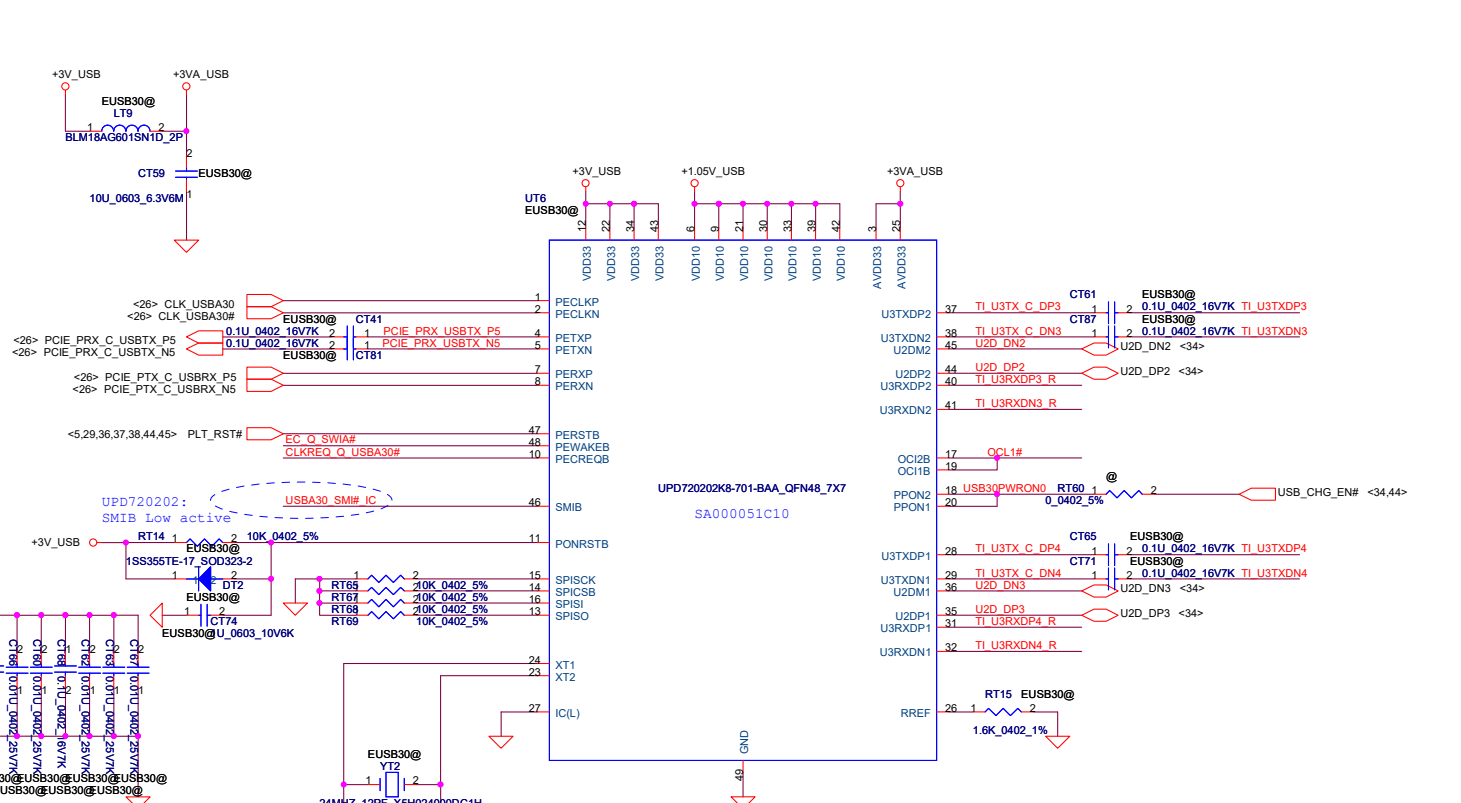
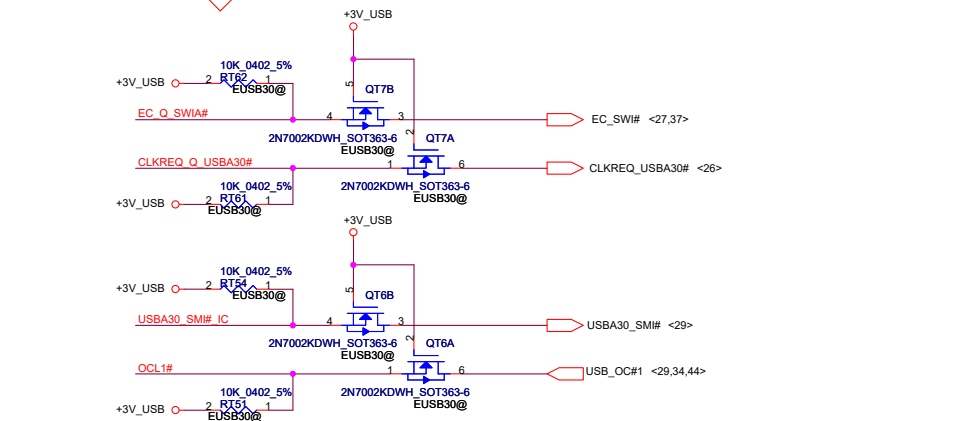
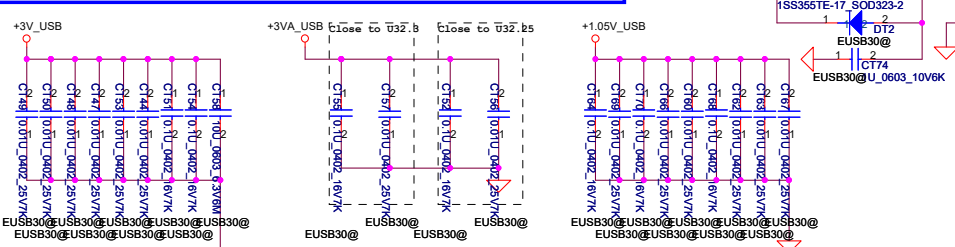
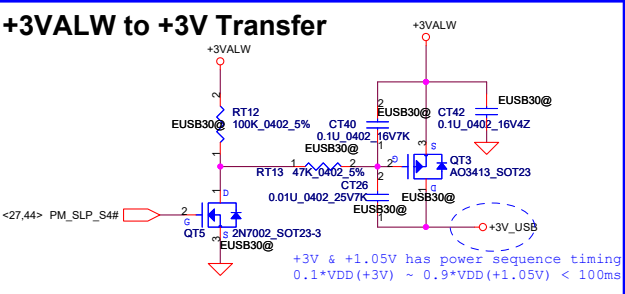
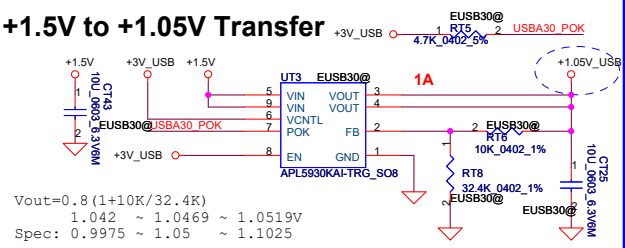
Parade suggest EQ1(Pin2) & EQ2(Pin17) to pull High use 7dB. All control has internally pulled down at ~150Kohm.
 If add ESD Diode A_DE0(Pin16) and B_DE0(Pin3) need pull high to 7dB otherwise 3dB

A_EQ1(Pin15)	A_EQ0(Pin17)	B_EQ1(Pin4)	B_EQ0(Pin2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
adaptive EQ enable Loss up to 7dB		adaptive EQ enable Loss up to 7dB	
Loss up to 14.5dB		Loss up to 14.5dB	
Loss up to 11.5dB		Loss up to 11.5dB	
A_DE1(Pin18)	A_DE0(Pin16)	B_DE1(Pin6)	B_DE0(Pin3)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
3.5dB		3.5dB	
No de-emphasis		No de-emphasis	
7dB		7dB	
5dB with boost output swing		5dB with boost output swing	

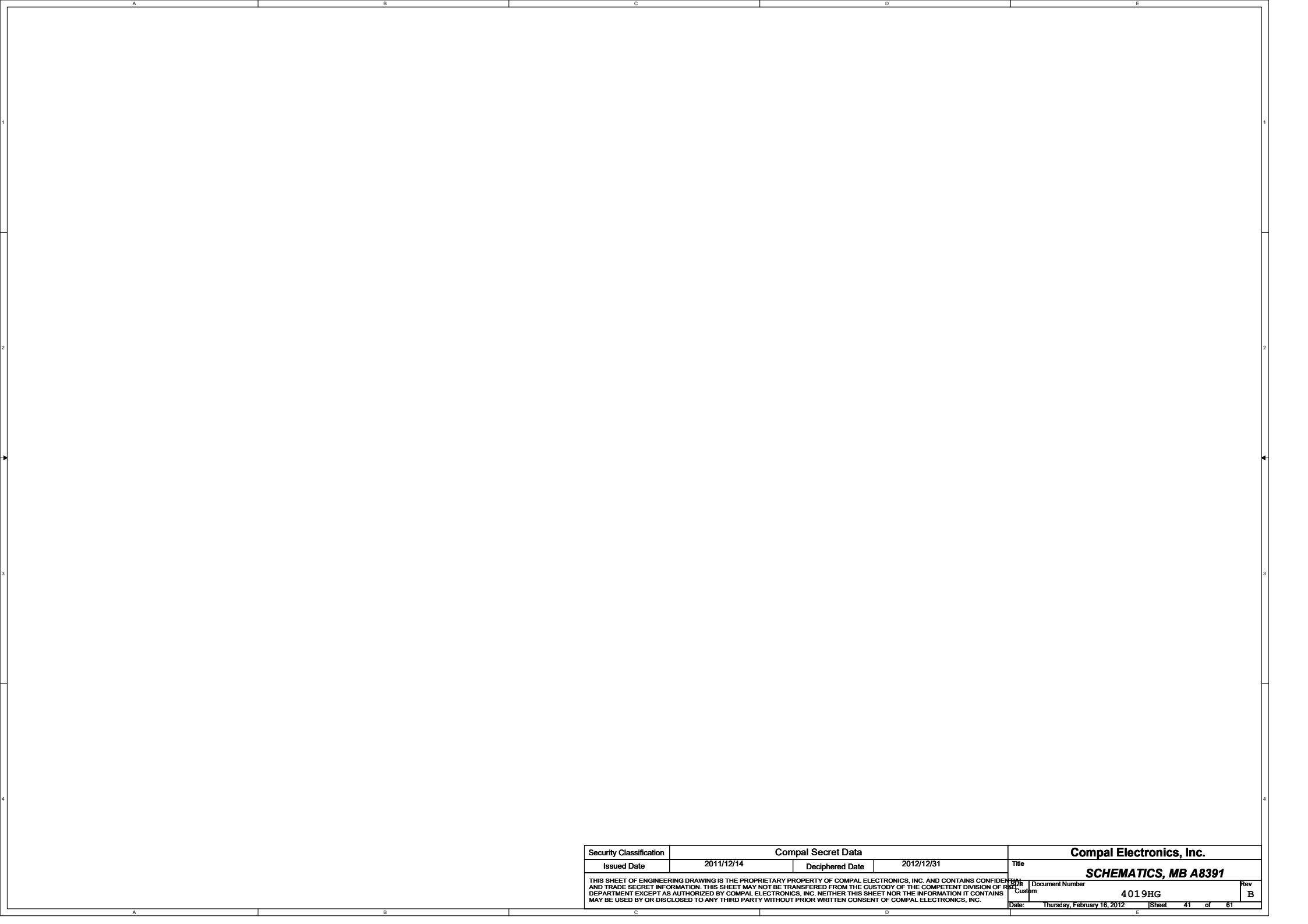
BOM Structure

Pericom	PCUR@
TI	TIUR@
Parade	PRUR@
USB3.0	USB30R@

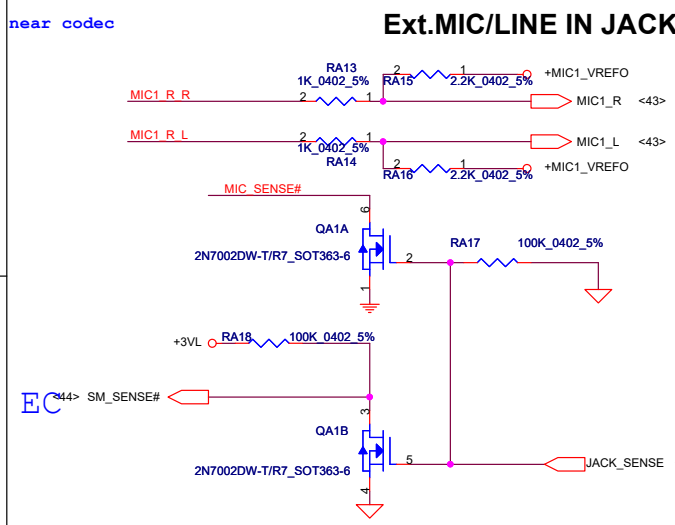
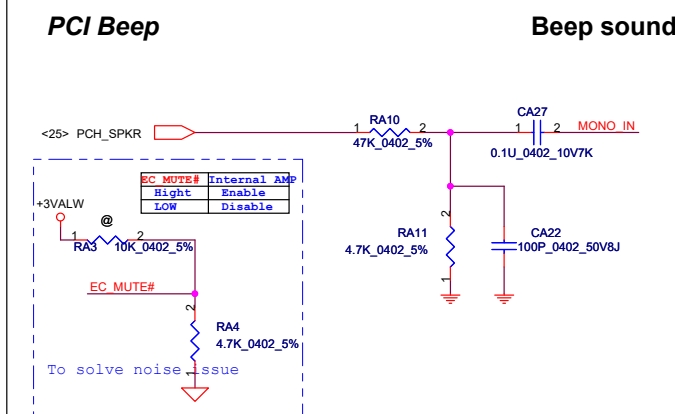
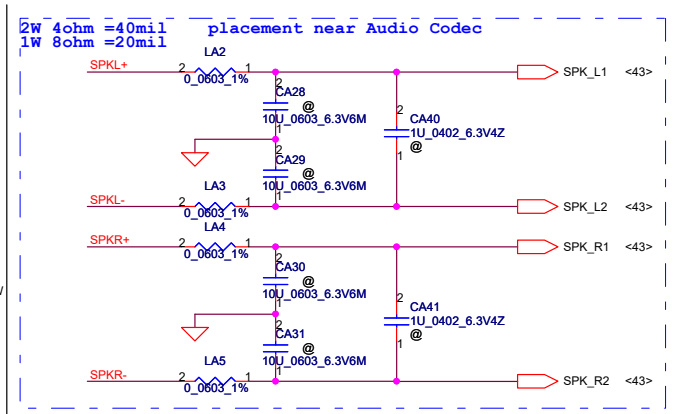
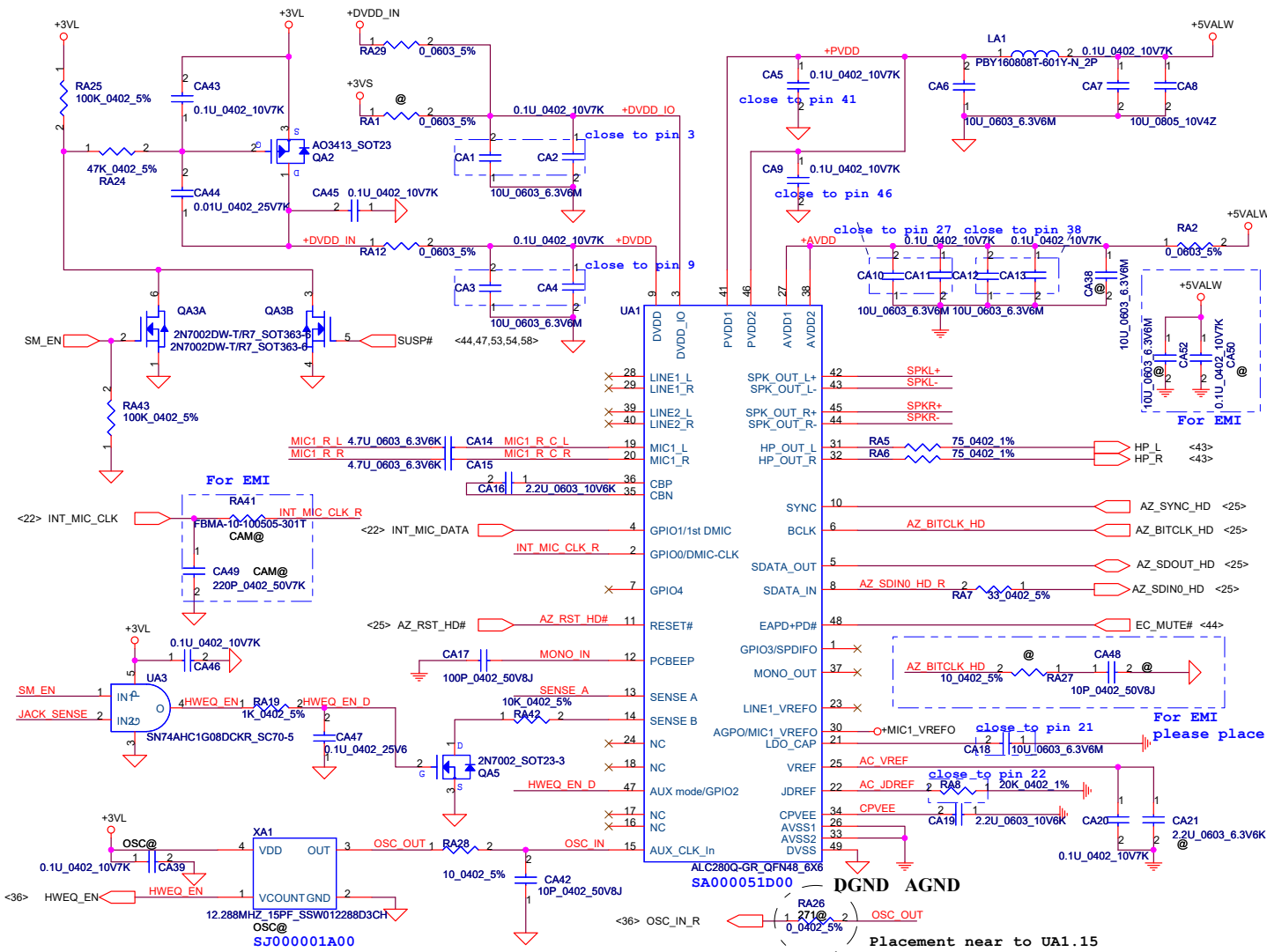




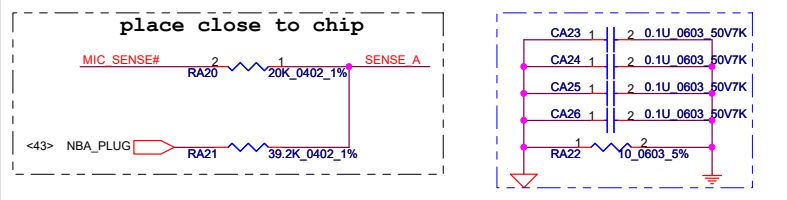
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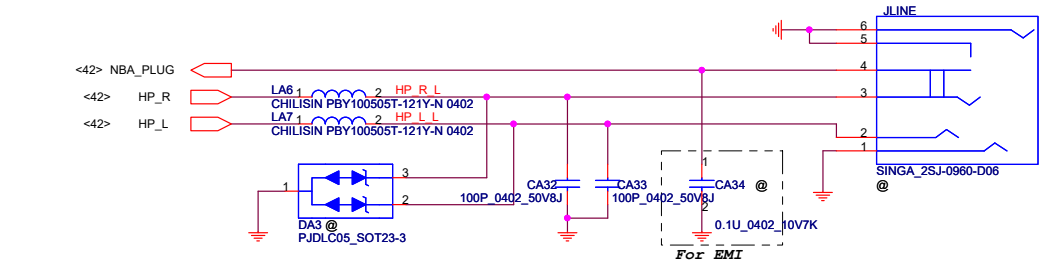
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								Item		Document Number		Rev	
								Custom		4019HG		B	
								Date:		Thursday, February 16, 2012		Sheet 41 of 61	



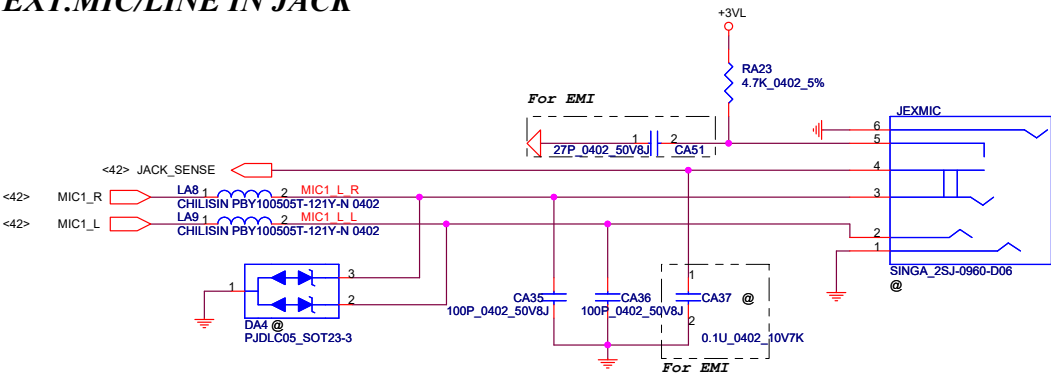
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 31, 32)	Headphone out
	20K	PORT-B (PIN 19, 20)	Ext. MIC
	10K	PORT-C (PIN 28, 29)	
	5.1K	PORT-E	
SENSE B	39.2K		
	20K		
	10K		



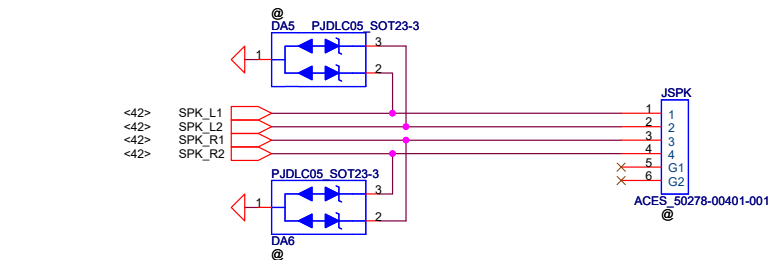
HeadPhone/LINE OUT JACK



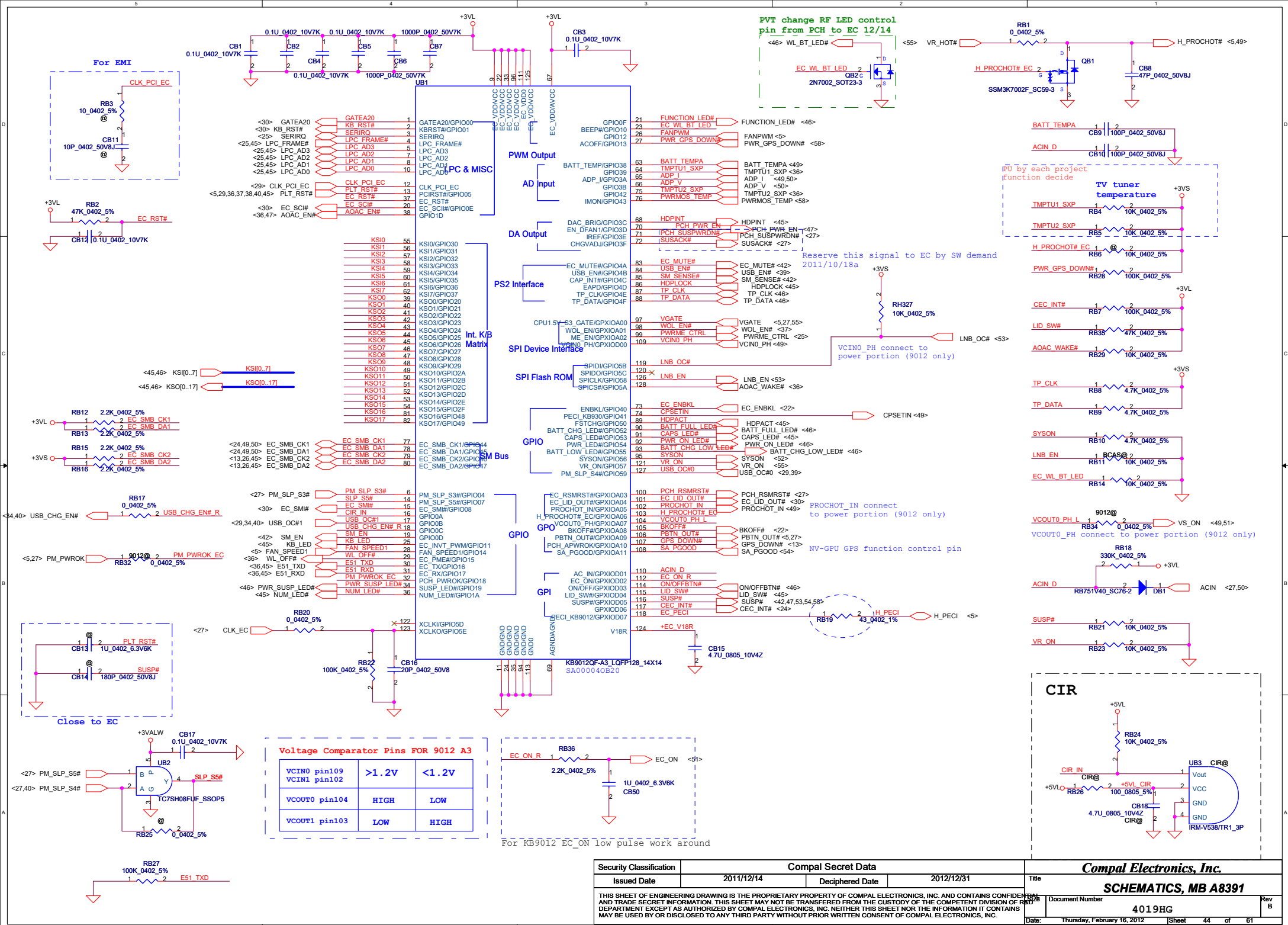
EXT.MIC/LINE IN JACK

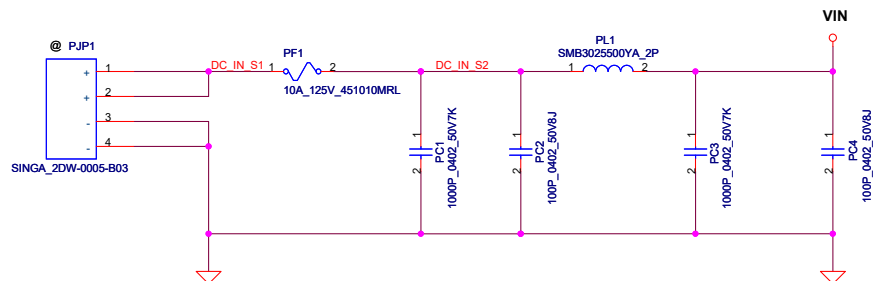


SPK CONN.

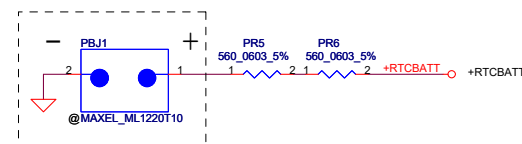


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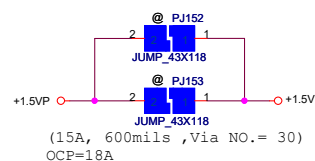
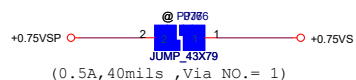
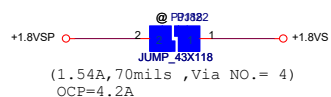
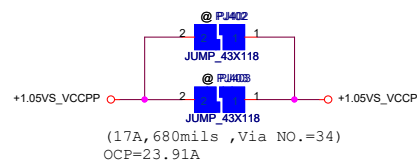
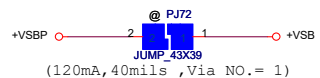
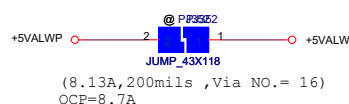
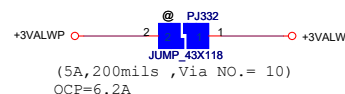
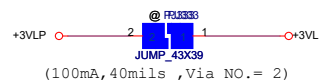




RTC Battery



SP093MX0000



ACIN

Precharge detector			
	Min.	typ.	Max
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

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PH1 under CPU botten side :

CPU thermal protection at 90 degree C
Recovery at 56 degree C

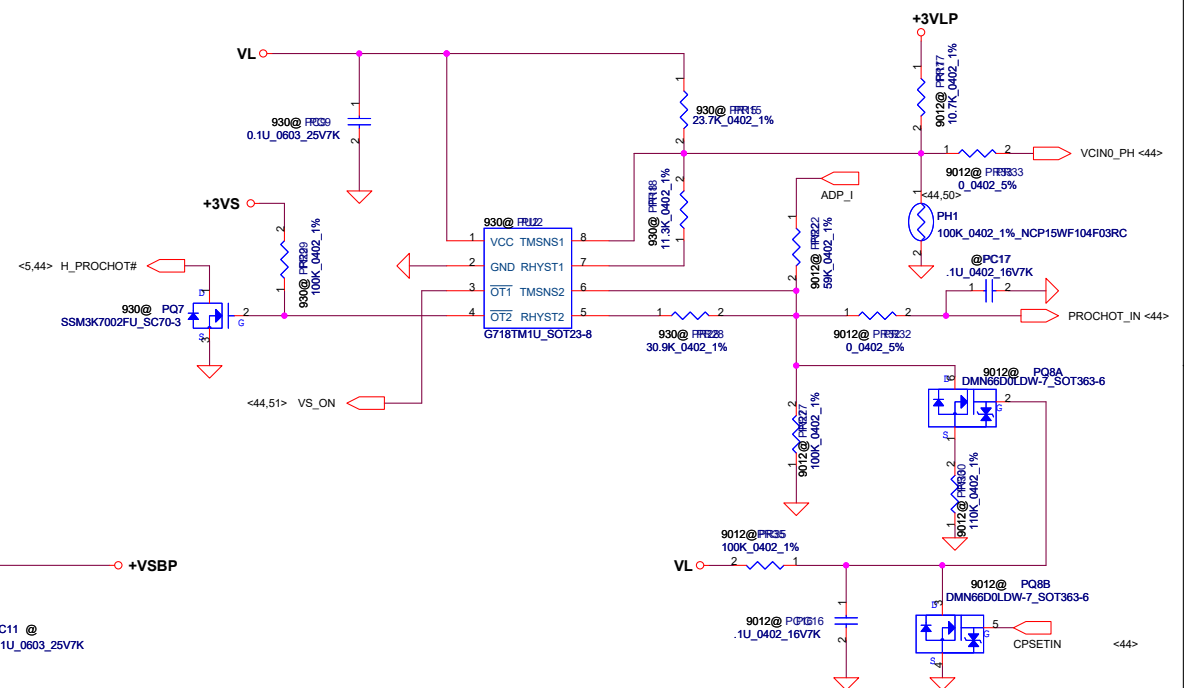
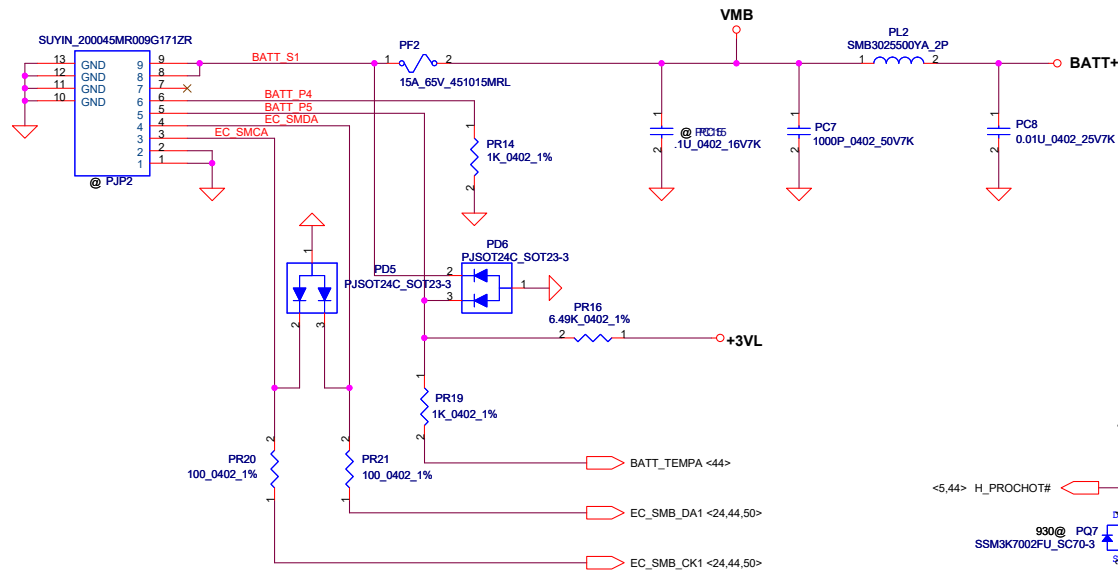
$$R_{set} = 3 * R_{tmh}$$

$$R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$$

$$R_{tmh} \text{ at } 90C = 7.87K, R_{tml} \text{ at } 56C = 26.1K$$

$$R_{set} = 3 * 7.87K = 23.61K \Rightarrow 23.7K$$

$$R_{hyst} = (23.7K * 26.1K) / (3 * 26.1K - 23.7K) = 11.33K \Rightarrow 11.3K$$



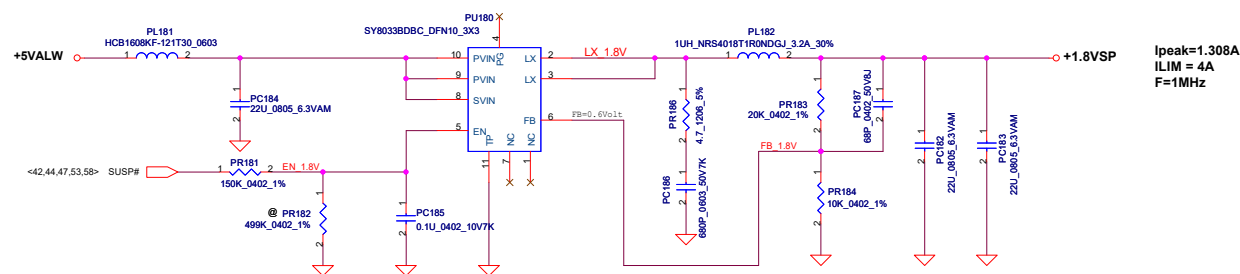
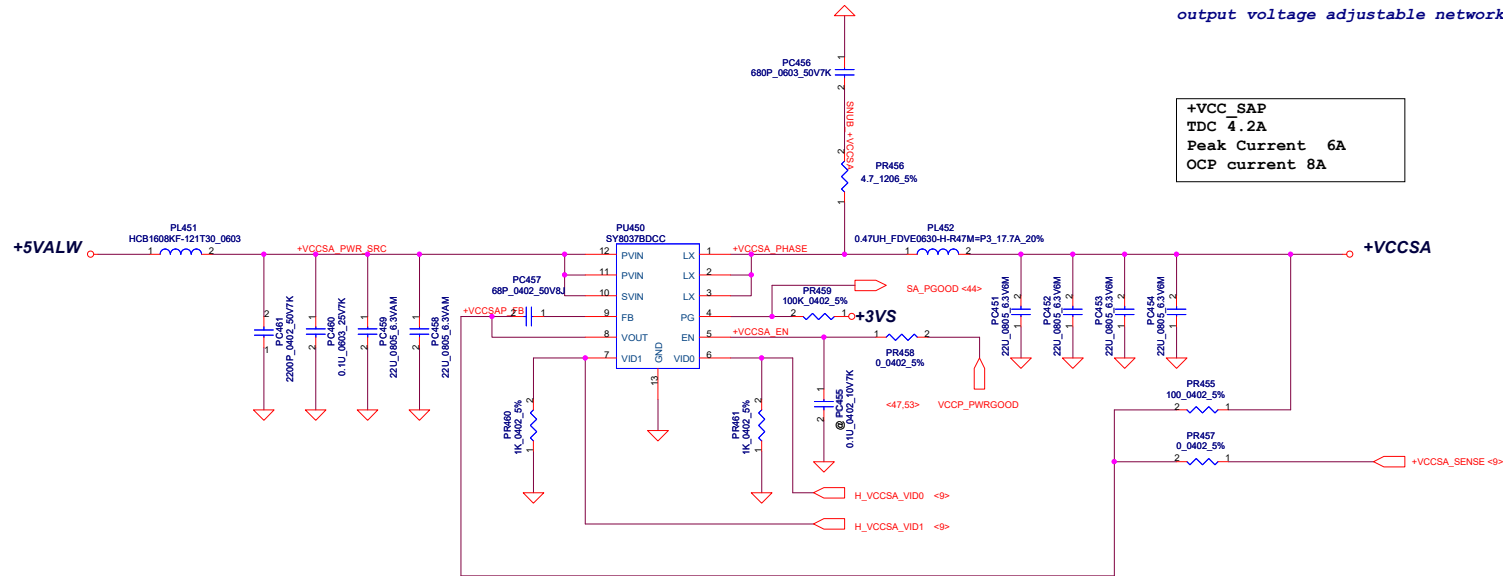
Adaptor protection				
Adaptor	Throttling point	ADP_I	Recovery point	ADP_I
90W	113.5W	1.783V	86.4W	1.357V
65W	71.8W	1.504V	62.5W	1.308V

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

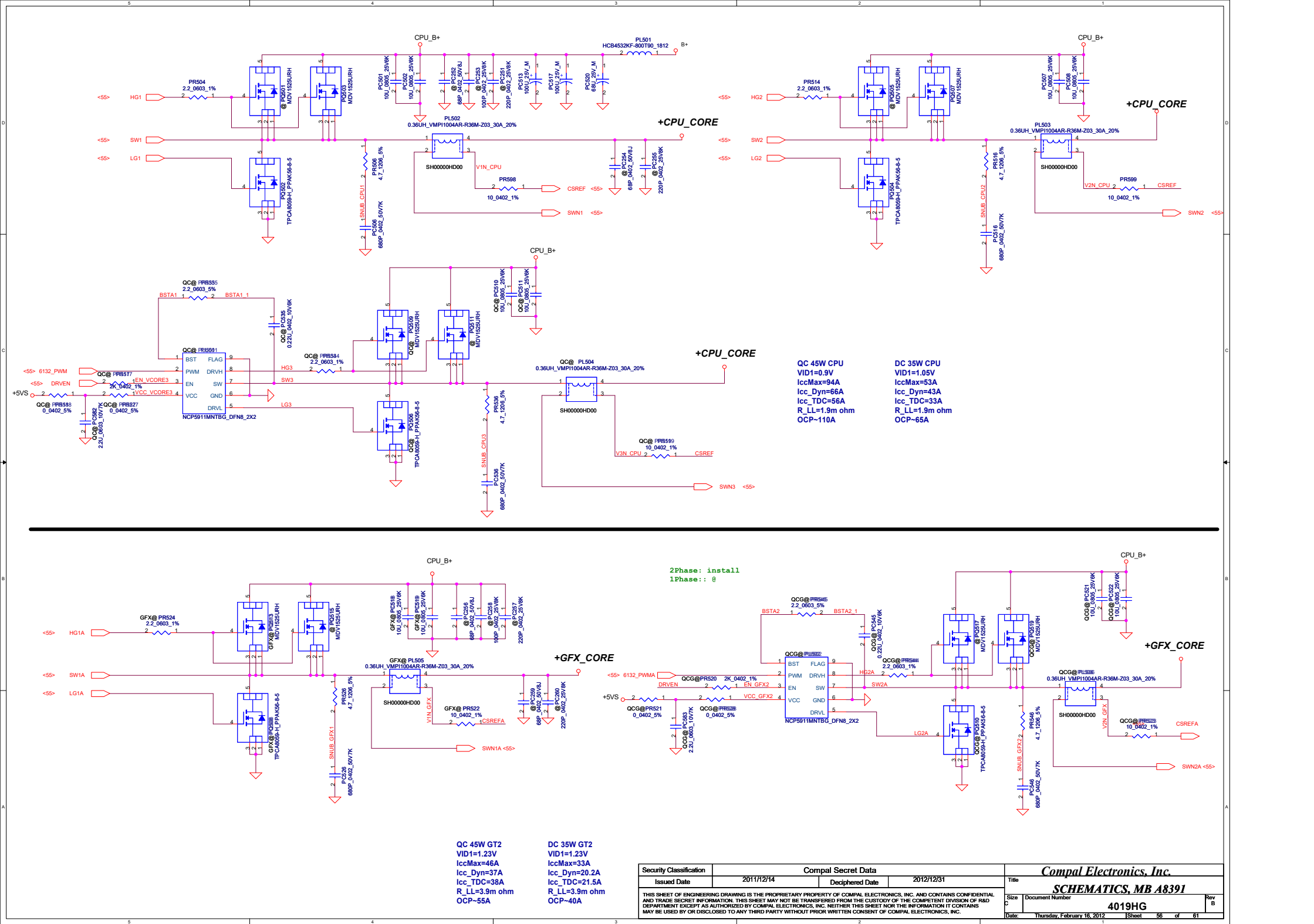
output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 8A

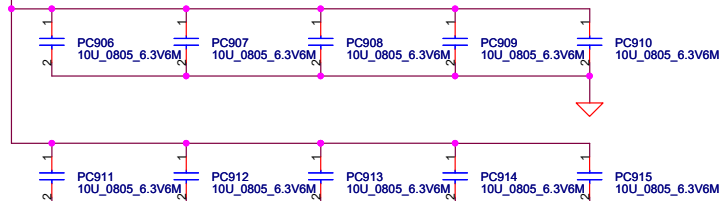




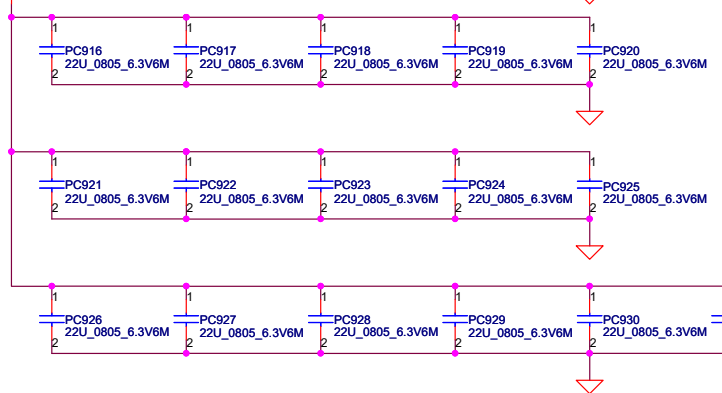
Date: Thursday, February 16, 2012 Sheet 55 of 61



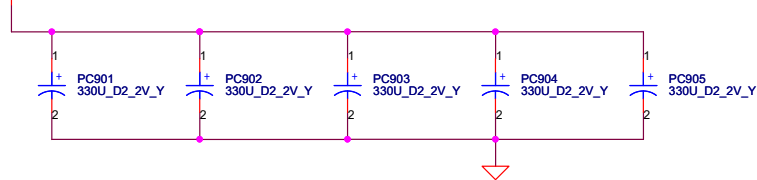
+CPU_CORE



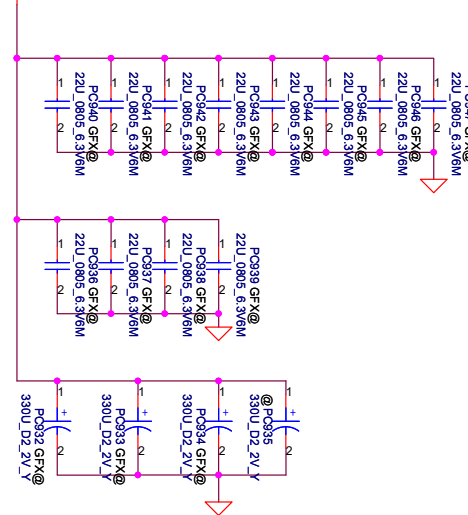
+CPU_CORE



+CPU_CORE



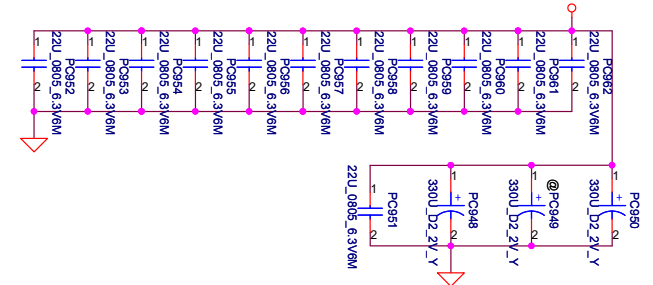
+GFX_CORE



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+1.05VS_VCCP



Chief River	330uF*9m	470uF*4.5m	22uF	10uF
8layer for DC CPU	4		16	10
8layer for QC CPU	5		16	10
6layer for DC CPU	5		16	10
6layer for QC CPU	4	1	16	10
GFX_CORE DC	2		12	
GFX_CORE QC	3		12	
1.05V_VCCP	2		12	

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NO DATE	PAGE	PARTITION LIST	PURPOSE
1.	2011/09/29	P51-PWR_+3VALWP/+5VALWP	Change PU330 to RT8205L
2.	2011/09/29	P53-PWR_+1.05VS VCCP/+16VSP	Change PU400 to RT8237C
3.	2011/09/29	P54-PWR_+VCCSAP/1.8VSP	Change PU450 to SY8037B
4.	2011/09/29	P57-PWR_+CPU_CORE DECOUPLING	Change HMOS to MDV1525
5.	2011/09/29	P53-PWR_+1.05VS VCCP/+16VSP	Change HMOS to MDV1525
6.	2011/09/29	P49-PWR_BATTERY CONN / OTP	Change PD5,PD6 to SCA00001G00
7.	2011/09/29	P57-PWR_+CPU_CORE DECOUPLING	Change PR589 from 348 to 8.06k
8.	2011/09/29	P57-PWR_+CPU_CORE DECOUPLING	Change PR590 from 3.65k to 806
10.	2011/09/29	P57-PWR_+CPU_CORE DECOUPLING	Change PC574 from 680P to 0.033u
11.	2011/09/29	P57-PWR_+CPU_CORE DECOUPLING	Change PC577 from 4700P to 0.033u
12.	2011/09/29	P57-PWR_+CPU_CORE DECOUPLING	Change PR548 from 1.21k to 8.06k
13.	2011/09/29	P57-PWR_+CPU_CORE DECOUPLING	Change PR550 from 10.7k to 806
14.	2011/09/29	P57-PWR_+CPU_CORE DECOUPLING	Change PC547 from 680P to 0.033u
15.	2011/09/29	P57-PWR_+CPU_CORE DECOUPLING	Change PC551 from 4700P to 0.033u
16.	2011/09/29	P57-PWR_+CPU_CORE DECOUPLING	Add snubber and boost resistor
17.	2011/09/29	P49-PWR_BATTERY CONN / OTP	Add PR22 120k,PR27 100k, PR32 0 Ohm
18.	2011/09/29	P58-PWR_VGA_CORE	Remove PC803, PC804 add PC806 47u
19.	2011/09/29	P51-PWR_+3VALWP/+5VALWP	Change PC360 to SE000006R80
20.	2011/09/29	P58-PWR_VGA_CORE	Change PC702 to SE00000H180
21.	2011/09/29	P49-PWR_BATTERY CONN / OTP	Add PR17 14k, PR33 0 Ohm
22.	2011/09/29	P51-PWR_+3VALWP/+5VALWP	Add PR373 0 Ohm
			Change source
			Change source
			Change source
			Change source
			Change source
			ESD team request
			F&E suggestion
			F&E suggestion
			F&E suggestion
			F&E suggestion
			F&E suggestion
			For 3x3 H-MOS solution
			For 120W adapter protect(9012)
			For Nvidia suggestion
			Change source
			Change source
			For CPU temperature protect(9012)
			For 3/5 V always power on(9012)

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HW PIR (Product Improve Record)

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REVISION CHANGE: 0.2

GERBER-OUT DATE: 2011/11/11

Item	Page	Date	Request	Solution
1)	44	2011/9/27	in order to add one AD channel for PWR VR protect of GPU GPS	change PWR GPS_DOWN# to EC GPIO43. change HDPACT to EC_GPIO50
2)	44	2011/9/27	in order to reduce BOM	change CB50 to SE000000K80
3)	15	2011/9/27	for N13PGL strap pin by NV review	modify VRAM Table change RV77 to @ due to it is for X76 change RV98 to @ for N13PGL change RV76 to @ for N13PGL change RV73 to 45.3k (SD034453280) for N13PGL change RV89 to 34.8k (SD034348280) for N13PGL change RV89 to 30k (SD034300280) for N13PGL change RV73 BOM sstructure to N13PGS@(34.8K) & N13PGL@(45.3K) change RV54 to @ change RV79 BOM astructure to N13PGS@(20K) & N13PGL@(10K) change RV76 to 10K and N13PGS@ change RV98 to GSDIS@ change RV75 to GSOPT@ change D84 to SCA00001L00 change D82 to SCA00001L00 change D92 to SCA00001L00
4)	15	2011/9/28	for N13PGL strap pin by NV review	reserve decoupling cap CC66, CC67, CC70 for H_PM_SYNC & H_PECI, BUF_CPU_RST#
5)	15	2011/9/28	for N13PGS strap pin by NV review	add LVDS dual channel signal add LVDS dual channel signal and 0ohm: R267 R268 R269 R270 R283 R329 R333 R337 (OPTFHD@) and R500 R501 R502 R503 R504 R505 R507 R508 (3D@) add RH277 BOM structure : OPTFHD@ add unused Dual MOS: Q7B,Q6B change RV89 to 10k (SD034100280) for N13PGL change RC79 from @ to always mount change Function_LED from EC_GPIO4D, PIN86 to EC_GPIO11, PIN25 change HDPLOCK from EC_GPIO11, PIN25 to EC_GPIO4D, PIN86 add GPUPWR_SKIN# on EC_GPIO13, pin27 change PWRMOS_TEMP from EC_GPIO50, PIN89 to EC_GPIO43, PIN76 change HDPACT from EC_GPIO43, PIN76 to EC_GPIO50, PIN89 change RB28 pin1 from PWR_GPS_DOWN# to GPUPWR_SKIN# reserve SUSACK# and PCH_SUSPWRDN# by SW demand change PCH_SUSPWRDN_R to PCH_SUSPWRDN#_R add PCH_SUSPWRDN# to EC and RH132 remove T75 change SUSACK# to SUSACK#_R add RH133 and SUSACK# to EC add JTP connector Pin 5 (PM_SMBCLK) , Pin6 (PM_SMBDATA) add RM15 and RM16 reserve for TV tuner (BCAS) reserve RA43 for SM_EN 100K pull down reserve exchange location of RA28 and CA42 RA26 pin2 change name from OSC_IN to OSC_OUT delete DA1. add RA19 ,QA5 ,RA42 , delete CH57 ,PJ3 then add PJ5, QH6, CH59, RH228 add R5545, Q5527, R5529, R5534 R434 change from 220K to 330K change net name from DGPU_PWR_EN# to VGA_PWROK# reserve RH228 change D21 power from +5VL to +5VALW add EC pin 70 for PCH_PWR_EN delete RH287 for NV sequence RH175 change to always mount delete RH174 and RH1 change PCH D44 ball add RH326 for LNB_OC# pull high exchange CA42 and RA28 location add RT67 RT68 RT69 RT70 RT72 RT73 reserve CCL10 for EMI request reserver RL29 CL43 for EMI request PCH pin F46 and RH299 chagne net name from WL_OFF# to PCH_GPIO55 change EC pin 29 net name from CPSETIN to WL_Off# add R5546 for WL_OFF# pull high to +3V WLAN CPSETIN signal change from EC pin 29 to EC pin 74 add RH327 pull high to +3VS for LNB_OC# change YCL1 from SJ10000CU00 to SJ10000EF00, CCL4 and CCL5 from 30pF to 15pF change BOM structure of RV54 from @ to N13PGS@ change R460 from 470ohm to 22ohm change BOM structure of CCL10 from @ to GCLK@ change BOM structure of RL29, CL43 from @ to GCLK@
6)	22	2011/9/29B	by ESD demand	
7)	35	2011/9/29B	by ESD demand	
8)	37	2011/9/29B	by ESD demand	
9)	05	2011/10/05A	follow HW4 check list	
11)	28	2011/10/05A	by Customer demand	
12)	22	2011/10/05A	by Customer demand	
13)	26	2011/10/05A	by Customer demand	
14)	47	2011/10/05A	follow HW4 check list	
15)	15	2011/10/18a	by NV demaend	
16)	10	2011/10/18a	for PEG reversal	
17)	44	2011/10/18a	discuss with EC	
18)	27	2011/10/18a	by SW ME demand	
19)	46	2011/11/1	new touch pad add new function	
20)	36	2011/11/1	TV tuner(BCAS) 16V reserve	
21)	42	2011/11/1	avoid SM_EN floating	
22)	42	2011/11/1	for vendor request	
23)	42	2011/11/1	for vendor request	
24)	42	2011/11/1	for vendor request, S&M HP need shut down	
25)	32	2011/11/2	for lot6 0.5W power consumption	
26)	47	2011/11/2	for lot6 0.5W power consumption	
27)	47	2011/11/3	for NV power sequence	
28)	47	2011/11/3	for NV power sequence	
29)	32	2011/11/3	for lot6 0.5W power consumption	
30)	46	2011/11/3	for lot6 0.5W power consumption	
31)	44	2011/11/7	for lot6 0.5W power consumption	
32)	29	2011/11/7	for NV sequence	
33)	29	2011/11/7	for NV sequence	
34)	29	2011/11/7	for TV tuner 16VS over current Pin	
35)	29	2011/11/7	for TV tuner 16VS over current Pin	
36)	29	2011/11/7	for TV tuner 16VS over current Pin	
37)	42	2011/11/9	for vendor request	
38)	40	2011/11/9	for vendor request	
39)	36	2011/11/9	for EMI request	
40)	37	2011/11/9	for EMI request	
41)	29	2011/11/9	EC common core for WL_OFF#	
42)	44	2011/11/9	EC common core for WL_OFF#	
43)	36	2011/11/9	EC common core for WL_OFF#	
44)	44	2011/11/9	EC common core for WL_OFF#	
45)	44	2011/11/9	LNB_OC# change from PCH pin D44 to EC pin 119	
46)	36	2011/11/15	for vendor demand	
47)	15	2011/11/15	for NV recommend	
48)	47	2011/11/15c	for NV DG demand	
49)	36	2011/11/15d	by EMI demand	
50)	37	2011/11/15d	by EMI demand	

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HW PIR (Product Improve Record)

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REVISION CHANGE: 0.3

GERBER-OUT DATE: 2011/12/22

Item	Page	Date	Request	Solution
1)	27	2011/11/29a	For DVT hang	Add CH23 CH24 CH25 for SW-node noise.
2)	13	2011/11/29a	For ME request	Change location from JLVD5 to JLVD54
3)	47	2011/12/05a	For reduce Rds-on of +VRAM_1.5VS	Add Q44
4)	05	2011/12/07a	For leakage	Change from +3VALM to +3VALM_PCH of UC1
5)	44	2011/12/13a	For design change	Change LNB_EN from PCH to EC and delte RH315, add RB11
6)	24	2011/12/13a	For HDMI leakage	Change Pin 5 of U9 from +5VL to +HDMI_5V_OUT
7)	44	2011/12/13a	For design change RF LED control pin	Change RF_LED control pin from PCH to EC.
8)	35	2011/12/15a	For ME request	Change +FFV/JPOWER/JFON from +if to non-+if
9)	40	2011/12/15a	For adjust EXT USB3.0 sequence	Change +3V to +3V_USB control pin from syson to PM_SLP_S4#
10)	41	2011/12/15a	For adjust EXT USB3.0 sequence	Change +3V to +3V_USB control pin from syson to PM_SLP_S4#
11)	22	2011/12/17a	For prevent LVDS burn issue	Add F3 (Poly fuse to prevent burn)
12)	46	2011/12/19a	For ME delete stand-off	Delete H25,H26,H27
13)	46	2011/12/19a	For Wimax flash issue	Change +5VS to +3VS of Wimax_LED
14)	46	2011/12/19a	For layout request	Add net name +5VS_FUNC With Function conn power pin
15)	15	2011/12/20a	For NV request	Change RV76 from 10K to 20K
16)	46	2011/12/21a	For power rail change	Change WIMAX_LED power rail from +5VS to +5VALM
17)	16	2011/12/22a	For NV request	Change LV6 from bead to 4.3ohm resistor
18)	29	2011/12/22a	For EMI request	Add CH29 for EMI request

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REVISION CHANGE: 1.0

GERBER-OUT DATE: 2012/02/02

Item	Page	Date	Request	Solution
1)	36	2012/01/12a	For GCLK	Add CCL13(0.1u) for +3VALM
2)	15	2012/01/12a	For NV suggestion	Change RV 76 from 20K to 45K(Support GEN3)
3)	36	2012/01/12a	For MSATA pin define.	Add RM30 (MSATA define that pin22 is reserve, so other function need to add PLT_RST#).
4)	36	2012/01/18a	For GCLK	Change CCL13 from +3VLAW to +3VALM_GCLK
5)	41	2012/01/30a	For TV tuner use PCIE interface	Add RM31-RM35 and QM2
6)	26	2012/01/30a	For TV tuner use PCIE interface	Change PCIE 6 from USB to TV tuner
7)	26	2012/01/30a	For TV tuner use PCIE interface	Change CLK_USB30 to CLK_TV and CLKREQ_USB30# to CLKREQ_TV#
8)	11	2012/01/30a	For MI only	Unmount RC117/RC118/qc7/Qc8
9)	46	2012/01/30a	For MP	Unmount SW3
10)	15	2012/01/30a	For NV suggestion	Change RV 73 to 5K
11)	43	2012/01/30a	For EMI request	Add CA51
12)	41	2012/01/30a	For Internal USB30 only	Delete Page 41

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