


LCFC Confidential

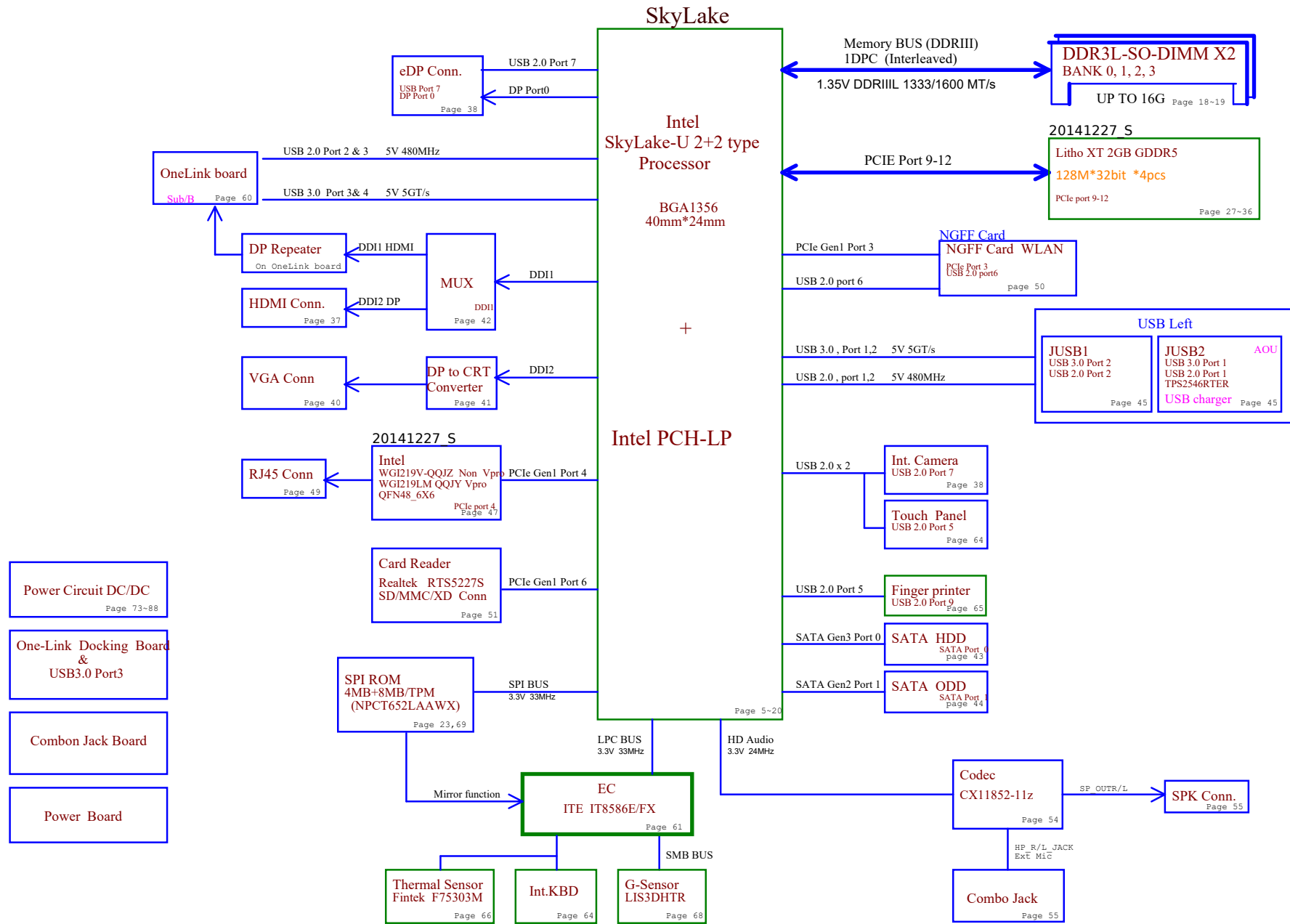
BE560 Rev1.0 Schematic

Intel SkyLake Processor with DDRIII + PCH-LP
AMD Litho XT GDDR5 2GB
2015-07-28 Rev1.0

<http://www.repair1.ru/>

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/11/04	Deciphered Date	2014/09/07	COVER PAGE	
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				Custom	BE560
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				Rev	0.1





Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW +1.8VALW +1VALW	+1.35V	+5VS +3VS +VCC_CORE +VCC_IO +VCC_SA +VCC_ST +VCC_STG +VGA_CORE +3VS_VGA +1.8VS_VGA +1.35VS_VGA +0.675VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON2	EC_ON	SUSP#
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF

SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY	G sensor
EC_SMB_CK1 EC_SMB_DA1	IT8580F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8580F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	X	V +3VALW_GS
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	V +3VS	X	X	X	V +5VS	V +3VS	X	X
PCH_SML0_CLK PCH_SML0_DAT	PCH +3V_PCH	X	X	X	X	X	X	X	X	V +3VALW	X

USB2 Port

Port	Device
1	JUSB2
2	JUSB3
3	Sub Board
4	Docking
5	Touch Panel
6	BT
7	CMOS
8	FP/Smart

USB3 Port

Port	Device
1	JUSB2
2	JUSB3
3	Sub Board
4	Docking
5	3D CCD (PCIe1)

PCIe Port

Port	Device
1	3D CCD (USB3)
2	X
3	WLAN
4	LAN
5	X
6	CardReader
7	X
8	X
9	GPU
10	GPU
11	GPU
12	GPU

SATA Port

Port	Device
1	HDD
2	ODD
3	X
4	X

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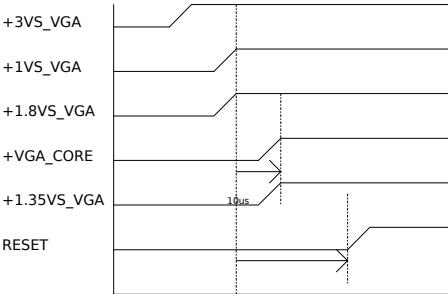
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Issued Date	2013/11/04	Deciphered Date	2014/09/07	NOTE LIST	
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Rev 0.1

VGA and DDR3 Voltage Rails (Litho XT 2GB DDR3) 20141227_S

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	N/A	
GPIO5	IN	-	GPIO5_AC_BATT
GPIO6	IN	-	GPIO6
GPIO7	OUT	N/A	
GPIO8	OUT	-	GPIO8_ROMSO
GPIO9	OUT	-	GPIO9_ROMSI
GPIO10	OUT	-	GPIO10_ROMSCK
GPIO11	OUT	N/A	
GPIO12	OUT	N/A	
GPIO13	OUT	N/A	
GPIO15	IN	N/A	SVI2_SVD
GPIO16	OUT	N/A	
GPIO17	OUT	N/A	
GPIO19	OUT	N/A	GPIO19_CTF
GPIO20	IN	IN	GPIO20
GPIO21	OUT	N/A	
GPIO22	OUT	N/A	GPIO22_ROMCSB
GPIO29	OUT	N/A	
GPIO30	OUT	N/A	



1. all power rail ramp up time should be within 20ms

	Device ID		setting	I2C Slave addresses ID
JET-XT	0xFFFF	SMB_ALT_ADDR (ROM_SO Bit 1)	0	0xFF
			1	0xFF

BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
XDP@	Debug port
UMA@	UMA SKU ID
DIS@	Optimus SKU ID
DIMM2@	For DIMM2 function
DIMM1@	For DIMM1 function
VPRO@	For VPRO function
ME@	ME Connector
EMC@	For EMC function
EMC_2D@	For EMC function
EMC_NS@	For EMC function
RF_NS@	For RF function
S2G@	For VRAM Strap
CHA@	For VRAMA function
CHB@	For VRAMB function
RANKA@	GPU DDR5 Setting
X76@	GPU VRAM Setting
3DCCD@	3D Camera Setting
VGA@	VGA Setting
MUX@	MUX Setting
ODD@	ODD Setting
TPM@	Trusted Platform Module (TPM)
NVPRO@	For Non-VPRO function
MIRROR@	For mirror function

GPU		Litho XT 2GB DDR3	
FB Memory (DDR3L)		PS_3 (RV114)	PS_3 (RV117)
Samsung 1000MHz	K4W4G1646D-BC1A		
	256Mx16	PH 3.4K	PD 10K
Hynix 1000MHz	H5TC4G63AFR-11C		
	256Mx16	PH 4.75K	NC
Micro 1000MHz	MT41J256M16HA-093G		
	256Mx16	PH 3.24K	PD 5.62K

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[SKL PDG]H_THERMTRIP# goes active, the CPU is indicating an overheat condition, and the PCH will immediately transition to an S5 state. CPU_GP can be used from external sensors for the thermal management.

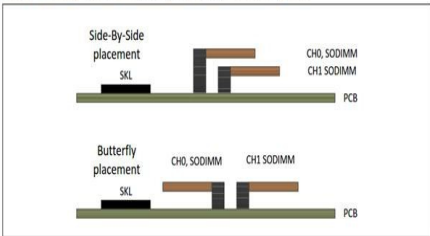
[SKL PDG]PROC_OPI_RCOMP: Signal should be pulled down to ground with a resistance of 50 ohm
[SKL PDG]PCH_OPI_RCOMP: Signal should be pulled down to ground with a resistance of 50 ohm

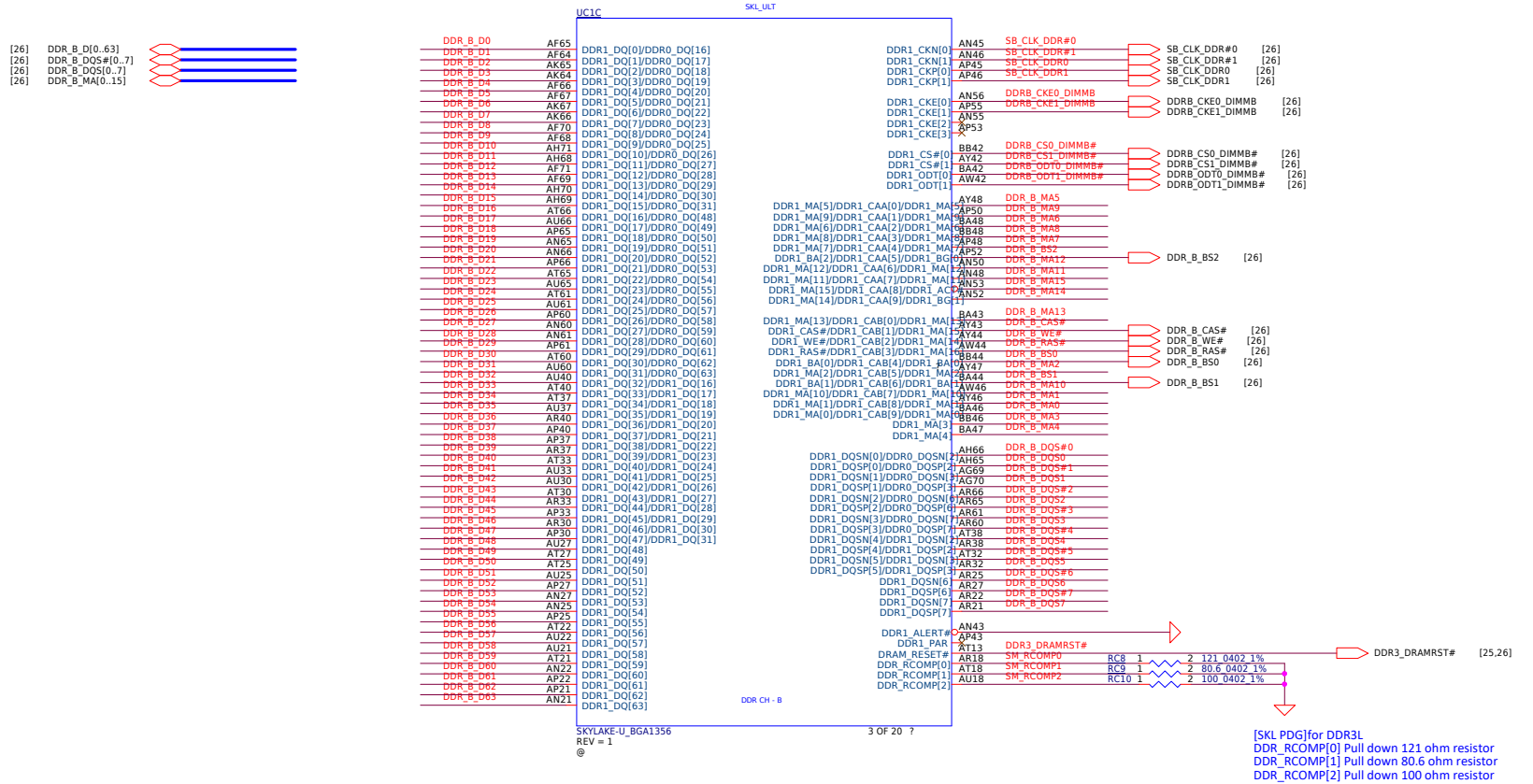
[SKL PDG]On Package Interface Compensation (OPI) Guidelines
- Should be referenced to VSS plane only. VSS reference planes must be continuous
- Require low DC resistance routing <0.2 ohm
- Avoid routing next to clock pins or noisy signals.

[SKL PDG]Refer Figure 45-1

[SKL PDG]Refer Figure 45-1

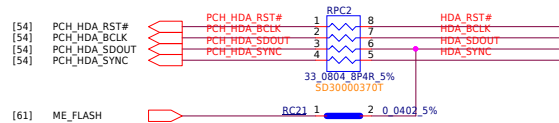
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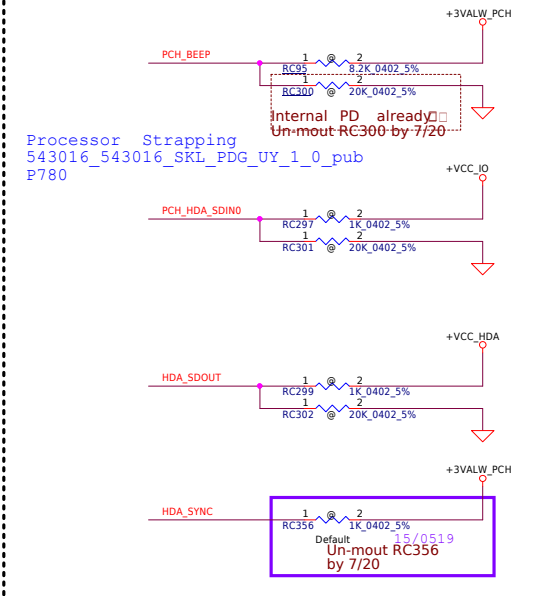


[SKL PDG] Manufacturing Mode Jumper

1. If strap is sampled low, the security measures defined in the Flash Descriptor will be in effect (default)
2. If sampled high, the Flash Descriptor Security will be overridden.



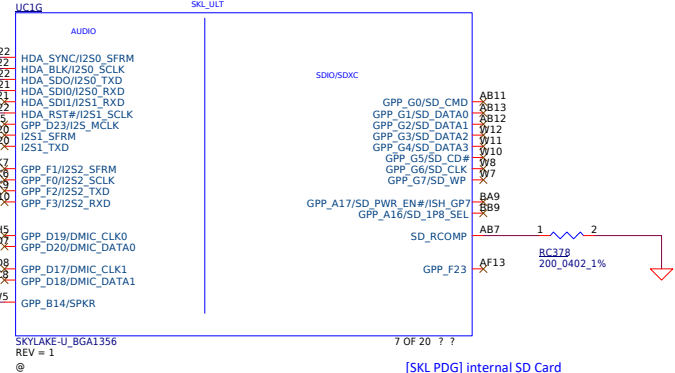
GPP_B14, Internal PD 20K
No Reboot on TCO
Timer expiration
pull-up to VCC3_3 through a 10K 5% resistor to disable this capability



Check RC377 to remove by 7/20

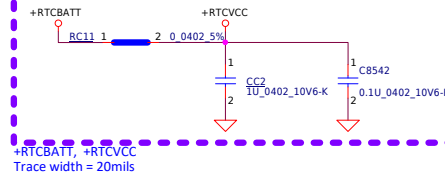
[54] PCH_HDA_SDOIN0

[55] PCH_BEEP

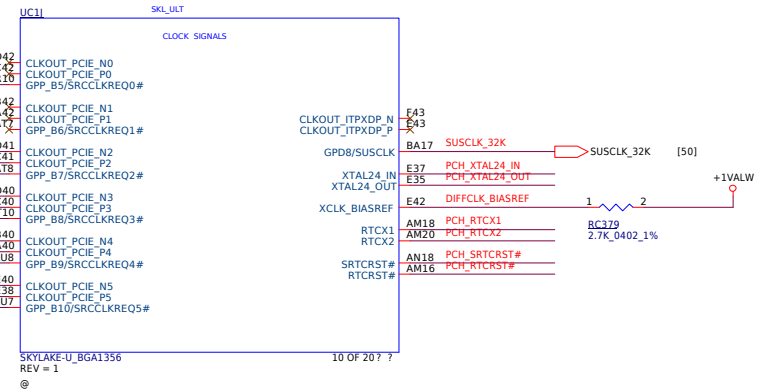
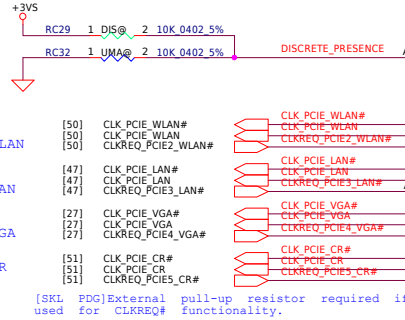
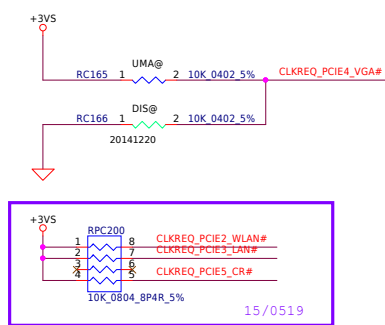
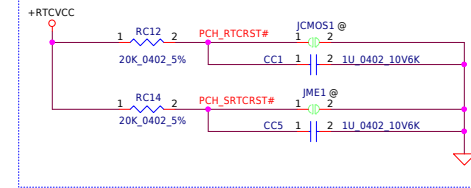


20150514

RTC External Circuit



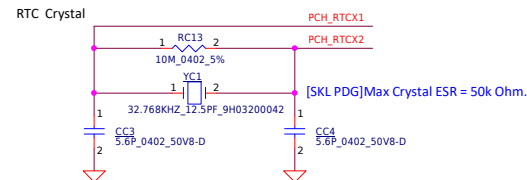
JCMOS, JME Setting, Need Under DDR Door



[SKL PDG]Used to set BIAS reference for differential clocks. Connect to a [RC379] 2.71K 0.5% precision resistor to 1.0v.

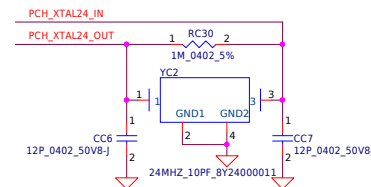
[SKL PDG]

- 1.Space > 15mils
 - 2.No trace under crystal
 - 3.Place on opposite side of MCP for temperature
 - 4.The exact capacitor values for C1 and C2 must be based on the crystal maker's recommendation
- Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.



[SKL PDG]

- 1.A 24 MHz crystal with crystal frequency tolerance and stability of +/-30 ppm
- 2.Two External Load Capacitors (Ce1 and Ce2)
- 3.A 1 Mohm bias resistor (Rf)



L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
 *:Enable Intel ME Crypto Transport Layer Security (TLS) cipher
 suite with confidentiality).Support Intel AMT with TLS and
 SBA (Small Business Advantage) with TLS.

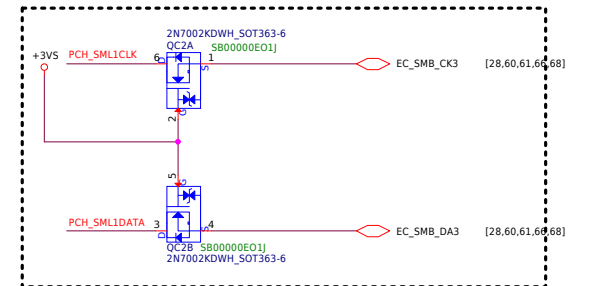
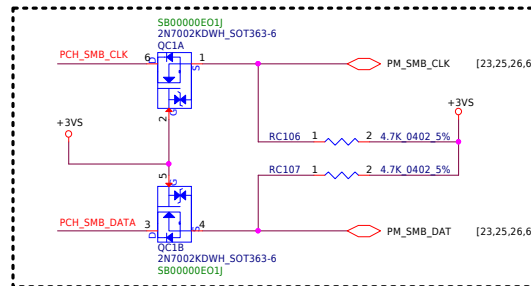
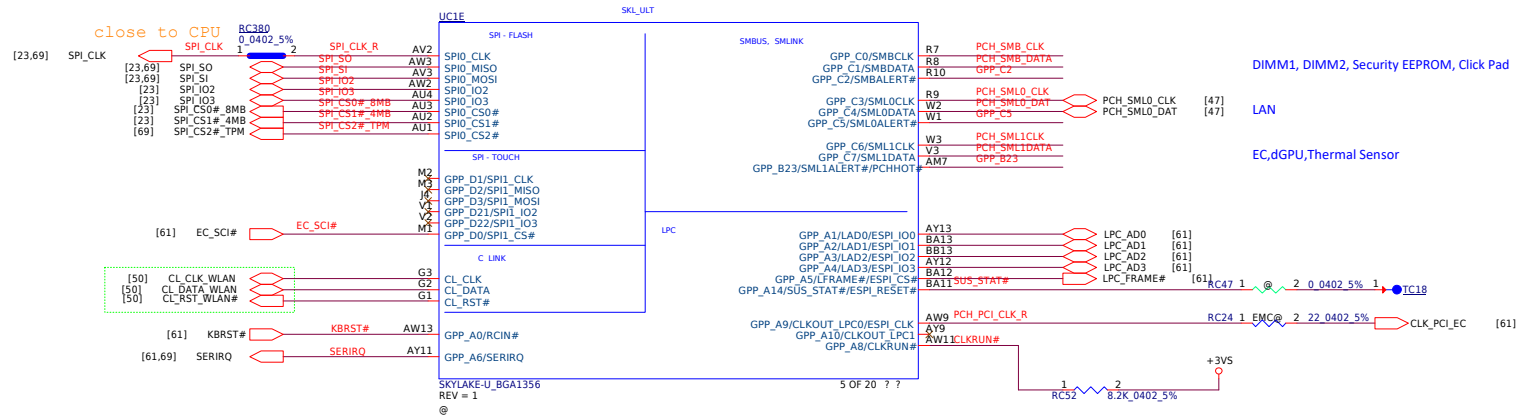
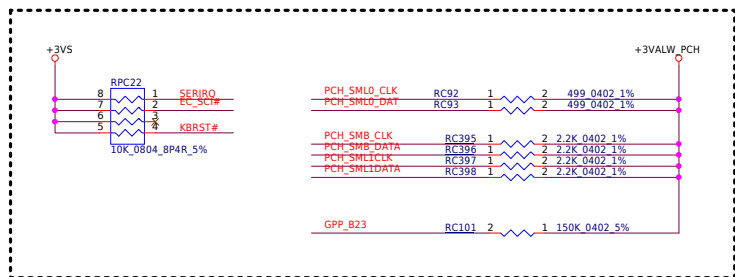
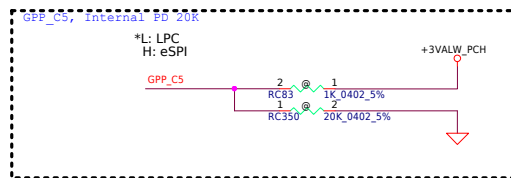
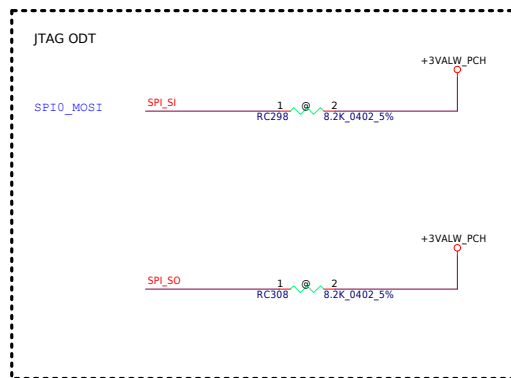
GPP_C2


1 RC306 2 1K_0402_5%

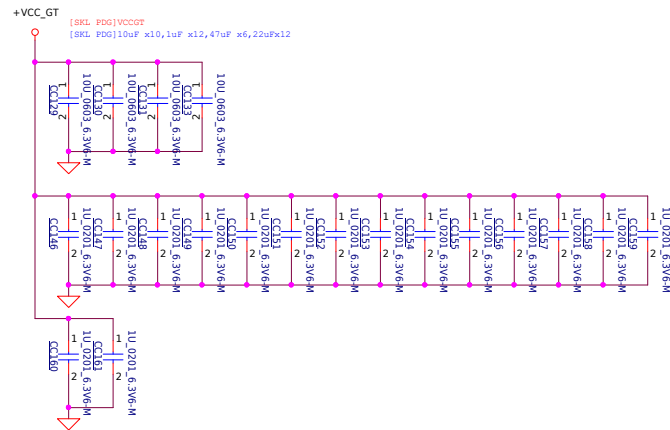
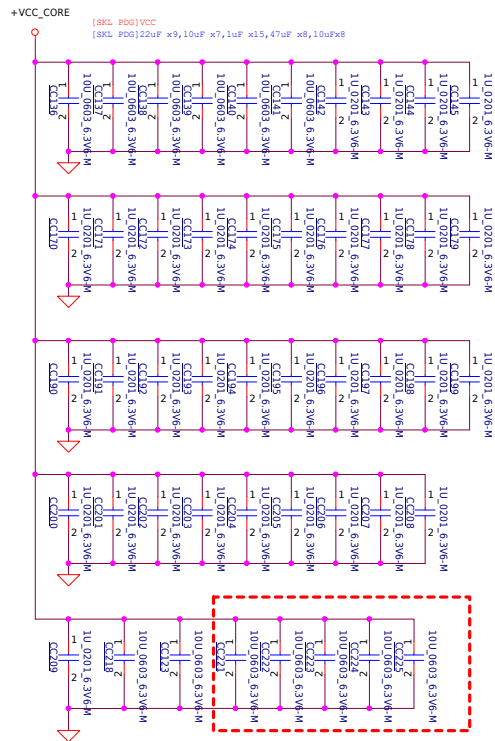
1 RC307 20K_0402_5%

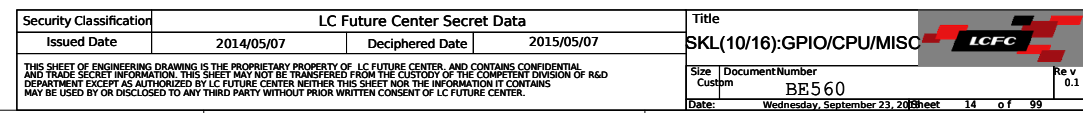
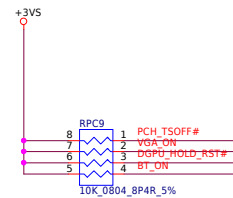
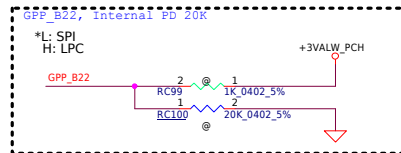
+3VALW_PCH

GPP_C2, Internal PD 20K



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3D CCD

WLAN

LAN

Card Reader

HDD

ODD, only for 15"

GPU

UC1H

SKL_ULT

PCIEUSB3SATA

SSIC / USB3

3D camera

USB3.0 on board

ChargerPort

Docking

Sub/B Charger Port

ONE DOCK

Touch Panel

BT

Camera

WWAN

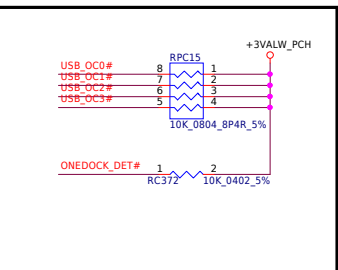
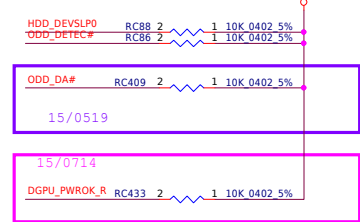
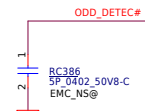
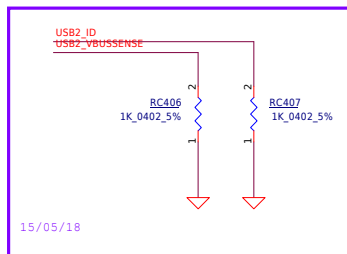
FPR

Smart Card

GPU

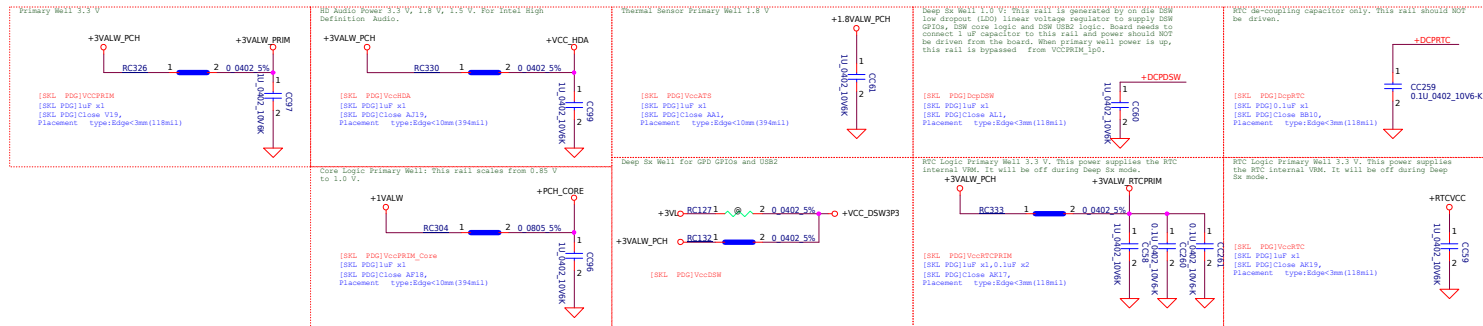
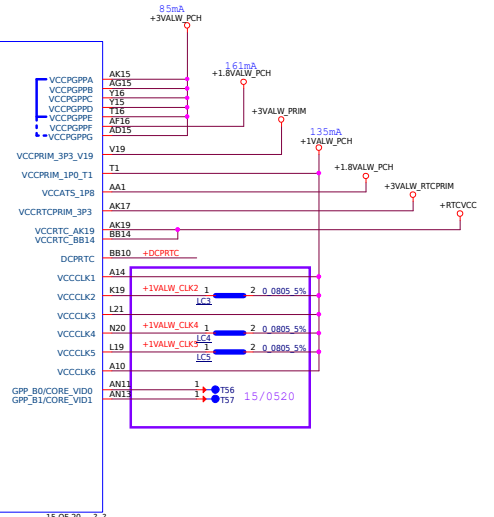
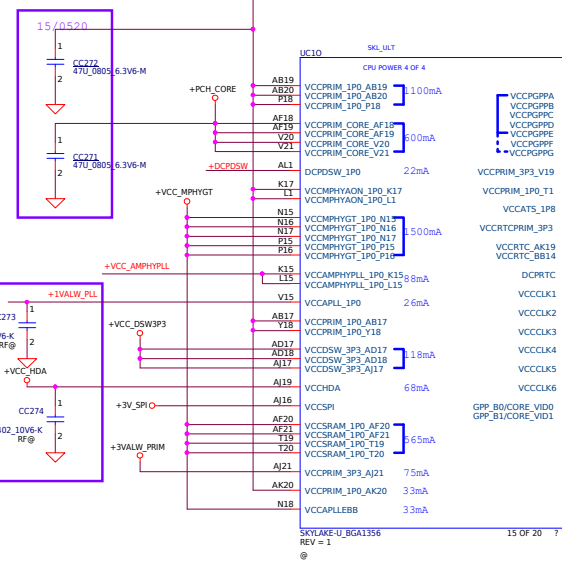
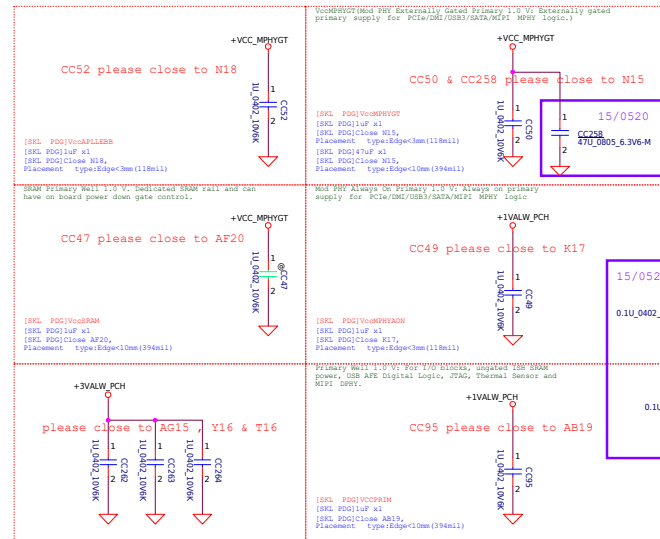
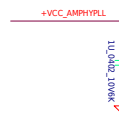
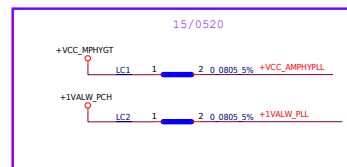
SKYLAKE-U_BGA1356

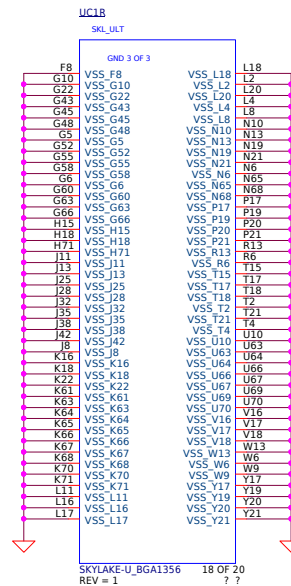
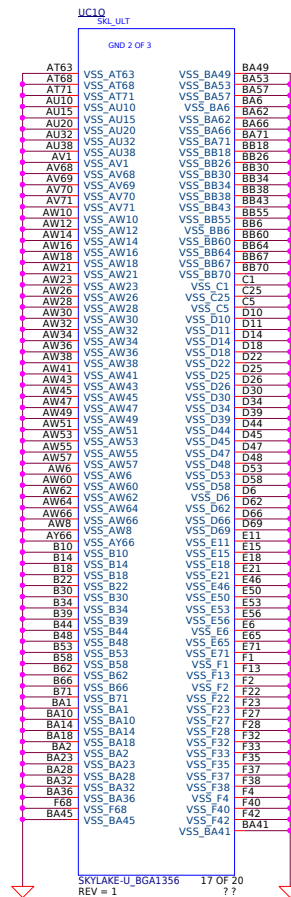
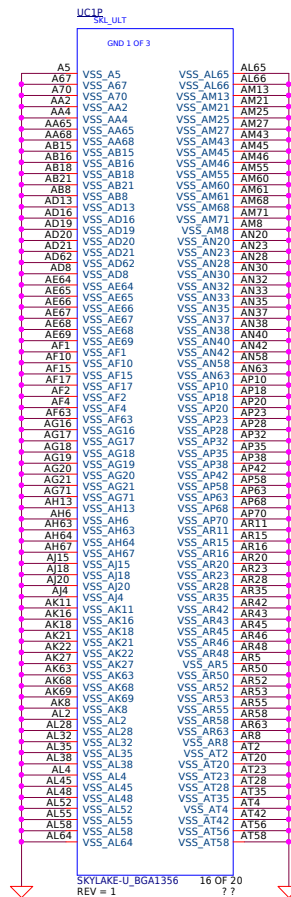
REV = 1




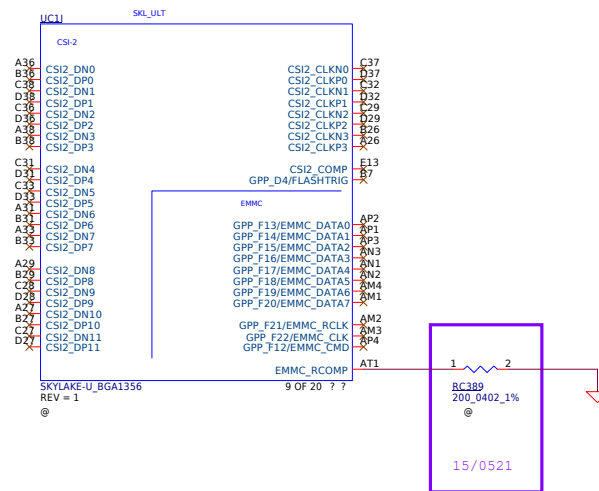
USB_OC0#	Port 1, Port2
USB_OC1#	Port 3, Port4
USB_OC2#	Port 5, Port6
USB_OC3#	Port 7, Port8

20150308

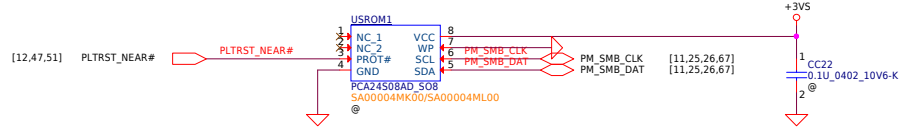




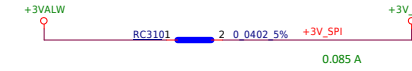
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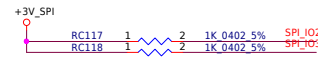
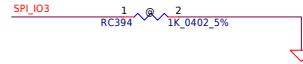
Security ROM



M3 Support + Intel LAN PHY / Wireless LAN Solution



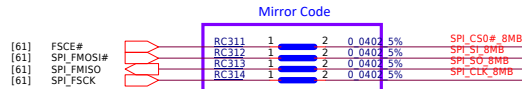
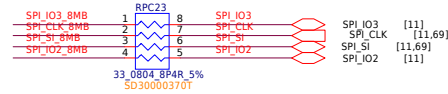
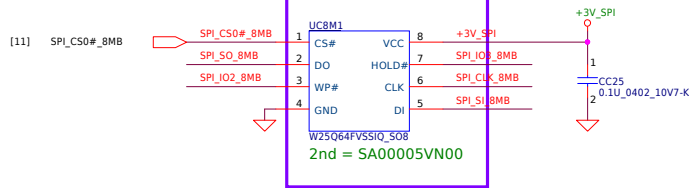
20141220



[SKL]SPI0_CS0#: SPI FLASH
SPI0_CS1#: SPI FLASH
SPI0_CS2#: SPI TPM

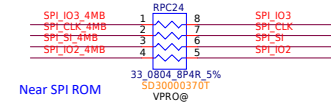
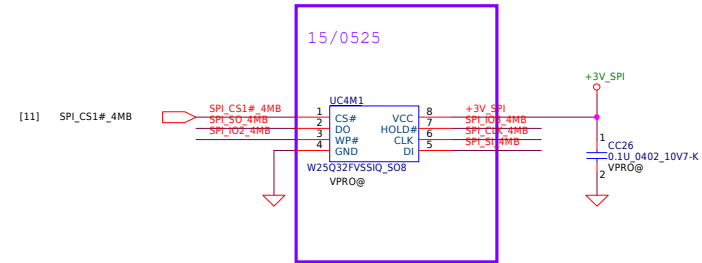
8MB(64Mb)

feedback to SDV rev..
15/0522

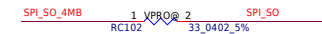


Close to SPI ROM (UC8M1).

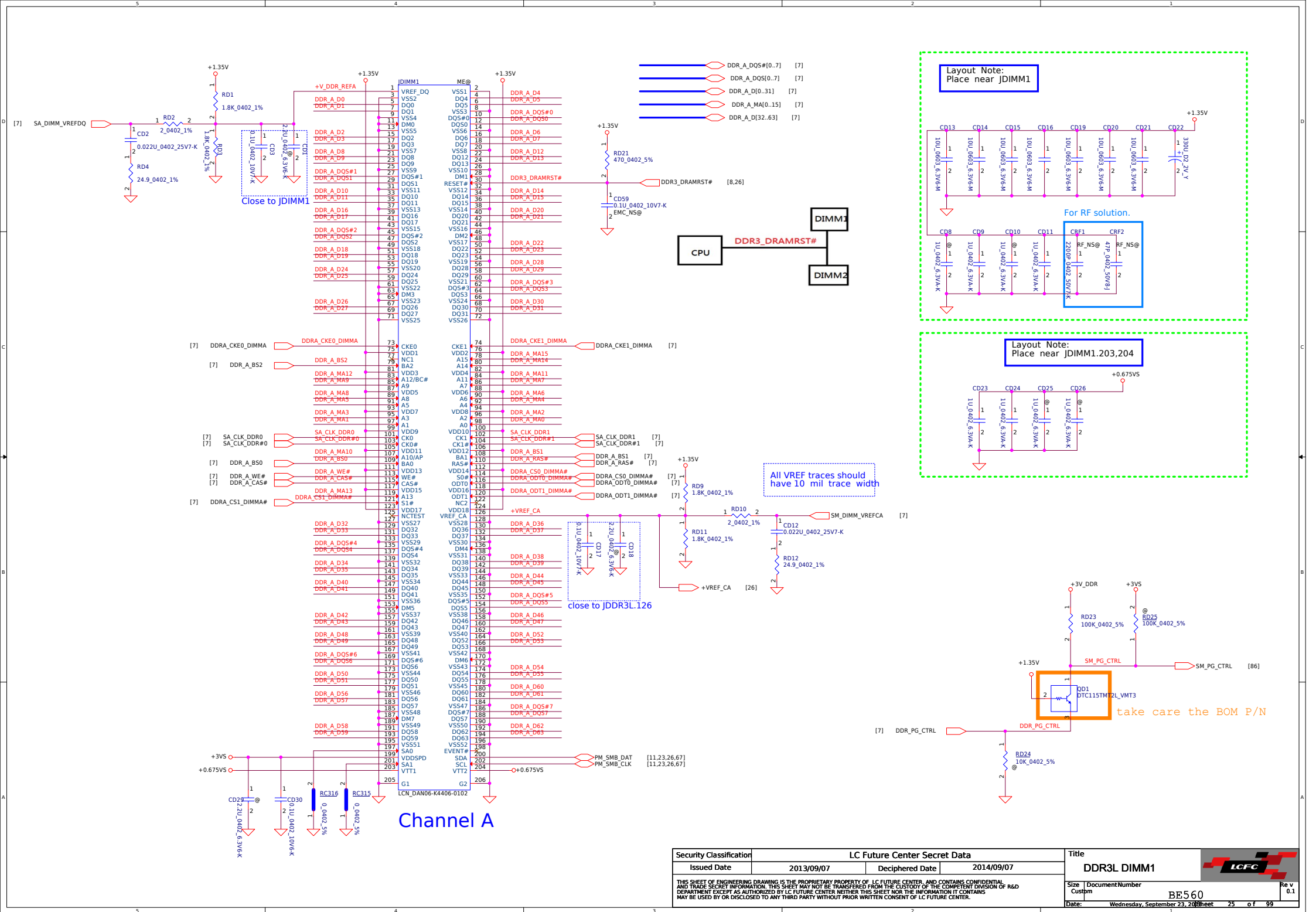
4MB(32Mb) for VPRO SKU

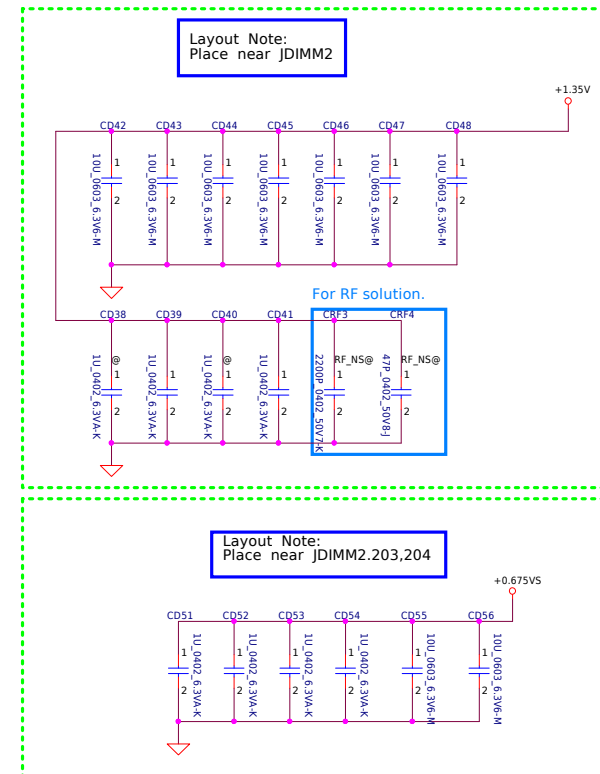



Near SPI ROM

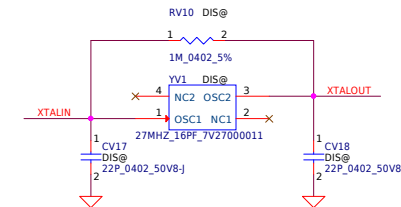
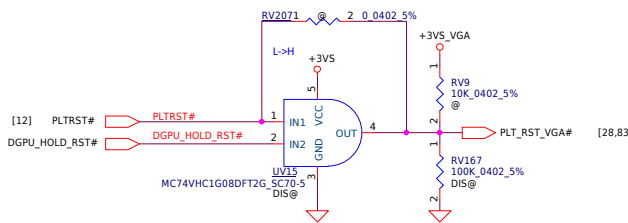
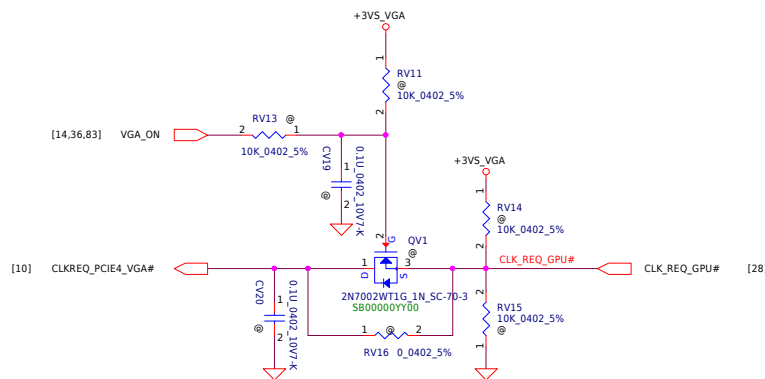
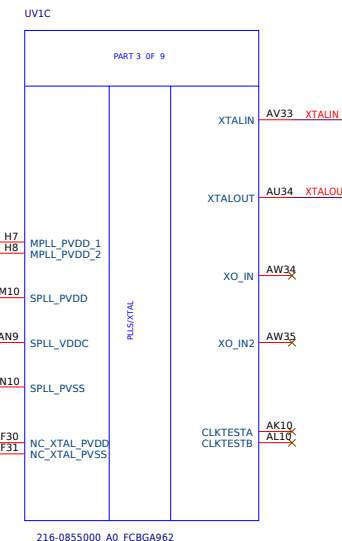
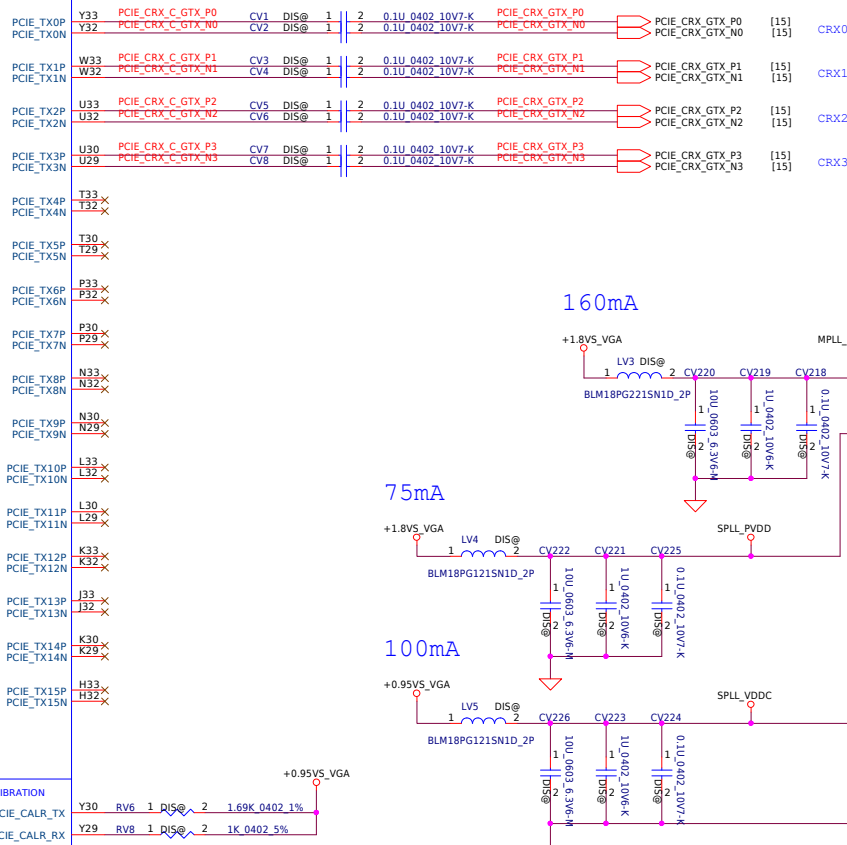
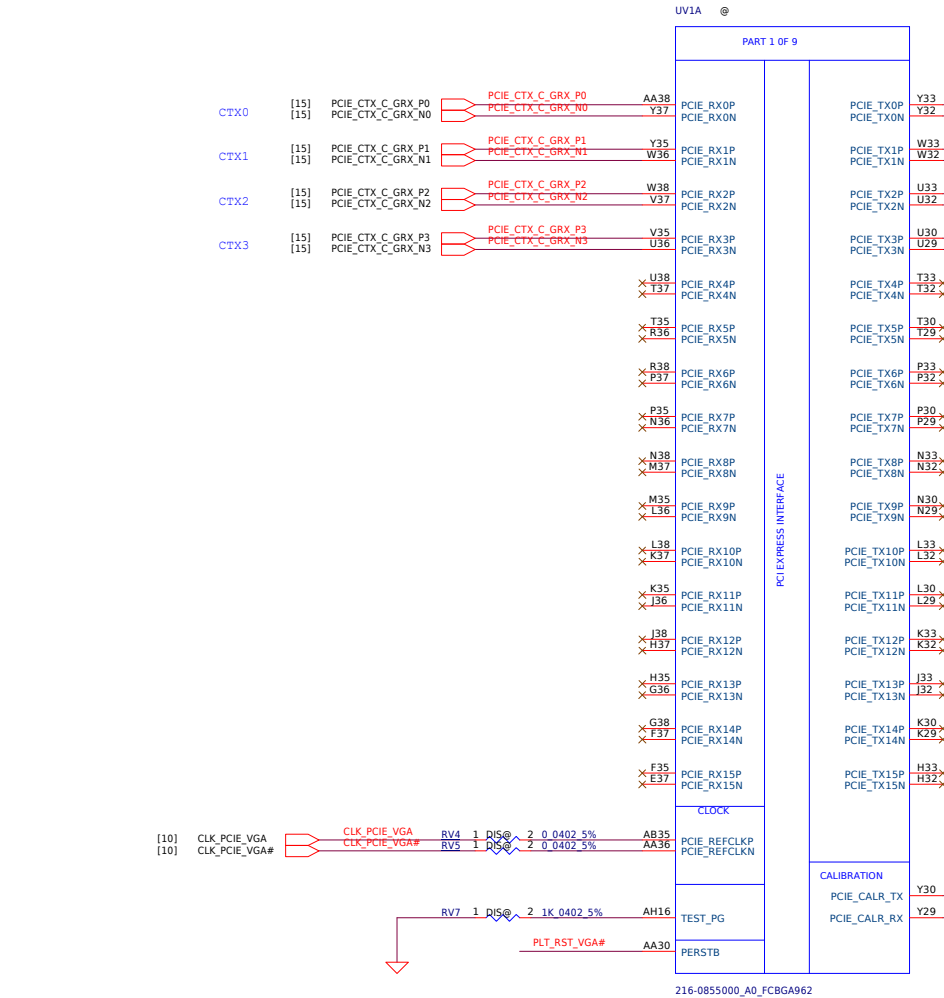


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Date:				Wednesday, September 23, 2014	
				Sheet 23 of 99	

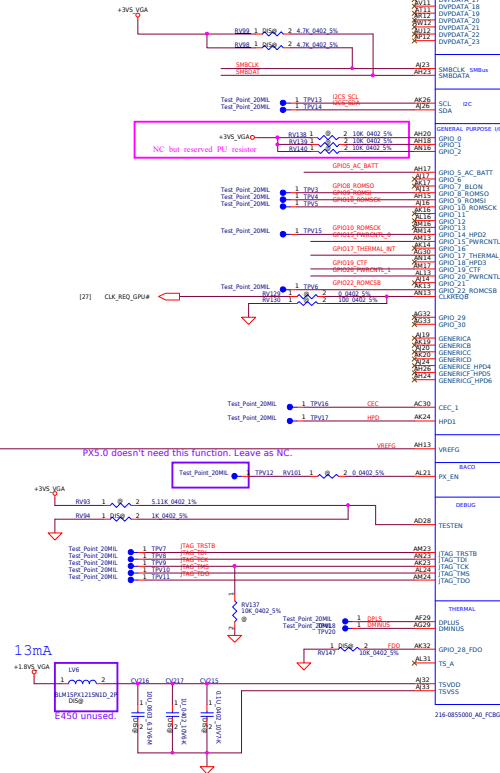
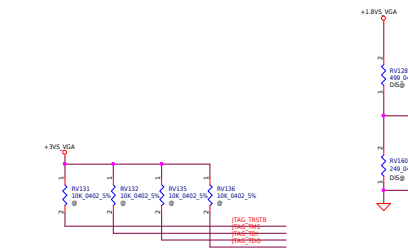
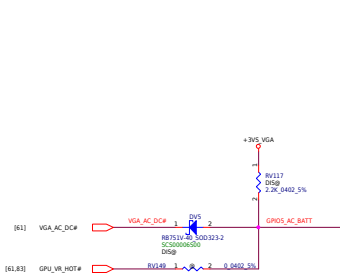
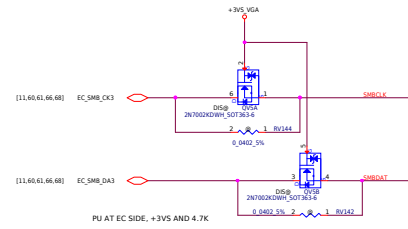




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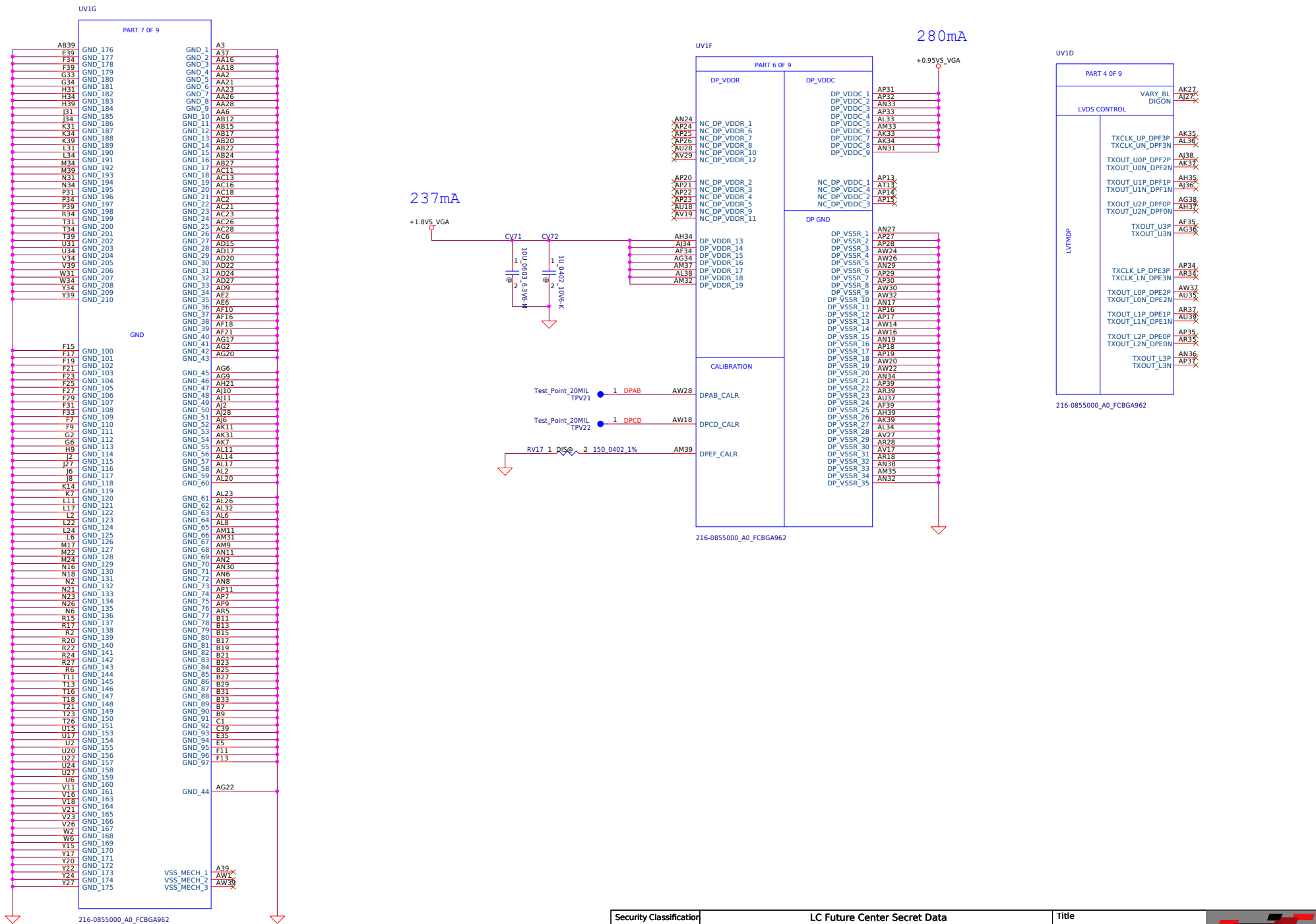


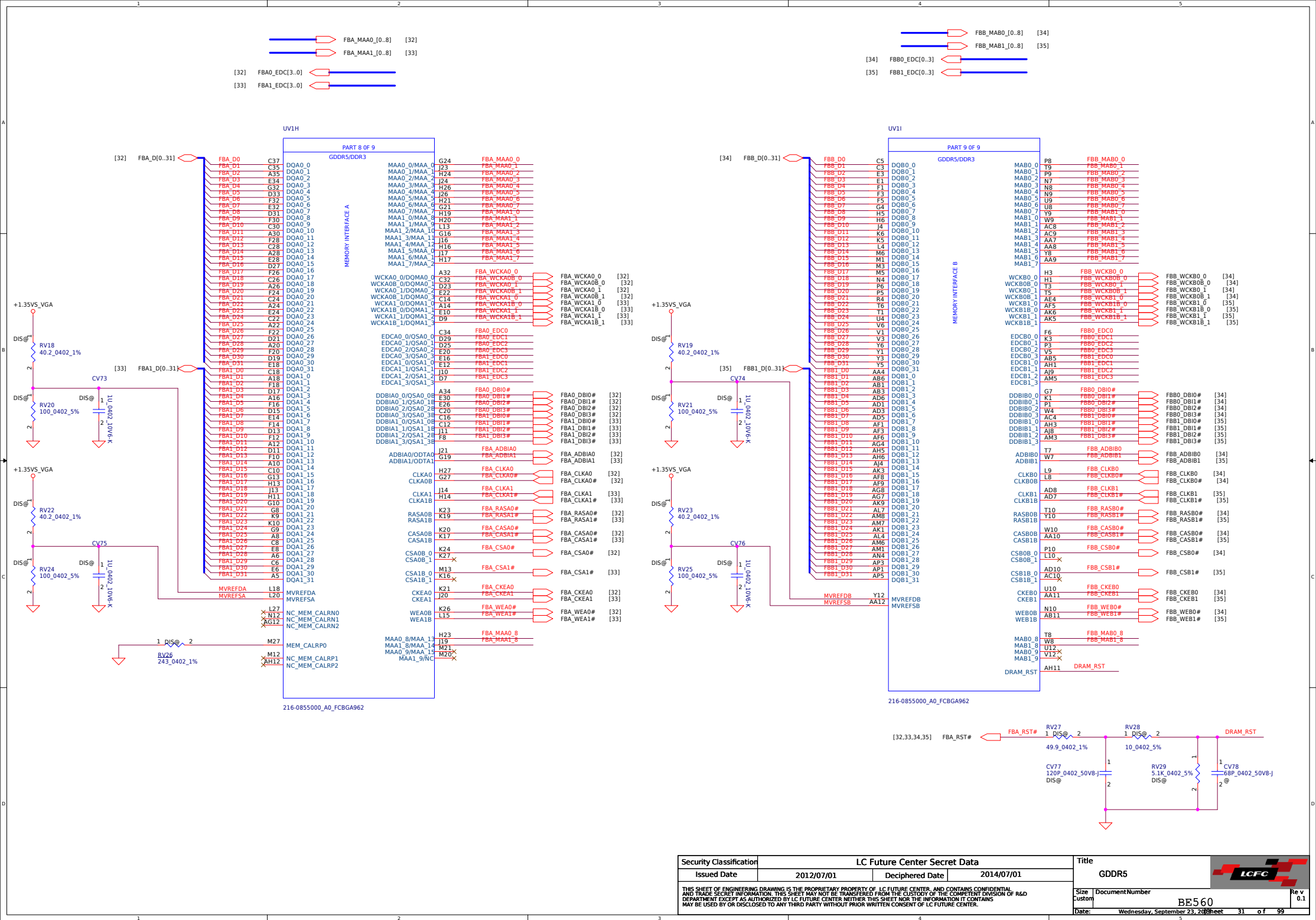
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Date	Wednesday, September 23, 2014	Sheet	27 of 99



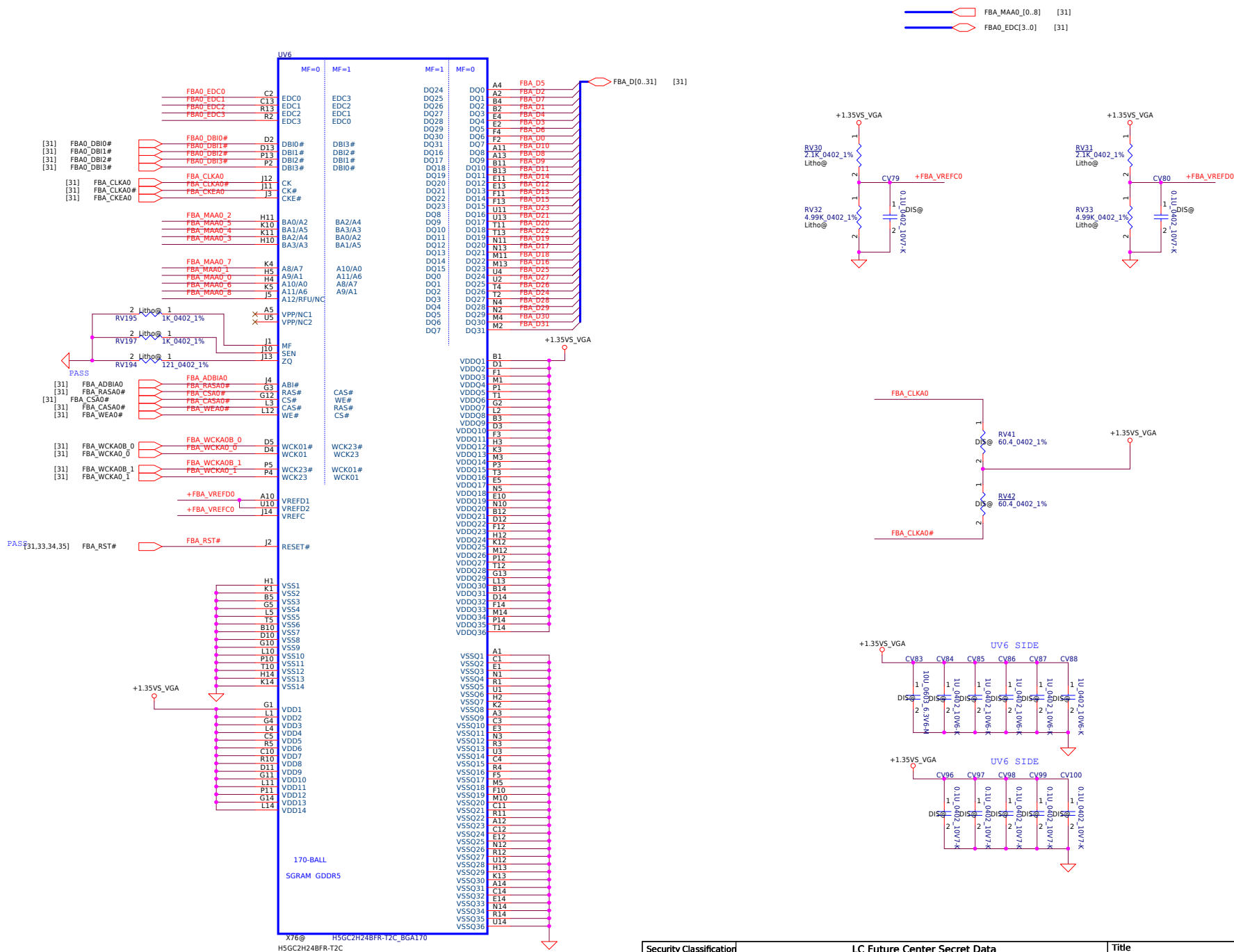
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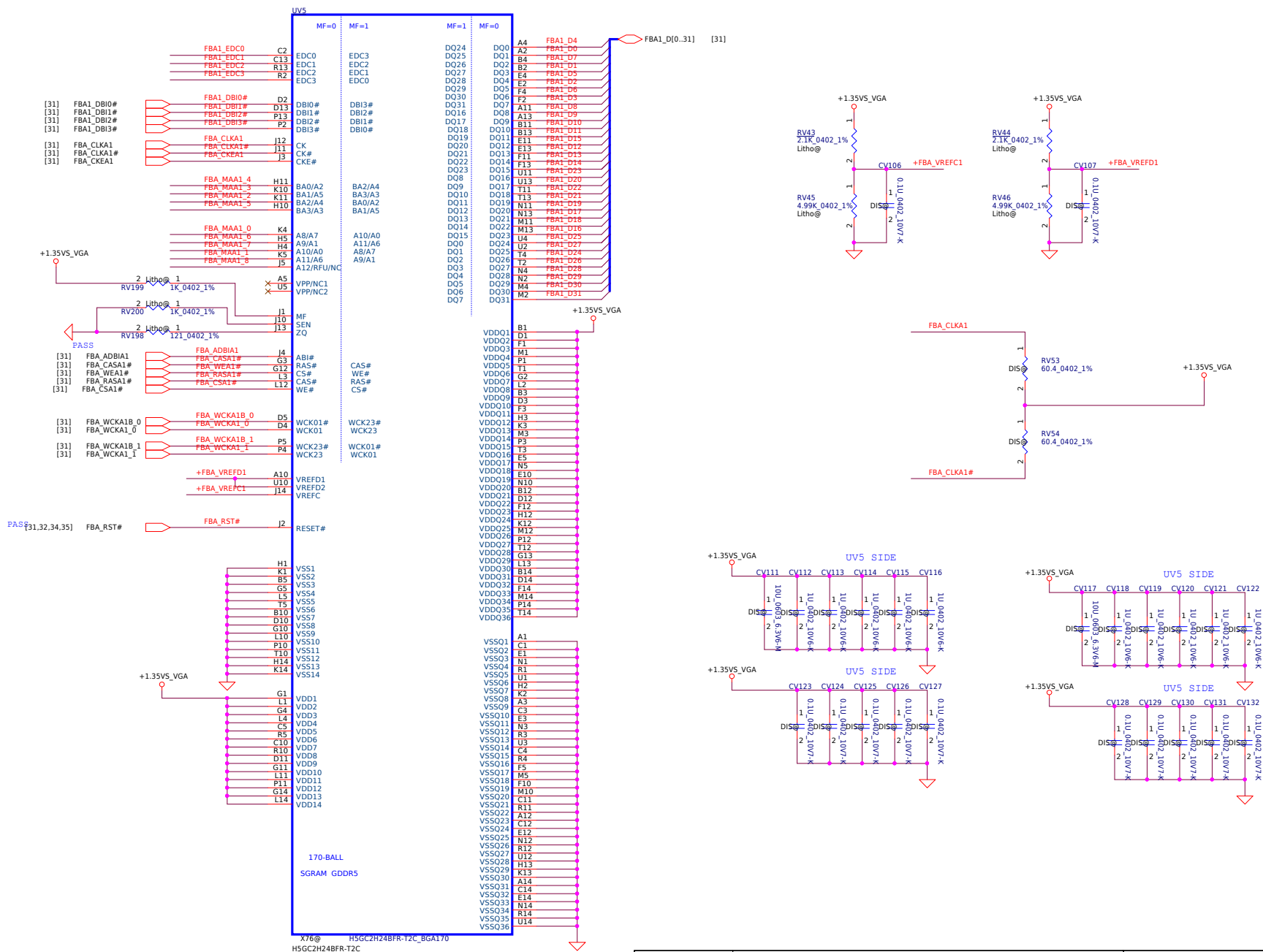



Memory Partition A - Lower 32 bits



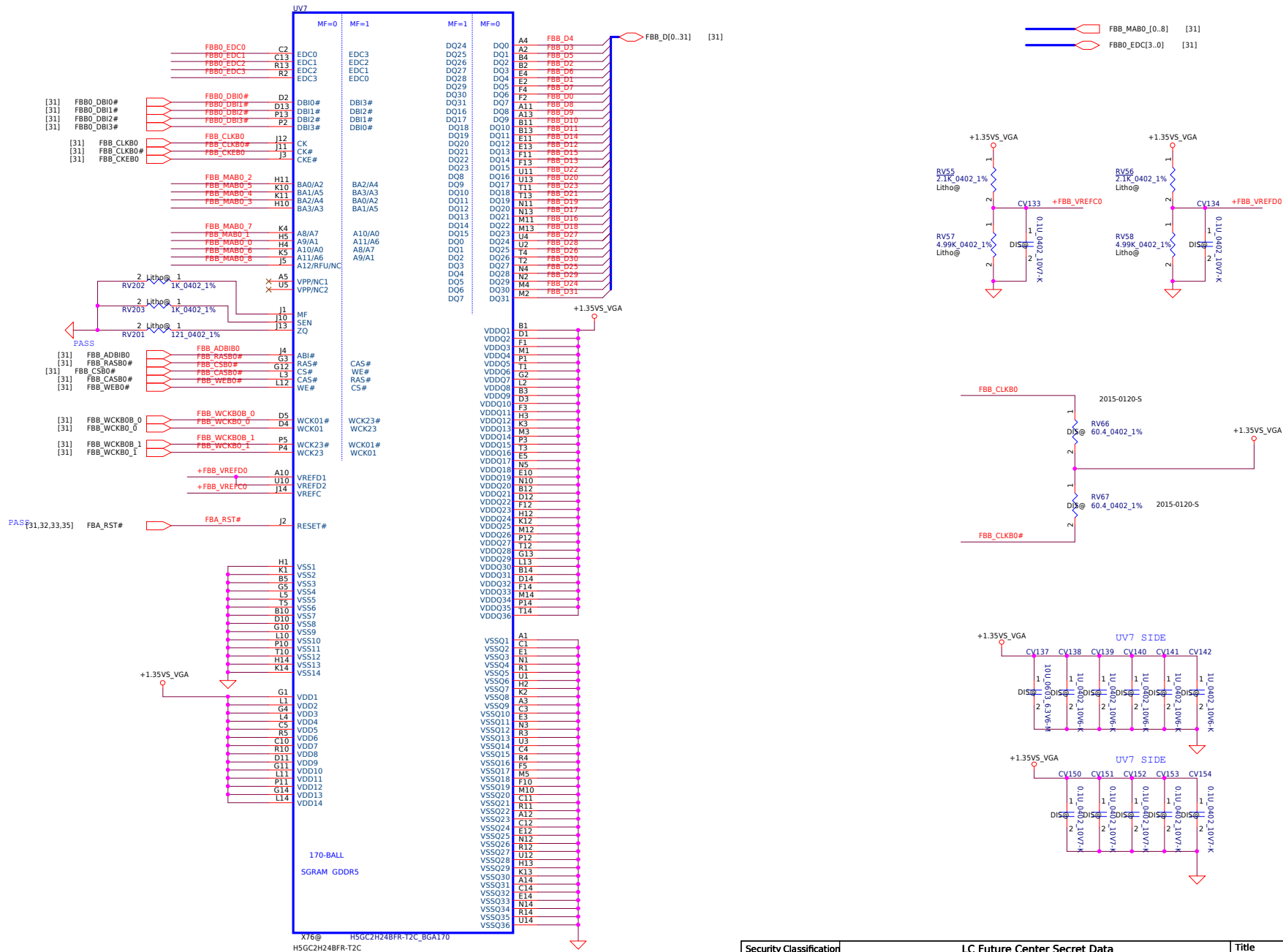
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	GDDR5	
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Memory Partition A - Upper 32 bits

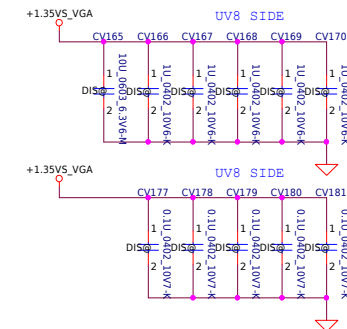



Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	GDDR5	
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				Document Number	
				BE560	Rev 0.1
				Date: Wednesday, September 23, 2014	33 of 99

Memory Partition A - Lower 32 bits

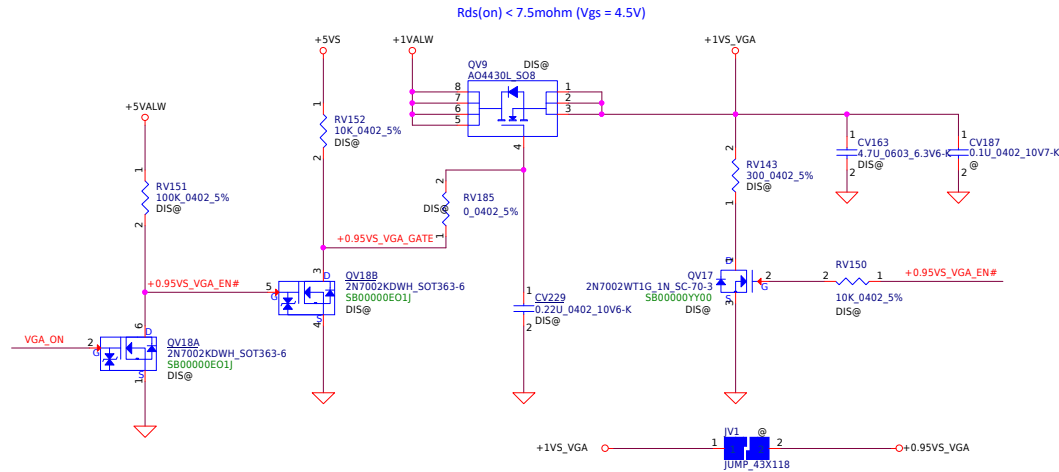


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				Date:	Wednesday, September 23, 2014	Sheet 34 of 99

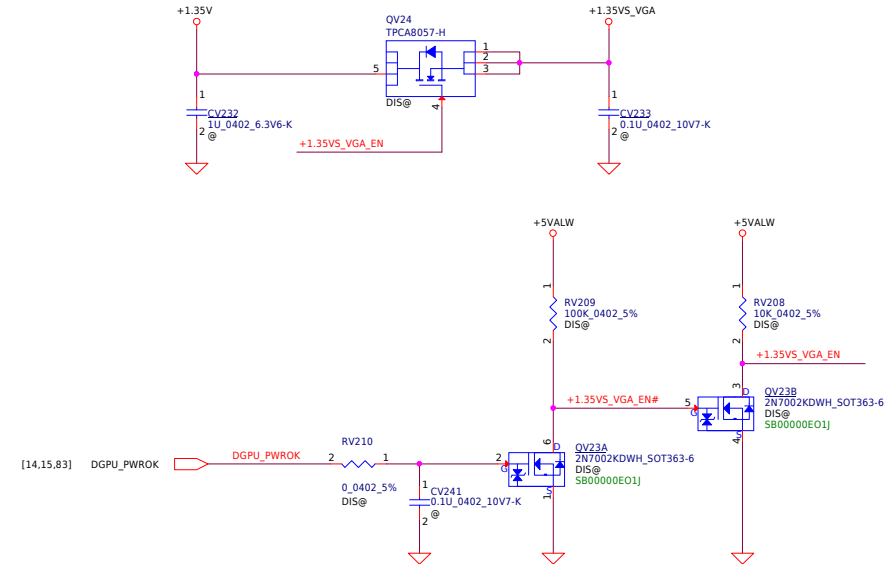


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Issued Date	2012/12/05	Deciphered Date	2014/12/05	GDDR5		
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				Date:	Wednesday, September 23, 2014	Re v 0.1

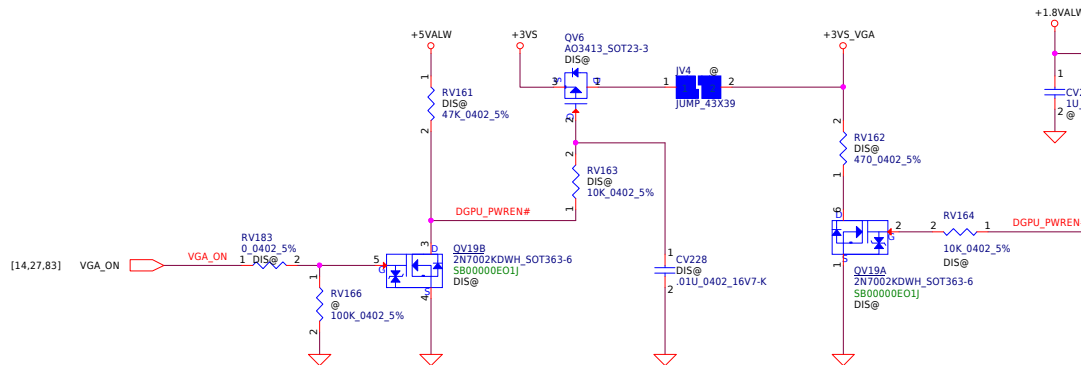
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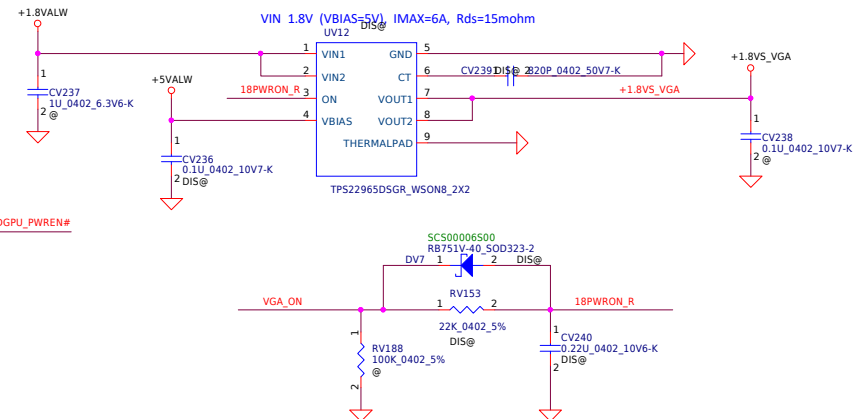
+1.35V to +1.35VS_VGA



+3VS to +3VS_VGA




+1.8VALW to +1.8VS_VGA



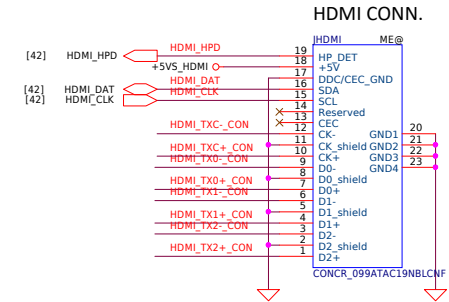
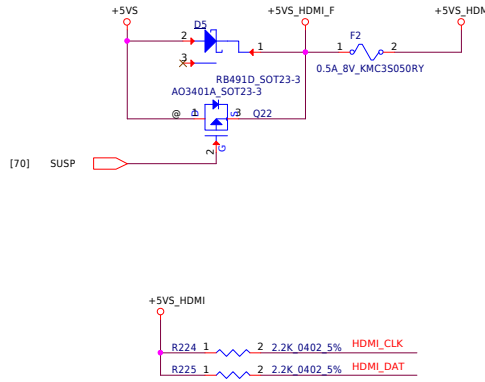
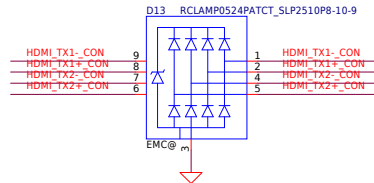
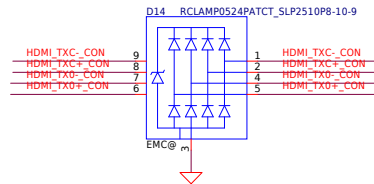
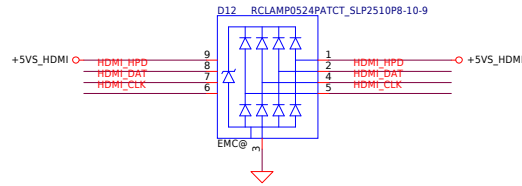
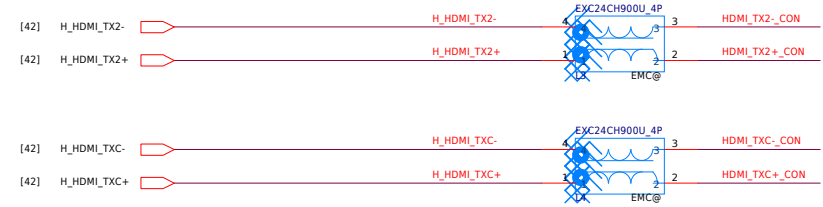
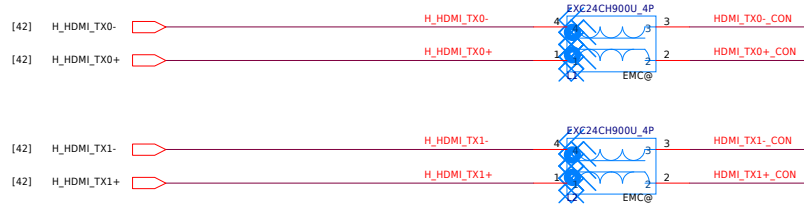
MLPS	Bit				
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PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X

<http://www.repair1.ru/>

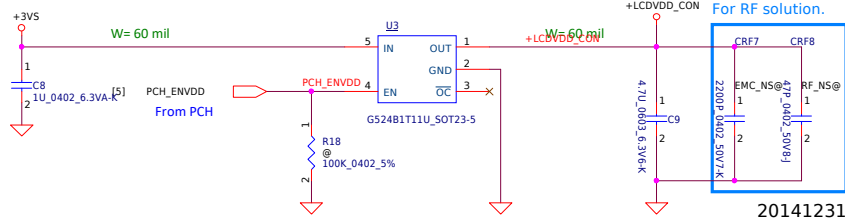
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Issued Date	2012/12/05	Deciphered Date	2014/12/05	Litho switch power	
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				Date:	Wednesday, September 23, 2014
				Sheet	36 of 99



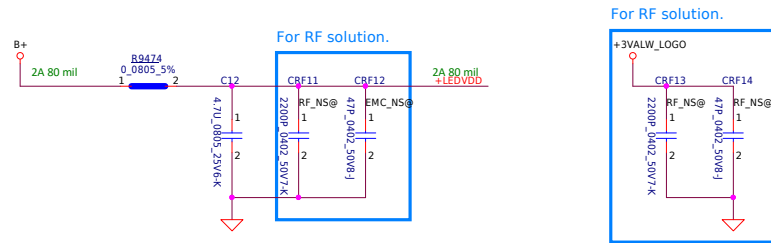
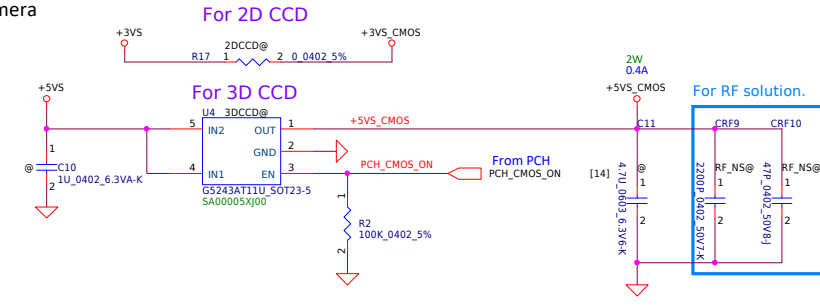
Rev 0.1



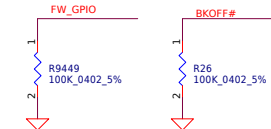
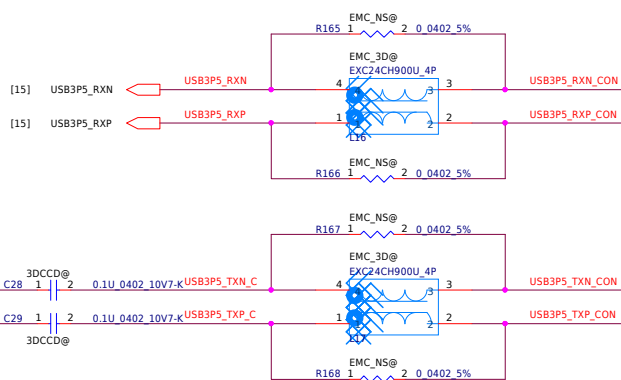
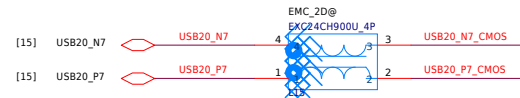
LCDVDD Circuit



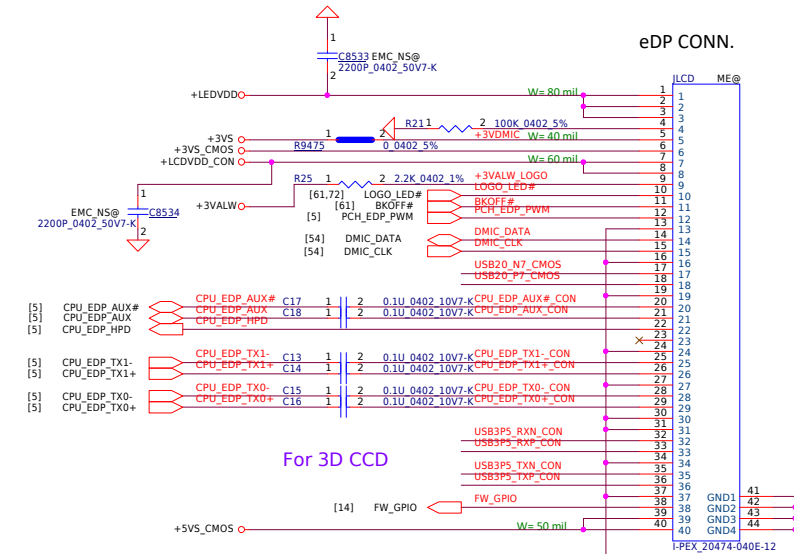
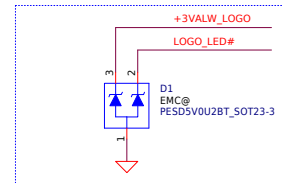
CMOS Camera



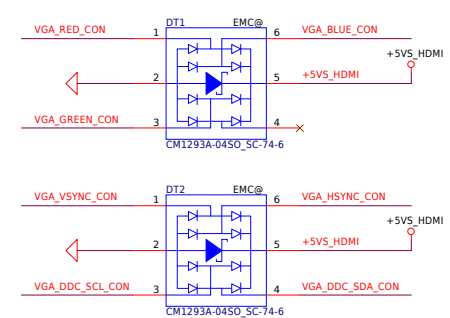
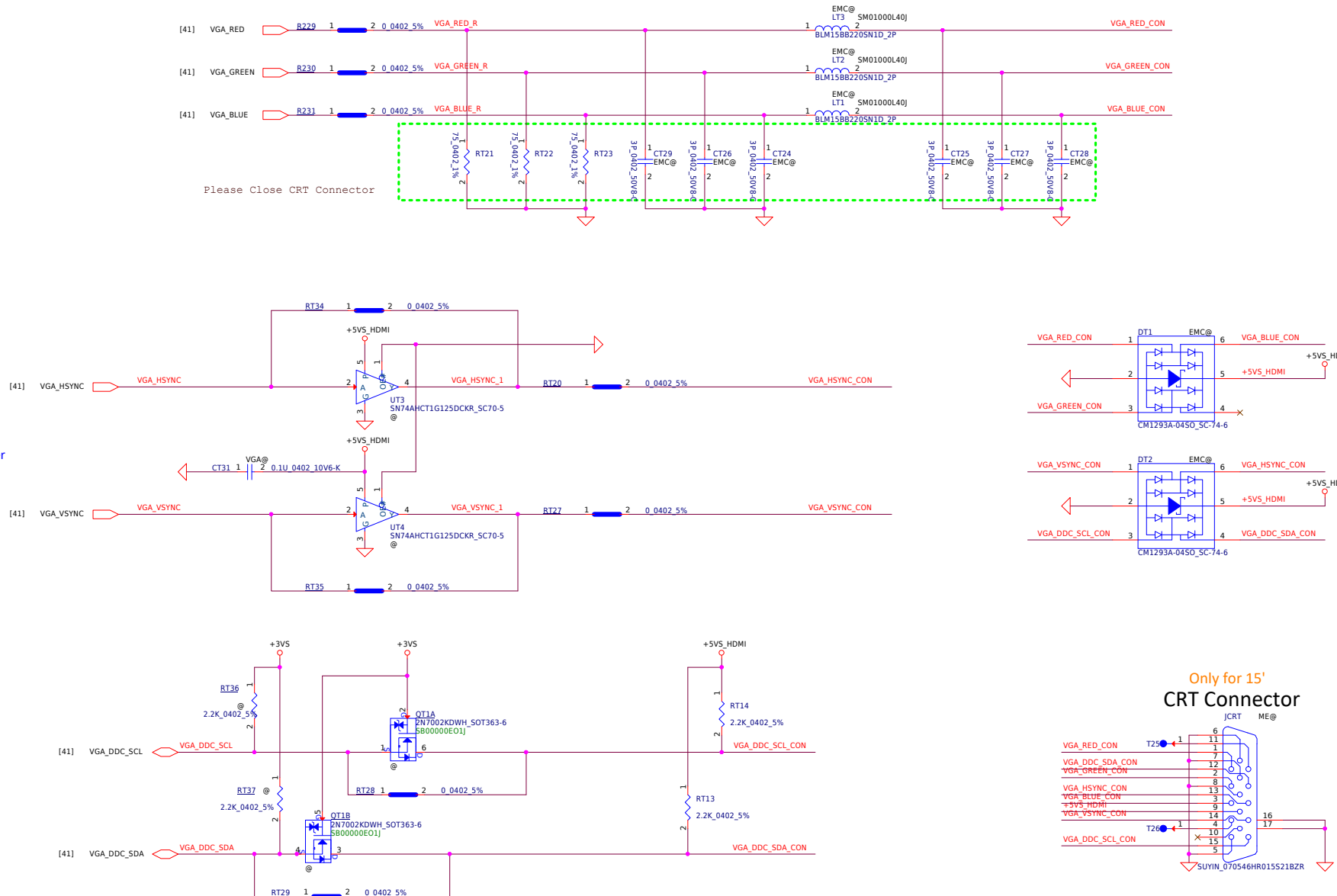
CMOS USB Port 2



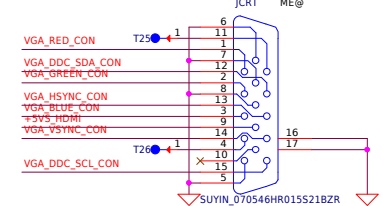
ESD request



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Date:	Wednesday, September 23, 2014		Sheet	38	of 99



Only for 15'
CRT Connector



Traslater

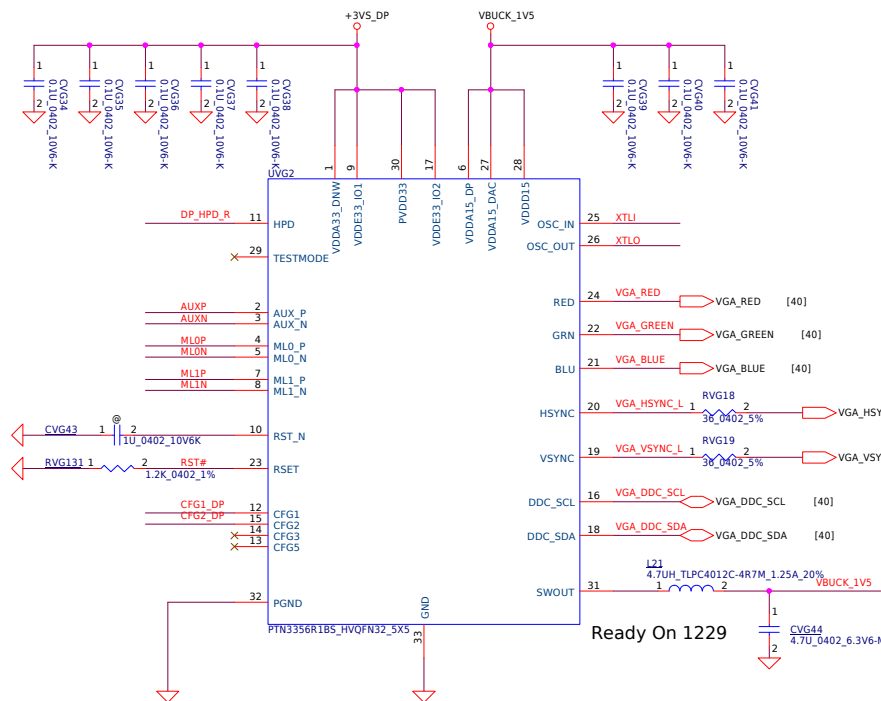
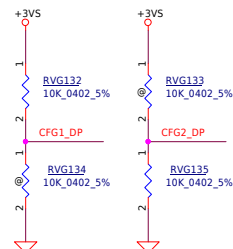
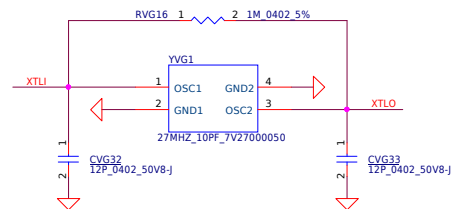
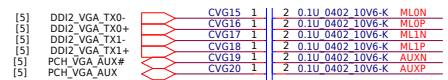
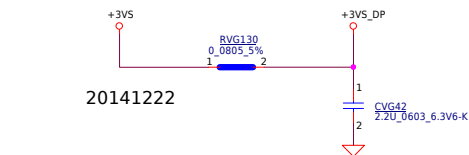
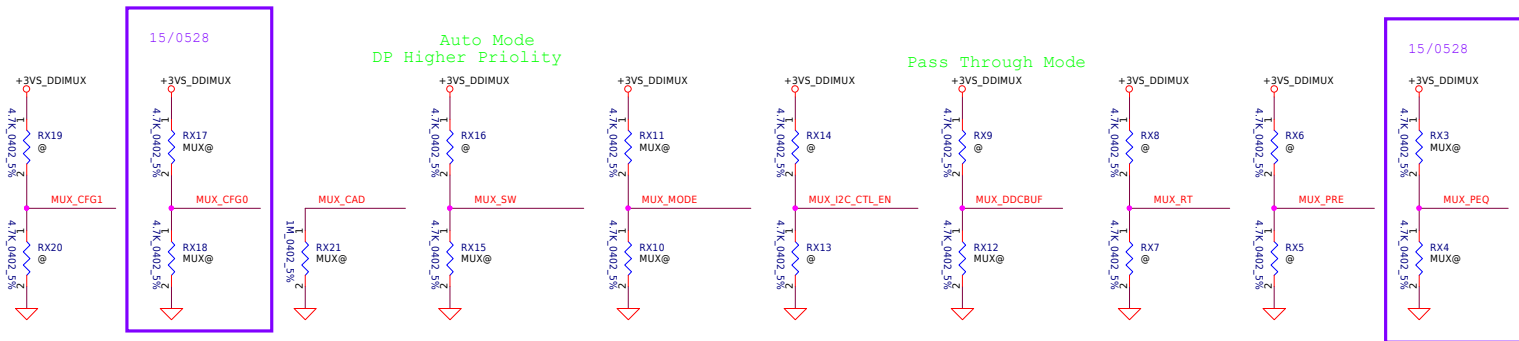
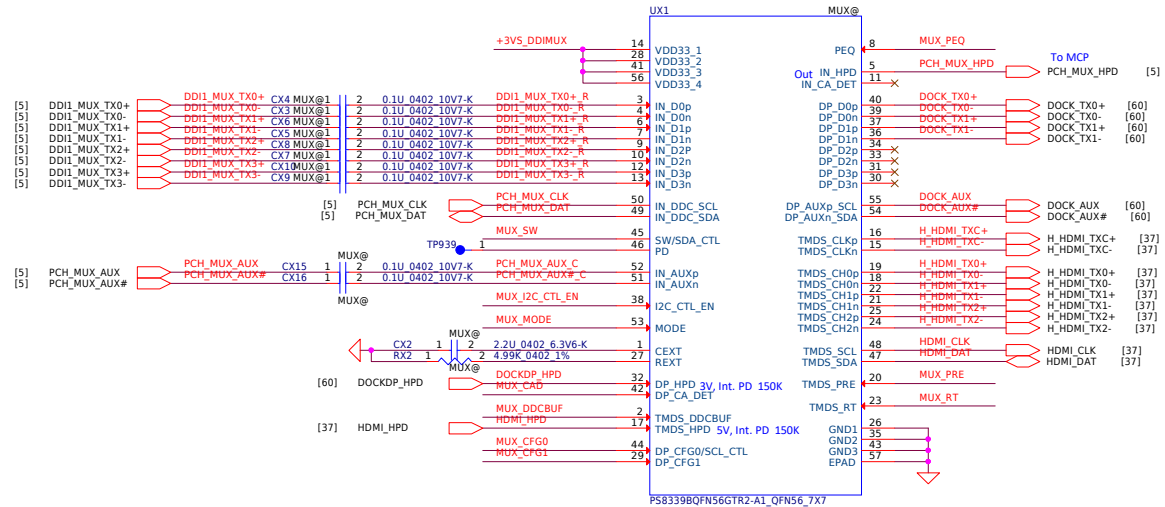
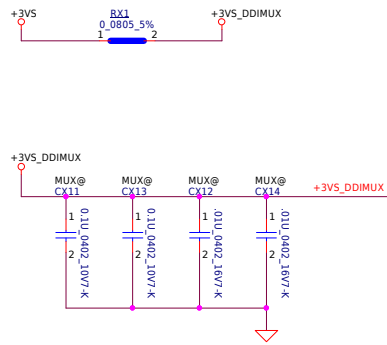


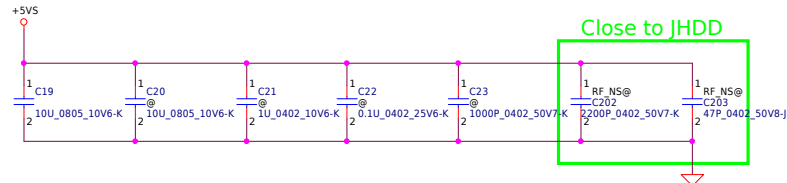
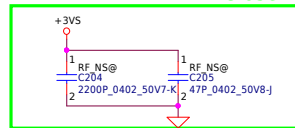
Table 7. CFG1/CFG2 pin definitions

Pin value	System behavior
00	Compliant HPD behavior
01	Most interoperable (non-compliant) HPD behavior
10	Most interoperable (non-compliant) HPD behavior
11	(Default) Compliant behavior



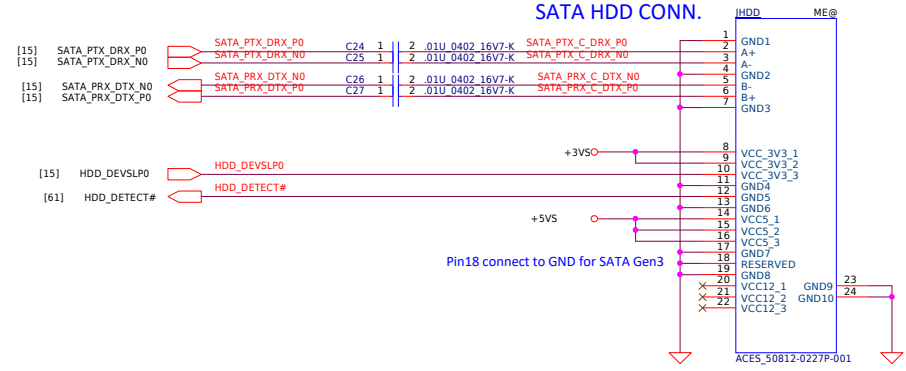
SATA HDD CONN.

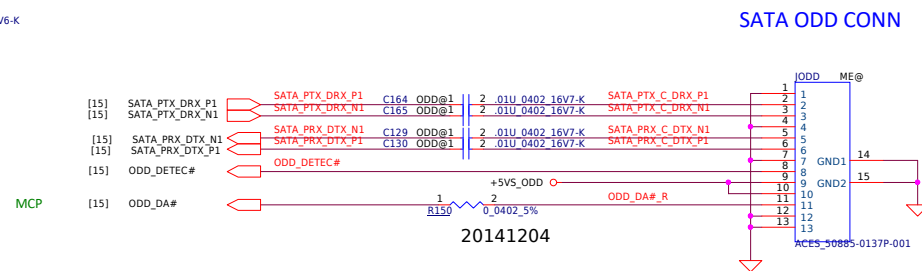
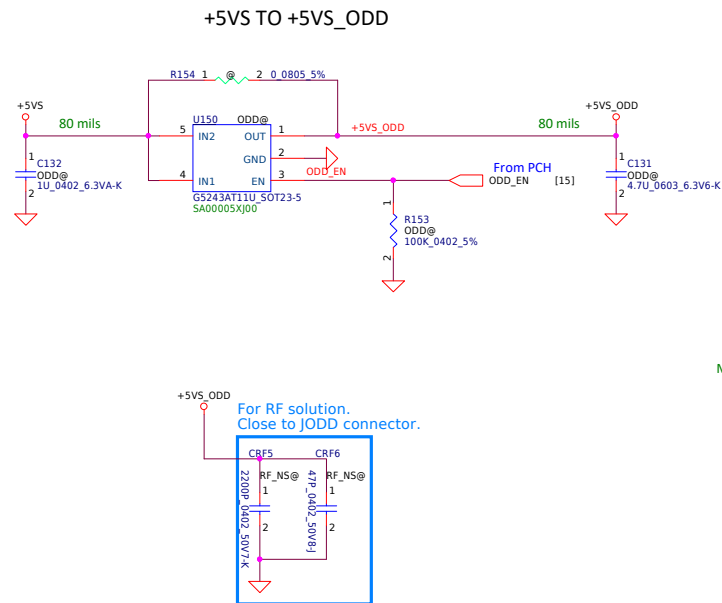
Close to JHDD



Close to JHDD

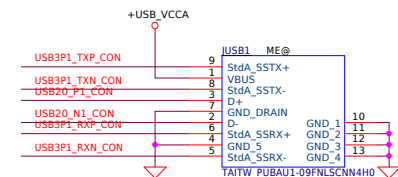
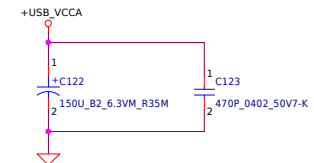
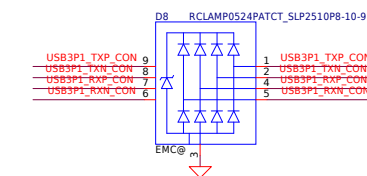
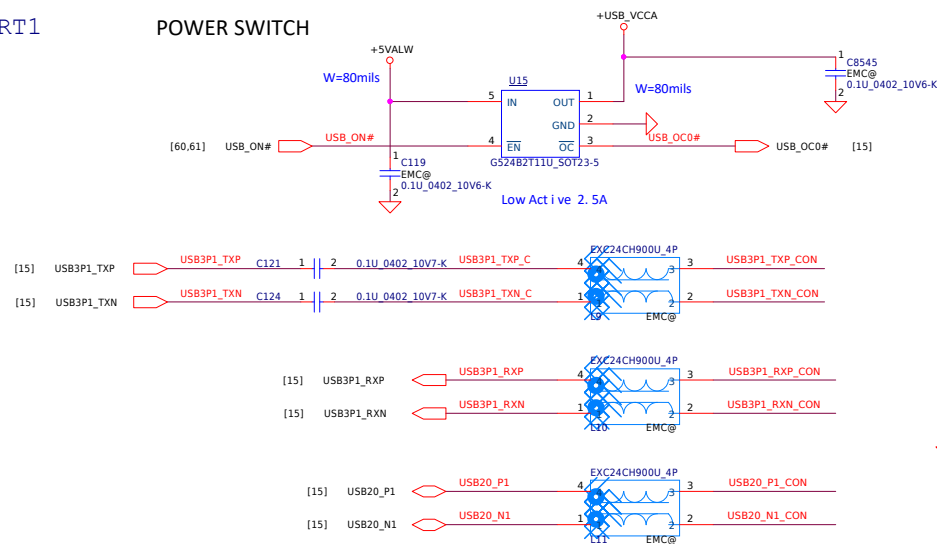
SATA HDD CONN.



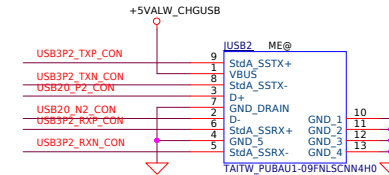
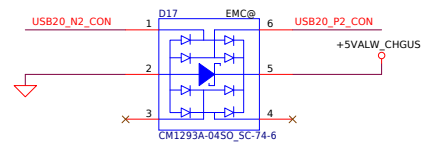
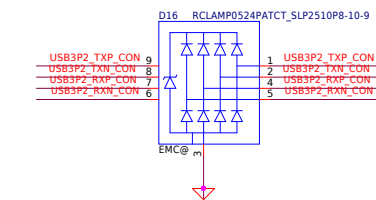
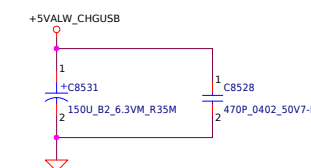
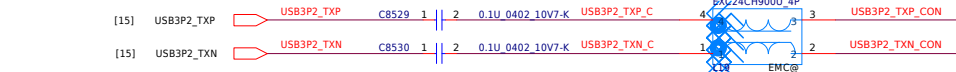
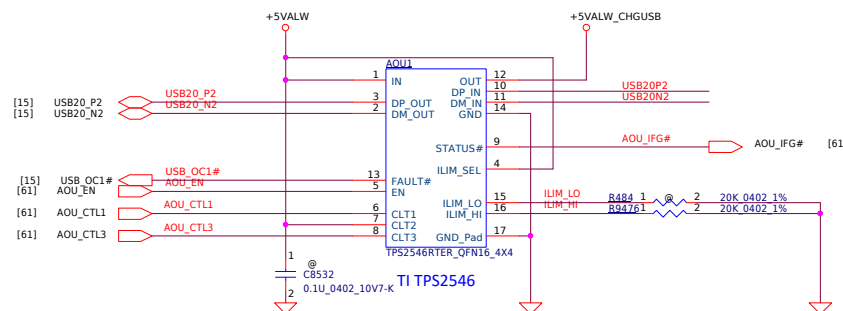


USB3 PORT1

POWER SWITCH

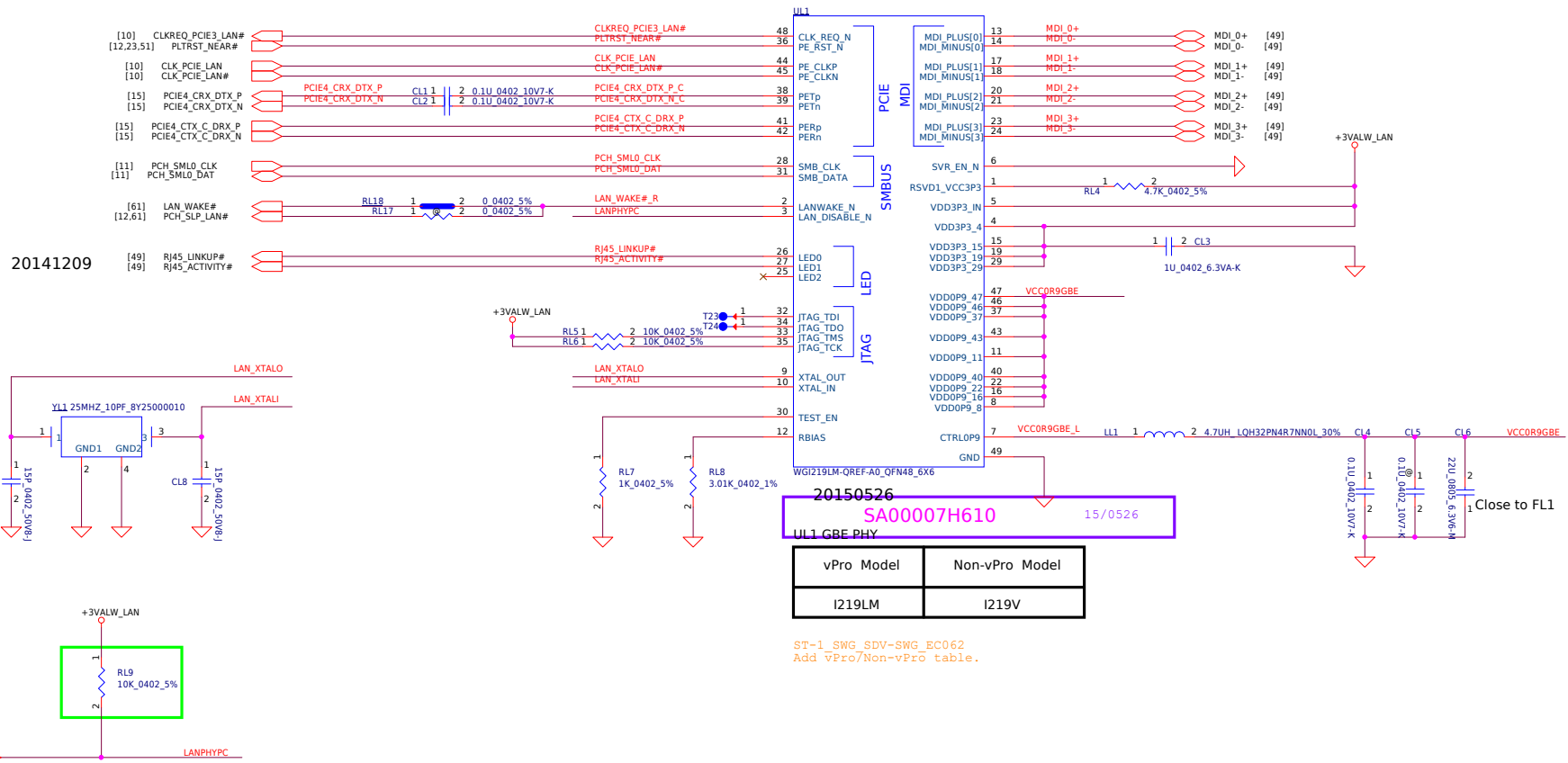
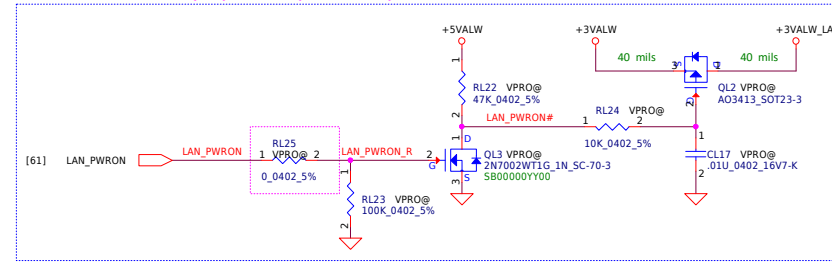
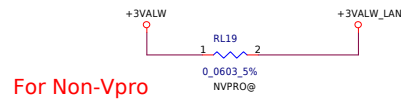


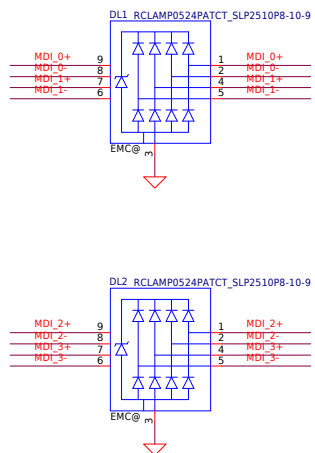
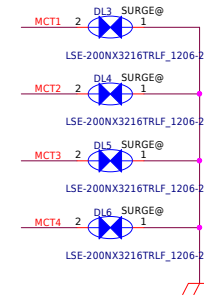
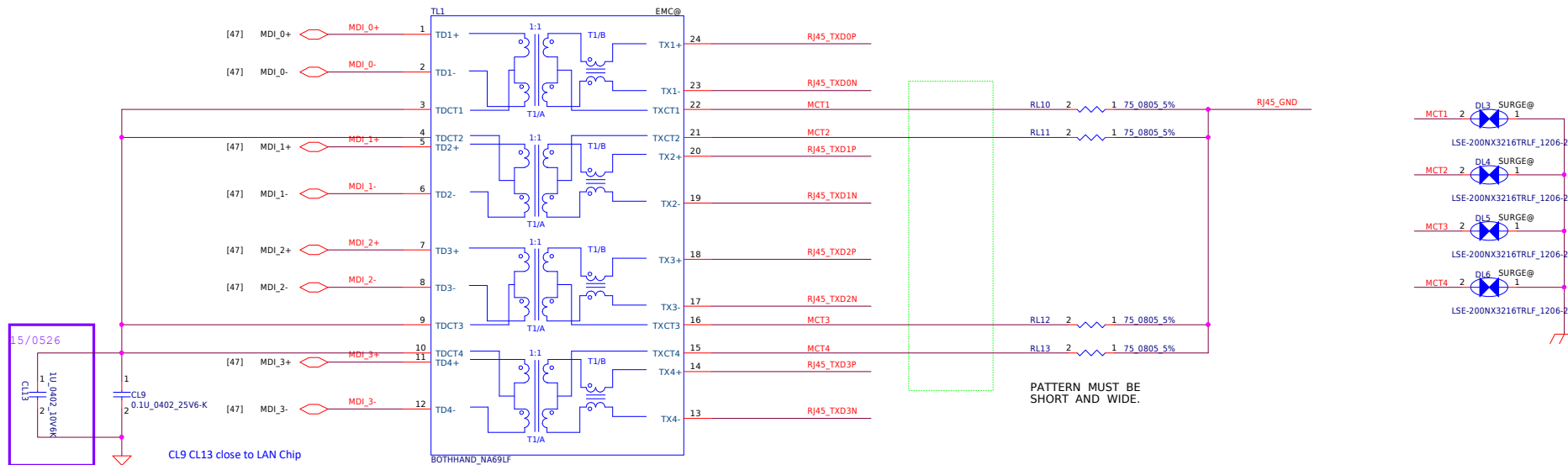
PORT2 (AOU)



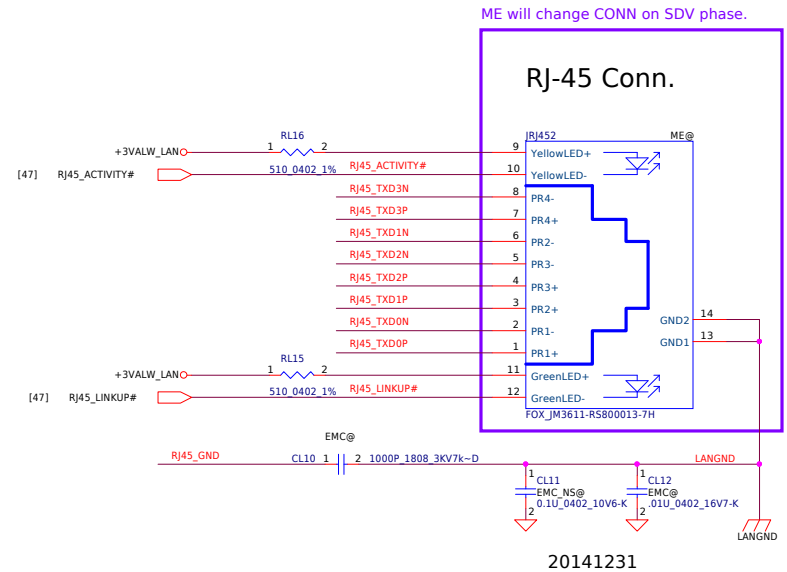
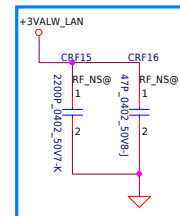
CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCH OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active

VPRO SKU : RL2 (@), RL25(VPRO@)

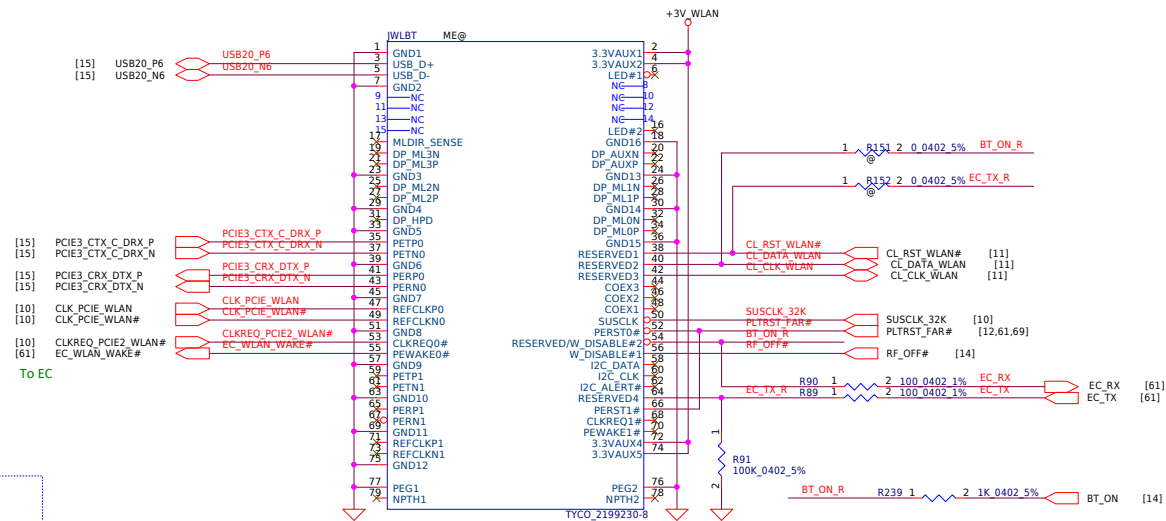
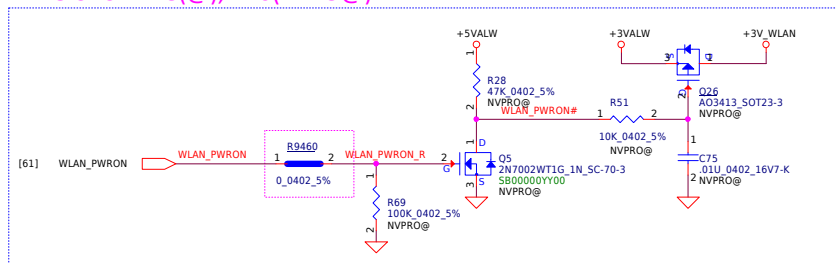
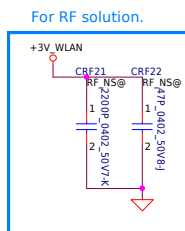





For RF solution.

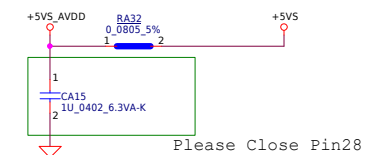
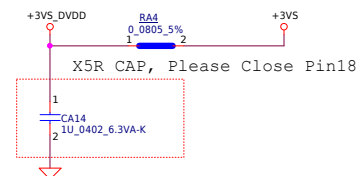
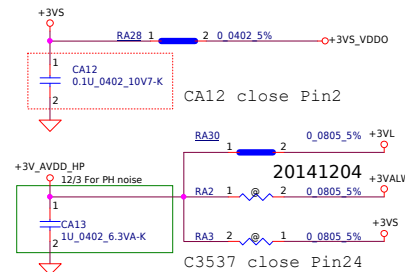
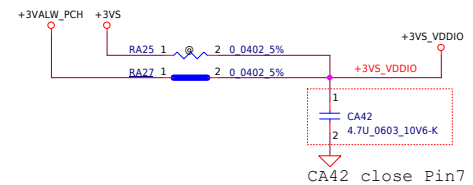
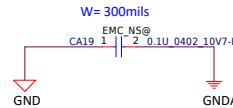
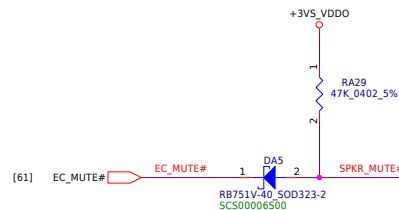
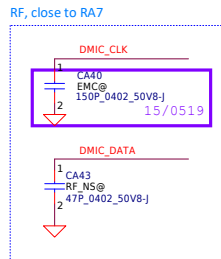
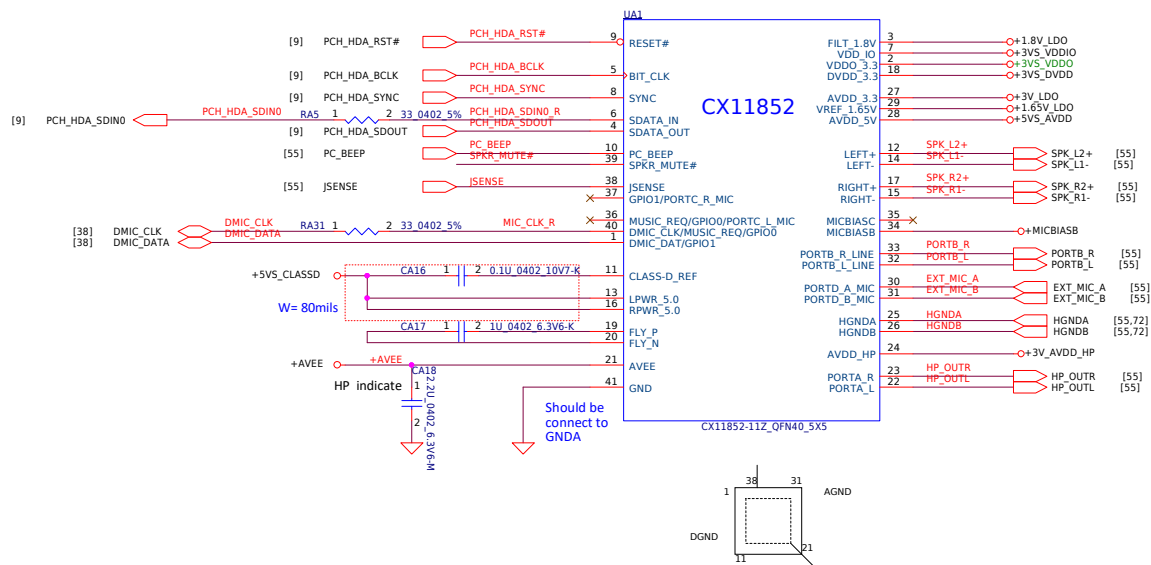
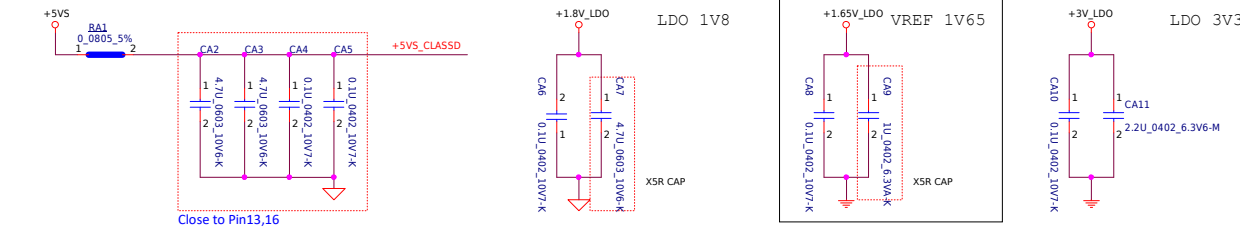


VPRO SKU : R48(@), R70(VPRO@)



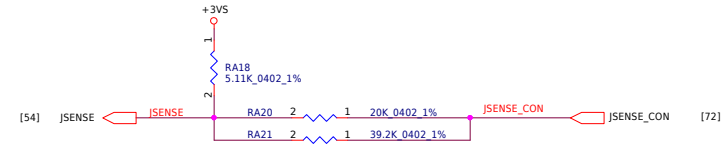
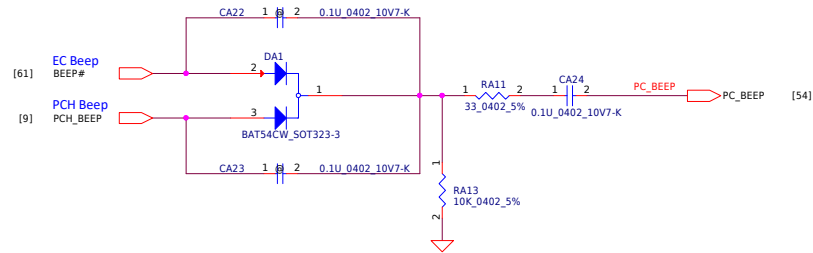
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				Size	DocumntNumber	Rev	
				Custpm	BE560	0.	
				Date:	Wednesday, September 31, 2014 5:56 PM		

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Issued Date	2013/09/07	Deciphered Date	2014/09/07	Card Reader	
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				Date:	Wednesday, September 23, 2014
				Sheet	51 of 99

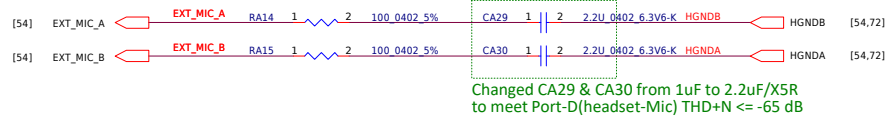


Apple --> EXT_MIC_A, HGND B
Nokia --> EXT_MIC_B, HGND A

PC BEEP



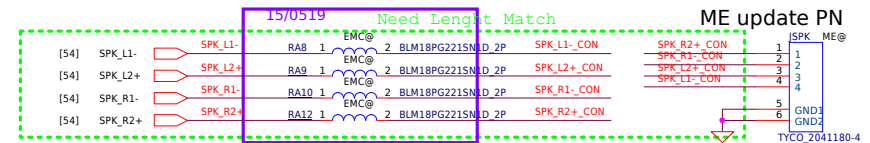
EXT. MIC/LINE IN Apple --> EXT_MIC_A, HGND B
Nokia --> EXT_MIC_B, HGND A



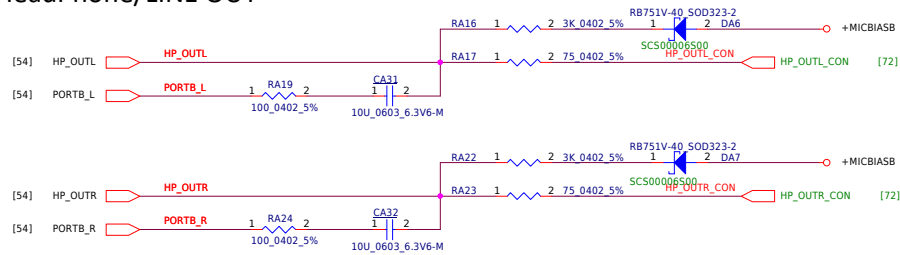
Changed CA29 & CA30 from 1uF to 2.2uF/X5R to meet Port-D(headset-Mic) THD+N <= -65 dB

Speaker OUT

SPK CONN.

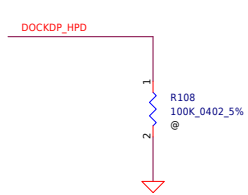
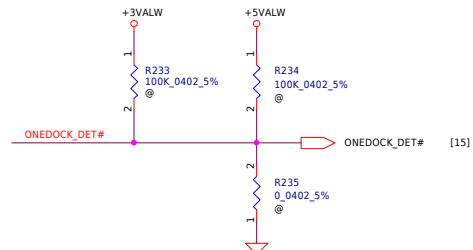
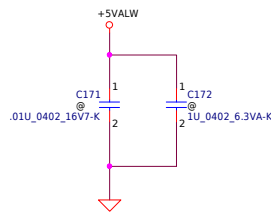
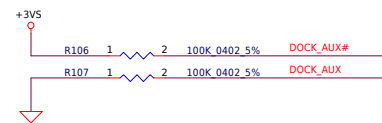
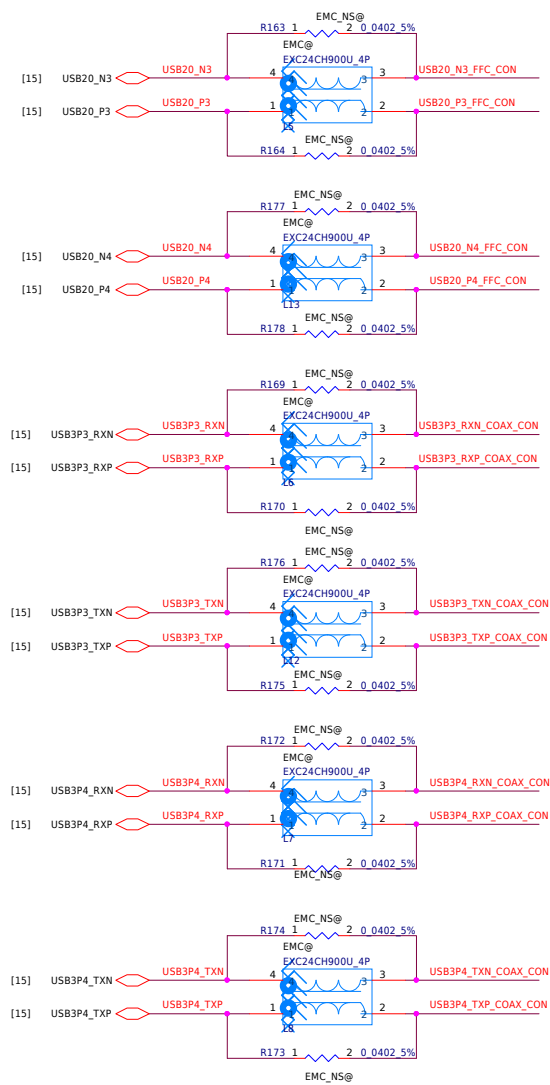


HeadPhone/LINE OUT

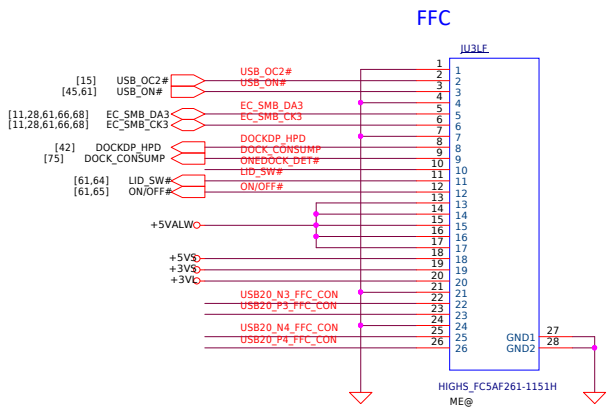
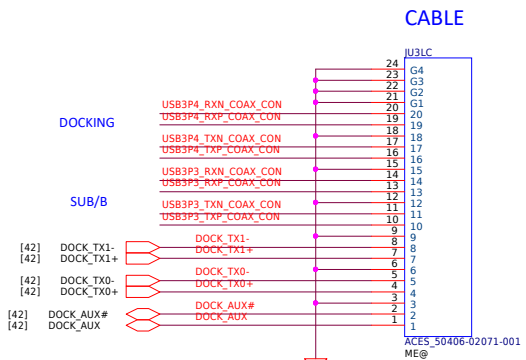


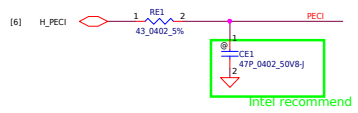
CA31, CA32 change to 4.7uF for Quality requirement

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				Custom	0.1
				BE560	
				Date:	Wednesday, September 23, 2014
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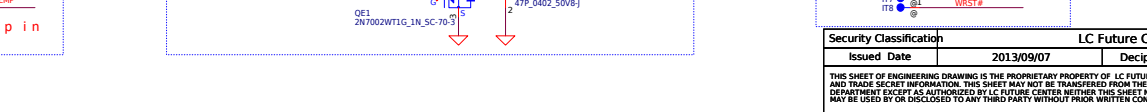
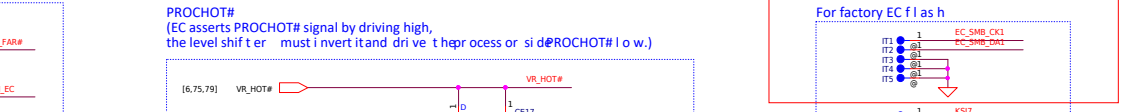
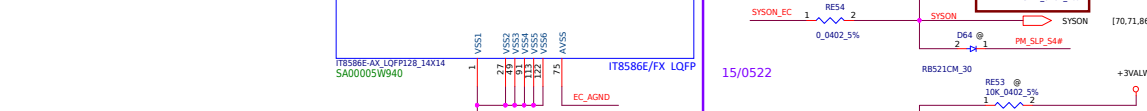
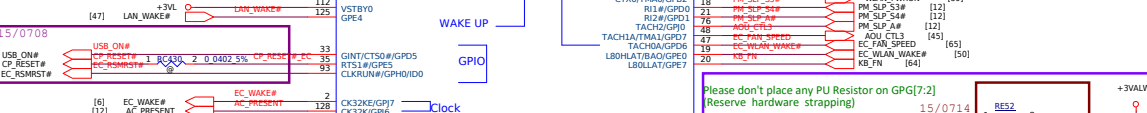
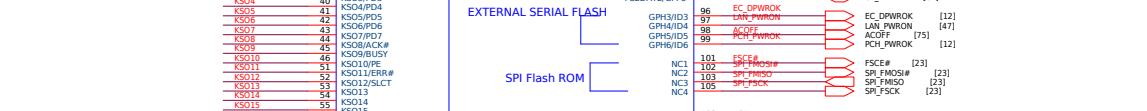
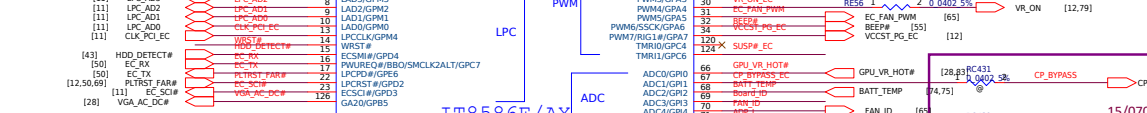
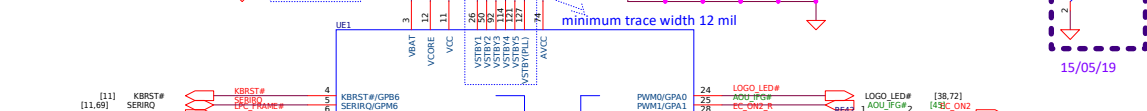
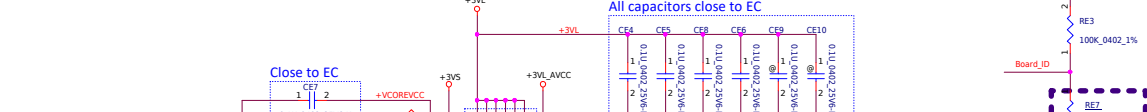
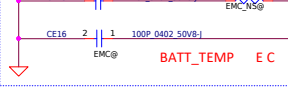
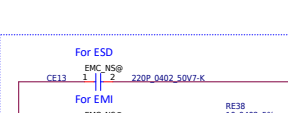
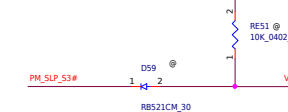
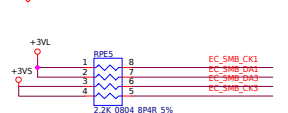
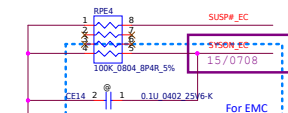
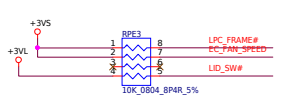
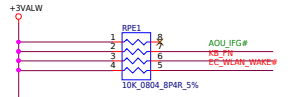
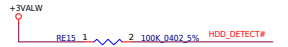
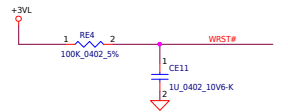


1. AC Capacitor place on Sub/B
2. Need to check with MUX IC vendor whether st ill need AC cap bet ween MUX IC and device.

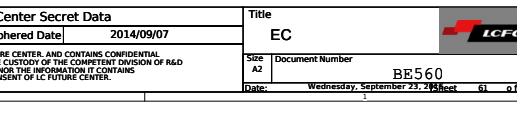
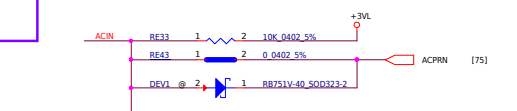
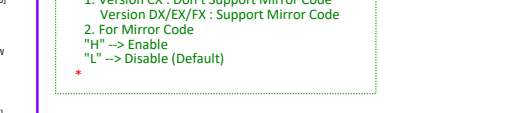
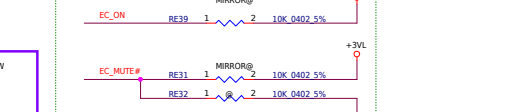
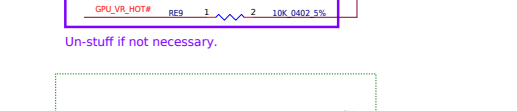
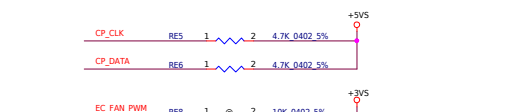
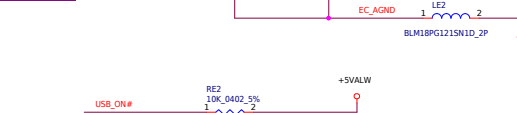
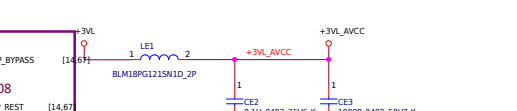
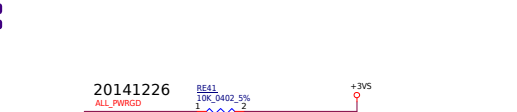




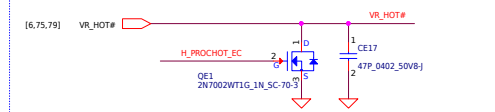
Intel recommend



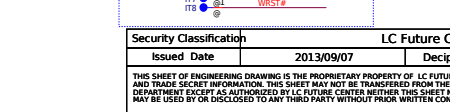
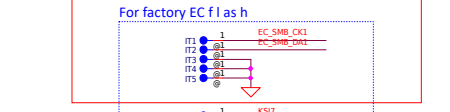
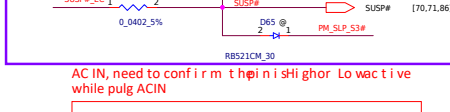
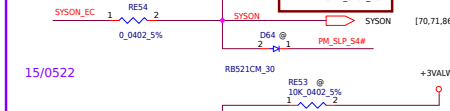
Vcc	3.3V +/- 5%				
RE3	100K +/- 1%				
Board ID	RE7	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SVT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	



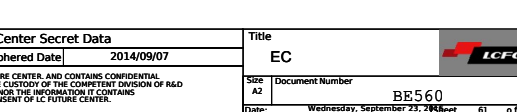
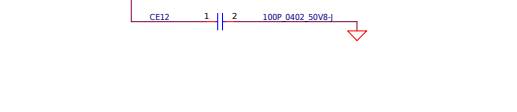
PROCHOT#
(EC asserts PROCHOT# signal by driving high, the level shifter must invert and drive the process or silicon PROCHOT# low.)



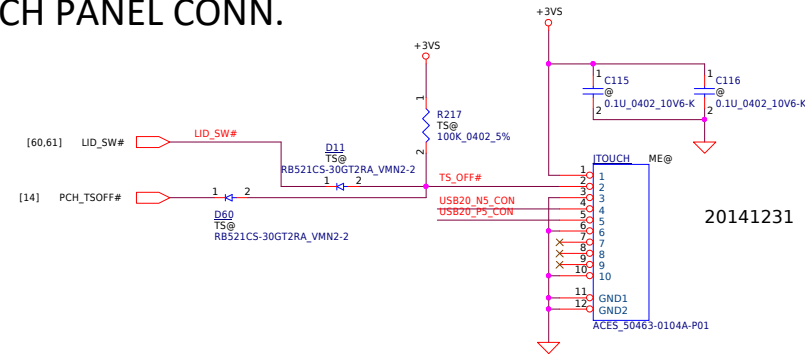
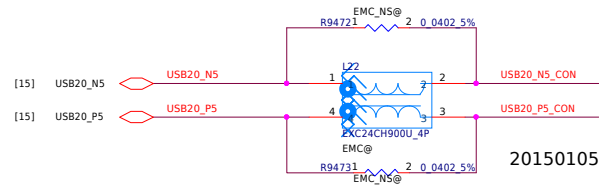
Please don't place any PU Resistor on GPG[7:2] (Reserve hardware strapping)



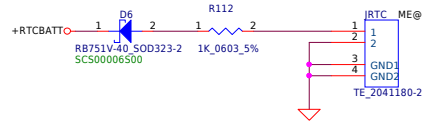
AC IN, need to confirm the pin in the shigor low active while pulg ACIN



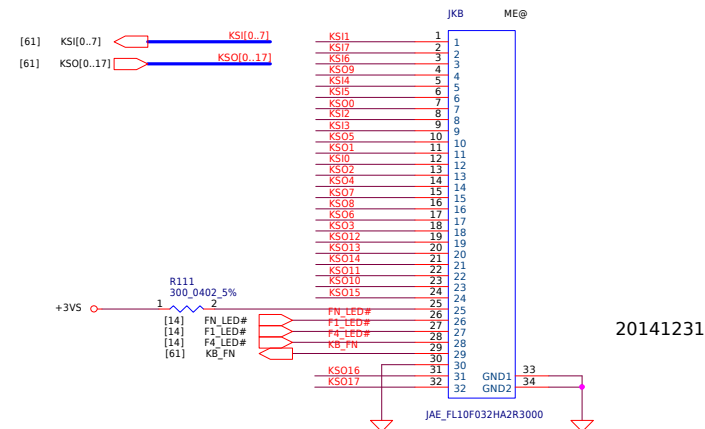
TOUCH PANEL CONN.



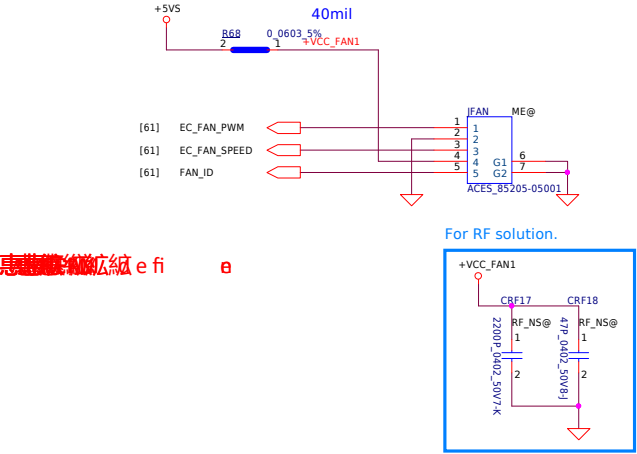
RTC CONN.



KB CONN



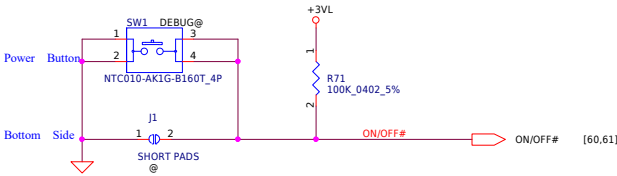
FAN CONN.



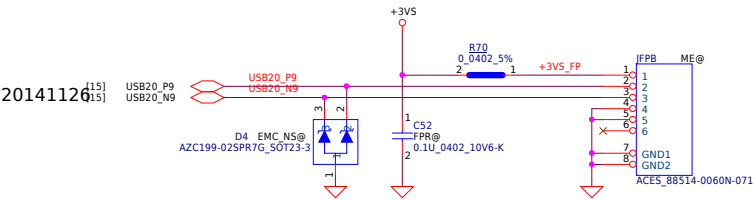
PWR BTN/LID SW CONN.

For 14" on board
For 15" on Sub/B

ON/OFF Switch --> Sub/ B

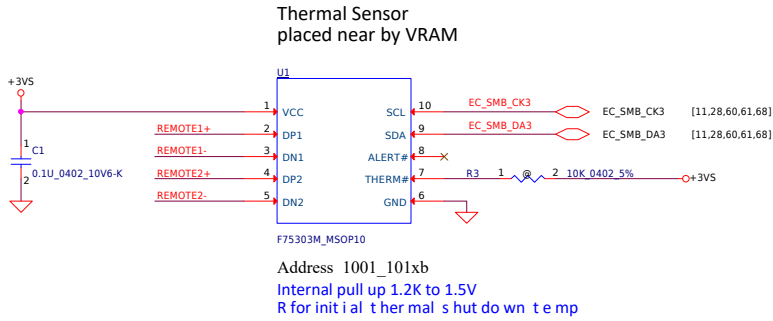


FingerPrint CONN.

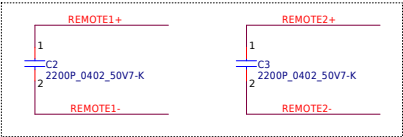


Lid Switch --> Sub/B

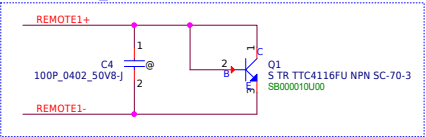
Thermal Sensor



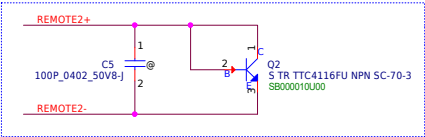
Close to U1



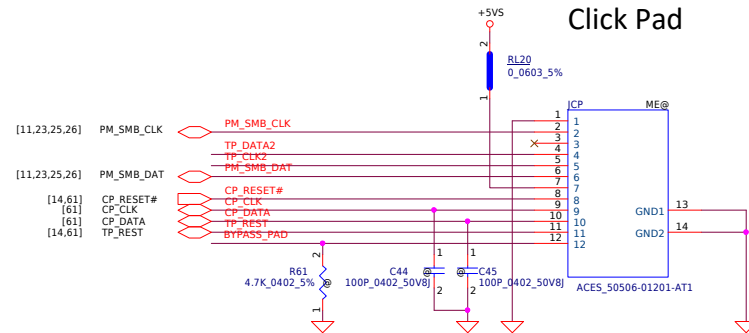
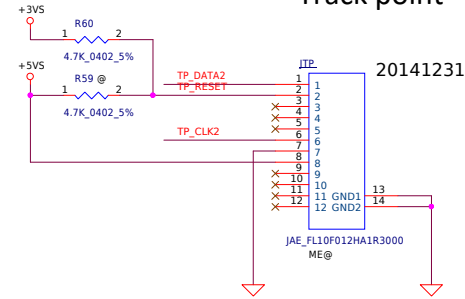
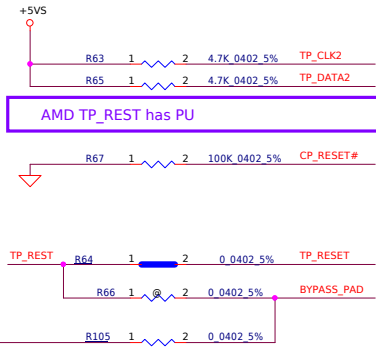
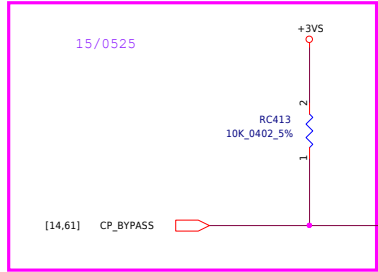
Close to +VCC_CORE

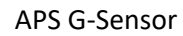


Close JDIMM1&JDIMM2

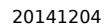


REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

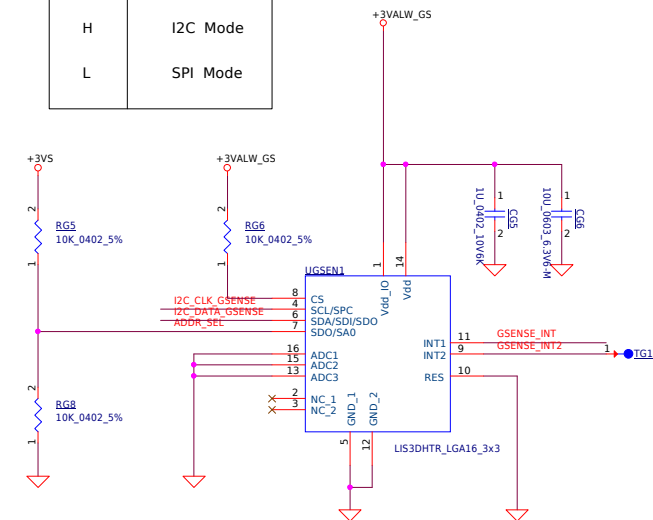





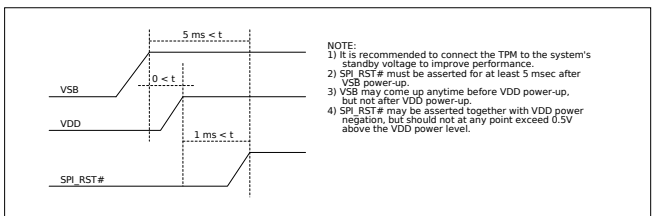
P/N	ADDR_SEL	Address
LIS3DH	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX023-1025	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)



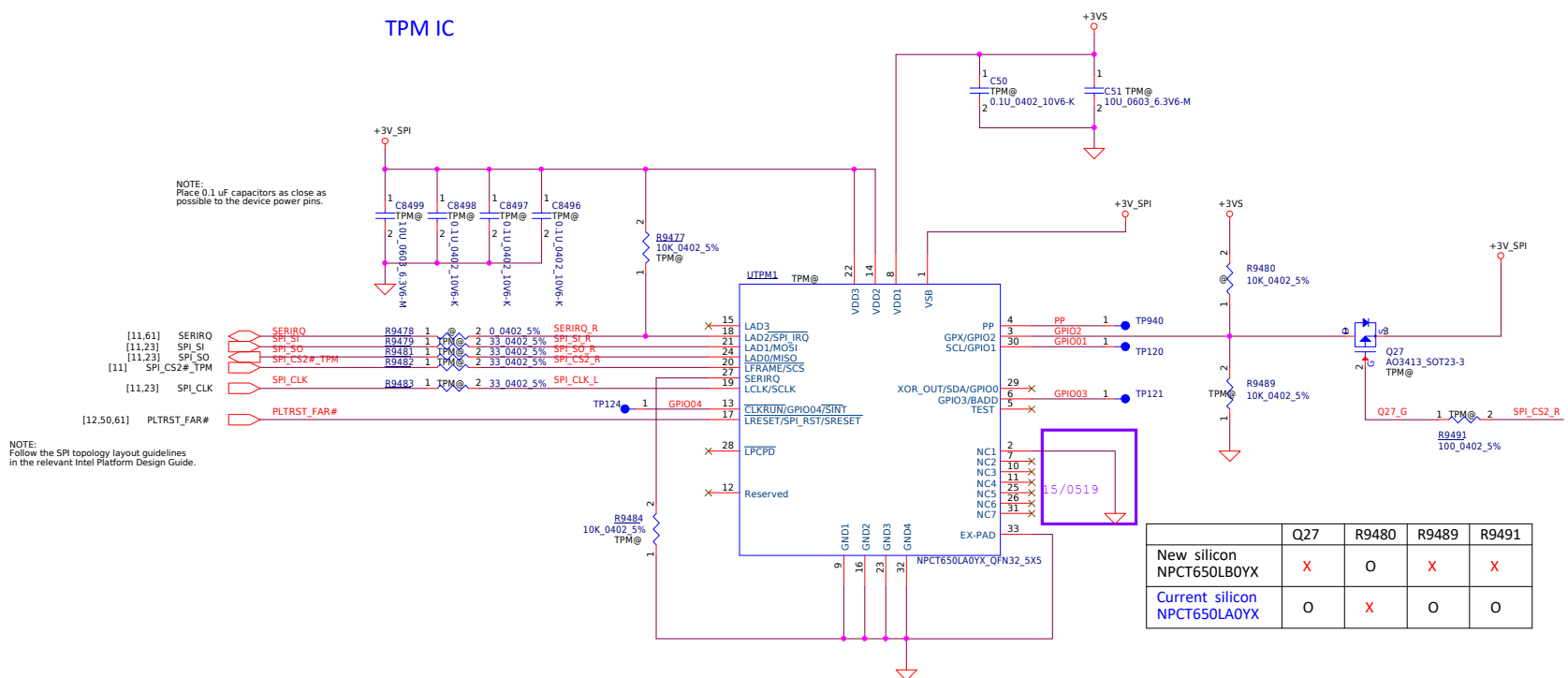
P/N	Mode Selection
H	I2C Mode
L	SPI Mode



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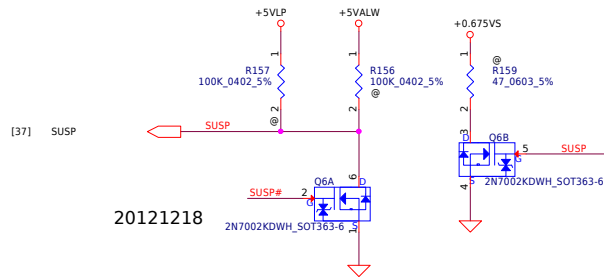
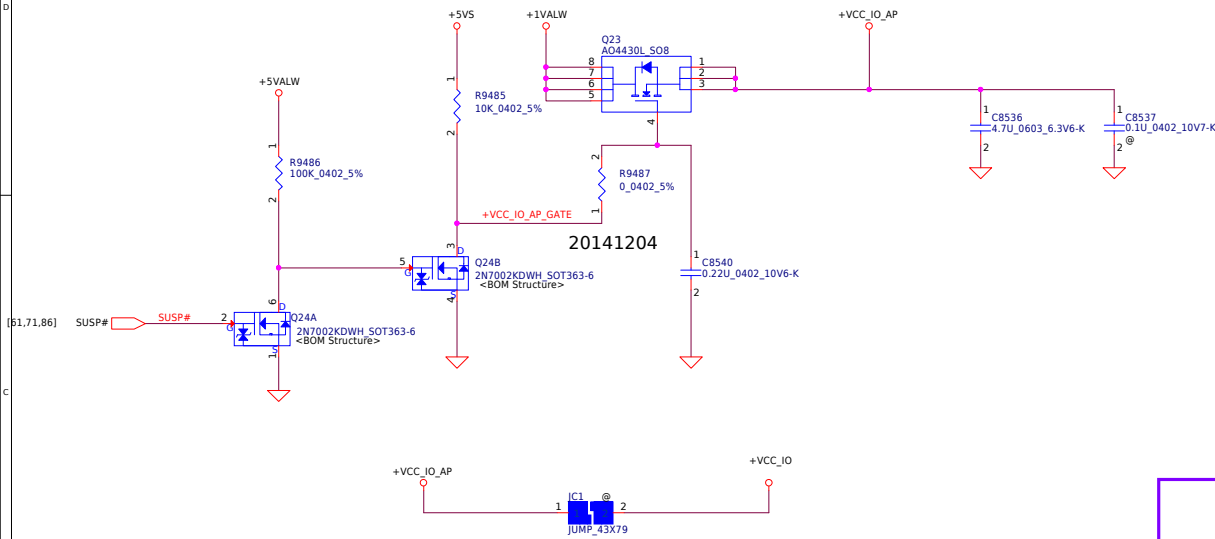
TPM IC



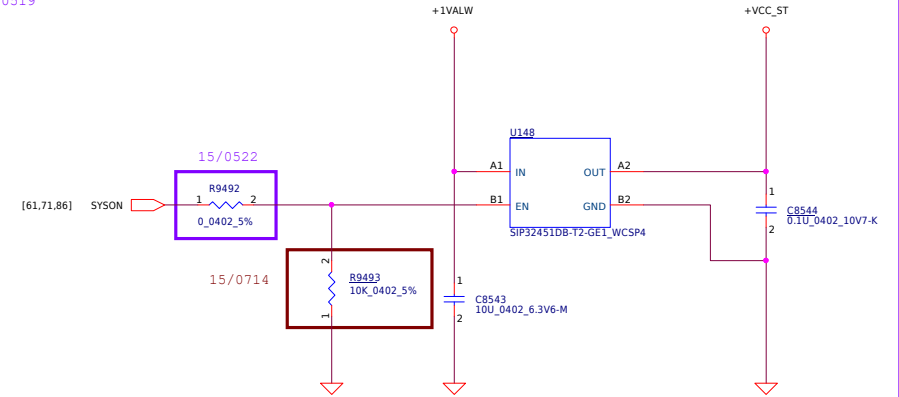
	Q27	R9480	R9489	R9491
New silicon NPCT650LB0YX	X	O	X	X
Current silicon NPCT650LA0YX	O	X	O	O

+1VALW to +VCC_IO_AP

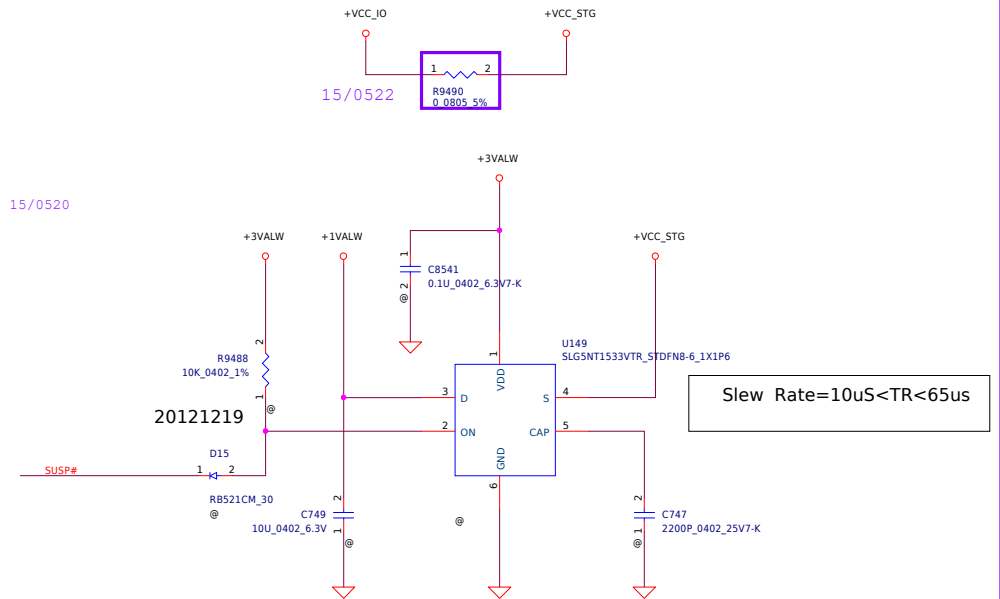
3A



15/0519

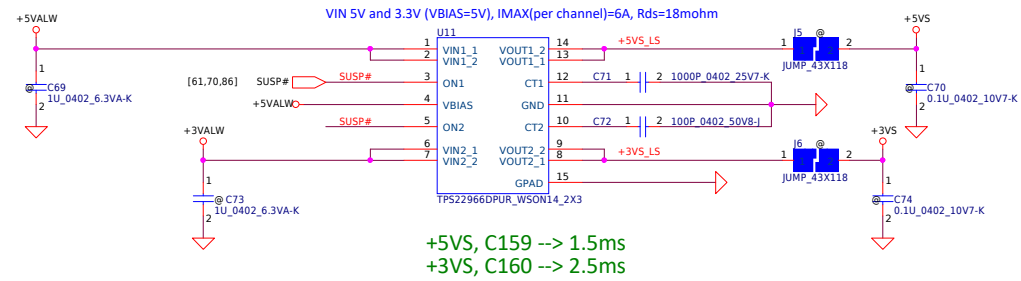


15/0520

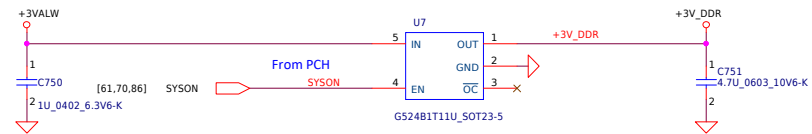


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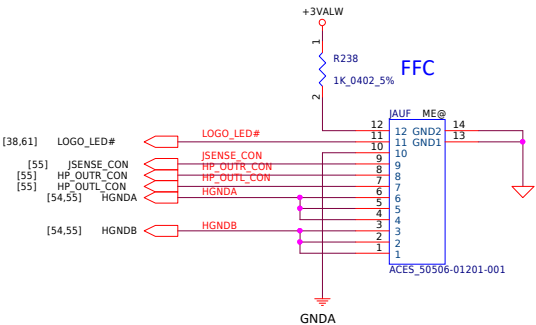
Load Switch
+5VALW To +5VS
+3VALW To +3VS

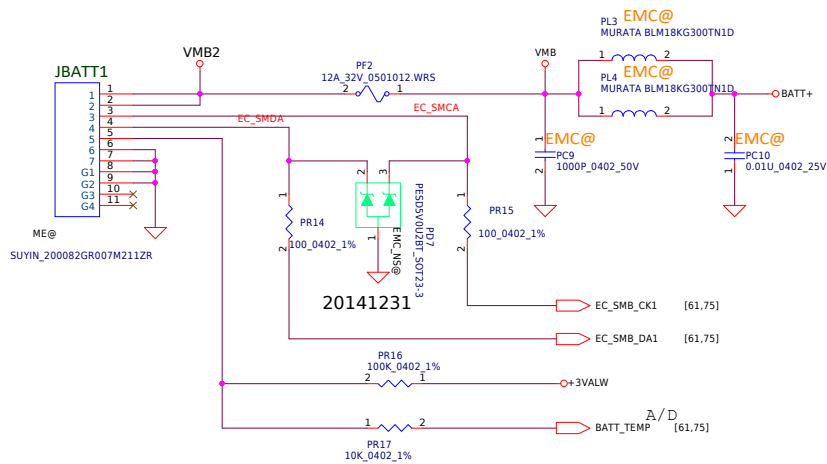


+3VALW to +3V_DDR

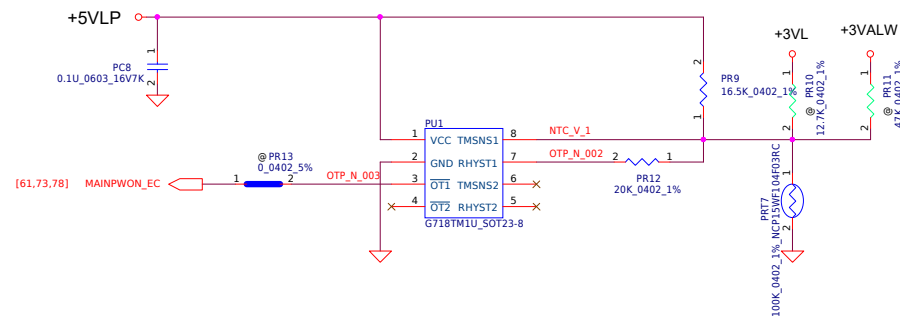


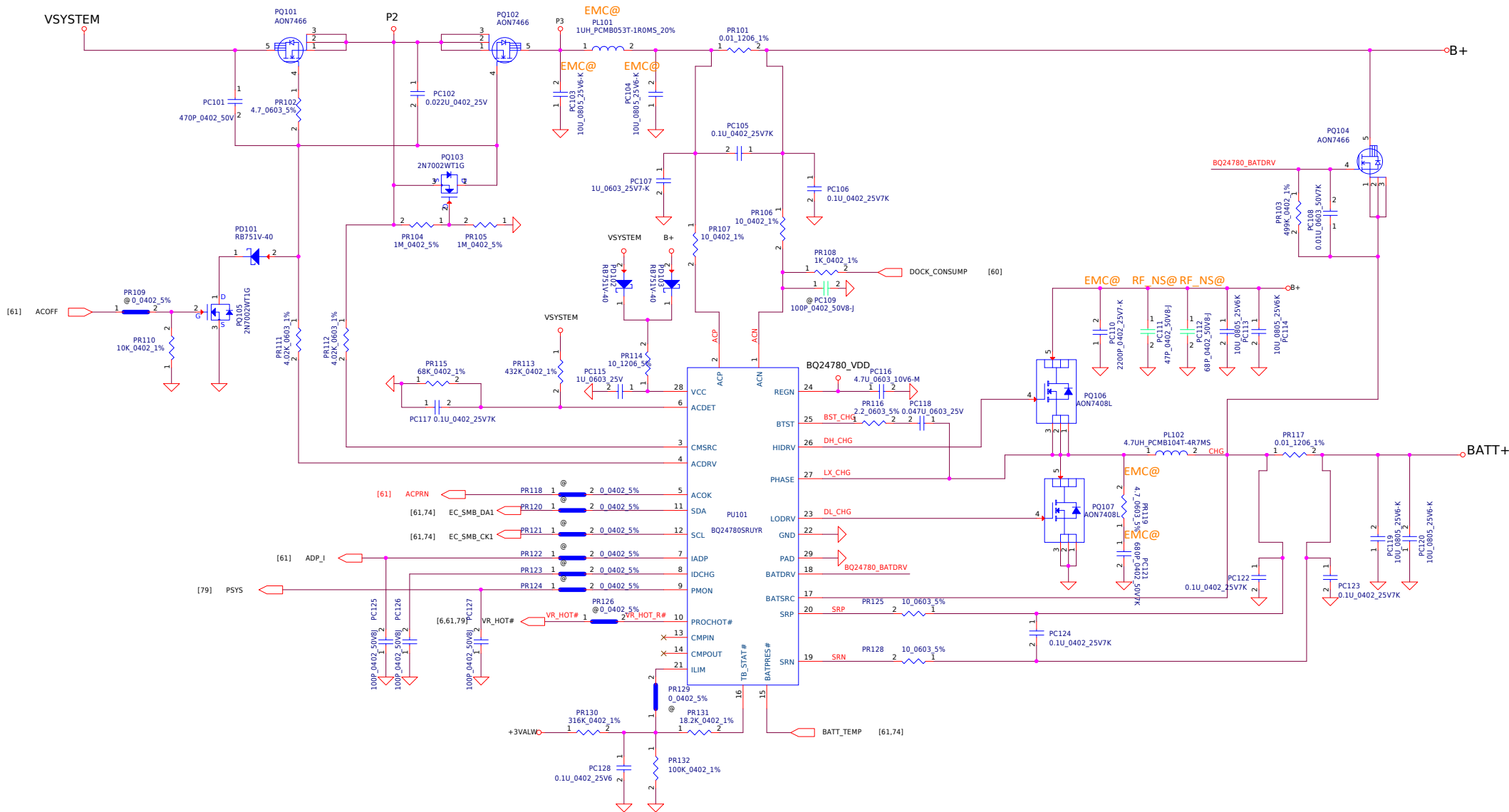
For Edge 15" Audio board CONNECTOR




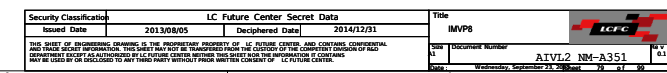


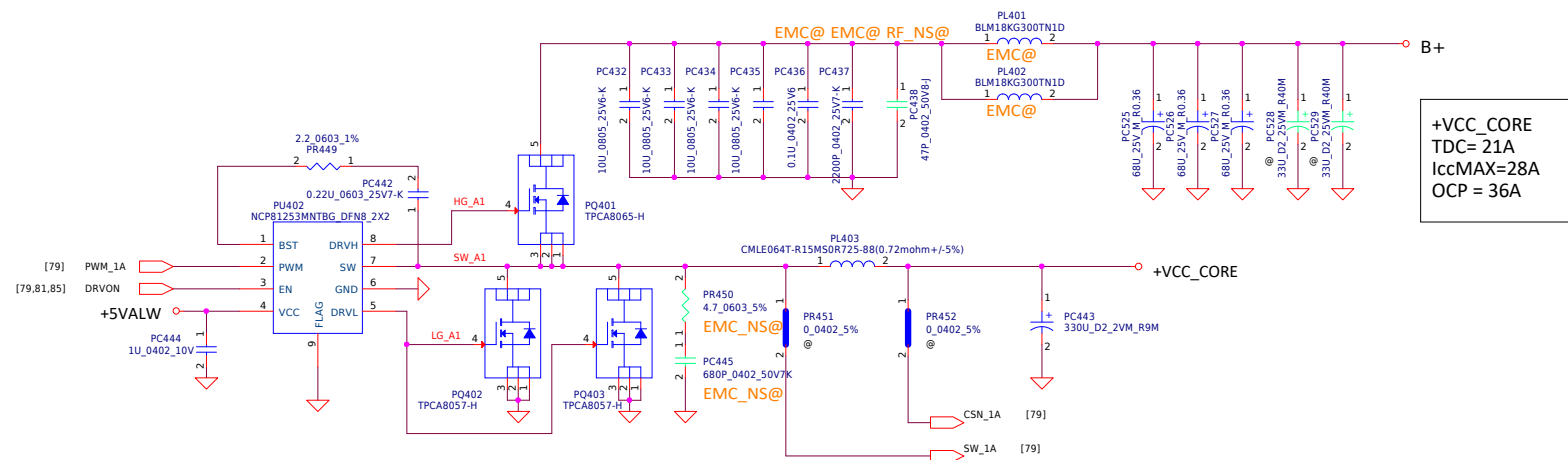
PRT7 under CPU bottom side :
CPU thermal protection at 93 \pm 3 degree C
Recovery at 56 \pm 3 degree C



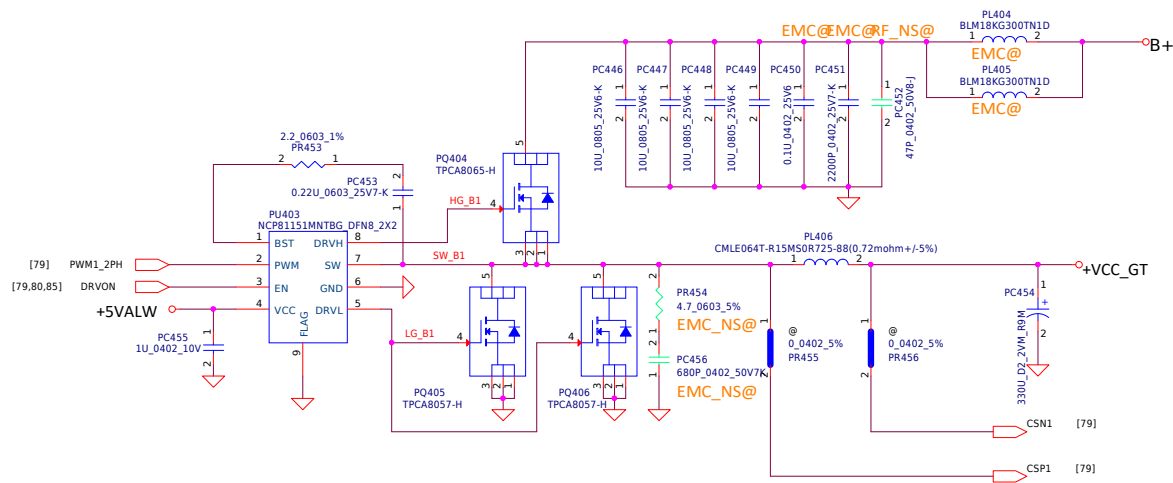


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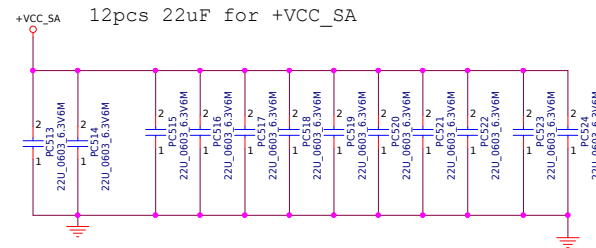
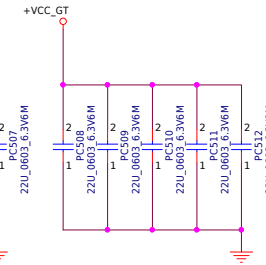
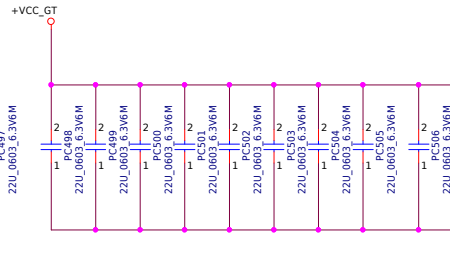
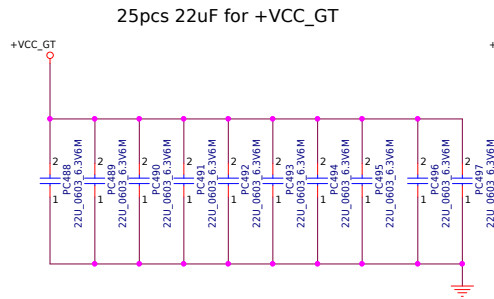
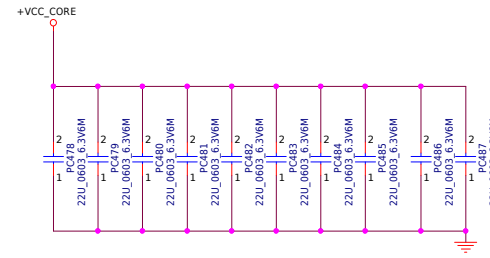
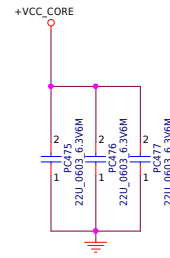
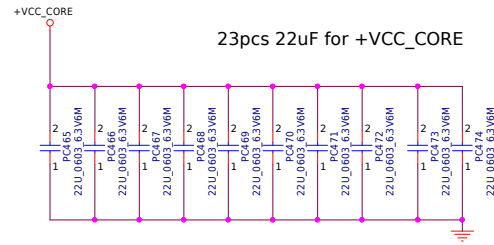


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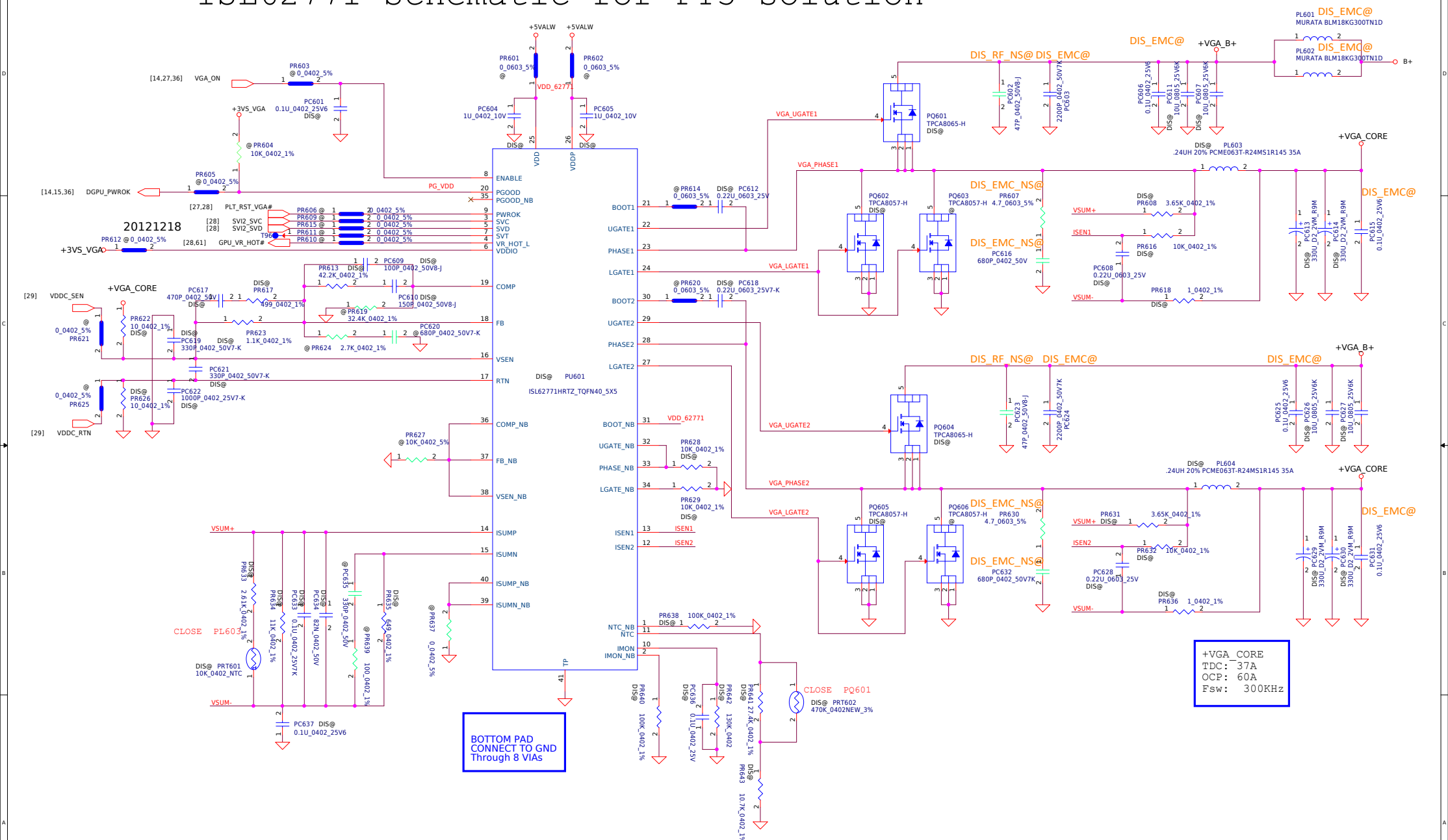
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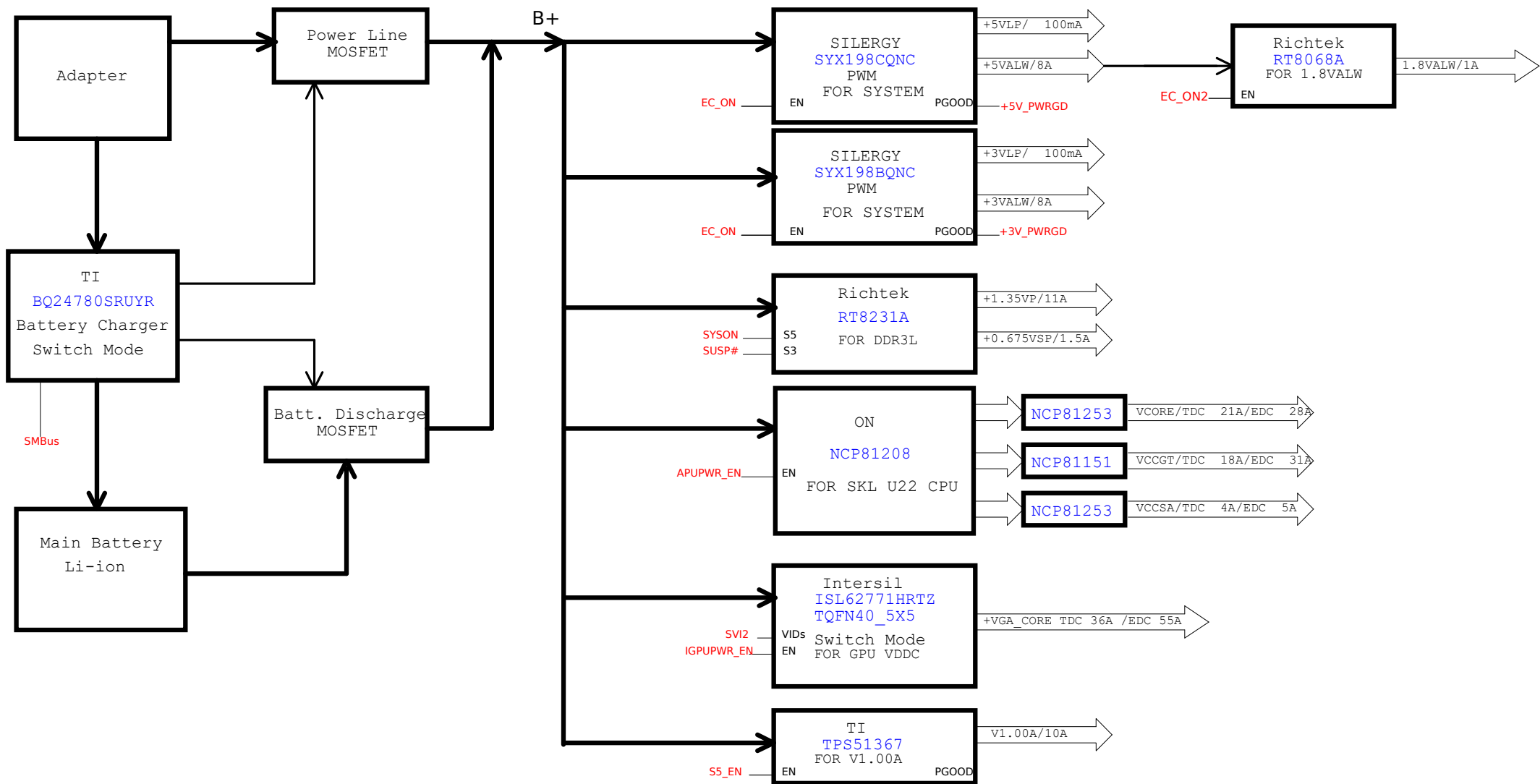
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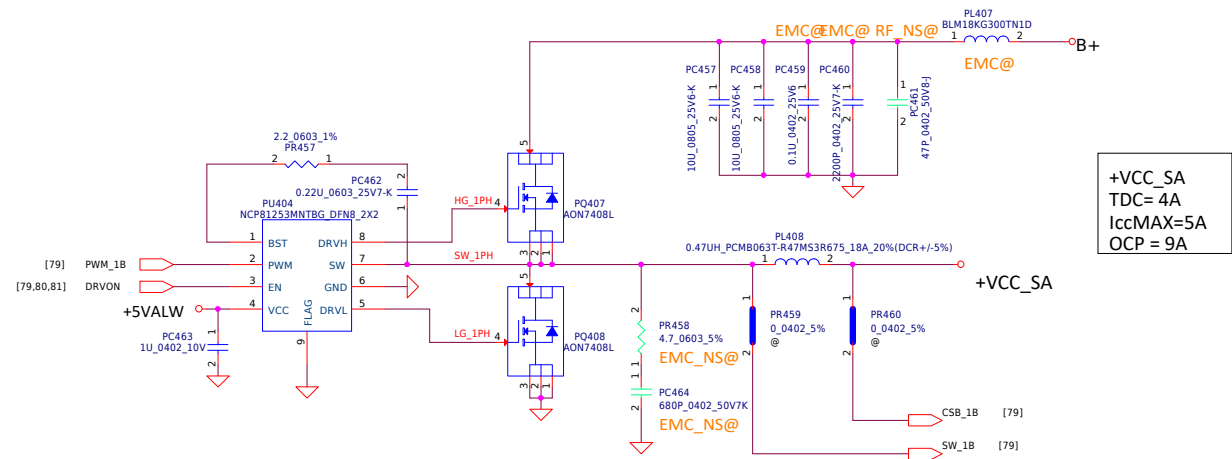


ISL62771 Schematic for FT3 solution

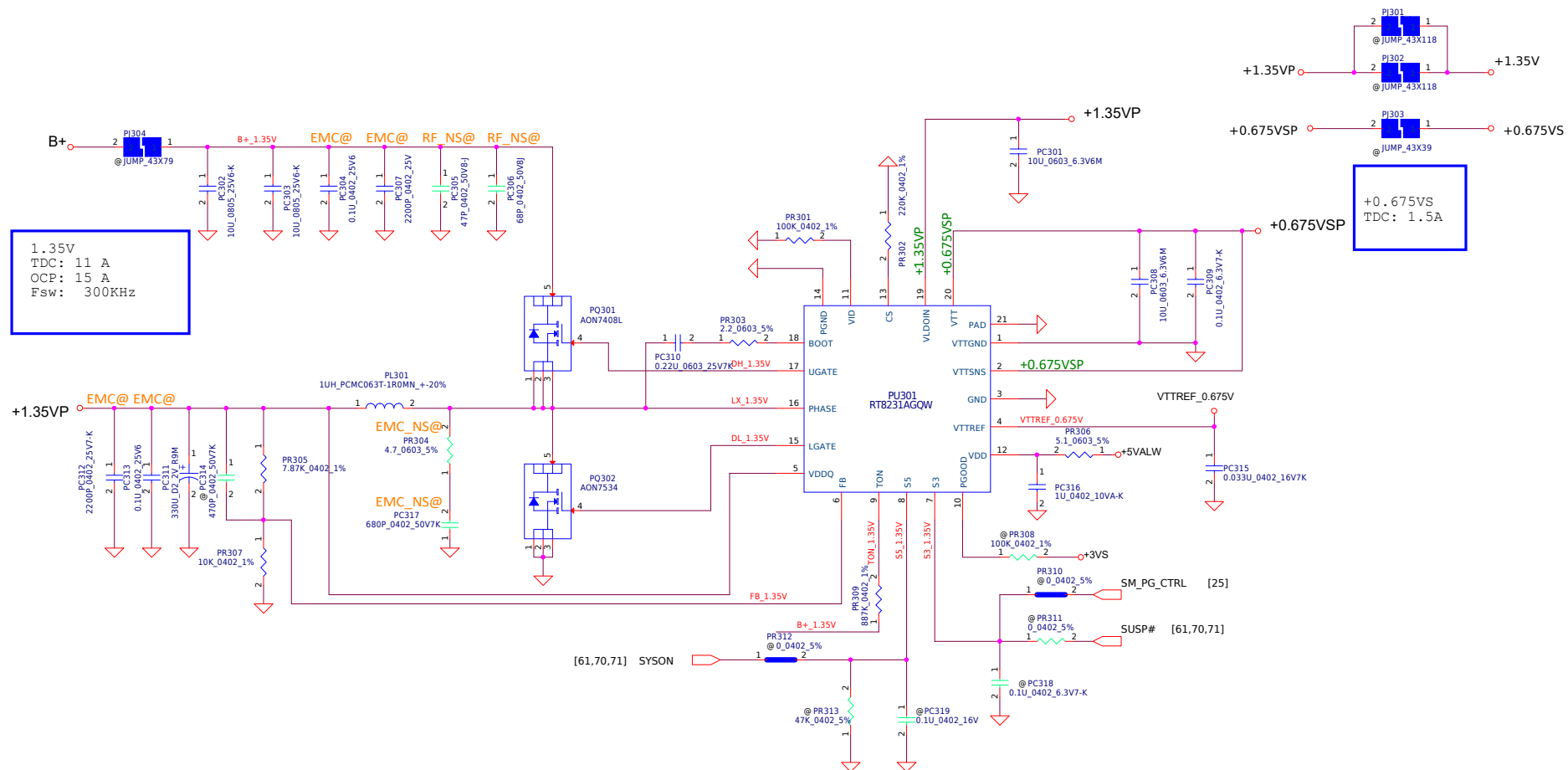


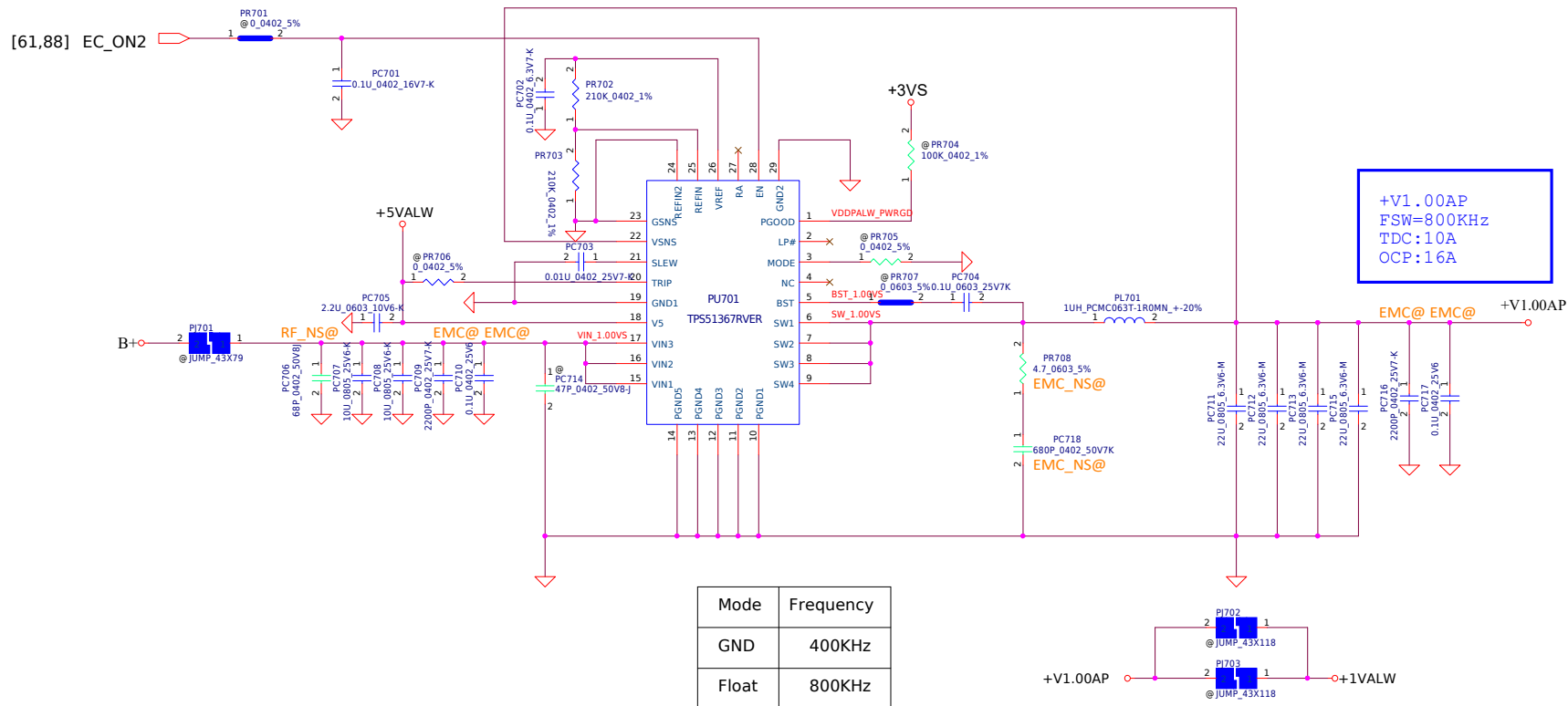
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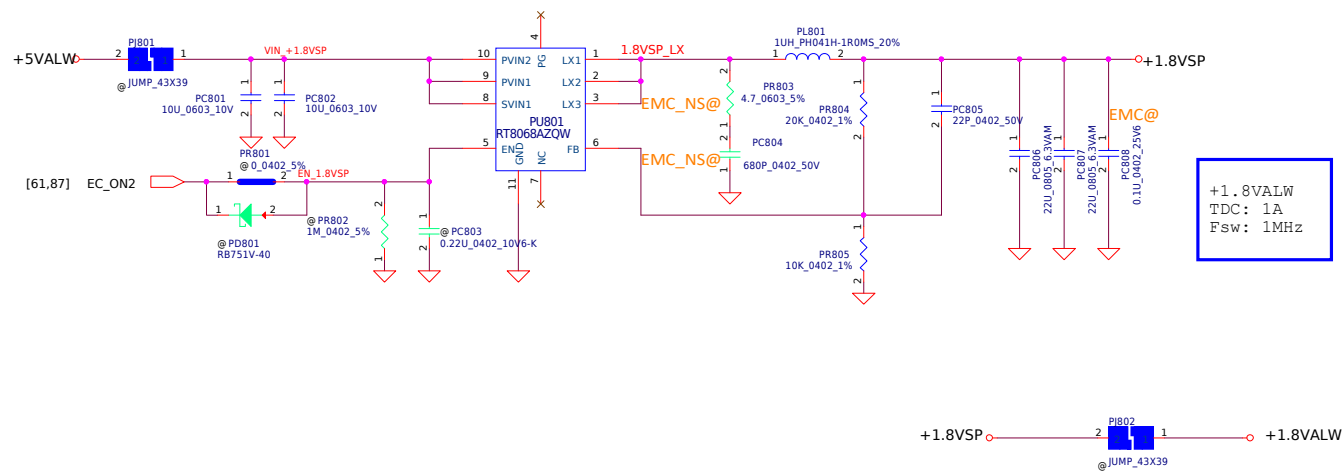




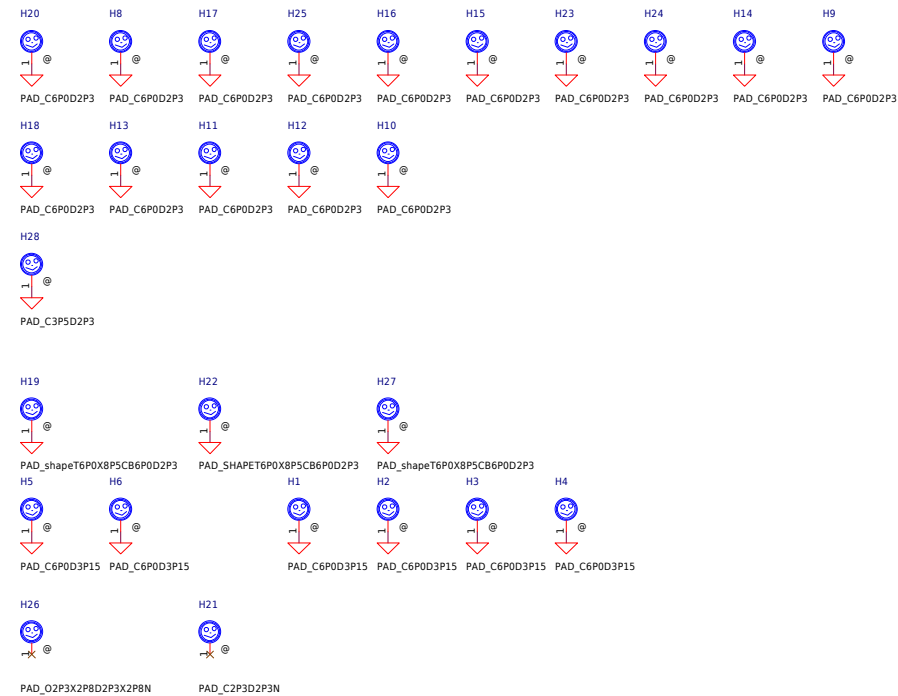
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Screw Hole



PCB Fedical Mark PAD



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