

LCFC Confidential

G Project M/B Schematics Document


AMD FT3B Beema SOC with DDRIIL

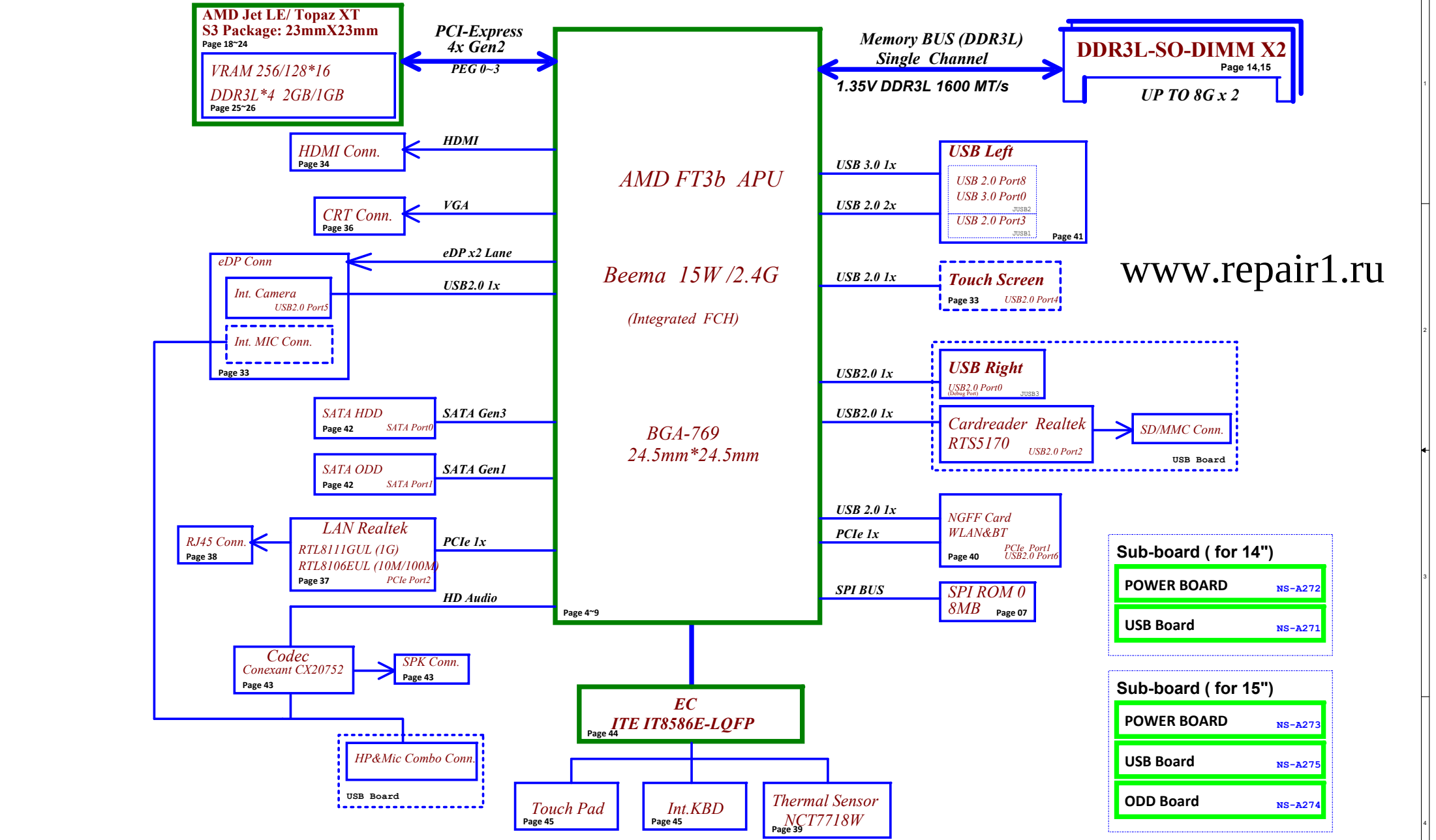
AMD JET-LE

2014-2-12


REV: 0.4

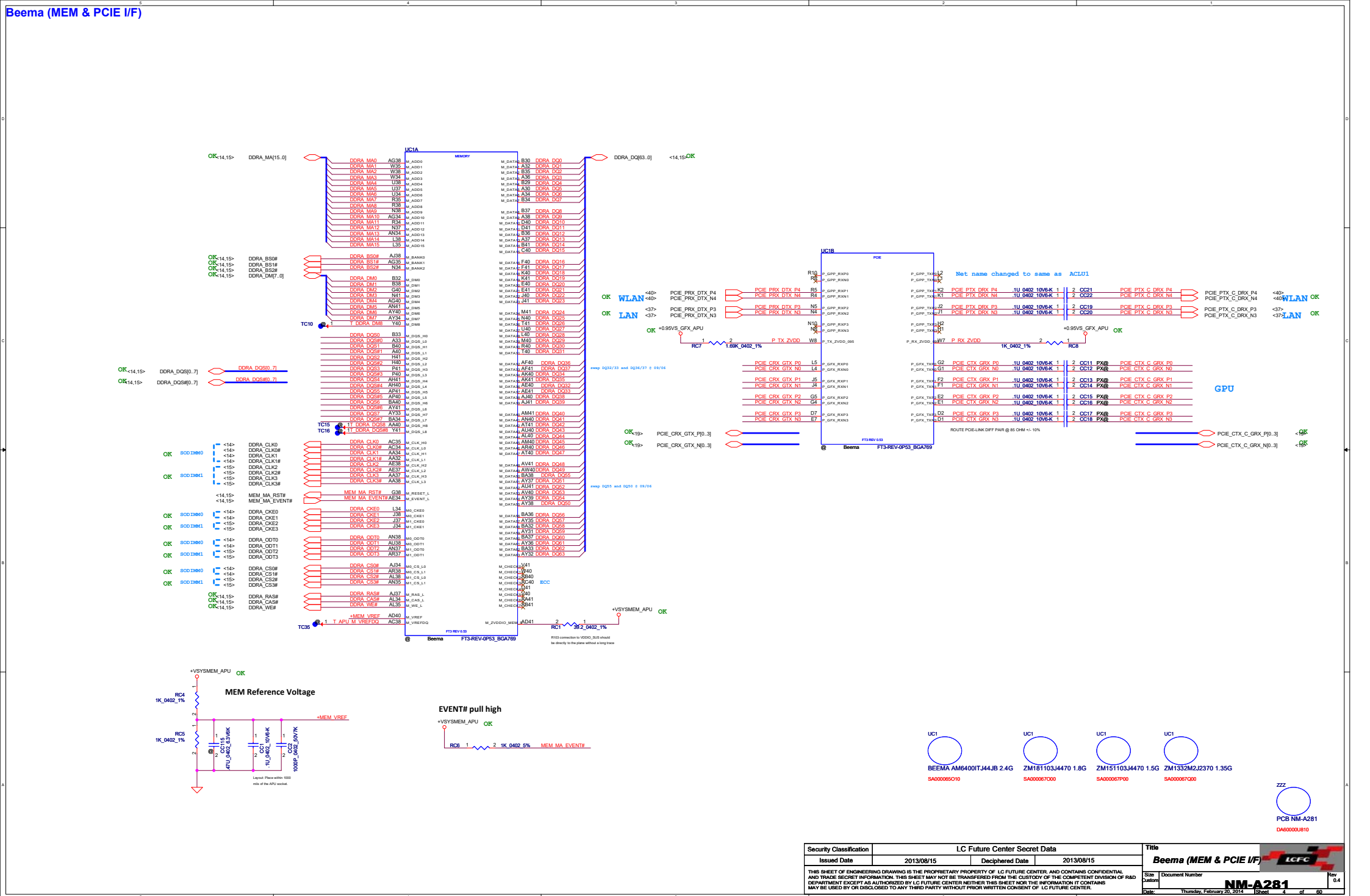
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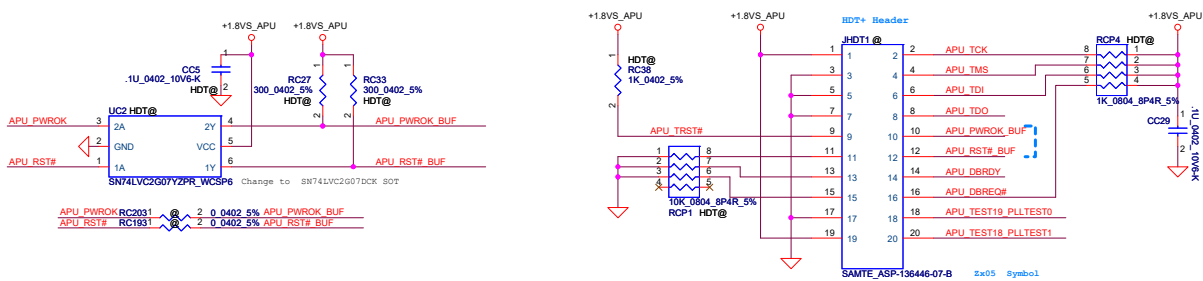
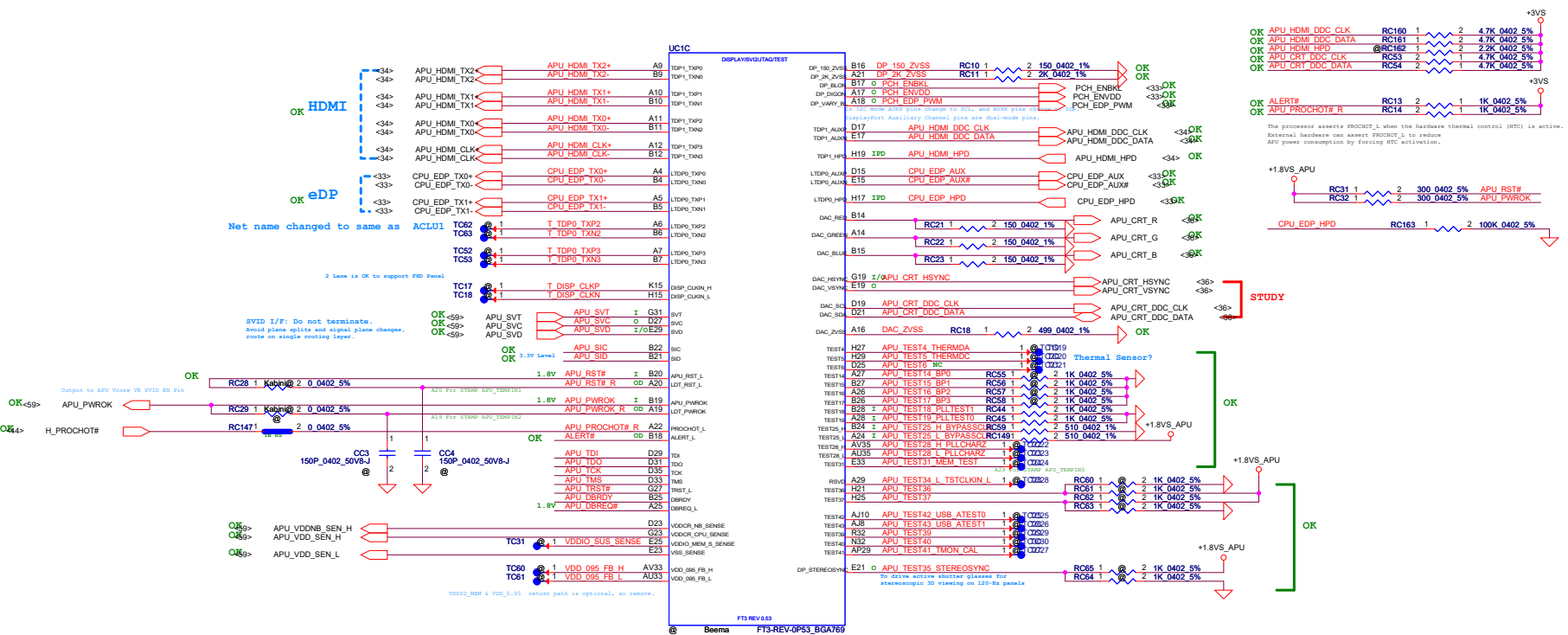
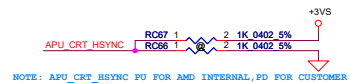
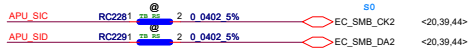



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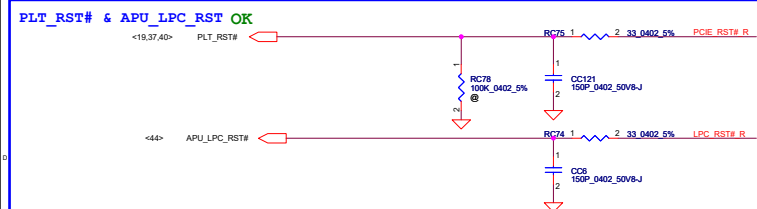


Beema (DISPLAY/CLK/MISC)



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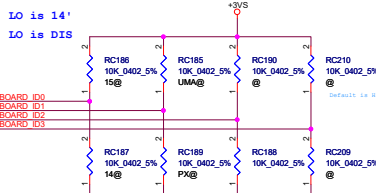
Beema (GEVENT/GPIO/SD/AZ)



Broad ID OK

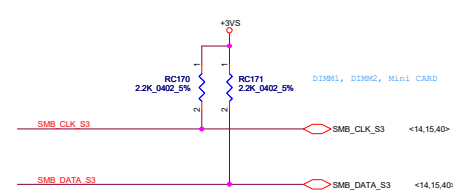
ID0 HI is 15' , LO is 14'
ID1 HI is UMA , LO is DIS

GP1049
GP1051
GP1071
GP1070

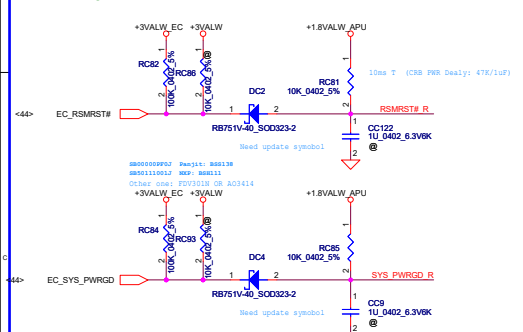


SP093/50/71 requires material R0 or R1, so used for Board 1
GP1070 is reserved and has internal R0

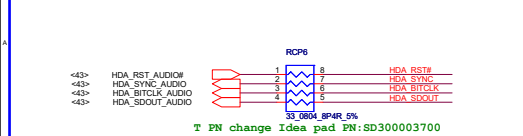
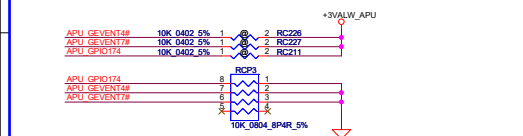
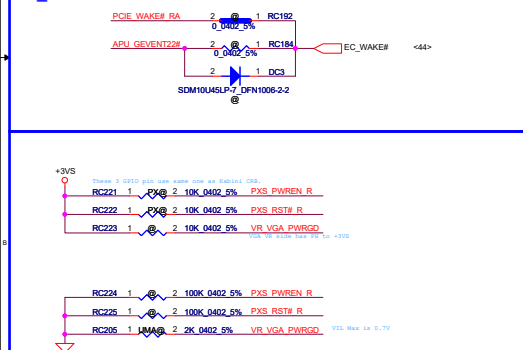
SMB_CLK_S3 OK



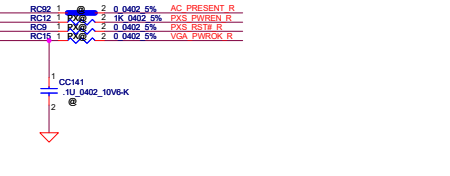
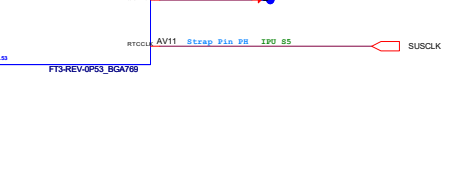
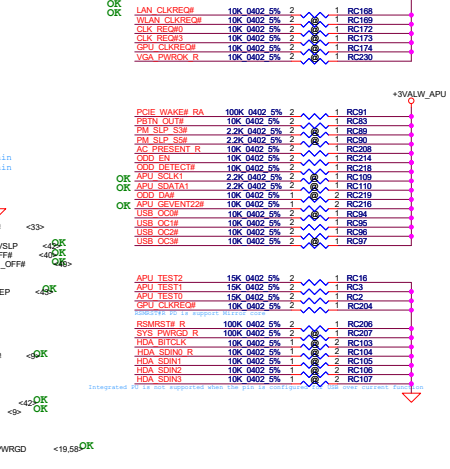
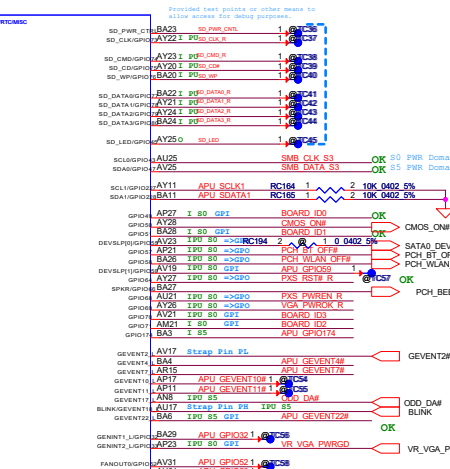
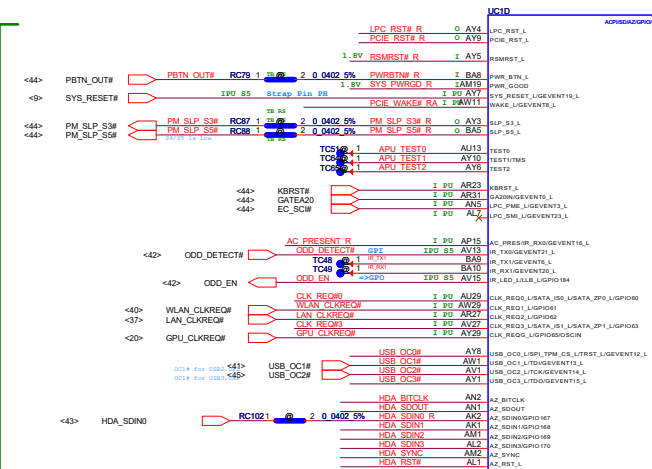
RSRST# OK



EC_WAKE# OK



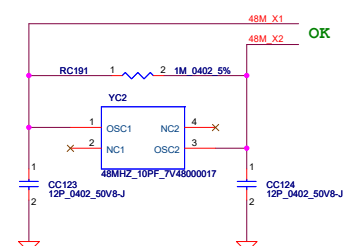
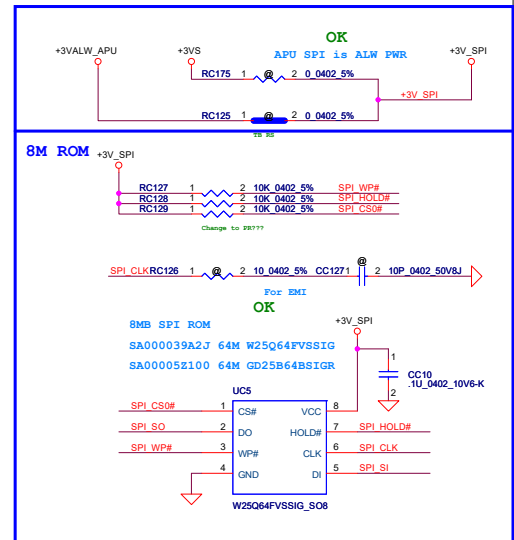
OK




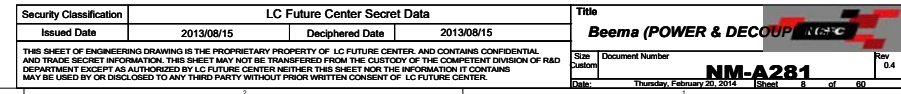
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48MHz/10pF Crystal



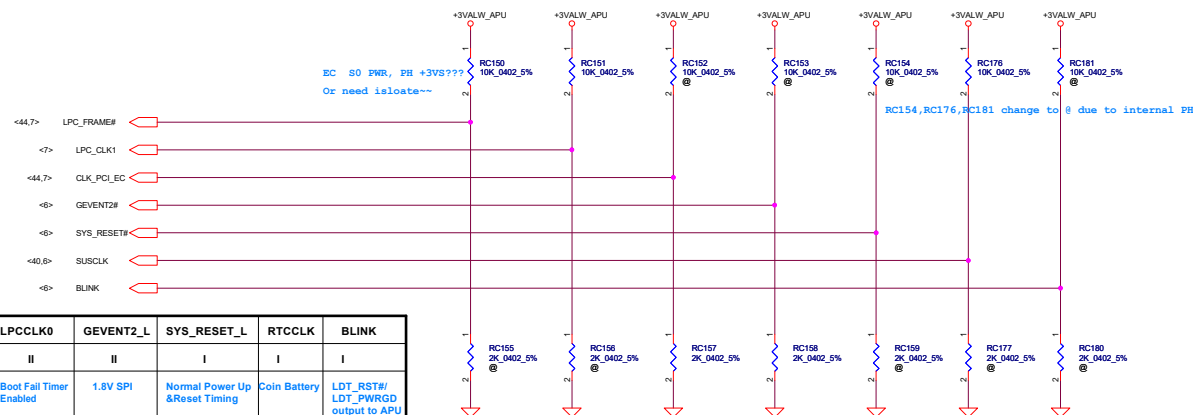
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STRAP PINS

Signal	LFRAME_L	LPCCLK1	LPCCLK0	GEVENT2_L	SYS_RESET_L	RTCCLK	BLINK
Type	II	II	II	II	I	I	I
PULL HIGH	SPI ROM Default	Internal CLK Gen Default	Boot Fail Timer Enabled	1.8V SPI	Normal Power Up & Reset Timing Default	Coin Battery Default	LDT_RST#/ LDT_PWRGD output to APU Default
PULL LOW	LPC ROM	External CLK Gen	Boot Fail Timer Disabled Default	3.3V SPI Default	Reserved	Direct DC	Reserved

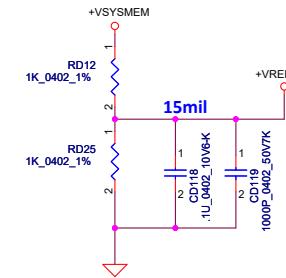
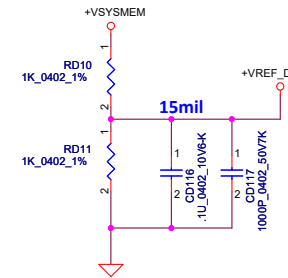
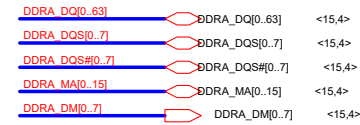
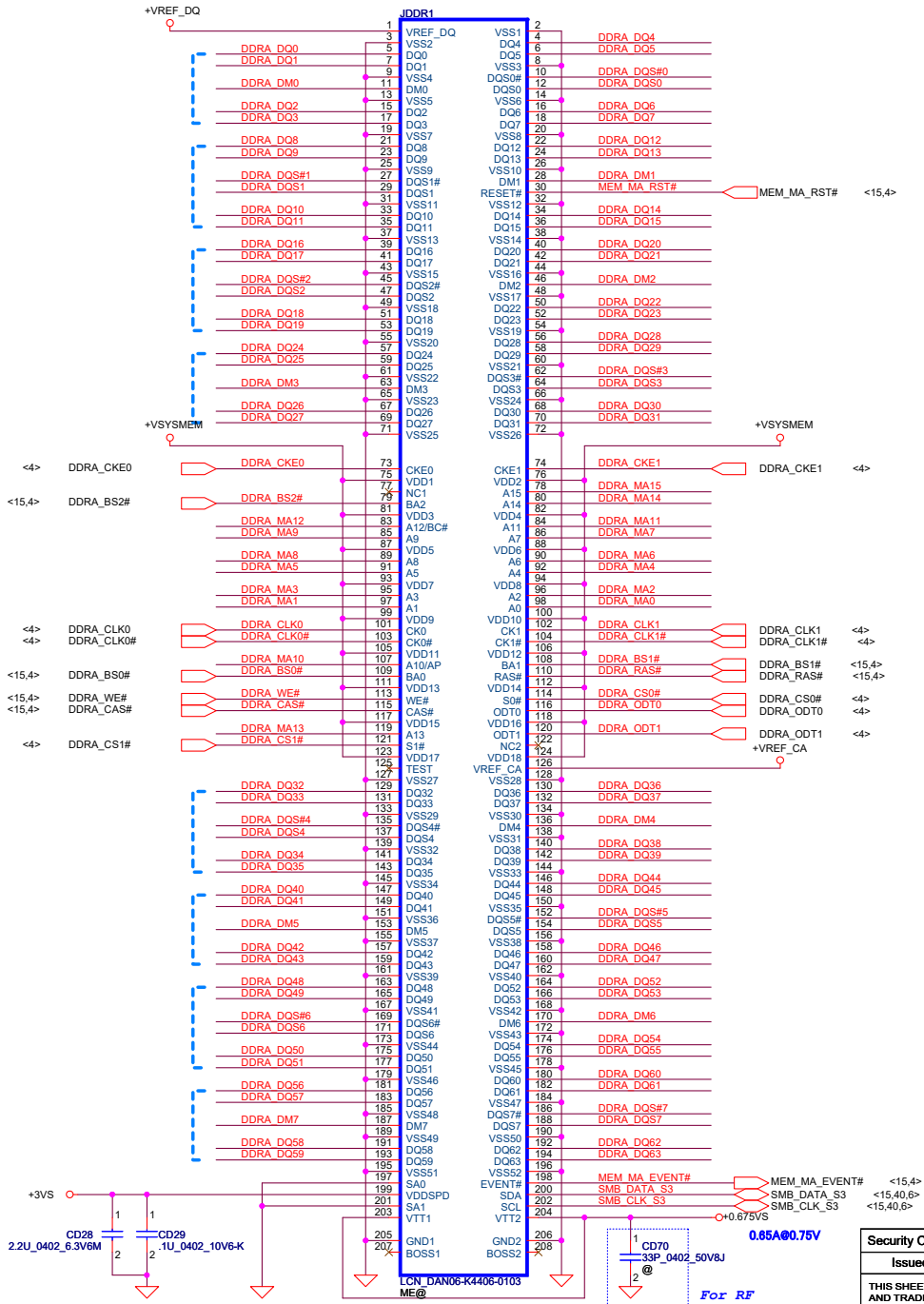
Type I straps become valid immediately after capture with the rising edge of RSMRST_L.
Type II straps become valid after PWR_GOOD is asserted
All Strap pins must be configured with either external pull-up or pull-down resistors.



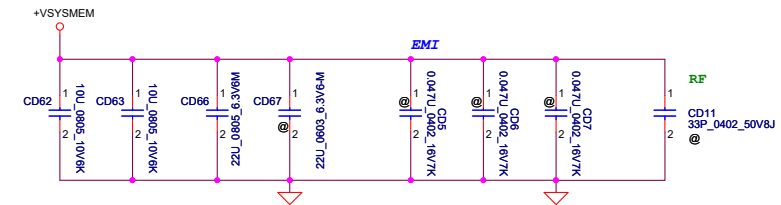
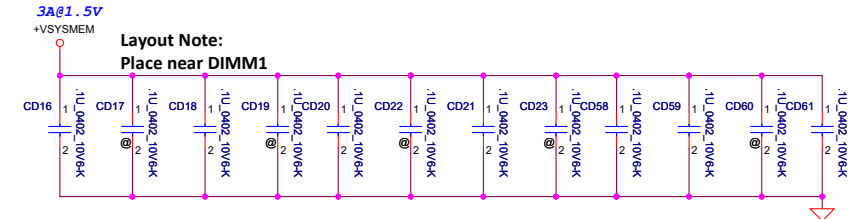
5					4					3					2					1				
D																								
C																								
B																								
A																								
5					4					3					2					1				

5	4	3	2	1																																			
D				D																																			
C				C																																			
B				B																																			
A				A																																			
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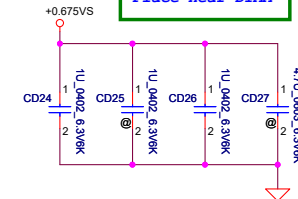


DDR3 SO-DIMM A

Layout Note:
Place near DIMM1



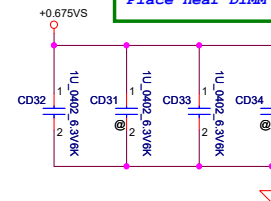
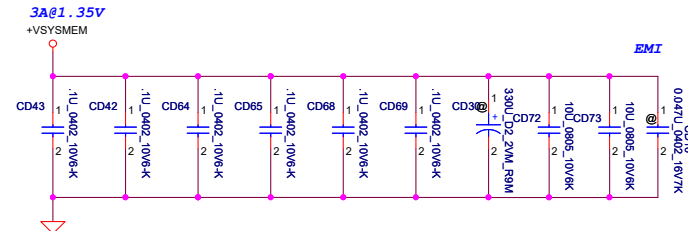
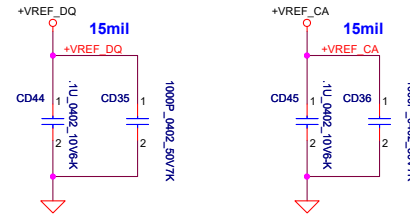
Layout Note:
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Title DDRIII SO-DIMM A			
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DDRA_DQS[0..7]	DDRA_DQS[0..7]	<14,4>
DDRA_DQS#[0..7]	DDRA_DQS#[0..7]	<14,4>
DDRA_MA[0..15]	DDRA_MA[0..15]	<14,4>
DDRA_DM[0..7]	DDRA_DM[0..7]	<14,4>



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DDRIII SO-DIMM B			
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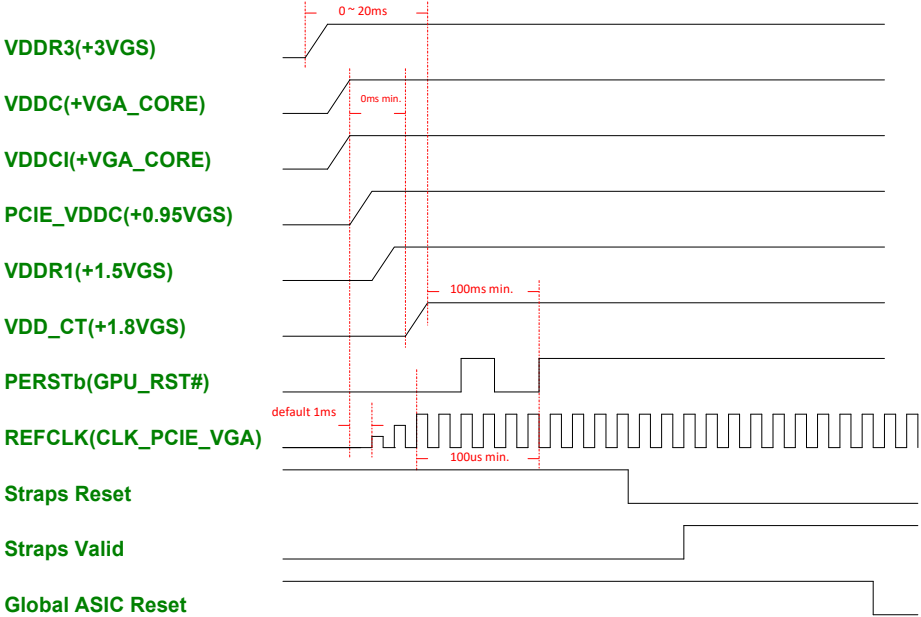
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VGA Note list need to be update!

Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

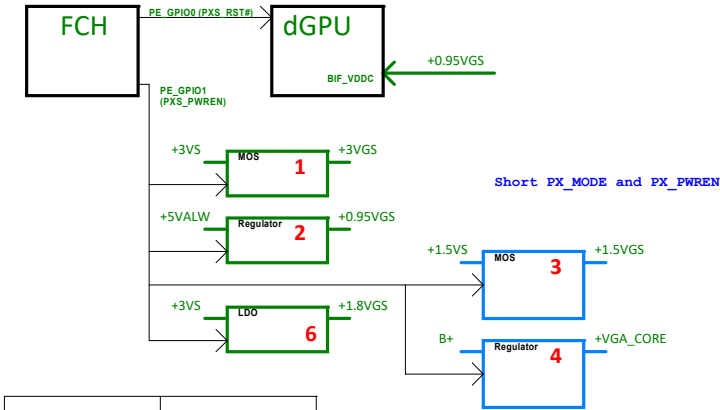


Without BACO option :

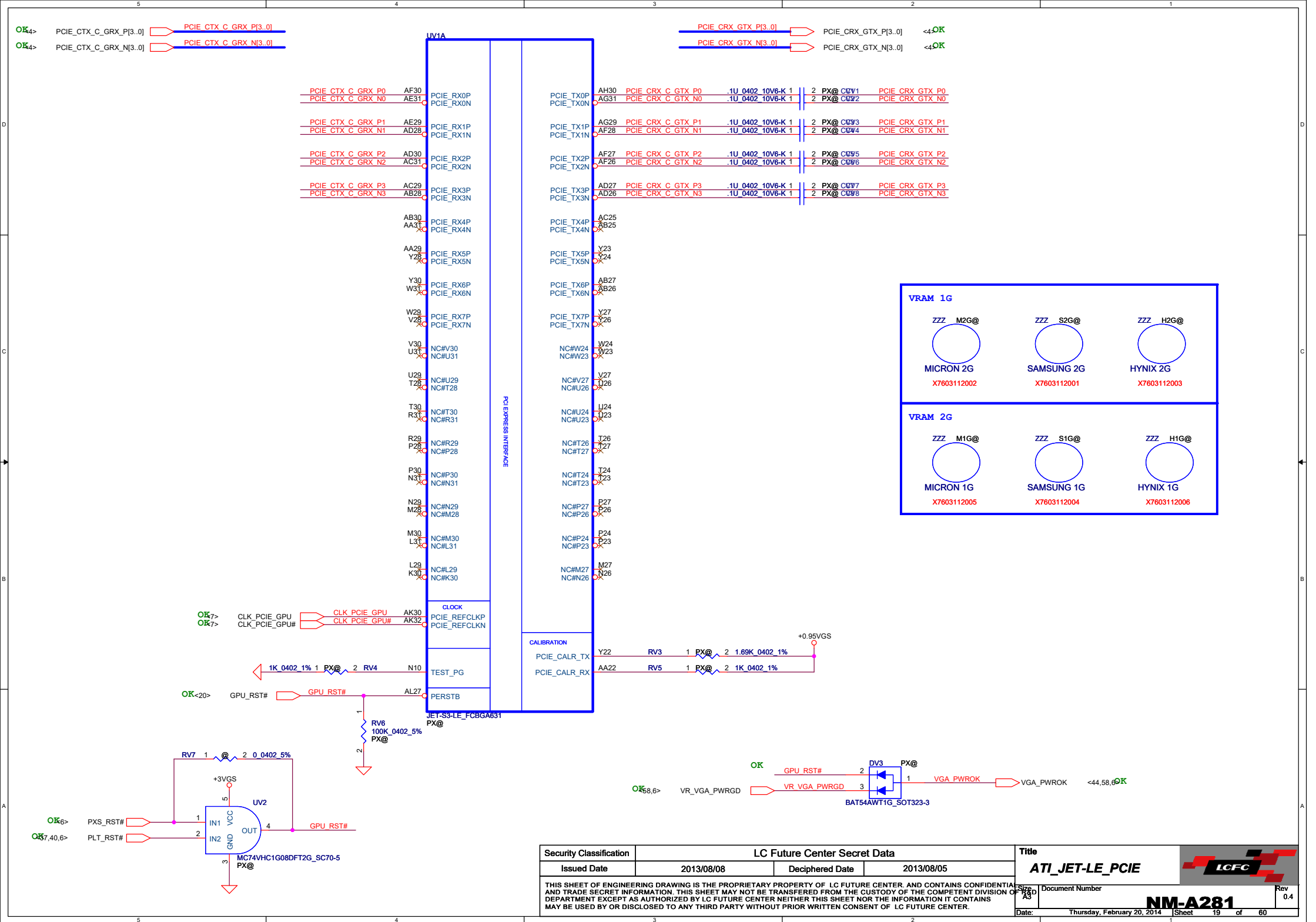
PE_GPIO0 : Low -> Reset dGPU ; High -> Normal operation
PE_GPIO1 : Low -> dGPU Power Off ; High -> dGPU Power ON

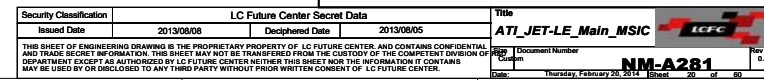
dGPU Power Pins	Voltage	Max current
VDD_CT, DP_VDDC, SPLL_PVDD, MPLL_PVDD, PCIE_PVDD, TSVDD, VDDR4, AVDD, VDD1DI	1.8V	1243mA
DP_VDDC, SPLL_VDDC, PCIE_VDDC, BIF_VDDC	0.95V	4560mA
VDDR3	3.3V	25mA
VDDR1	1.5V	1.5A
VDDC	0.8~1.125V	TBD
VDDCI	0.8~1.1V	8.8A

PX5.5



Name	Pin Assignment
PE_GPIO0	GPIO191
PE_GPIO1	GPIO192





MILPS	Bit				BOM		
	5	4	3	2	R _{pd} (G)	R _{pd} (G)	C (nF)
P8_0[5:1]	1	1	0	0	RV71=0k, 45k	RV77=2K	CV15=5nC
P8_1[5:1]	1	1	0	0	RV74=4N	RV77=4.75K	CV16=5nC
P8_2[5:1]	1	1	0	0	RV60=4N	RV69=4.75K	CV16=5nC
P8_3[5:1]	1	1	X	X	RV60=4N	RV69=4K75	CV16=X7.6

Capacitor Value (nF)	Bits [5:4]	R _{pd} (K)		Bits [3:2]	
		4K	7K	4K	7K
		NC	4750	000	
		8450	2000	001	
		4330	2000	010	
		6980	4990	011	
		4330	4990	100	
680	00	3240	5620	101	
82	01	3400	10000	110	
10	10	4750	NC	111	
NC	11				

Note: 4052 nF resistors are required



UV1F

NC_VARY_BL
NC_DIGON

AB11
AB12

NC_UPHYAB_TMDPA_TX0N
NC_UPHYAB_TMDPA_TX0P

AL15
AK14

NC_UPHYAB_TMDPA_TX1N
NC_UPHYAB_TMDPA_TX1P

AH16
AJ15

NC_UPHYAB_TMDPA_TX2N
NC_UPHYAB_TMDPA_TX2P

AL17
AK16

NC_UPHYAB_TMDPA_TX3N
NC_UPHYAB_TMDPA_TX3P

AH18
AJ17

NC_TXOUT_L3P
NC_TXOUT_L3N

AL19
AK18

TMDP

NC_UPHYAB_TMDPB_TX0N
NC_UPHYAB_TMDPB_TX0P

AH20
AJ19

NC_UPHYAB_TMDPB_TX1N
NC_UPHYAB_TMDPB_TX1P

AL21
AK20

NC_UPHYAB_TMDPB_TX2N
NC_UPHYAB_TMDPB_TX2P

AH22
AJ21


NC_UPHYAB_TMDPB_TX3N
NC_UPHYAB_TMDPB_TX3P

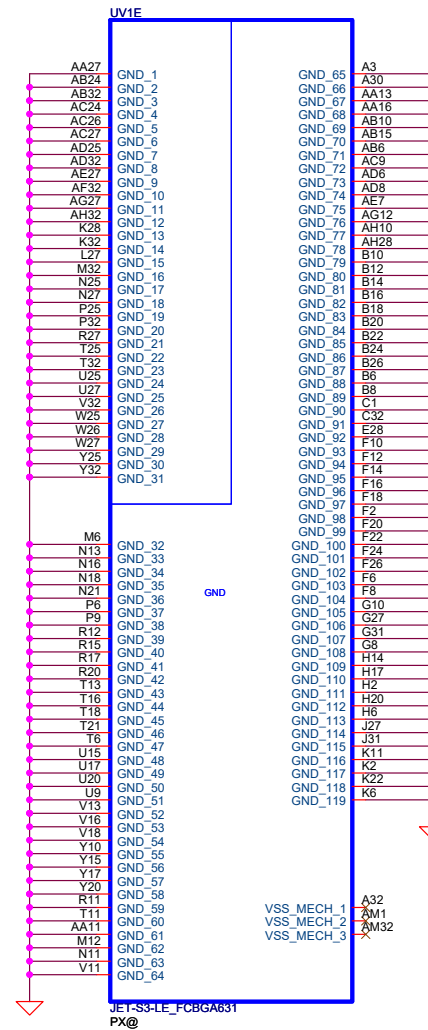
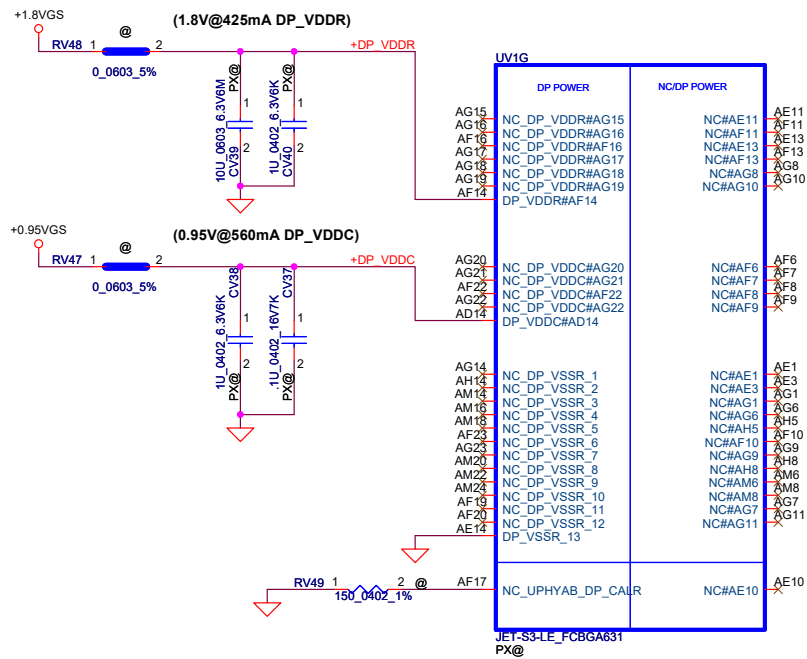
AL23
AK22


NC_TXOUT_U3P
NC_TXOUT_U3N

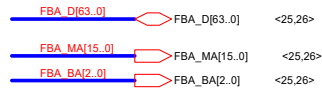
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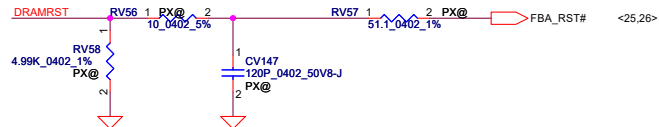
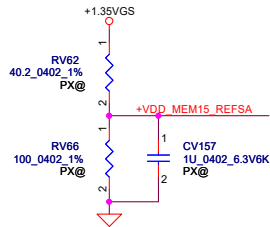
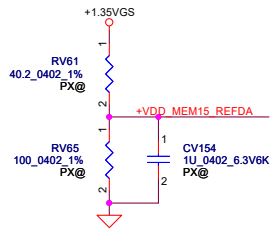
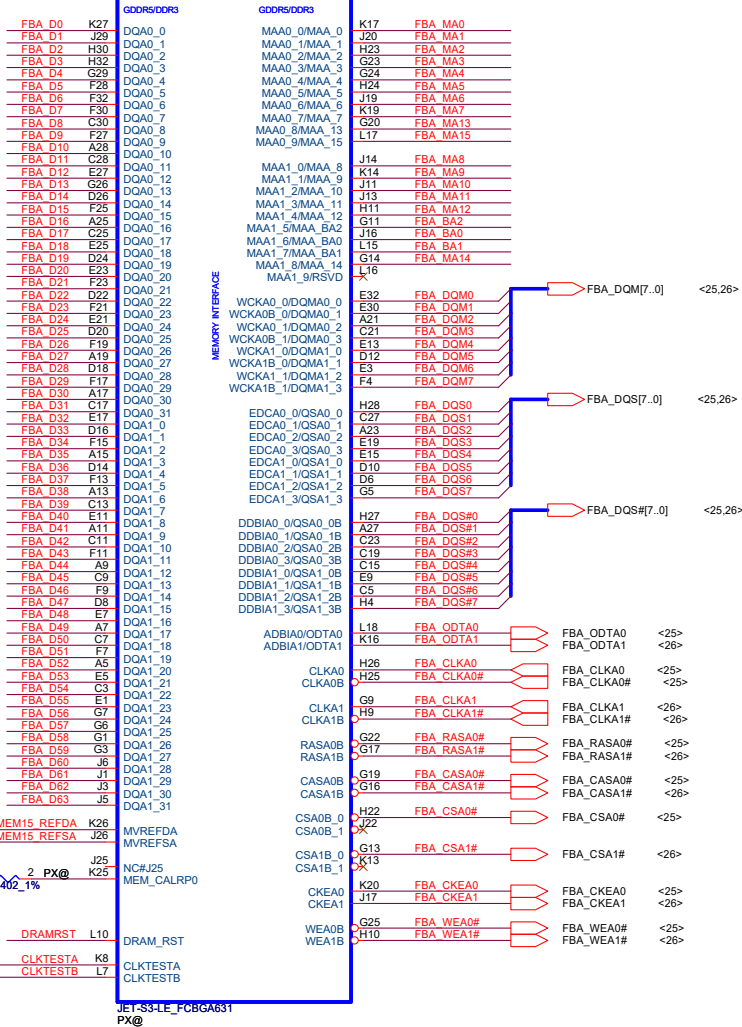
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Issued Date		2013/08/08		Deciphered Date		2013/08/05					ATI_JET-LE_DP Power	
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Size		Custom		Document Number		Date: Thursday, February 20, 2014		Sheet 22 of 60				



UVIC

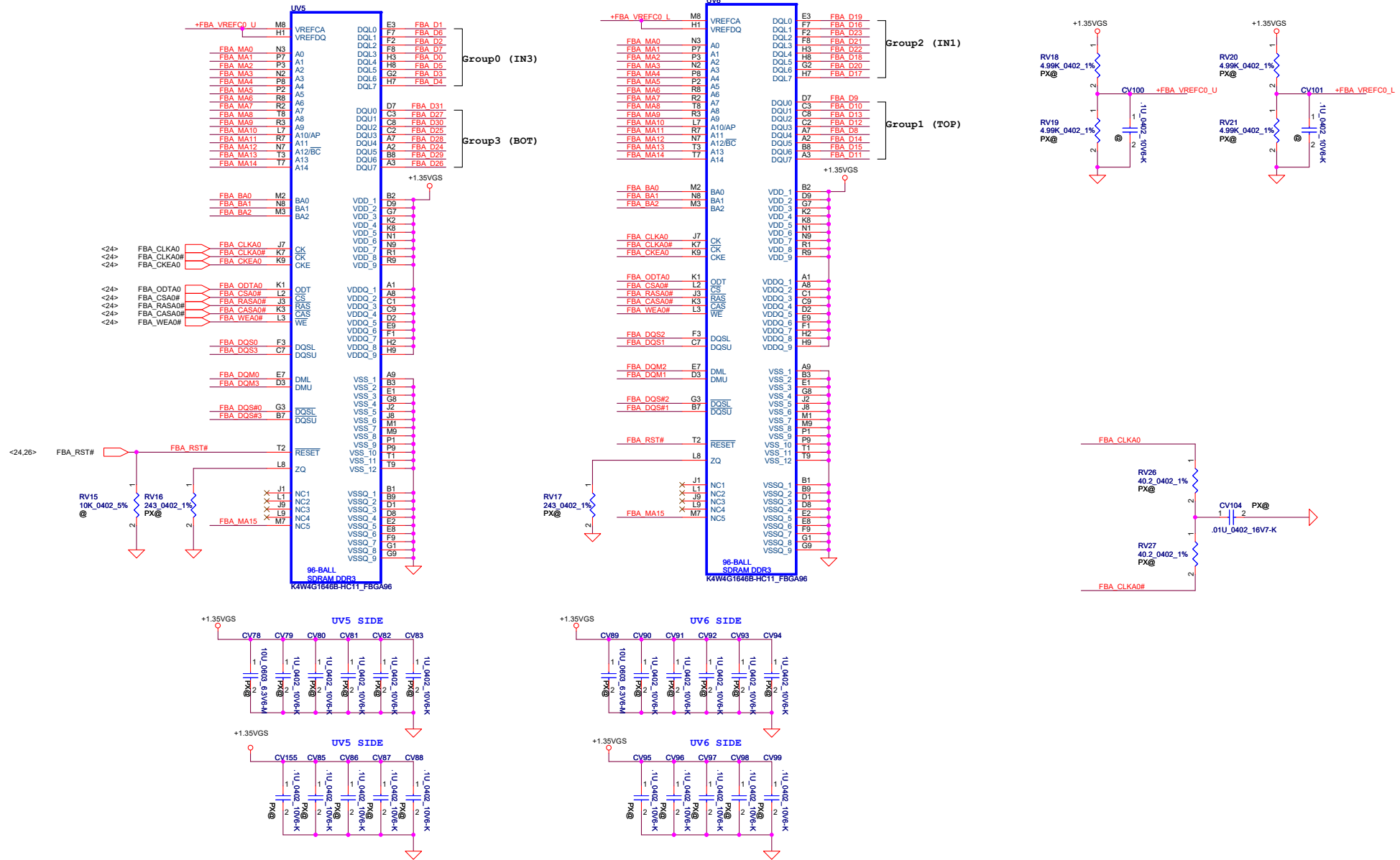


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Issued Date	2013/08/08	Deciphered Date	2013/08/05	ATI_JET-LE_MEM IF
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				Document Number
				Rev 0.4
				NM-A281
				Date: Thursday, February 20, 2014
				Sheet 24 of 60

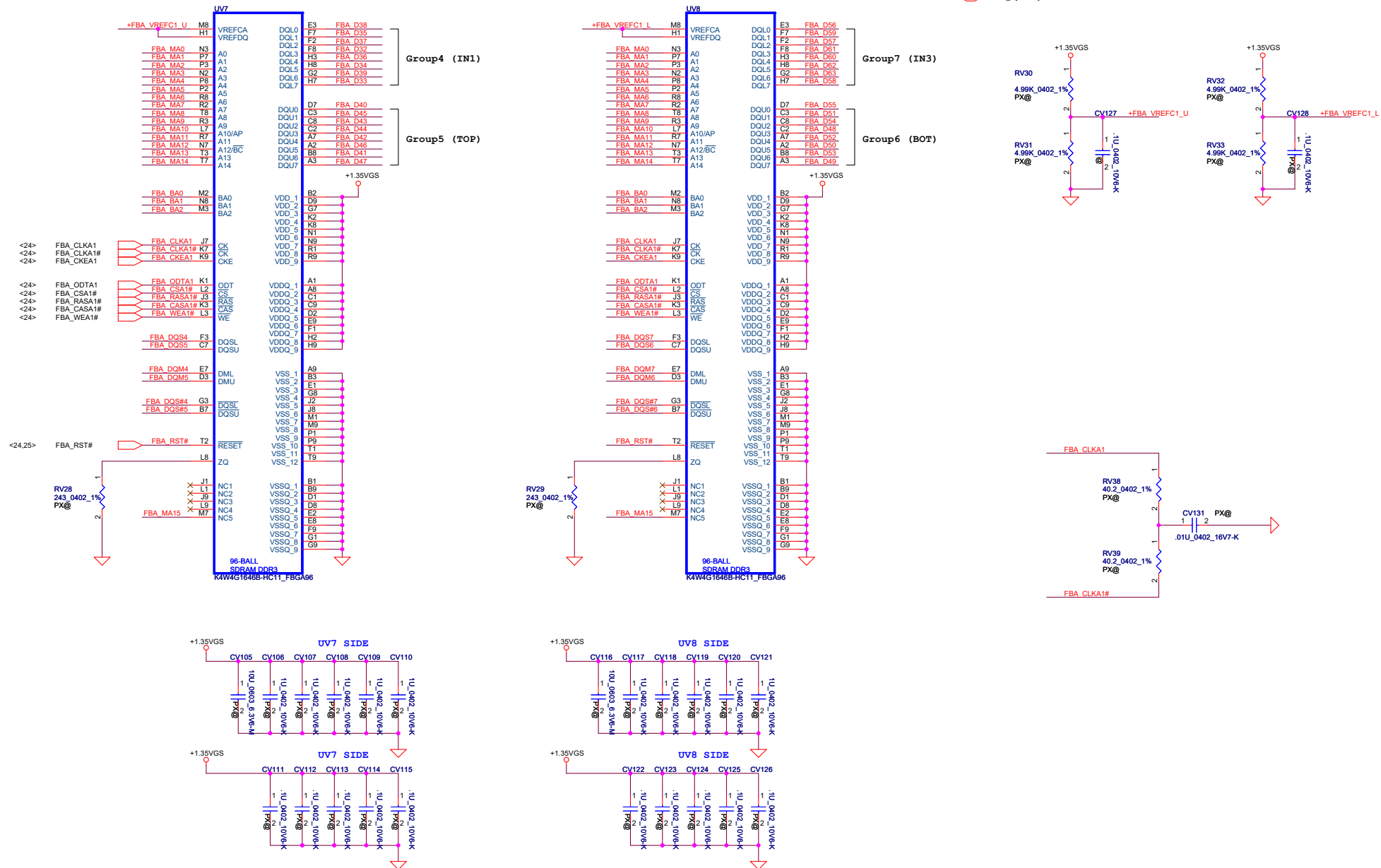
Memory Partition A - Lower 32 bits


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FBA_D[31..0] <24>


ACLU5 swap the VRAM Data @ 08/26
VRAM 8 pcs change to 4 pcs @ 09/26




Memory Partition A - Upper 32 bits





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				Document Number NM-A281	
				Date: Thursday, February 20, 2014 Sheet 26 of 60 Rev 0.4	


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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Blank	
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Date: Thursday, February 20, 2014				Sheet 28 of 60		

	5		4		3		2		1
D									D
C									C
B									B
A									A
					Security Classification		LC Future Center Secret Data		
					Issued Date		2013/08/08	Deciphered Date	2013/08/05
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					Size		Document Number		Rev
					Custom		NM-A281		0.4
					Date:		Thursday, February 20, 2014		Sheet 29 of 60

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				Date: Thursday, February 20, 2014		Rev 0.4
				Sheet 31 of 60		NM-A281

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Issued Date	2013/08/08	Deciphered Date	2013/08/05	Blank		
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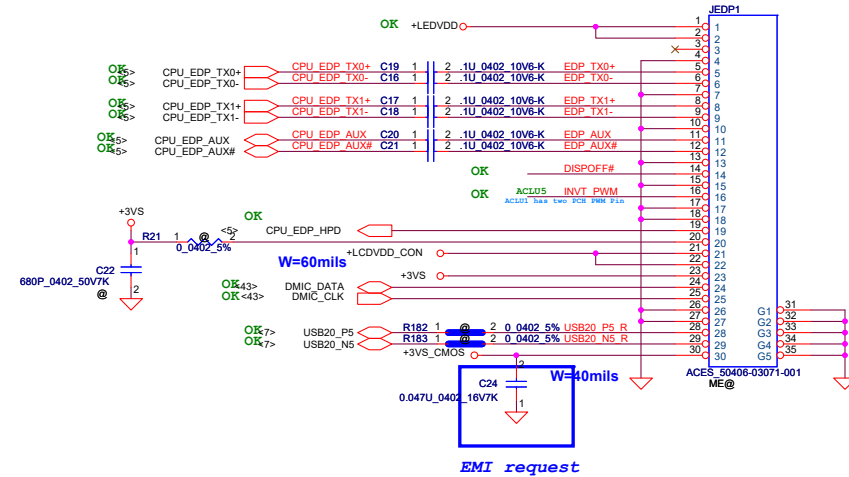
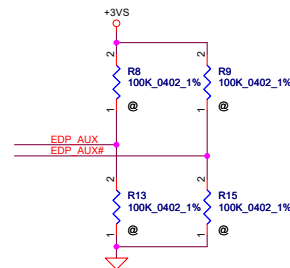
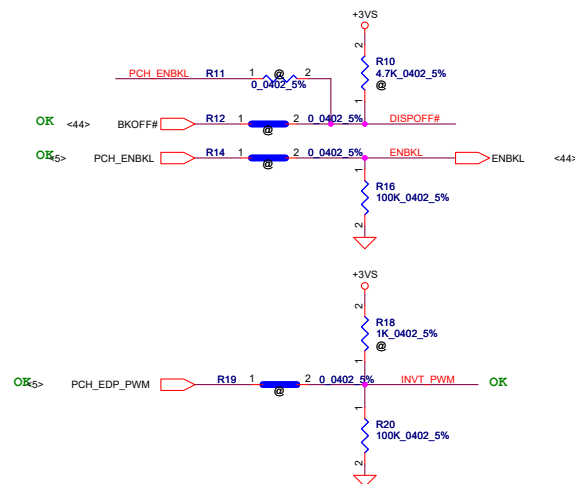
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OK



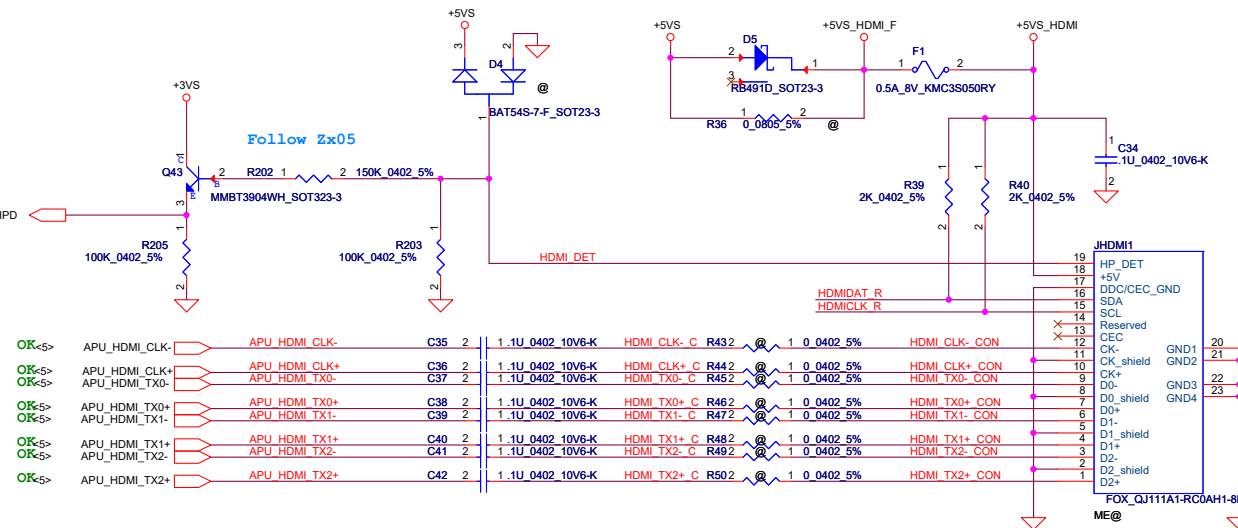
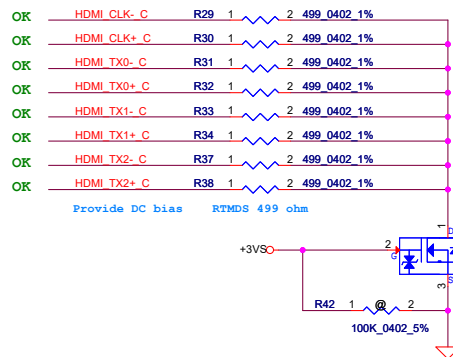
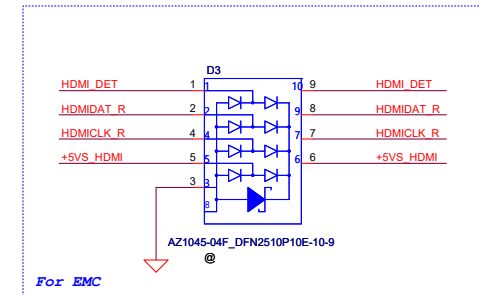
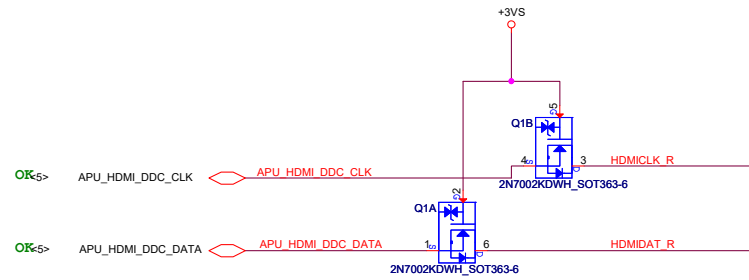
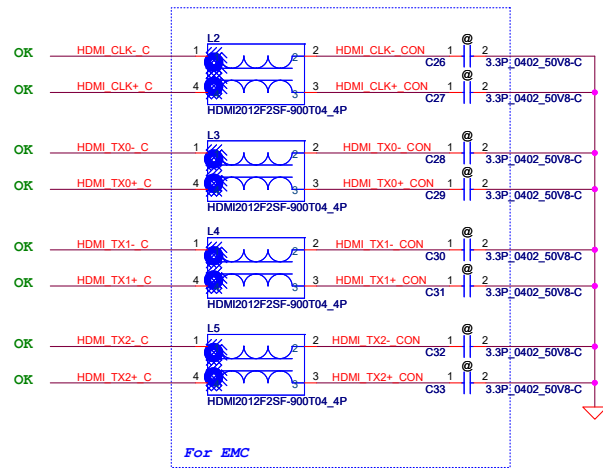
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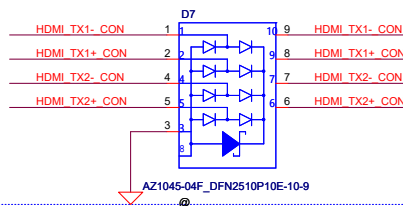
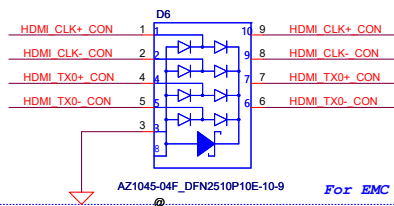
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Rev	0.4
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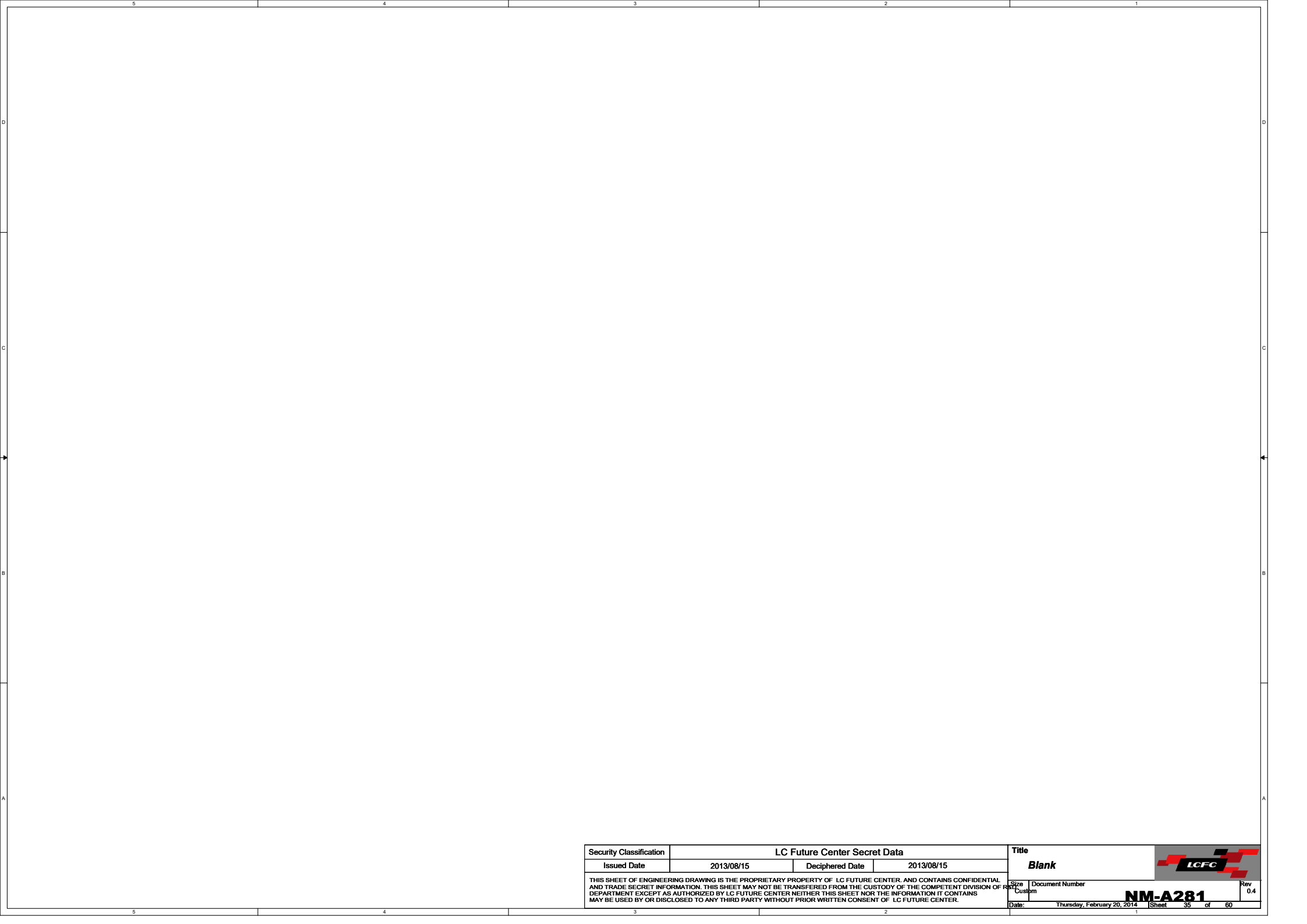
Close to JHDMI1




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Issued Date	2013/08/15	Deciphered Date	2013/08/15			Size	Document Number		
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						Date:	Thursday, February 20, 2014	Sheet	34 of 60

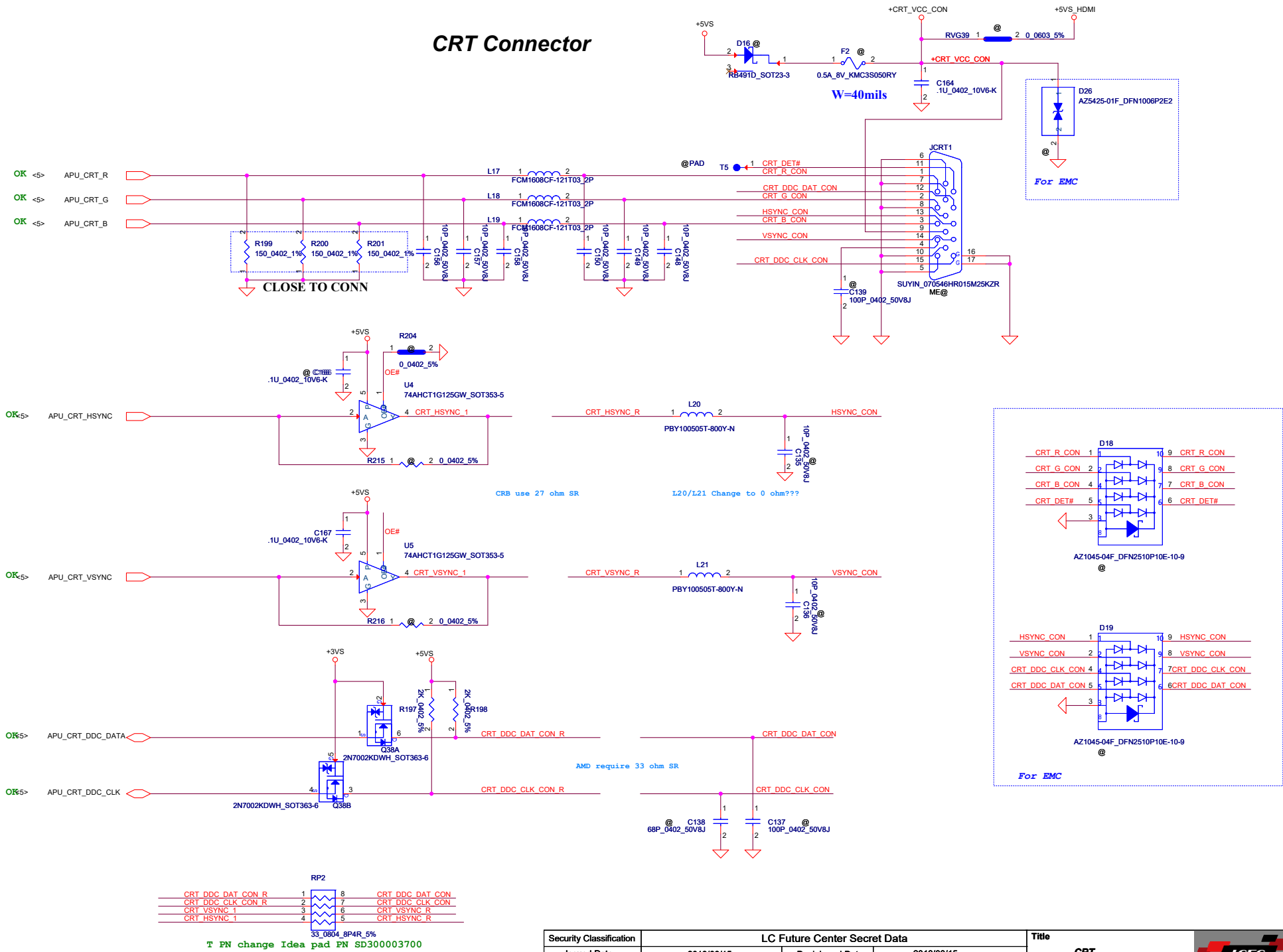
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				Custom		NM-A281		0.4	
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CRT Connector

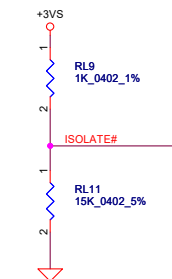
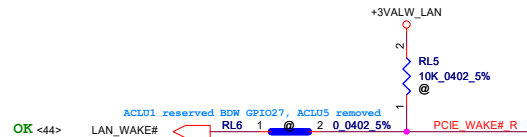
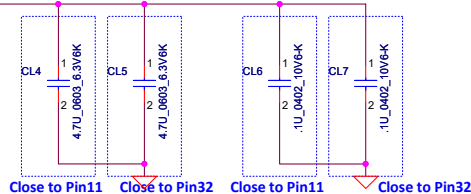


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				Custom			
				Date:	Thursday, February 20, 2014	Sheet	36 of 60

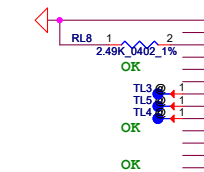
+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms~spec~100ms

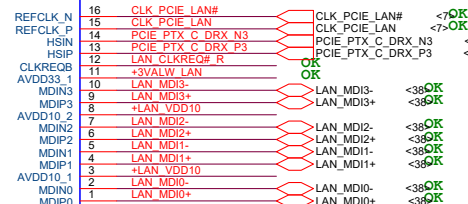
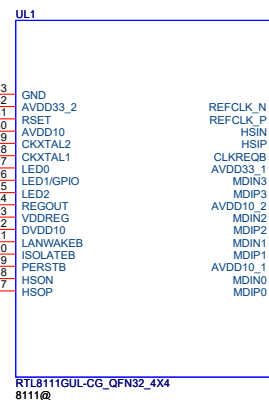
width : 40 mils



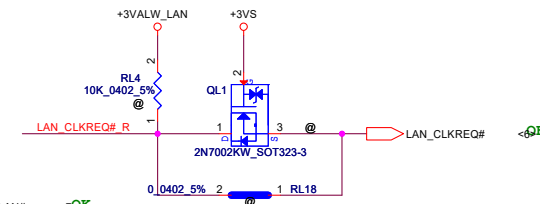
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OK <4>
OK <4>



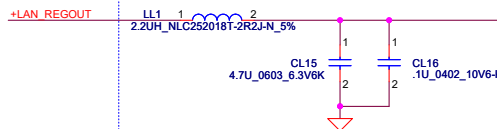
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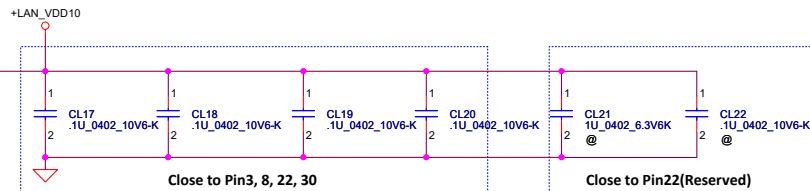
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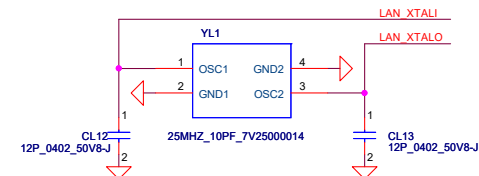
For RTL8111GUL/ RTL8106EUL (SWR mode)



Layout Note: LL1 must be within 200mil to Pin36,
CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

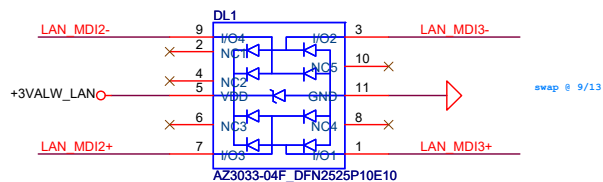


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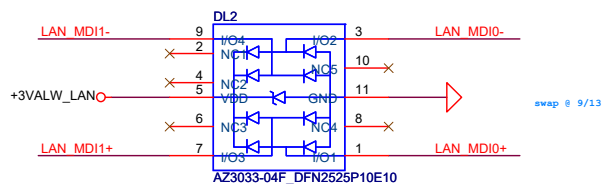


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		NM-A281		Sheet		37 of 60	

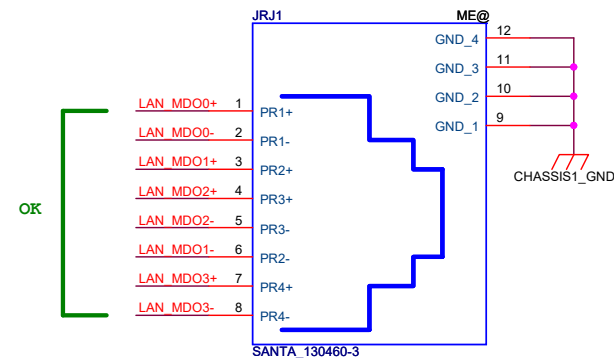
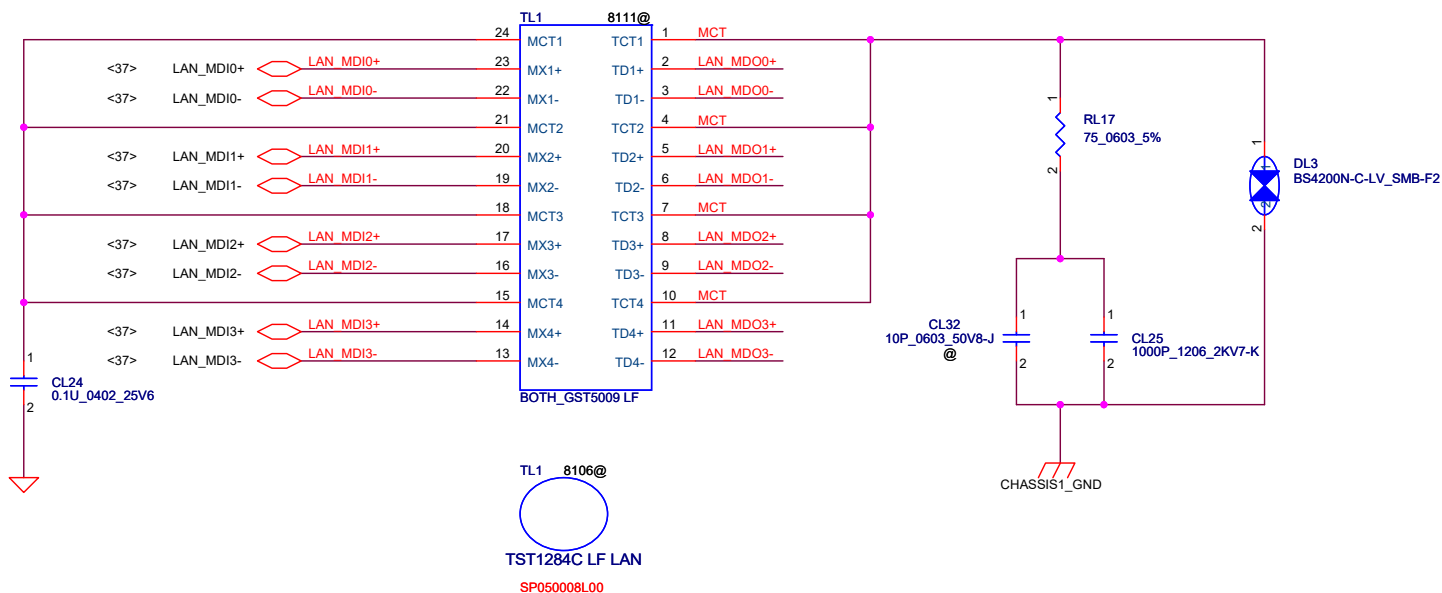
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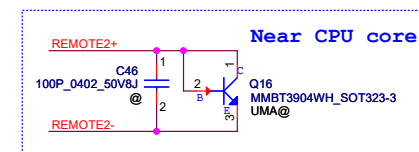
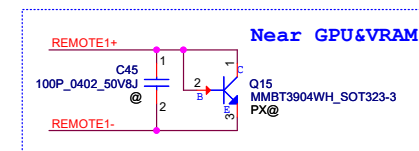
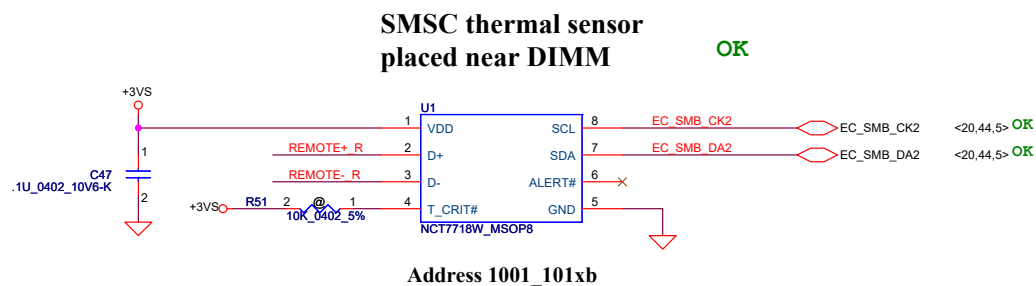
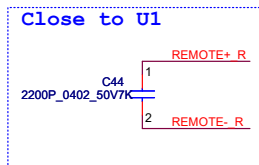
Place Close to TL1



Place Close to TL2



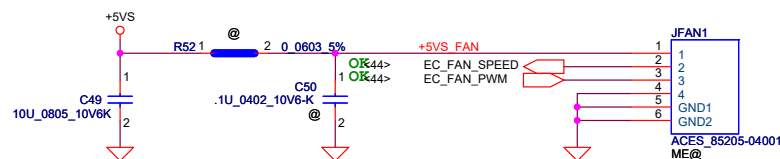
Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	LAN_Transformer	
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REMOTE1+ R175 1 PX@ 2 0 0402 5%
 REMOTE2+ R176 1 UMA@ 2 0 0402 5% REMOTE+ R
 REMOTE2- R177 1 UMA@ 2 0 0402 5% REMOTE- R
 REMOTE1- R178 1 PX@ 2 0 0402 5%

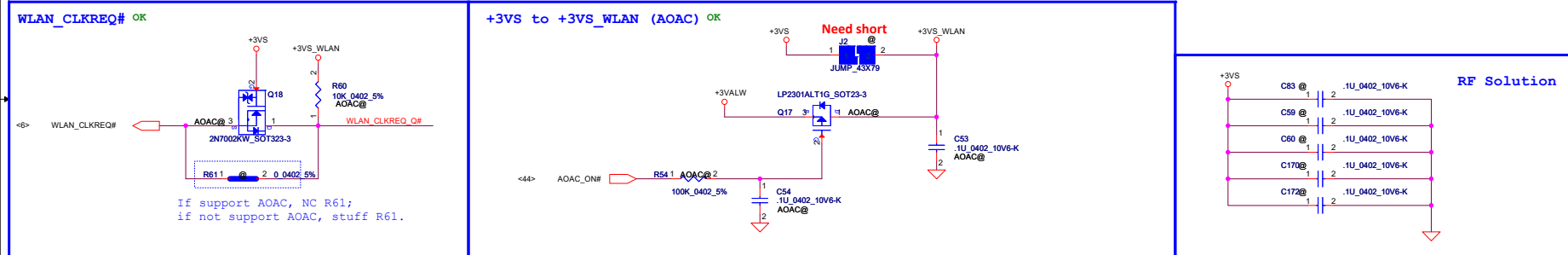
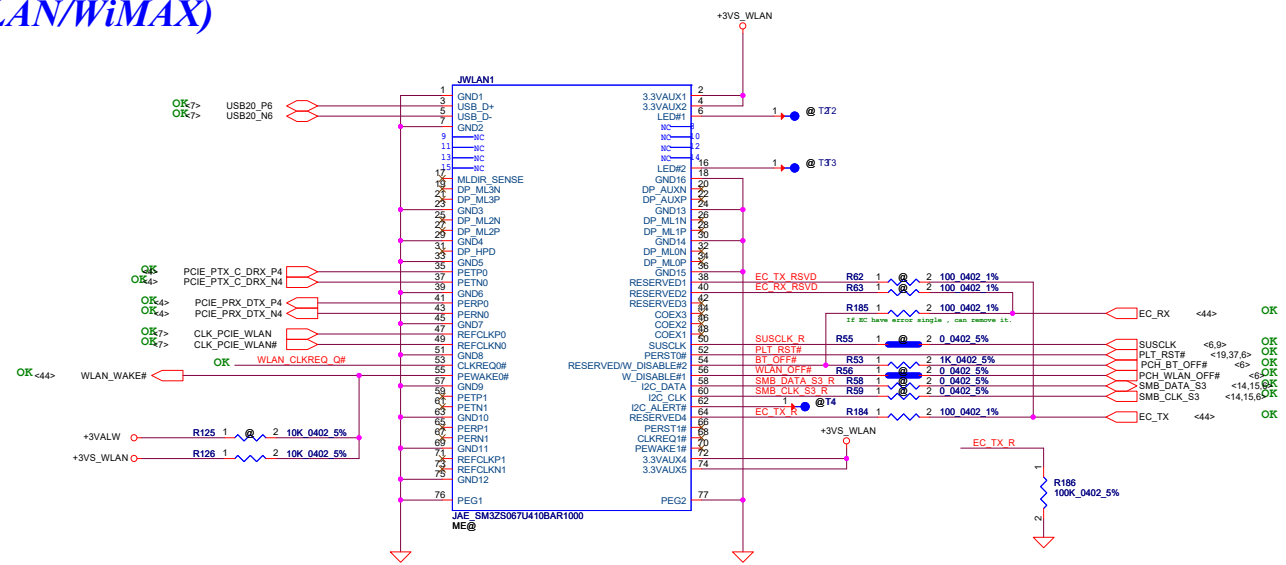
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
 Trace width/space:10/10 mil
 Trace length:<8"


FAN Conn



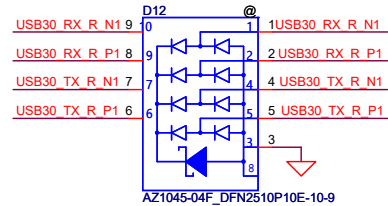
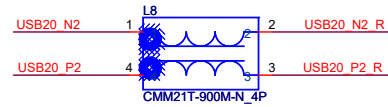
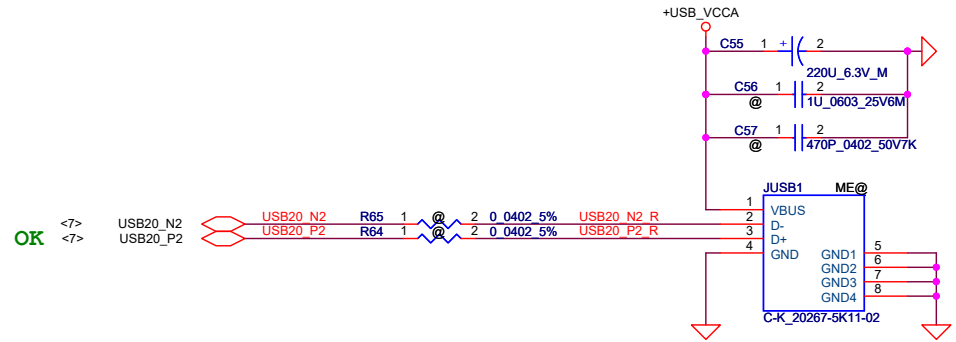
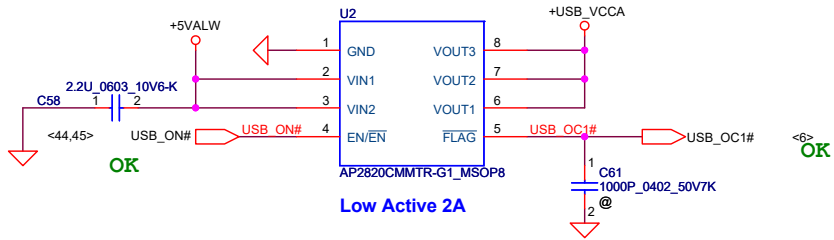
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					Rev 0.4 NM-A281

Mini-Express Card(WLAN/WiMAX)

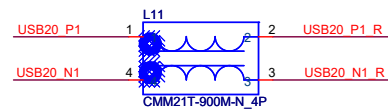
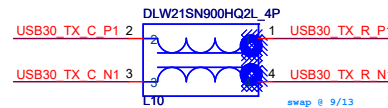
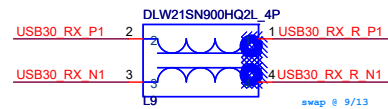
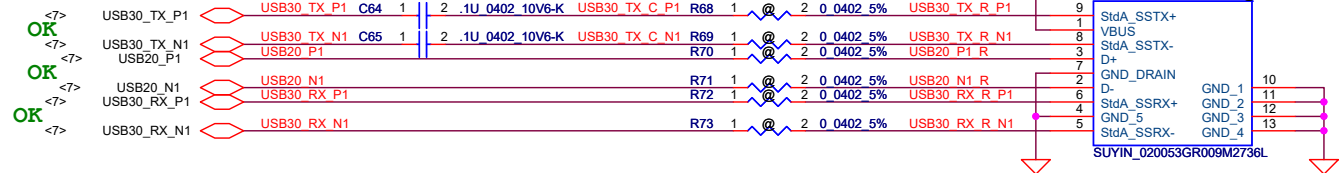
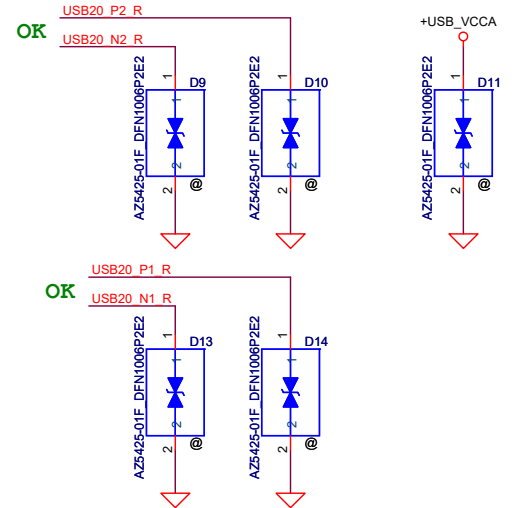


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				Custm	NM-A281	Rev
				Date:	Thursday, February 20, 2014	Sheet 40 of 60


LEFT SIDE USB3.0 PORT X2

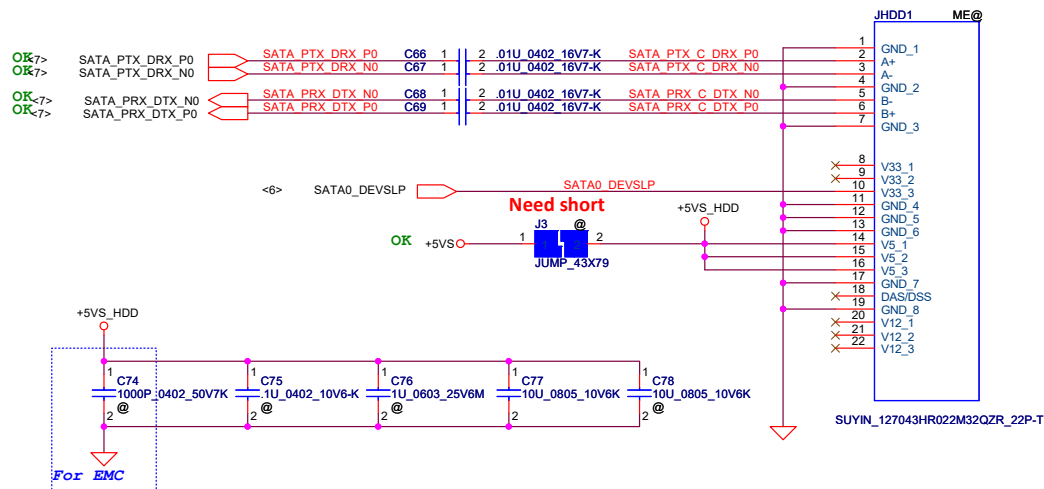


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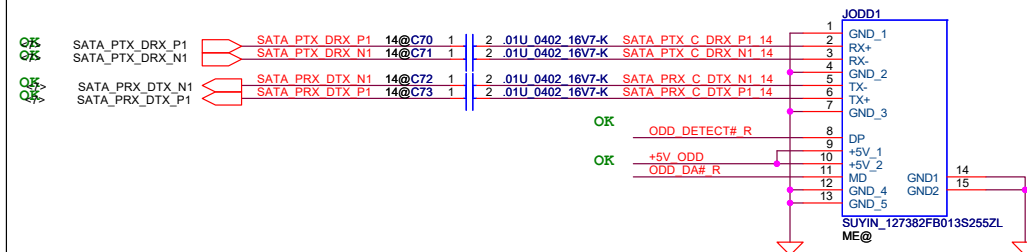


For EMC

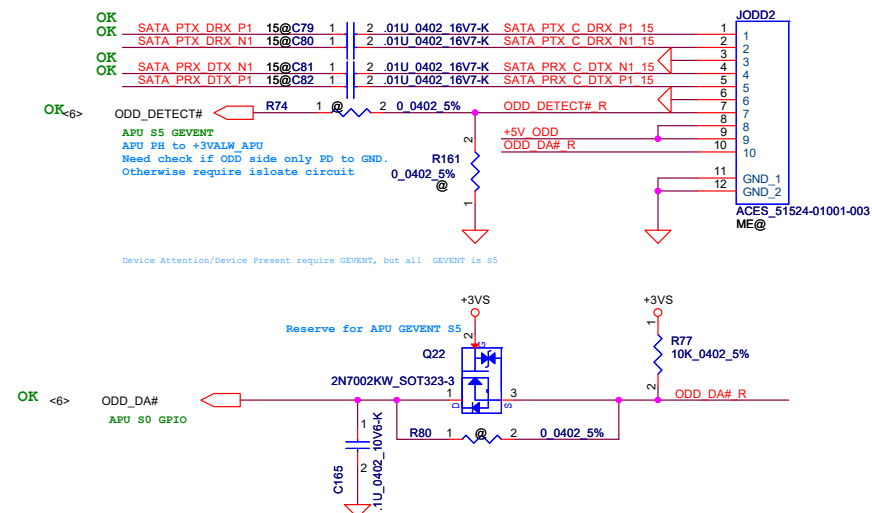
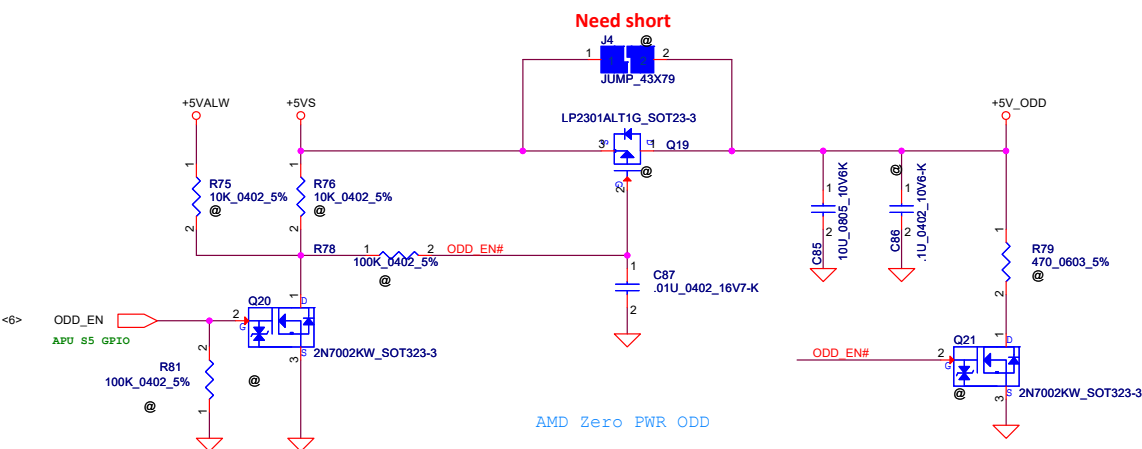
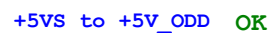
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						Date:	Thursday, February 20, 2014	


SATA HDD Conn.

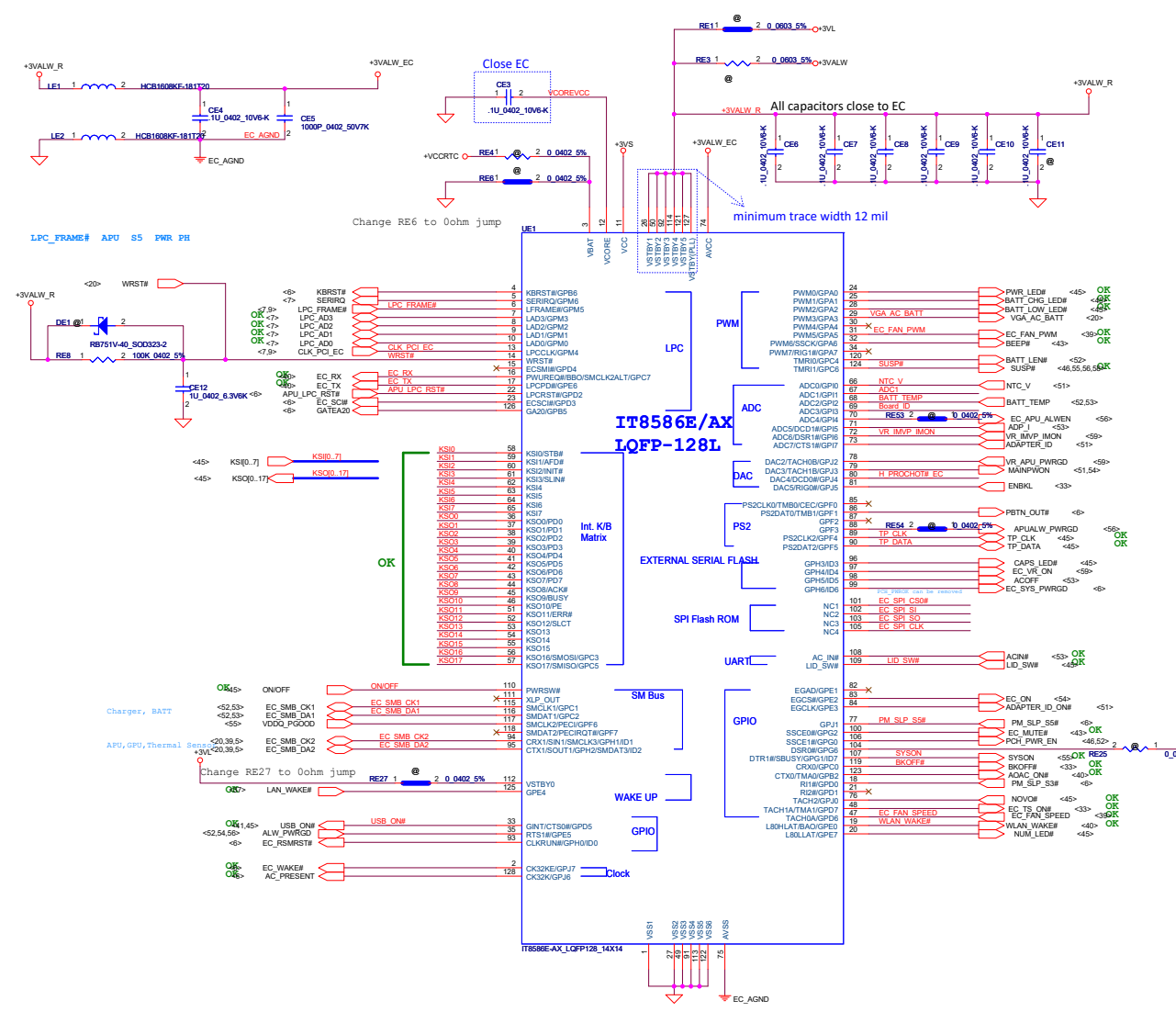
FOR 14"
SATA ODD Conn.



FOR 15"
SATA ODD FFC Conn

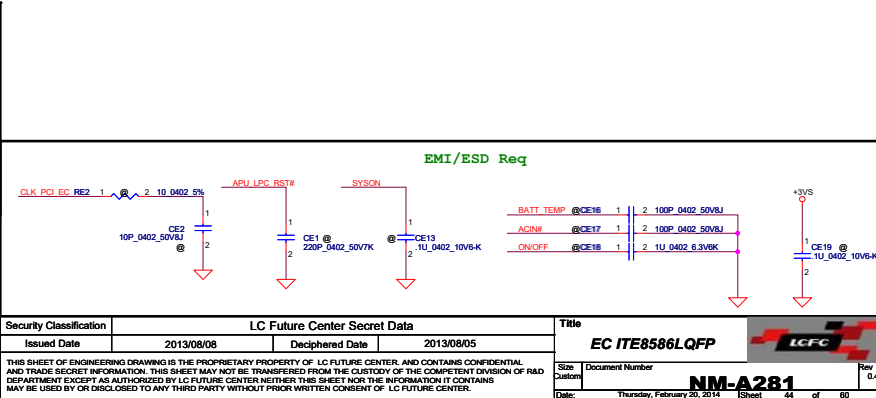
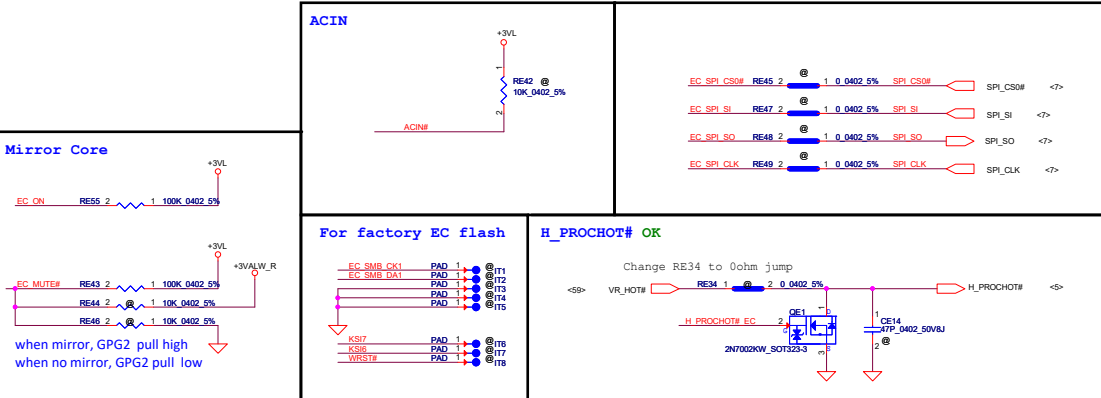


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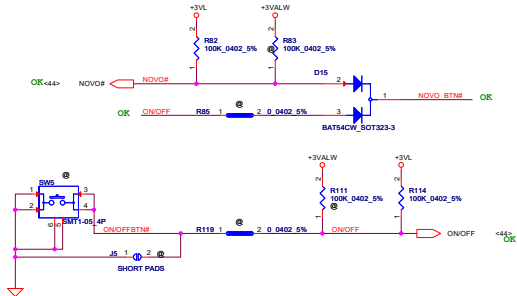


BORAD ID Config

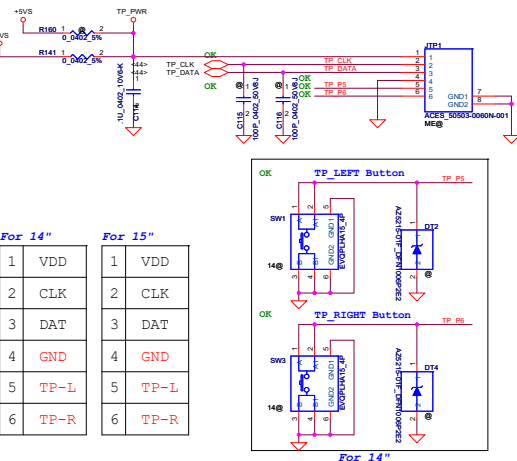
Vcc	RE33	RE34	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Phase
3.3V +/- 5%	100K +/- 1%					
Board ID	RE33	RE34	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	Phase
0	OK +/- 5%	0 V	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V		
2	18K +/- 5%	0.436 V	0.503 V	0.538 V		
3	33K +/- 5%	0.712 V	0.819 V	0.875 V		
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V		
5	24K +/- 5%	0.612 V	0.638 V	0.664 V		



ON/OFF switch



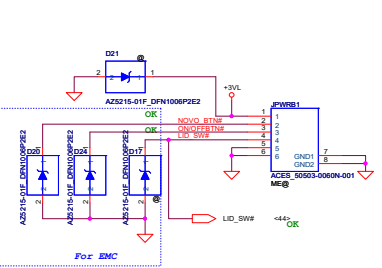
TP/B Connector



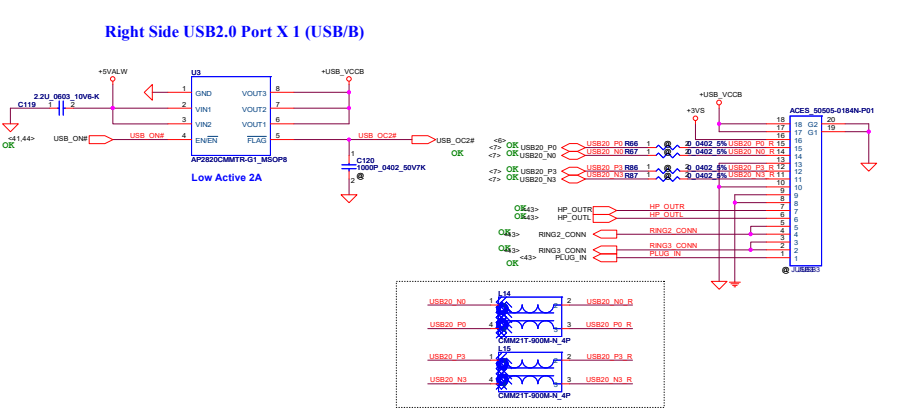
K/B Connector



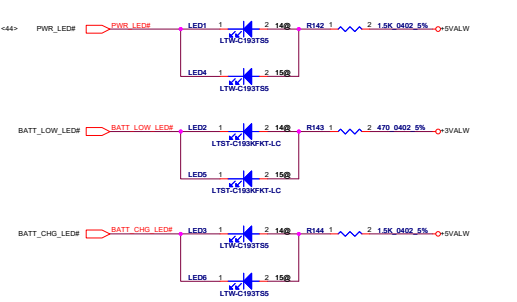
PWR/B Connector



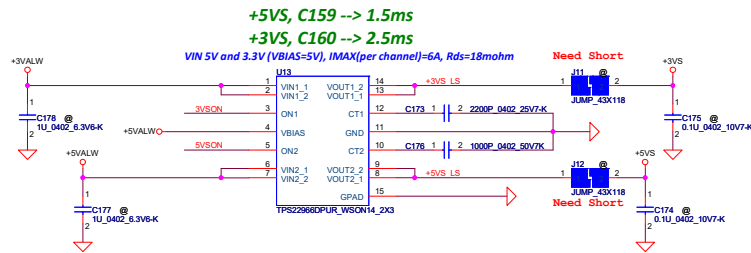
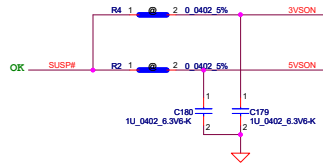
USB I/O Connector



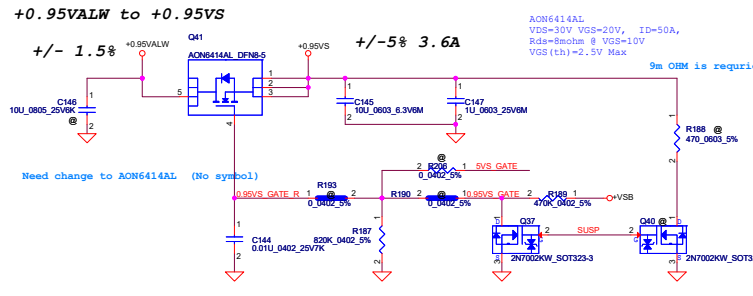
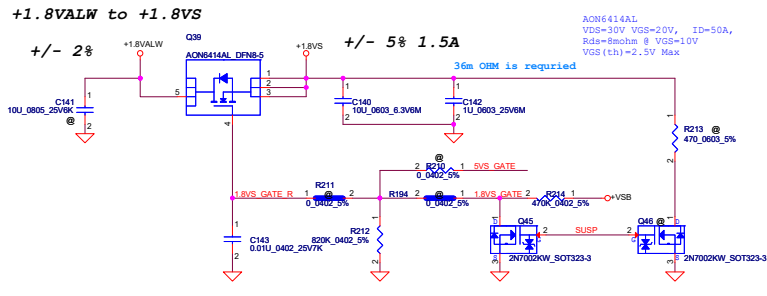
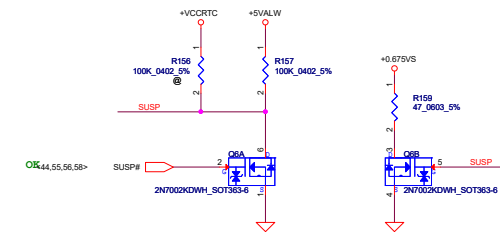
LED



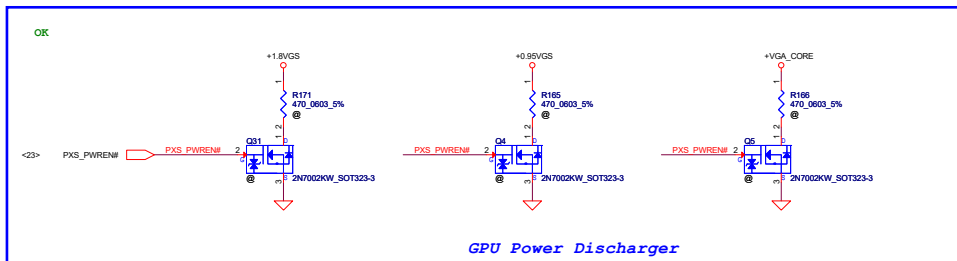
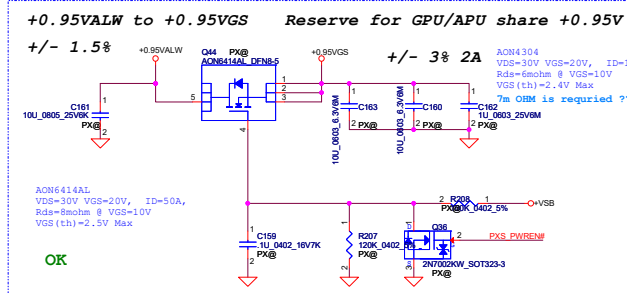
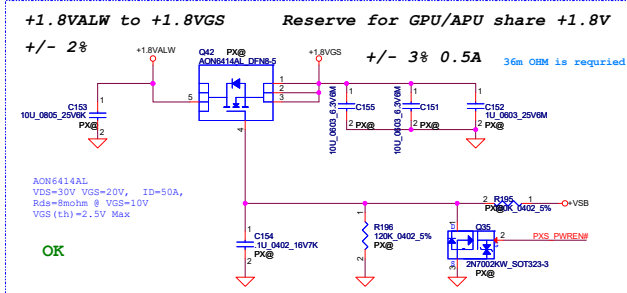
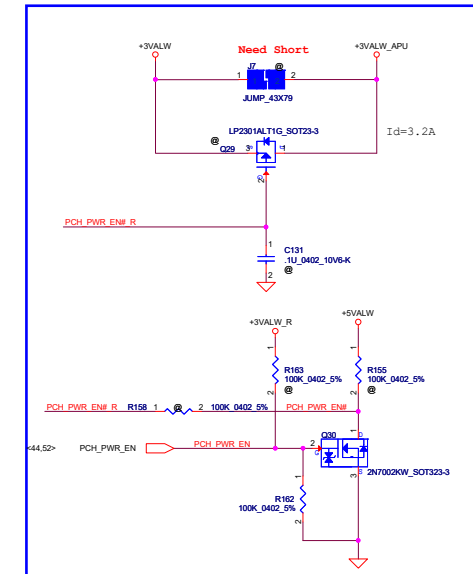
Load Switch
+5VALW To +5VS OK
+3VALW To +3VS



For DisCharge



Need check all the EN pin and PWR Sequence.



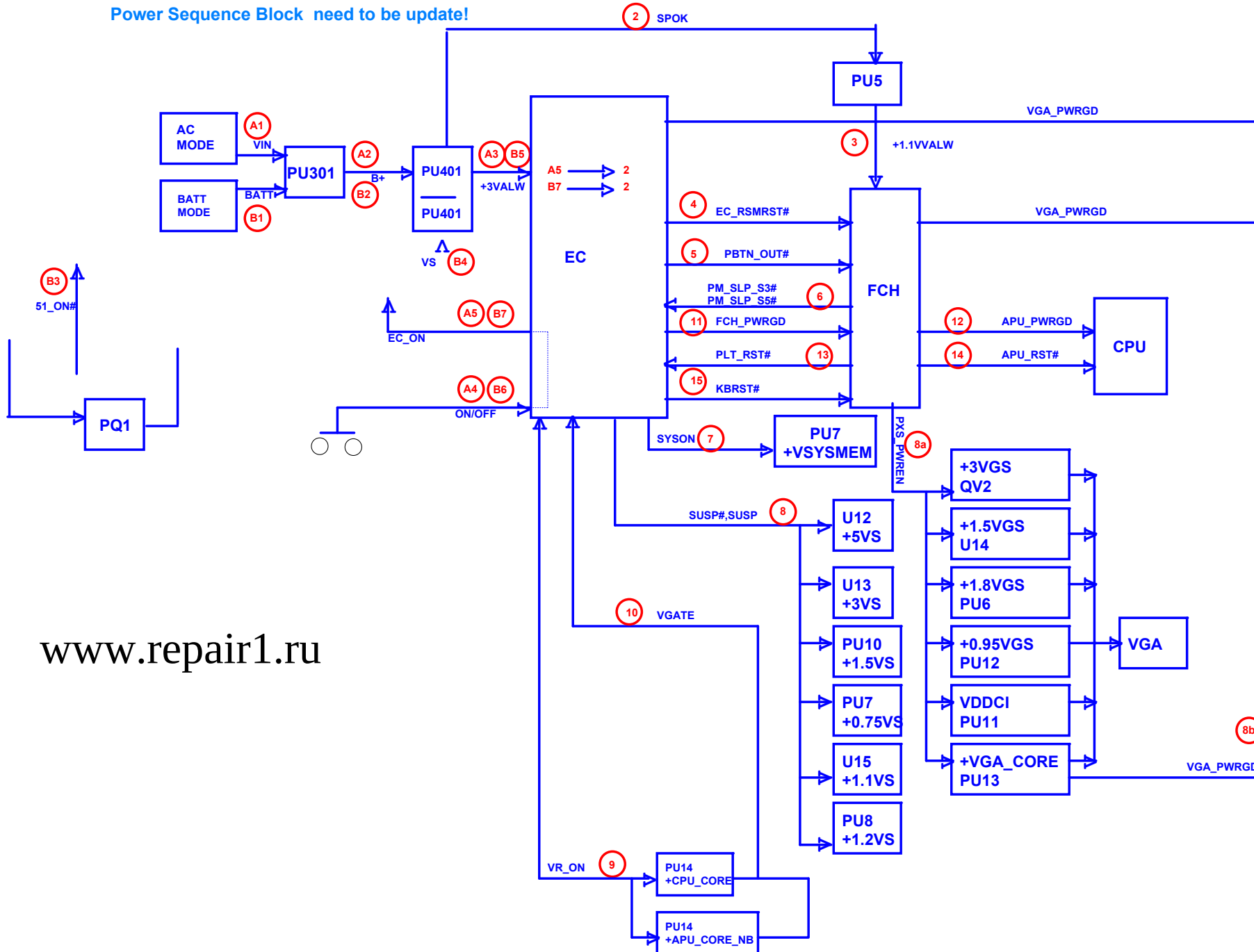
GPU Power Discharge

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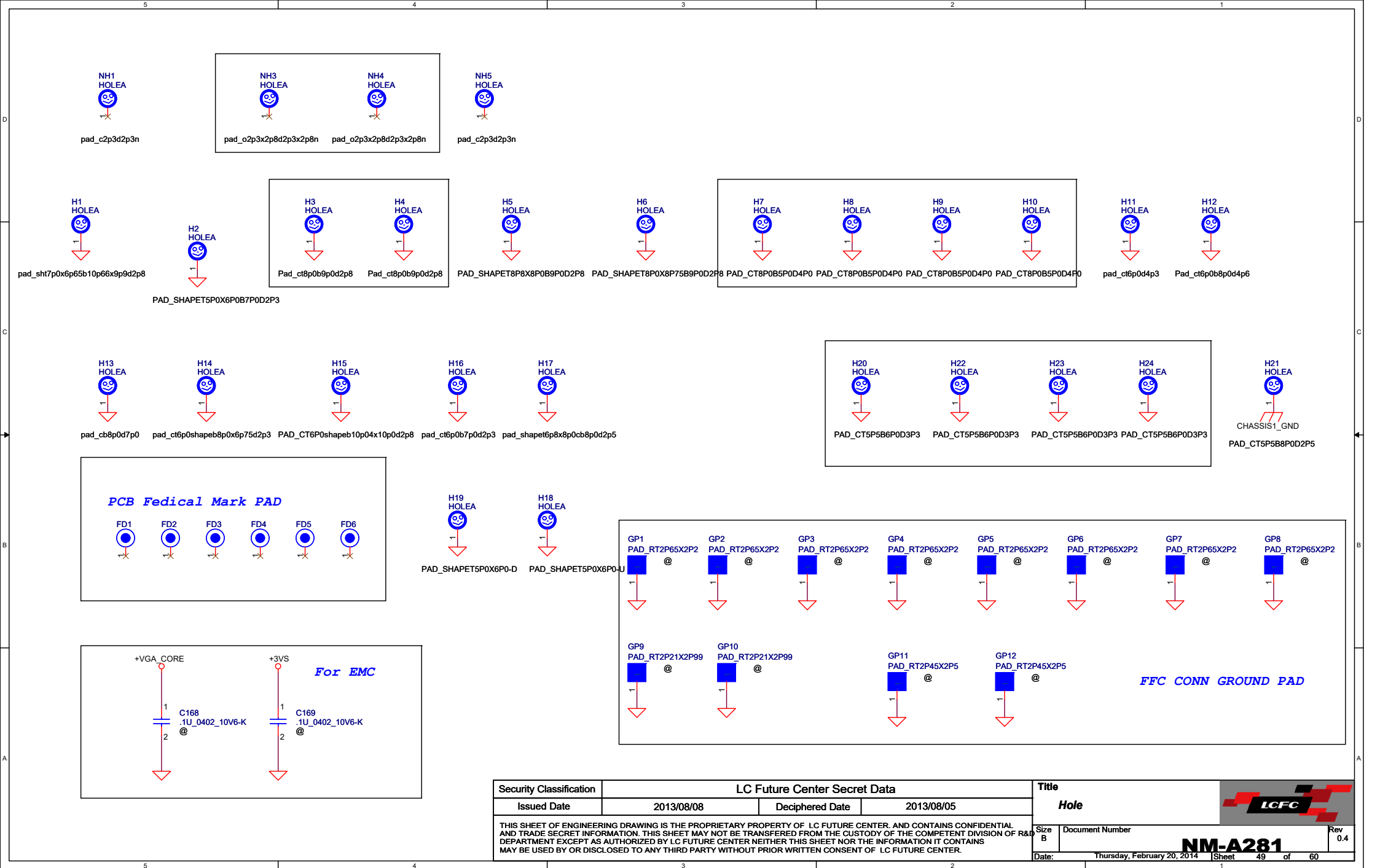
Rev 0.4

Power Sequence Block need to be update!

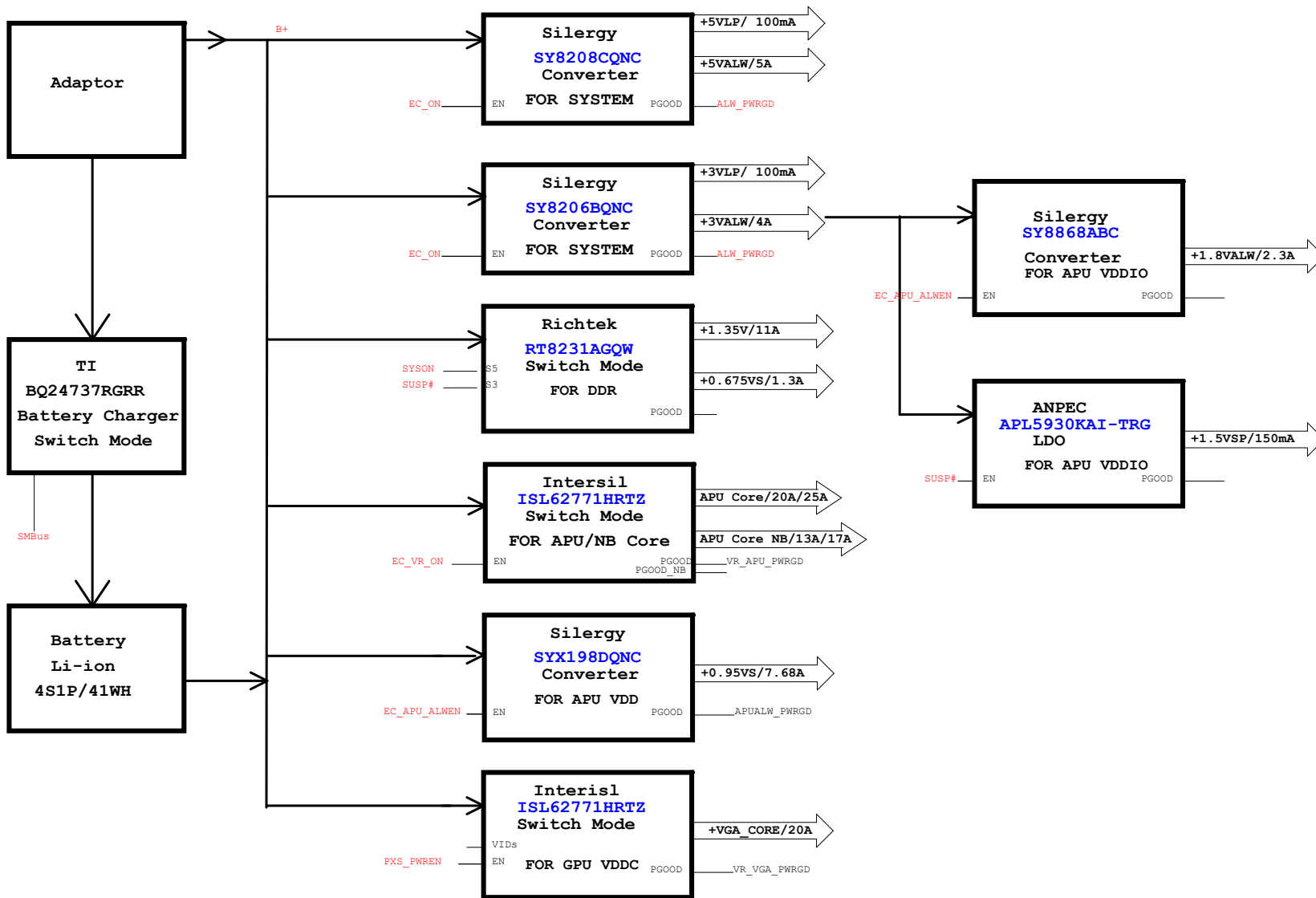


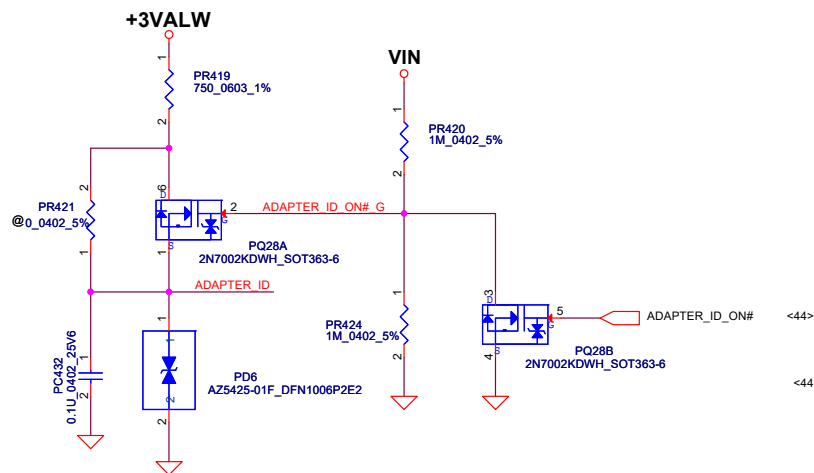
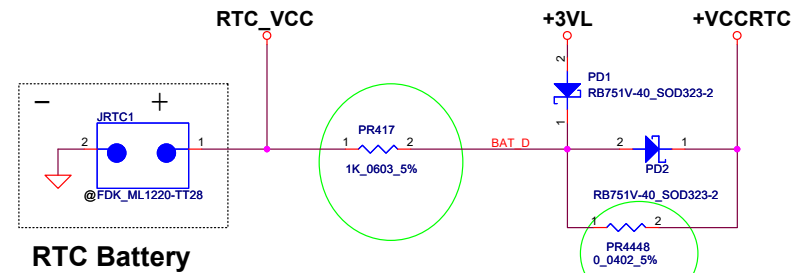
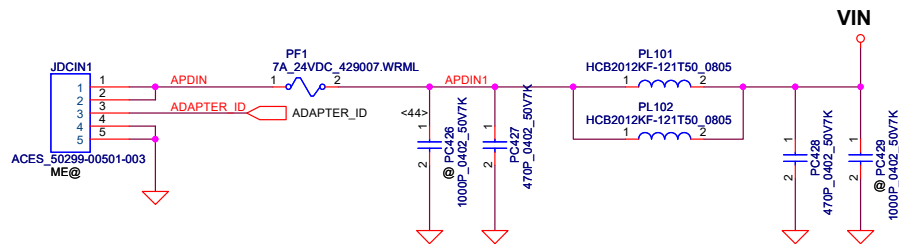
www.repair1.ru

Security Classification	LC Future Center Secret Data			<div> <div>Title</div> <div>Virtual symbol</div> <div>  </div> </div>	
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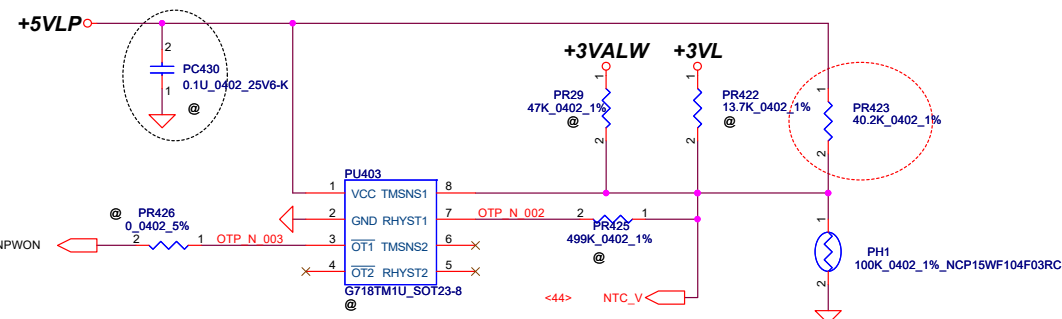


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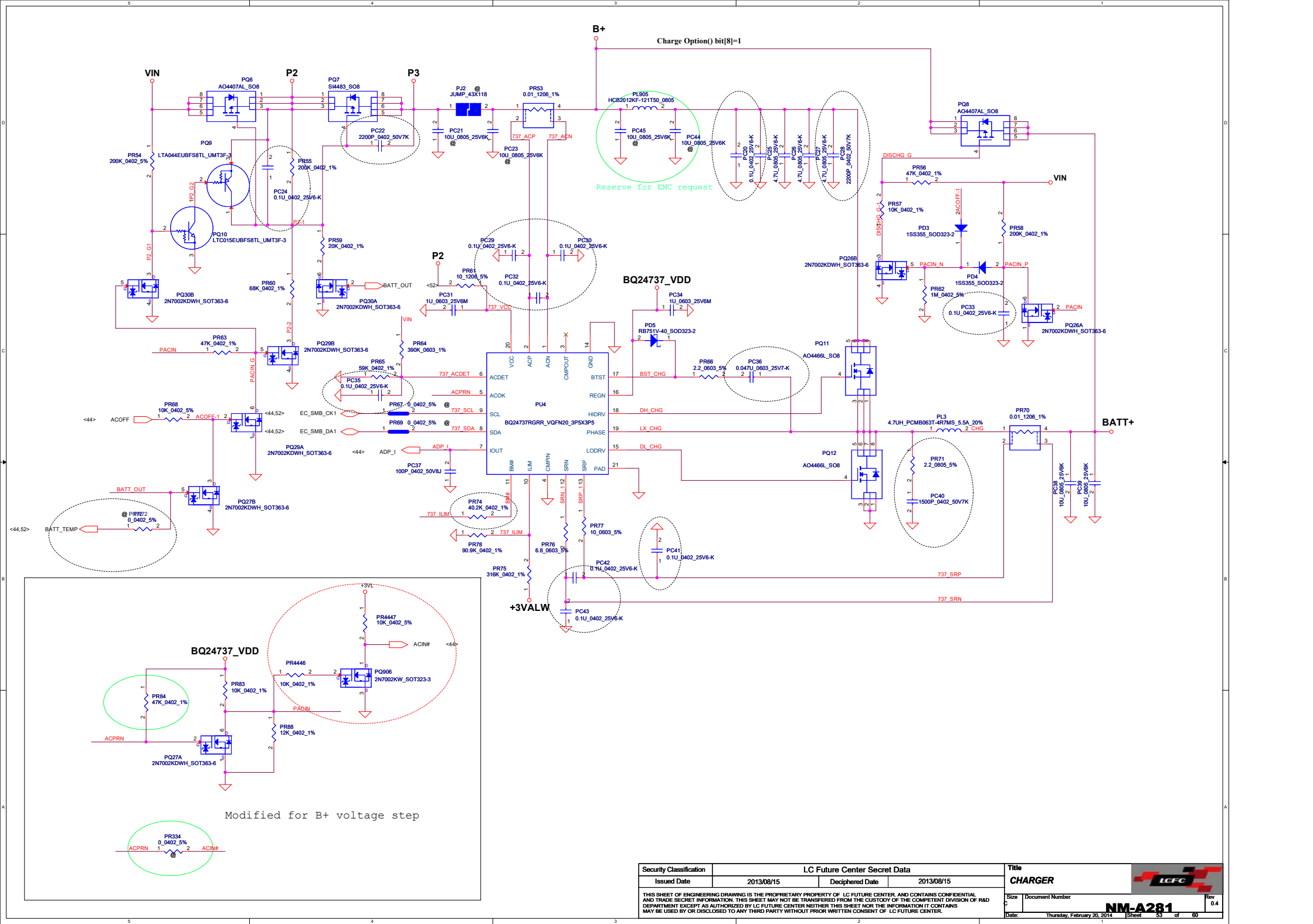


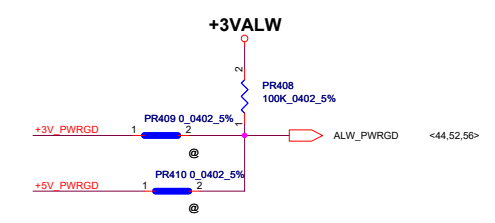
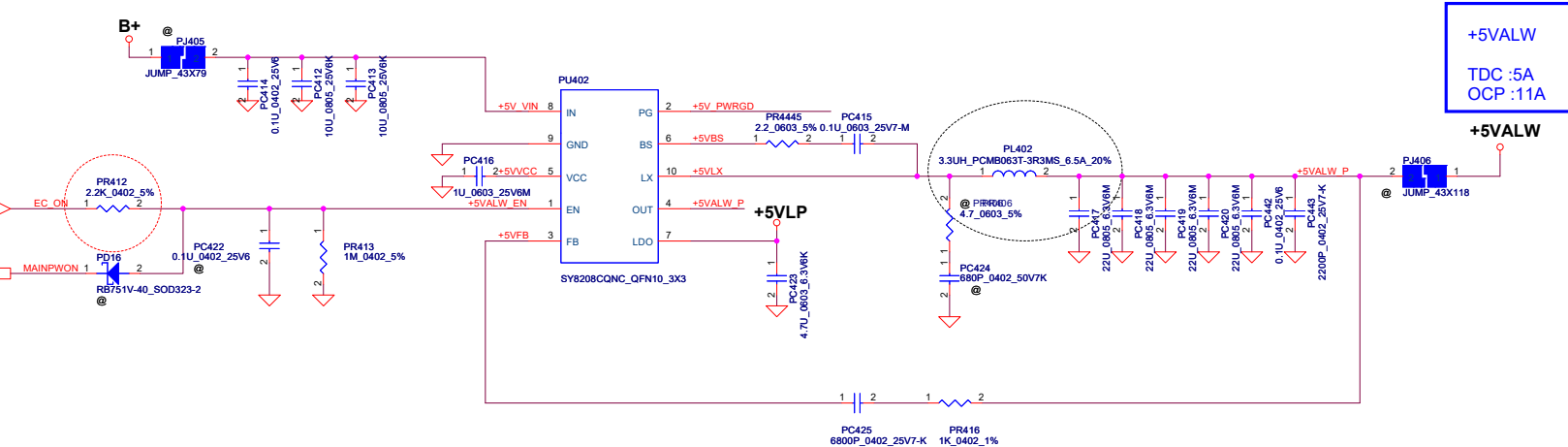
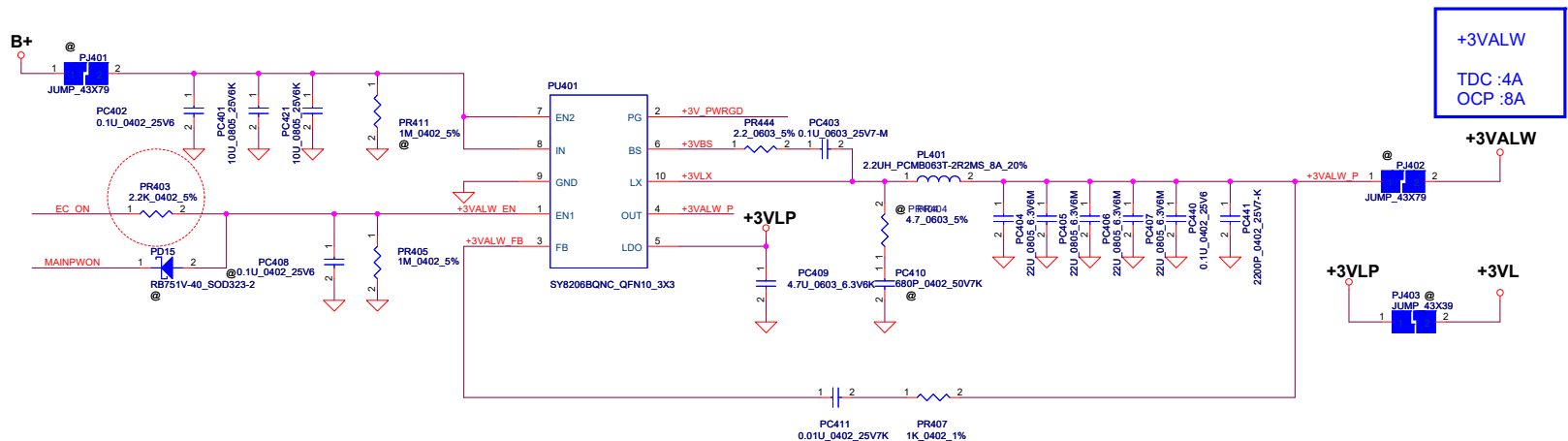
PH1 under CPU bottom side :
CPU thermal protection at 92+/-3 degree C
Recovery at 56 +/-3 degree C

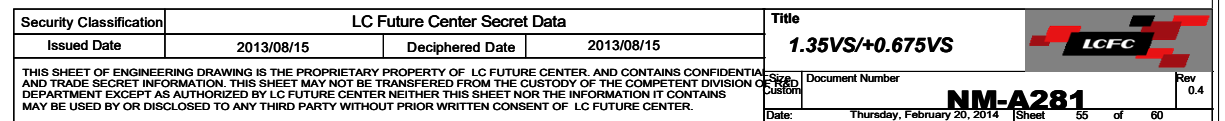


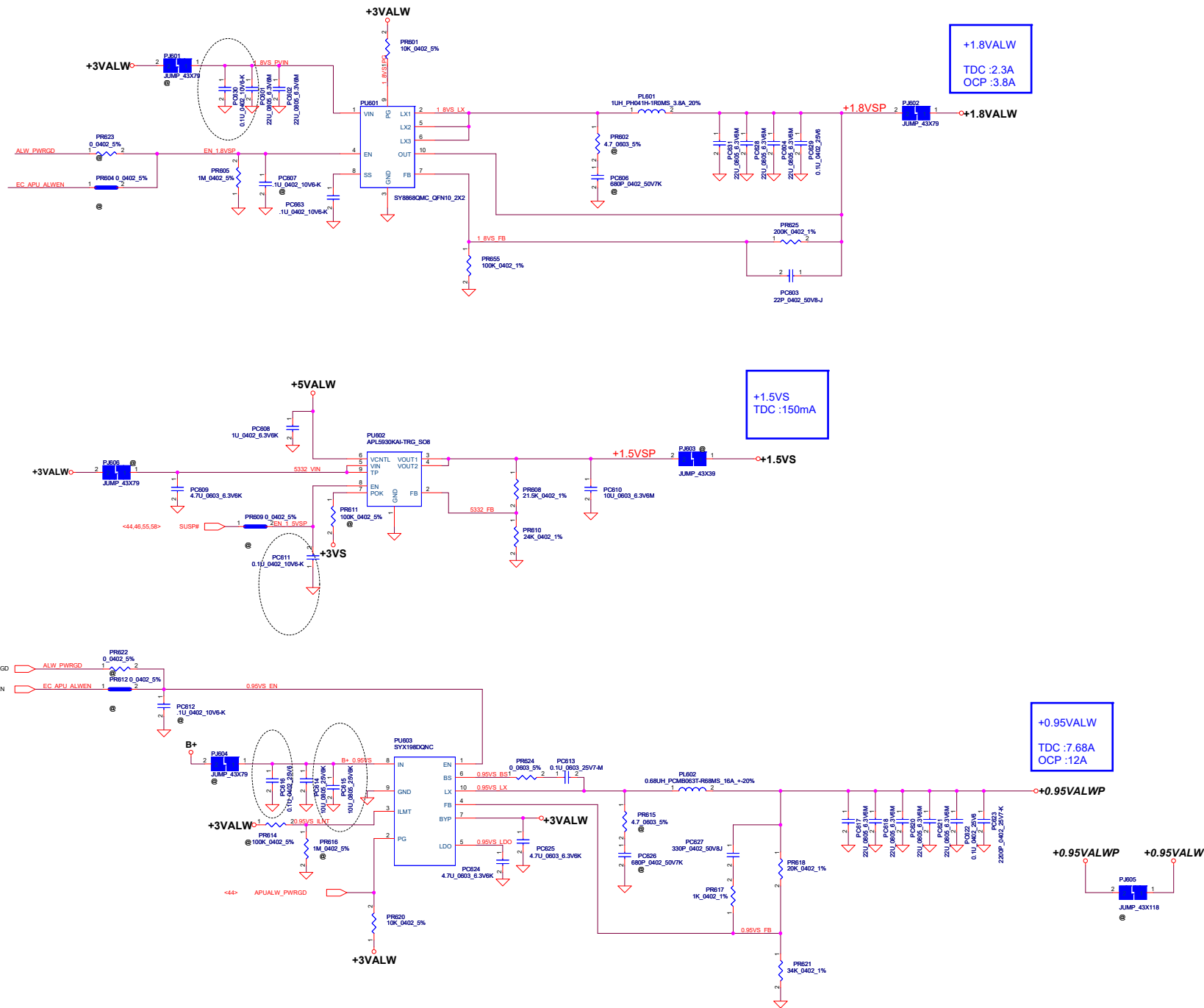
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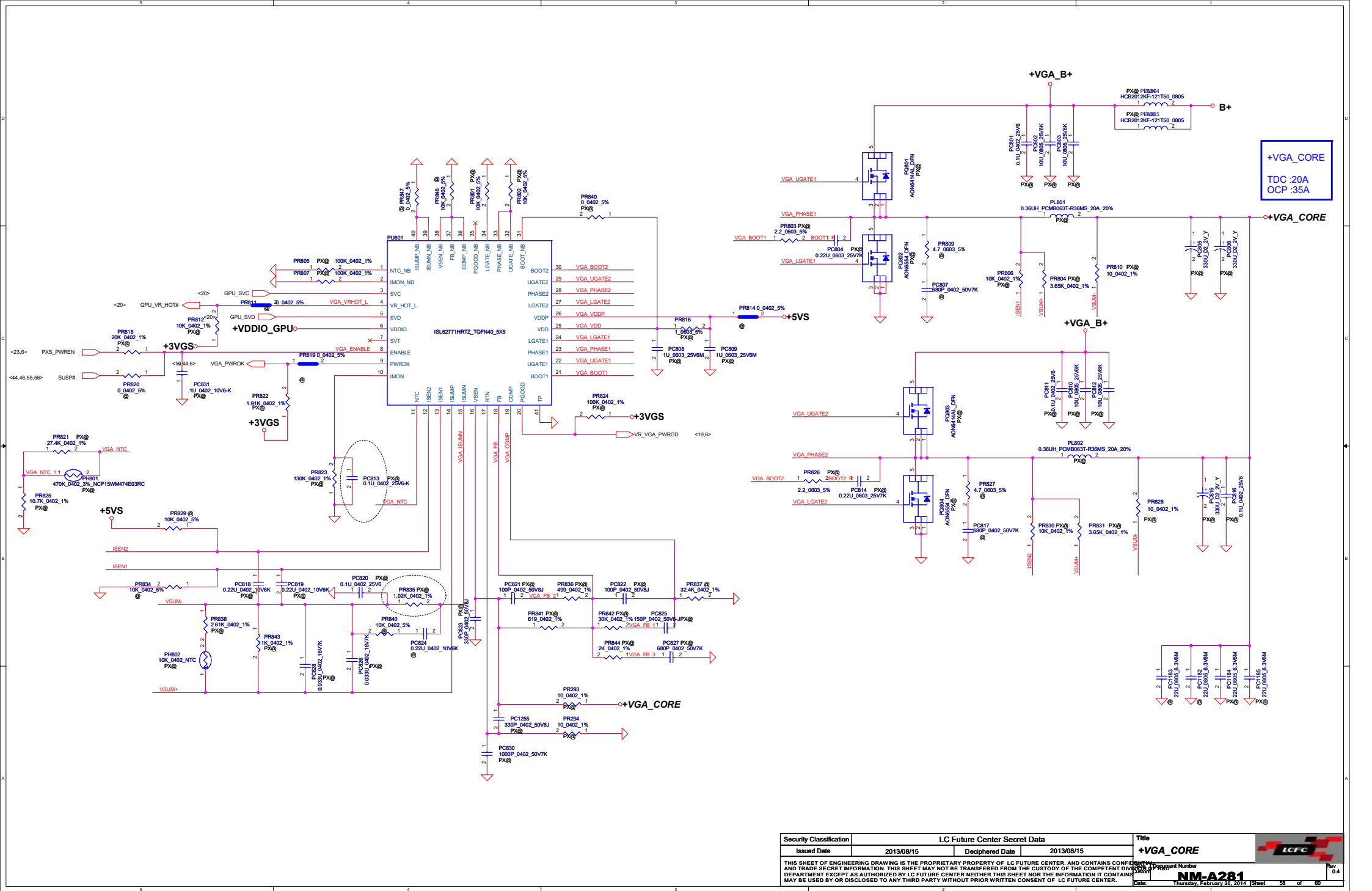




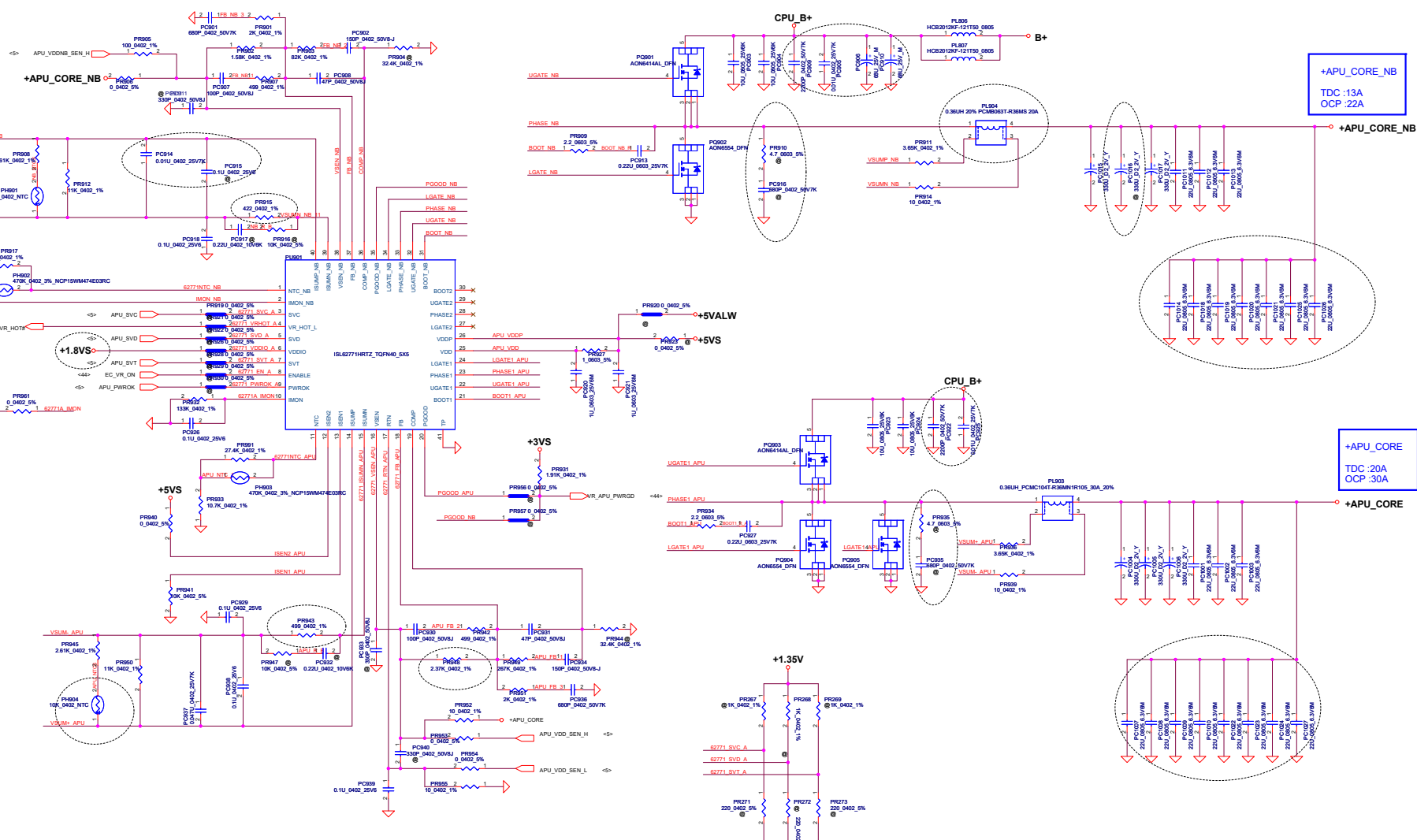




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PRE-PWROK METAL VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V(Default)

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