

# COMPAL CONFIDENTIAL

MODEL NAME :DDM70

PCB NO : LA-F401P

BOM P/N : 431A8F31LXX

## BR MLK14 KBL-U UMA

**Kabylake U42**

**2018-08-17**

**REV :3.0 (A02)**

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

U42@ : KBL-R U42 Component

U22@ : KBL-R U22 Component

DS3@ : Support DS3 Component

NDS3@ : No Support DS3 Component

650@ : Pop NPCT650VB2YX Component

750@ : Pop NPCT750JAAYX Component

[www.repair1.ru](http://www.repair1.ru)

MB PCB	
Part Number	Description
DAA000EE000	PCB 25A LA-F401P REV0 MB 1

Layout Dell logo



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REV:X00  
PWB: TXD2X

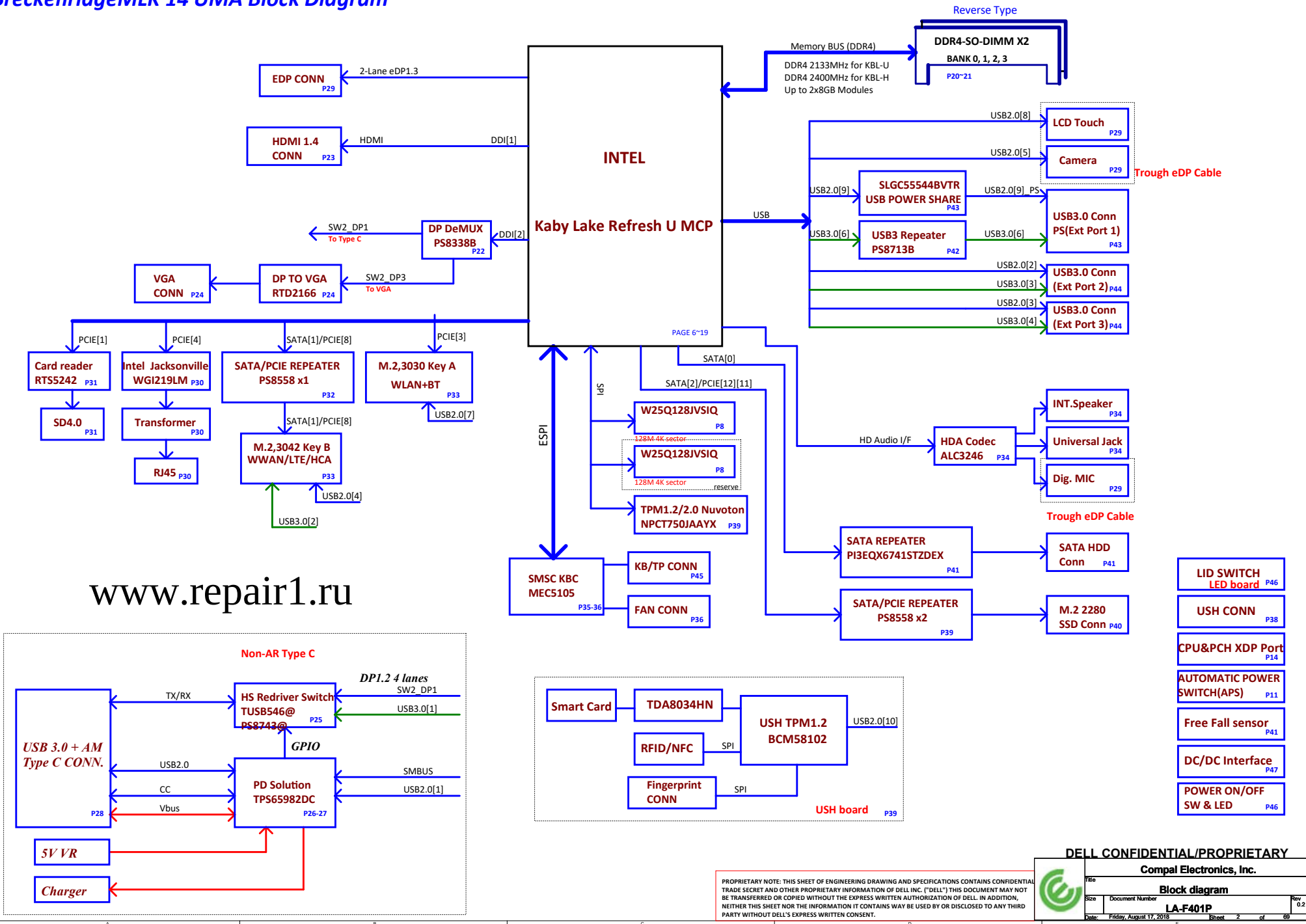
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BreckenridgeMLK 14 UMA Block Diagram



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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT	+3.3V_CV2 +1.2V_MEM +2.5V_MEM +1.0V_VCCST	+5V_RUN +3.3V_RUN +0.6V_DDR_VTT +1.8V_RUN +VCC_CORE +VCC_GT +VCC_SA +1.0VS_VCCIO
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				Type-C Port
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Left
USB3.0-4				JUSB3-->Rear Left
USB3.0-5		PCIE-1		Card Reader
USB3.0-6		PCIE-2		JUSB1-->Right
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		LOM
		PCIE-5		NA
		PCIE-6		NA
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	M.2 3042(SATA Cache or HCA)
		PCIE-9		NA
		PCIE-10		NA
		PCIE-11	SATA-1*	M.2 2280 SSD (PClex2 or SATA)
		PCIE-12	SATA-2	

12" not support JUSB3

For Breckenridge12/14/15 UMA

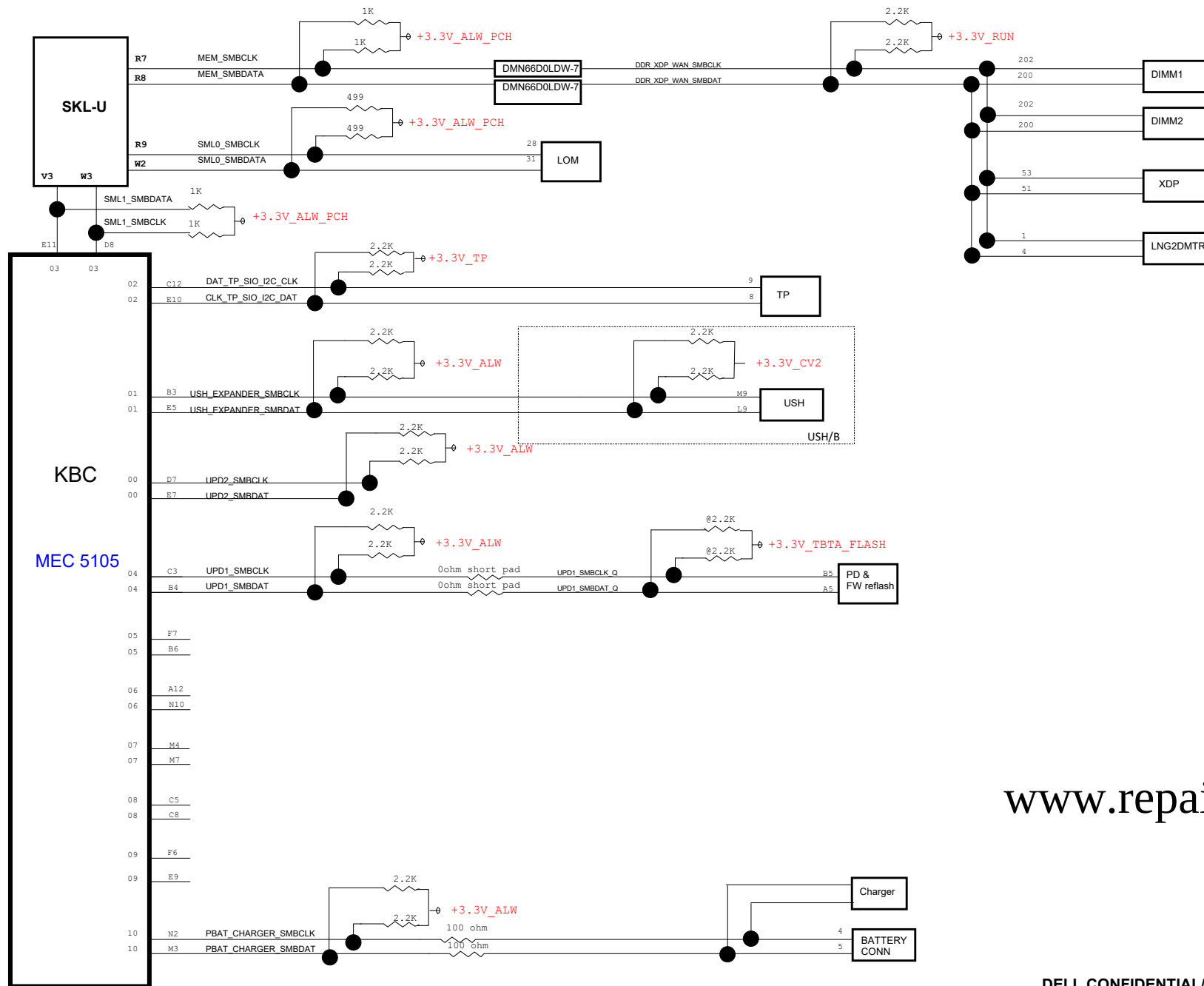
USB PORT#	DESTINATION
1	Type-C Port
2	JUSB2-->Left
3	JUSB3-->Rear Left
4	M2 3042(WWAN)
5	Camera
6	NA
7	M.2 3030(BT)
8	Touch Screen
9	JUSB1-->Right
10	USH

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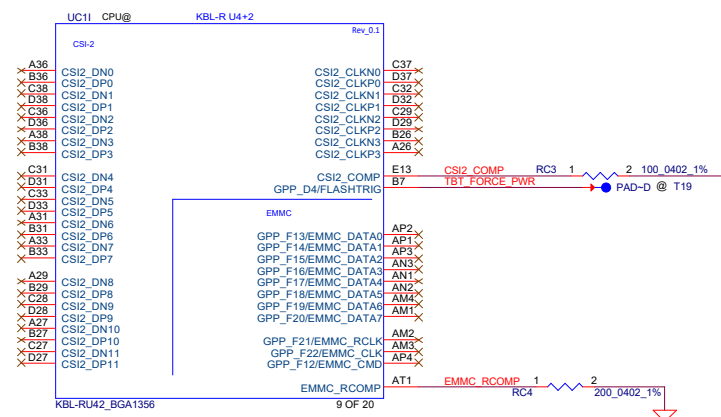
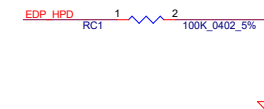
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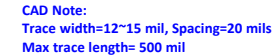
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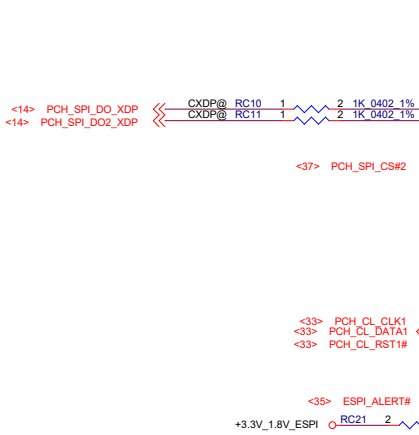
Port assignment

LA-F401P

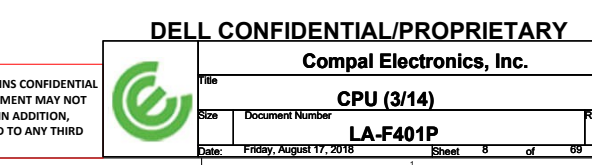
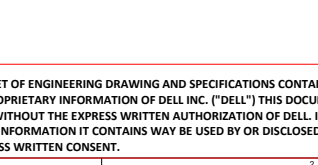
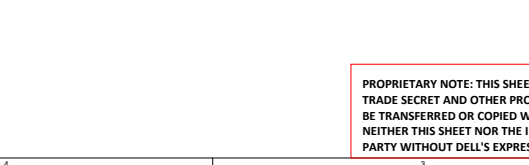
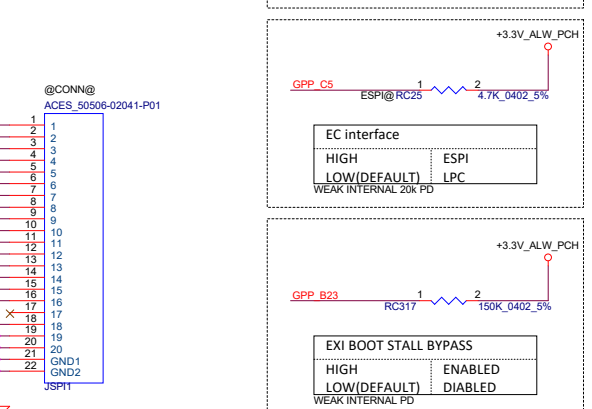
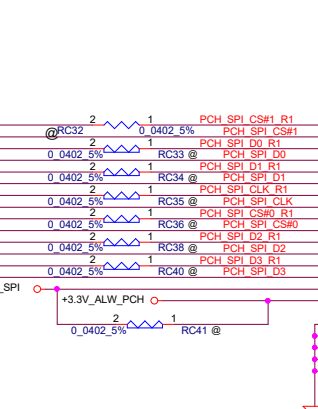
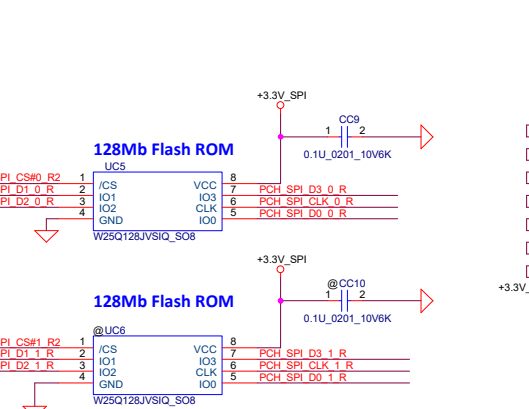
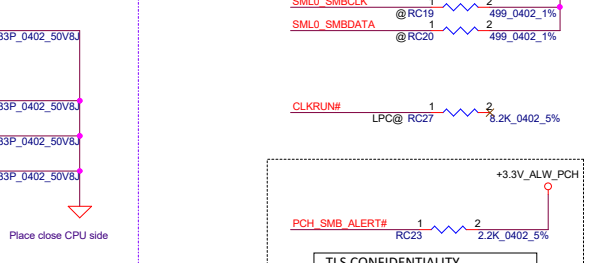
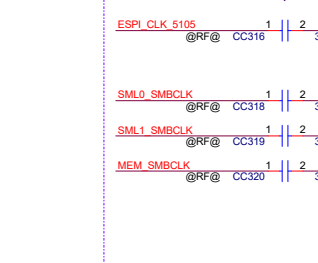
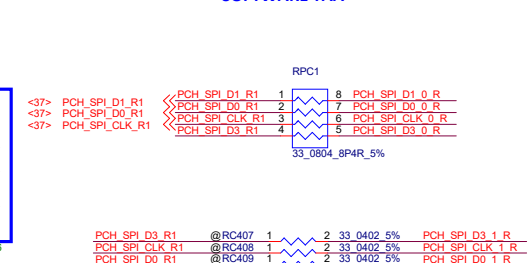
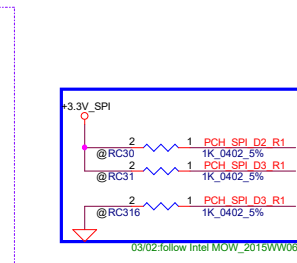
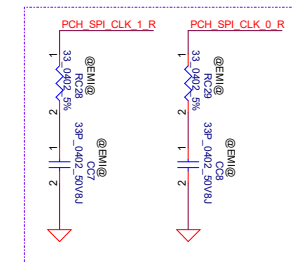
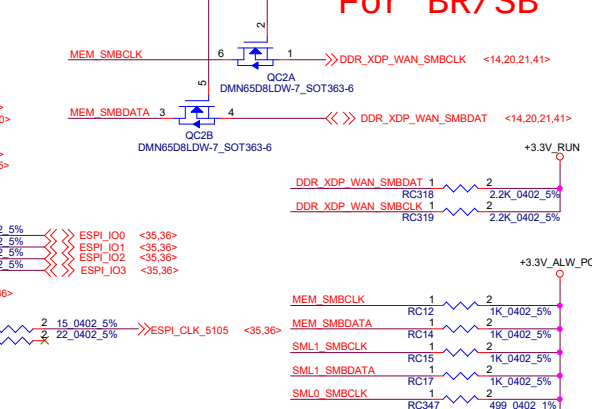
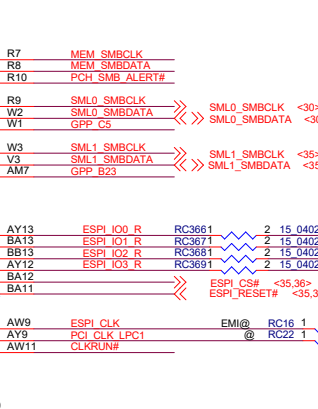
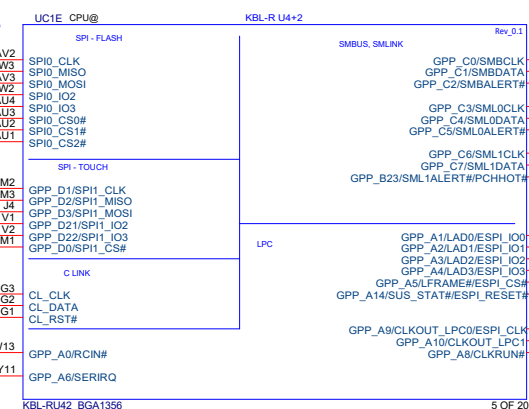
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SPI\_MOSI= SPI\_I00  
SPI\_MISO= SPI\_I01  
PCH EDS R0.7 p.235~236



### SOFTWARE TAA

### RF Request

### TLS CONFIDENTIALITY

HIGH LOW(DEFAULT) WEAK INTERNAL 20K PD

### EC interface

HIGH LOW(DEFAULT) WEAK INTERNAL 20K PD

### EXI BOOT STALL BYPASS

HIGH LOW(DEFAULT) WEAK INTERNAL PD

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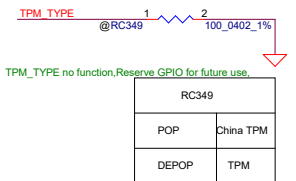
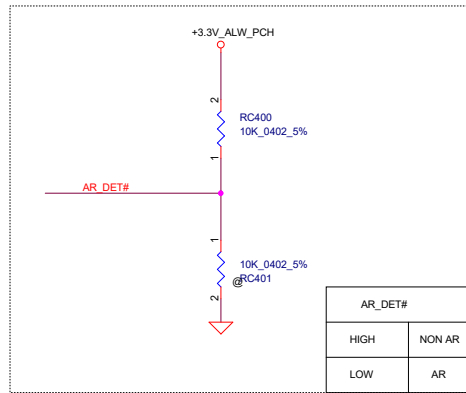
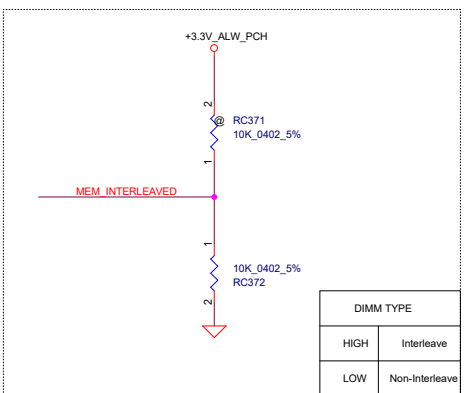
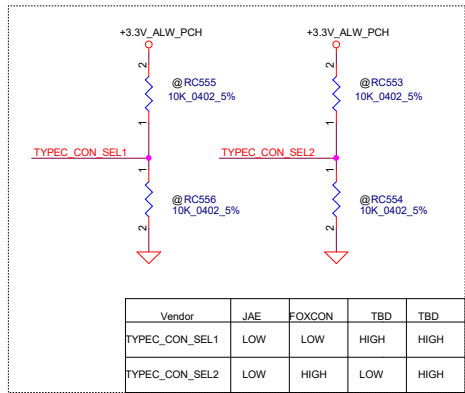
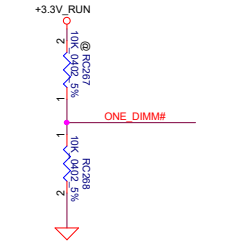
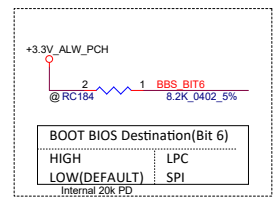
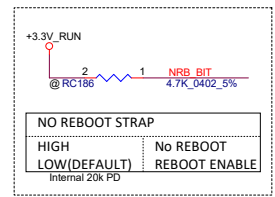
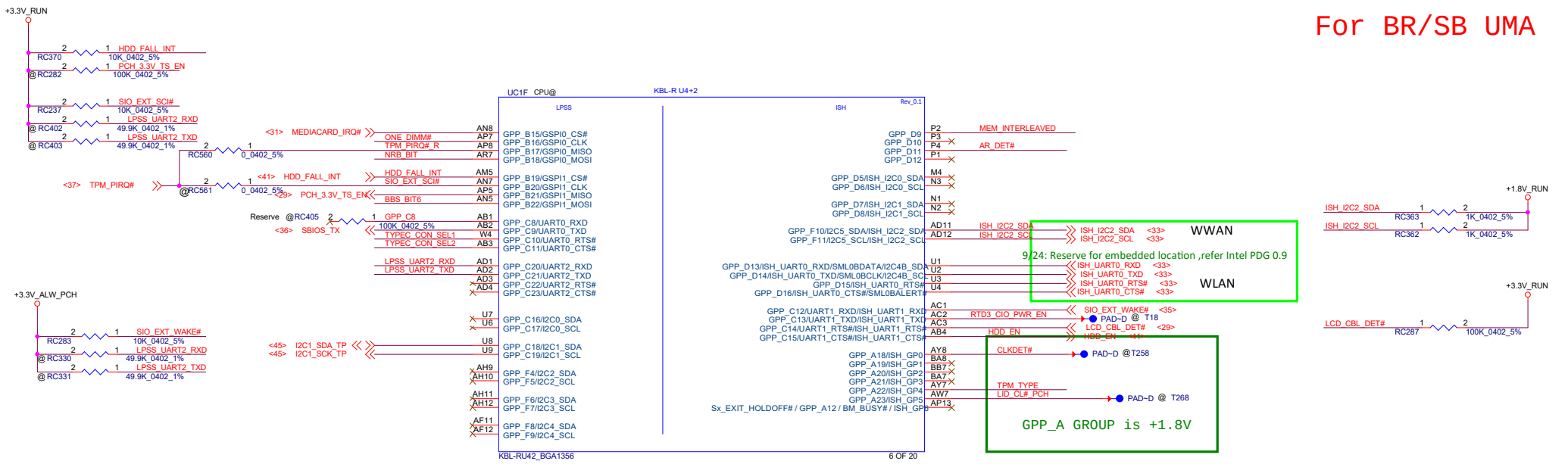
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**CPU (4/14)**

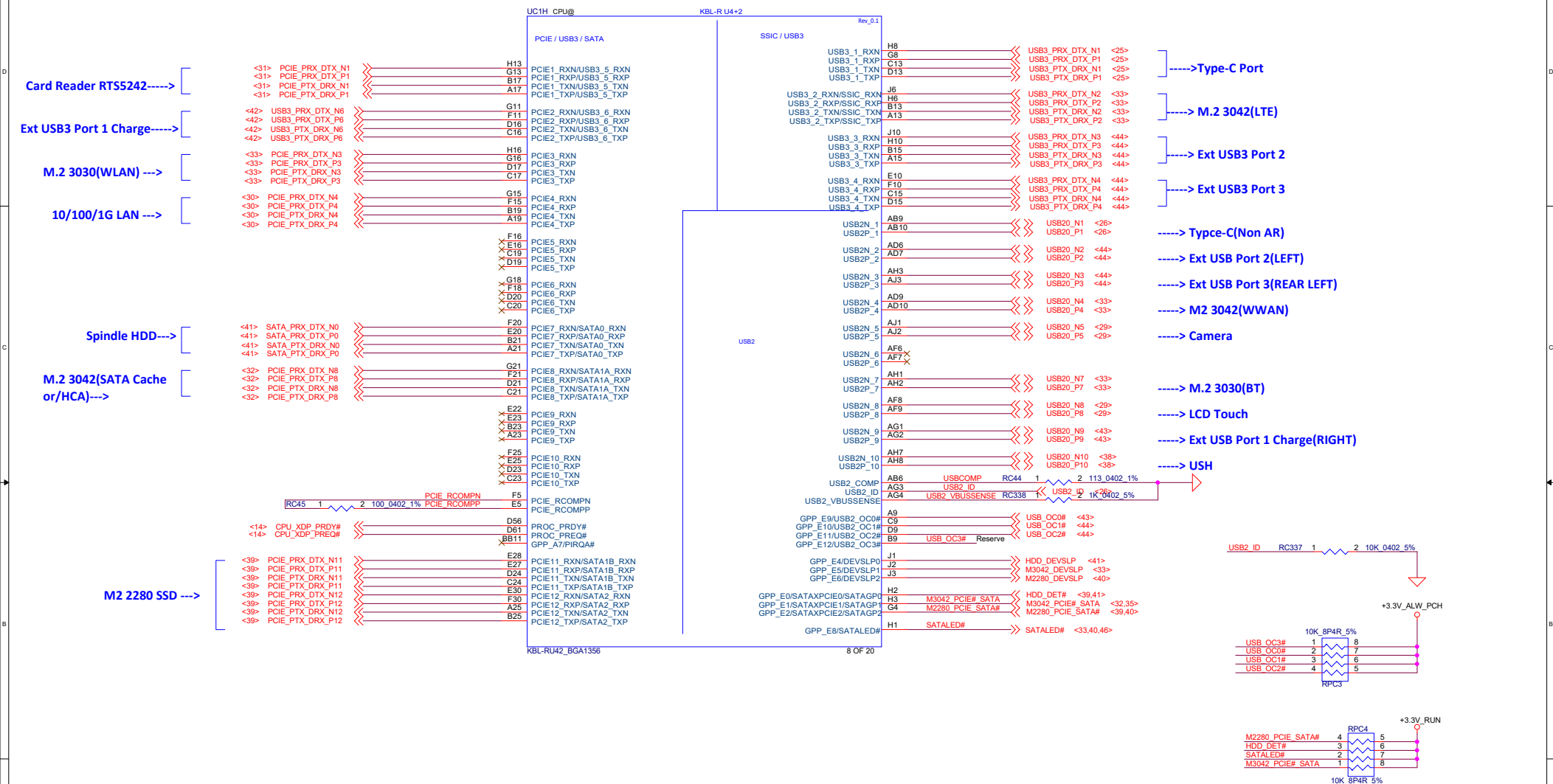
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For NON AR, Breckenridge 12/14/15 UMA



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**CPU (5/14)**

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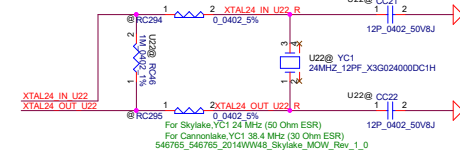
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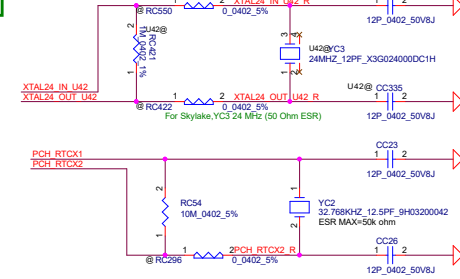


For BR UMA

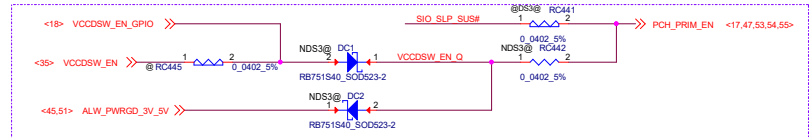
For KBL-R U22



For KBL-R U42



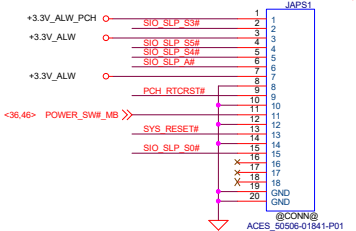
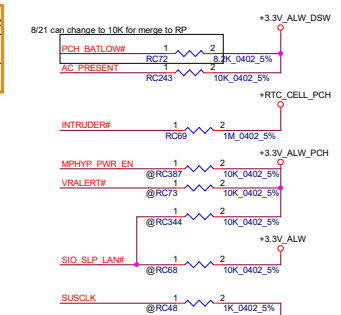
CMOS1 must take care short & touch risk on layout placement



	RC439	RC440	RE536	RC215	RC441	RC442
Support DS3	V	X	V	X	V	X
No Support DS3	X	V	X	V	X	V

'V' mean POP,

'X' mean DE-POP

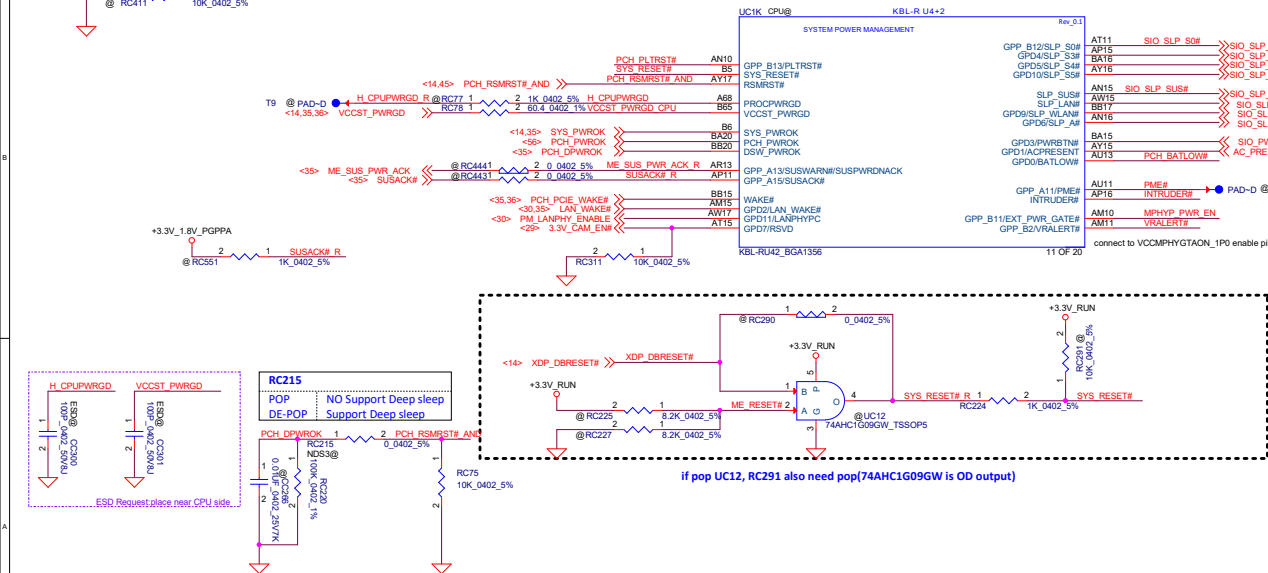
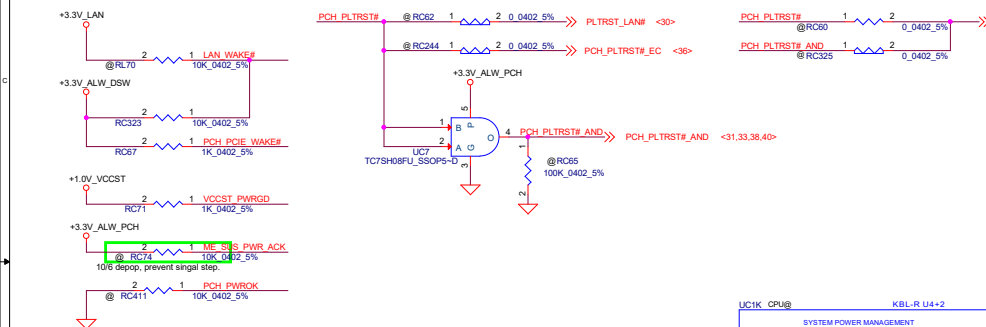
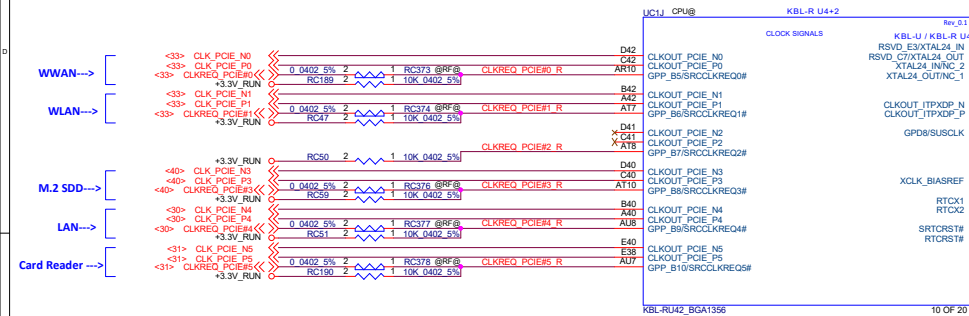


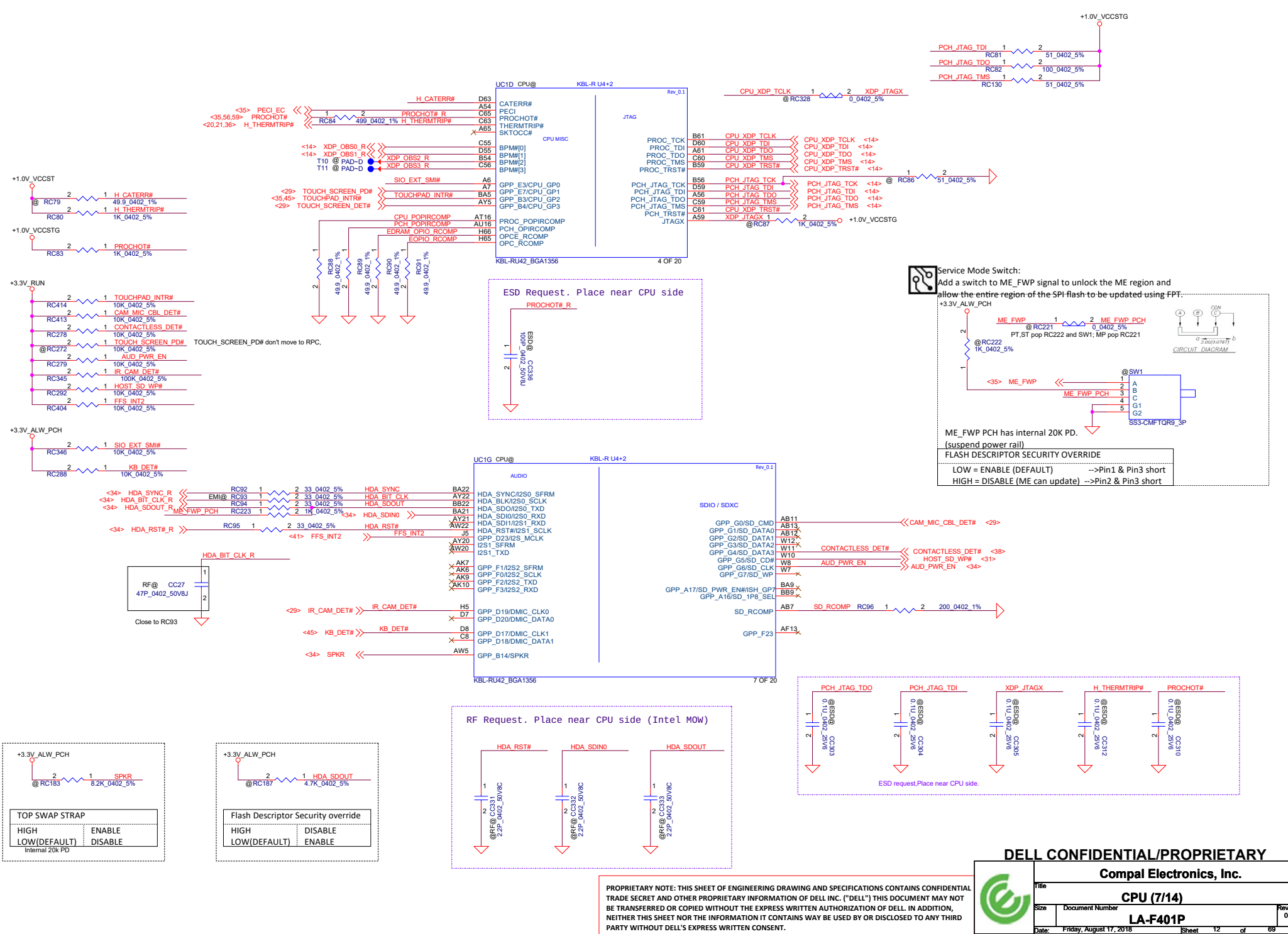
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+3.3V\_ALW\_PCH

RC183 2 1 8.2K\_0402\_5%

SPKR

TOP SWAP STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Internal 20K PD

+3.3V\_ALW\_PCH

RC187 2 1 4.7K\_0402\_5%

HDA\_SDOUT

Flash Descriptor Security override	
HIGH	DISABLE
LOW(DEFAULT)	ENABLE

RF Request. Place near CPU side (Intel MOW)

HDA\_RST#

ESD@ CC331 1 2 2.2P\_0402\_5V08C

HDA\_SDIN0

ESD@ CC332 1 2 2.2P\_0402\_5V08C

HDA\_SDOUT

ESD@ CC333 1 2 2.2P\_0402\_5V08C

ESD request, Place near CPU side.

PCH\_JTAG\_TDO

ESD@ CC303 1 2 0.1u\_0402\_25V0

PCH\_JTAG\_TDI

ESD@ CC304 1 2 0.1u\_0402\_25V0

XDP\_JTAGX

ESD@ CC305 1 2 0.1u\_0402\_25V0

H\_THERMTRIP#

ESD@ CC312 1 2 0.1u\_0402\_25V0

PROCHOT#

ESD@ CC310 1 2 0.1u\_0402\_25V0

Service Mode Switch:

Add a switch to ME\_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT:

ME\_FWP PCH

PT.ST pop RC222 and SW1; MP pop RC221

CIRCUIT DIAGRAM

ME\_FWP PCH

SW1

SS3-CMFQ09\_3P

ME\_FWP PCH has internal 20K PD.

(suspend power rail)

FLASH DESCRIPTOR SECURITY OVERRIDE	
LOW = ENABLE (DEFAULT)	-->Pin1 & Pin3 short
HIGH = DISABLE (ME can update)	-->Pin2 & Pin3 short

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CPU (7/14)

LA-F401P

Rev 0.2

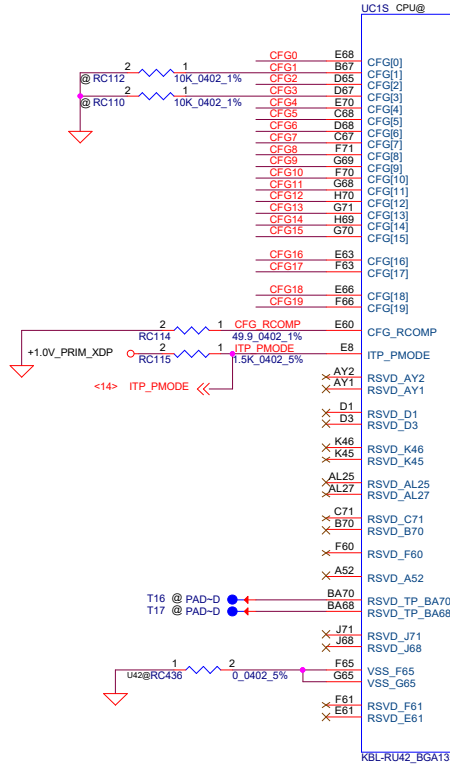
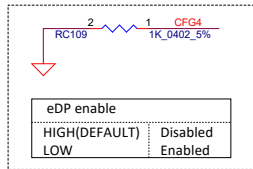
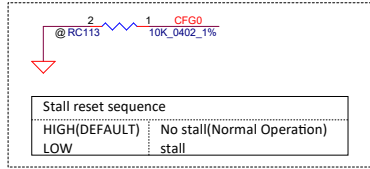
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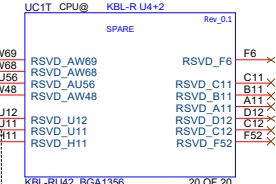
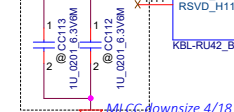
<14> CFG[0..19] <<

### CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin

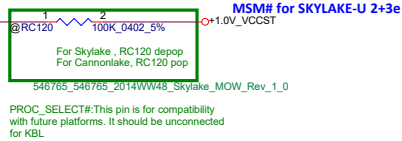


1/5 2014WW52 MOW reserve to support Cannonlake-U PCH compatibility close UC1 U11/U12 and <400mil

+1.8V\_PRIM @RC313



ZVM# for SKYLAKE-U 2+3e



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CPU (8/14)

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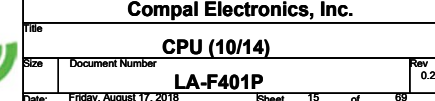


+VCC\_CORE

+VCC\_CORE



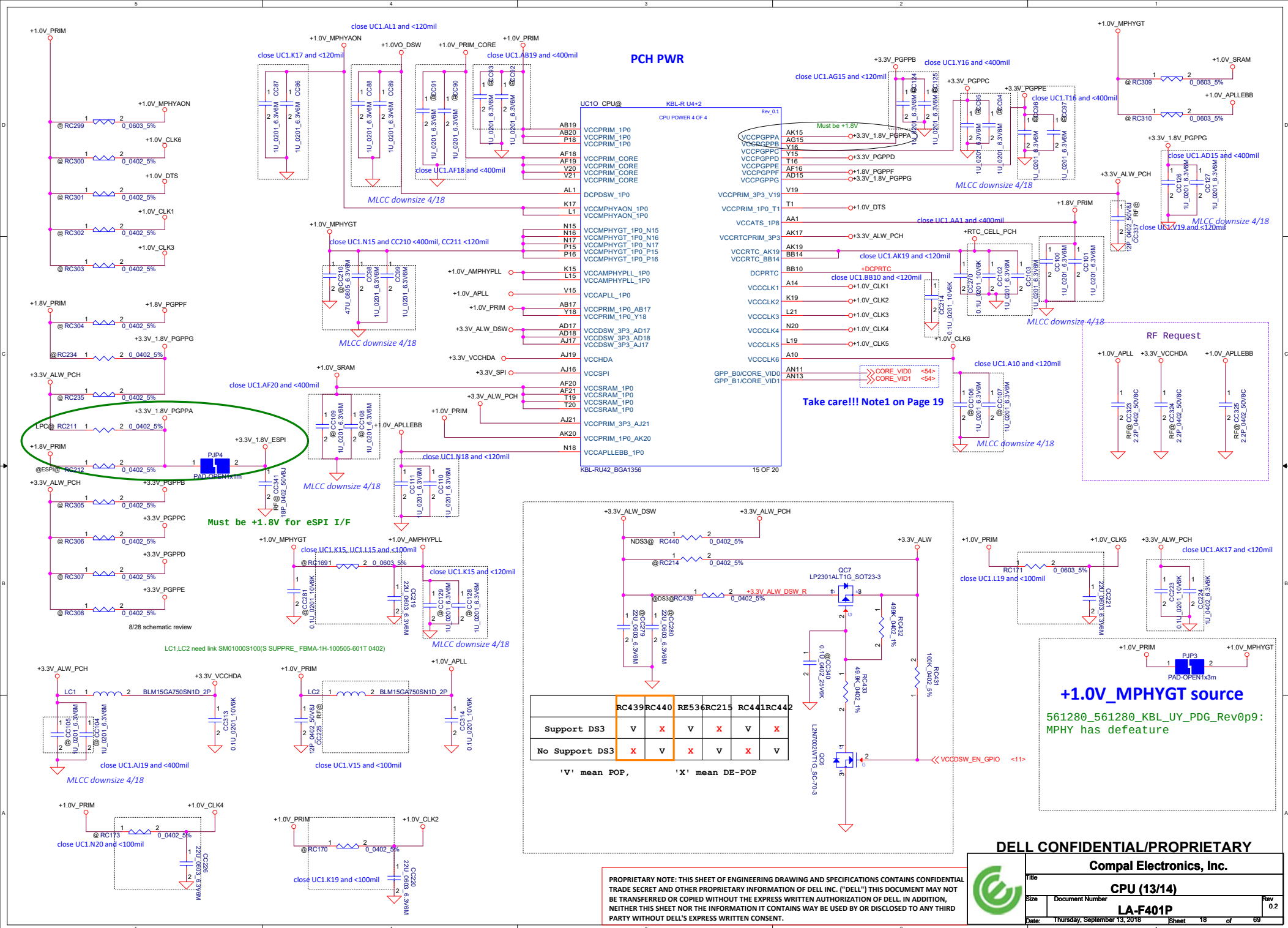
**Component placement order:**  
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source











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**CPU (13/14)**

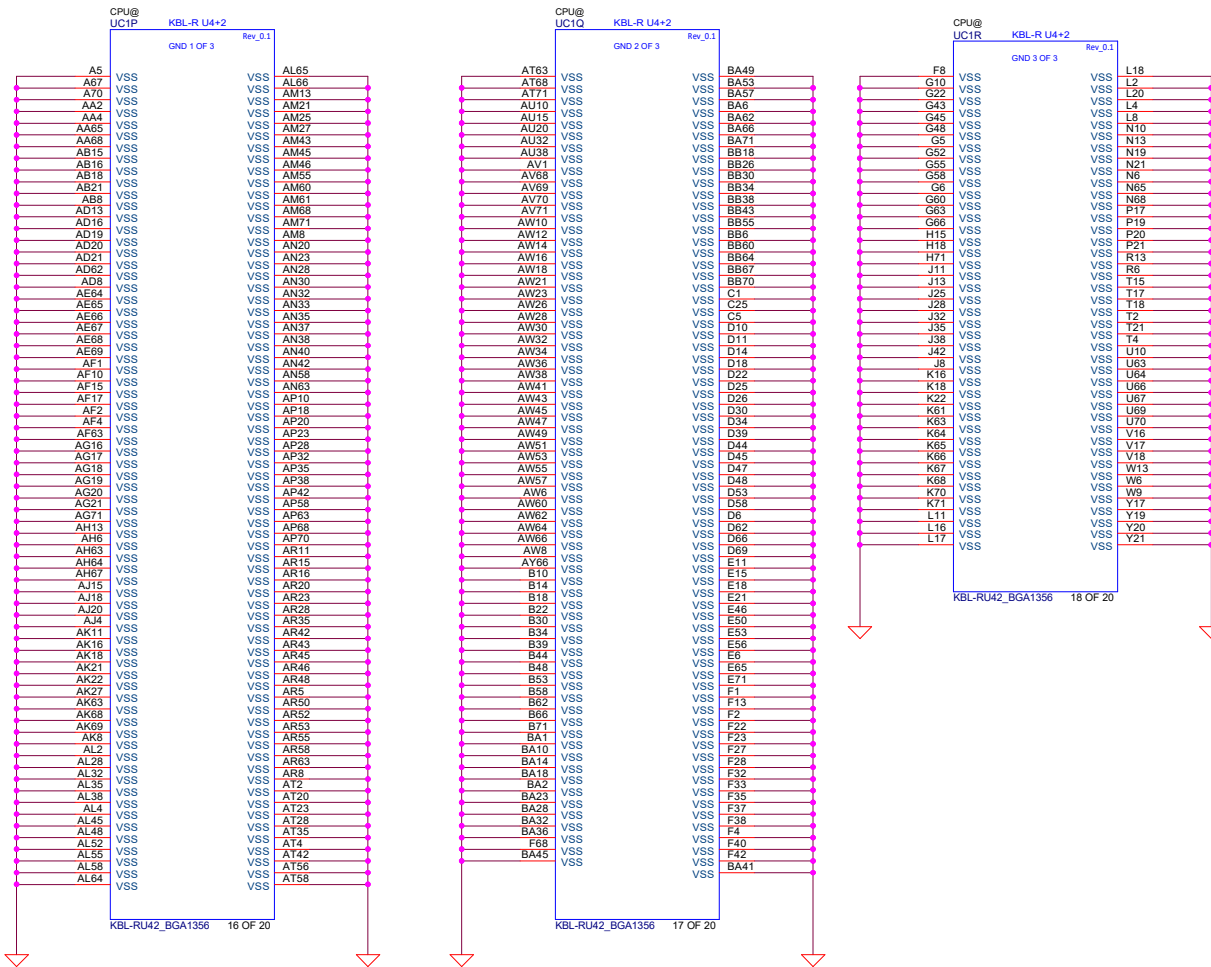
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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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Note1: VCCPRIM\_CORE Implementation with PCH CORE\_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



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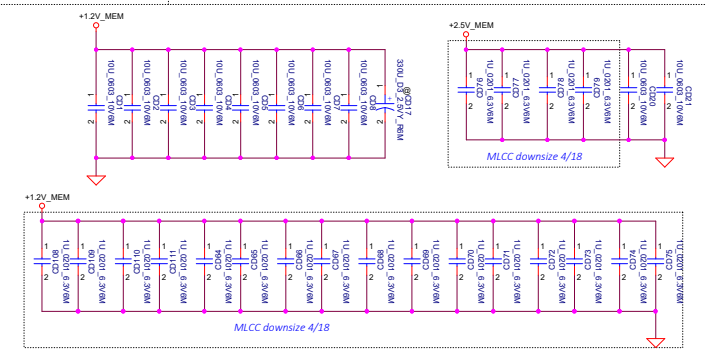
Compai Electronics, Inc.

Title			
CPU (14/14)			
Size	Document Number		Rev
	LA-F401P		0.2
Date:	Friday, August 17, 2018	Sheet 19 of 89	

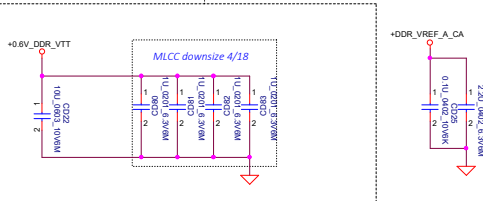
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<7> DDR\_A\_QS[0..7] << >>  
 <7> DDR\_A\_QD[0..63] << >>  
 <7> DDR\_A\_QS[0..7] << >>  
 <7> DDR\_A\_MA[0..16] << >>

Layout Note:  
Place near JDIMM1

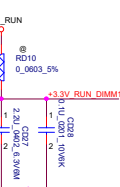
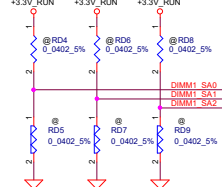


Layout Note:  
Place near  
JDIMM1.258

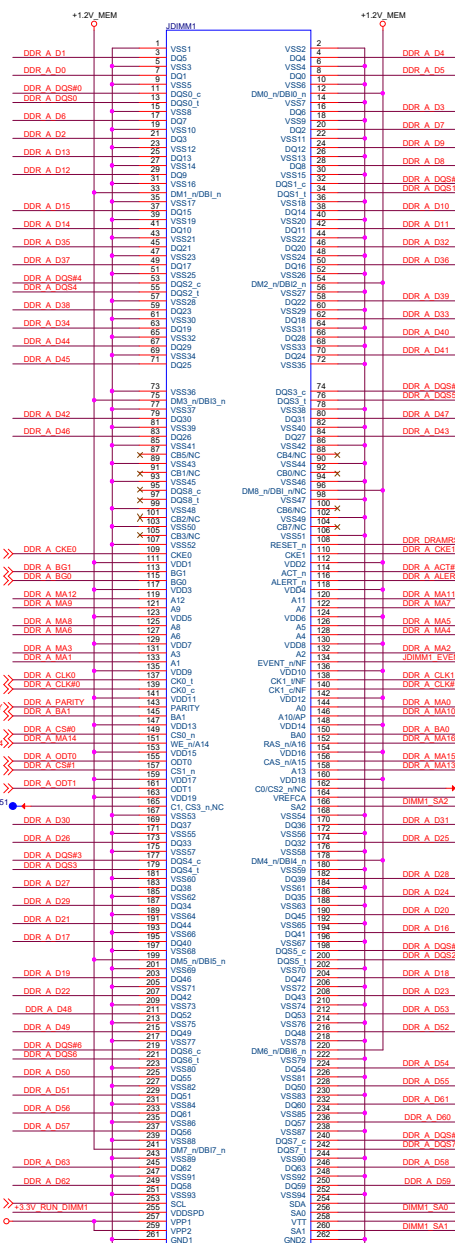


## DIMM Select

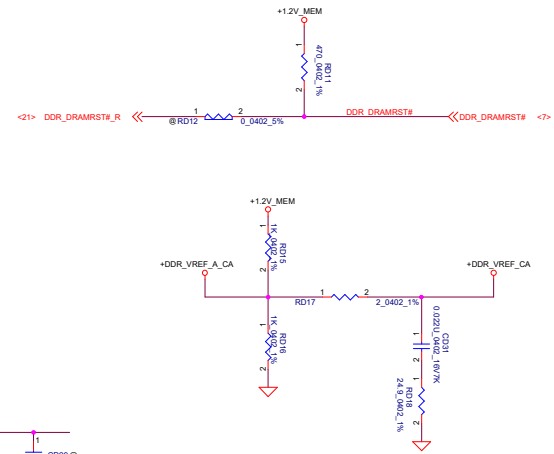
	SA0	SA1	SA2
DIMM1	0	0	0
DIMM2	1	0	0
DIMM3	0	1	0
DIMM4	1	1	0



<8,14,21,41> DDR\_XDP\_WAN\_SMBCLK << >>  
 +2.5V\_MEM



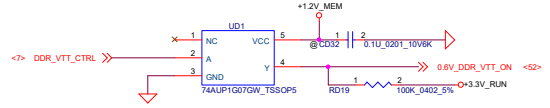
LINK DAN05-Q0406-0103  
 LINK DAN05-Q0406-0103 DONE



<7> DDR\_A\_QS[0..7] << >>  
 <7> DDR\_A\_QD[0..63] << >>  
 <7> DDR\_A\_QS[0..7] << >>  
 <7> DDR\_A\_MA[0..16] << >>



## 6/8 Change to SA00007WE00 DII



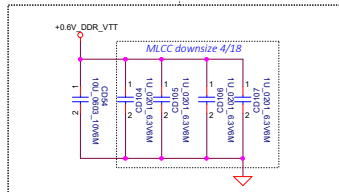
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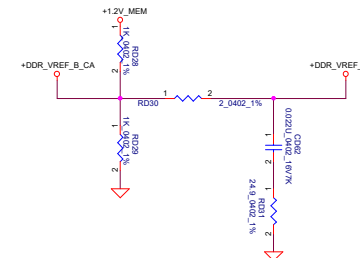
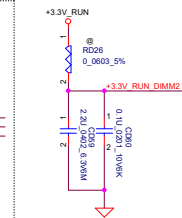
Rev	Document Number	Rev
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Date	Friday, August 17, 2018	Sheet 20 of 60

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Layout Note:  
Place near  
JDIMM2.258



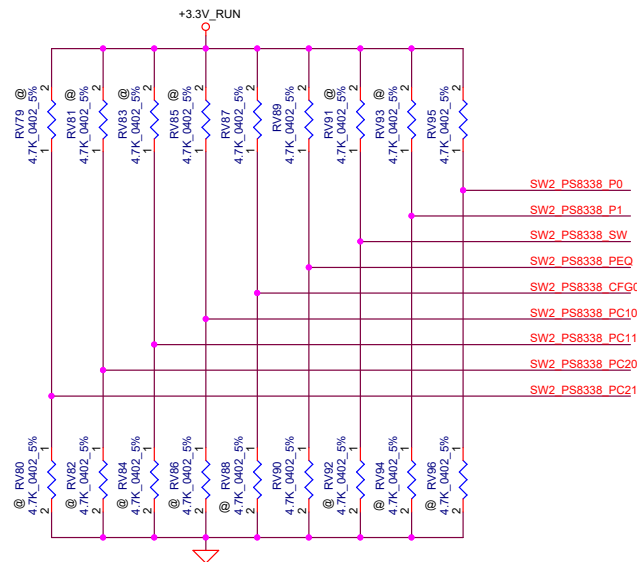
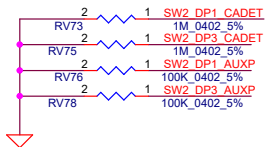
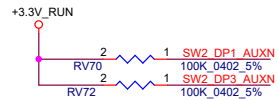
The schematic diagram illustrates a test circuit with three identical parallel branches. Each branch is connected to a +3.3V\_RUN supply. The first branch contains a resistor labeled @RD20 0\_0402\_5% in series with a diode labeled DMM2. The second branch contains a resistor labeled @RD22 0\_0402\_5% in series with a diode labeled DMM2. The third branch contains a resistor labeled @RD24 0\_0402\_5% in series with a diode labeled DMM2. The diodes are connected to ground through resistors labeled RD21, RD23, and RD25, respectively. The ground connections are indicated by red triangles at the bottom of each branch.



Title		DDR4		Rev	0.2
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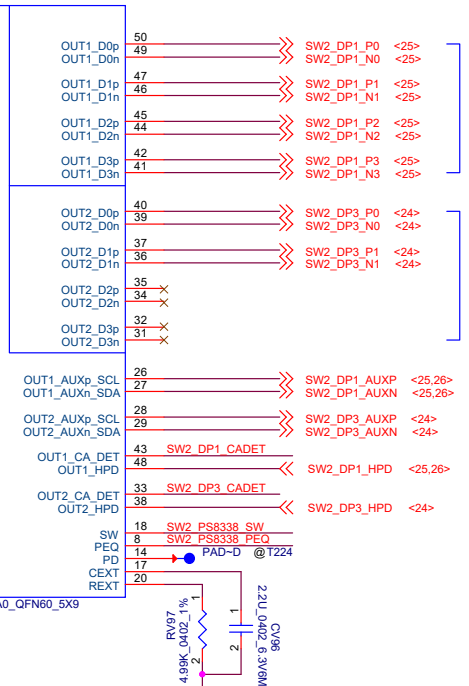
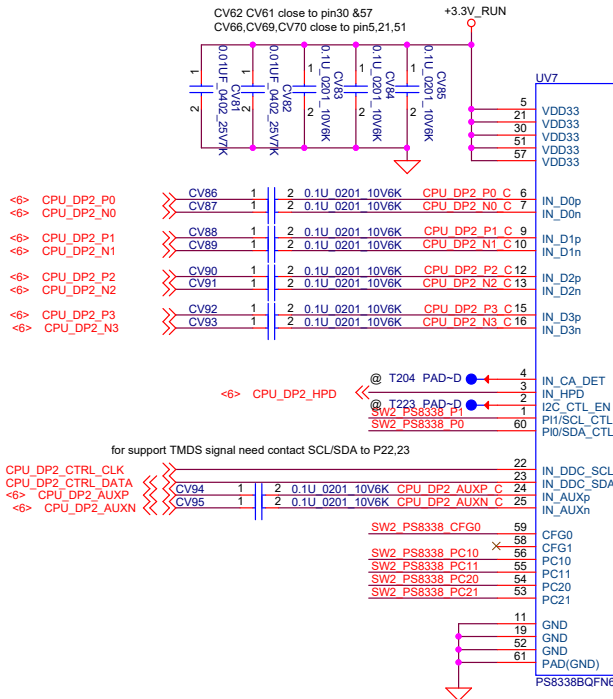
For Breckenridge 12/14/15

Priority: Type-C -> VGA



Port switching control or priority configuration. Internal pull down ~150K $\Omega$ , 3.3V I/O  
 For Control Switching Mode (CFG0 = L):  
 SW = L: Port1 is selected (default)  
 SW = H: Port2 is selected  
**For Automatic Switching Mode (CFG0 = H):**  
 SW = L: Port1 has higher priority when both ports are plugged  
 SW = H: Port2 has higher priority when both ports are plugged (default)  
 vendor suggest MUX use LLEQ, PEQ=M and PIO=H !!!  
 Programmable input equalization levels, Internal pull down at ~150Kohm, 3.3V I/O  
 PEQ =  
 L: default, LEQ, compensate channel loss up to 11.5dB @HBR2  
 H: HEQ, compensate channel loss up to 14.5dB @HBR2  
**H: LLEQ, compensate channel loss up to 8.5dB @HBR2**

PIO: Automatic EQ disable, Internal pull down ~150K ohm, 3.3V I/O  
 PIO = L: Automatic EQ enable (default)  
**H: Automatic EQ disable**

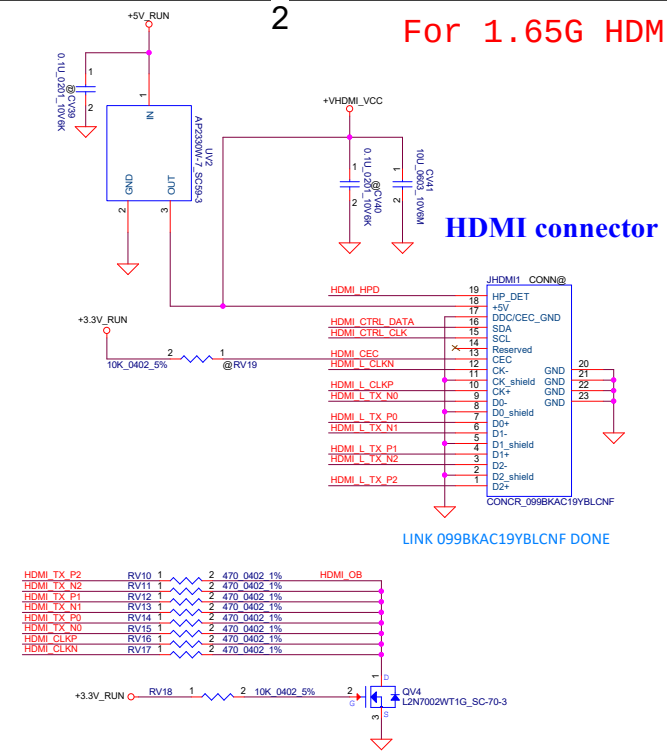
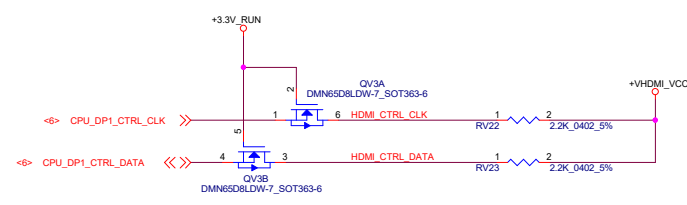
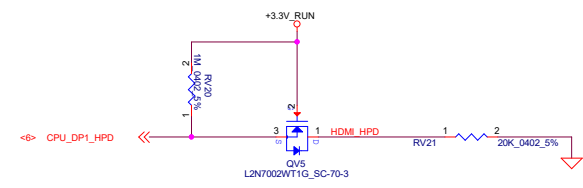
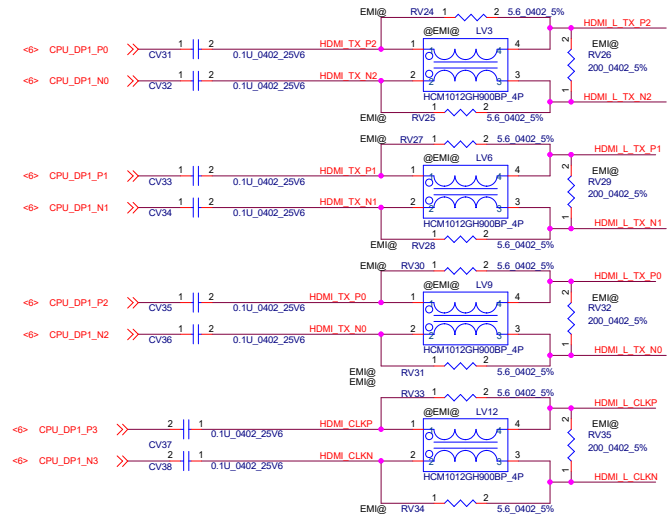


-----> TYPE C

-----> VGA

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Title <b>DP SW2 PS8348B</b>			
Size	Document Number	Rev 0.2	
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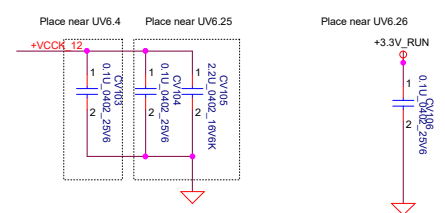


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		POL1(P10)	
		0	1
POL2 (P9)	0	X	X
	1	ROM	EEPROM



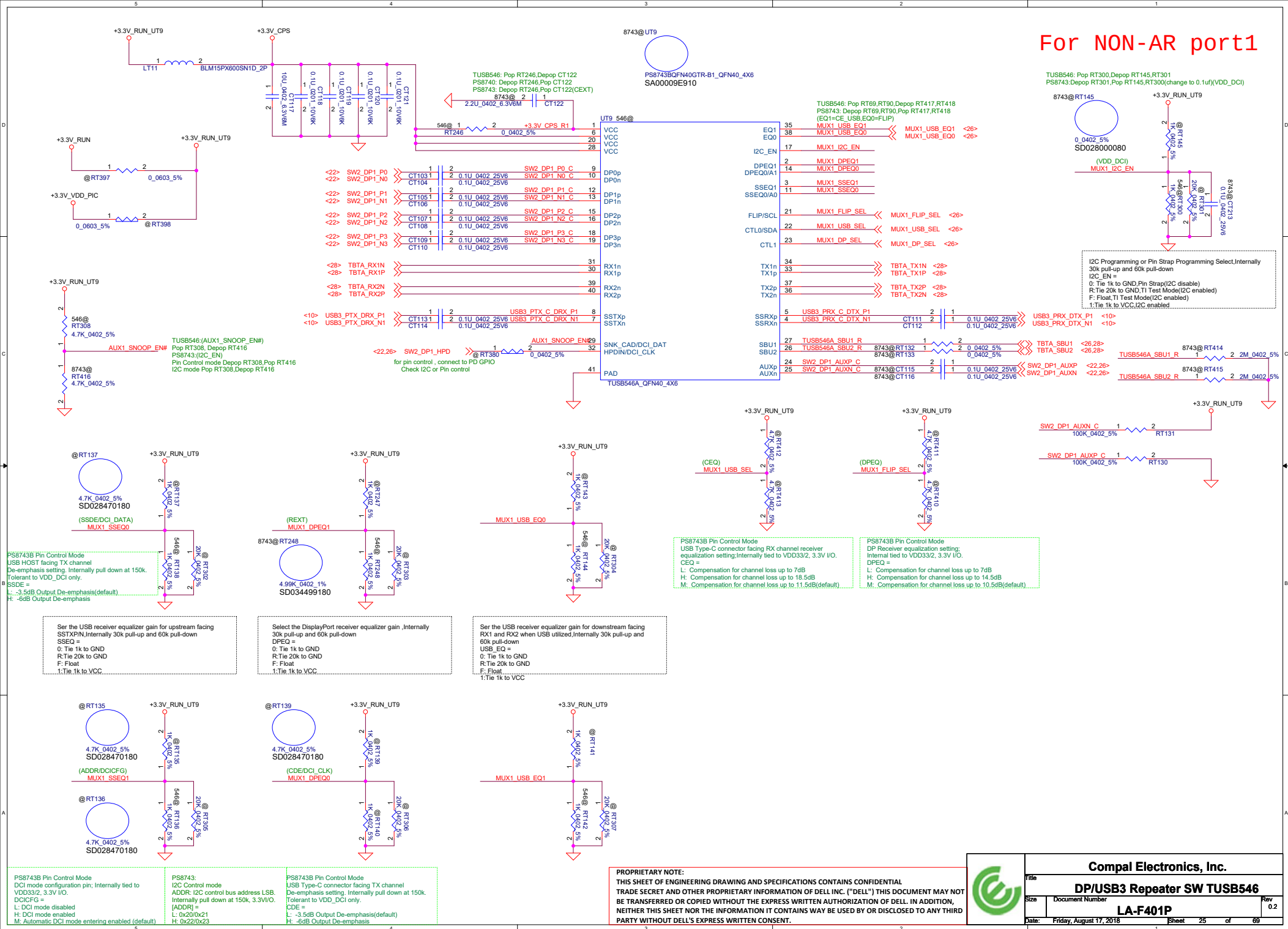
**Compal Electronics, Inc.**

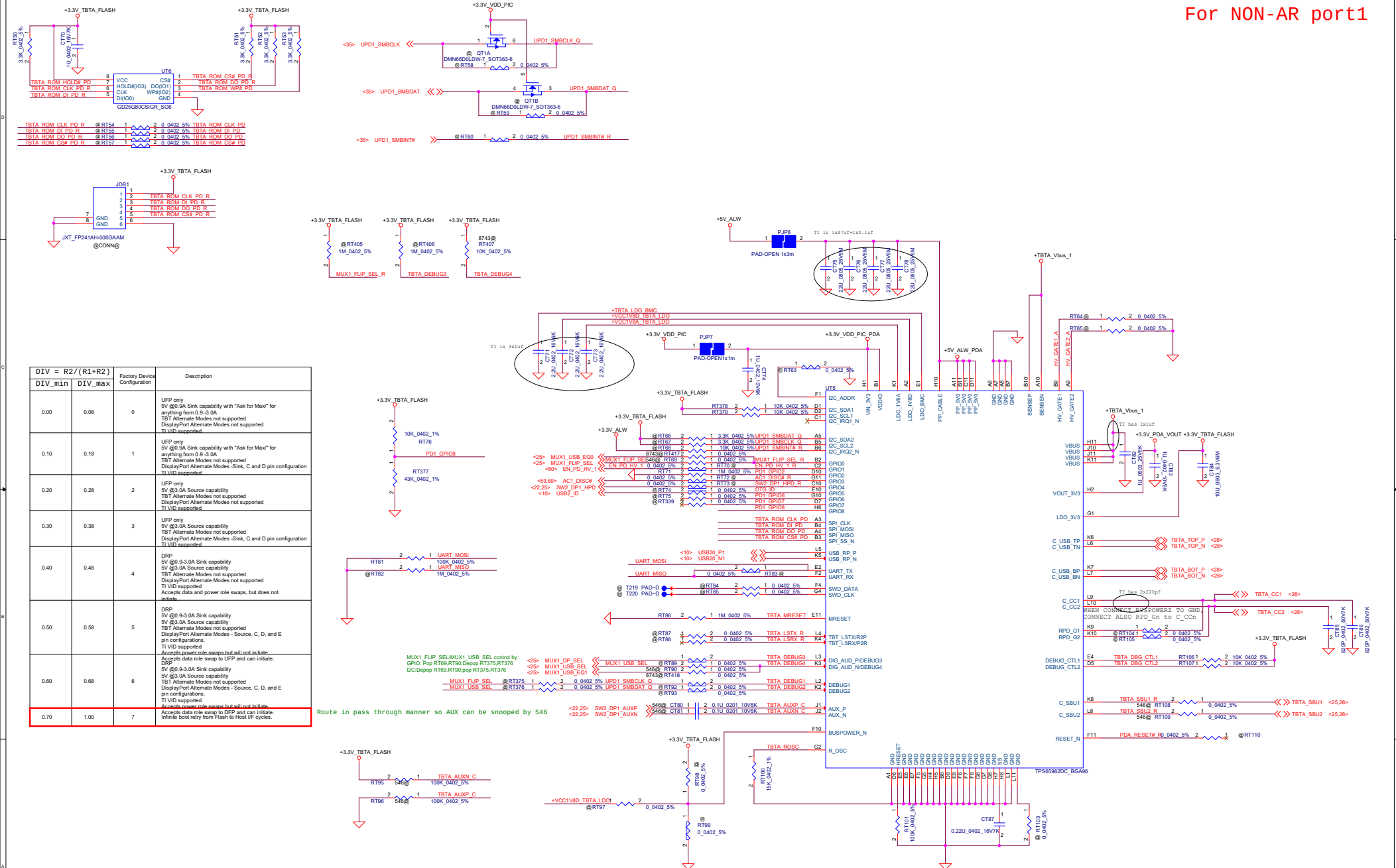
**LA-F401P**

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Link TPS65982DC (from SA00009W200 to SA00009W210) 08/04  
running change from SA00009W210 to SA0000AK400 12/31

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Compal Electronics, Inc.

Type CIPD Controller TI

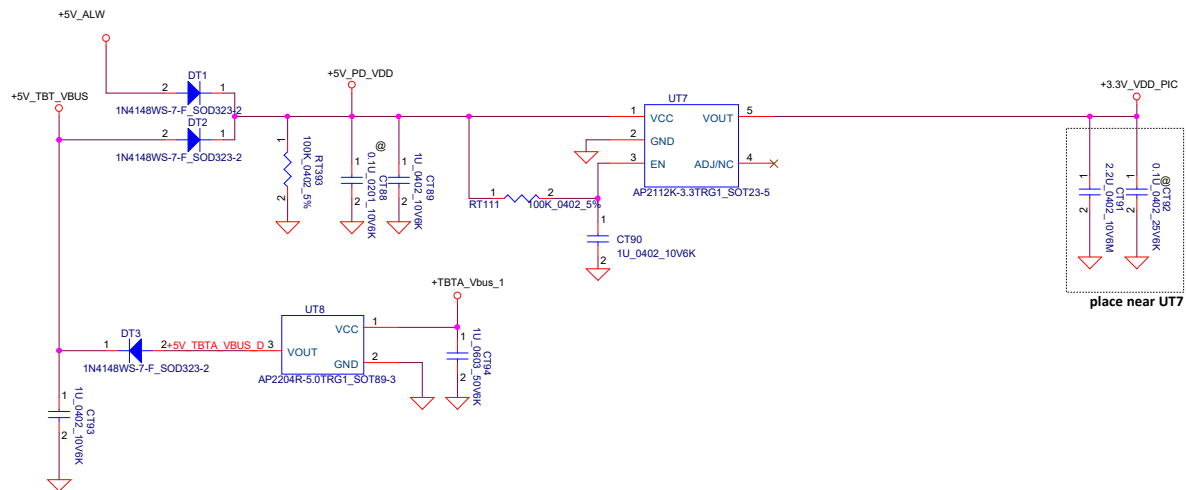
LA-F391P

Rev 0.2

Date: Friday, August 17, 2018

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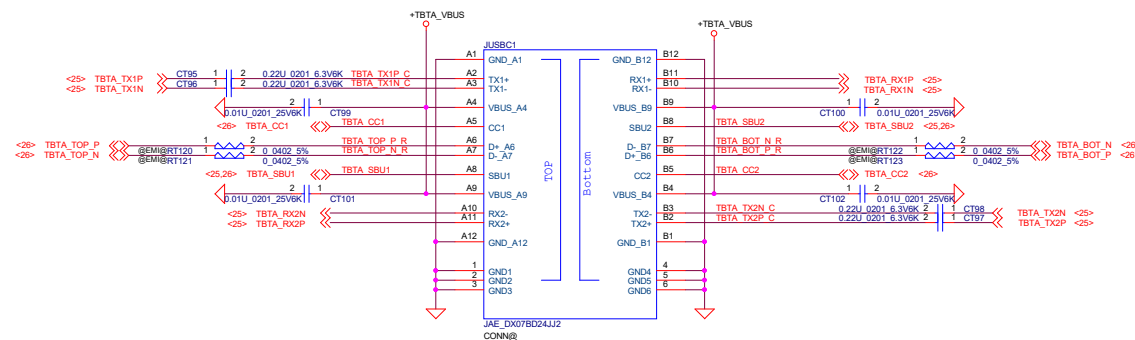
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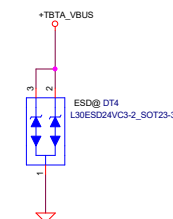
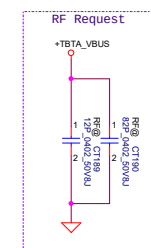
Compal Electronics, Inc.

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Size	Document Number	LA-F401P	Rev 0.2
Date:	Friday, August 17, 2018	Sheet 27 of 89	

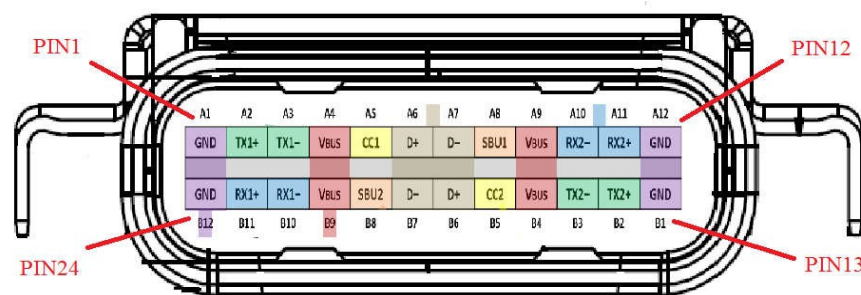
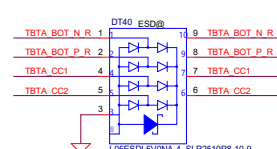
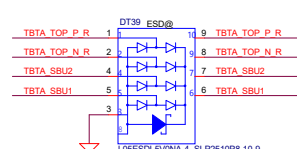
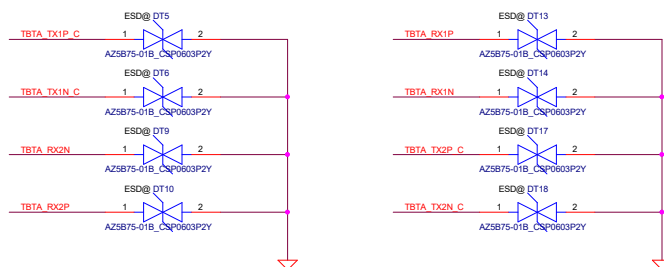


DX07BD24JJ2 LINK DONE

Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B



DT5, DT6, DT9, DT10, DT13, DT14, DT17,DT18,  
change CPN from SC40000AT00 to SC40000DF00 06/07/2017



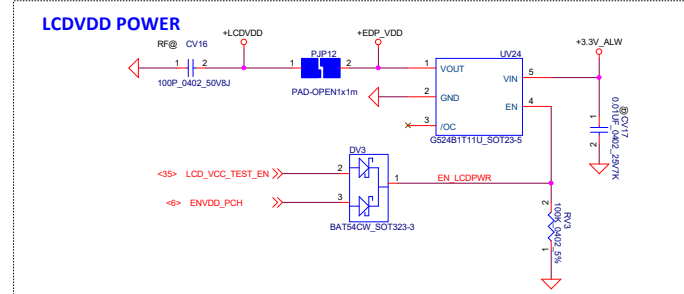
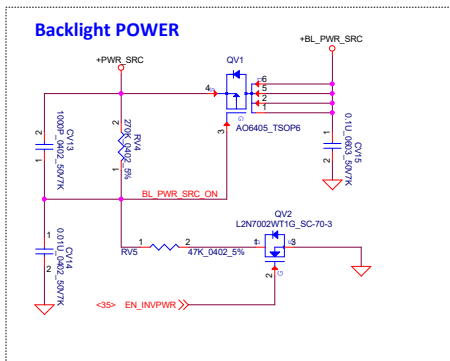
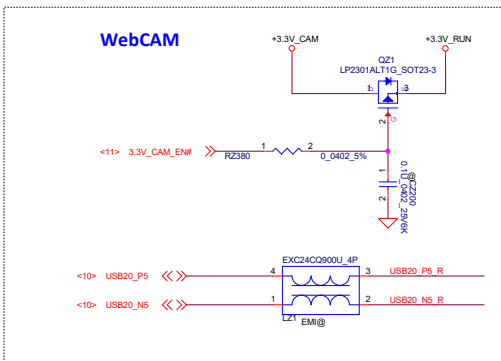
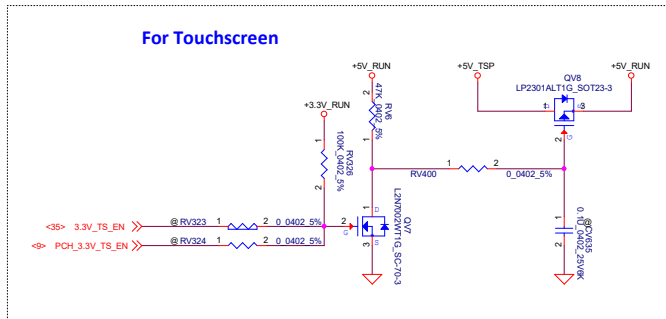
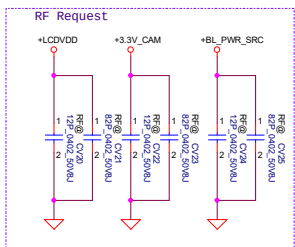
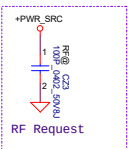
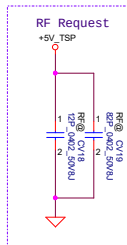
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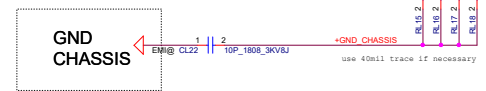
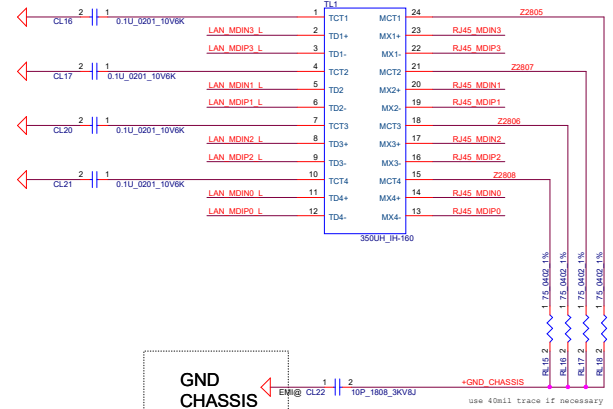
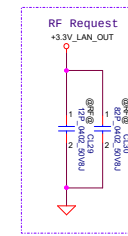
**Compal Electronics, Inc.**

Title	USB 3.0 CONN TYPE C
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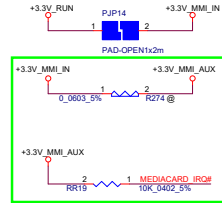
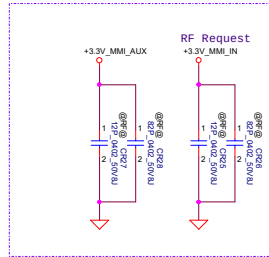
Size	Document Number	Rev
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	<b>Compal Electronics, Inc.</b>			
	Title			
	<b>eDP CONN &amp; Touch screen</b>			
	Size	Document Number	Rev	
	<b>LA-F401P</b>	<b>0.2</b>		
Date:	Friday, August 17, 2018	Sheet	20 of 60	

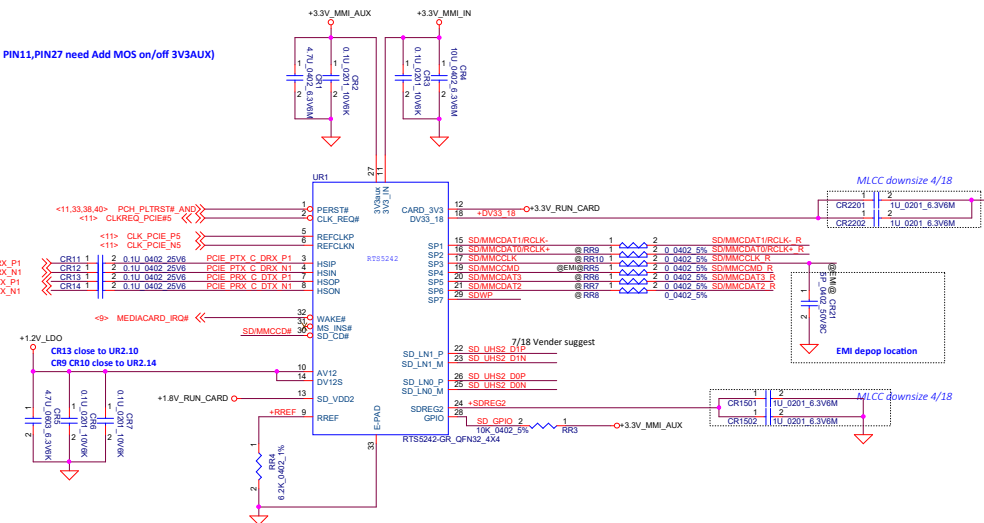


# For PCIE Interface

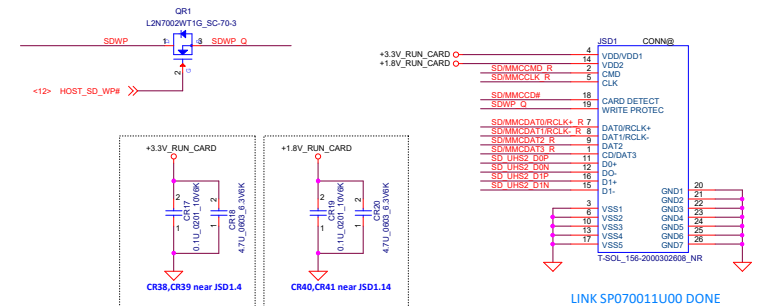


support D3 Hot(if D3 cold PIN11,PIN27 need Add MOS on/off 3V3AUX)

7/18 Vender suggest.



HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
High	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
Low	Low	High	Write Protect(FW LOCK)



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Card Reader RTS5242

LA-F401P

Rev 0.2

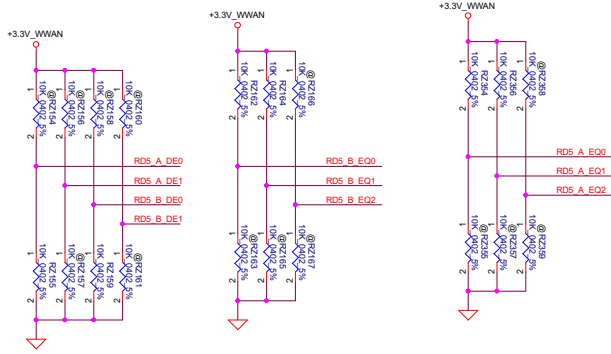
Friday, August 17, 2018

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# PCIE Repeater for 3042

Only for BR15U\_UMA&BR14U\_UMA



Programmable output de-emphasis level setting for channel A.  
A\_DE0: internally pulled up at ~150K;  
A\_DE1 internally pulled down at ~150K

[A\_DE1,A\_DE0] ==  
LL: -2dB  
HL: -7.5dB  
LH: -3.5dB (default)  
HH: -6dB

Programmable output de-emphasis level setting for channel B.  
B\_DE0: internally pulled up at ~150K;  
B\_DE1 internally pulled down at ~150K

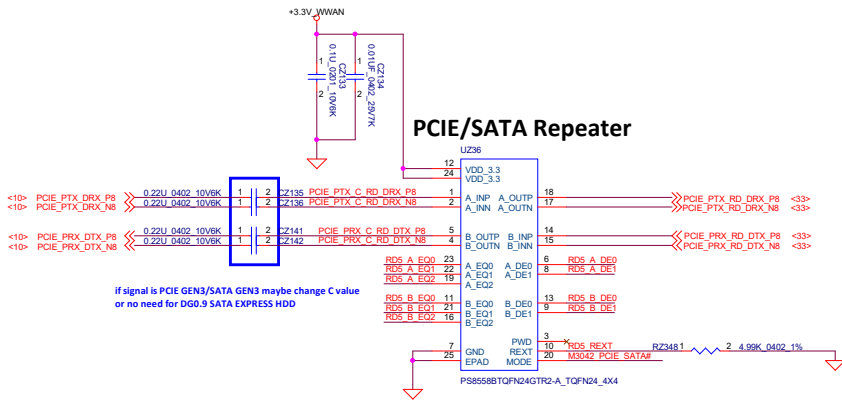
[B\_DE1,B\_DE0] ==  
LL: -2dB  
HL: -7.5dB  
LH: -3.5dB (default)  
HH: -6dB

Equalizer control and program for channel A.  
A\_EQ0, A\_EQ1 and A\_EQ2: internally pulled down at ~150K

[A\_EQ2,A\_EQ1,A\_EQ0] ==  
LLL: For channel loss up to 17dB (default)  
LHL: For channel loss up to 14dB  
HLL: For channel loss up to 19dB  
HHL: For channel loss up to 21dB  
LHH: For channel loss up to 18dB  
LHH: For channel loss up to 10dB  
HHH: For channel loss up to 20dB

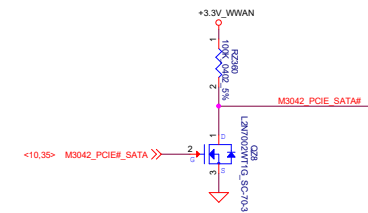
Equalizer control and program for channel B.  
B\_EQ0, B\_EQ1 and B\_EQ2: internally pulled down at ~150K

[B\_EQ2,B\_EQ1,B\_EQ0] ==  
LLL: For channel loss up to 17dB (default)  
LHL: For channel loss up to 14dB  
HLL: For channel loss up to 19dB  
HHL: For channel loss up to 21dB  
LHH: For channel loss up to 18dB  
LHH: For channel loss up to 10dB  
HHH: For channel loss up to 20dB



If signal is PCIE GEN3/SATA GEN3 maybe change C value  
or no need for DQ0.9 SATA EXPRESS HDD

M3042_PCIE_SATA#	DEVICE interface
0	SATA
1	PCIE



## SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>

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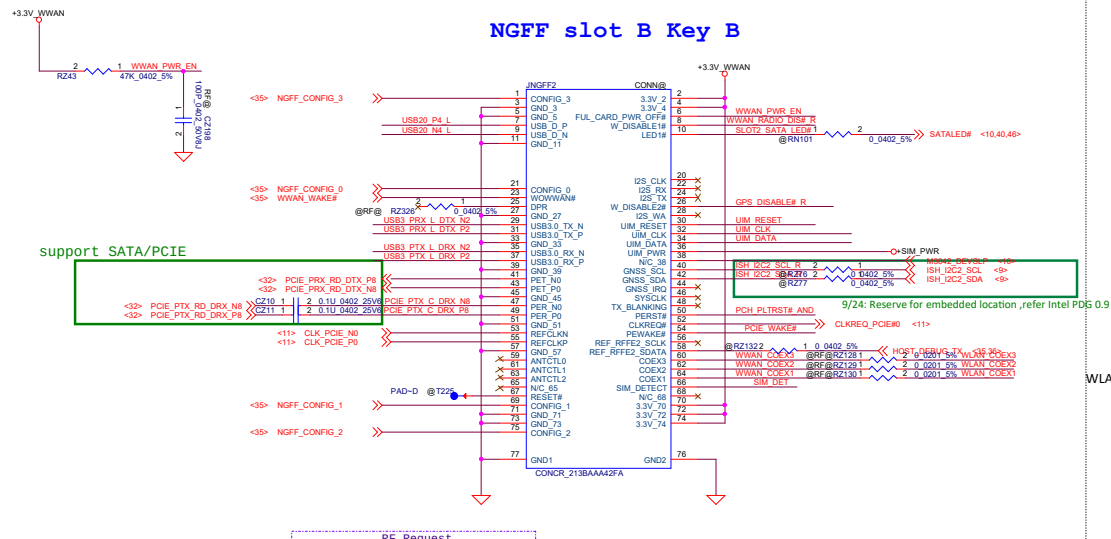
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File	PCIE REPEATER for M.2 3042
Size	Document Number LA-F401P
Date	Friday, August 17, 2018
Sheet	32 of 66

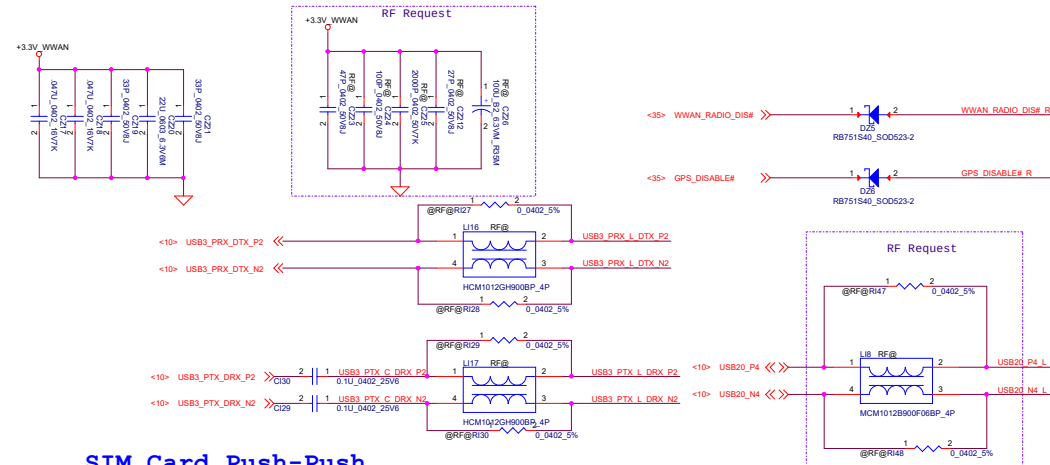
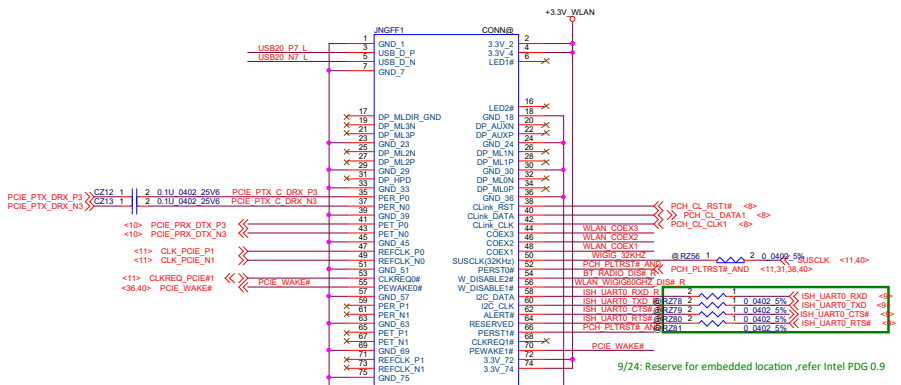


for no AR, Breckenridge 12/14/15 UMA/Steamboat

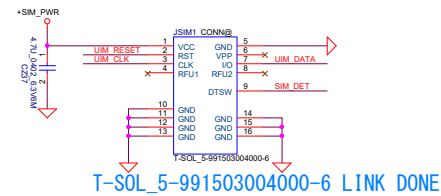
NGFF slot B Key B



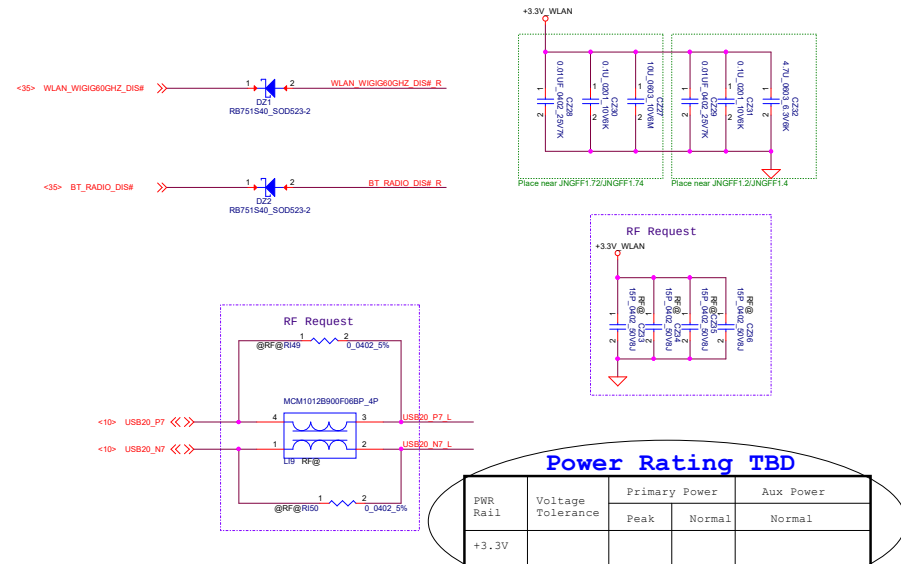
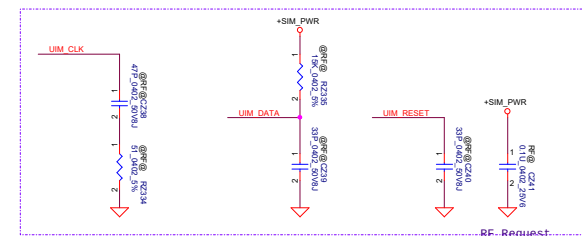
NGFF slot A Key A



## SIM Card Push-Push



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M3042_PCIE#_SATA
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low



## Power Rating TBD

	PWR Rail	Voltage Tolerance	Primary Power		Aux Power
			Peak	Normal	Normal
	+3.3V				

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**Compal Electronics, Inc.**

### NGFF Card

LA-F401P

Date: Friday, August 17, 2018

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Sheet

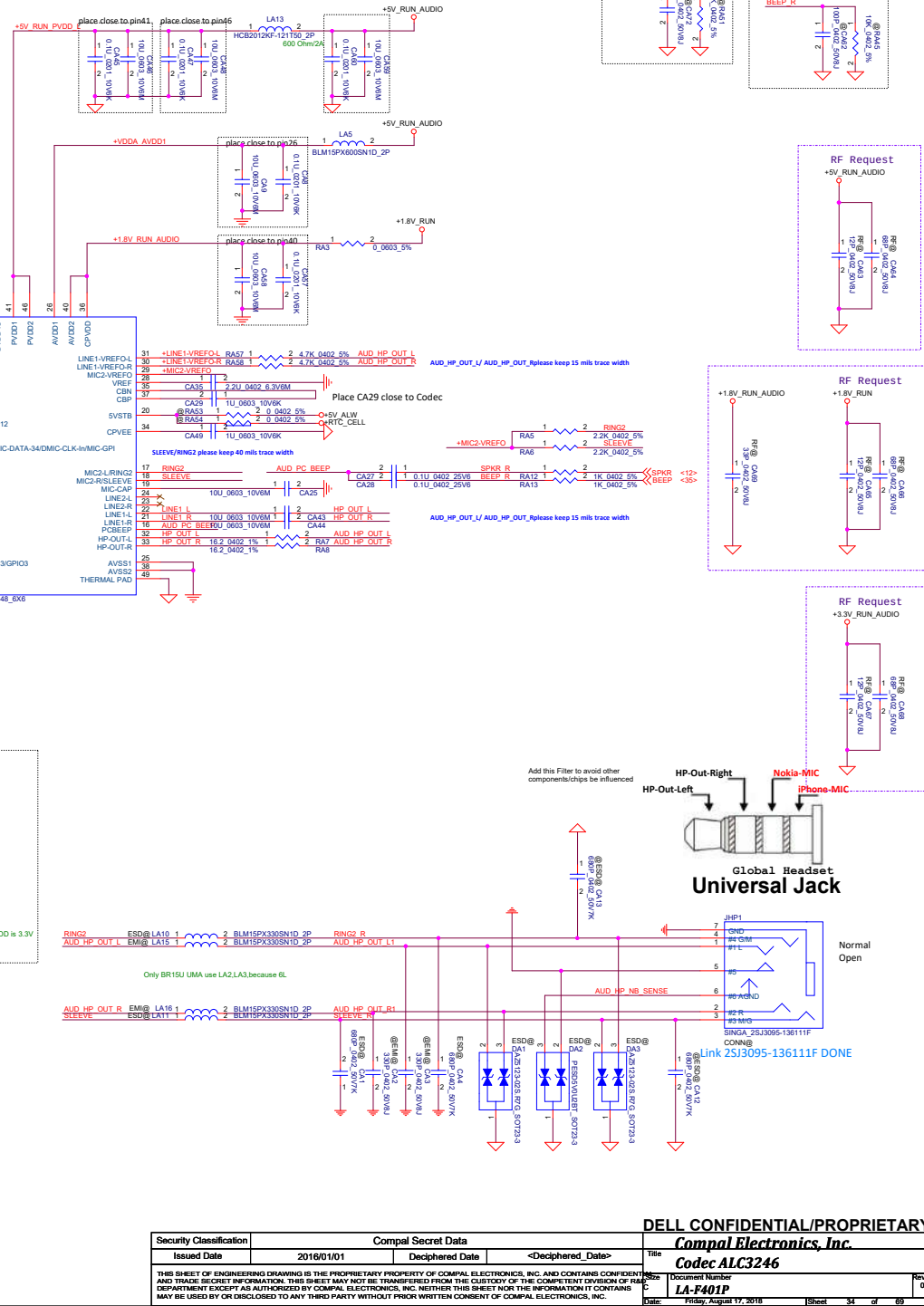
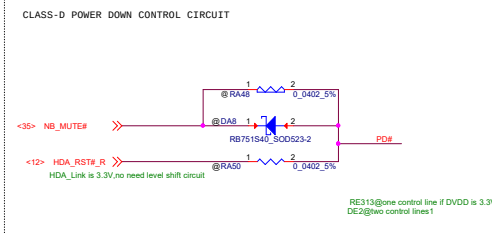
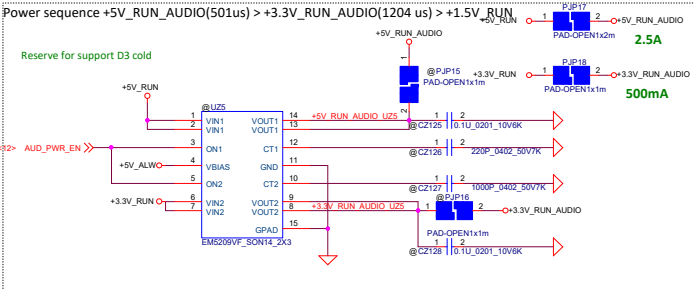
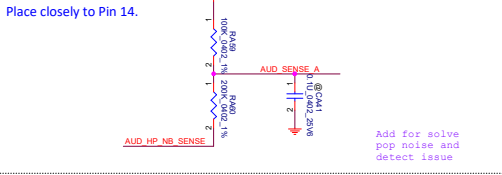
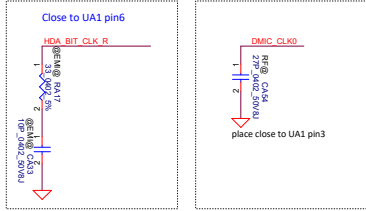
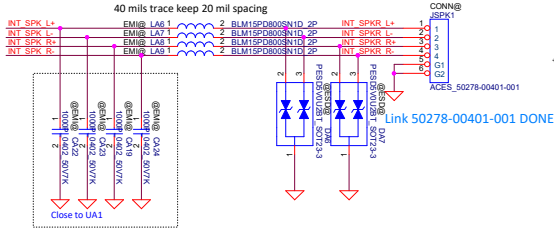
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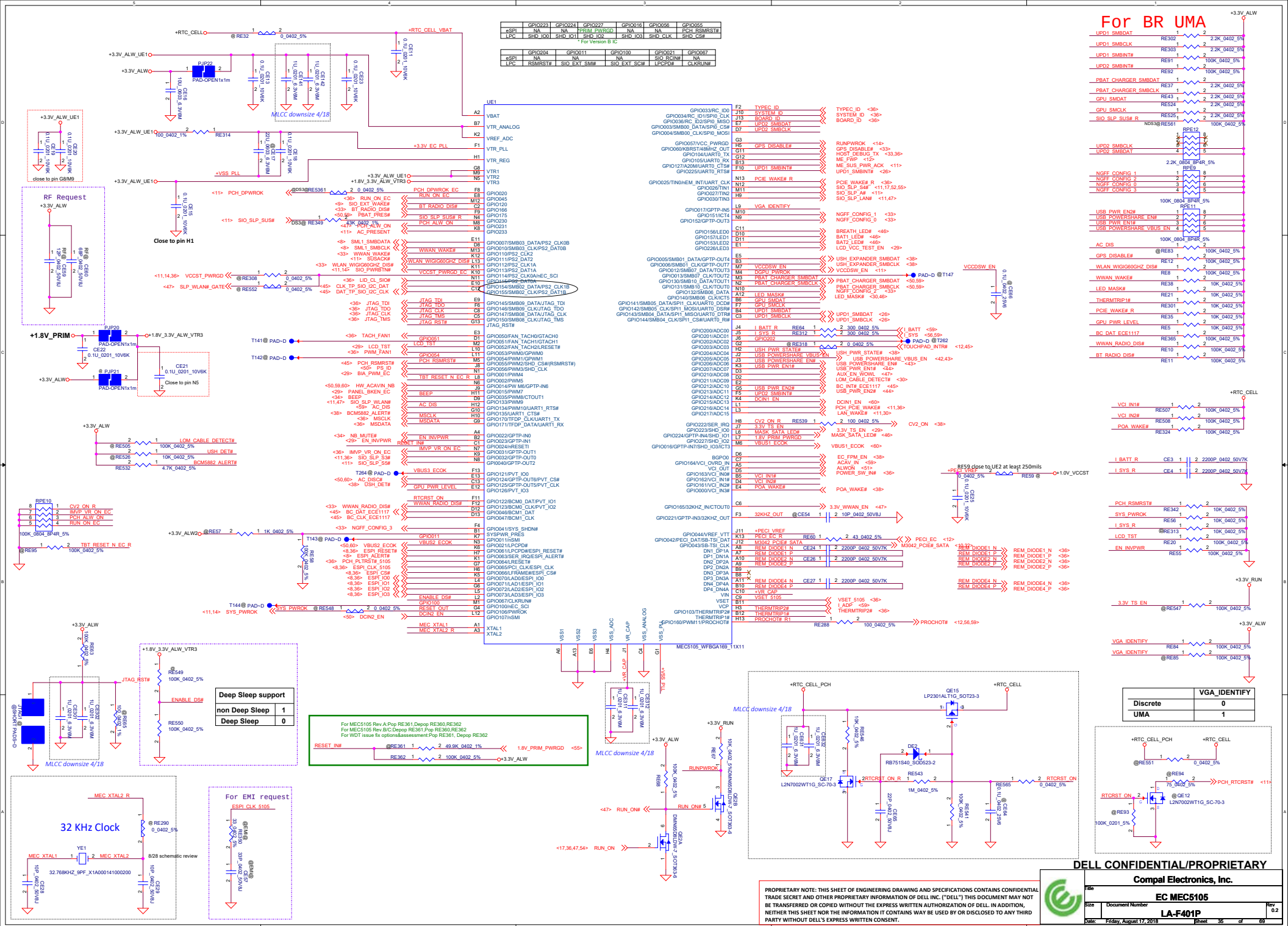
1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

## Internal Speakers Header

40 mils trace keep 20 mil spacing



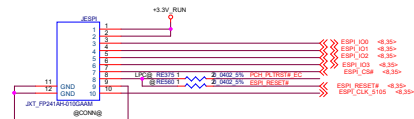
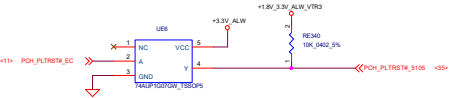
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Issued Date		Deciphered Date		<Deciphered Date>	
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Compal Electronics, Inc.	
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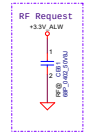
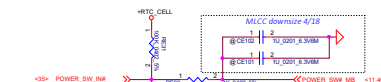
6/8 Change to SA00007WE00 DII



JXT\_FP241AH-010GAAM LINK DONE

LPC BBPort Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_I00
4	LPC_LAD1	ESPI_I01
5	LPC_LAD2	ESPI_I02
6	LPC_LAD3	ESPI_I03
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	



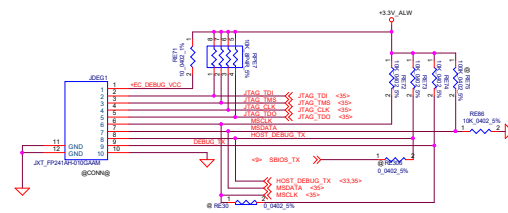
For WHEA BSOD issue respin,  
board ID change to A01(RE79=240K) 8/17

RE343	CE62	REV
* 240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	
2K	4700p	
1K	4700p	

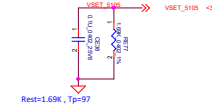
RE79	CE40	REV
* 240K	4700p	A02
130K	4700p	
62K	4700p	
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

RE300	CE47	PANEL SIZE
* 240K	4700p	11"
130K	4700p	12"
62K	4700p	13"
* 33K	4700p	14"
8.2K	4700p	15"
4.3K	4700p	17"
2K	4700p	18P
1K	4700p	

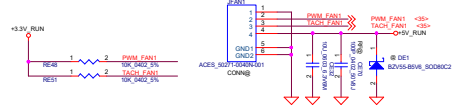
PD ACE DET# rise time is measured from 5%~68%. BOARD\_ID rise time is measured from 5%~68%. SYSTEM\_ID rise time is measured from 5%~68%.



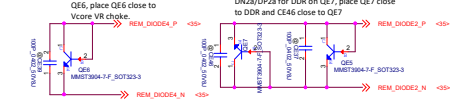
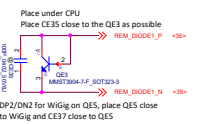
JXT\_FP241AH-010GAAM LINK DONE



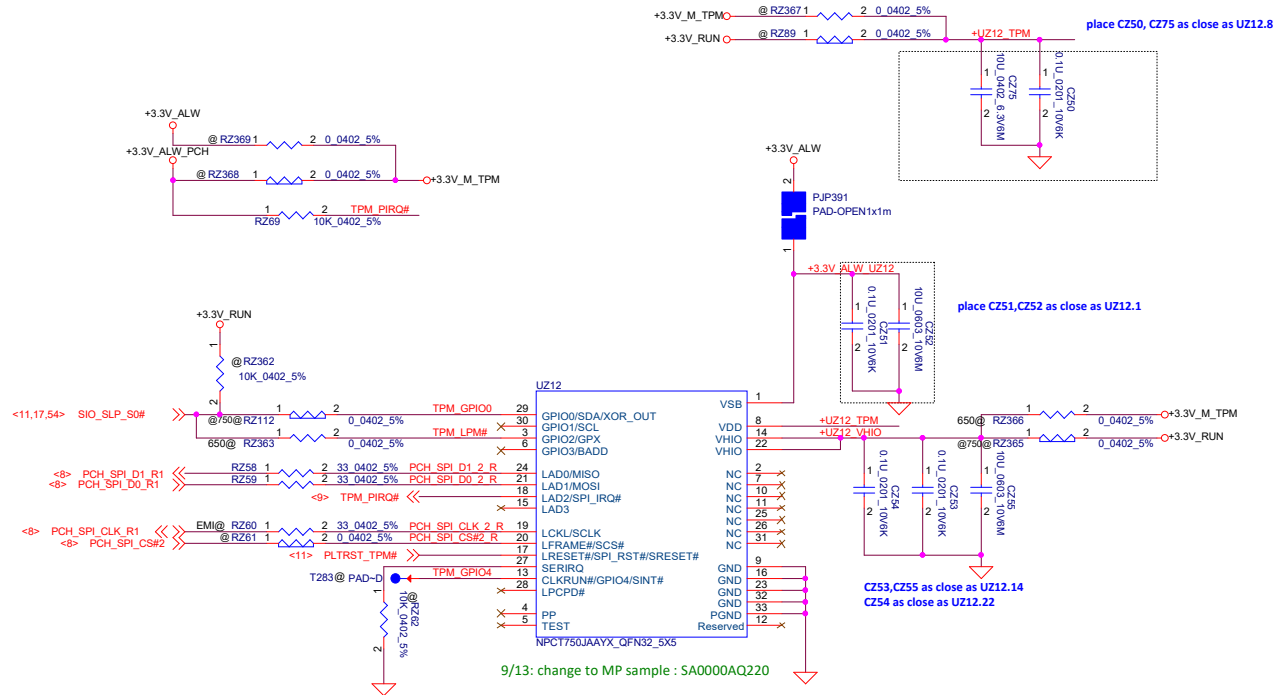
Link S0271-0040N-001 DONE



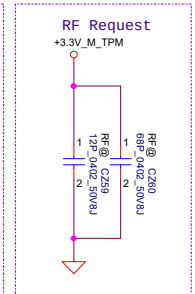
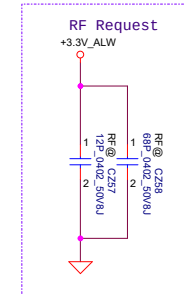
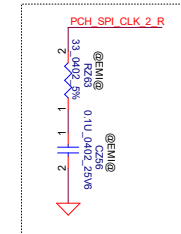
5085 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DN2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)



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	Pop	Depop	Comment
NPCT65x	RZ89, RZ366, RZ62, RZ363	RZ365, RZ367, RZ112	VDD - V_RUN Power VHIO - V_SPI Power
NPCT75x	RZ89, RZ365, RZ112	RZ367, RZ366, RZ62, RZ363	Option1 (recommended) VDD and VHIO - V_RUN power
NPCT75x	RZ367, RZ366	RZ89, RZ365, RZ62	Option2 (for Z1 sample [early sample]) VDD and VHIO - V_SPI power

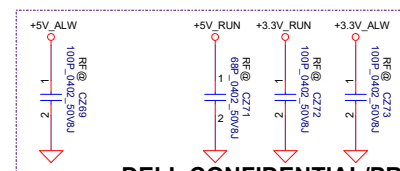
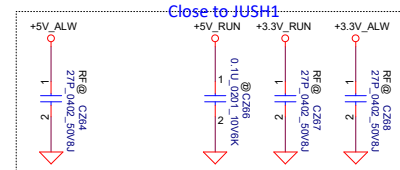
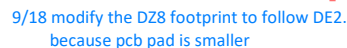


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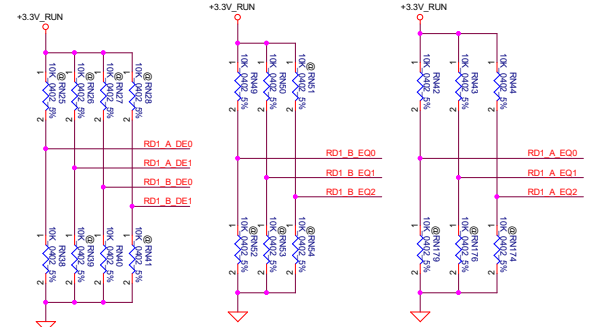


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<b>USH &amp; TPM</b>			
<b>Size</b>	<b>Document Number</b>	<b>Rev</b>	
	<b>LA-F401P</b>	0.2	
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# For Parade 2 Lane solution

	PCIE/SATA Redriver for 2280
Brekenridge12	Need
Brekenridge14U UMA	Need
Brekenridge14U DSC	Need
Brekenridge15U UMA	Need
Brekenridge15U DSC	Need
Steamboat12	No need
Steamboat14	Need
Kirkwood12&13	Check

PWD	Funtion
0	Normal mode(default)
1	power down mode



Programmable output de-emphasis level setting for channel A.  
A\_DE0: internally pulled up at ~150K;  
A\_DE1 internally pulled down at ~150K

[A\_DE1, A\_DE0] ==  
LL: -2dB  
HL: -7.5dB  
LH: -3.5dB (default)  
HH: -6dB

Programmable output de-emphasis level setting for channel B.  
B\_DE0: internally pulled up at ~150K;  
B\_DE1 internally pulled down at ~150K

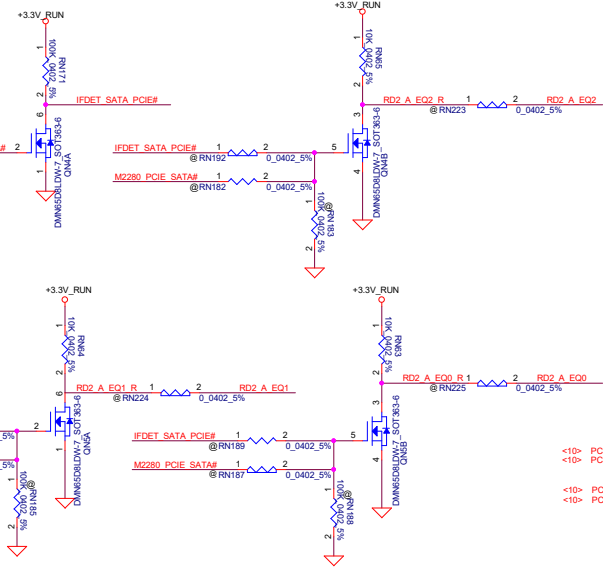
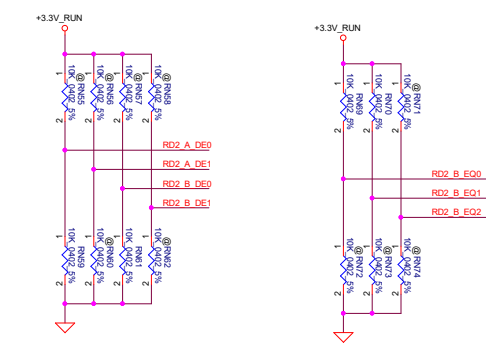
[B\_DE1, B\_DE0] ==  
LL: -2dB  
HL: -7.5dB  
LH: -3.5dB (default)  
HH: -6dB

Equalizer control and program for channel A.  
A\_EQ0, A\_EQ1 and A\_EQ2: internally pulled down at ~150K

[A\_EQ2, A\_EQ1, A\_EQ0] ==  
LLL: For channel loss up to 17dB (default)  
LHL: For channel loss up to 14dB  
HLL: For channel loss up to 19dB  
HLH: For channel loss up to 18dB  
LHH: For channel loss up to 10dB

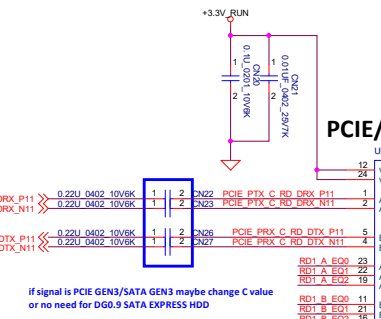
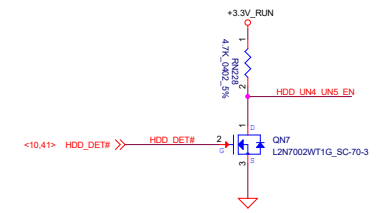
Equalizer control and program for channel B.  
B\_EQ0, B\_EQ1 and B\_EQ2: internally pulled down at ~150K

[B\_EQ2, B\_EQ1, B\_EQ0] ==  
LLL: For channel loss up to 17dB (default)  
LHL: For channel loss up to 14dB  
HLL: For channel loss up to 19dB  
HLH: For channel loss up to 18dB  
LHH: For channel loss up to 10dB



SATA / PCI Express\* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF <sup>2</sup>	None	None <sup>3</sup>



PCIE/SATA Repeater

PCIE/SATA Repeater

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File: **SATA/PCIE REPEATER for M.2 2280**

Size: Document Number **LA-F401P**

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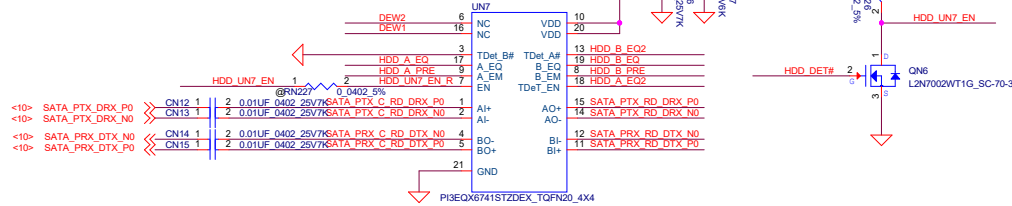






	pin 3	pin 6	pin 13	pin 16	pin 18
<b>Pericom</b>	TDet_B#	NC	TDet_A#	NC	TDet_EN
<b>TI</b>	GND	DEW2	GND	DEW1	GND
<b>Parade</b>	GND	REXT	B_EQ2	DEW	A_EQ2

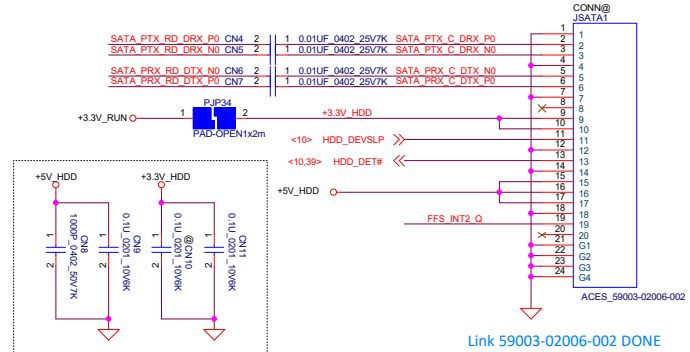
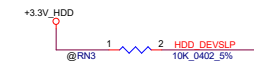
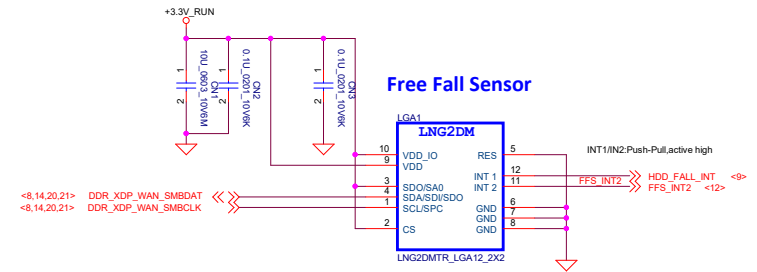
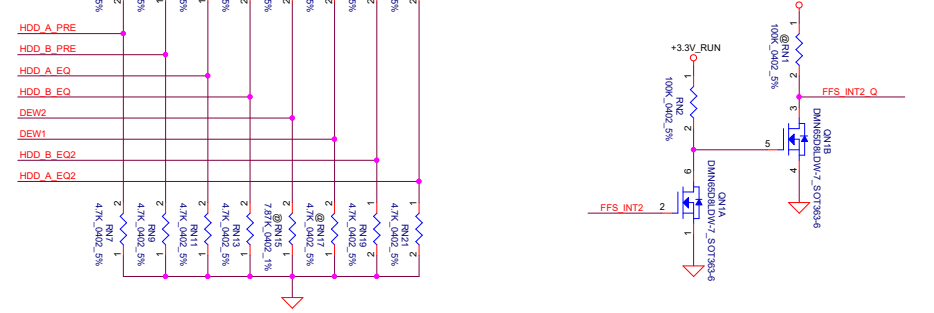
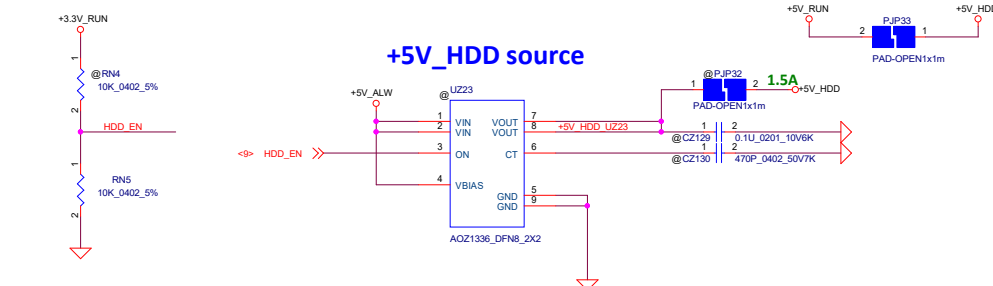
## SATA Repeater



	HDD_A_EQ2 PIN17	HDD_B_EQ2 PIN19	HDD_A_EQ2 PIN18	HDD_B_EQ2 PIN13	DEW1 PIN16	DEW2 PIN6	HDD_A_PRE PIN9	HDD_B_PRE PIN8
<b>Pericom PI3EQX6741ST</b>	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC	NC	PD (RN7)	PD (RN9)
<b>TI SN75LVCP601</b>	PD (RN11)	NC	PD (RN21)	PD (RN19)	NC (I PU)	NC (I PU)	PH (RN6)	PH (RN8)
<b>Parade PS8527C</b>	PD (RN11)	PD (RN13)	PD (RN21)	PD (RN19)	NC (1/2 VDD)	PD (RN15)	NC	NC (1/2 VDD)

			A_EQ	B_EQ		A_EM	B_EM
<b>Main</b>	<b>Pericom</b>	0 NC 1	3dB 6dB 9dB	3dB 6dB 9dB	0 NC 1	0dB 1.5dB	0dB 1.5dB
<b>2nd</b>	<b>TI</b>	0 NC 1	7dB 0dB 14dB	7dB 0dB 14dB	0 NC 1	0dB -4dB -2dB	0dB -4dB -2dB
<b>3rd</b>	<b>Parade</b>	EQ2 EQ1 (M = VDD/2) 0 M 0 0 0 1 M M M 0 M 1 1 M 1 0 1 1	A_EQ B_EQ 2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	B_EQ A_EQ 2.4dB 7.4dB 14.4dB 12.2dB 9.4dB 13.3dB 6.2dB 11.2dB 5dB	0 M 1 0 1 0 1 0 1 0 1	0dB -3.5dB -1.5dB	0dB -3.5dB -1.5dB

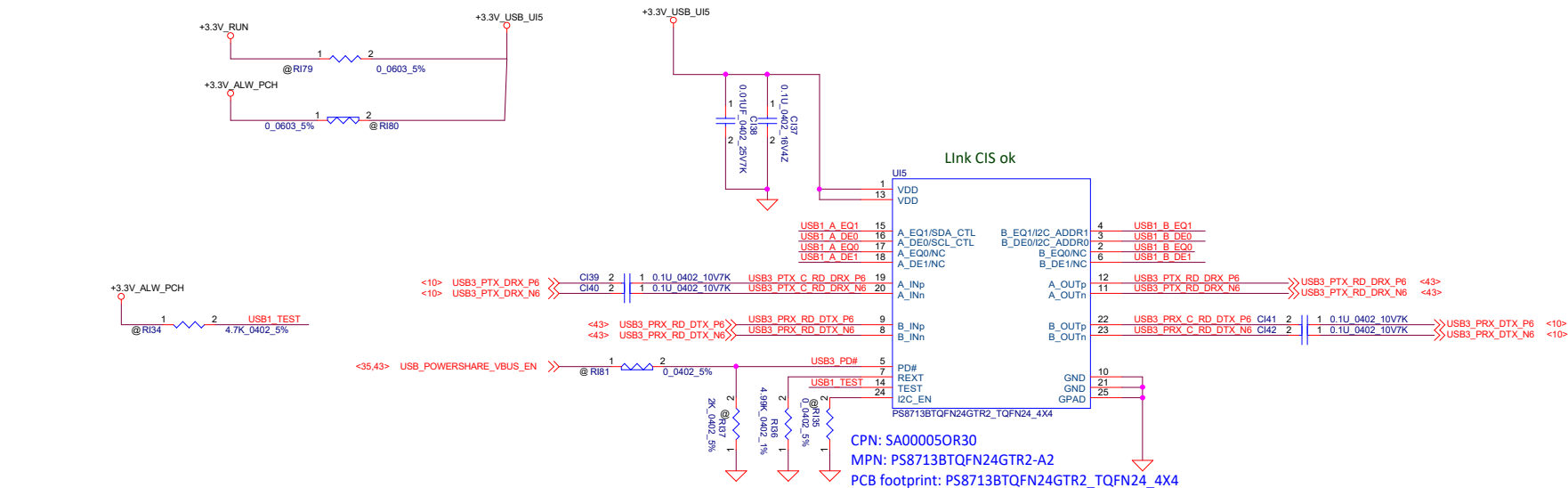
\* red color is current setting



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<b>Compal Electronics, Inc.</b>	
<b>SATA Repeater&amp;HDD CONN</b>	
<b>LA-F401P</b>	
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### Parade\_PS8713B

A_EQ1	A_EQ0	B_EQ1	B_EQ0	Recommended EQ
0	0	0	0	loss up to 9.5dB
0	1	0	1	loss up to 13dB
1	0	1	0	loss up to 4.5dB
1	1	1	1	loss up to 7.5dB

Both A\_EQ&B\_EQ have internal pull-down 150k

A_DE1	A_DE0	B_DE1	B_DE0	Recommended DE
0	0	0	0	3.5dB de-emphasis
0	1	0	1	No de-emphasis
1	0	1	0	2.7dB de-emphasis
1	1	1	1	5dB de-emphasis

Both A\_DE&B\_DE have internal pull-down 150k

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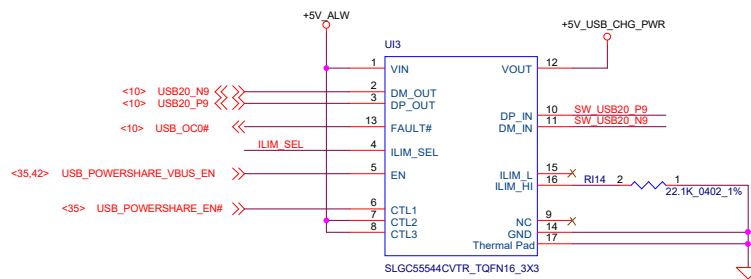
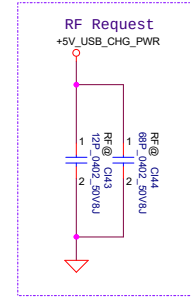
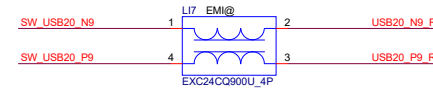
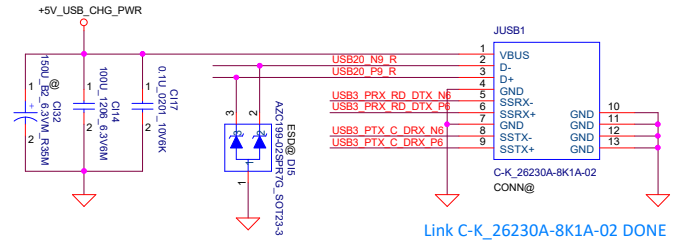
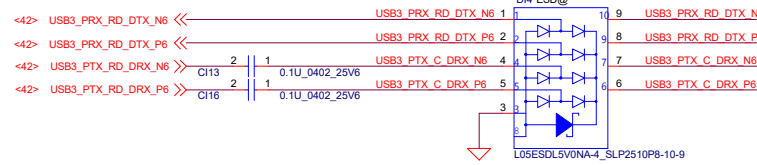
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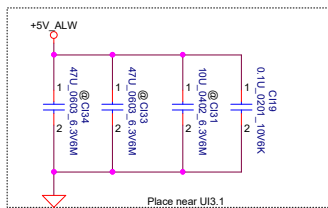
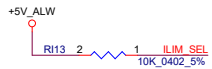


Title		Rev
USB3.0 Repeater		0.2
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For w/ Repeater



Link Seligro SA000097E10 Done  
MAIN: SLGC55544CVTR



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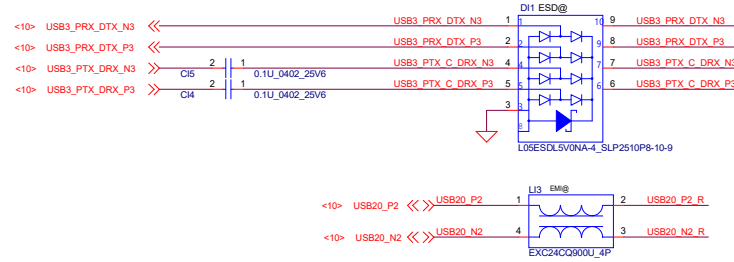
Compal Electronics, Inc.



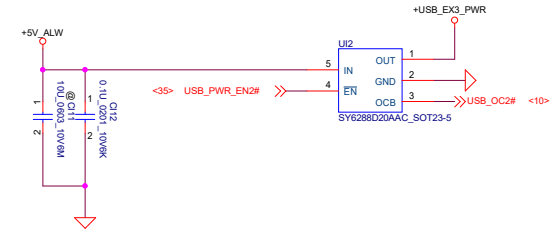
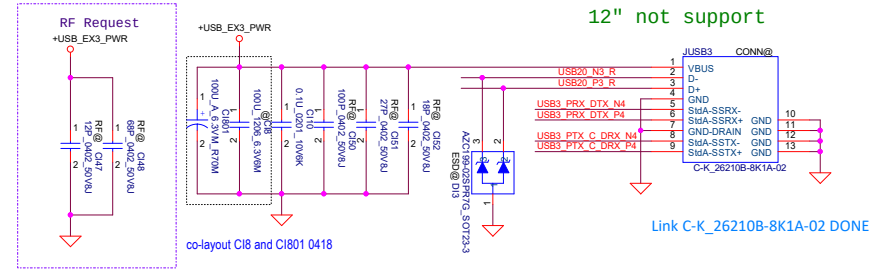
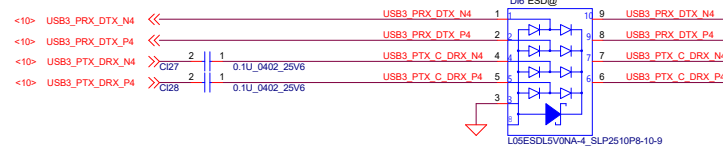
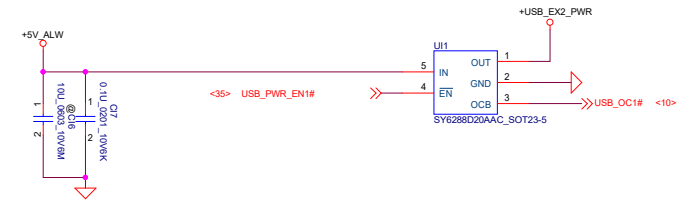
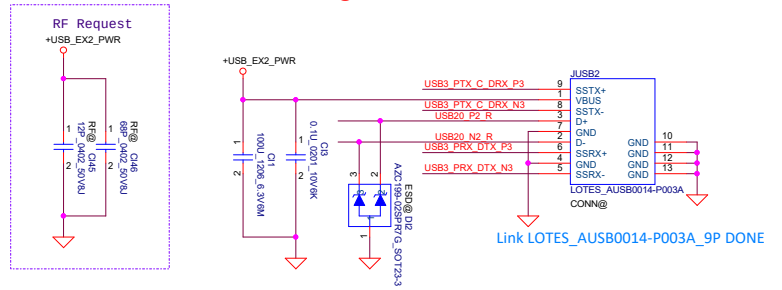
Title		JUSB1+PS	
Size	Document Number	LA-F401P	
Date:	Friday, August 17, 2018	Sheet	43 of 89

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# For Breckenridge 14&15/Steamboat 14



DfB request:  
 man SM070003200 (INPAQ\_MCM1012B900F068P\_4P)  
 Footprint use 2nd source SM070004400 (PANAS\_EXC24CQ000U\_4P)  
 Pitch change from 0.5mm to 0.55mm

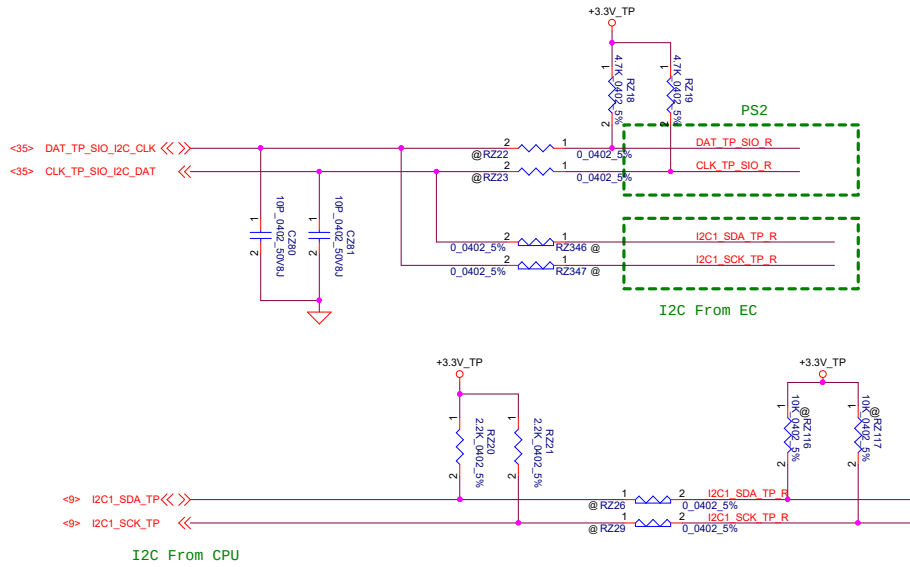


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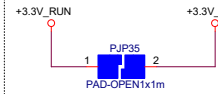
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JUSB2&JUSB3			
LA-F401P			
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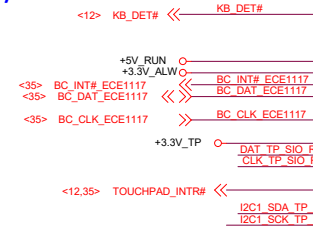
## Touch Pad



Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)  
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows  
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

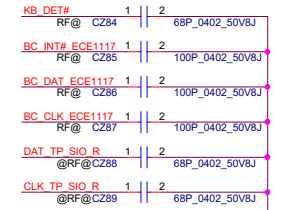


## Keyboard



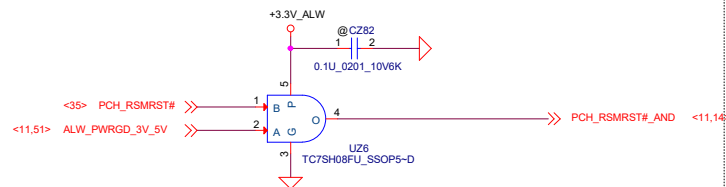
Link HRS\_TF49-20S-0P55SH done

## RF Request



Place close to JKBT1

## RSMRST circuit



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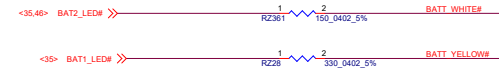
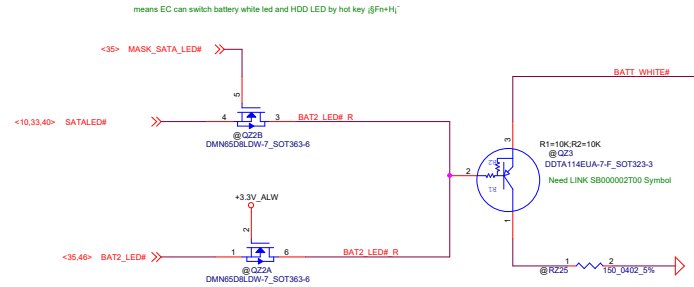
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Keyboard			
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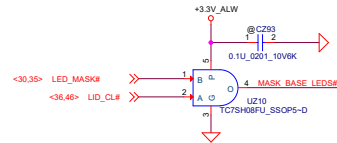
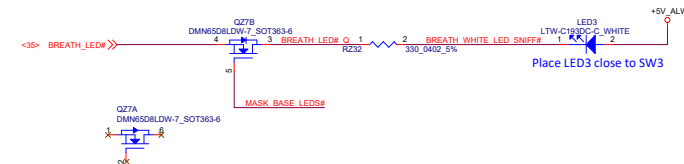
## Battery LED

### HDD LED MUX

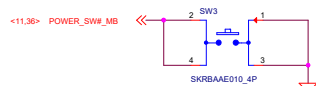


## Breath LED

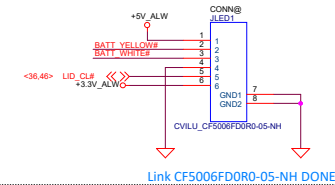
LED PIN change to SC55000FL00 from SC55000BA00



## POWER & INSTANT ON SWITCH



## LED board CONN

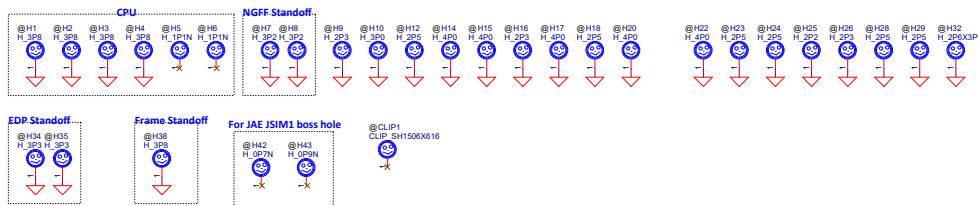


### Fiducial Mark



### LED Circuit Control Table

	LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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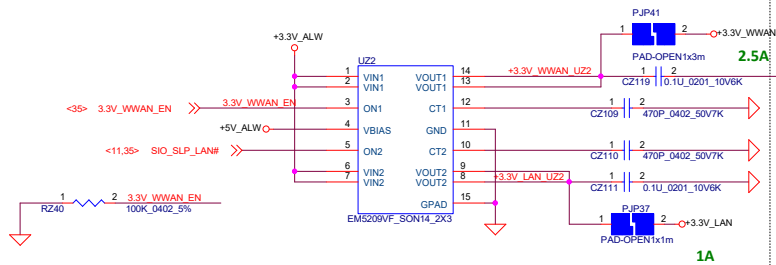
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PAD, LED

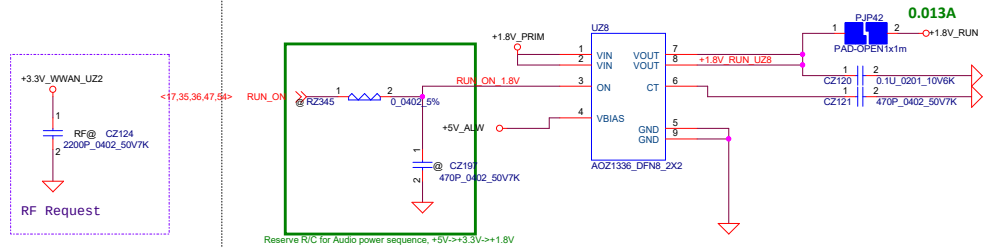
LA-F401P

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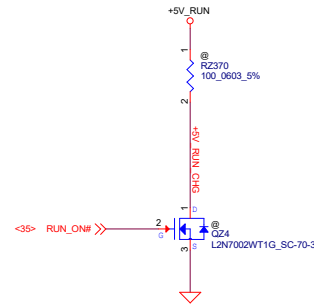
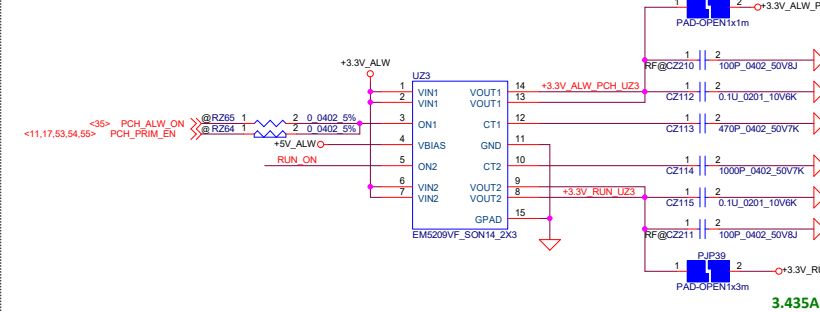
### +3.3V\_WWAN/+3.3V\_LAN source



### +1.8V\_RUN source

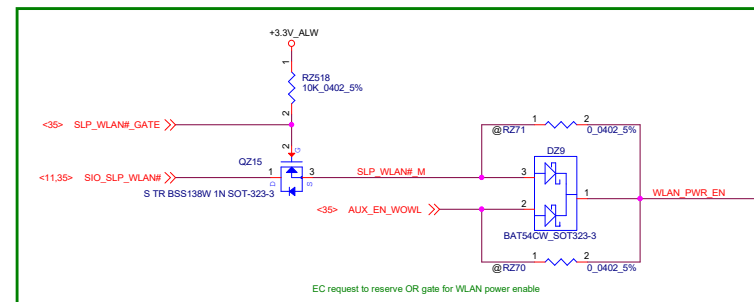
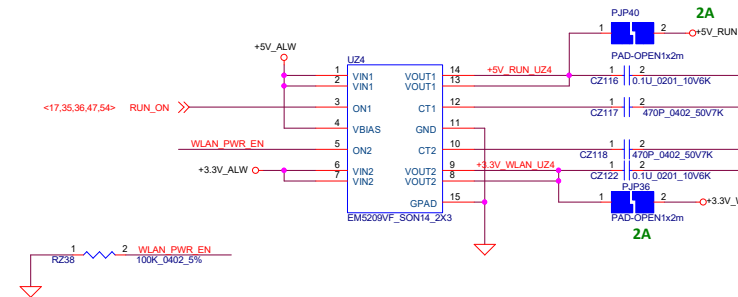


### +3.3V\_ALW\_PCH/+3.3V\_RUN source



Reserve for S3 no power issue (+5V\_RUN discharge circuit)

### +5V\_RUN/+3.3V\_WLAN source



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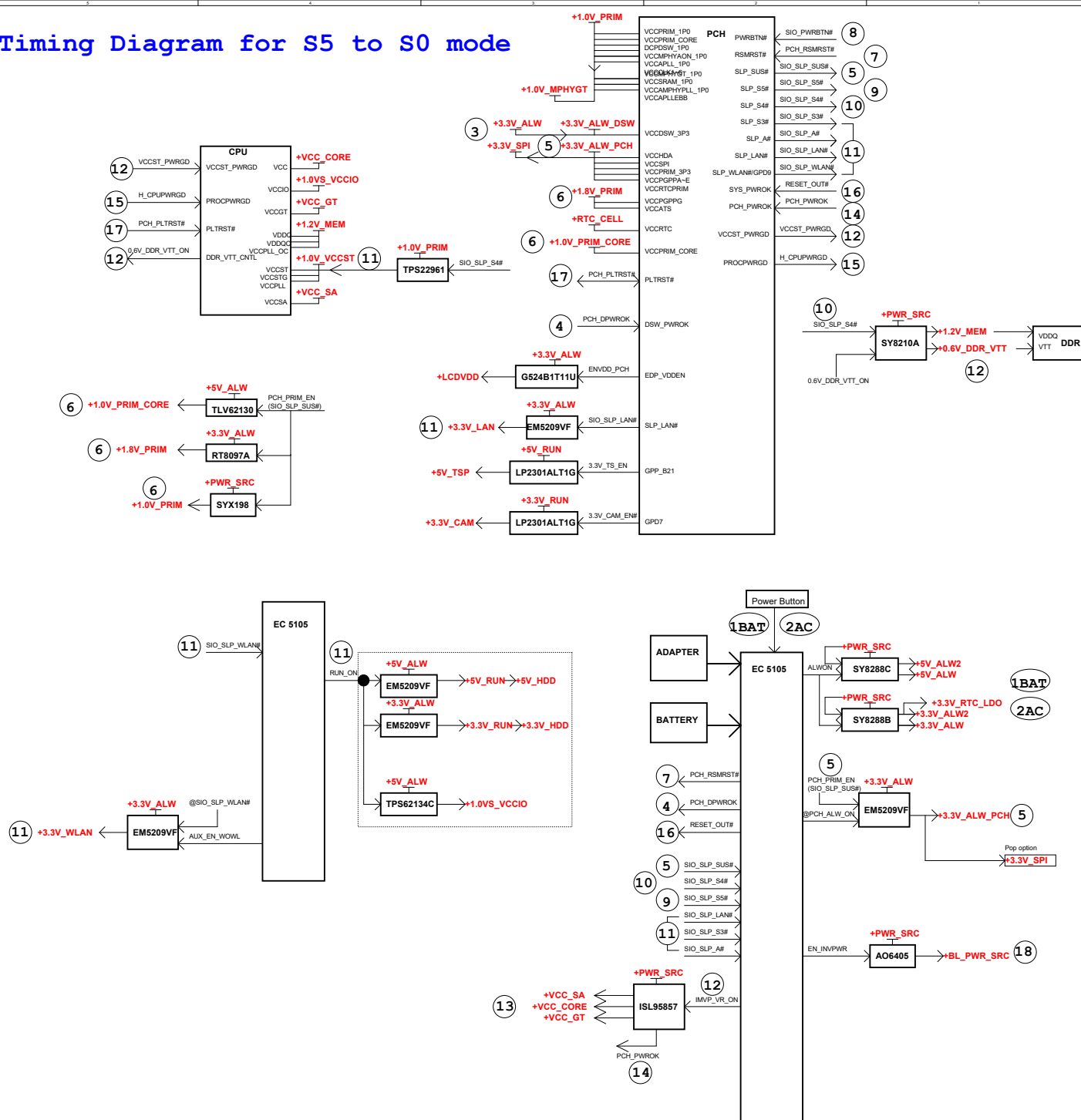
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Power control			
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### Timing Diagram for S5 to S0 mode



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5

4

3

2

1

D

D

1

C

C

B

B

A

A

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Compal Electronics, Inc.				
Title	Stack-up			
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5

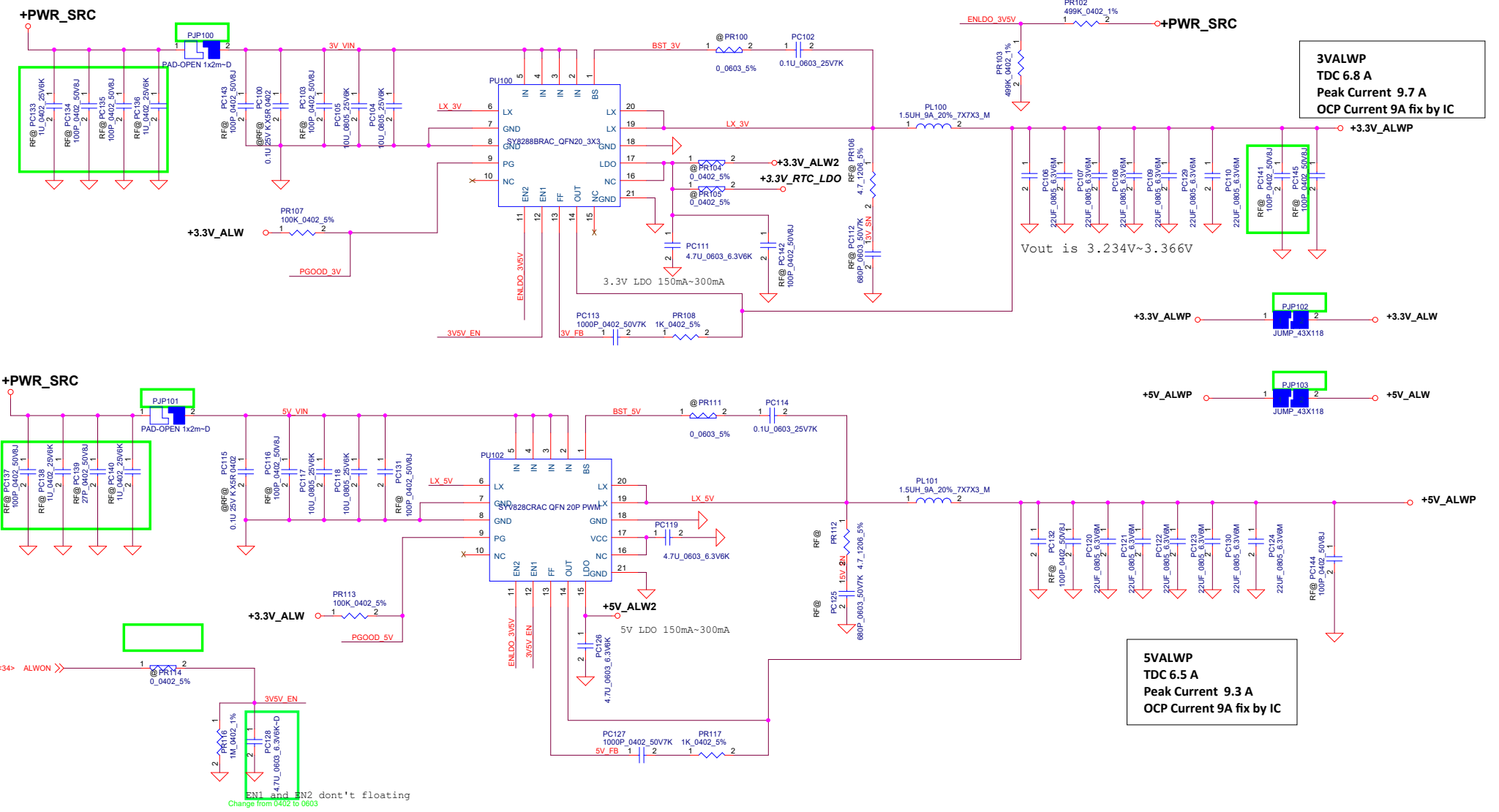
4

3


2

1





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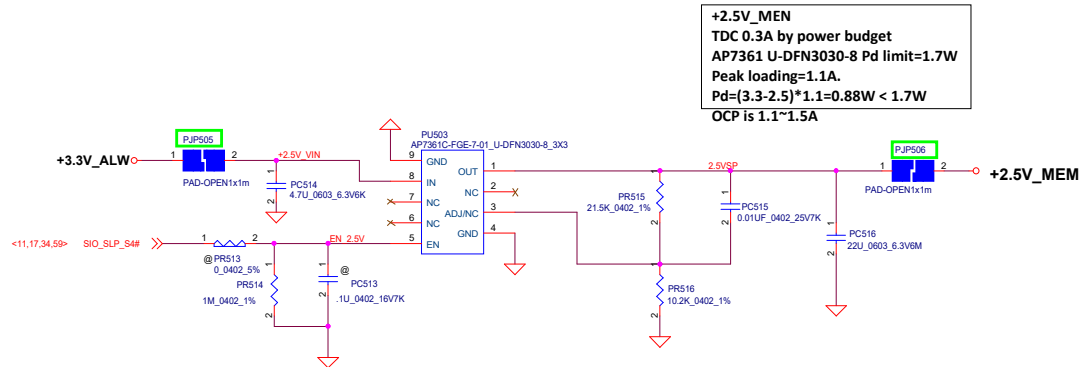
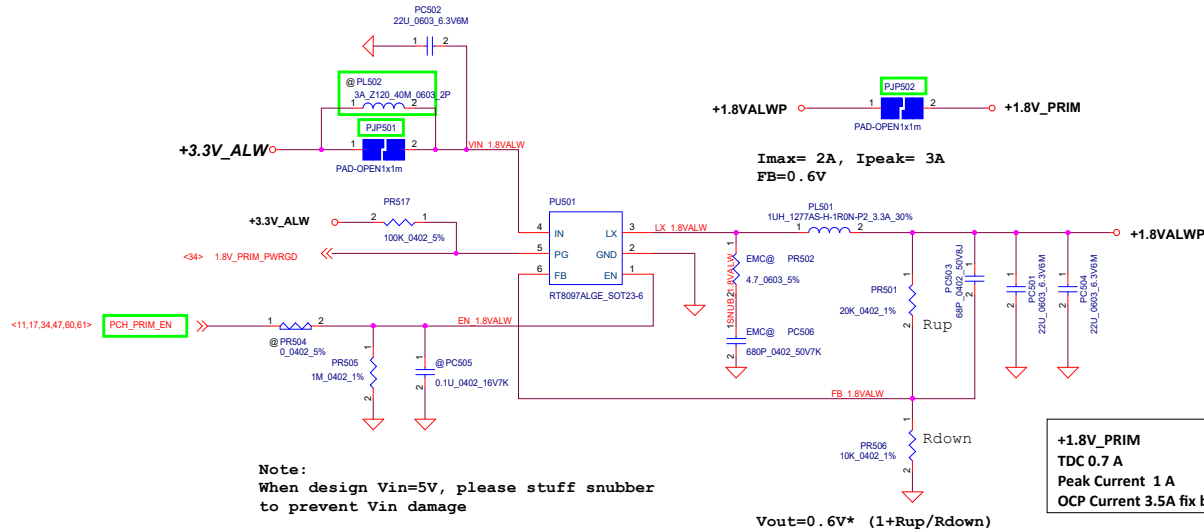
		Compal Electronics, Inc.	
		+5V_ALW/3.3V_ALW	
Size	Document Number	LA_F401	
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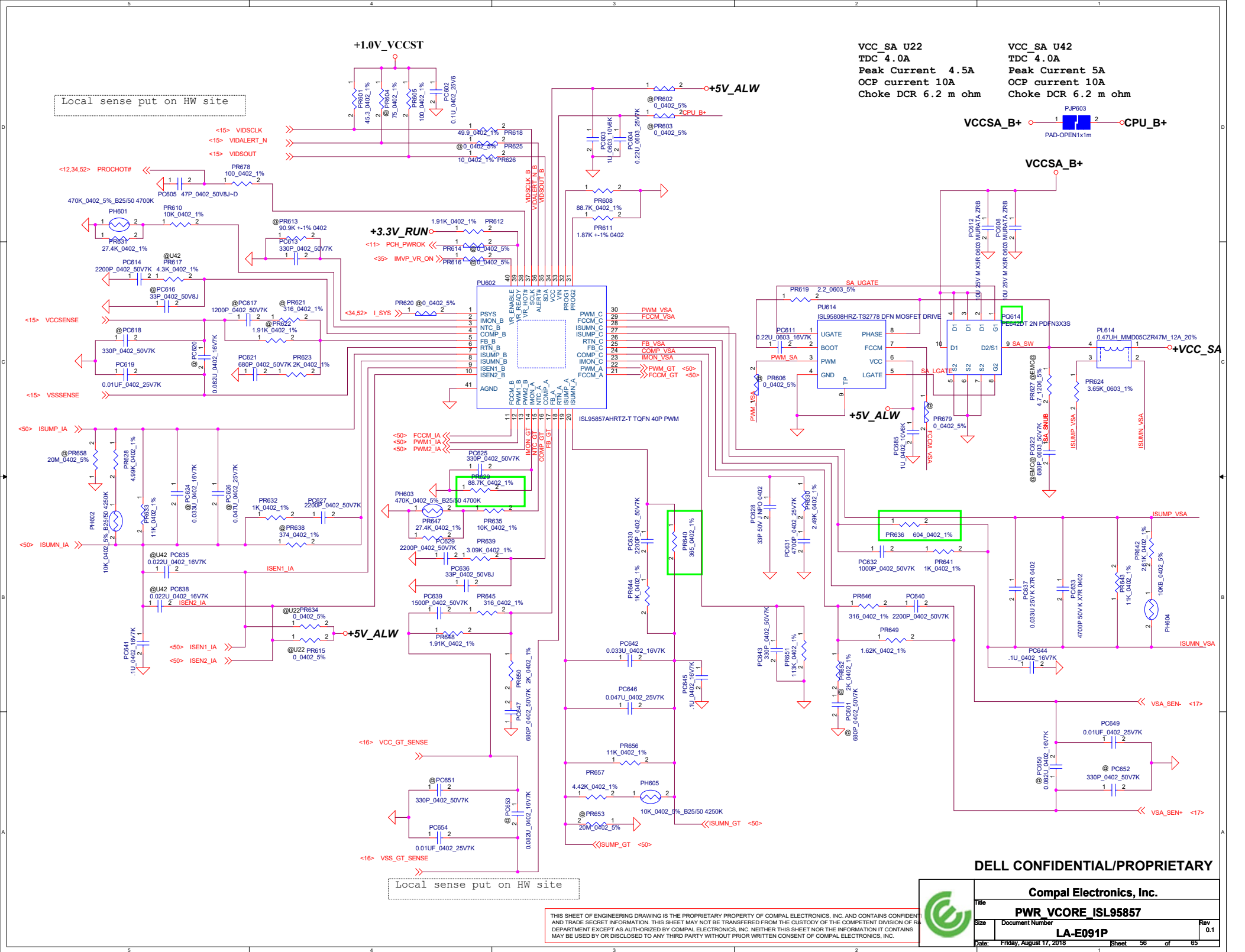


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File	+1.8VALWP/2.5V_MEM	
Size	Document Number	Rev 0.2
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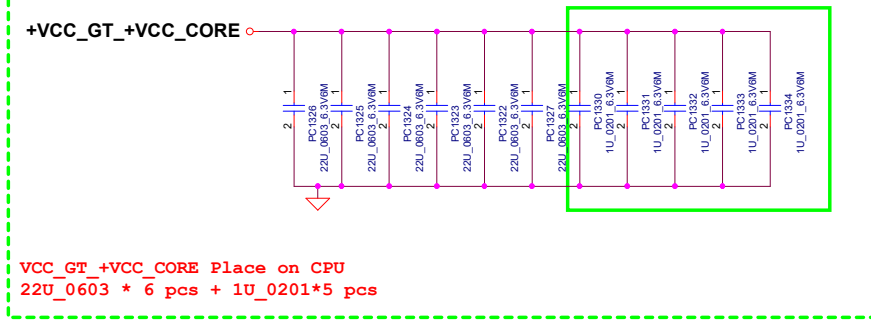
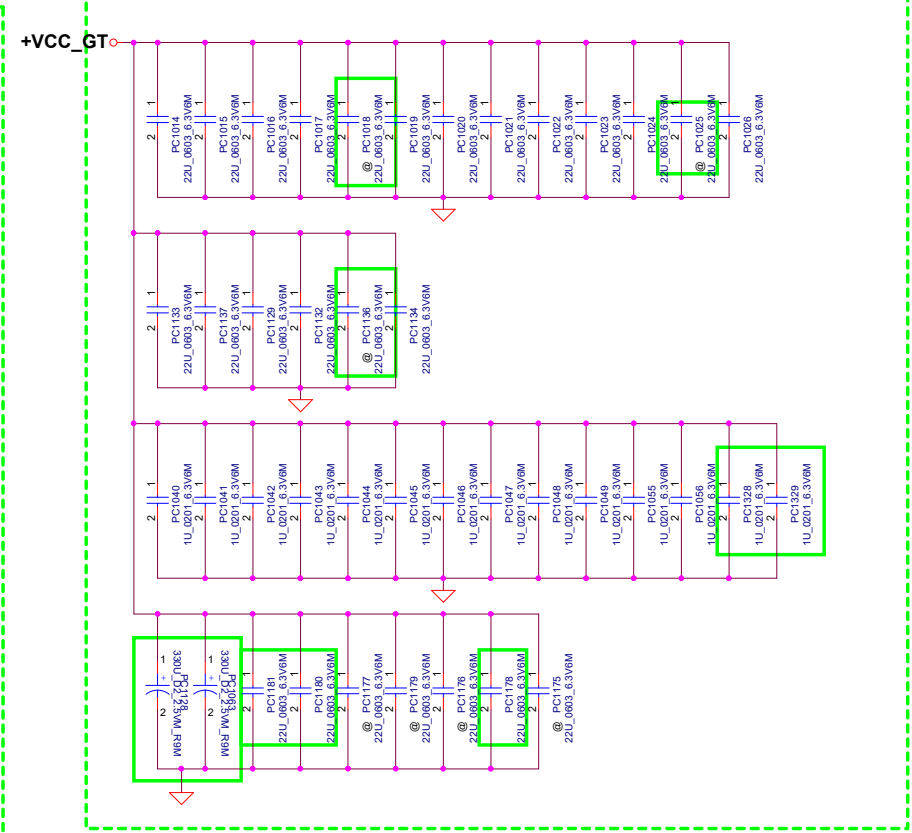
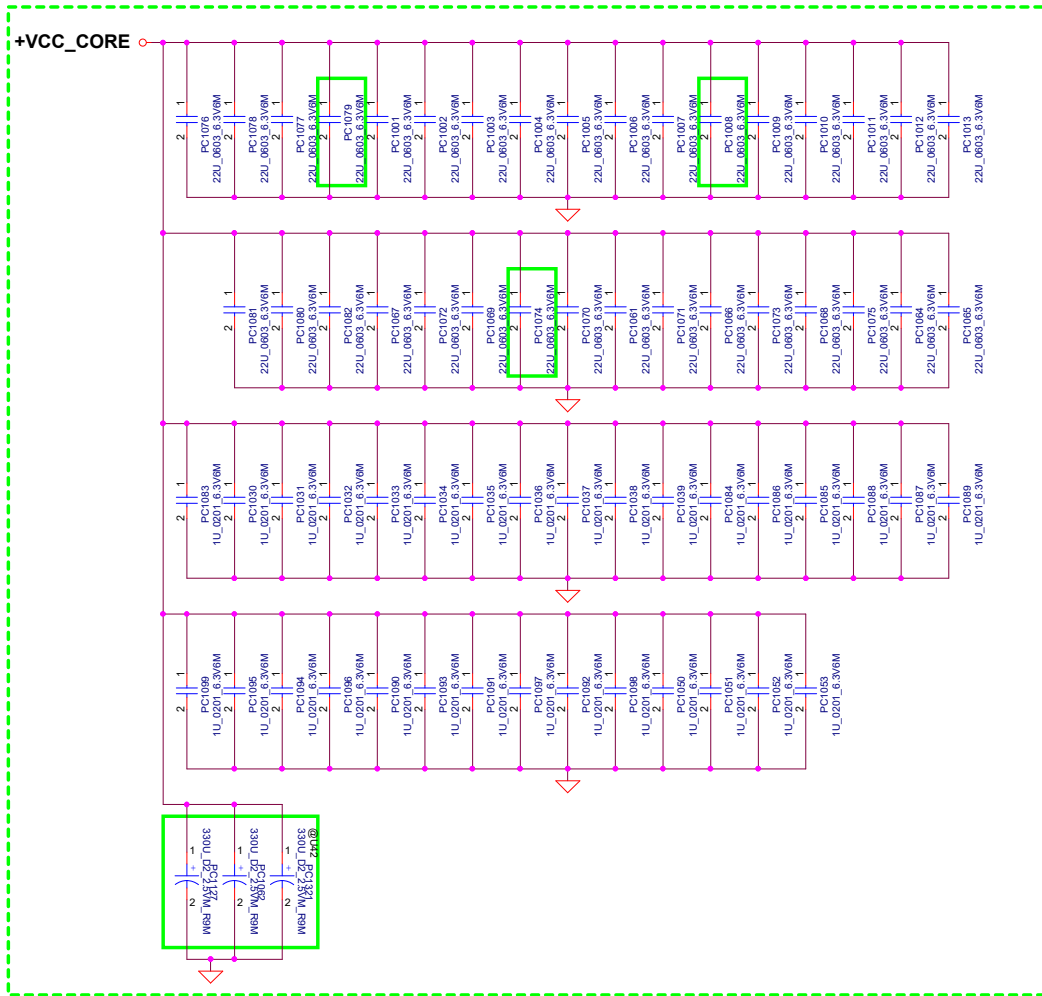




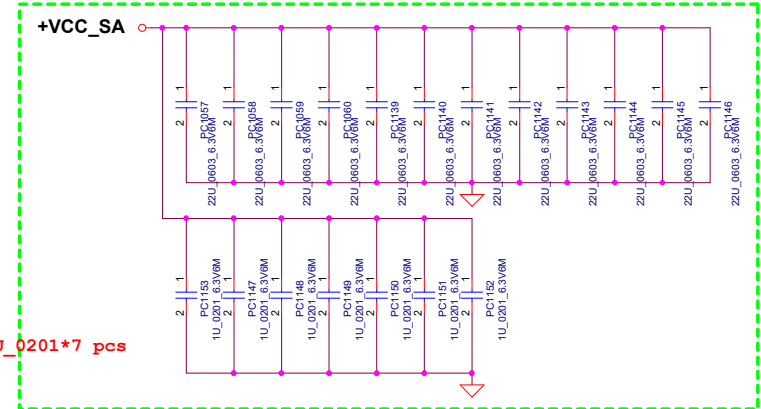


VCC\_CORE Place on CPU  
 22U\_0603 \* 33 pcs +1U\_0201\*31 pcs  
 +330u\_D7\*3 pcs

VCC\_GT Place on CPU (U22)  
 22U\_0603 \* 19 pcs +1U\_0201\*14 pcs  
 +330u\_D7\*2 pcs




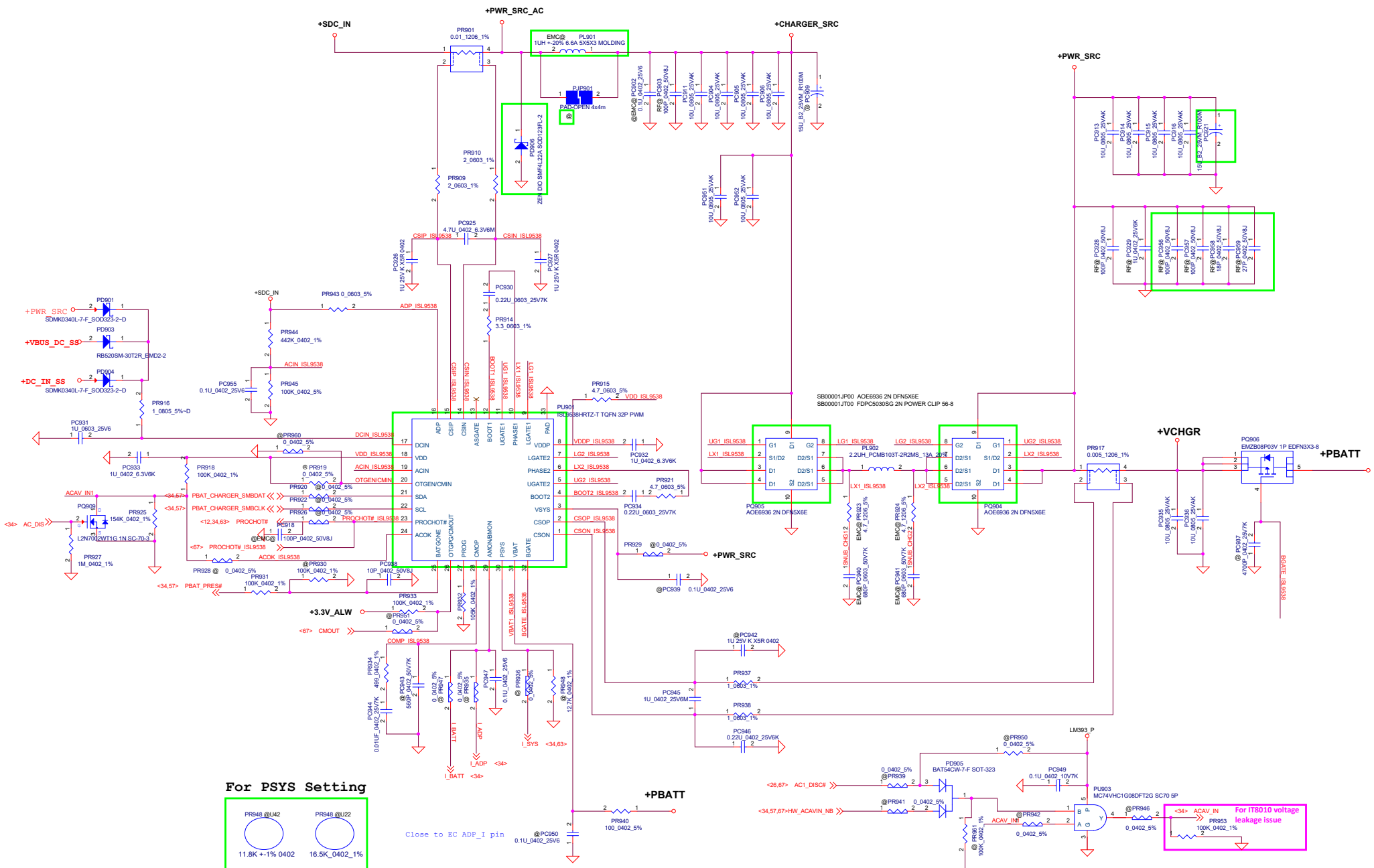
VCC\_SA Place on CPU  
 22U\_0603 \* 12 pcs + 1U\_0201\*7 pcs



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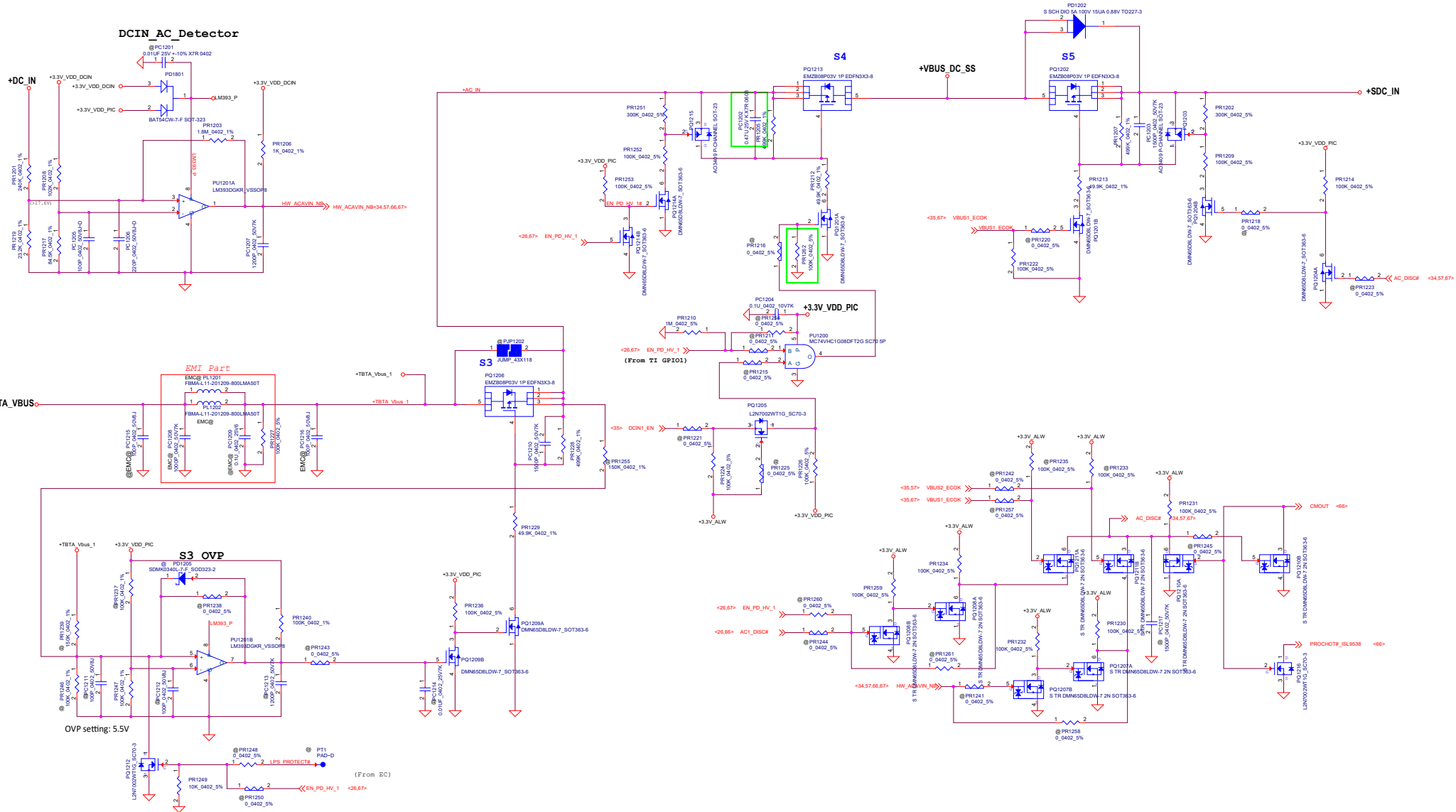
		Compal Electronics, Inc.	
		PROCESSOR DECOUPLING	
Title	Document Number	LA-E111P	
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		PWR_charger_ISL9538	
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	<b>Compal Electronics, Inc.</b>		
	File <b>Breckenridge_TypeC_PD</b>		
	Size	Document Number <b>LA_F401</b>	Rev <b>0.2</b>
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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	57	Change DrMOS	2017 06/07	Compal	Change DrMOS from TI to Fairchild	1. DrMOS change from CSD97396 to FDMF3035 2. PR660, PR672, PR665 Change from 2.2R to 3.9R 3. Remove PC679, PC680, PC681 4. PC686, PC687, PC688 change from 10P to 0.1U	X01
2	51 57 59	Add EMI portion	2017 06/09	Compal	EMI request & modify Components	1. Depop PC133, PC134, PC135, PC136, PC137, PC138, PC139, PC140, PC689, PC690, PC691, PC692, PC956, PC957, PC958, PC959 2. Pop PL901.	X01
3	53 54 56 57	Add RF team portion	2017 06/13	Compal	RF request & modify Components	Pop PC622, PR627, PC401, PR405, PC419, PR409, PC506, PR502, PC409, PC303	X01
4	56 57 59	Acoustic solution	2017 06/13	Compal	For acoustic solution CPU input MLCC change to 0603 low noise MLCC	1. Remove PC917, PC918, PC919, PC920, add PC921 B2 POS CAP 2. CPU input MLCC size change from 0805 to 0603 low noise MLCC PC608, PC612, PC656, PC657, PC658, PC664, PC665, PC672, PC673, PC674, PC675, PC682, PC683, PC684 3. Pop PC607	X01
5	59	Change Charger Dual-MOS	2017 06/13	Compal	Change Dual-MOS from TI to AOS	Dual-MOS change from CSD87351 to AOE6936	X01
6	57~ 76	MLCC	2017 07/31	Compal	LD request to change cap to 0-end P/N	0-end P/N for all cap	X02
7	66	EMI		Compal	EMI request	Type-C PD Bead EOL, so change BR MLK12_14_15 PL1201/PL1202 Bead to 80 ohm bead, CPN:SM01000P200,,»SM01000U300(2nd) CPN:SM01000P200,,»SM01000U400(main)	X02
8	57 65 66	2nd source		Compal	HW request for 2nd source list change	For Main source SA000000H00, 2nd source change SA007080100 ;÷ SA741080400	X02
9	65	charger resister		Compal	Charger current sense resister derating	PR937, PR938, PR909, PR910, PR915 0402>0603 SD014100B80 - S RES 1/10W 1 +-1% 0603 PR937, PR938 SD00001QK00 - S RES 1/10W 2 +-1% 0603 PR909, PR910 SD013470B80 - S RES 1/10W 4.7 +-5% 0603 PR915	X02
10	57~ 76	0 ohm shortpad		Compal	0ohm change to 0 ohm short pad	For 0ohm no short pad: Keep PR943, PR421, PR671, PR692 pop SD028000080	X02
11	65	charger		Compal	For adapter plug-in bouncing issue	Add PD906 SC40000EL00(S ZEN DIO SMF4L22A SOD123FL-2) before PL901 Isum choke	X02
12	65	charger		Compal	Buyer request	PD901, PD904 change from SCS0340L010 to SCS00009P00, for common part	X02
13	58 63	RF portion		Compal	RF request	Add MLCC for RF 100P_0402_50V: PC1335 PC141 PC142 PC143 PC314 PC317 PC144 PC145 PC319 PC320 27P_0402_50V: PC315 PC224 1U_0402_50V: PC316 PC318 PC321	X02
14							

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PWR P.I.R			
LA F401			
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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	40	M2 2280 Socket	2017/03/9	EE	For align with spindle HDD.	Add UZ37 circuit for 2280 SSD imdenpenden loadswitch --> add CN50~51, UZ37, PJP30_1*2(and no stuff all)	0.1(X00)
2	All	All	2017/03/9	EE	X9 request	UC1 CPU change from U22 to U42.	0.1(X00)
3	11	CPU (6/14)	2017/03/14	EE	KBL-R U42 X'tal	Add RC417~RC422,CC334,CC335, YC3 for U42 crystal	0.1(X00)
4	34	USH & TPM	2017/03/17	EE	Prevent POA_WAKE# ESD	Add RZ364 100 ohm to POA_WAKE#	0.1(X00)
5	All	All	2017/03/17	EE	Remove IO expander	1-1.Delete expander IO UE2 relating circuit(RE524,@RE525 change to 0 ohm) remove UE2, CE1, CE2, RE13~18, RE6, CE500, CE504, CE505 4/13 add UMA RE524/525(2.2kohm)--> B6/F7 4/17 B6/F7 change netname to GPU_SMDAT/CLK 1-2. GPIO change (RE374 reserve) PCH_RSMRST# GPIO204 -> USH_PWR_STATE# (delete RE363) PORT80_DET# -> DCIN1_EN (delete RE512,RE513,RZ131) SHD_IO3 -> VBUS1_ECOK (delete RE366~RE373, RE376,RE377,RE98,UE9) SHD_IO1 -> SATA_LED_EN ENVDD_PCH -> DCIN2_EN SIO_RCIN#_EC -> VBUS2_ECOK 1-3 For DSC (keep RE524, RE525)change name GPU_SMDAT/GPU_SMCLK SIO_EXT_SCI#_EC -> GPU_PWR_LEVEL (delete RE341) EXPANDER_GPU_SMCLK -> DGPU_PWROK RTCRST_ON_GPIO141(B6) -> GPU_SMDAT	0.1(X00)
6	36	MEC5105 Support	2017/03/24	EE	Remove Reset Threshold circuit	1. Delete F017~RE517 circuit. keep RE536 only remove UE7, QE13, RE34, RE348, RE536, RE537, RE530 CE5, CE6, CE503 add RE536 on EC side	0.1(X00)
7	All	All	2017/03/24	EE	Add RTC reset circuit	1. RTCRST_ON_GPIO122 change to RTCRST_ON... 2-1. +RTC_CELL_PCH circuit (Dell request) Delete RE514,RE515... Add QE14~QE17... Add RE540~RE546... Add CE63... Change RC56.2 net name to +RTC_CELL_PCH... Change UC1.AK19, UC1.BB14 net name to +RTC_CELL_PCH... 2-2.based on ARD1.3 Y[!^~iRTC circuit4WY[ RE551A~X\$K+RTC_CELL_PCH`S^1q. 3. +3.3V_ALW_DSW enable circuit (Dell request) Delete RE524... Add RC431~RC433... Add UC13,UC14... Change UE1.M7 net name to VCCDSW_EN_GPIO... 4. GPIO change USH_SMBCLK -> USH_EXPANDER_SMBCLK USH_SMBDAT -> USH_EXPANDER_SMBDAT Delete RTCRST_ON_GPIO141 PRIM_PWRGD_GPIO024 -> RESET_IN# 5. UC13 chante to QC6, UC14 change to QC7 4/17 RTC power Gate circuit rev.2 Delete RE540, RE542, RE544, RE545, QE14, QE16 Change RE543 to 1M ohm and RE546 to 10K ohm Add DE2, CE65, Reserve CE66 for VCCDSW_EN	0.1(X00)
<p>DELL CONFIDENTIAL/PROPRIETARY</p> <p>Compal Electronics, Inc.</p> <p>EE P.I.R (1/7)</p> <p>LA-F401P</p> <p>Friday, August 17, 2018 Sheet 63 of 69</p>							0.2

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# Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
8	All	All	2017/03/14	EE	co-lay DS3/non-DS3	1. DS3 / non-DS3 co-lay Add DC2, (DC1 add NDS3 @) Add RC501, RC503, RC505 for DS3 Add RC502, RC504, RC506 for Non-DS3 Use the original 0ohm, RC215 instead of RC504, RE536 instead of RC503 3/14 1. based on EDS that add RC503 / RC504 on SUSACK # / ME_SUS_PWR_ACK for DS3 2. UZ3 enable pin change netname to PCH_PRIM_EN 3. RE349 + DS3 @ 4. UZ34 input in form SIO_SLP_SUS # to PCH_PRIM_EN 3/15 1. For align KW that change as below "Part Reference" A RC501 -> RC439 B. RC502 -> RC440 C. RC503 -> RC443 D RC504 -> RC444 E. RC505 -> RC441 F RC506 -> RC442 3/27 Parallel 0ohm in DC2, reserved to avoid NDS3 @, EC too late to load code	0.1 (X00)
9	09	CPU (4/14)	2017/03/27	EE	For antenna request	4/17 BTC Power Case 0ohm for UART1 power option Add RC445, RC446, RC447 for UART1 power option RC445 change to connect to VCCDSW_EN and pop 4/17 UART whether pin swap, Align with SB. --> Pin swap align SB --> EVT phase pop UART, DVT phase remove 4/20 2. Remove RC435	0.1 (X00)
10	38	USH & TPM	2017/03/27	EE	Prevent contactless_det# backdrive	1. Add DZ8 to prevent contactless_det# backdrive	0.1 (X00)
11	37	USH & TPM	2017/03/15	EE	TPM650 include	1. TPM a. Delete RZ113, RZ111, QZ9 b. Add RZ365 and connect to +UZ12 TPM Add RZ366 and connect to +3.3V_M_TPM	0.1 (X00)
12	13	CPU (8/14)	2017/03/15	EE	Follow CRB	UC1.F65 & G65 to GND add RC436 to GND before UC1.F65 & G65	0.1 (X00)
13	16	CPU (11/14)	2017/03/15	EE	Follow MOW08	UC1.K52/AK52 Must be NOT connected	0.1 (X00)
14	10	CPU (5/14)	2017/03/28	EE	X9 Port MAP check	1. USB3.0 port1 with port6 swap 2. USB2.0 port1 with port9 swap	0.1 (X00)
15	9	CPU (4/14)	2017/03/29	EE	For Layout power trace	add +UART1_R power netname on UART1	0.1 (X00)
16	8	CPU (3/14)	2017/03/29	ME	Connector check	JSPI1 change from ENTERY_SP01001FW00 to ACES_SP01001CB10	0.1 (X00)
17	31,11	Card Reader RTS5242 CPU (6/14)	2017/03/29	EMI	EMI request	1. RR5~RR10 change to 0ohm 2. RC417~RC420 change from 0ohm to 33ohm	0.1 (X00)
18	28	USB 3.0 CONN TYPE C	2017/03/29	ESD	ESD request	1. Change DT7, DT8, DT11, DT12 to DT39 2. Change DT15, DT16, DT19, DT20 to DT40	0.1 (X00)

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19	16	CPU (11/14)	2017/03/29	EE	For BRMLK12 layout request	Let AK70,BB57,BB66,AU58,AU63 floating	0.1(X00)
20	All	All	2017/03/31	EE	Follow ARD1.3 remove WIGIG	1-1.change Source 1:3 demultiplexer(P83348B) to 1:2 demultiplexer(P83338B) 1-2,remove RV71, RC74, RV77, CV80 2-1. (DP)JNGFF1 remove CV145~150, CV152, CV153, CV156, CV157 2-2. (PCIE)JNGFF1 remove CZ14, CZ15 UC1 remove RC375	0.1(X00)
21	37	USH & TPM	2017/03/31	EE	TPM NPCT65X and NPCT75X schematic colay	UZ12 relating circuit and change UZ12 to SA0000AQ200	0.1(X00)
22	35	EC MEC5105	2017/04/05	EE	RTCRST_ON glitch	Reserve CE64	0.1(X00)
23	8	CPU (3/14)	2017/04/05	EE	Winbond 16MB SPI ROM EOL (change to J-die)	Change UC5, UC6 to SA00005VV20	0.1(X00)
24	26	[Type C]PD Controller TI	2017/04/05	EE	Change PD to PD3.0	Change UT5 to SA0000AP500	0.1(X00)
25	36	MEC5105 Support	2017/04/05	EE	Board ID define change	change RE79 to 240K for X00	0.1(X00)
26	All	All	2017/04/05	EE	EC GPIO check	1. rename form AUD_NB_MUTE# to NB_MUTE# for EC team request 2. rename form SYS_LED_MASK# to LED_MASK# for EC team request 3. change net name form THERMATRIP1# to THERMTRIP1# for EC team request 4. swap WWAN_RADIO_DIS# from UE1.M2 to UE1.F12 5. swap LCD_TST from UE1.D1 to UE1.M2 1. rename form FAN1_TACH to TACH_FAN1 for EC team request 2. DSC swap DGPU_PWR_EN to GPIO100 for save level shift at BR MLK project 3-1. DSC_swap GPU_PWR_LEVEL to GPIO126 for save level shift at BR MLK projcet 3-2. DSC_remove RE5 of GPIO126, 3-3. UMA_remove RE341 of SIO_EXT_SCI# 4. SYS_PWROK reserved 0ohm add netname to RESET_OUT 5. rename form ME_FW_EC to ME_FWP for EC team request rename from ME_FWP to ME_FWP_PCH 6. rename from THERMATRIP2# to THERMTRIP2# for EC team request 7. rename from HW_GPS_DISABLE# to GPS_DISABLE# for EC team request 8-1. rename from VGA_ID to VGA_IDENTIFY for EC team request 8-2. swap to GPIO035 form GPIO017 for Ecteam suggestion BEEP need change to PWM function 8-3. Swap BEEP pin to GPIO035 form GPIO017 EC team request. 9. rename from H_PROCHOT# to PROCHOT# for EC team request 10. rename from USB_PWR_SHR_VBUS_EN to USB_POWERSHARE_VBUS_EN for 1. Add but not stuff QZ4 and RZ370 2. Add zener diode DE1 (no stuff) for + 5V_RUN discharge 3. RZ370 into 0603 packaging, add net name	0.1(X00)
27	All	All	2017/04/06	EE	EC GPIO check		0.1(X00)
28	47	Power control	2017/04/07	EE	+5V_RUN discharge circuit for S3 no power issue		0.1(X00)
29	8	CPU (3/14)	2017/04/07	ME	JSPI1 footprint pin1 Reversal 180 of ENTERY to ACES	Symbol reverses 180 degrees	0.1(X00)
30	24	DP to VGA & VGA Conn	2017/04/07	EE	When the system can not read the VGA EDID, the maximum resolution will be pressed at 1024x768	reserve RV620 PU to +3.3V_RUN ** Pop RV620	0.1(X00)
31	36	MEC5105 Support	2017/04/07	EE	To increase power current rail for each debug card	RE71 changed to SD034100A80, that change 49.9 to 10ohm current limiting resistor to smaller.	0.1(X00)

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32	All	All	2017/04/07	EE	EC GPIO check	1. rename from USB_PWR_SHR_LFT_EN# to USB_POWERSHARE_EN# for EC team request	0.1(X00)
33	All	All	2017/04/10	EE	EC GPIO check	1. 3.3V_TS_EN rename to PCH_3.3_TS_EN SHD_I00 change to 3.3V_TS_EN and delete RE366 and PU 100K RE547 Add RV323/RV324 for 3.3V_TS_EN/PCH_3.3V_TS_EN option 2. SHD_CLK -> PS_ID and delete RE374 3. CLKRUN#_EC -> ENABLE_DS# and delete RE337 and add RE549, RE550 4. change net name form PANEL_ID to SYSTEM_ID 5. SIO_EXT_SMI#_EC -> free and delete RE338 6. SIO_RCIN#_EC -> VBUS2_ECOK and delete RE339/RC13 7. rename from SATA_LED_EN to MASK_SATA_LED# for EC team request 8. rename form FAN1_PWM_1 to PWM_FAN1 for EC team request 9. GPIO054(PS_ID) swap to GPIO056 for EC team request 10. PCH_ALW_ON keep GPIO231 and assign DCIN2_EN to GPIO107 11. EXPANDER_GPU_SMCLK -> free and delete RE525 12. this pin should be change to reserved,Current EC no use PCH_ALW_ON to control +3.3V_ALW_PCH, it control by SIO_SLP_SUS# directly 13. rename from SLOT2_CONFIG_1 to NGFF_CONFIG_1 for EC team request 14. rename from ACAVIN_IN_NB to HW_ACAVIN_NB for EC team request 15. rename from SLOT2_CONFIG_0 to NGFF_CONFIG_0 for EC team request 16. rename from SB_reserve_SLOT2_CONFIG_net to NGFF_CONFIG_2 for EC team request 17. rename from SB_reserve_LID_CLK_NB# to LID_CLK_SIO# for EC team request	0.1(X00)
34	All	All	2017/04/11	EE	PCH GPIO check	1. Follow SB reserve SIO_EXT_SCI#,for no use LPC mode 2. Follow SB reserve PCI_CLK_LPC1, for no use LPC mode 3. DEL SIO_RCIN# net,for no use LPC mode 4. Follow SB reserve SIO_EXT_SMI# net, for no use LPC mode 5. Rename PCH_3.3V_TS_EN from 3.3V_TS_EN 6. Follow SB reserve PME#, for no use LPC mode 8. Follow SB reserve SIO_EXT_SMI# net, for no use LPC mode	0.1(X00)
35	All	All	2017/04/11	EE	Following port MAP	LOM port to be replaced to port 4	0.1(X00)
36	All	All	2017/04/13	EMI	EMI request	change 0ohm short pad to 0ohm of as below. RC328,RT54~57,RZ56,RN99	0.1(X00)
37	All	All	2017/04/17	EE	For All of Repeater	4/17 PWD pin setting double check for all of redrive(dual, signal, USB3) 4/21 UMA 1. SATA repeater --> add QN6, RN226, RN227 2. PCIE/SATA repeater --> add QN7, RN228,RN229,RN230 DSC 1. PCIE/SATA repeater --> add QN6, RN226, RN227	0.1(X00)
38	All	All	2017/04/17	EE	GPIO map change	4/17 PCH_3.3V_TS_EN PU +3.3V_RUN change page to QV7.2 -->Add RV326 and depop RC282/RE547 for 3.3V_TS_EN/PCH_3.3V_TS_EN 1. RC443 BOM structure change to @ 2. UMA : GPIO126->GPU_PWR_LEVEL 3. Add RTCRST_ON_R net neme for QE17.2 4. Add SIO_SLP_SUS#_R net name and PU RE561 5. RC27.2->NC for CLKRUN# 6. UMA : HDD_DET#->SATAGP0 7. Remove RE360/RE364	0.1(X00)

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39	47	Power control	2017/04/19	EE	EC request to reseve OR gate for WLAN power EN	Reserve DZ9 4/20 RZ38 PD change to WLAN_PWR_EN_UZ2	0.1 (X00)
40	36	MEC5105 Support	2017/04/19	EE	EC request to reseve ESPI_RESET# for JESPI	Reserve RE560	0.1 (X00)
41	All	All	2017/04/19	EE	OTG support	Pop RT74, Depop RC337 4/20 RC337 10K to GND	0.1 (X00)
42	35	EC MEC5105	2017/04/19	EE	Dell request to add test point for EC free pins	Add test point T141 for UE1.D1->GPIO051 Add test point T142 for UE1.L11->GPIO054 Add test point T264 for UE1.F13->VBUS3_ECOK Add test point T143 for UE1.K7->GPIO011 Add test point T144 for UE1.M1->GPIO100 Add test point T262 for UE1.J6->GPIO202 Add test point T147 for UE1.M4->DGPU_PWROK only UMA	0.1 (X00)
43	38	USH & TPM	2017/04/19	EE	JUSH1 add net name	1. Add net name at DZ8.1 .	0.1 (X00)
44	37	USH & TPM	2017/04/21	EE	TPM change to NPCT650x	Change UZ12 to SA00008EL80 and related resistors	0.1 (X00)
45	37	USH & TPM	2017/04/24	EE	BOM option by i\$650@i" or i\$750@	1.The pop option for VHIO power: NPCT750: VHIO=+3.3V_RUN NPCT650: VHIO=+3.3V_ALW_PCH 2.The pop option for SLP_S0# connection: NPCT750: pop RZ112 (SLP_S0#=GPIO0) NPCT650: pop RZ363 (SLP_S0#=GPIO2) 3.RZ62 can be removed	0.1 (X00)
46	9	CPU (4/14)	2017/04/24	EE	JUART1 remove	remvoe JUART1, RC434	0.1 (X00)
47	11	CPU (6/14)	2017/04/24	EE	Schematic align	INTRUDER# PU change to +RTC_CELL_PCH	0.1 (X00)
48	All	All	2017/04/24	EE	GPIO map change	GPIO013 net name change to DGPU_PWROK UPD1_ALERT#-->UPD1_SMBINT# UPD1_SMBUS_ALERT#-->UPD1_SMBINT#_R	0.1 (X00)
49	28	USB 3.0 CONN TYPE C	2017/04/13	EE	Swap ESD diode pin for layout	DT39 & DT40 swap pin	0.1 (X00)
50	11	CPU (6/14)	2017/04/19	EMI	EMI request	1. Add RC550 for KBL-R U42 .	0.1 (X00)
51	35	MEC5105 ESPI EC	2017/06/06	EE	GPIO map change	UPD2_ALERT#-->UPD2_SMBINT#	0.2 (X01)
52	47	Power control	2017/06/06	EE	Change netname align with SB	WLAN_PWR_EN_U2--> WLAN_PWR_EN	0.2 (X01)
53	16	MCP(11/14) PWR-VCCGT	2017/06/06	EE	Add netname for layout	RC437.2 --> +VCC_GT_K52 RC438.1 --> +VCC_GT_AK52	0.2 (X01)
54	35	MEC5105 ESPI Power control	2017/06/06	EE	EC request to reseve OR gate for WLAN power EN	Add QZ15 and RZ518 Change SIO_SLP_WLAN# to SLP_WLAN#_GATE (EC side UE1.K10) & Add RE552	0.2 (X01)
55	26	[Type C]PD Controller TI-1	2017/06/06	EE	PD ROM main source change	UT6 change to SA000095R10 (GD)	0.2 (X01)
56	11	MCP(6/14) CLK,PM,RTC	2017/06/07	EE	Schematic align, avoid SUSACK#_R floating	Reserve RC551	0.2 (X01)

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57	37	NuvotonTPM1.2	2017/06/07	EE	Nuvoton request to change TPM_PIRQ# power rail TPM change to NPCT750	TPM PIRQ# power rail change to +3.3V_ALW_PCH Change UZ12 to SA0000AQ200 and related resistors	0.2 (X01)
58	24	DP to VGA & VGA ConnRTD2166	2017/06/07	EE	RTD2166 question	UV6.12 add RV622 PU to +3.3V_RUN	0.2 (X01)
59	28	[Type C]USB 3.0 CONN TYPEC1	2017/06/07	ESD	ESD request	DT10, DT13, DT14, DT17,DT18,DT5,DT6,DT9 change from SC40000AT00 to SC40000DF00	0.2 (X01)
60	37	NuvotonTPM1.2	2017/06/07	EE	For RBOM request.	CZ75 from 4.7uF to 10uF	0.2 (X01)
61	33	NGFF Card	2017/06/07	EE	Correct the symbol	Update JNGFF1/JNGFF2 symbols	0.2 (X01)
62	20,36	All	2017/06/08	EE	Main source change	UD1, UE4, UE6 change to SA00007WE00	0.2 (X01)
63	46	All	2017/06/08	DFB	DFB request	PCB hole from 3.2mm to 3.3mm Location:H34,H35 LA13 symbol change to " TAI-T_HCB2012KF-121T50_2P"	0.2 (X01)
64	ALL	All	2017/06/12	DELL	Dell request to change cap to L-end P/N	L-end P/N for all cap	0.2 (X01)
65	36	MEC5105 Support	2017/06/14	EE	BOARD_ID change	Change RE79 to 130Kohm? (rev. X01)	0.2 (X01)
66	11	HDMI conn	2017/06/14	EE	Crystal Vendor suggest	CC21,CC22=12pF	0.2 (X01)
67	12	MCP(7/14)MISC, JTAG,HDA,SDIO	2017/06/14	ESD	ESD request	Add CC336 100P, place near CPU side	0.2 (X01)
68	34	DMIC	2017/06/14	RF	RF request	CA54 change to 27pf	0.2 (X01)
69	41	All	2017/06/15	DELL	DELL request	1-1. pop PJP33 1-2. Non-pop UZ23,CZ129,CZ130,PJP32 2-1. del UZ37,CN50,CN51,PJP30	0.2 (X01)
70	9	MCP(4/14)GSPI, I2C,UART,ISH	2017/06/15	EE	GPIO map change	Add TypeC_CON_SEL1/TypeC_CON_SEL2 for UC1.W4/UC1.AB3 Reserve RC553-RC556 for connector selection	0.2 (X01)
71	47	Power Control	2017/06/15	EE	EC request to reseve OR gate for WLAN power EN	Change QZ15 to SB00000T000	0.2 (X01)
72	47	DP/USB Redriver SW1 TUSB546	2017/06/15	EE	PS8743 colay	Add RT410, RT411, RT412,RT413, RT414, RT415, RT416,CT213 Add RT405, RT406, RT407, RT417, RT418	0.2 (X01)
73	24	DP to VGA & VGA ConnRTD2166	2017/06/21	EE	RTK suggest	LV19/LV20 --> RV650/RV651 \$i75e[ ; CV132/CV133 \$i2P	0.2 (X01)
74	26	[Type C]PD Controller TI-1	2017/06/21	EE	TPS65982(UT5) update version	DB --> DC (SA0000AX700)	0.2 (X01)
75	34	Codec ALC3246	2017/07/26	ESD	ESD request	DA2, DA6, DA7 change main source from SCA00002900 to SCA00001A00	0.3 (X02)
76	All	All	2017/08/01	EE	Change cap to 0-end P/N	0-end P/N for all cap	0.3 (X02)
77	26	[Type C]PD Controller TI	2017/08/02	EE	TI TPS65982 request(TBTA_DEBUG4)	pop RT407 when pop 8743 & change to 10K	0.3 (X02)
78	28	USB 3.0 CONN TYPE C	2017/08/02	EE	SE part COS issue.	CT99, CT100, CT101, CT102 change to 0.01u_X5R_0201_25V (SE00000YH00)	0.3 (X02)

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79	25	DP/USB3 Repeater SW TUSB546	2017/08/02	EE	TI update version(TUSB546A)	TUSB546 change form SA00009R710 to SA00009R720	0.3 (X02)
80	All	All	2017/08/03	EE	To avoid in-rush current caused voltage drop	Add soft start solution(only reserved) on QV8,QZ1 (add CV635, CZ200, RZ380,RV400) 8/4 Add soft start solution(only reserved) on QE15,QC7 (add CC340,RE565)	0.3 (X02)
81	All	All	2017/08/07	RF	RF request	1. pop C219,CC220,CC221,CC225,CC337,CV11,CV16,CZ62,CZ6,CZ64,CZ67,CZ68, CZ85,CZ86,CZ87,CZ91,CZ92 2. add LZ2,CZ210,CZ211,CE70,CZ212,LE1,CI50~CI52,CC341 3. del RZ85,RZ87	0.3 (X02)
82	36	MEC5105 Support	2017/08/08	EE	BOARD_ID change	Change RE79 to 62Kohm? (rev. X02)	0.3 (X02)
83	9	CPU (4/14)	2017/08/09	EE	TPM Pin connectivity requirement	Add RC560,RC561(reserved) BOM options.	0.3 (X02)
84	All	All	2017/08/11	EE	Buyer request	main source change 1 .SC1N4148180 --> SC100005500 2. SC100000S00 --> SCS00003700	0.3 (X02)
85	36	Board ID	2017/9/11	EE	Board ID change	RE79 change to (A00)4.3K = SD028430180	1.0 (A00)
86	12	ME SW	2017/9/11	EE	ME SW depop	depop RC222,SW1 RC221 change to 0ohm short pad	1.0 (A00)
87	ALL	0 ohm change to short pad	2017/9/11	EE	0 ohm change to short pad	RC294,RC295,RC296,RC328,RC422,RC550,RC444,RC445,RE32,RE290,RE548,RE552, RN99,RN186,RN187,RN192,RN223,RN224,RN225,RR5~RR10,RT54~RT57,RT74,RV323, RZ56,RZ61,RZ64,RZ89,RZ368,RZ112,RZ365	1.0 (A00)
88	ALL	0 ohm change to short pad	2017/9/15	EE	Only support DS3 0 ohm change to short pad	RC439,RC441,RE536	1.0 (A00)
89	37	change P/N	2017/9/15	EE	TPM change to MP sample	UZ12 change to SA0000AQ220	1.0 (A00)
90	9	GPIO map change	2017/9/15	EE	GPIO map change	Drop win7 debug de-pop RC330, RC331	1.0 (A00)
91	ALL	DFX request	2017/9/18	EE	Close solder mask	LV3,LV6,LV9,LV12 RI47,RI48,RI49,RI50, RI27,RI28,RI29,RI30 CMOS1,CI32	1.0 (A00)
92	38	DFX request	2017/9/18	EE	Modify the DZ8 footprint	Modify the DZ8 footprint to follow DE2. because pcb pad is smaller	1.0 (A00)
93	26	(Type C) PD Controller TI	2017/11/14	EE	component poor supply	CT74,CT83 change from SE000000U00 to SE00000QL10	1.0 (A00)
94	11 13 17 18 20 21 23 31 35 36	MLCC downsize	2018/04/18	EE	component poor supply	delete f°CC24 CC25 CC199 CC203 CC204 CC205 CC206 CC207 CC208 CC211 CC212 CC213 CC215 CC216 CC217 CC218 CC222 CC251 CC253 CC264 CC265 CC326 CD9 CD10 CD11 CD12 CD13 CD14 CD15 CD16 CD18 CD19 CD23 CD24 CD41 CD42 CD43 CD44 CD45 CD46 CD47 CD48 CD50 CD51 CD55 CD56 CE10 CE14 CE30 CE31 CE63 CR15 CR22 CZ100 CZ102 CZ105; add: CC78~CC81, CC84~CC113, CC118,CC119, CC122~CC129,CD108~CD111, CD64~CD107, CE101 CE102 CE141 CE142 CE301 CE302 CE311 CE312 CE631 CE632 CR1501 CR1502 CR2201 CR2202 CZ1000~CE1005	2.0 (A01)

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95	44	USB POWER	2018/04/18	EE	component poor supply	CI8/CI801 CO-LAY	2.0 (A01)
96	36	Board ID	2018/04/18	EE	Board ID change	RE79 change to (A01)2K	2.0 (A01)
97	18	improve ripple	2018/08/11	EE	WHEA BSOD issue	CC221,CC219,CC220,CC226 from 0805 47uf to 0603 22uf ; RC171 from 0402 0ohm to 0603 0ohm	3.0 (A02)
98	36	EC MEC5105 Support	2018/08/17	EE	Board ID	Change RE79 to 240Kohm (rev. A02)	3.0 (A02)

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