

Model Name : ZIWB0/ZIWB1/ZIWE0

File Name :

Compal Confidential

ZIWB0/ZIWB1/ZIWE0 UMA M/B Schematics Document

Intel Bay Trail M

2014-02-10

REV:1.0

14PCB@
DA1 PCB

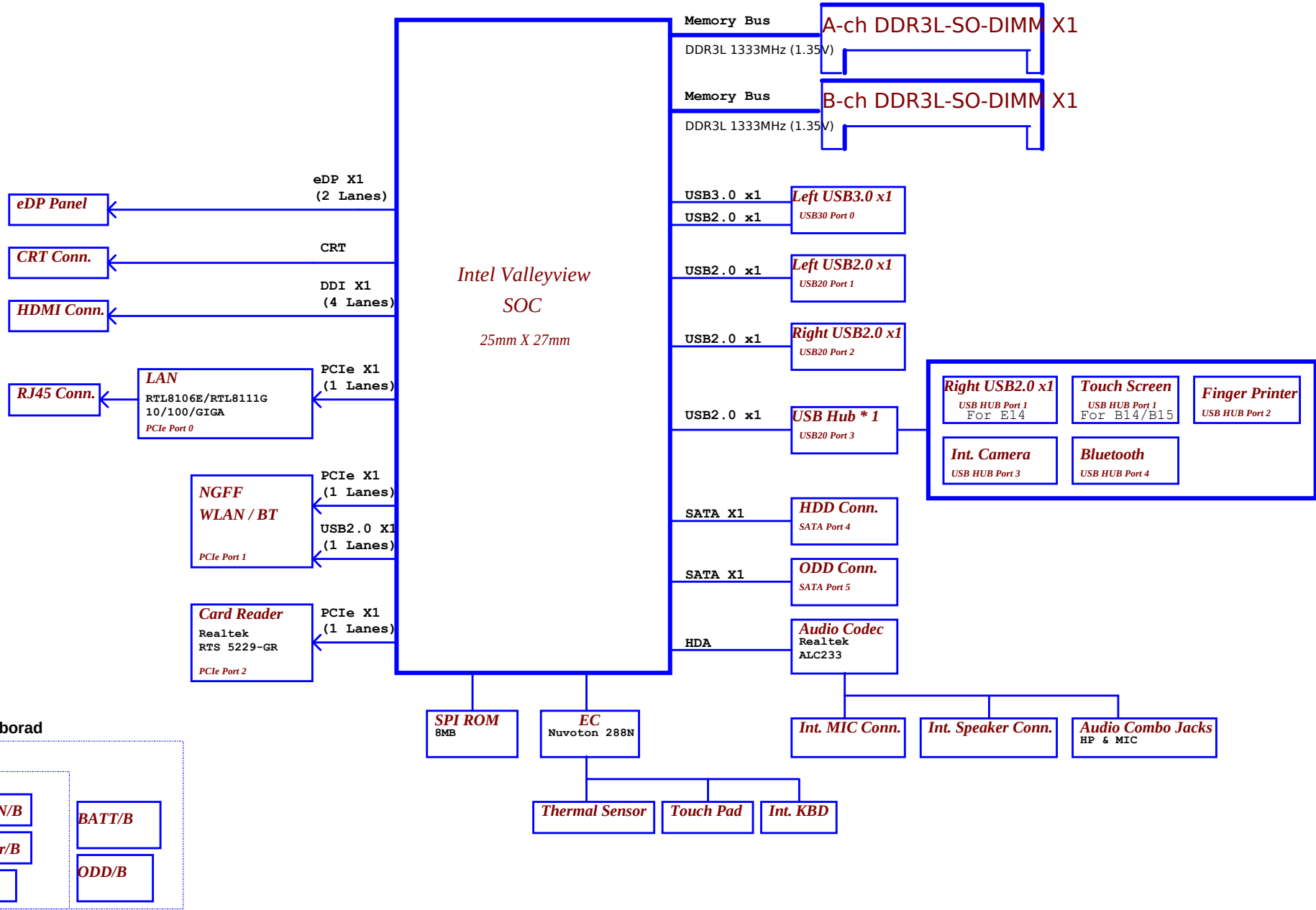
Part Number	Description
DA60013Z010	REV1.0 M/B

15PCB@
DA2 PCB

Part Number	Description
DA60013Z110	REV1.0 M/B

www.repair1.ru

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Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.0VALW	+1.0v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+SOC_VCC	Core voltage for SOC	ON	OFF	OFF
+SOC_VNN	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.0VS	+1.0v system power rail	ON	OFF	OFF
+1.05VS	+1.05v system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	

BOM Option Table

Item	BOM Structure
Unpop	@
Connector	ME@
XDP (Debug Port)	XDP@
EMC requirement	EMC@
EMC requirement unpop	@EMC@
ESD requirement	ESD@
ESD requirement unpop	@ESD@
Touch Screen	TS@
B/E series sku	B14@
B/E series sku	B15@
B/E series sku	E14@

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
Charger	0b00010010 (0x12H)

SOC SM Bus address

Device	Address
SO-DIMM A (JDIMM1)	A0h
SO-DIMM B (JDIMM2)	A2h

EC SM Bus2 address

Device	Address
GPU	0x9E
Thermal	1001_101xb

43 level BOM table

43 Level	Description	BOM Structure

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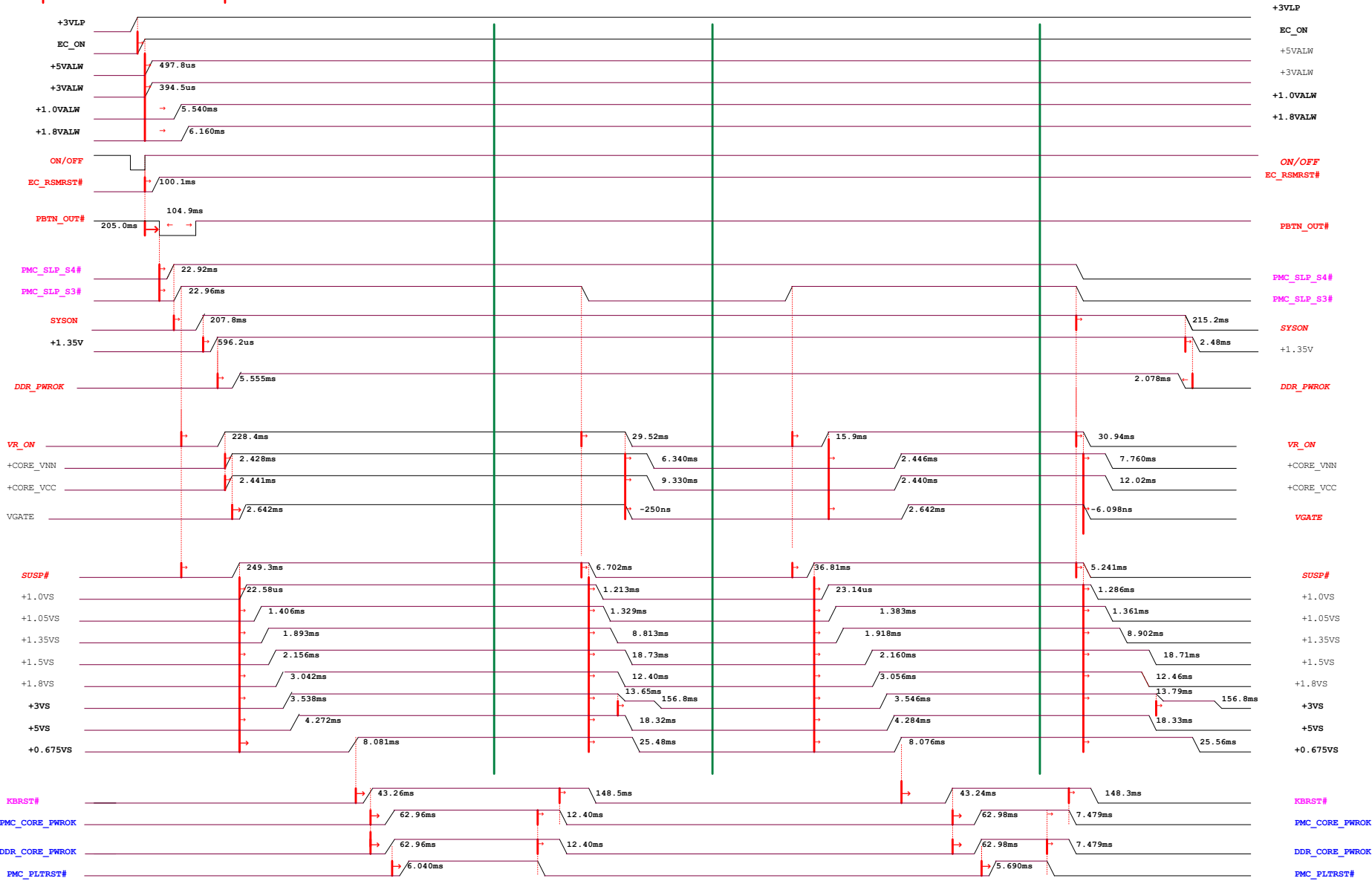
Power On

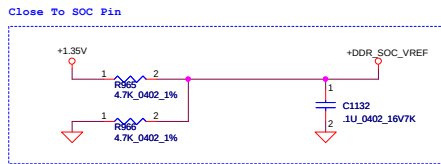
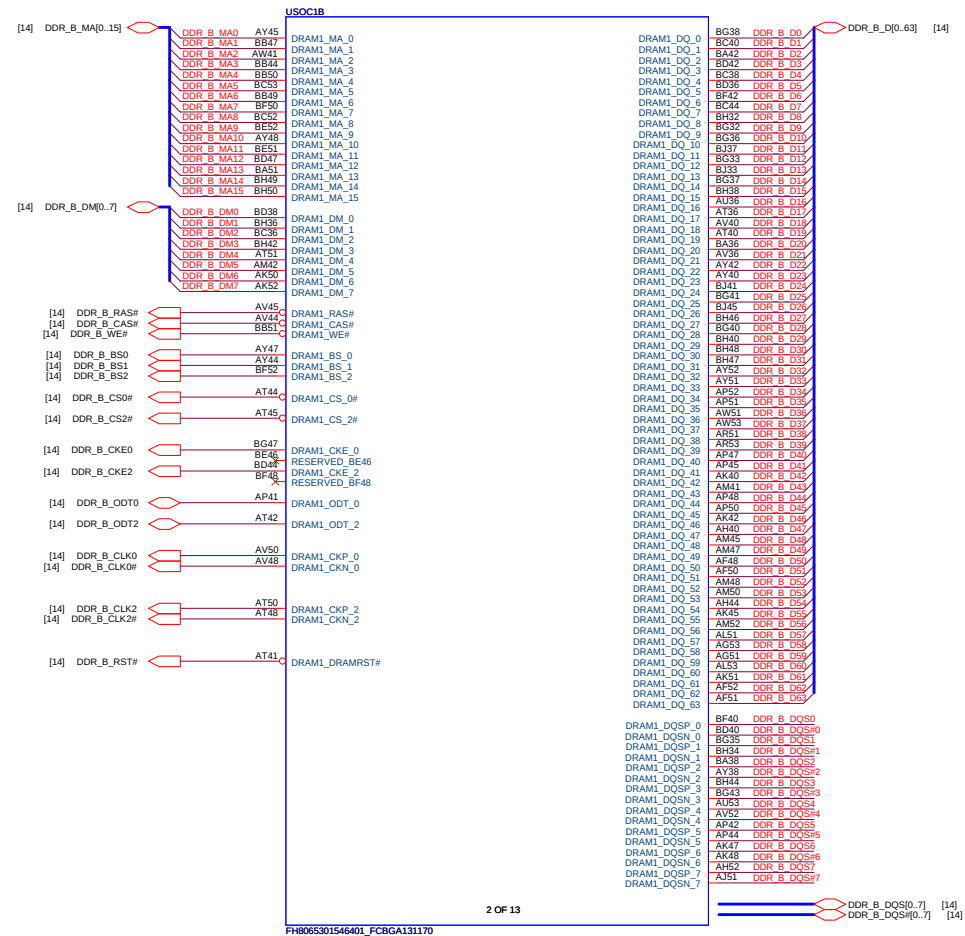
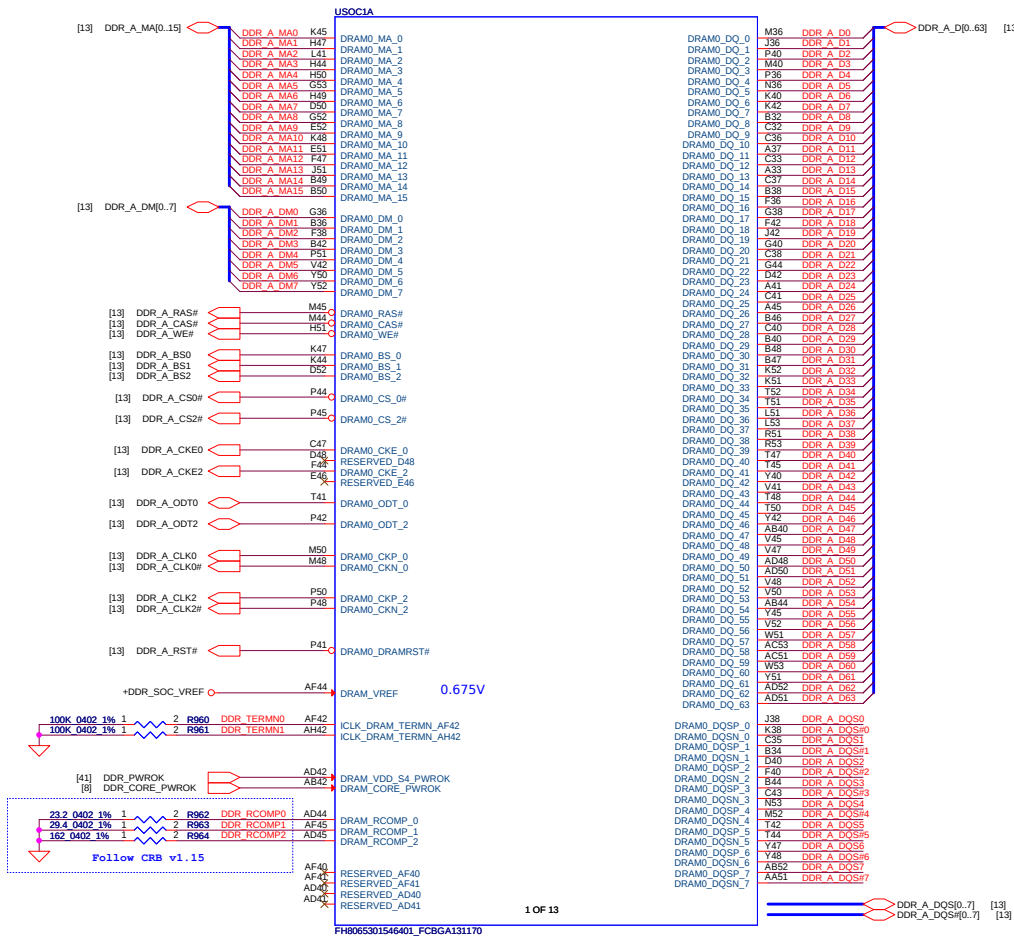
S3

S3 Resume

Power Off

Plug in





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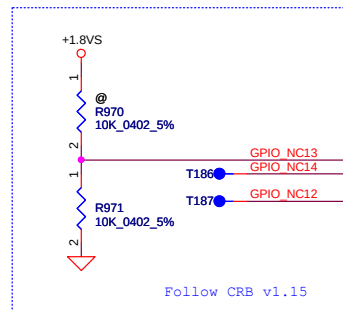
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Compal Electronics, Inc.
VLV-M SOC Memory DDR3L

Intel BayTrail-M Platform

HDMI

Follow CRB v1.15 0ohm till to GND



GPIO_S0_NC[13]:
Multiplexed with Hardware Straps Pin:MDSI_DDCDATA

USOC1C

1.0V

1.8V

1.8V

1.8V

1.8V

1.8V

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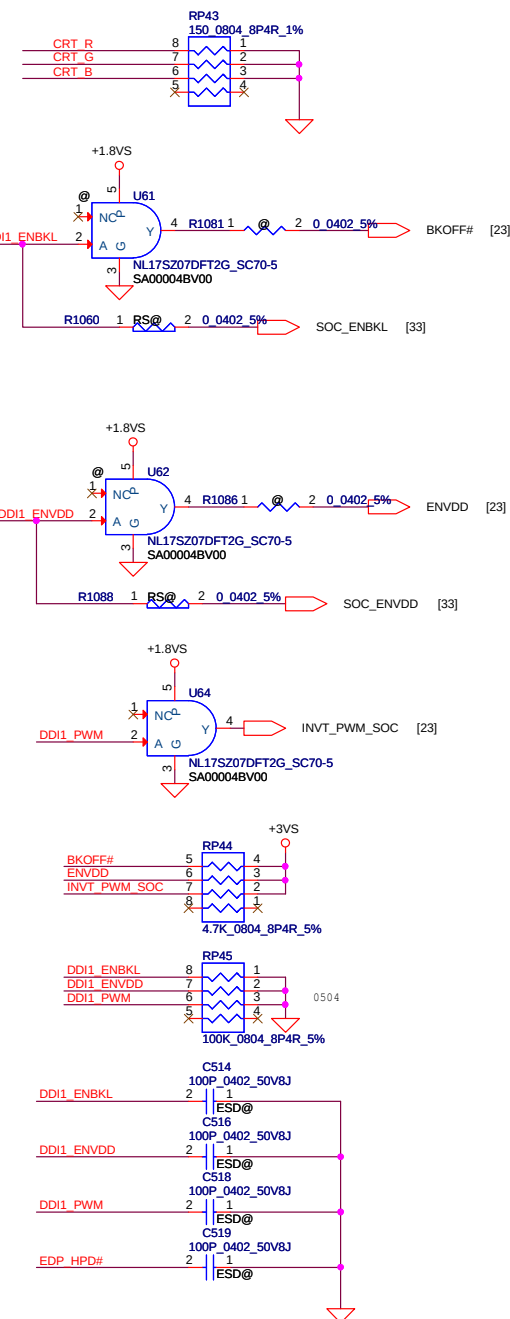
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1.0V

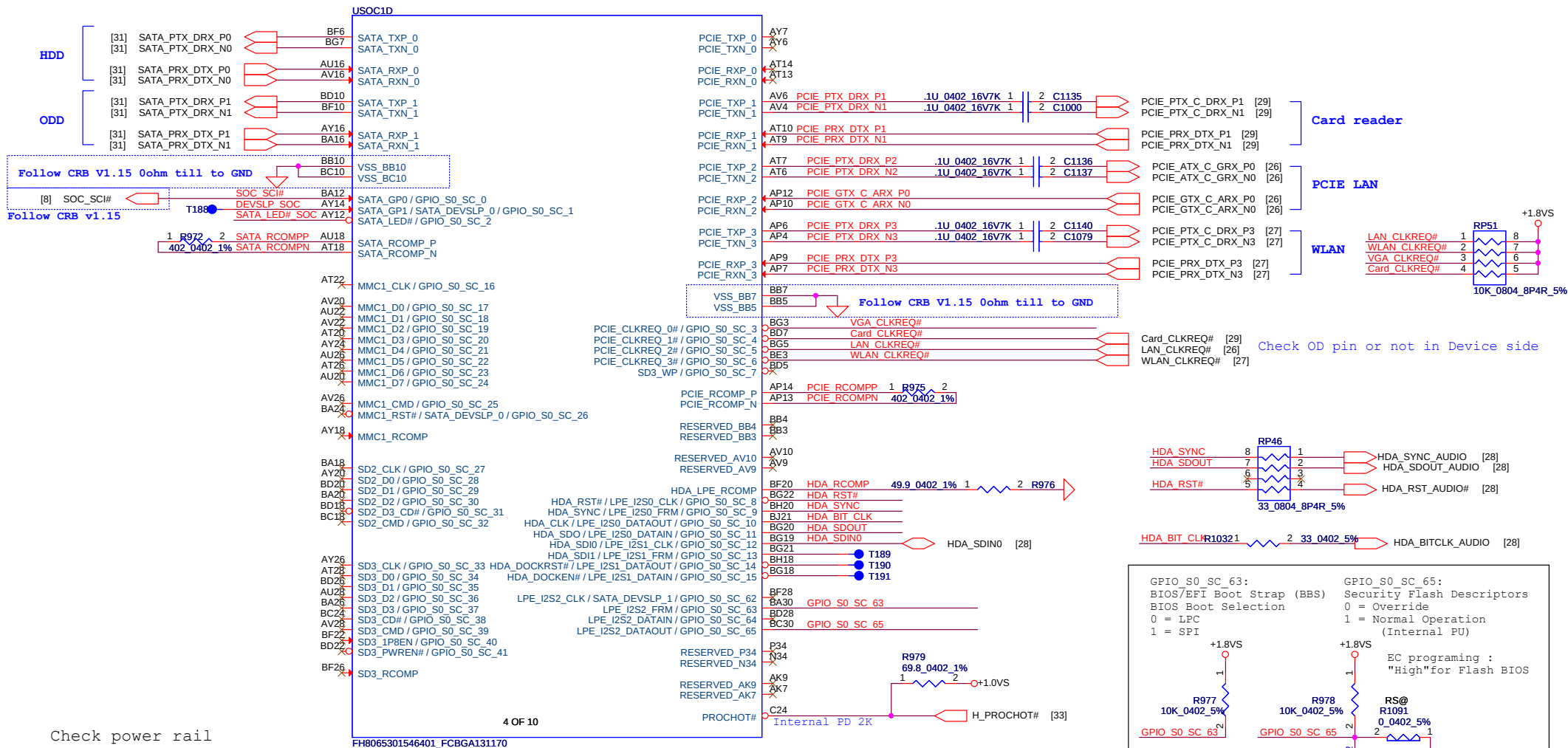
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eDP Panel

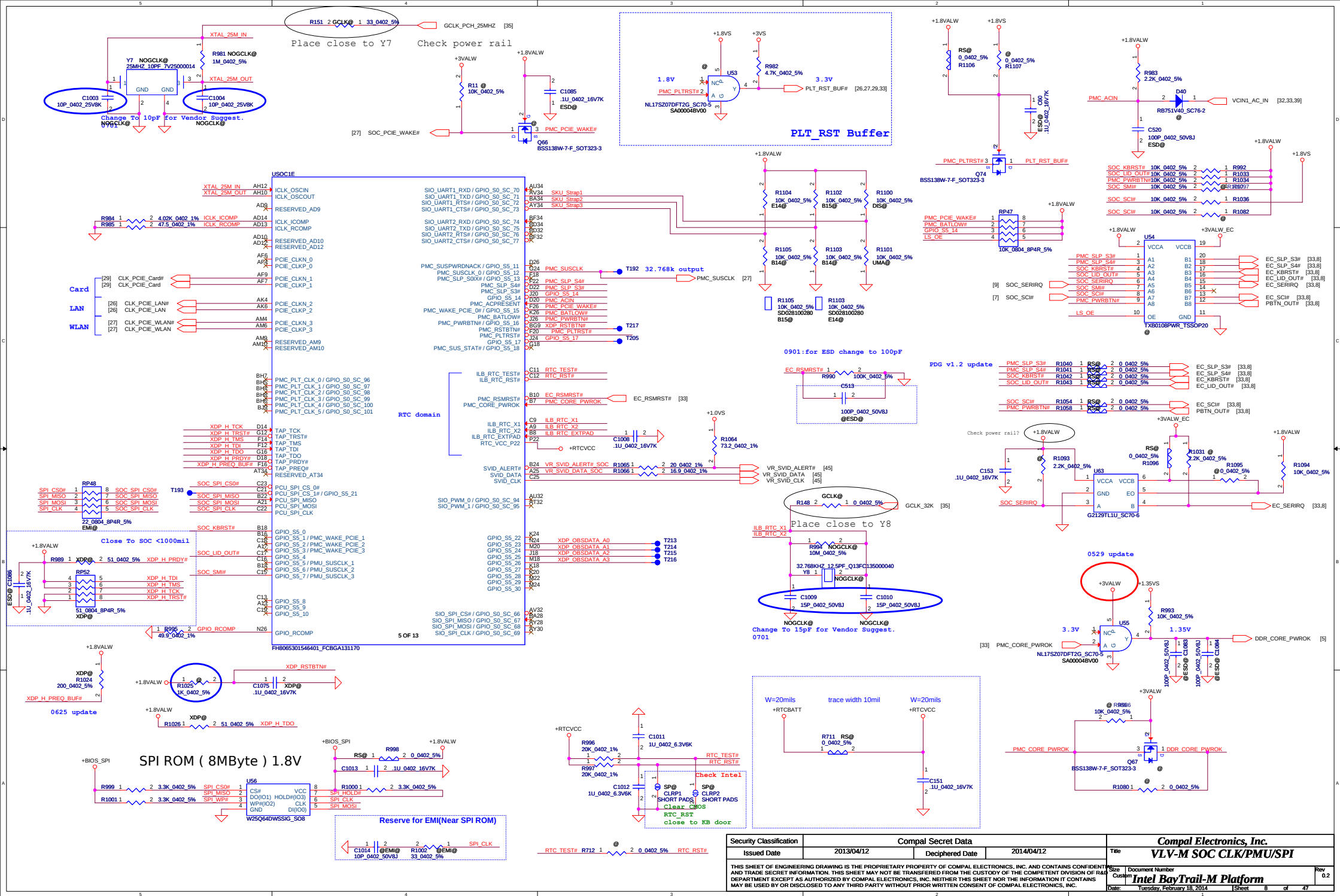
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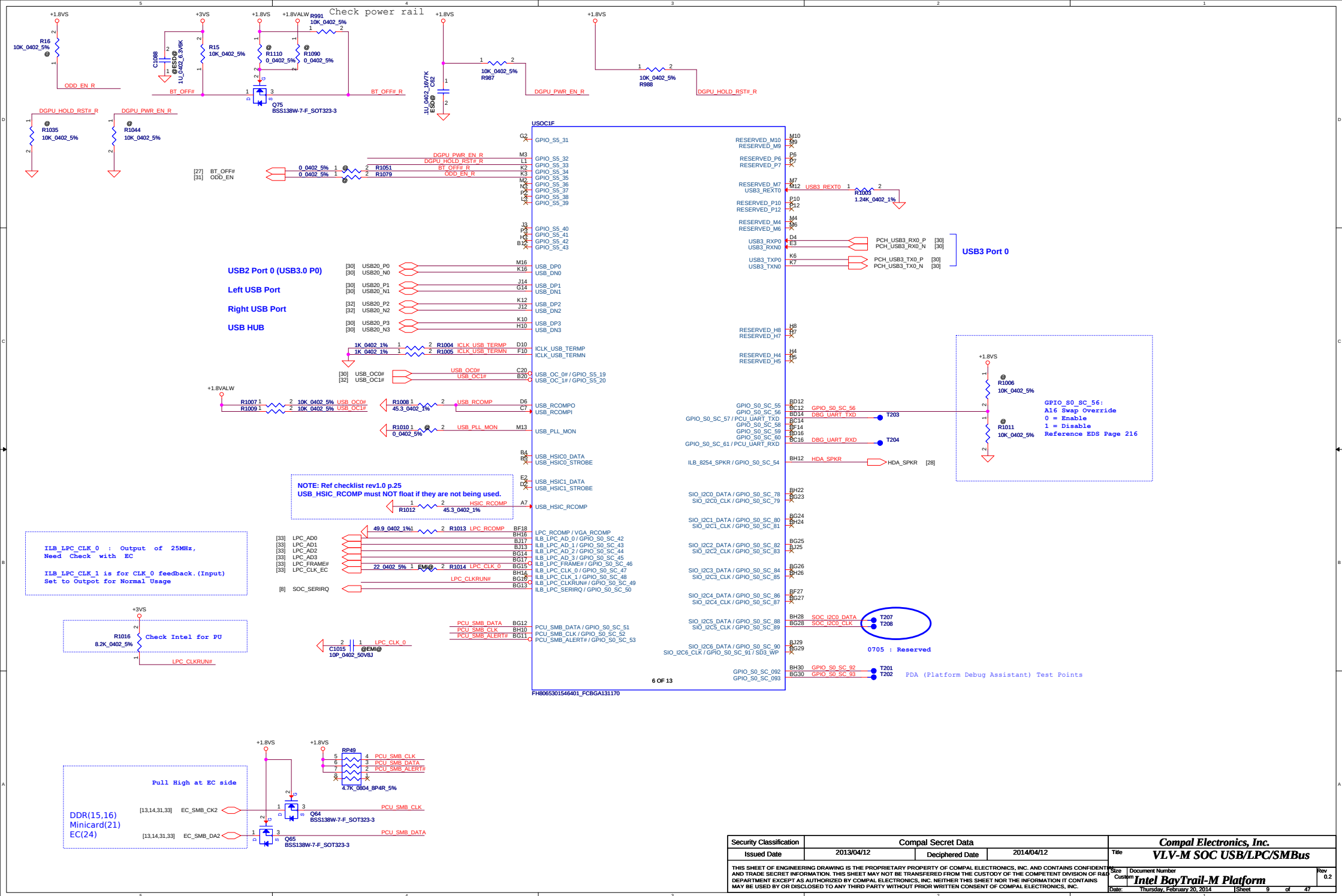


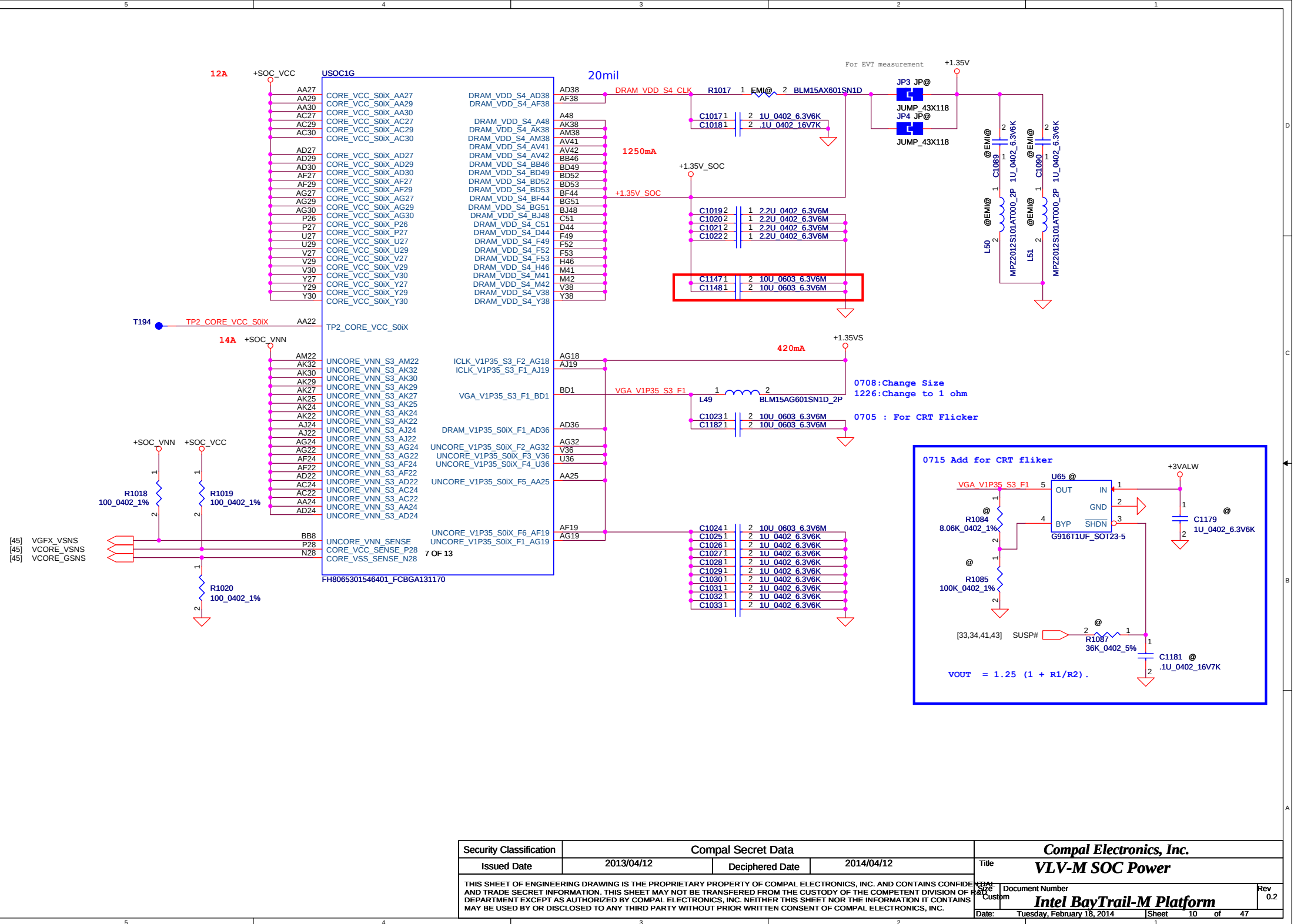
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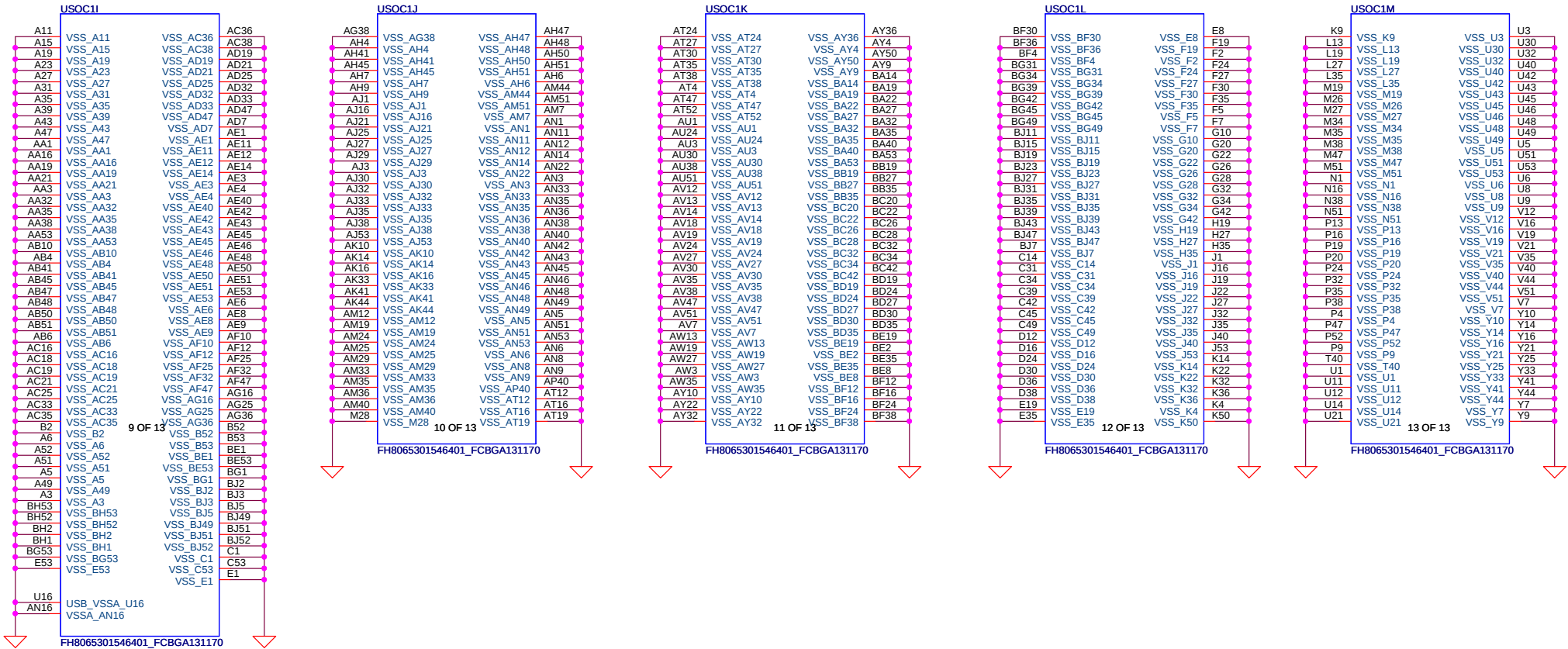


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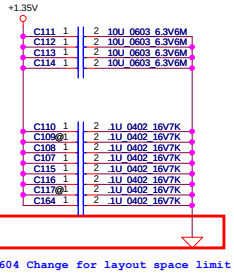




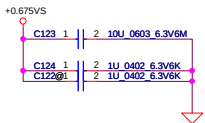




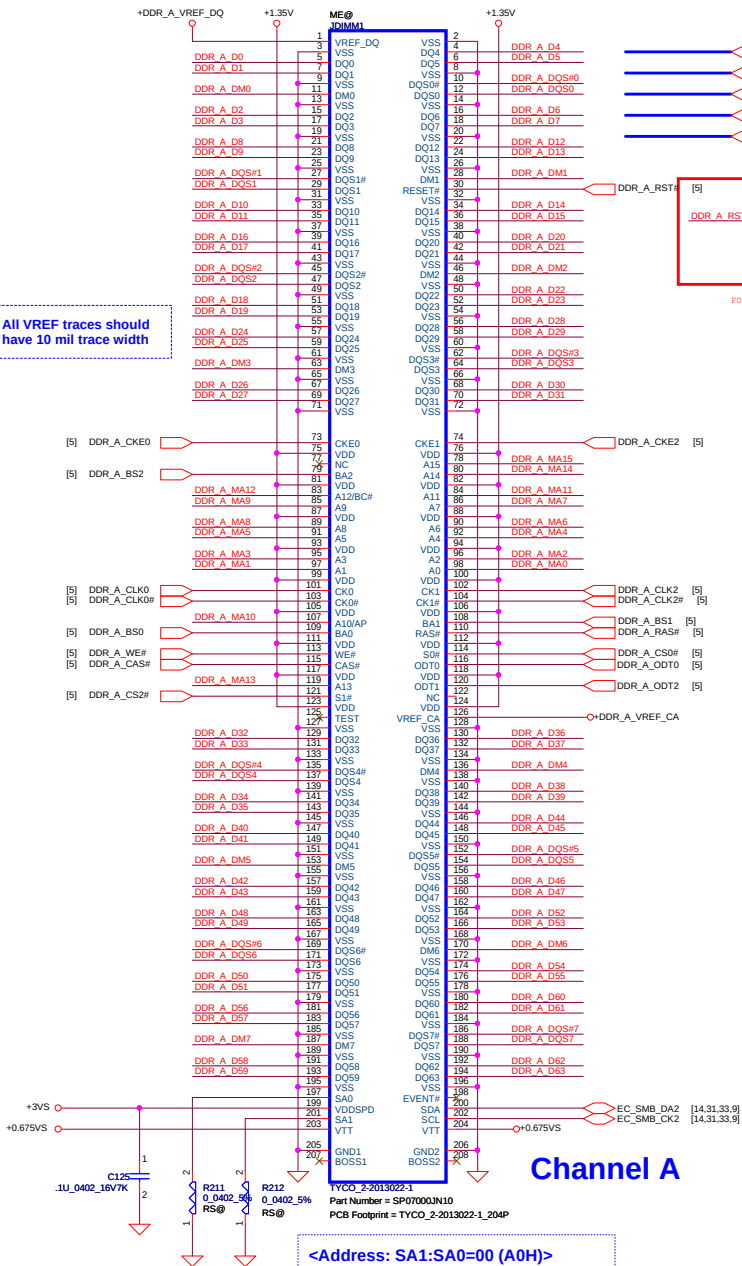
Layout Note:
Place near JDIMM1



All VREF traces should
have 10 mil trace width



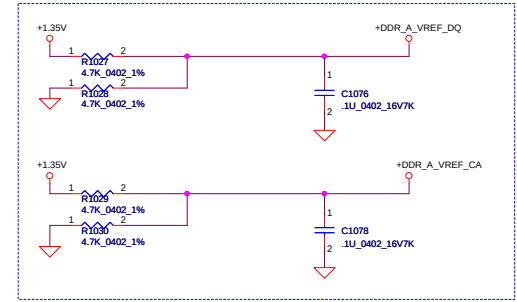
Layout Note:
Place near JDIMM1.203,204



Channel A

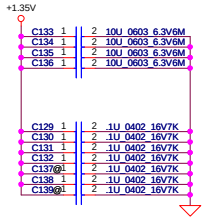
<Address: SA1:SA0=00 (A0H)>
DIMM_1 STD H:4mm

Signal voltage level = 0.675 V
PLACE TWO 4.7K RESISTORS CLOSE TO
DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
Decoupling caps are needed; one 0.1 uF placed close to VREF pins of each DDR3 SODIMM.

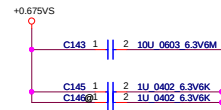


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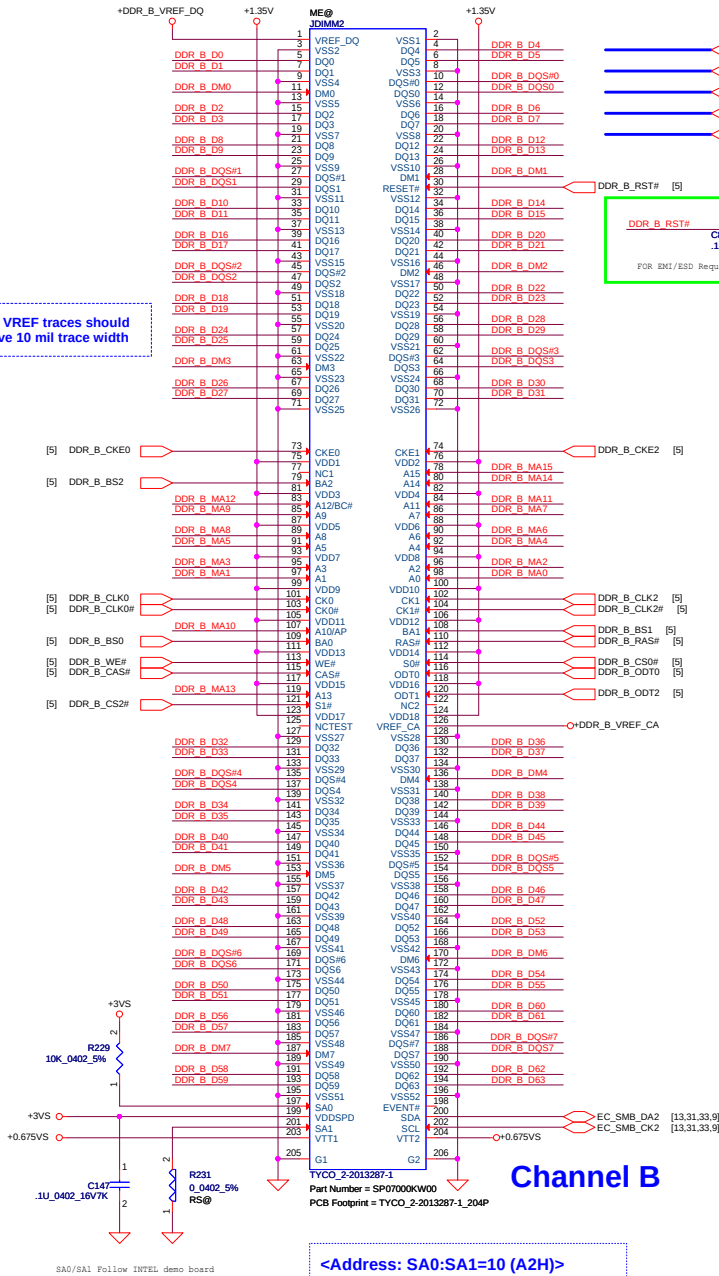
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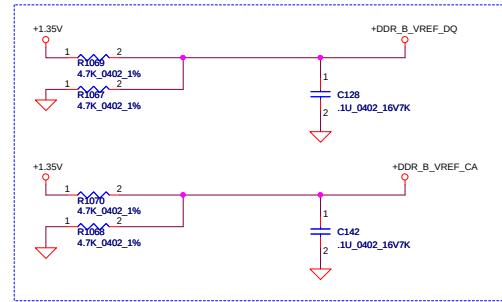
All VREF traces should
have 10 mil trace width



Layout Note:
Place near JDIMM2.203,204

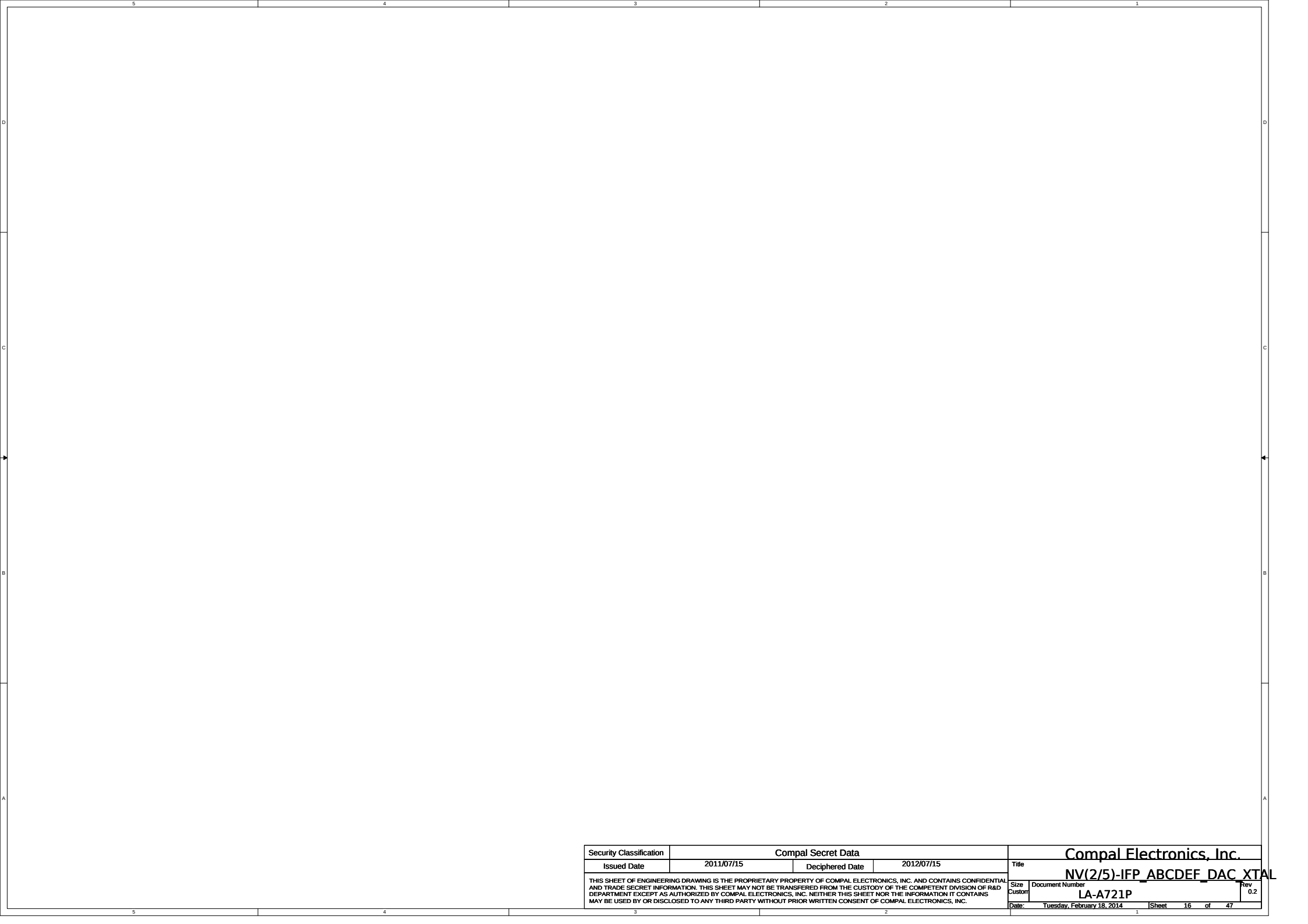


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DIMM_2 REV H:4mm



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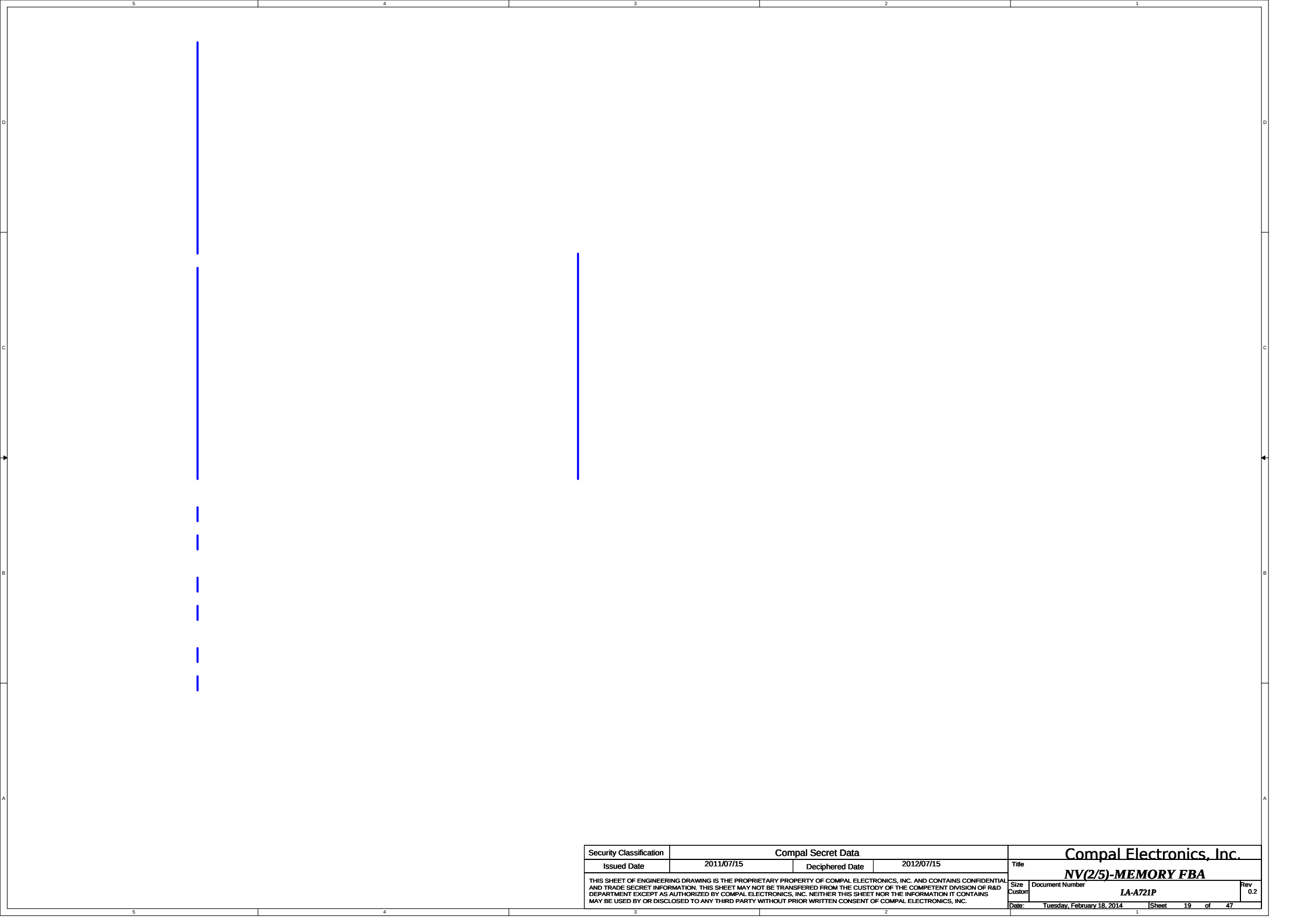


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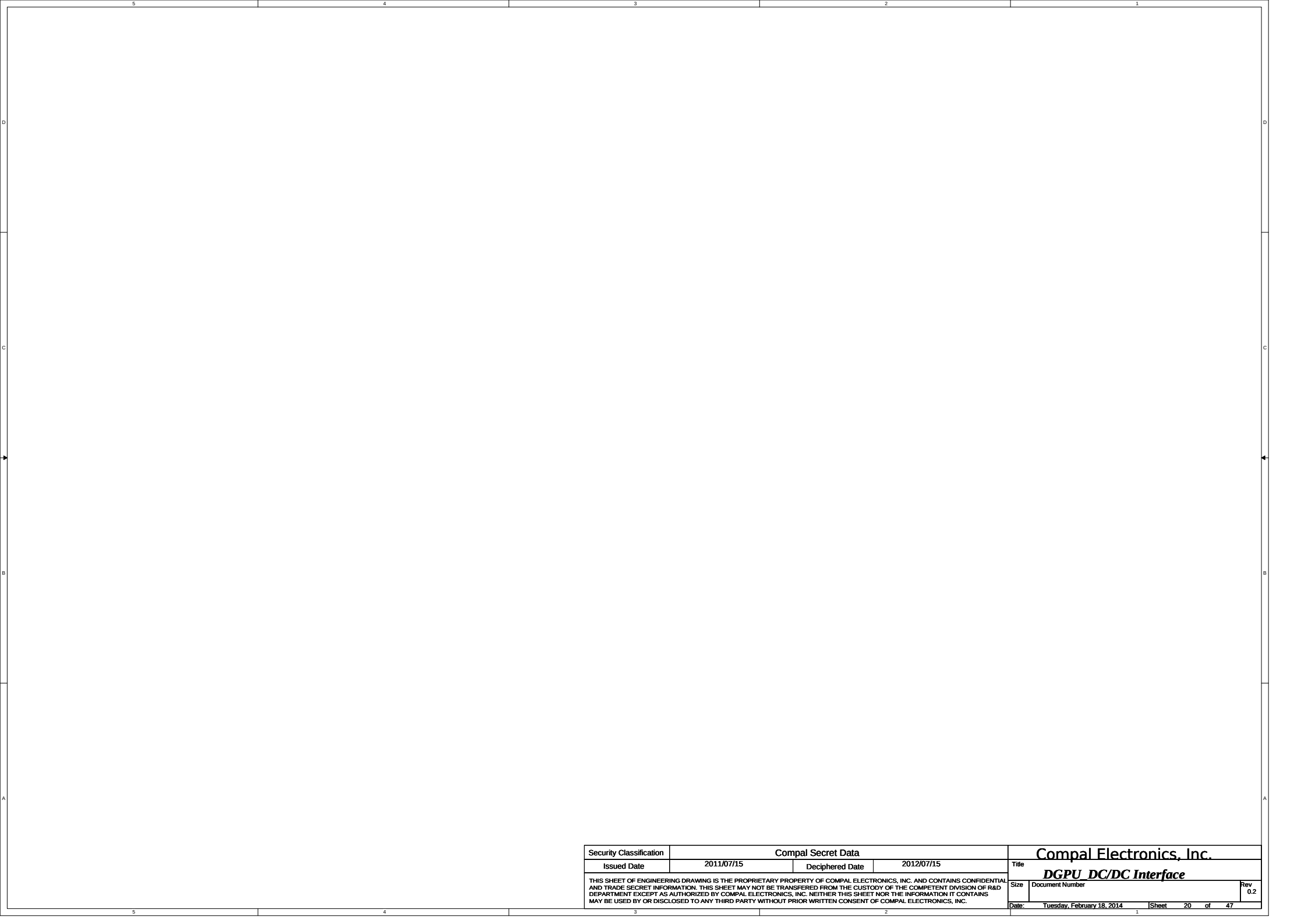
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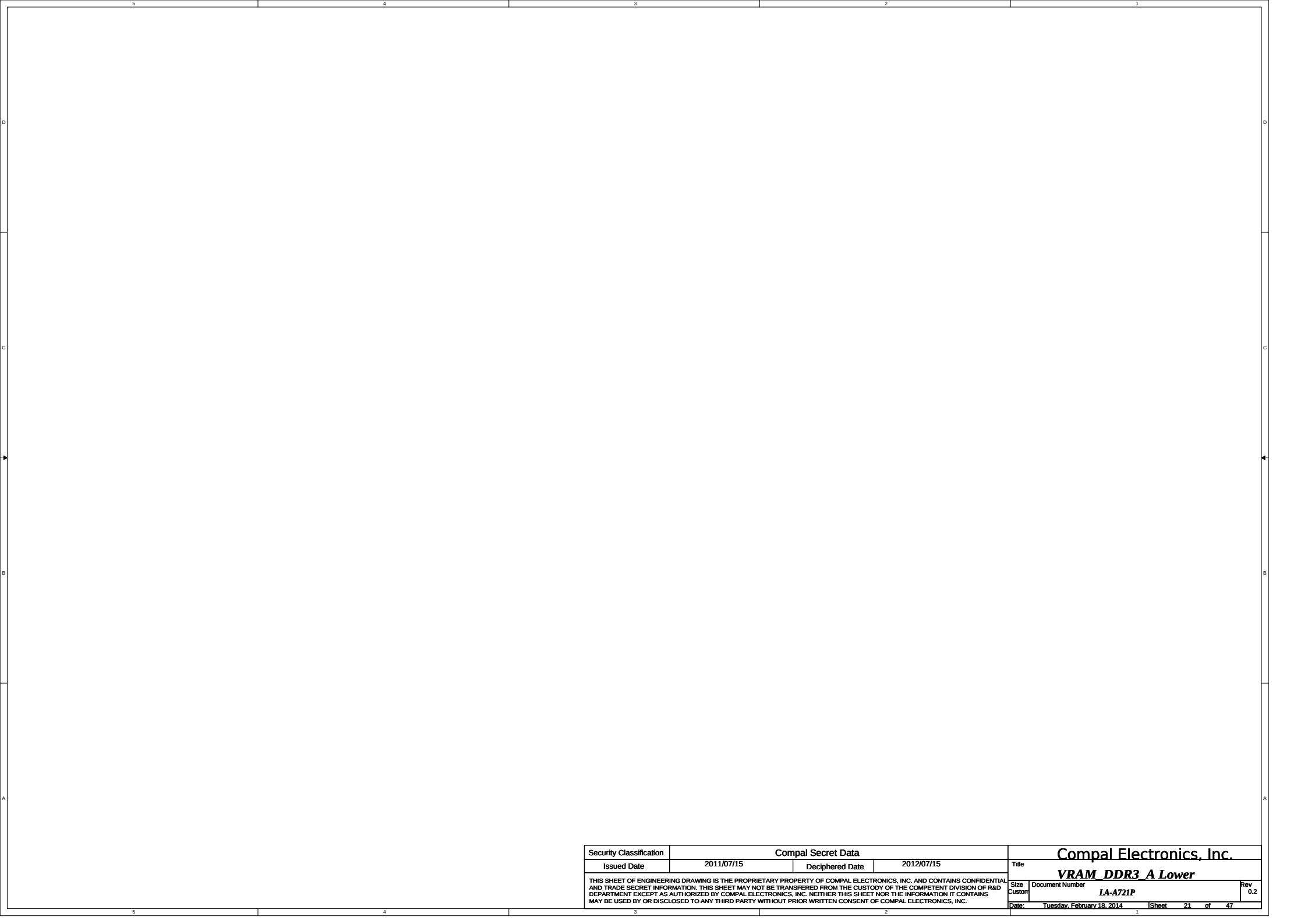
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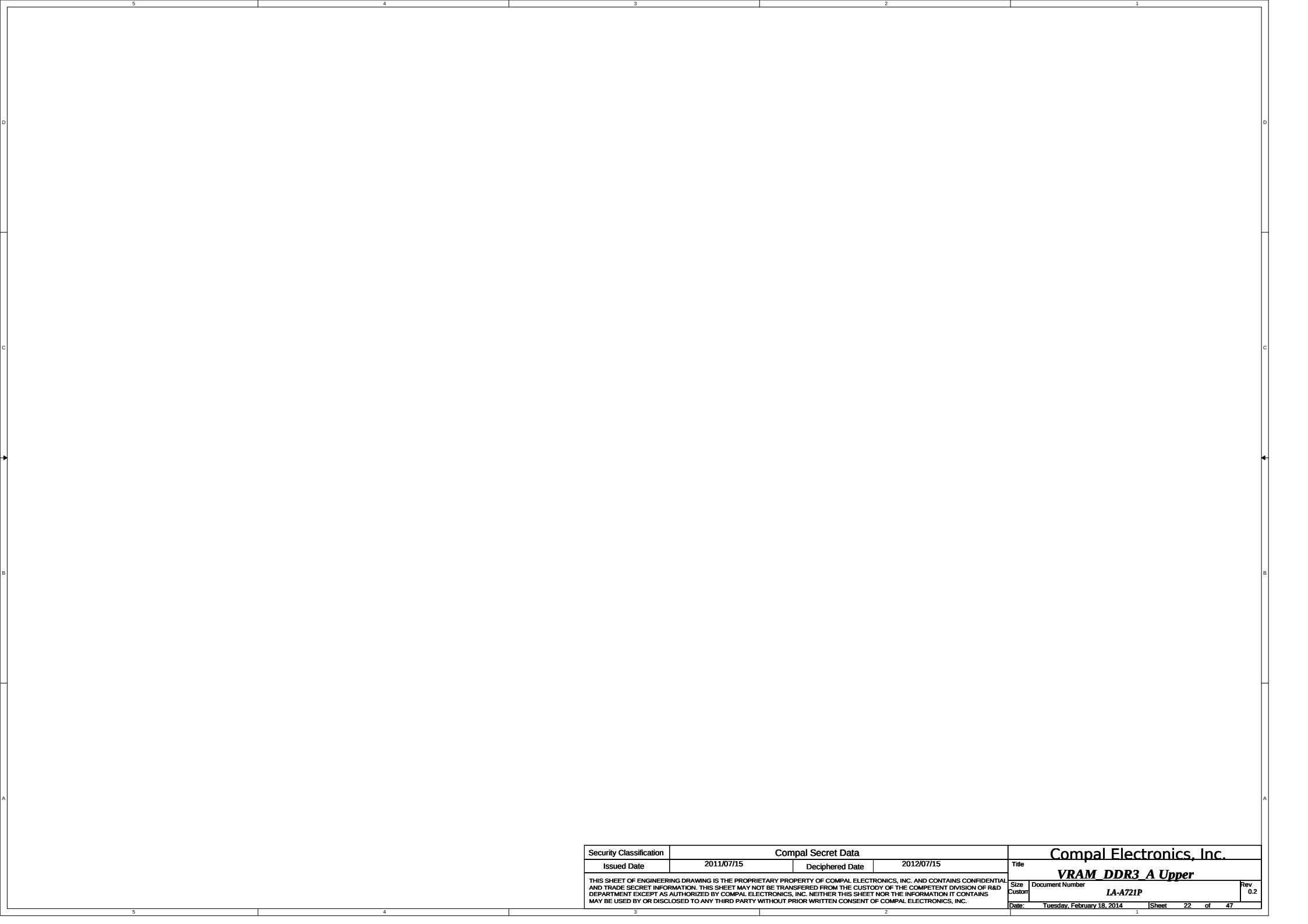
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				Rev	0.2
Date: Tuesday, February 18, 2014		Sheet 20 of 47			

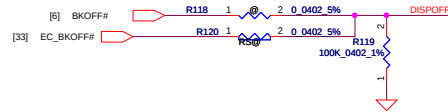
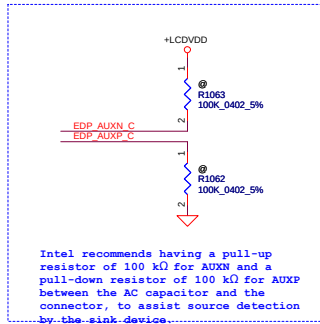
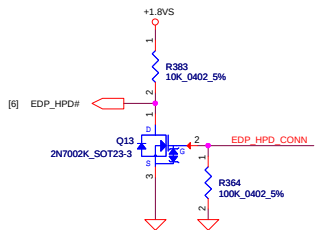
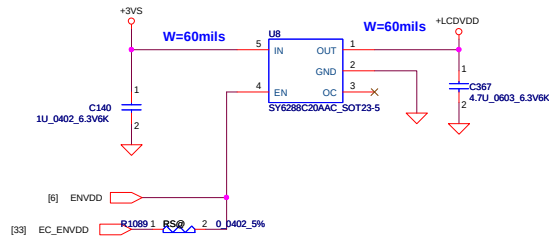


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				Date: Tuesday, February 18, 2014	Rev 0.2
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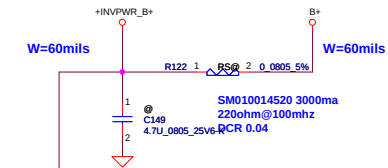


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				Date: Tuesday, February 18, 2014	Sheet 22 of 47

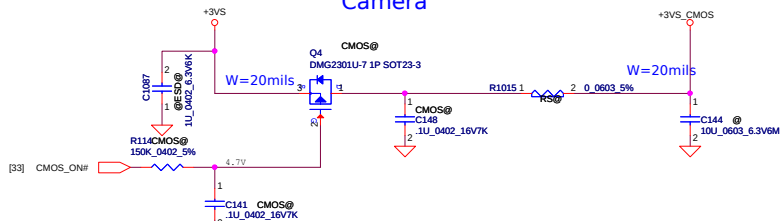
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LCD/ LED PANEL Conn.

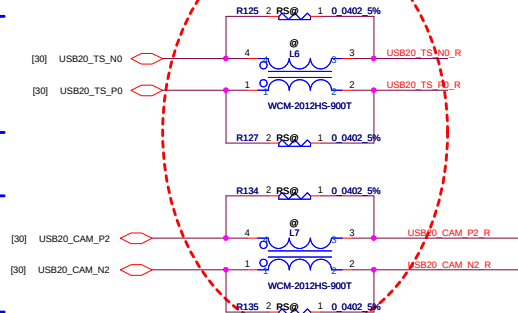


Camera



Camera

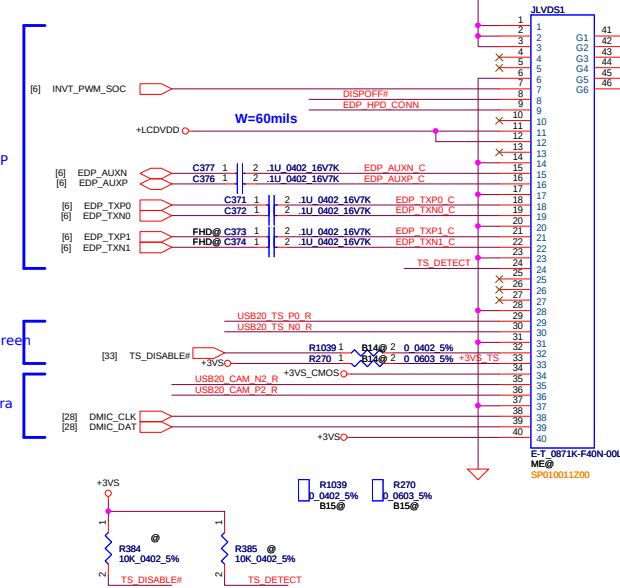
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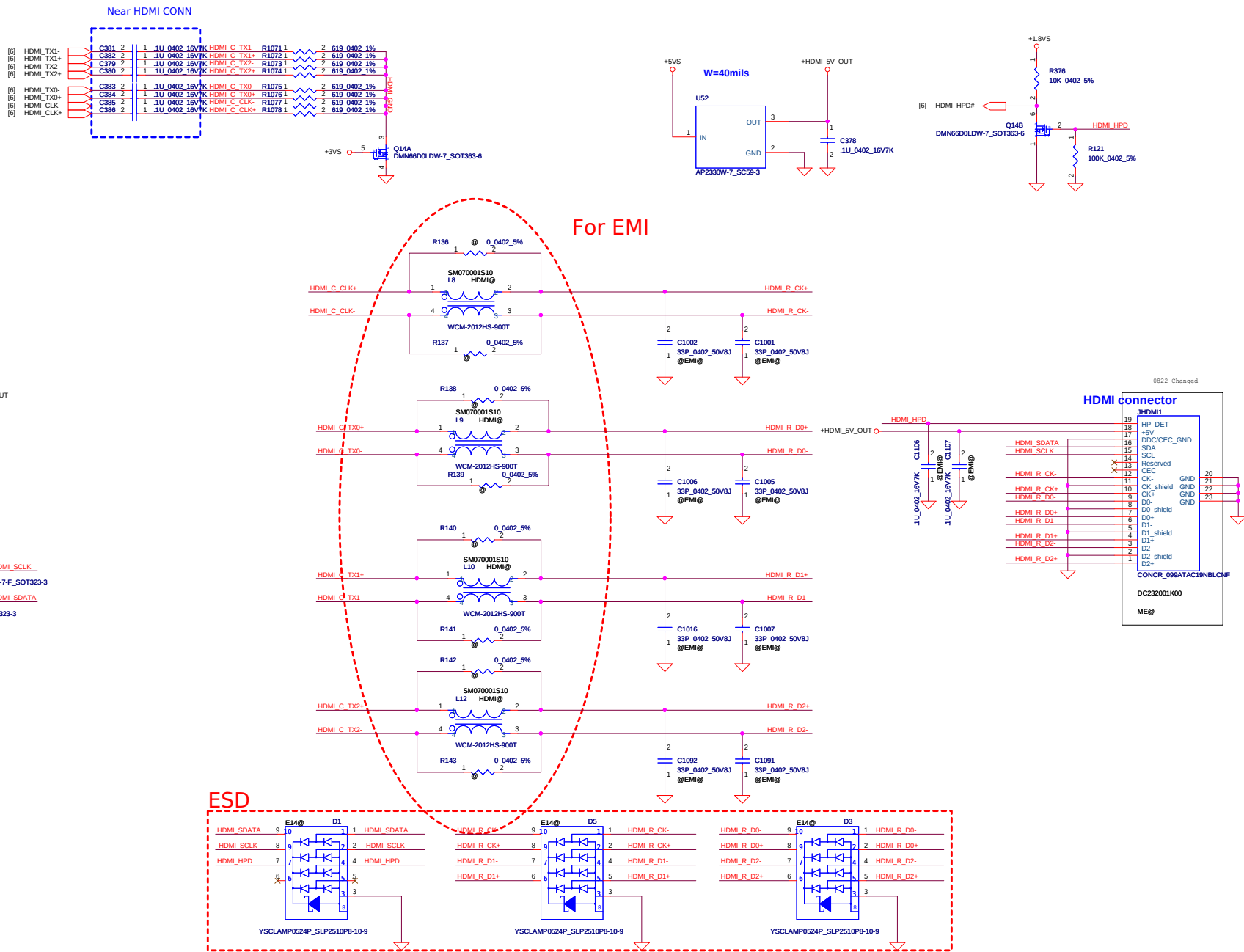
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Touch Screen

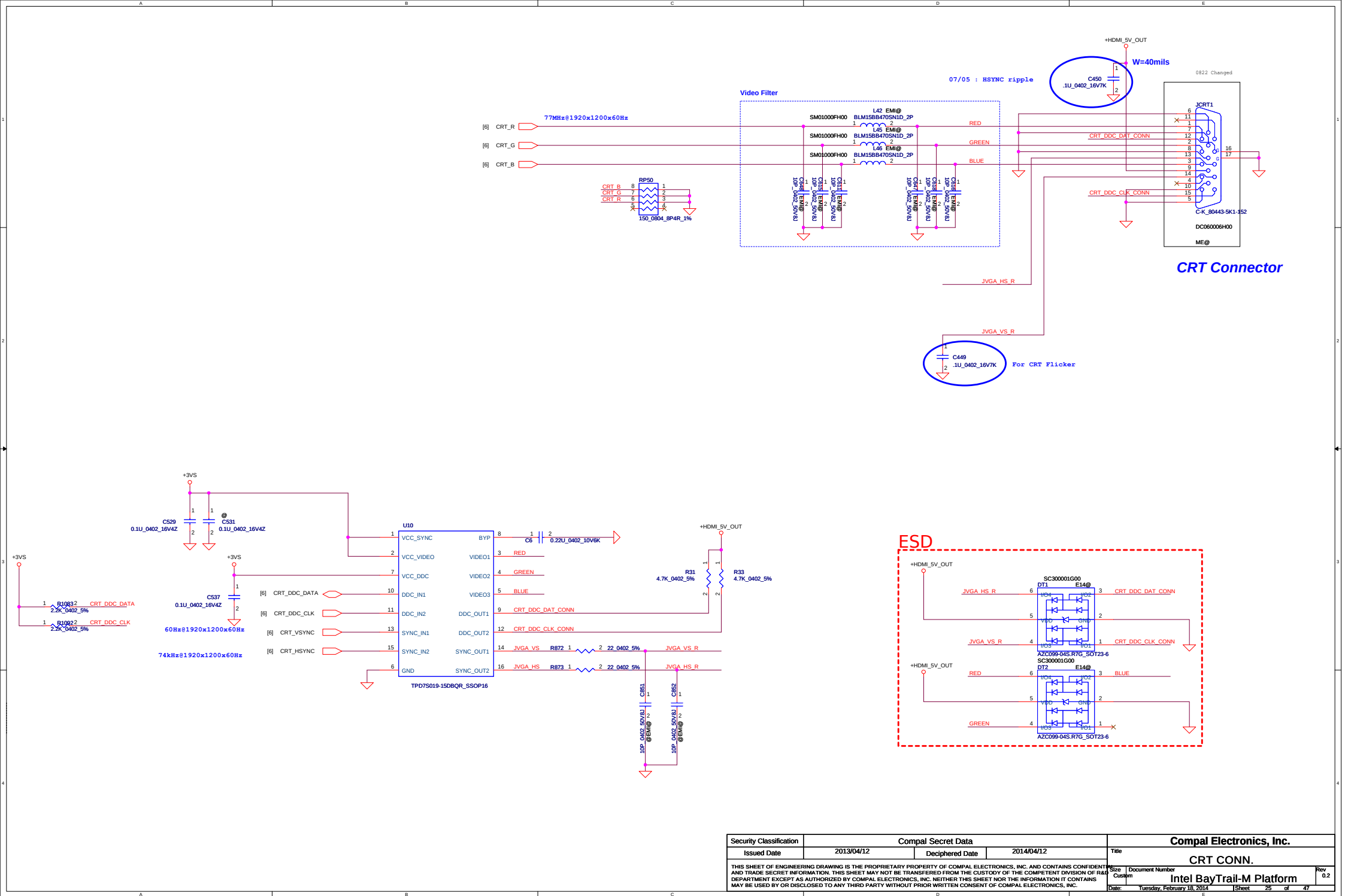
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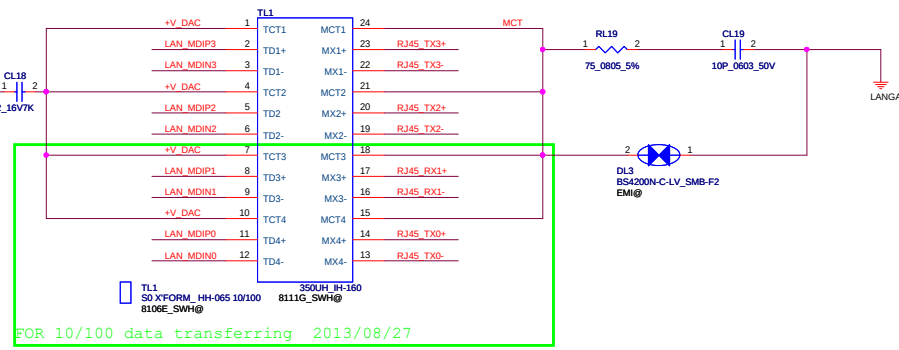
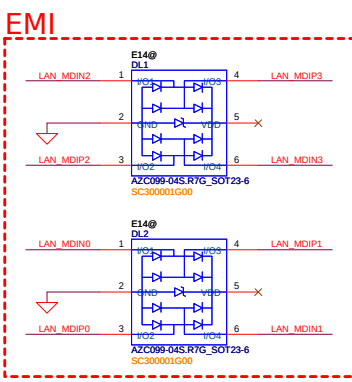
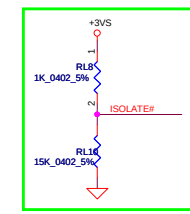
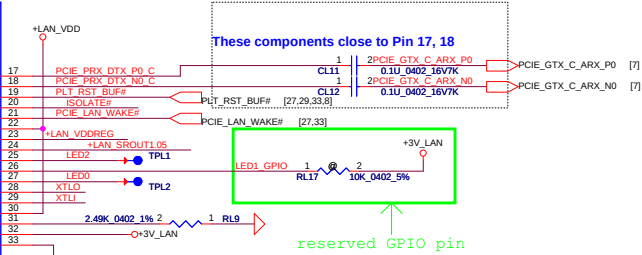
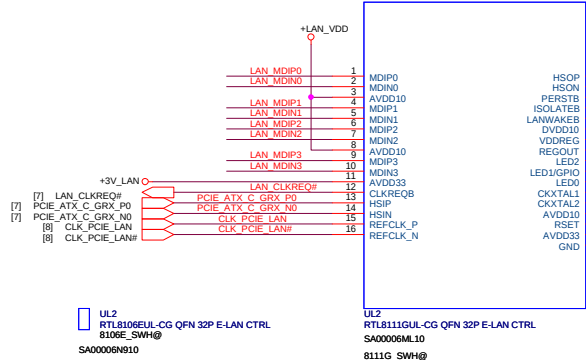
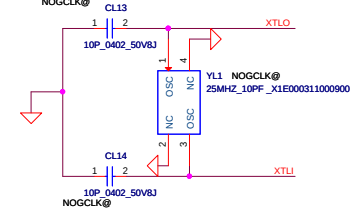
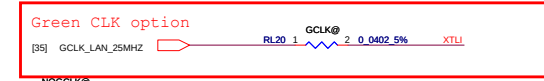
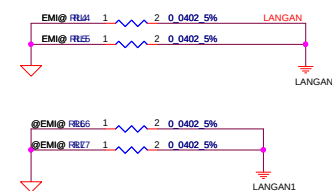
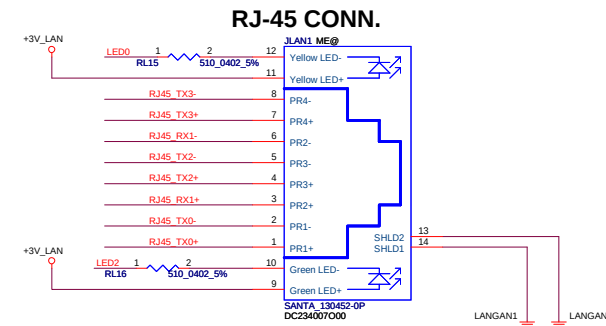
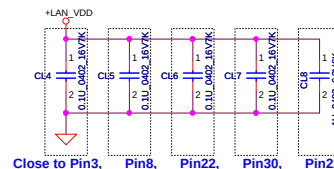
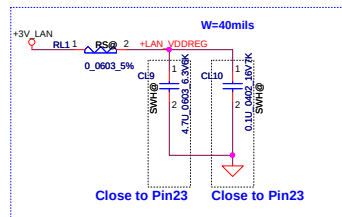
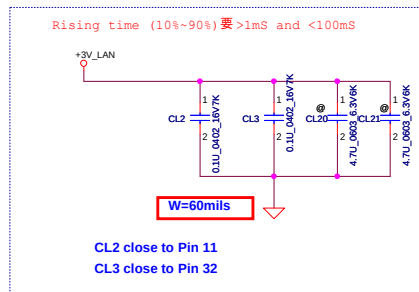
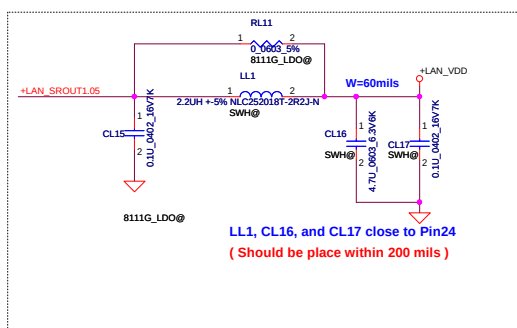
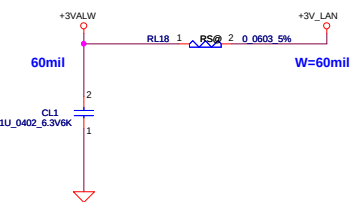


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Size		Document Number	Customer		Rev	
Date		Intel BayTrail-M Platform	Sheet		23 of 47	
Date		Tuesday, February 18, 2014	Sheet		23 of 47	



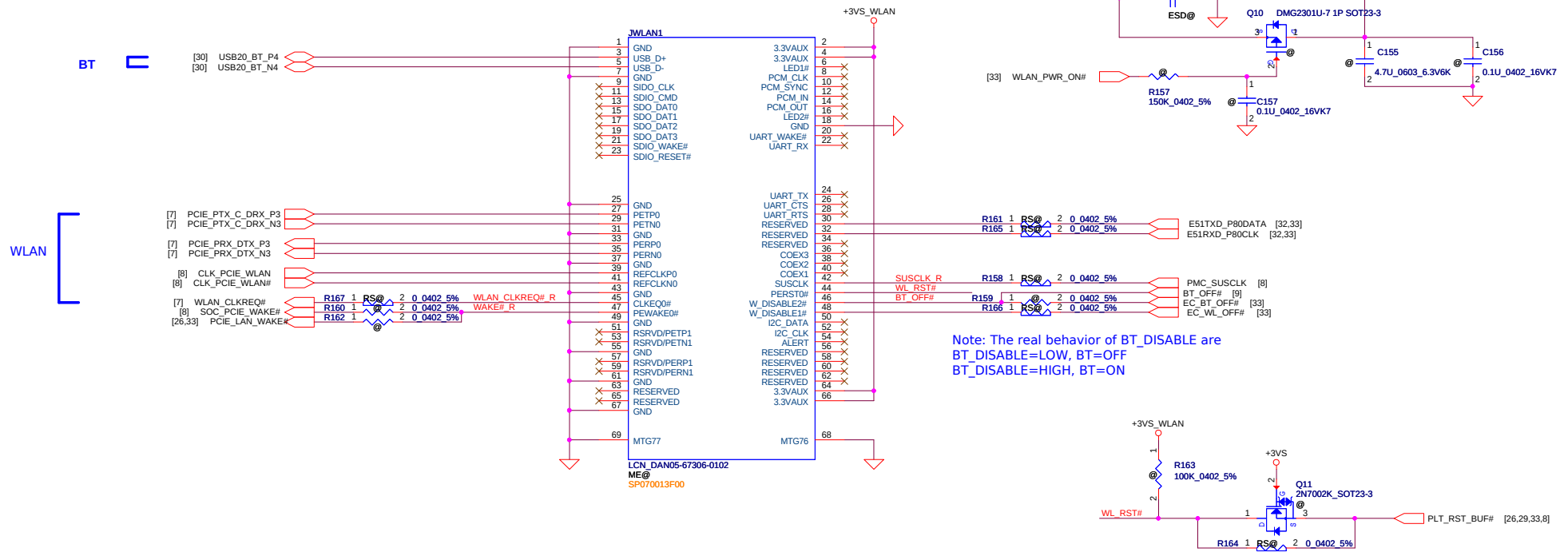
Security Classification			Compal Secret Data		Compal Electronics, Inc.	
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				Custom	Intel BayTrail-M Platform	0.2
				Date:	Tuesday, February 18, 2014	Sheet 24 of 47



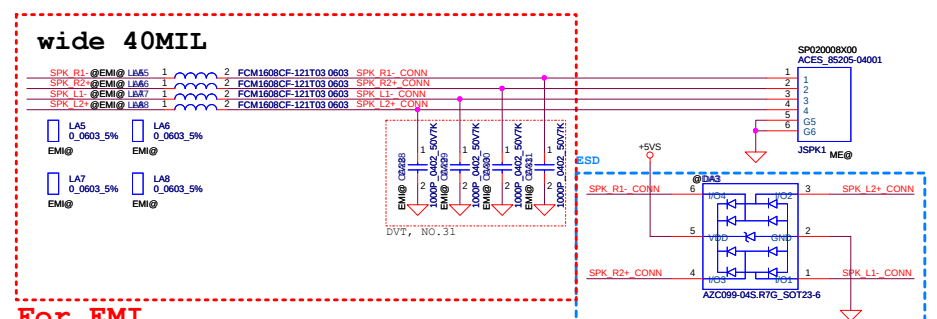
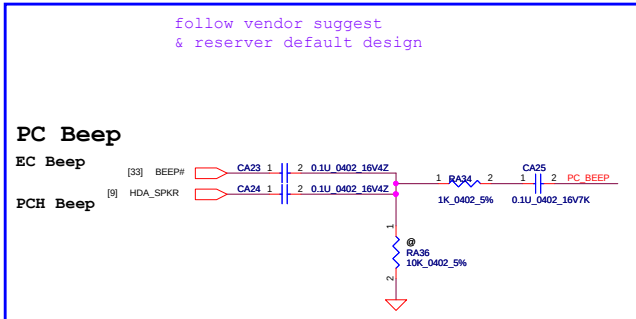
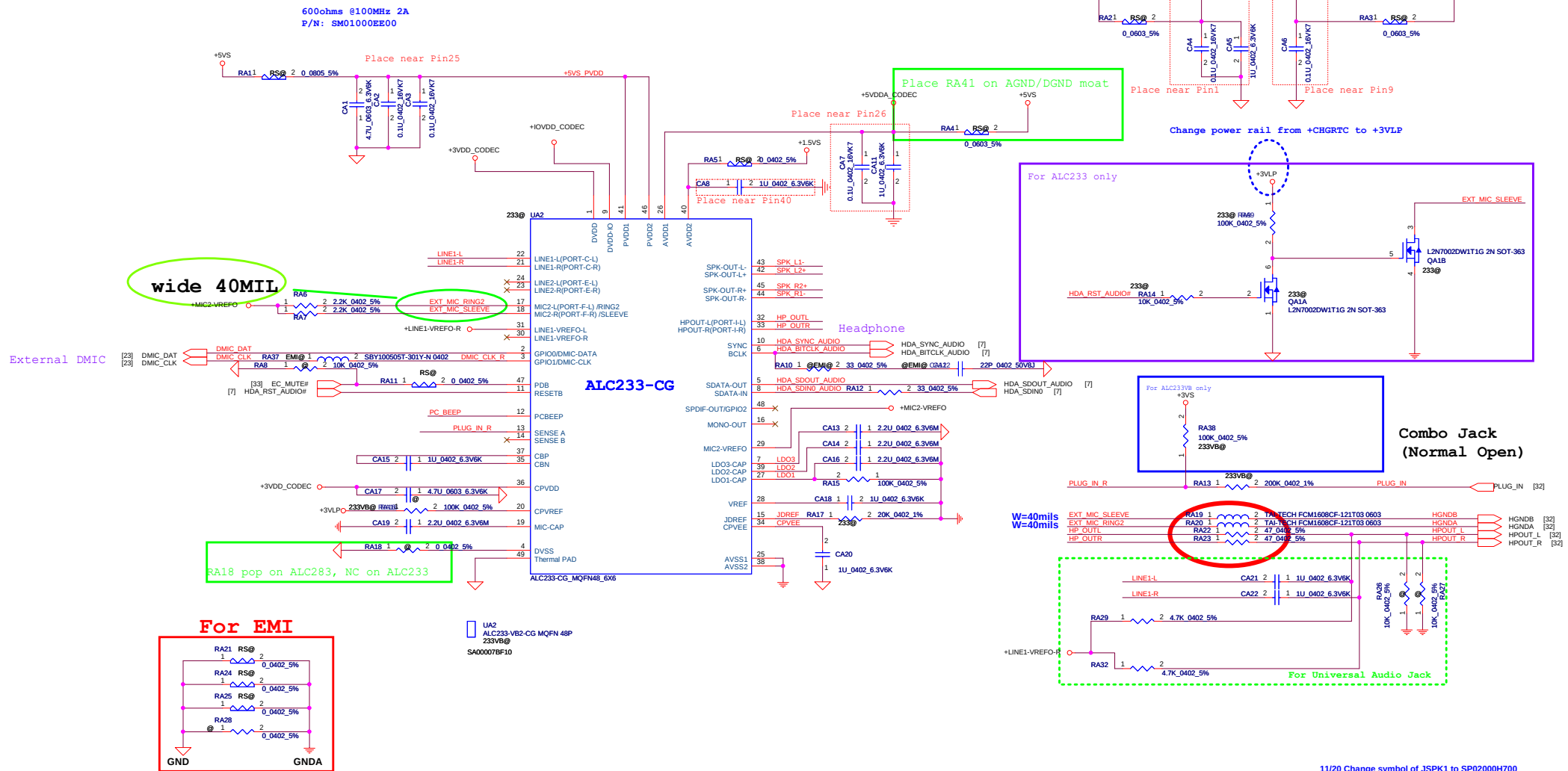


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				Custom	Intel BayTrail-M Platform	0.2
				Date:	Tuesday, February 18, 2014	Sheet 26 of 47

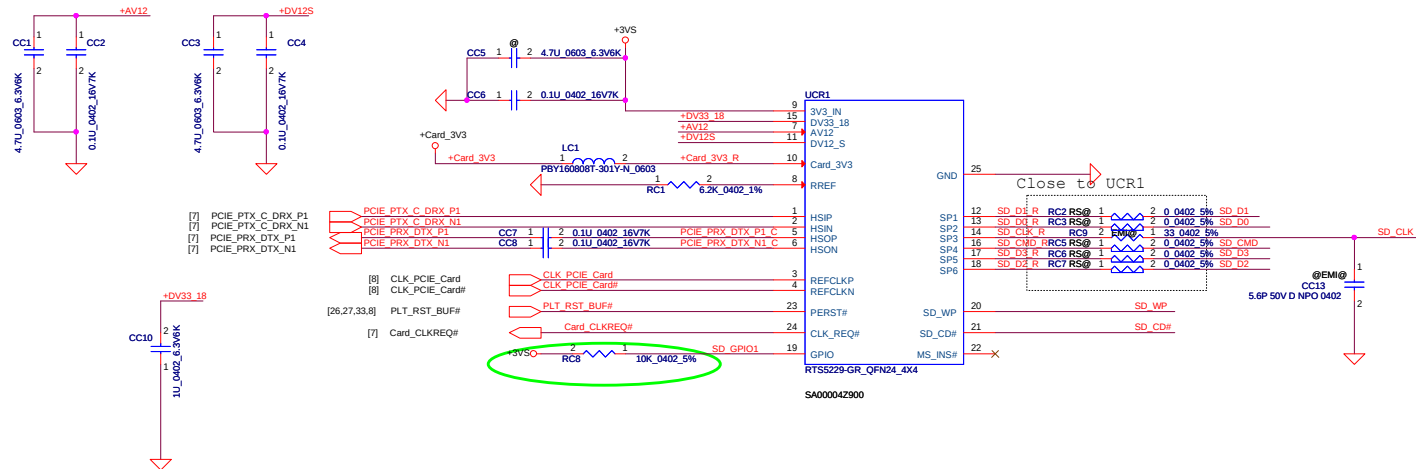
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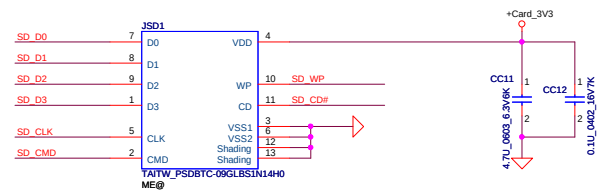
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Issued Date	2013/04/12	Deciphered Date	2014/04/12	Title	Mini PCIE(WLAN)
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				Document Number	Intel BayTrail-M Platform
				Rev	0.2
				Date:	Tuesday, February 18, 2014
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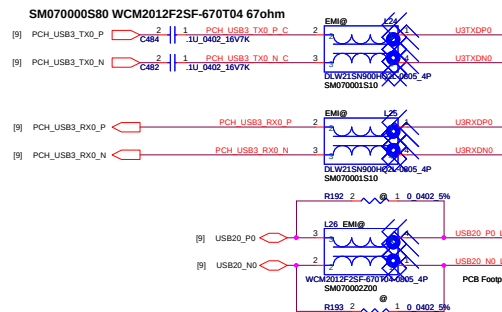
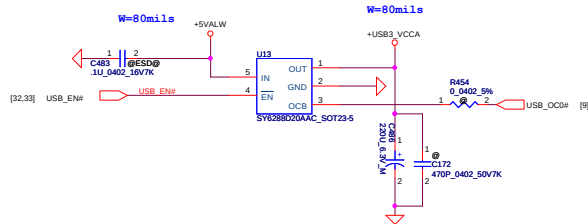
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Date	Rev
				Tuesday, February 18, 2014	02
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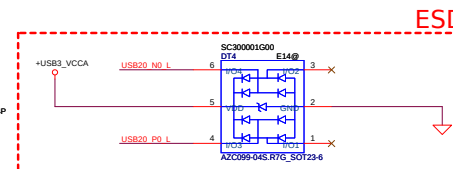
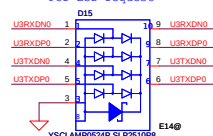
SD/SDXC



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Date: Tuesday, February 18, 2014				Sheet 29	of 47

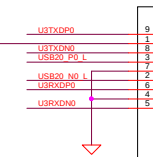


For ESD request

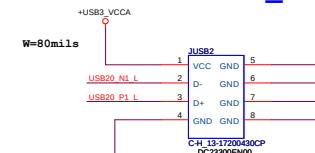
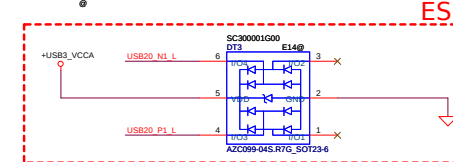
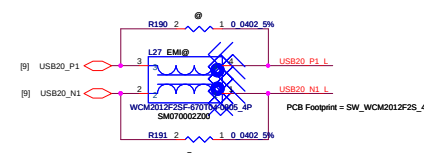


USB3.0_Port

USB3.0 Conn.

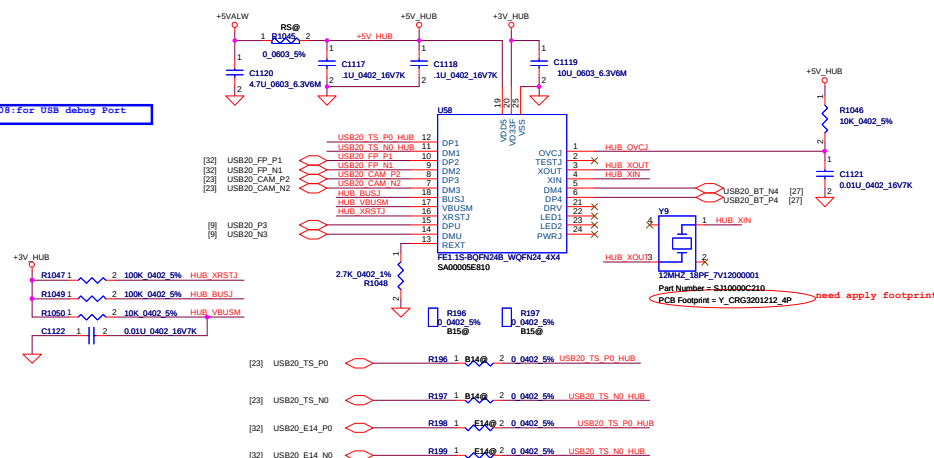


USB2.0_Port



USB2.0 HUB

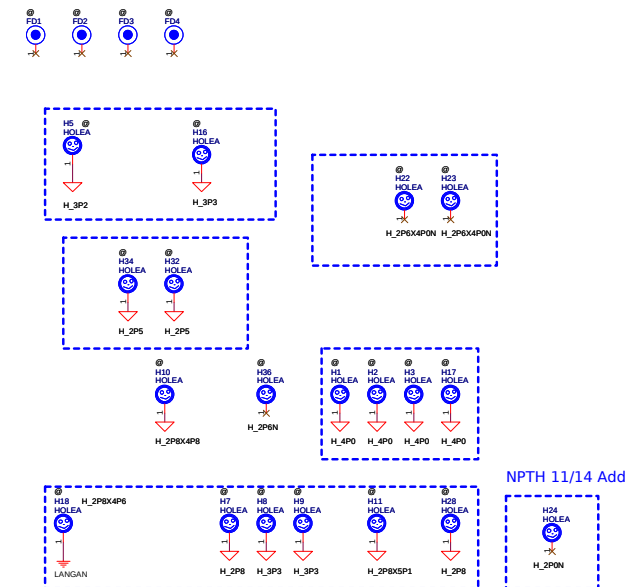
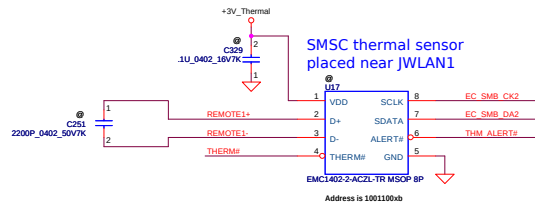
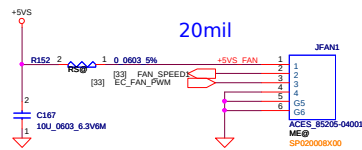
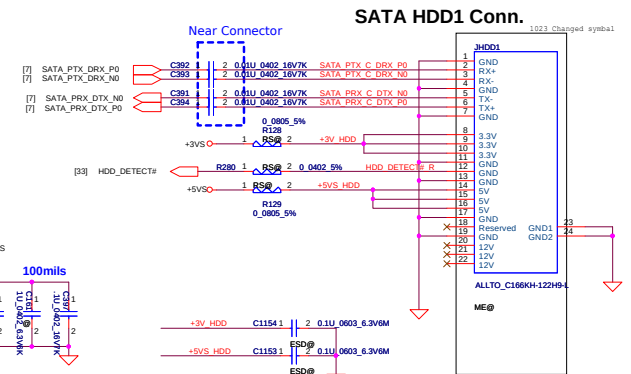
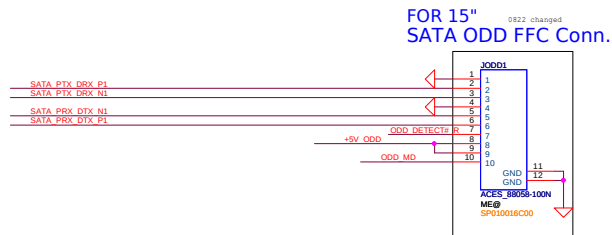
0708: for USB debug Port



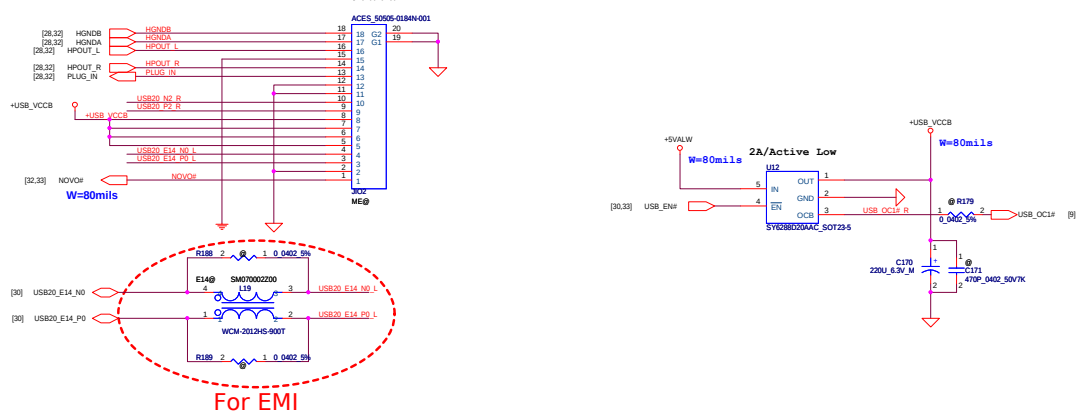
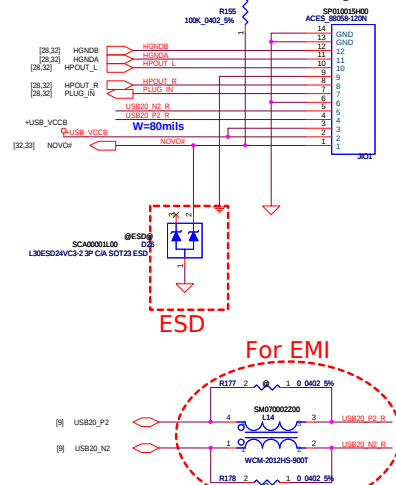
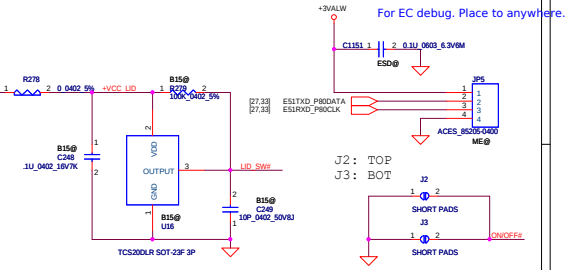
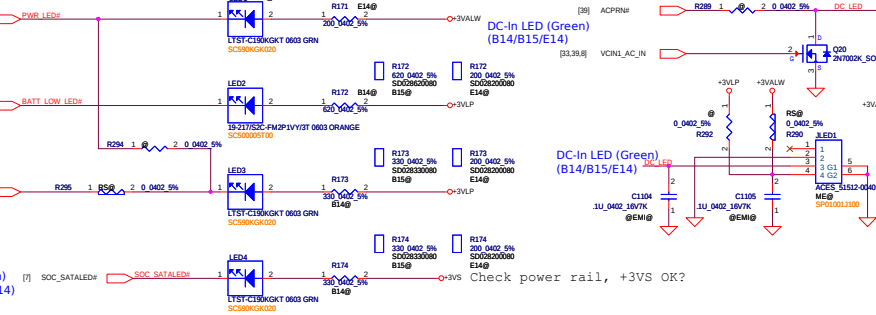
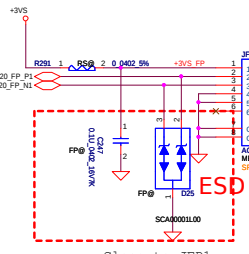
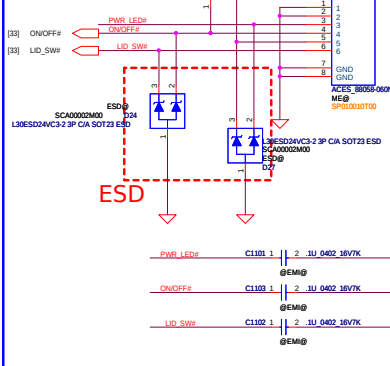
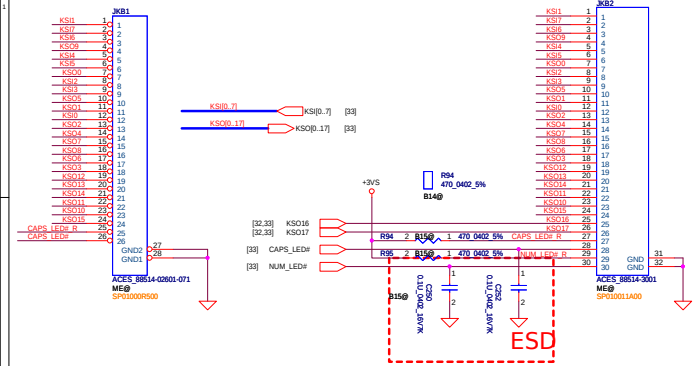
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Size	Document Number	Intel BayTrail-M Platform		Rev	0.2
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FOR 14"

SATA ODD Conn.



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				Intel Bay Trail-M Platform	
Date	Document	Project	Sheet	1	of 2



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Issued Date	20130412	Deciphered Date	20140412	File
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Size	Doc Number		KB/TP/LD/TPM	
Intel BayTrail-M Platform				
Date	Thursday, February 20, 2014		Sheet	32 of 47

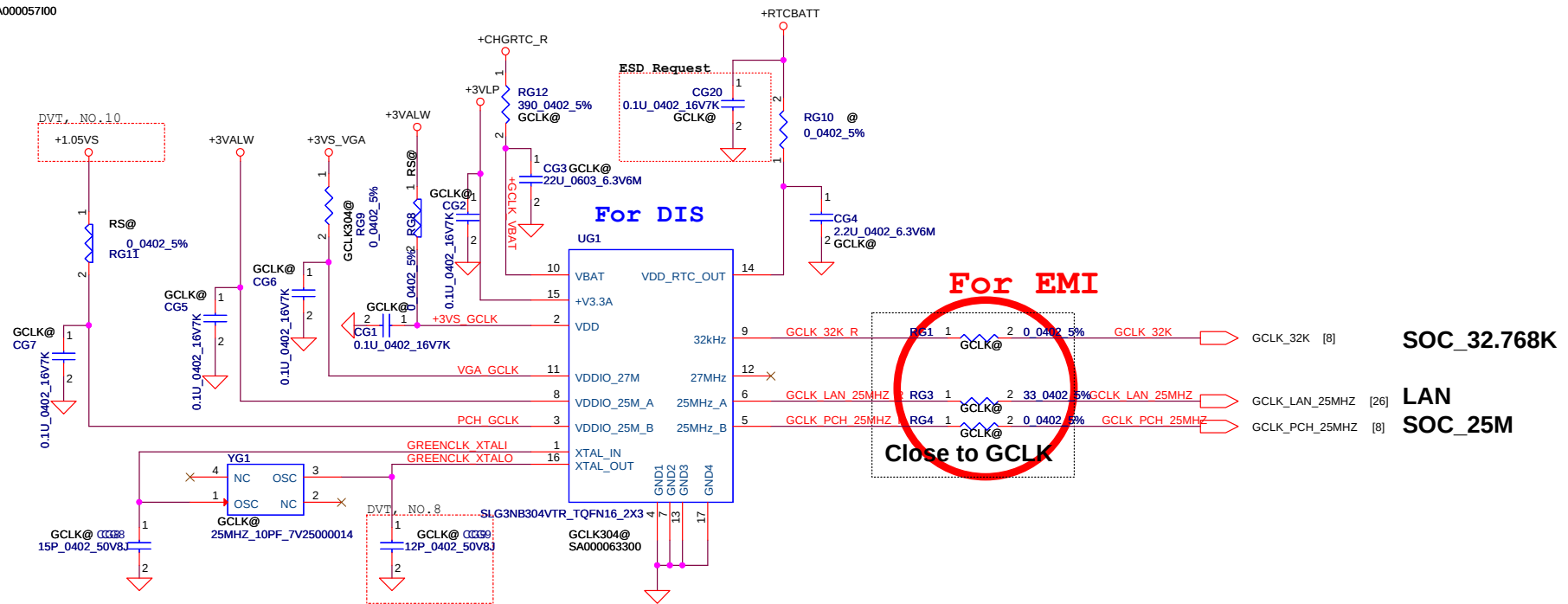
For UMA



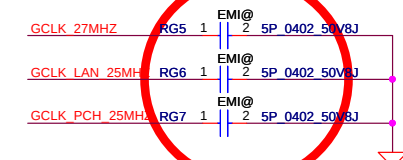
SLG3NB244VTR_TQFN16_2X3

SA000057100

Every power trace need:
W=20mils

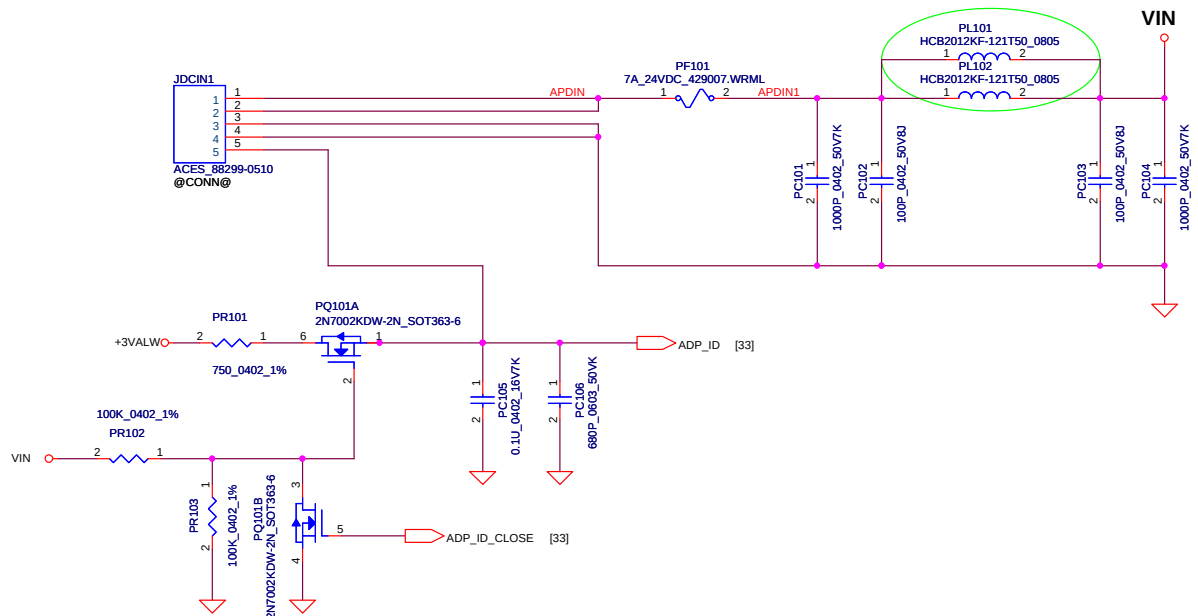


Reserved for Swing Level adjustment
(Close GCLK side)

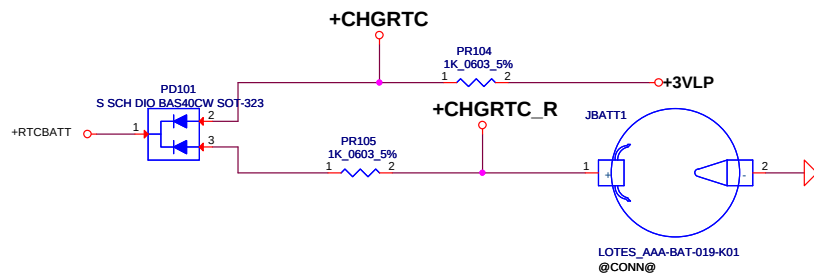


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5					4					3					2					1				
D																								
C																								
B																								
A																								

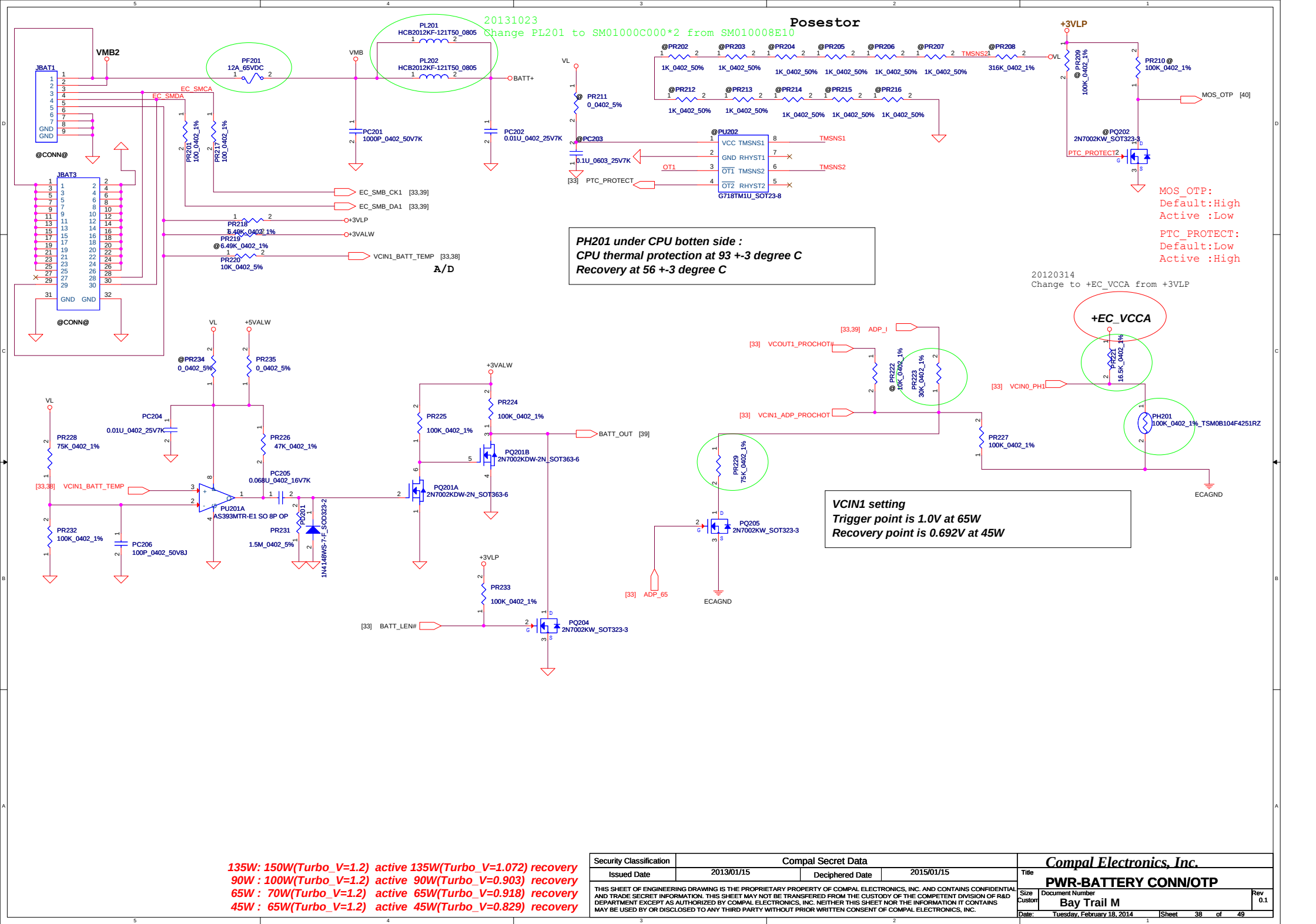


20131023
Change PL101 to SM01000C000*2 from SM010008E10



RTC Battery

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Date:				Sheet 37 of 49
Document Number				Rev 0.1
Custom				Bay Trail M



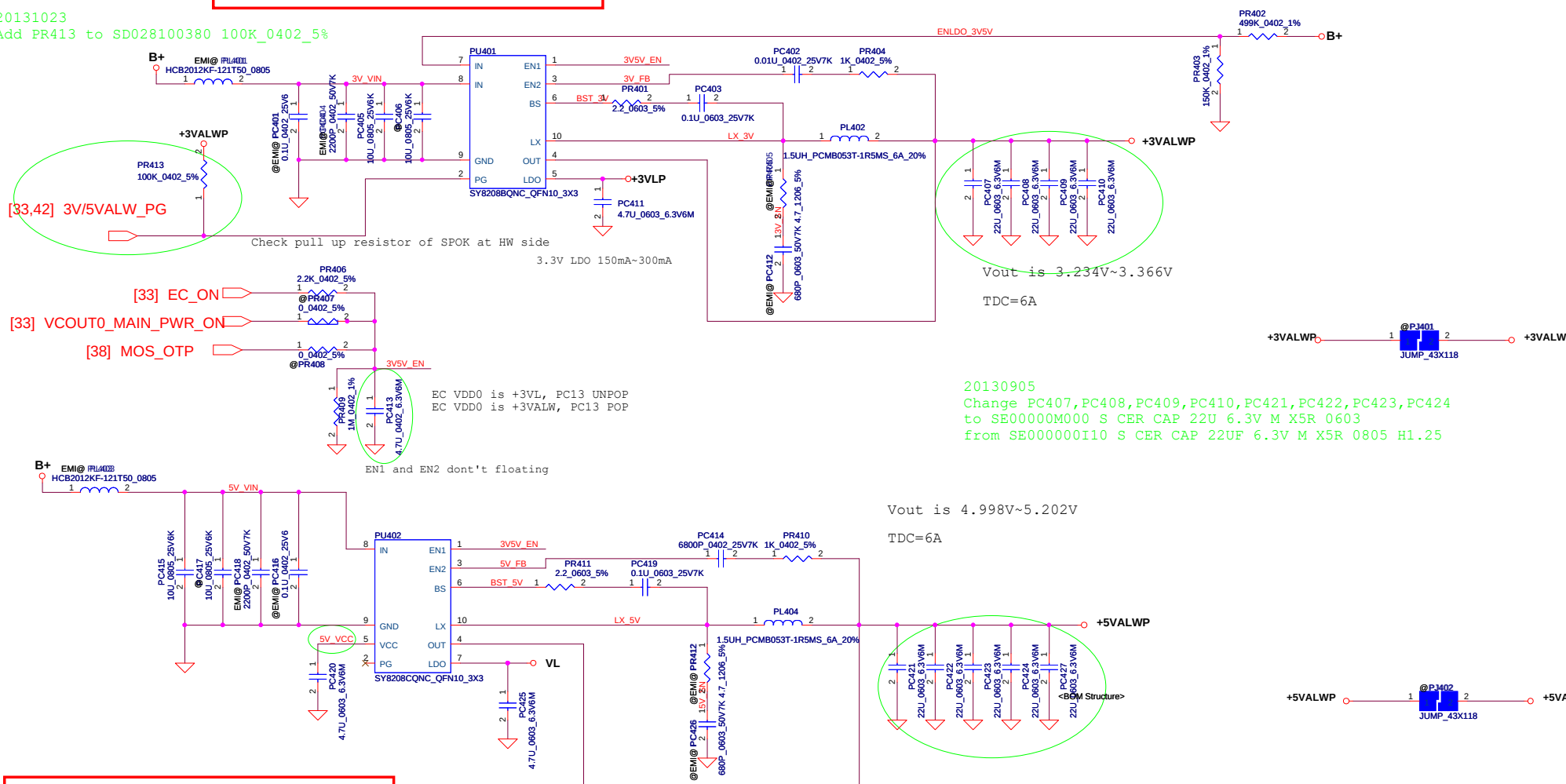
Module model information

SY8208B_V2.mdd

EN1 and EN2 don't floating

20130905
Change to 3V/5VALW_PG from SPOK

20131023
Add PR413 to SD028100380 100K_0402_5%



Module model information

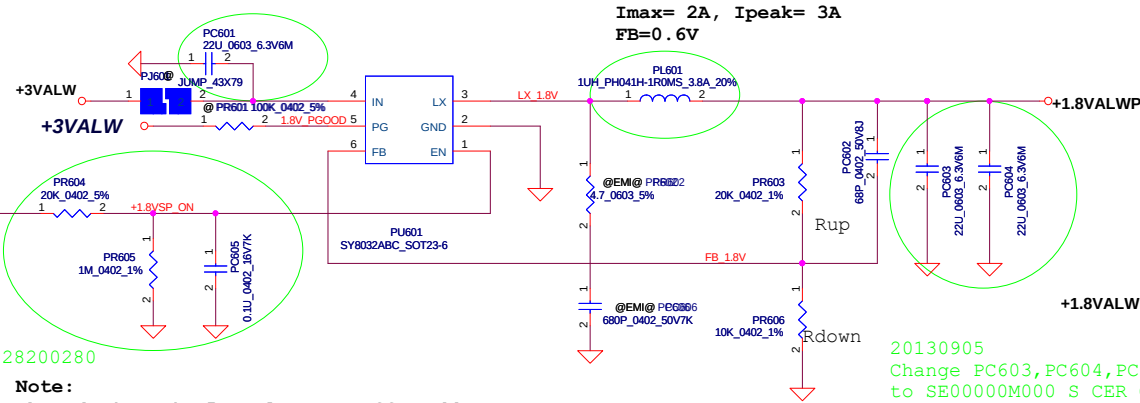
SY8208C_V2.mdd

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Module model information

SY8032_V1.mdd

20130913
Need to change PC702 to 0603 from 0805



20130905
Change to 3V/5VALW_PG from SPOK

20130924
Change PR604 to 20K SD028200280
Pop PC605 to 0.1u

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

$$V_{out}=0.6V* (1+R_{up}/R_{down})$$

20130905
Change PC603, PC604, PC617, PC618
to SE00000M000 S CER CAP 22U 6.3V M X5R 0603
from SE000000I10 S CER CAP 22UF 6.3V M X5R 0805 H1.25

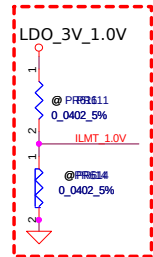
20130924
1. Change PR607 to 10K SD028100280
Pop PC607 to 0.1u_0402_16V7K SE076104K80

20130905
Change to 3V/5VALW_PG from SPOK

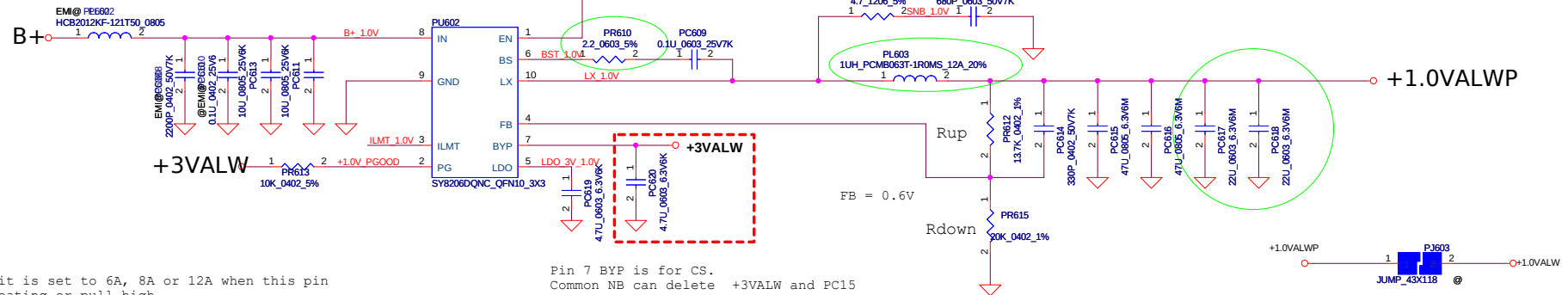
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

SY8206D_V1.mdd

Module model information



The current limit is set to 6A, 8A or 12A when this pin
is pull low, floating or pull high



Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

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				Document Number				Rev			
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								0.1			

Module model information

20130913
Need to change PC702 to 0603 from 0805

$I_{max}=2A$, $I_{peak}=3A$
 $FB=0.6V$

DIS:SY8003
UMA:SY8032

20130924
Change PR701 to 2.55k 1% SD034255180
Pop PC703 to 0.1u
unpop PR710

Note:
When design $V_{in}=5V$, please stuff snubber
to prevent V_{in} damage

$V_{out}=0.6V * (1+R_{up}/R_{down})$

20130905
Change PR702 to 75K SD034750280
PR705 to 100K SD034100380

20130905
Change PC701,PC703,PC704,PC711
to SE00000M000 S CER CAP 22U 6.3V M X5R 0603
from SE000000I10 S CER CAP 22UF 6.3V M X5R 0805 H1.25

change input cap from 0805 to 0603

2013/5/13
Change PR714 from 100kto 47k
Change PR720 from 47kto 100k

$V_{FB}=0.6V$
 $V_{out}=0.6V * (1+R_{up}/R_{down})$
 $V_{out}=1.011V$

Ultra Low Dropout 0.23V(typical) at 3A Output Current

2013/5/13
Change PR716 from 47kto 100k

20130924
Change PR706 to 51K SD028510280
Pop PC710 0.15U_0402_10V6K SE00000H300
unpop PR708

$V_{out}=0.8V * (1+R_{up}/R_{down})$
 $V_{out}=1.512V$

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Power module of ISL95833 VR
for 4.5W processor

PR15 and PR27
27.4K ohm for 100 degree
61.9K ohm for 110 degree

Alert assert
threshold: 100C

Close GFX choke

Close GFX L/S MOS

+3VALW

+5VALW

VR_Hot# assert
threshold: 100C

+1.0VS

+1.0VALW

Close CPU L/S MOS

Close CPU choke

SOC_VNN OCP is around 21A
SOC_VCC OCP is around 19A

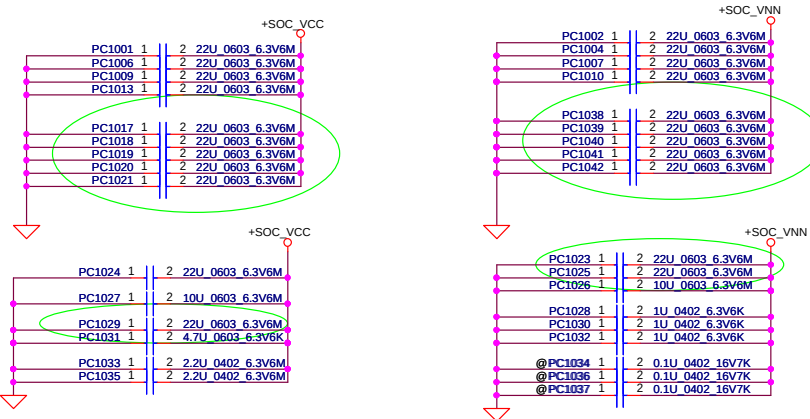
20130905

1. Del PC940 33U 25V_M
2. Change PC939 to 68U 25V_M R0.36 SF000000W00
From 33U 25V_M SF000005200

0.22uH DCR= 0.97+-5% m ohm, Idc~Isat= 25~34A

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22uF 0805 size change to 0603



Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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