

LCFC Confidential

GS454/GS554(NMD031) MB Schematics Document


ICL U42 with DDR4 + Nvidia N16V-GM

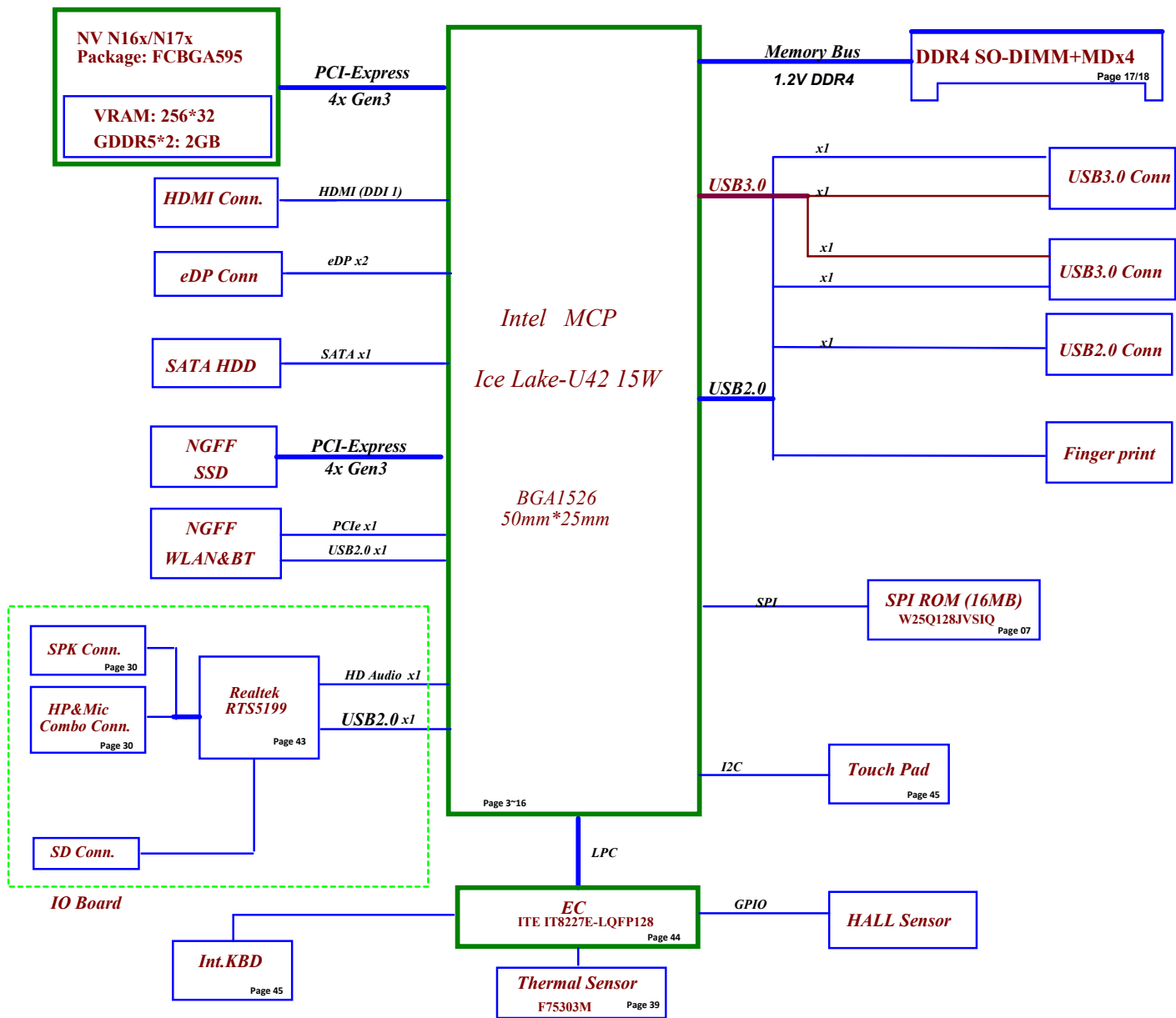
2019-10

REV: 0.1

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Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	Cover Page	
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Voltage Rails (O --> Means ON , X --> Means OFF)

<div>Power Plane</div> <div>State</div>	V9B+	+3VALW +5VALW +3VALW_PCH +1.8VALW VCC_AUX	+1.2V +2.5V_DDR +VCCST +VCCSTG	+5VS +3VS +1.8VS +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8227E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DAI	IT8227E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK0 EC_SMB_DAI	IT8227E +3VS	X	X	V +3VG_AON	V +3VS	X	X	X	X	V	X
EC_SMB_CK3 EC_SMB_DAI	IT8227E +3VAWL	X	X	X	V	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	X

EC SMBus1 address EC SMBus2 address EC SMBus3 address PCH SM Bus address

Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	PMIC	need to update	DDR4 SODIMM	need to update
Charger	0001 0010 b	DGPU	need to update				

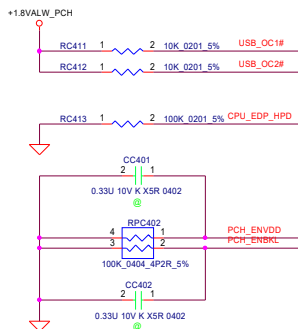
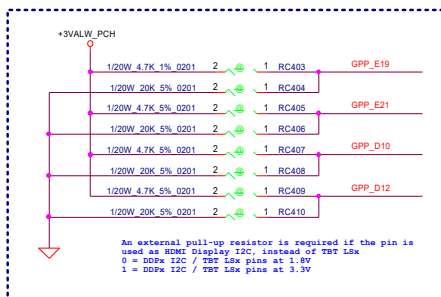
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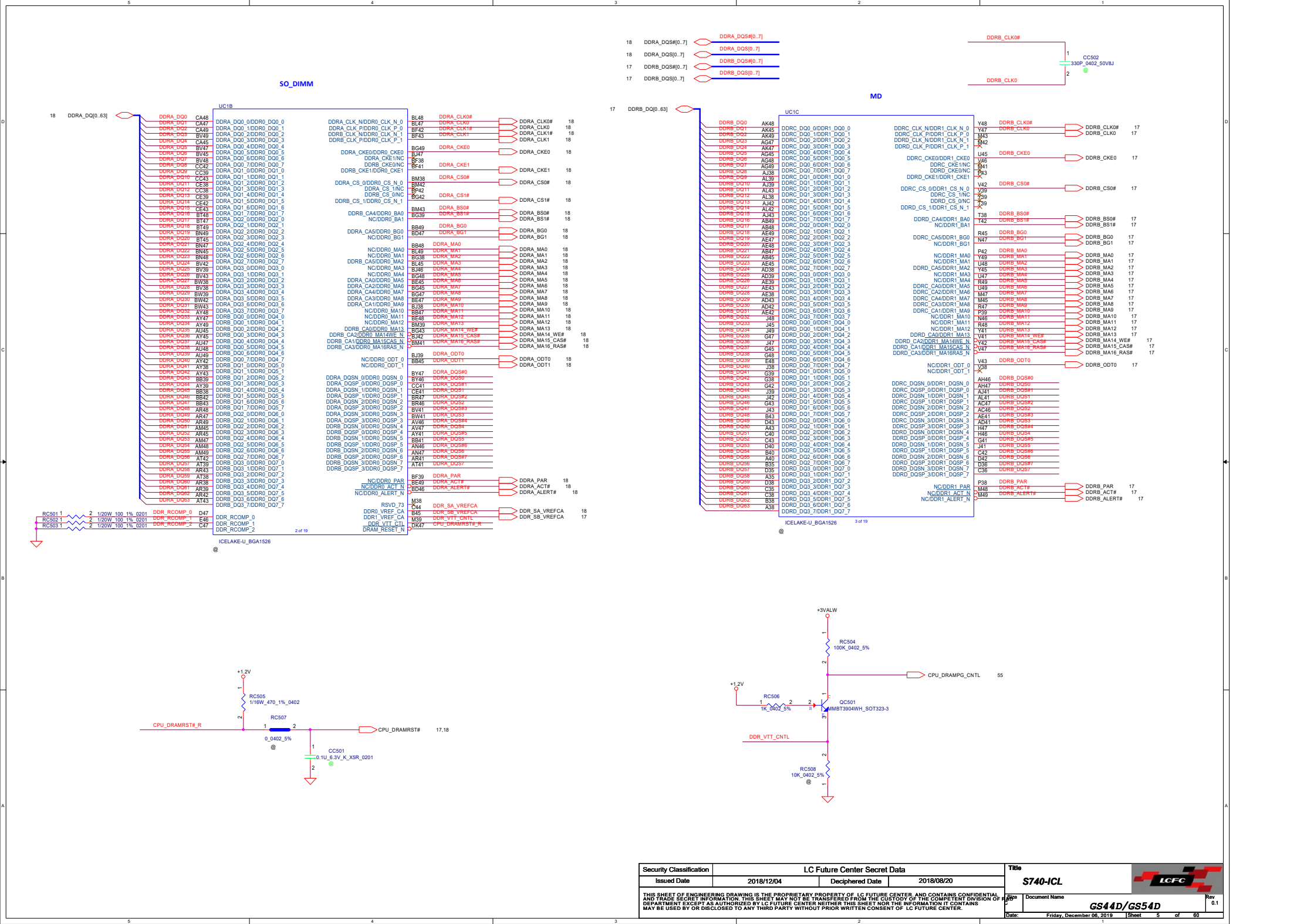
STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

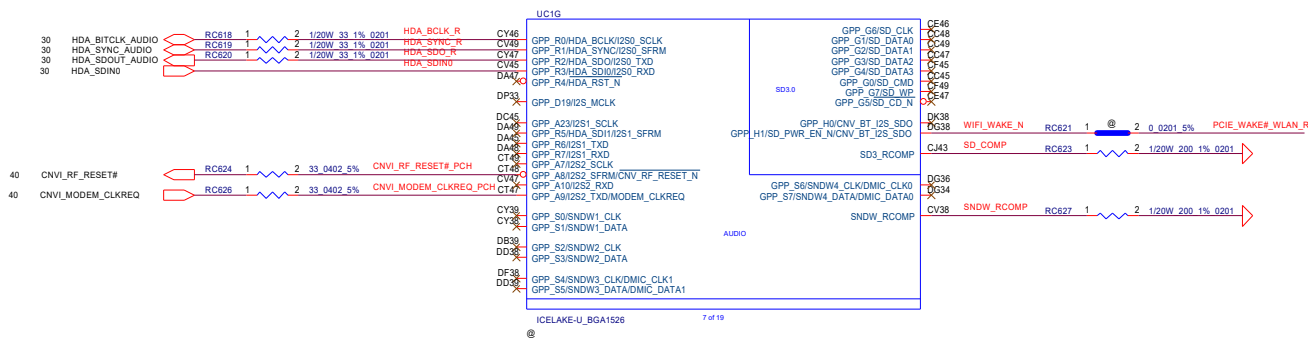
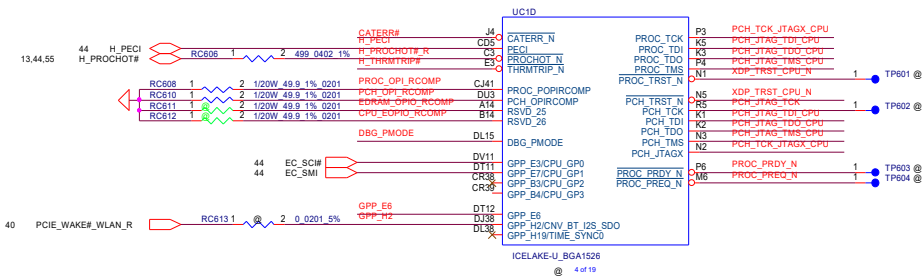
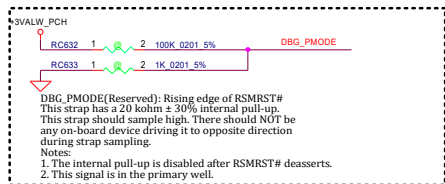
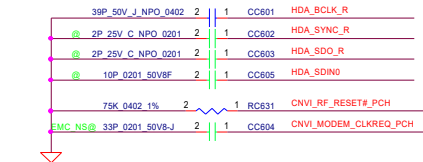
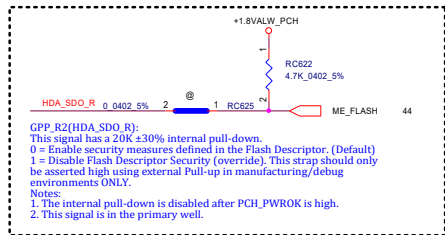
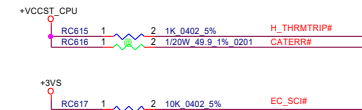
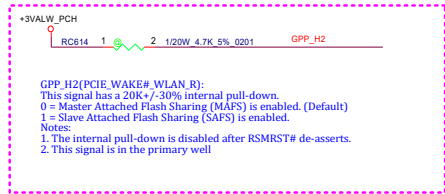
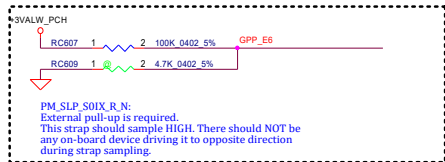
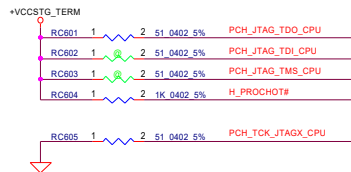
HSIO PORT	Function
USB3.0	1 USB3.0 Conn
	2 USB3.0 Conn
	3 NC
	4 NC
	5
	6
USB2.0	1 USB3.0 Conn
	2 USB3.0 Conn
	3 NC
	4 NC
	5 Camera
	6 Touch Screen
	7 Finger Print
	8 Card Reader
	9 USB2.0 conn
	10 Bluetooth
PCIE	5~8 X4 DGPU
	9 WLAN
	10 NC
	11 SATA HDD
	12 NC
	13~16 X4 PCIE/SATA SSD

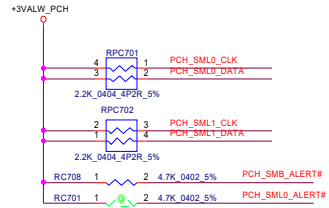
BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
CD@	For cost down
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
ME@	For ME part
UMA@	For UMA part
OPT@	For NV GPU part
OPTN16@	For NV N16S-GTR GPU part
OPTN17@	For NV N17S-G1 GPU part
TS@	For touch screen part
TP@	For TOuch Pad Part

GPIO Group	Power Supply
GPP_A	1.8V
GPP_B/C/D/E	3.3V
GPP_F	1.8V(only)
GPP_G/H	3.3V
GPP_R/S	1.8V
GPD	3.3V(only)



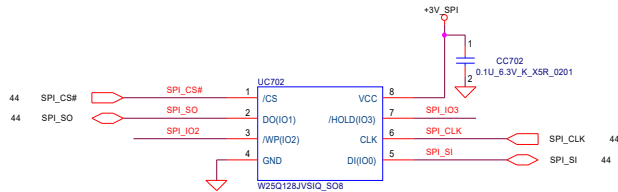
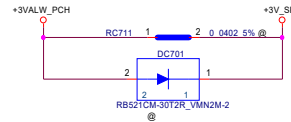
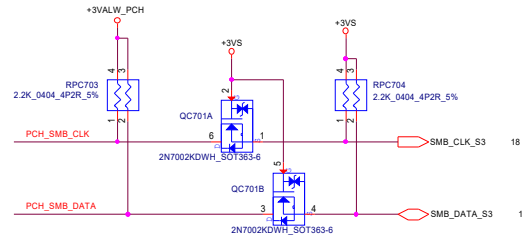
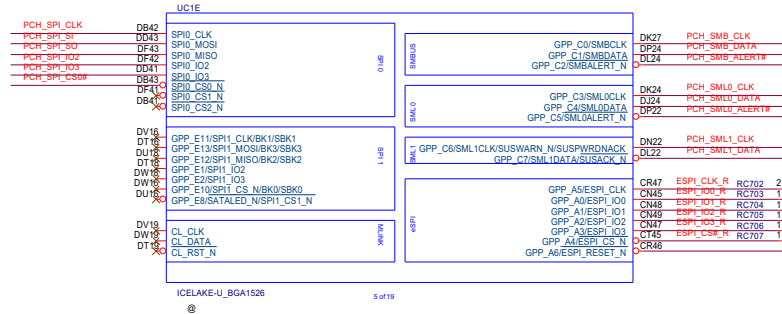
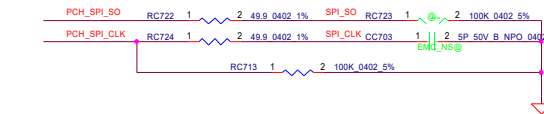
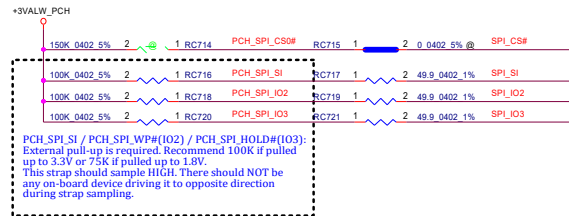
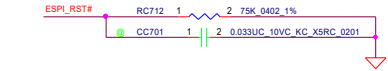
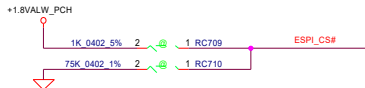


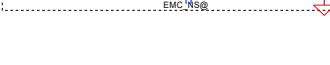
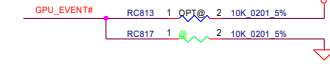
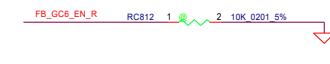
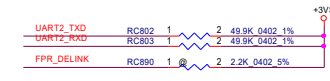
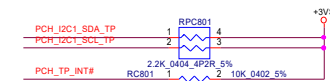
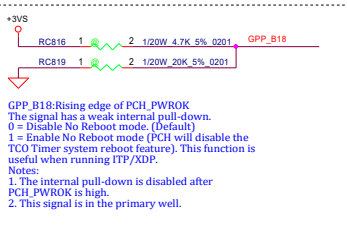
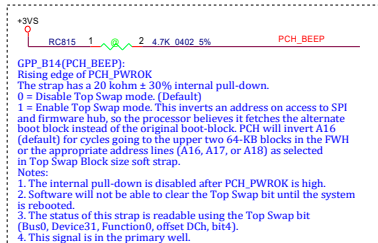
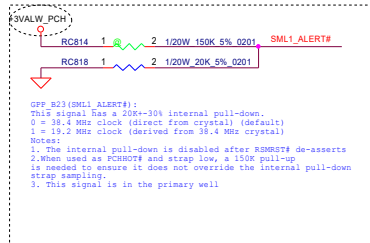
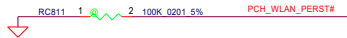
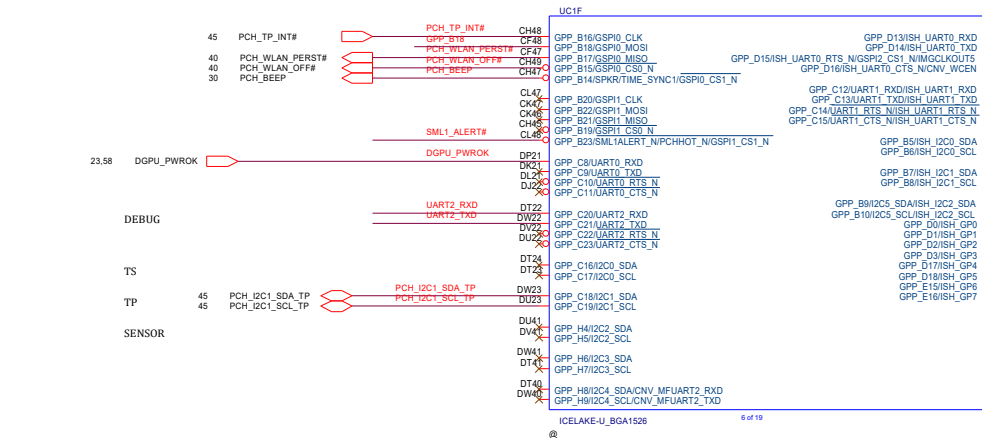


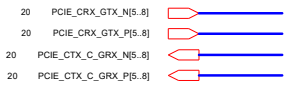


GPP_C2(PCH_SMB_ALERT#):
This signal is used to wake the system or generate SMI#.
External Pull-up resistor is required. Rising edge of RSMRST#
This signal has a 20K+/-30% internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS)
cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS)
cipher suite (with confidentiality). Must be
pulled up to support Intel AMT with TLS.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

GPP_C5(PCH_SML0_ALERT#):
Rising edge of RSMRST#
This signal has a 20K+/-30% internal pull-down.
0 = Disable eSPI (Default)
1 = Enable eSPI.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.







dGPU

WLAN

HDD

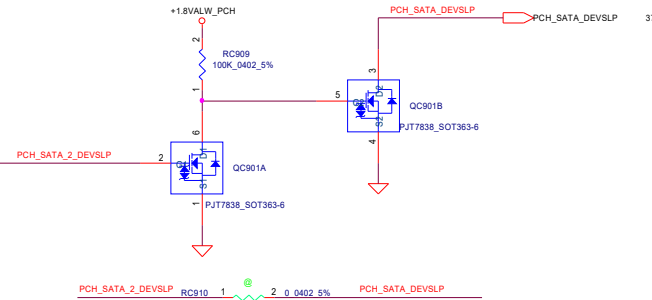
SSD

UC1H

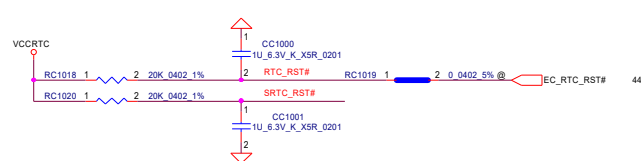
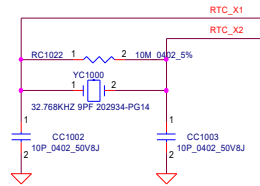
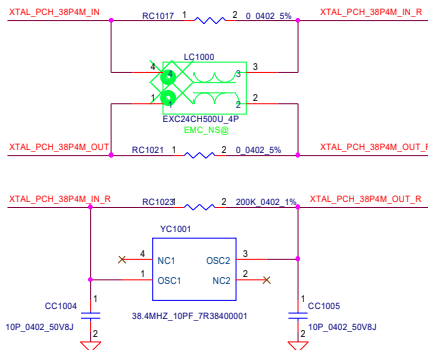
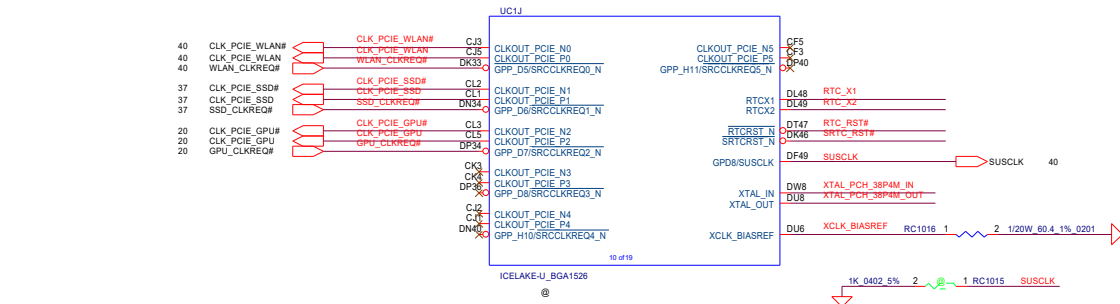
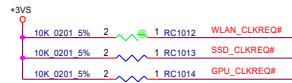
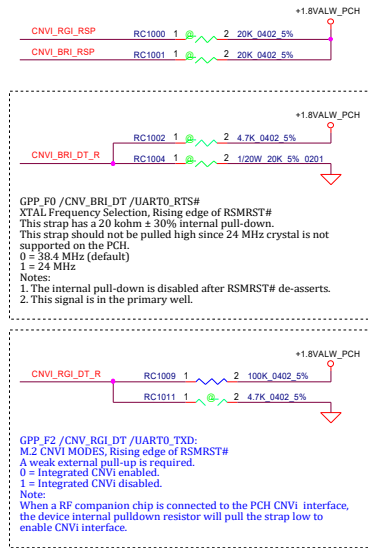
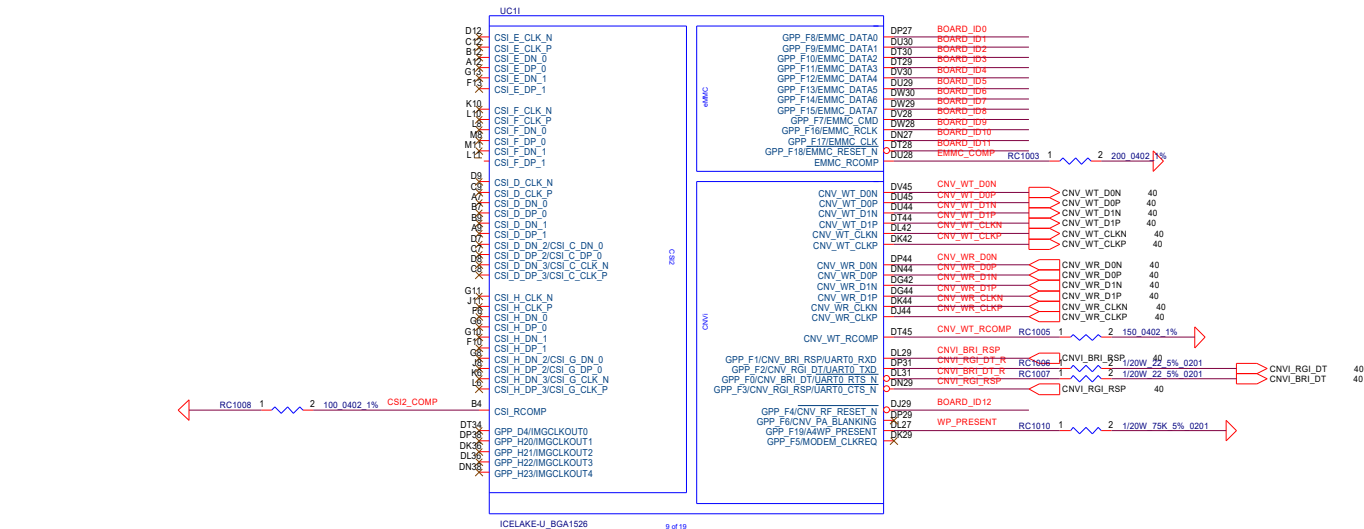
ICELAKE-U_BGA1526



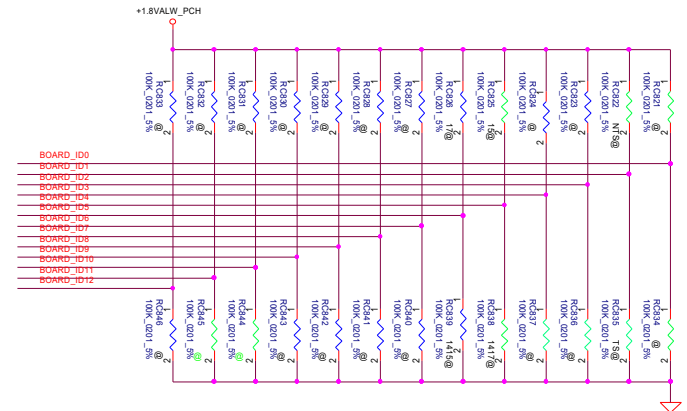
Native OD output



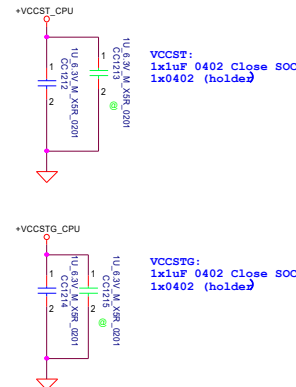
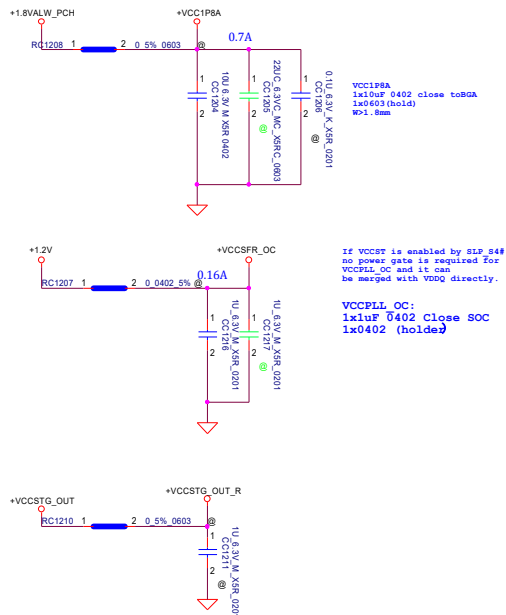
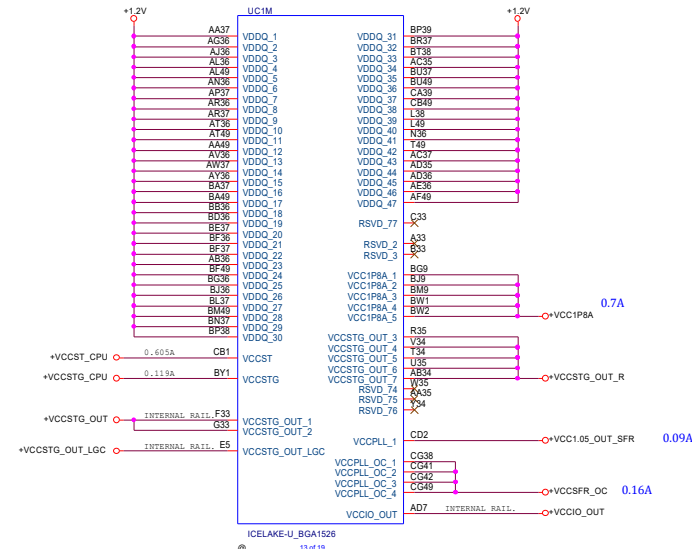
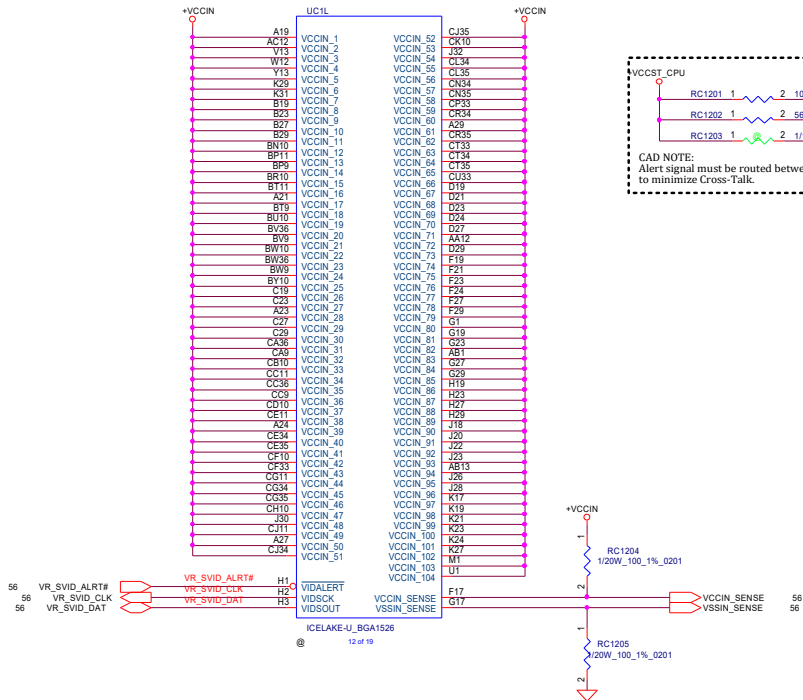
1. DEVSLP is an open-drain pin on the PCH side and is not required external pull-up or pull-down. The PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
2. DEVSLP is supported in direct connect, mSATA/mPCIe, uSBD, M.2.
3. 1 DEVSLP pin is required to support EACH DEVSLP enabled RAID storage device.
(Example: 2 DEVSLP pins are required to support 2 DEVSLP RAID storage devices).

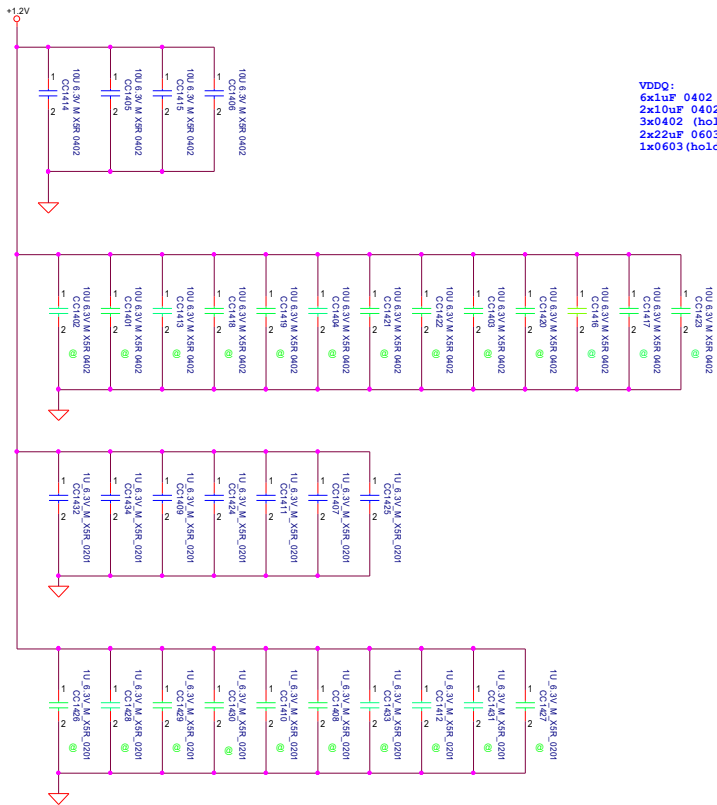


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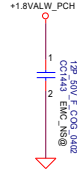
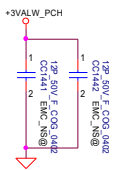
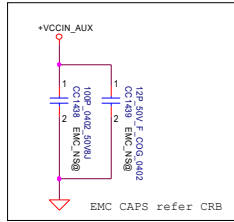
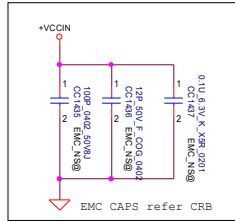


BOARD_ID5.4	14"	010R330 R330
BOARD_ID5.4	15"	010R330 R330
BOARD_ID5.4	17"	010R330 R330
BOARD_ID6/7/8/9	Sumang	0000
BOARD_ID6/7/8/9	Hynix	0001
BOARD_ID6/7/8/9	Micron	0010





VDDQ:
 6x10uF 0402 Back ,Outer row
 2x10uF 0402 back Outer row
 3x0402 (holder)
 2x22uF 0603 (80DMM need)
 1x0603 (holder)



UC10		
A11	VSS 1	VSS 75
A46	VSS 2	VSS 76
BA45	VSS 3	VSS 77
BA47	VSS 4	VSS 78
BB11	VSS 5	VSS 79
BB3	VSS 6	VSS 80
BB7	VSS 7	VSS 81
BC37	VSS 8	VSS 82
BD3	VSS 9	VSS 83
BD38	VSS 10	VSS 84
BD39	VSS 11	VSS 85
BD41	VSS 12	VSS 86
BD42	VSS 13	VSS 87
BD43	VSS 14	VSS 88
BD45	VSS 15	VSS 89
BD49	VSS 16	VSS 90
BD5	VSS 17	VSS 91
BD6	VSS 18	VSS 92
BD7	VSS 19	VSS 93
BE1	VSS 20	VSS 94
BE2	VSS 21	VSS 95
BF3	VSS 22	VSS 96
BF4	VSS 23	VSS 97
BF45	VSS 24	VSS 98
BF47	VSS 25	VSS 99
BF7	VSS 26	VSS 100
BC3	VSS 27	VSS 101
BC41	VSS 28	VSS 102
BC7	VSS 29	VSS 103
BC37	VSS 30	VSS 104
BJ1	VSS 31	VSS 105
BJ2	VSS 32	VSS 106
BJ3	VSS 33	VSS 107
BJ4	VSS 34	VSS 108
BJ45	VSS 35	VSS 109
BJ47	VSS 36	VSS 110
BJ49	VSS 37	VSS 111
BJ7	VSS 38	VSS 112
BJ7	VSS 39	VSS 113
BJ7	VSS 40	VSS 114
BM11	VSS 41	VSS 115
BM3	VSS 42	VSS 116
BM45	VSS 43	VSS 117
BM47	VSS 44	VSS 118
BM5	VSS 45	VSS 119
BM6	VSS 46	VSS 120
BM7	VSS 47	VSS 121
BP1	VSS 48	VSS 122
BP2	VSS 49	VSS 123
BP3	VSS 50	VSS 124
BP4	VSS 51	VSS 125
BP7	VSS 52	VSS 126
BR45	VSS 53	VSS 127
BR49	VSS 54	VSS 128
AB11	VSS 55	VSS 129
AB3	VSS 56	VSS 130
AB38	VSS 57	VSS 131
AB39	VSS 58	VSS 132
AB41	VSS 59	VSS 133
AB42	VSS 60	VSS 134
A17	VSS 61	VSS 135
AB43	VSS 62	VSS 136
AB5	VSS 63	VSS 137
AB6	VSS 64	VSS 138
AC45	VSS 65	VSS 139
AD45	VSS 66	VSS 140
AD10	VSS 67	VSS 141
AD11	VSS 68	VSS 142
AD34	VSS 69	VSS 143
AD37	VSS 70	VSS 144
A3	VSS 71	VSS 145
AE1	VSS 72	VSS 146
AF37	VSS 73	VSS 147
AF37	VSS 74	VSS 148

ICELAKE-U, BGA1526
@

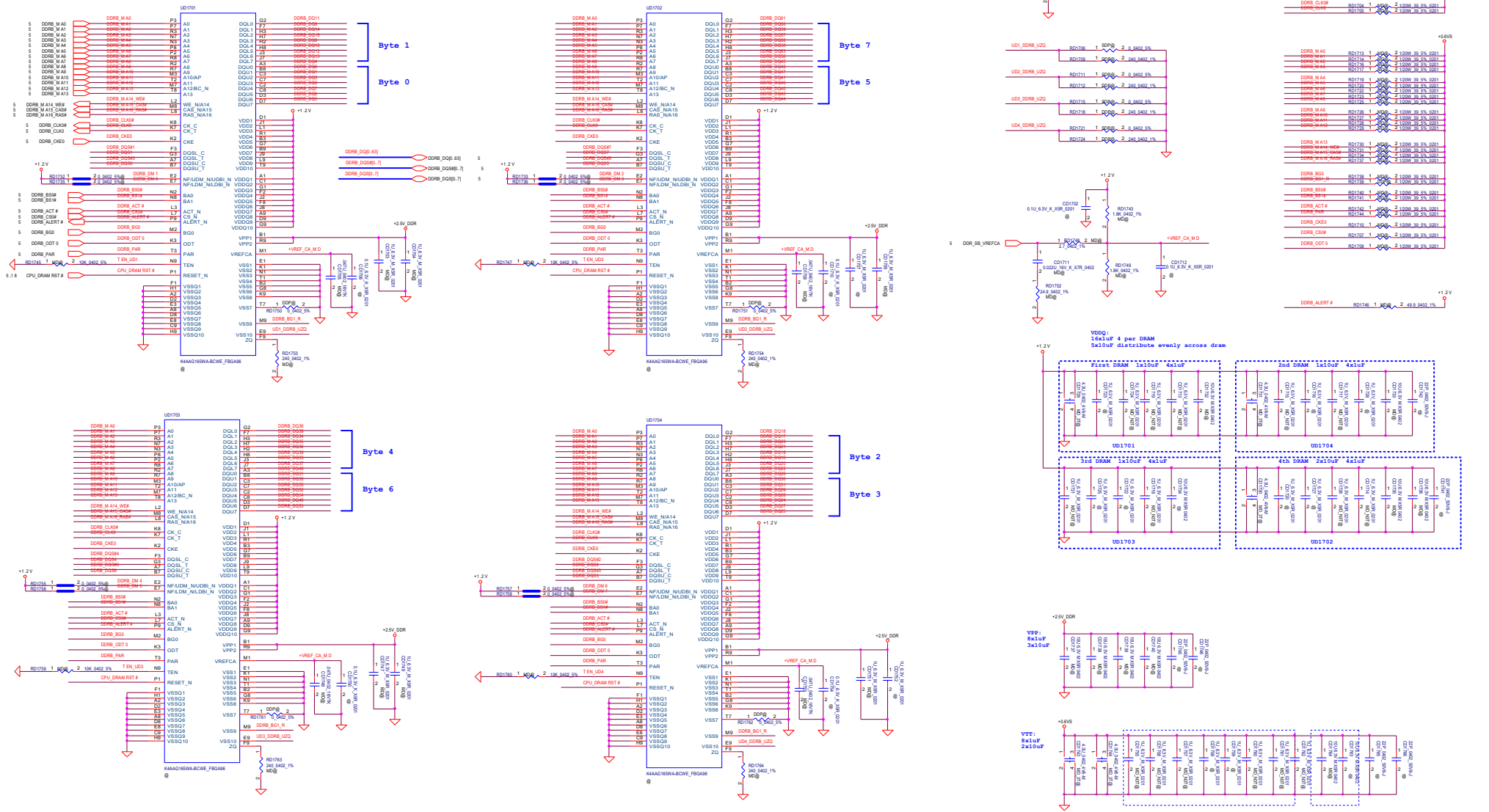
UC1P		
BT3	VSS 149	VSS 223
BT41	VSS 150	VSS 224
BT42	VSS 151	VSS 225
BT43	VSS 152	VSS 226
BT7	VSS 153	VSS 227
BU47	VSS 154	VSS 228
BU47	VSS 155	VSS 229
BU49	VSS 156	VSS 230
BV11	VSS 157	VSS 231
BV2	VSS 158	VSS 232
BV3	VSS 159	VSS 233
BV7	VSS 160	VSS 234
BW3	VSS 161	VSS 235
BW37	VSS 162	VSS 236
BW6	VSS 163	VSS 237
BW6	VSS 164	VSS 238
BW7	VSS 165	VSS 239
BV37	VSS 166	VSS 240
BV45	VSS 167	VSS 241
BV49	VSS 168	VSS 242
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C14	VSS 171	VSS 245
C17	VSS 172	VSS 246
C21	VSS 173	VSS 247
C24	VSS 174	VSS 248
C31	VSS 175	VSS 249
C34	VSS 176	VSS 250
C37	VSS 177	VSS 251
C48	VSS 178	VSS 252
C49	VSS 179	VSS 253
C6	VSS 180	VSS 254
CA3	VSS 181	VSS 255
CA38	VSS 182	VSS 256
CA41	VSS 183	VSS 257
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CB7	VSS 189	VSS 263
CC3	VSS 190	VSS 264
CC7	VSS 191	VSS 265
CE37	VSS 192	VSS 266
CE45	VSS 193	VSS 267
CE49	VSS 194	VSS 268
CE9	VSS 195	VSS 269
CG37	VSS 196	VSS 270
CG39	VSS 197	VSS 271
CG43	VSS 198	VSS 272
CG45	VSS 199	VSS 273
CG47	VSS 200	VSS 274
CG9	VSS 201	VSS 275
CH3	VSS 202	VSS 276
CH5	VSS 203	VSS 277
CJ37	VSS 204	VSS 278
CJ42	VSS 205	VSS 279
CJ45	VSS 206	VSS 280
CK45	VSS 207	VSS 281
CK49	VSS 208	VSS 282
CK9	VSS 209	VSS 283
CL37	VSS 210	VSS 284
CL42	VSS 211	VSS 285
CL49	VSS 212	VSS 286
CM45	VSS 213	VSS 287
CM47	VSS 214	VSS 288
CM9	VSS 215	VSS 289
CN3	VSS 216	VSS 290
CN37	VSS 217	VSS 291
CN39	VSS 218	VSS 292
CN5	VSS 219	VSS 293
CP9	VSS 220	VSS 294
CR32	VSS 221	VSS 295
CR32	VSS 222	VSS 296


ICELAKE-U, BGA1526
@

UC10		
DJ33	VSS 297	VSS 362
DJ36	VSS 298	VSS 363
DJ42	VSS 299	VSS 364
DK3	VSS 300	VSS 365
DK4	VSS 301	VSS 366
DK49	VSS 302	VSS 367
DK8	VSS 303	VSS 368
DL10	VSS 304	VSS 369
DL13	VSS 305	VSS 370
DL44	VSS 306	VSS 371
DL47	VSS 307	VSS 372
DM47	VSS 308	VSS 373
DN15	VSS 309	VSS 374
DN19	VSS 310	VSS 375
DN24	VSS 311	VSS 376
DN31	VSS 312	VSS 377
DN38	VSS 313	VSS 378
DN42	VSS 314	VSS 379
DP45	VSS 315	VSS 380
DR49	VSS 316	VSS 381
DT1	VSS 317	VSS 382
DT10	VSS 318	VSS 383
DT15	VSS 319	VSS 384
DT20	VSS 320	VSS 385
DT27	VSS 321	VSS 386
DT3	VSS 322	VSS 387
DT32	VSS 323	VSS 388
DT37	VSS 324	VSS 389
DT42	VSS 325	VSS 390
DT49	VSS 326	VSS 391
DT6	VSS 327	VSS 392
DT7	VSS 328	VSS 393
DT8	VSS 329	VSS 394
DT1	VSS 330	VSS 395
DT10	VSS 331	VSS 396
DT15	VSS 332	VSS 397
DT16	VSS 333	VSS 398
DT20	VSS 334	VSS 399
DT27	VSS 335	VSS 400
DT32	VSS 336	VSS 401
DT37	VSS 337	VSS 402
DT48	VSS 338	VSS 403
DT49	VSS 339	VSS 404
DT7	VSS 340	VSS 405
DV2	VSS 341	VSS 406
DV44	VSS 342	VSS 407
DV48	VSS 343	VSS 408
DV9	VSS 344	VSS 409
DW1	VSS 345	VSS 410
DW10	VSS 346	VSS 411
DW2	VSS 347	VSS 412
DW20	VSS 348	VSS 413
DW27	VSS 349	VSS 414
DW44	VSS 350	VSS 415
DW48	VSS 351	VSS 416
DW49	VSS 352	VSS 417
DW60	VSS 353	VSS 418
DW7	VSS 354	VSS 419
E11	VSS 355	VSS 420
E34	VSS 356	VSS 421
E38	VSS 357	VSS 422
E39	VSS 358	VSS 423
E42	VSS 359	VSS 424
E6	VSS 360	VSS 425
	VSS 361	VSS 426
	VSS 427	

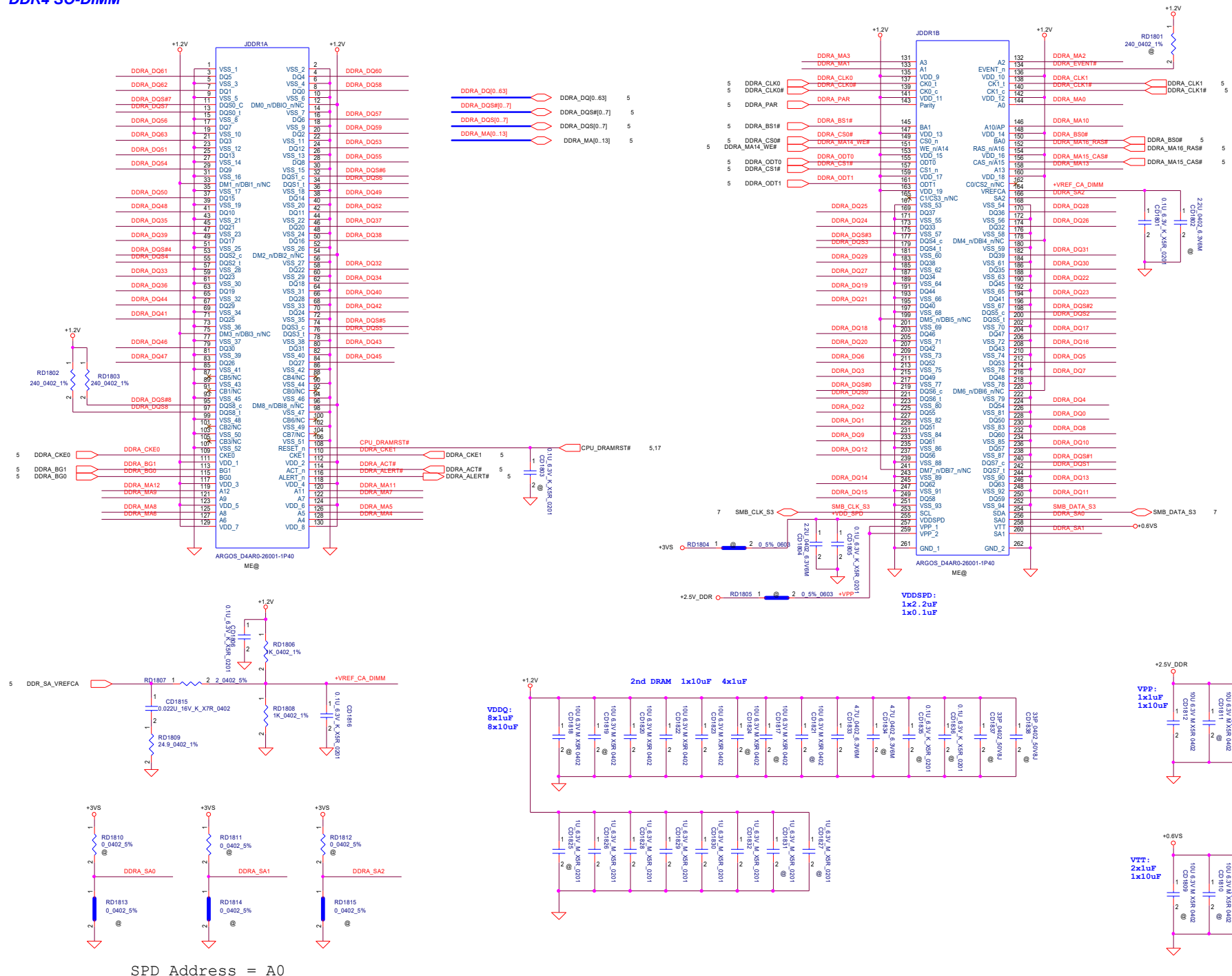
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17 of 19

DDR4 Memory Down




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Issued Date	2017/06/24	Dispersed date	2018/06/23	DDR4 Memory Down
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Version	1.0	Date	2018/06/23	
<p>Project Name: LC Future Center</p> <p>Project Location: 17-01-00</p>				

DDR4 SO-DIMM



SPD Address = A0

Security Classification		LC Future Center Secret Data		Title			
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2015/08/20		2016/08/20		Doc# Document Number GS44D/GS54D		Rev 0.1	
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N16x GPIO

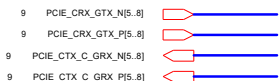
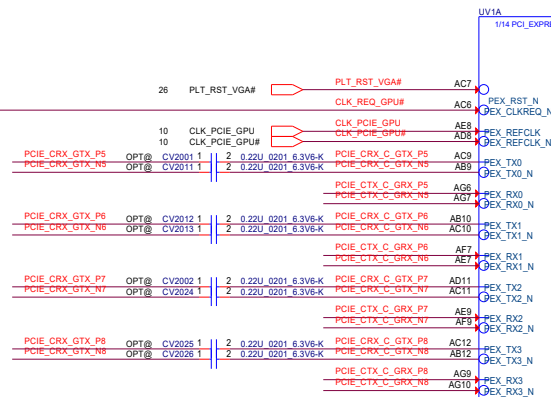
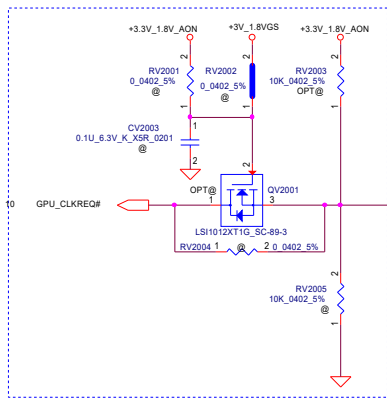
GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

	GPU	Mem	Min Core Clk	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		(1.05V) (6)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

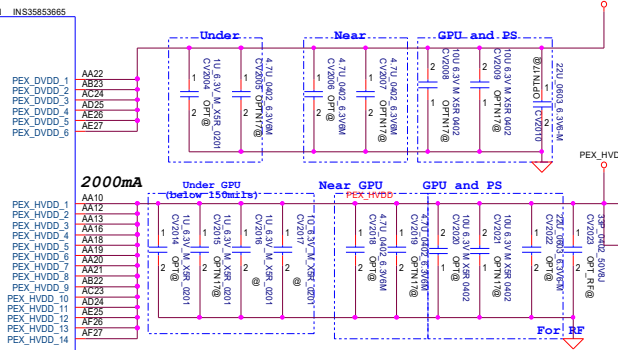
N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				



PEX LANES 15 - 4 ARE DEFEATED

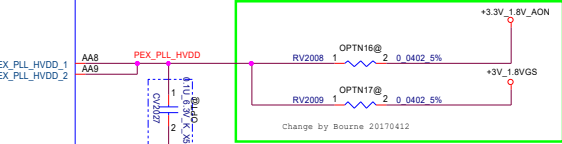
N17S-G1-A1_GB2C-64-595



PEX_DVDD
N16: +1.05VGS (recommend)
N17: +1.0VGS (Used)

PEX_HVDD
N16: +1.05VGS (recommend)
N17: +1.8VGS (Used)

Change by Bourne 20170412



PEX_PLL_HVDD
N16: +3.3V_AON
N17: +1.8VGS

Change by Bourne 20170412

PEX_DVDD/Q Decoupling





MLCC	N16	N17	location
1.0uF	1	1	Under
4.7uF	0	1	
4.7uF	1	2	
10uF	0	2	Midway
22uF	0	1	

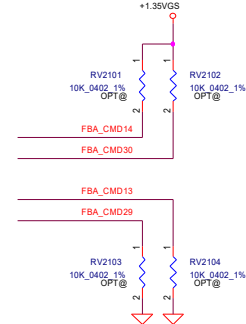
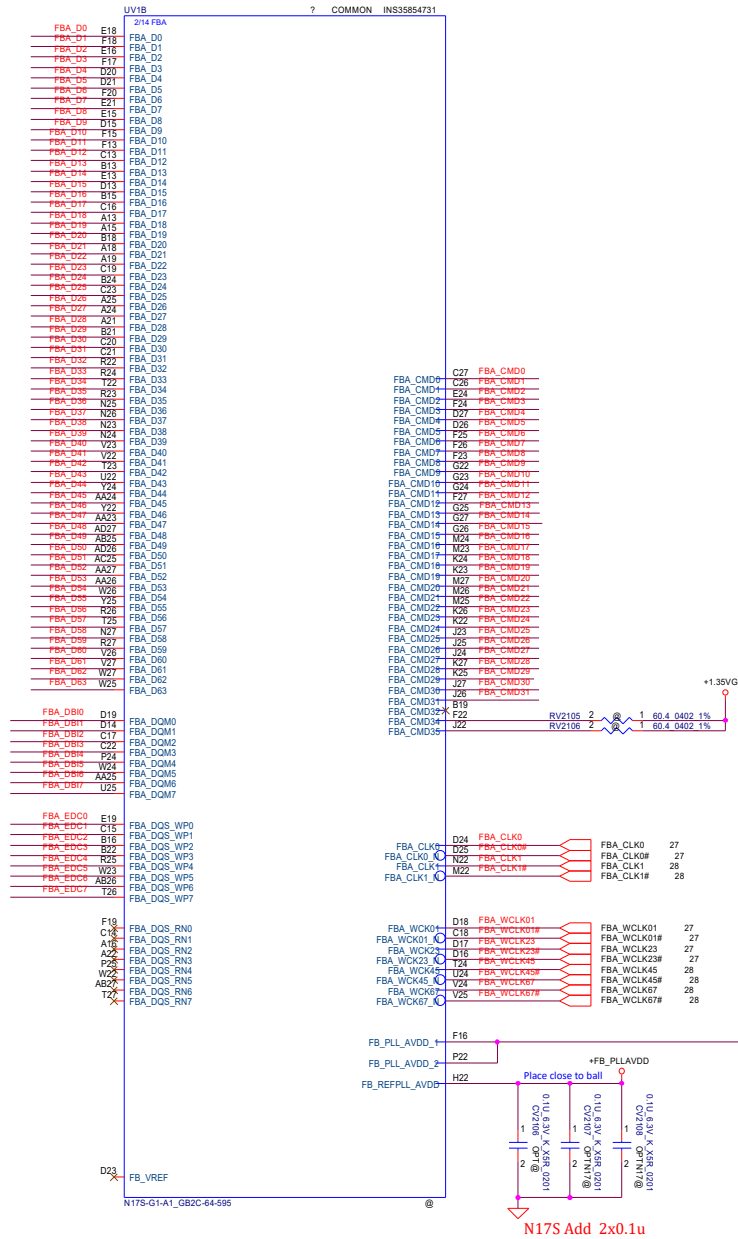
PEX_HVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	4	Under
4.7uF	1	2	Near
10uF	1	2	Midway
22uF	1	1	

PEX_PLL_HVDD/Q Decoupling

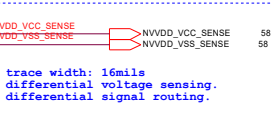
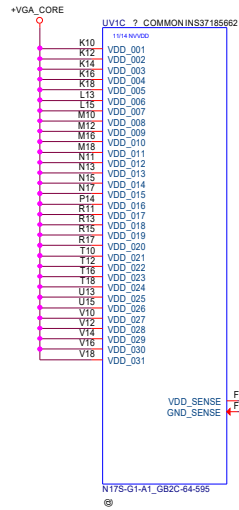
MLCC	N16	N17	location
0.1uF	1	1	Near

27.28 FBA_D[0:63] 
27.28 FBA_CMD[31:0] 
27.28 FBA_EDC[7:0] 
27.28 FBA_DB[7:0] 

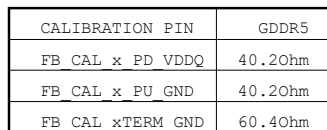


FB_PLL/VQ Decoupling

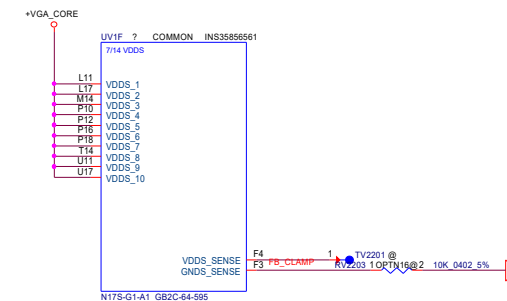
MLCC	N16	N17	location
0.1uF	2	4	Under
22uF	1	1	Near



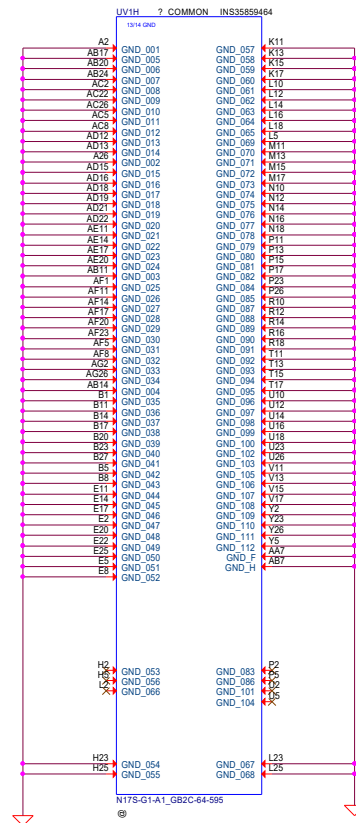
MLCC	N16	N17	location
4.7uF	10	12	Under
1.0uF	4	5	
47uF	1	0	
10uF	0	11	Near
22uF	1	4	
4.7uF	5	4	
330uF	1	2	




MLCC	N16	N17	location
0.1uF	2	0	Under
1.0uF	2	8	
4.7uF	2	0	
10uF	0	2	
10uF	1	1	Near
22uF	1	3	

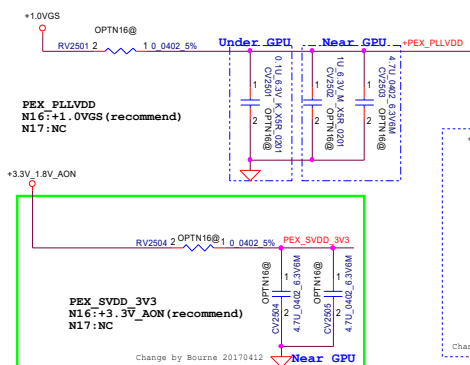




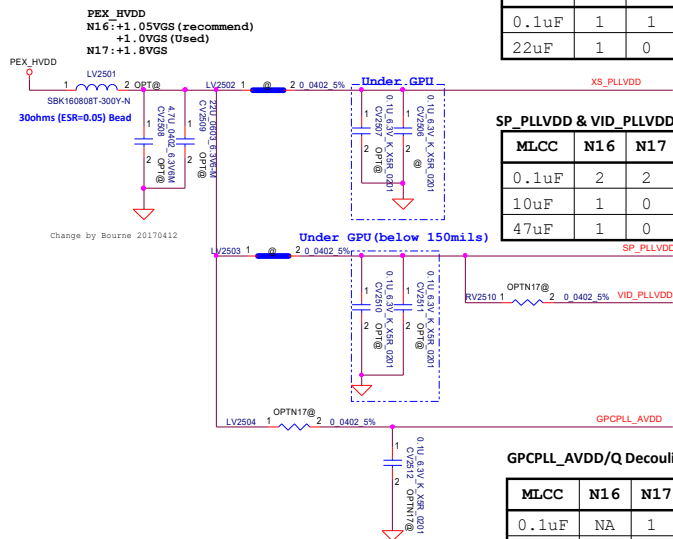


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		GS44D/GS54D						0.1	
Date:		Friday, December 06, 2019				Sheet		24 of 60	

MLCC	N16	N17	location
1.0uF	1	NA	Under
1uF	1	NA	Near
4.7uF	1	NA	



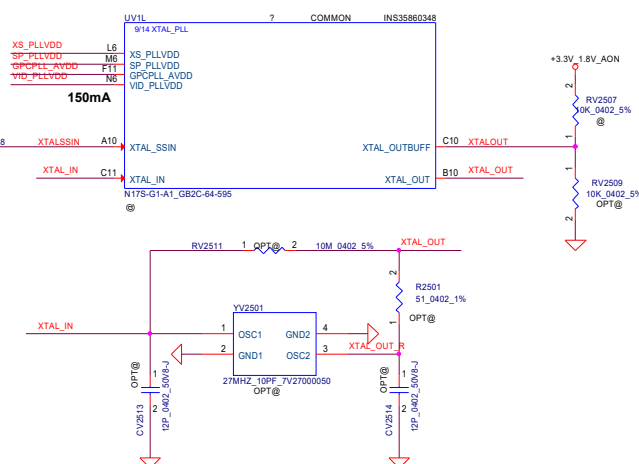
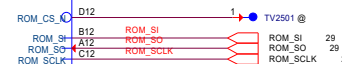
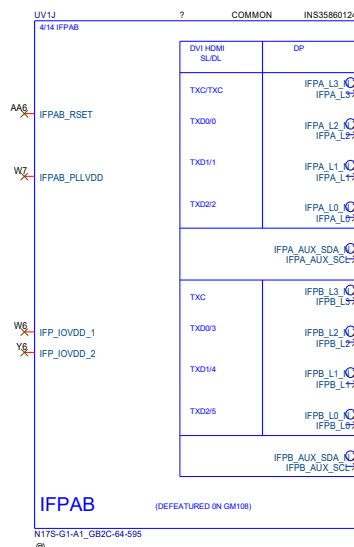
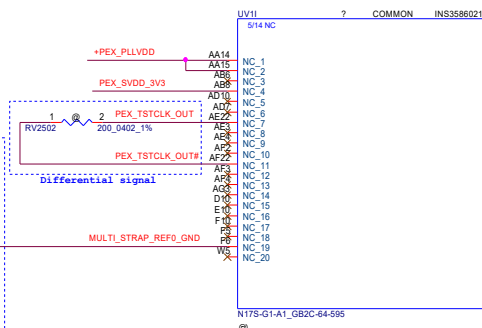
MLCC	N16	N17	location
4.7uF	2	NA	Near



MLCC	N16	N17	location
0.1uF	1	1	Under
22uF	1	0	Near

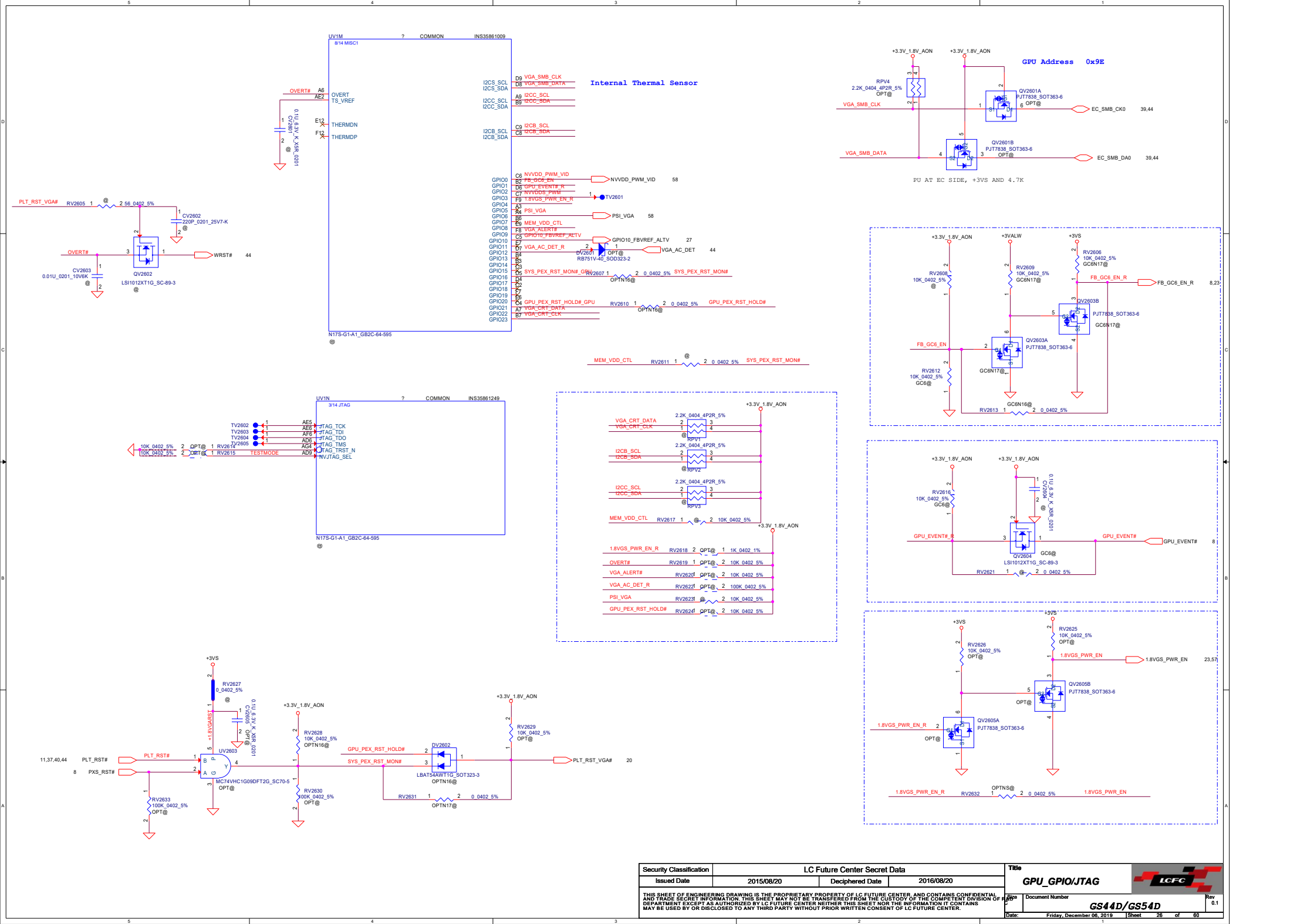
MLCC	N16	N17	location
0.1uF	2	2	Under
10uF	1	0	Near
47uF	1	0	

MLCC	N16	N17	location
0.1uF	NA	1	Under
4.7uF	NA	1	Near
22uF	NA	1	



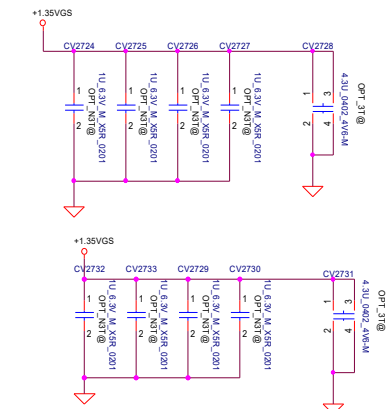
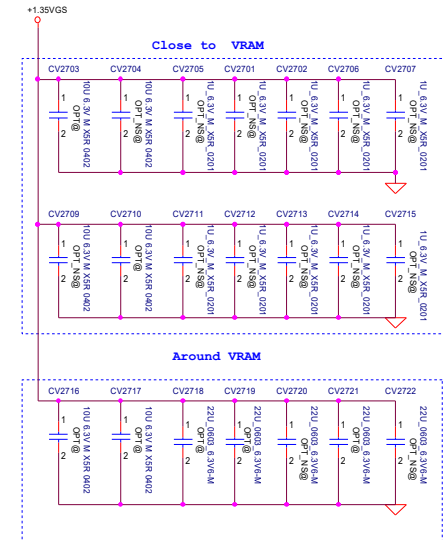
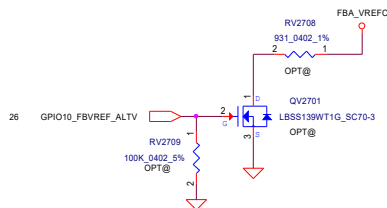
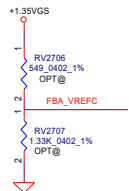
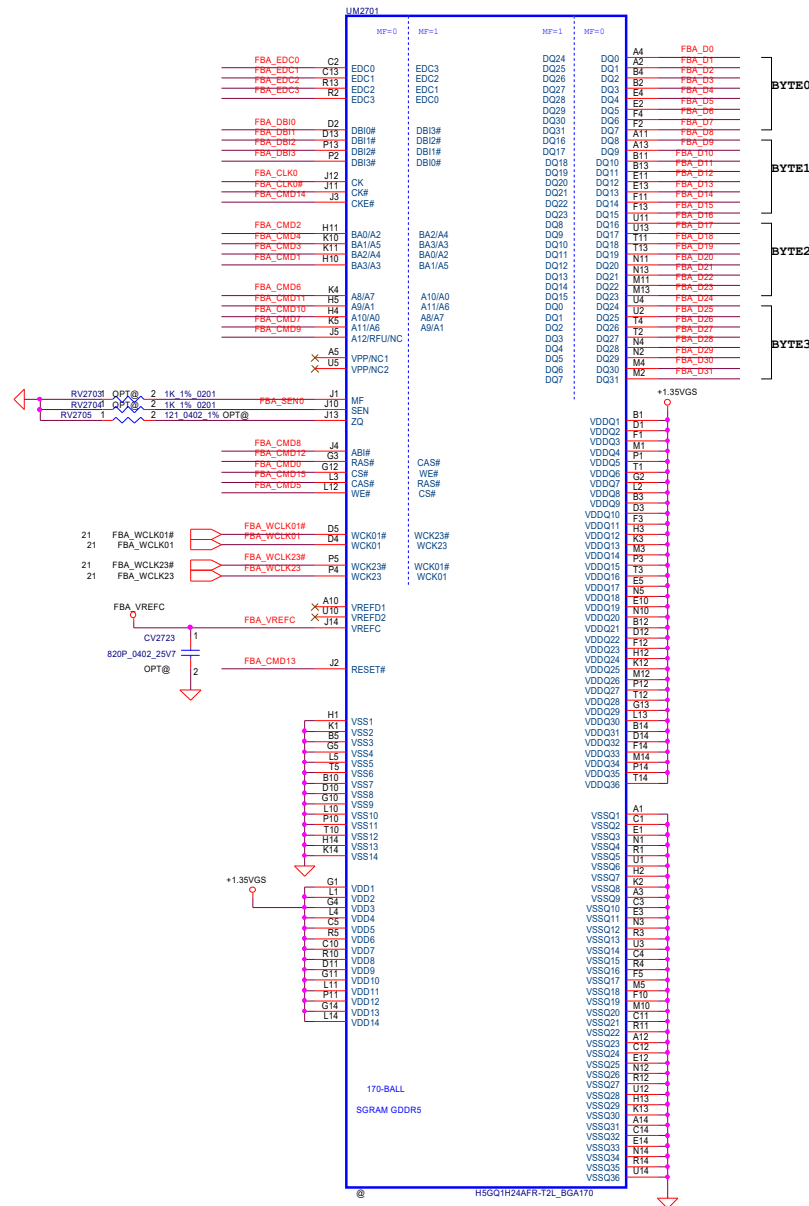
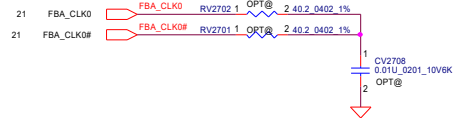
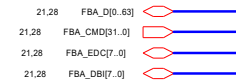
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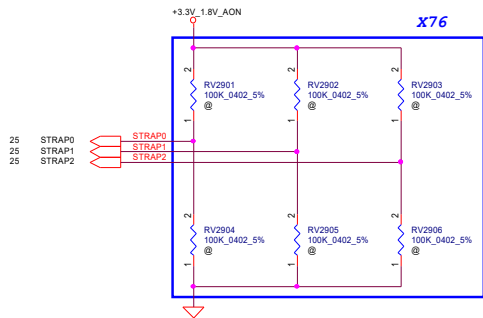


Lower 32 bits

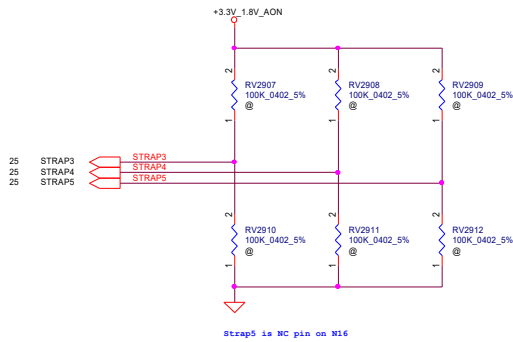
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Issued Date		Deciphered Date		GPU_GDDR5_Rank0 [31:0] 	
2015/08/20		2016/08/20		Docuement Number GS44D/GS54D	
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Date:		Friday, December 06, 2019		Sheet 27 of 60	



GPU	FB Memory (GDDR5)	RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0 (0x0000)	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1 (0x0001)	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2 (0x0010)	L	L



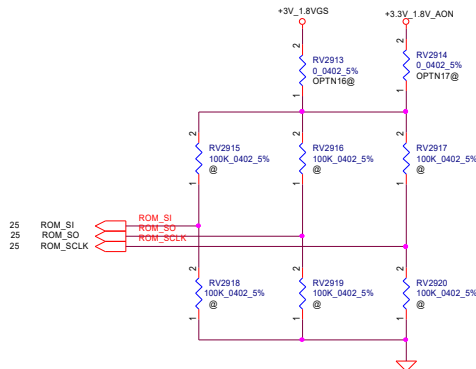
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGINAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE



	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17S-G1	H	H	M	0000
N16S-GTR				

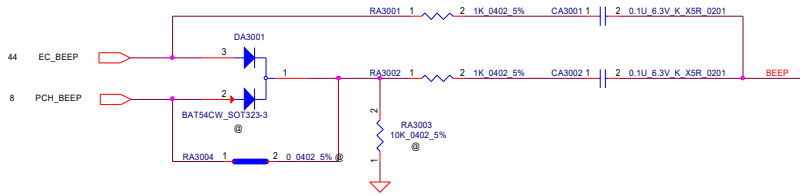
1: ENABLE 0: DISABLE
SOR0/1/2/3 DISABLE

DEVID_SEL	
0	(Default)
1	

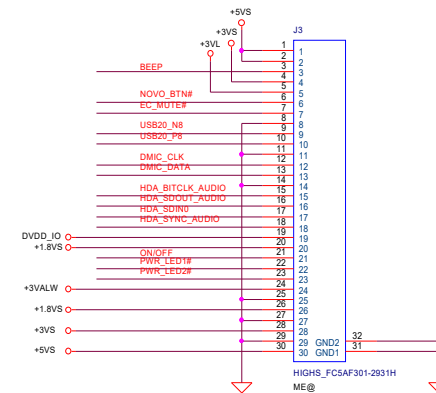
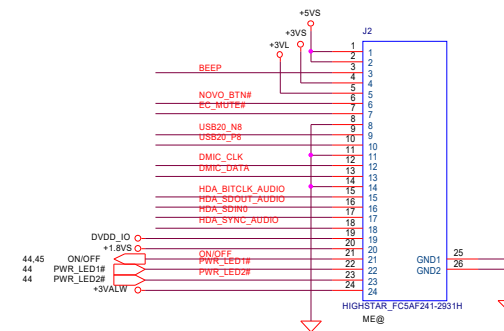
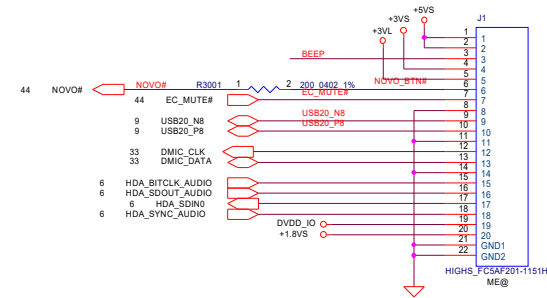
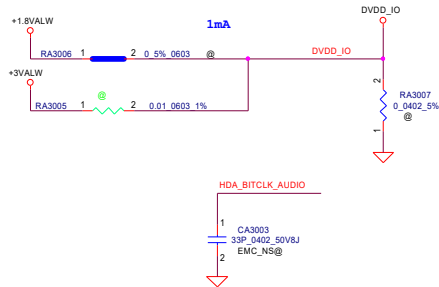
PCIE_CFG	
0	(Default)
1	


SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)


VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)



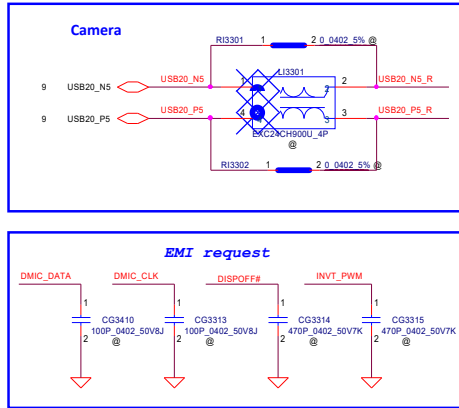
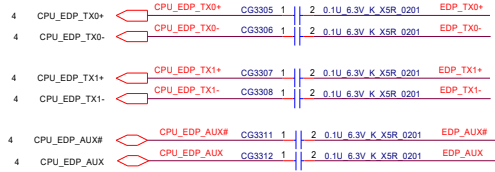
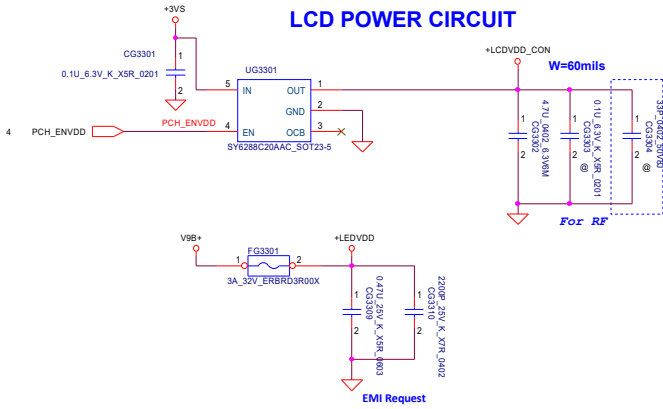
CPU HDA BUS power 1.8VALW



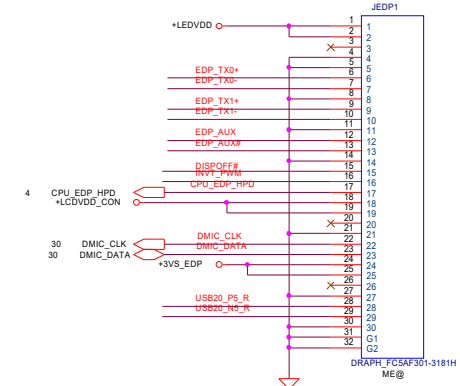
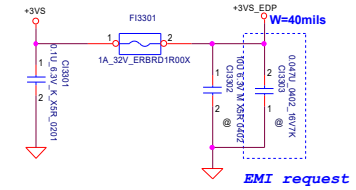
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GS44D/GS54D								Rev 0.1			

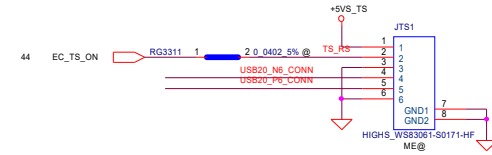
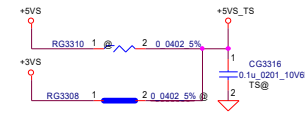
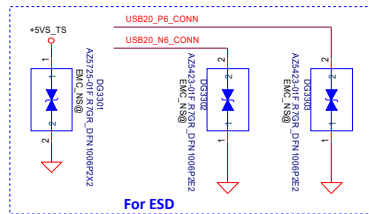
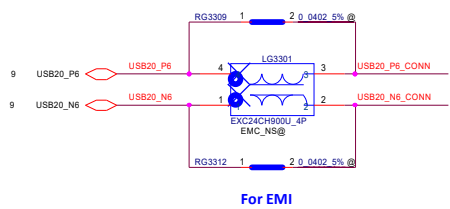
LCD POWER CIRCUIT

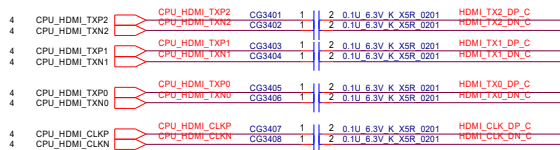


CMOS Camera

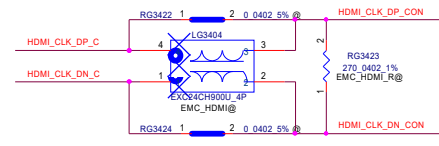
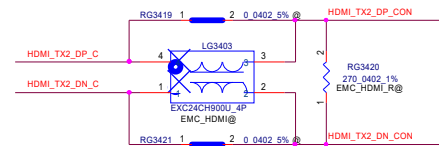
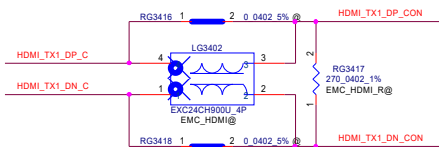
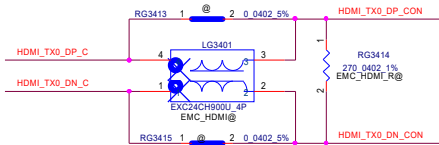
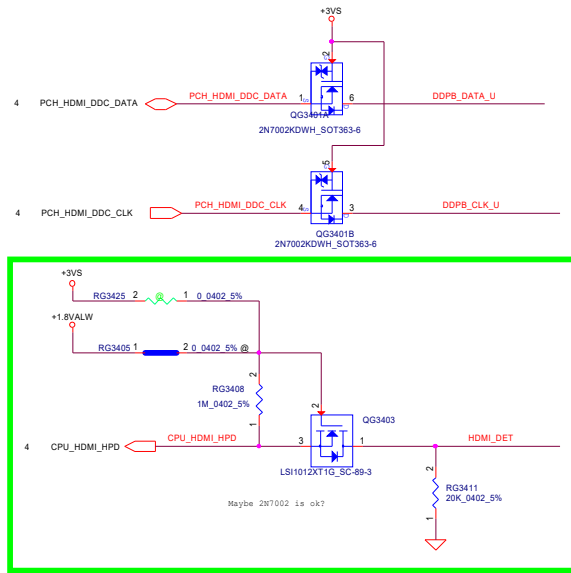
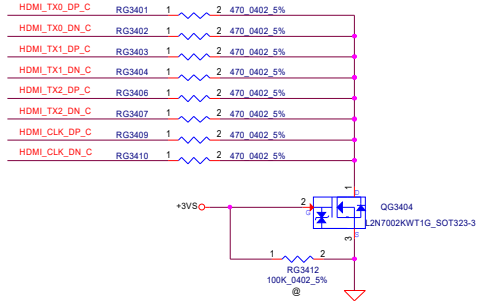


Touch Screen

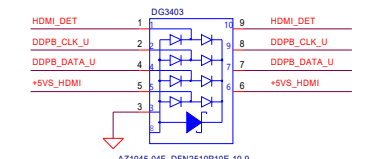
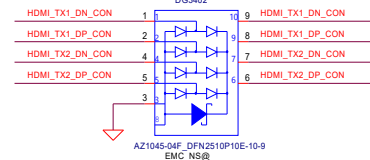
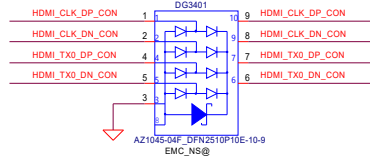




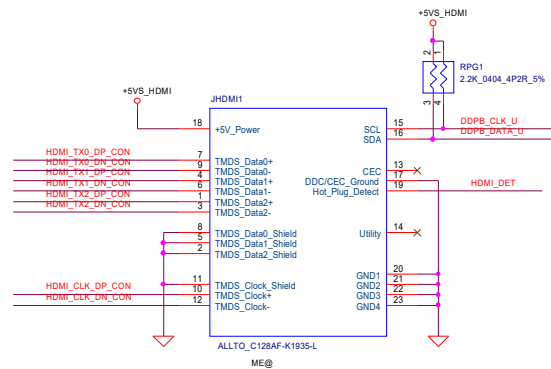
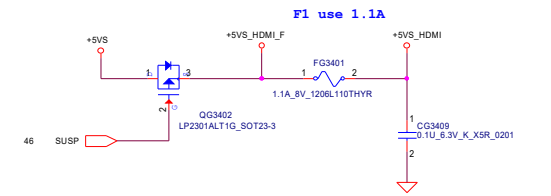
Need to change about 4700hm 5%-575412 Page115 Rev0.8





For EMC




For EMC

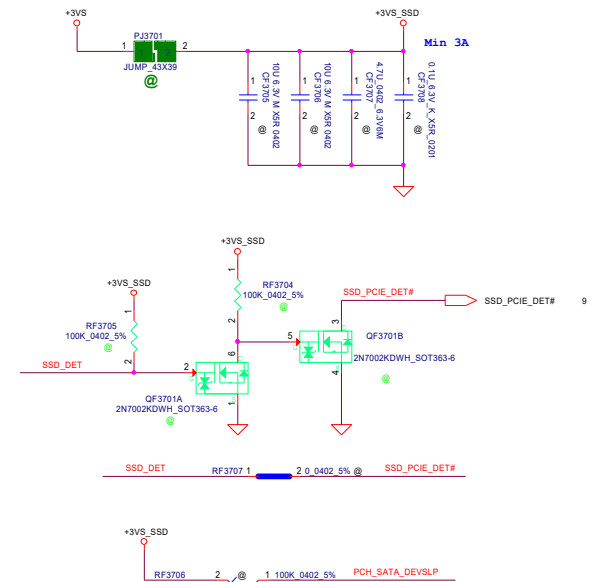
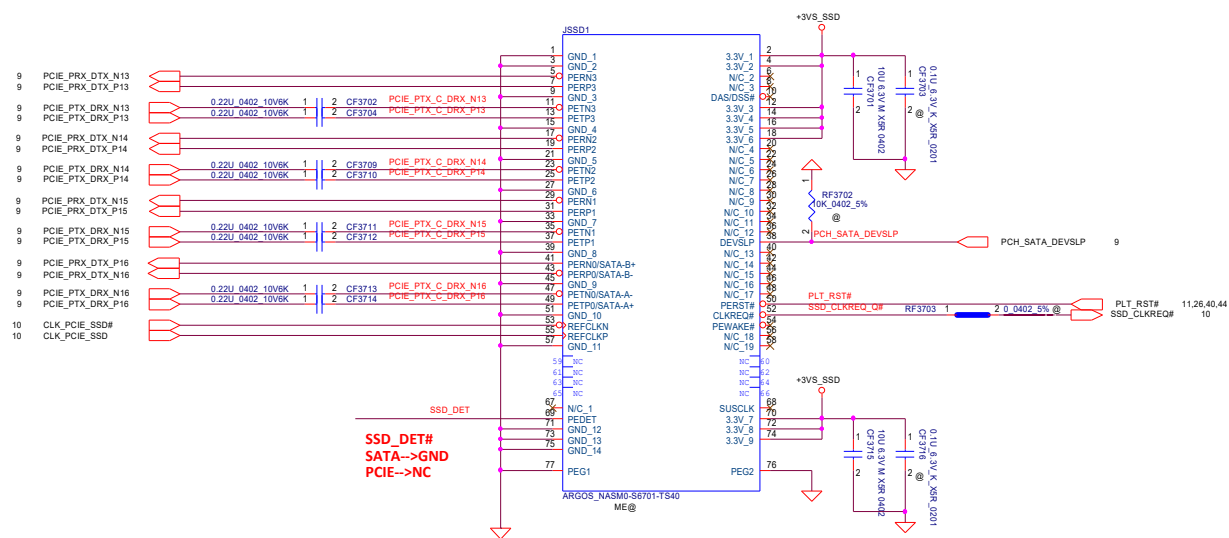


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Revision		Document Number				Rev
		GS44D/GS54D				0.1
Date:		Friday, December 06, 2019		Sheet		34 of 60

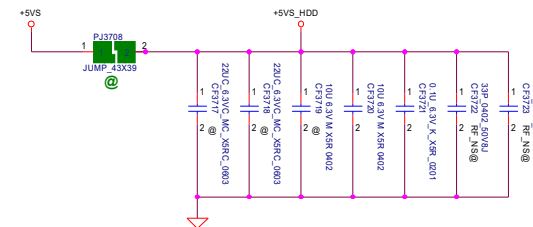
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Size						Document Number		Rev	
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Date:		Friday, December 06, 2019				Sheet		35 of 60	

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				Date	GS44D/GS54D	G.1	
				Date	Friday, December 06, 2019	Sheet 36 of 60	

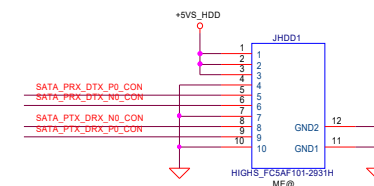
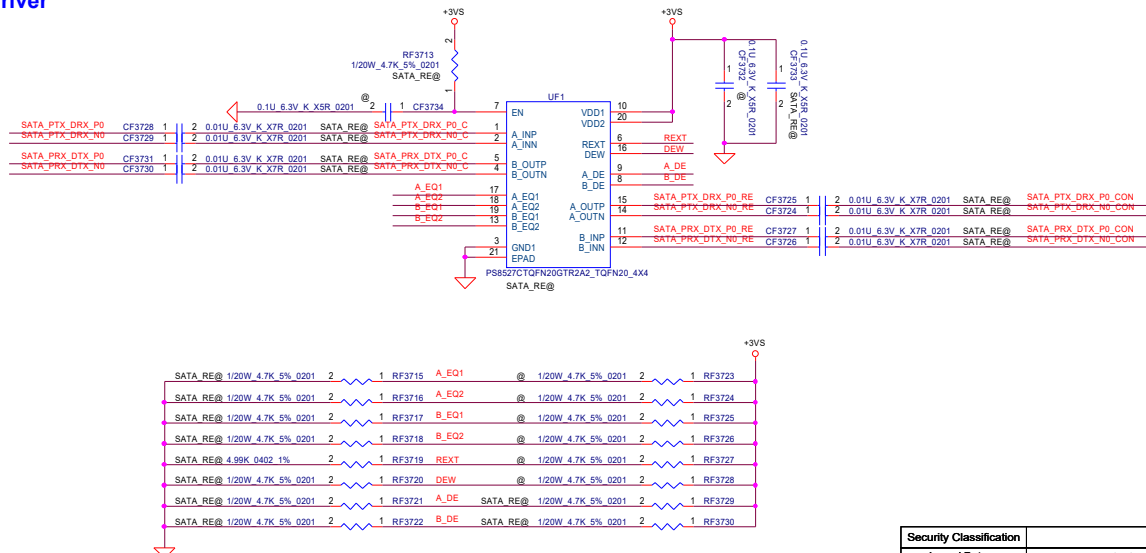
M.2 SSD





SATA



SATA Redriver

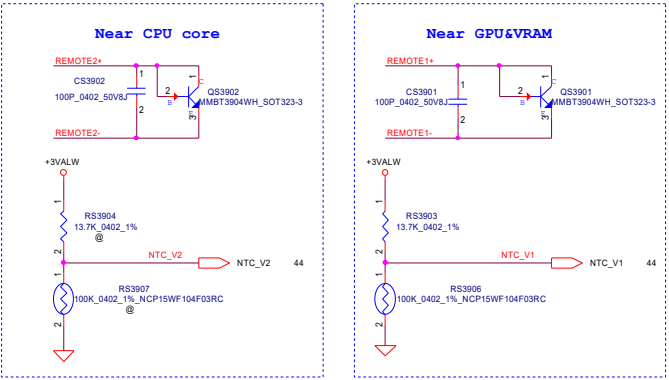
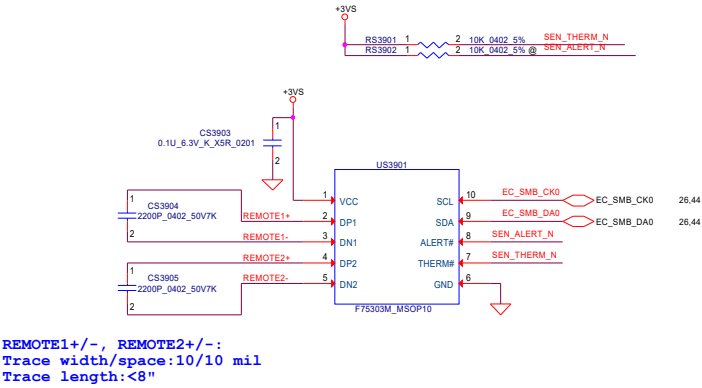


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										GS44D/GS54D			
Date:		Friday, December 08, 2019				Sheet 37 of 60							

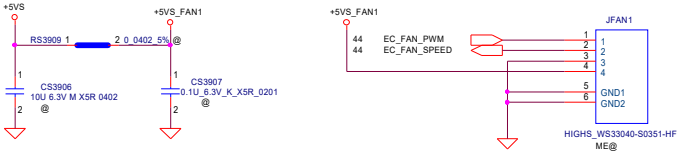
5					4					3					2					1				
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A																								
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Issued Date					2015/08/20					Deciphered Date					2016/08/20					Document Number				
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																				Rev 0.1				



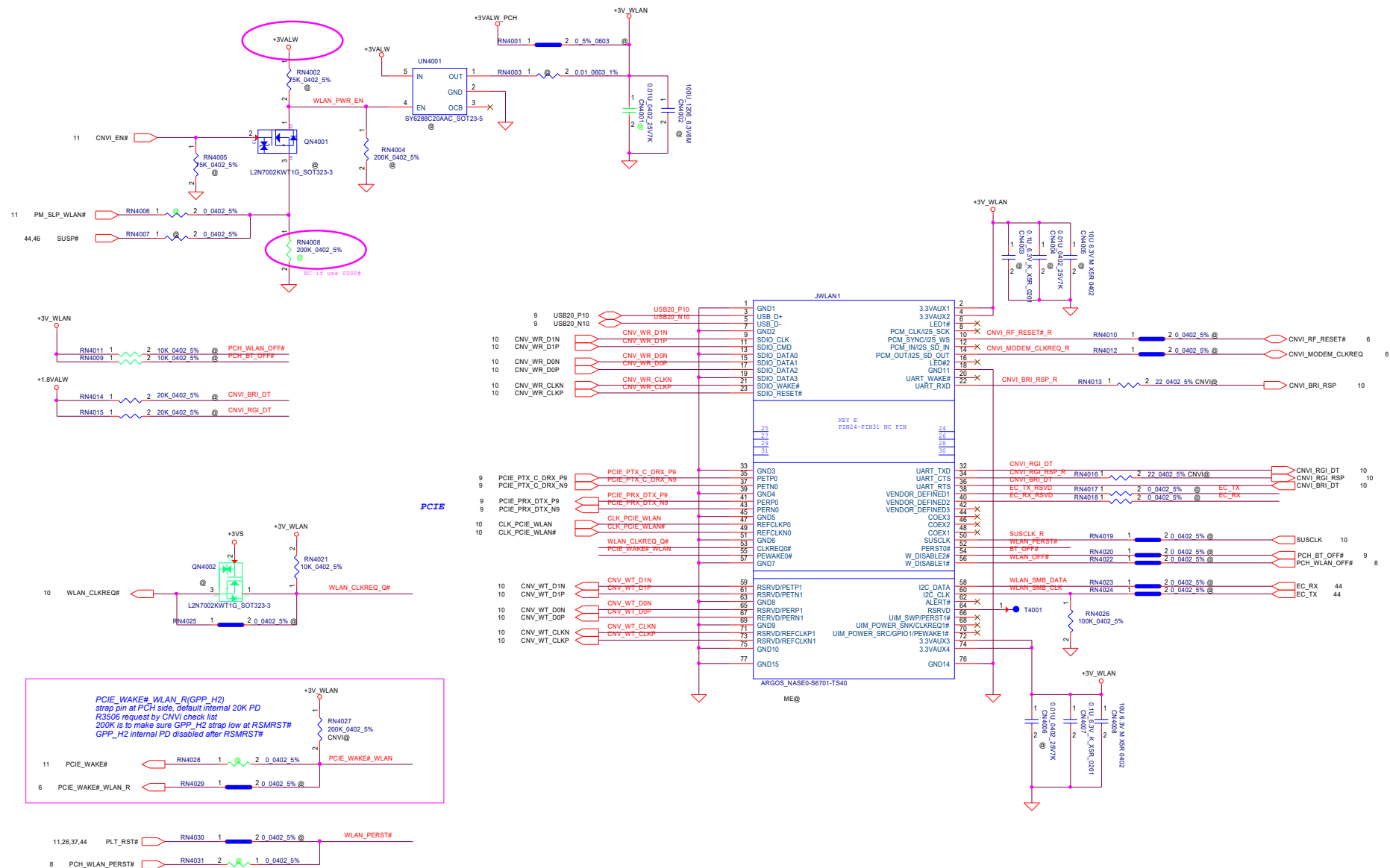
SMSC thermal sensor




FAN Conn

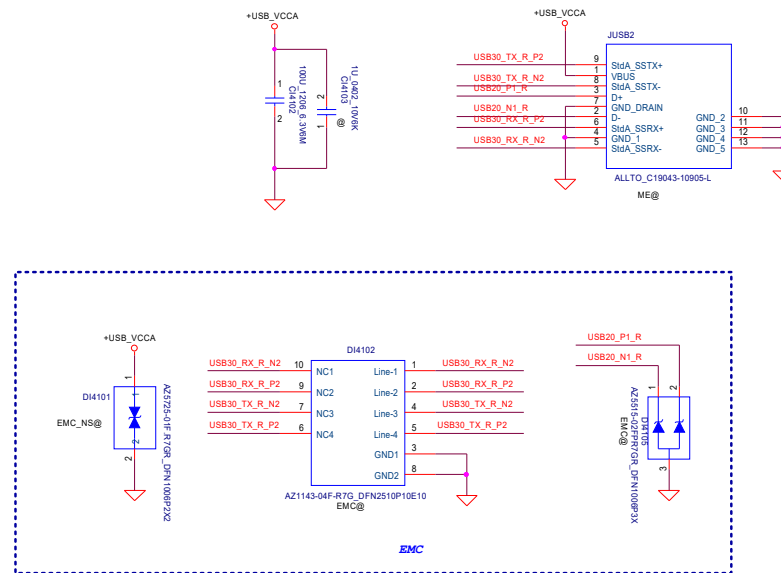
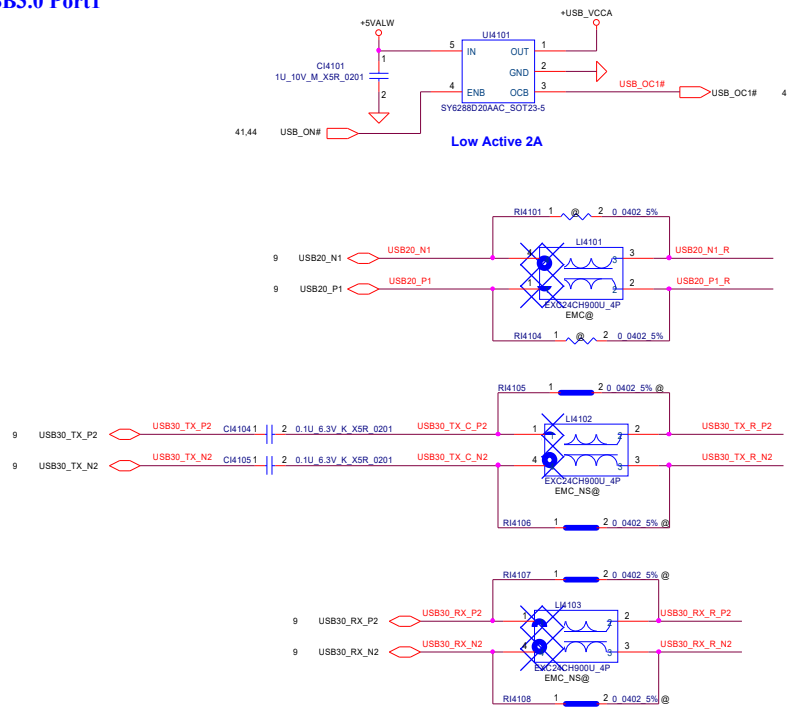


Mini-Express Card(WLAN/WiMAX)

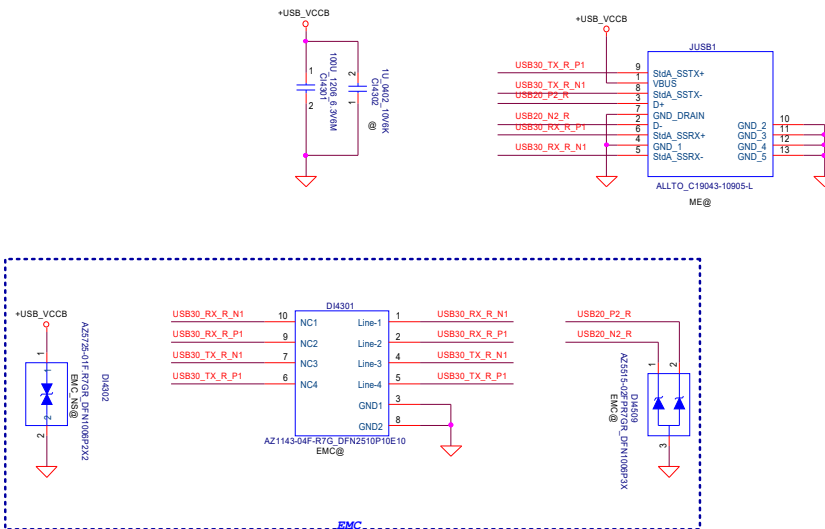
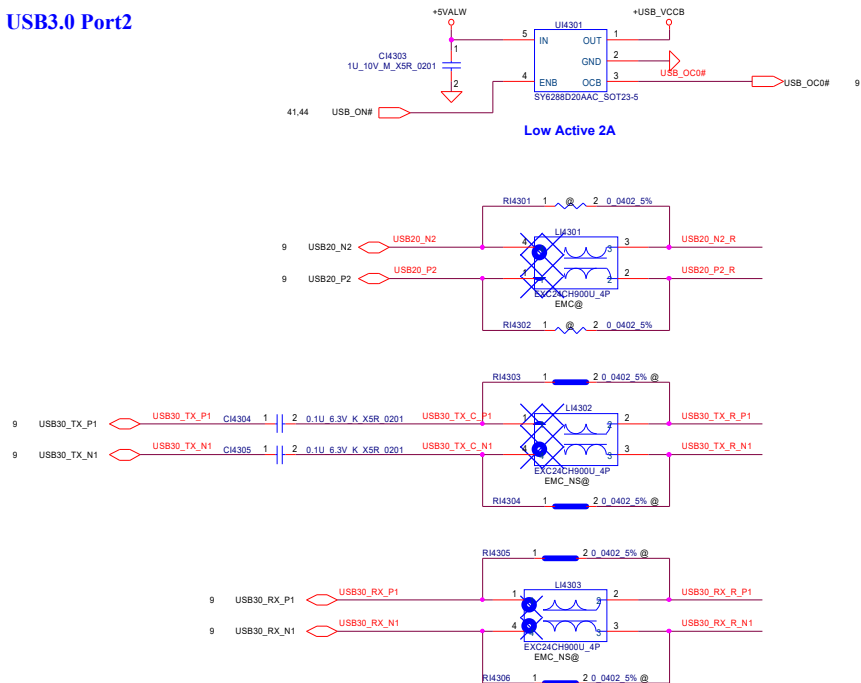


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				Document Number	Rev 0.
				Date: Friday, December 06, 2019	Sheet 40 of 60 GS44D/GS54D

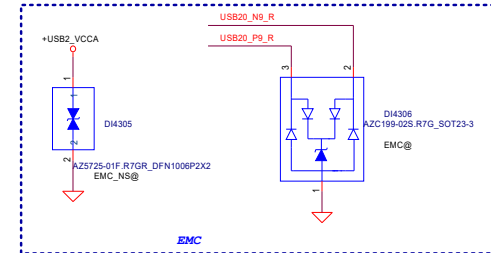
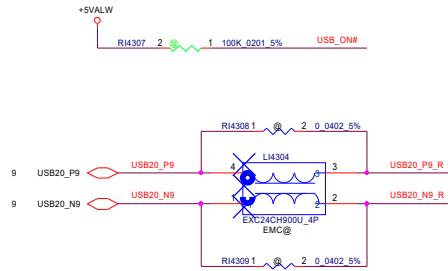
USB3.0 Port1




USB3.0 Port2

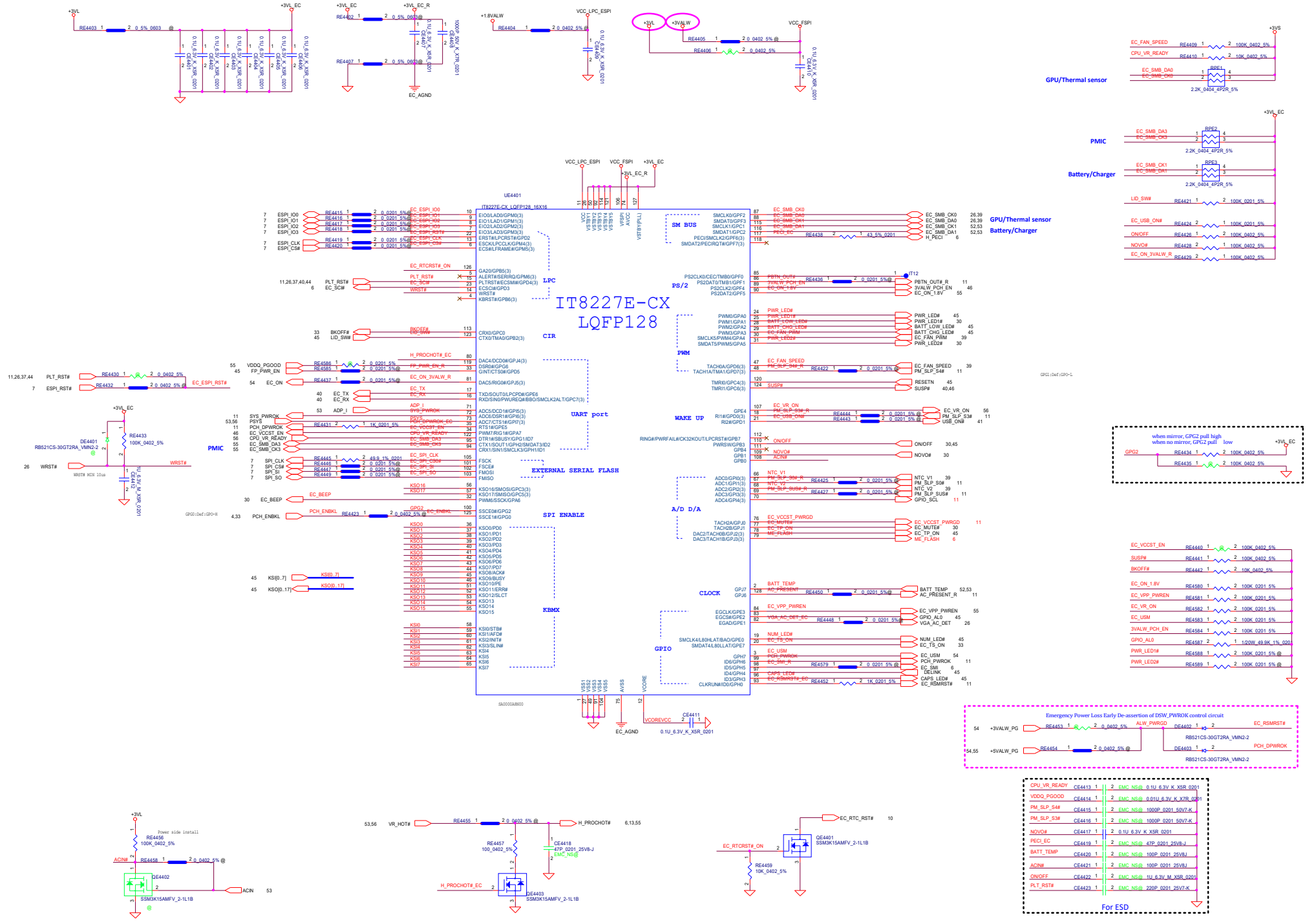


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Issued Date	2015/08/20	Deciphered Date	2016/08/20	Document Number	GS44D/GS54D
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Date: Friday, December 08, 2019 Sheet 41 of 60					

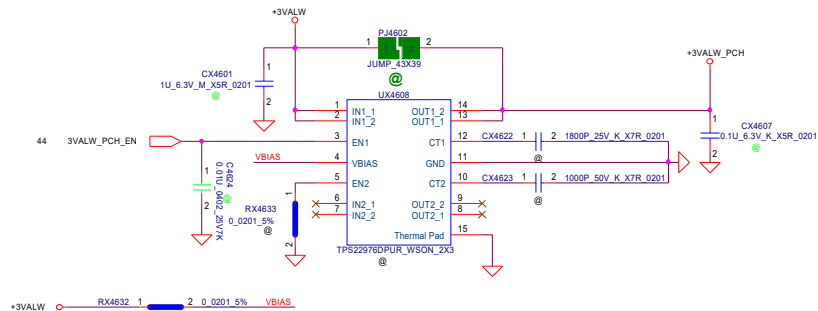
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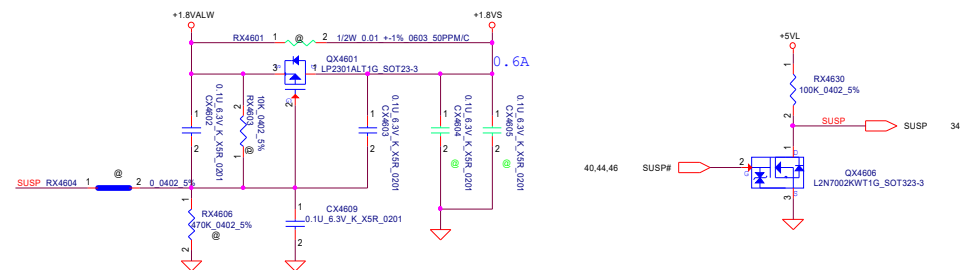
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+3VALW to PCH

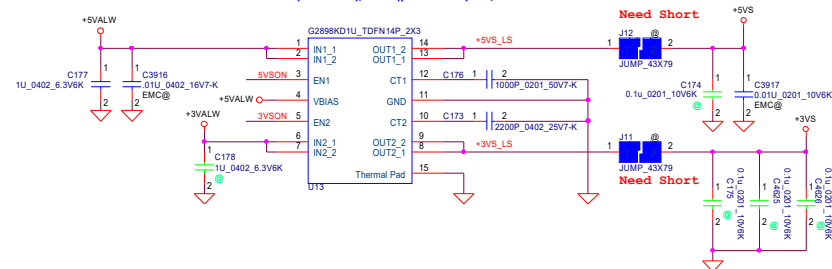


+1.8VALW to +1.8VS

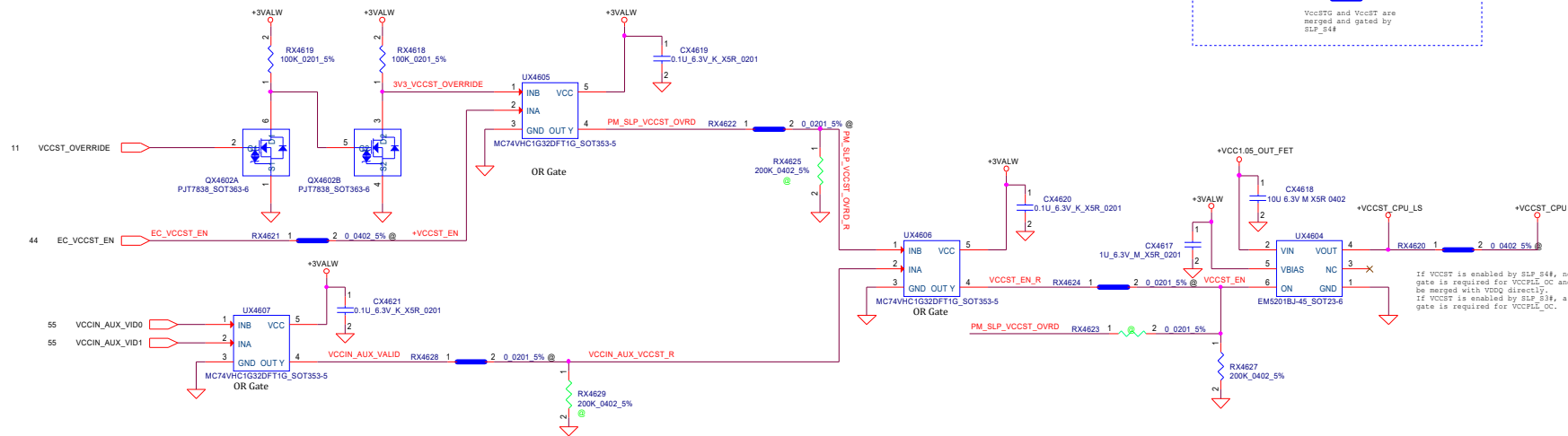


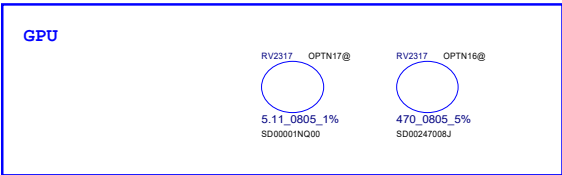
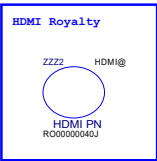
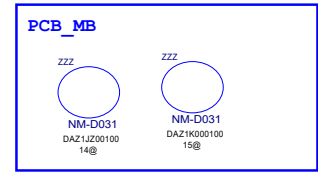
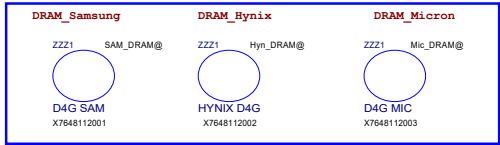
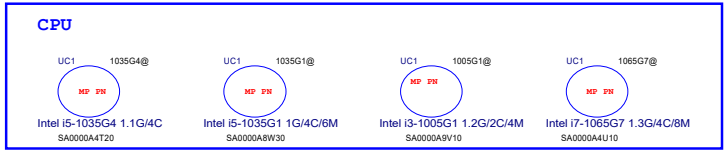
Load Switch +5VALW To +5VS +3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

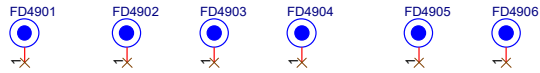


VCCST&VCCSTG

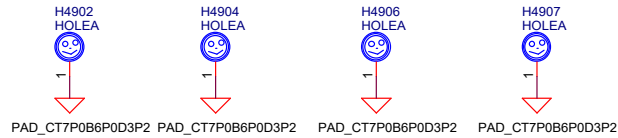




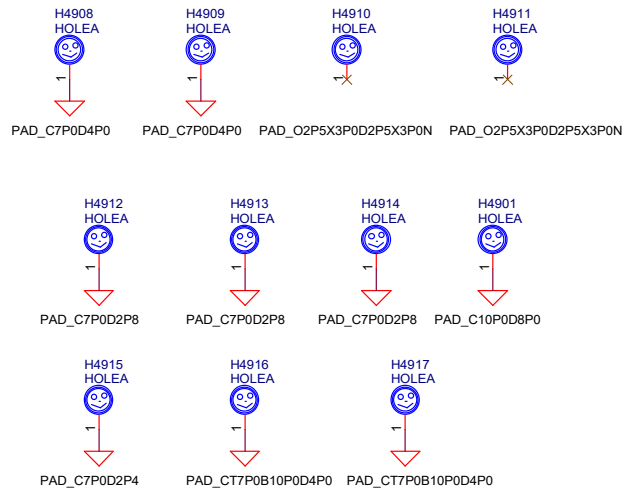
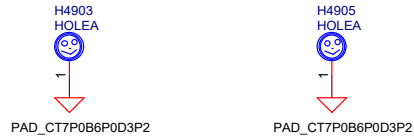
PCB Federal Mark PAD



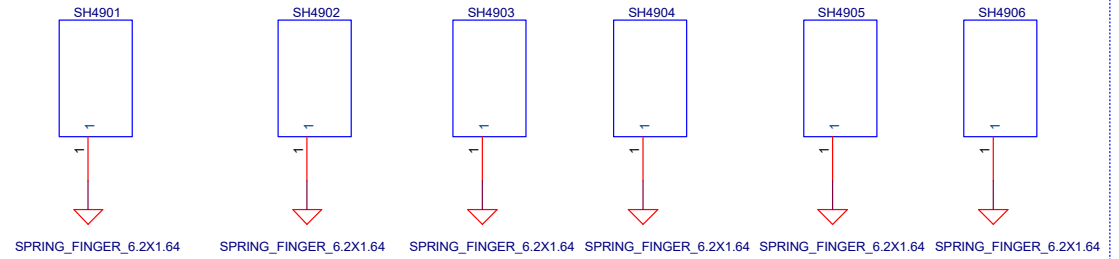
CPU Thermal Hole



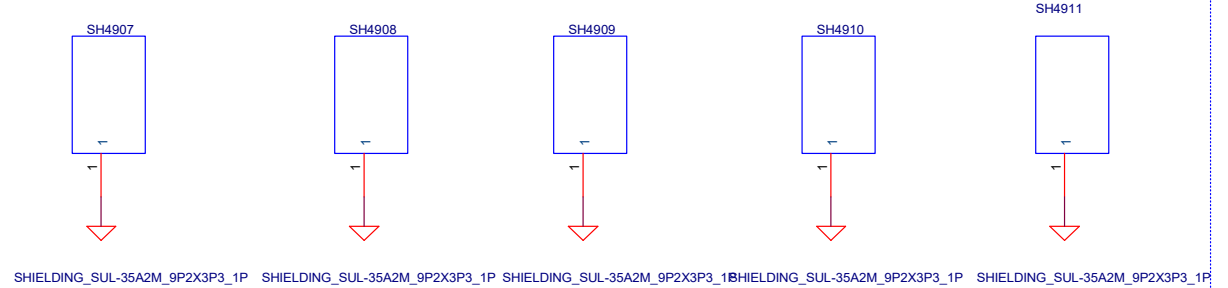
GPU Thermal Hole




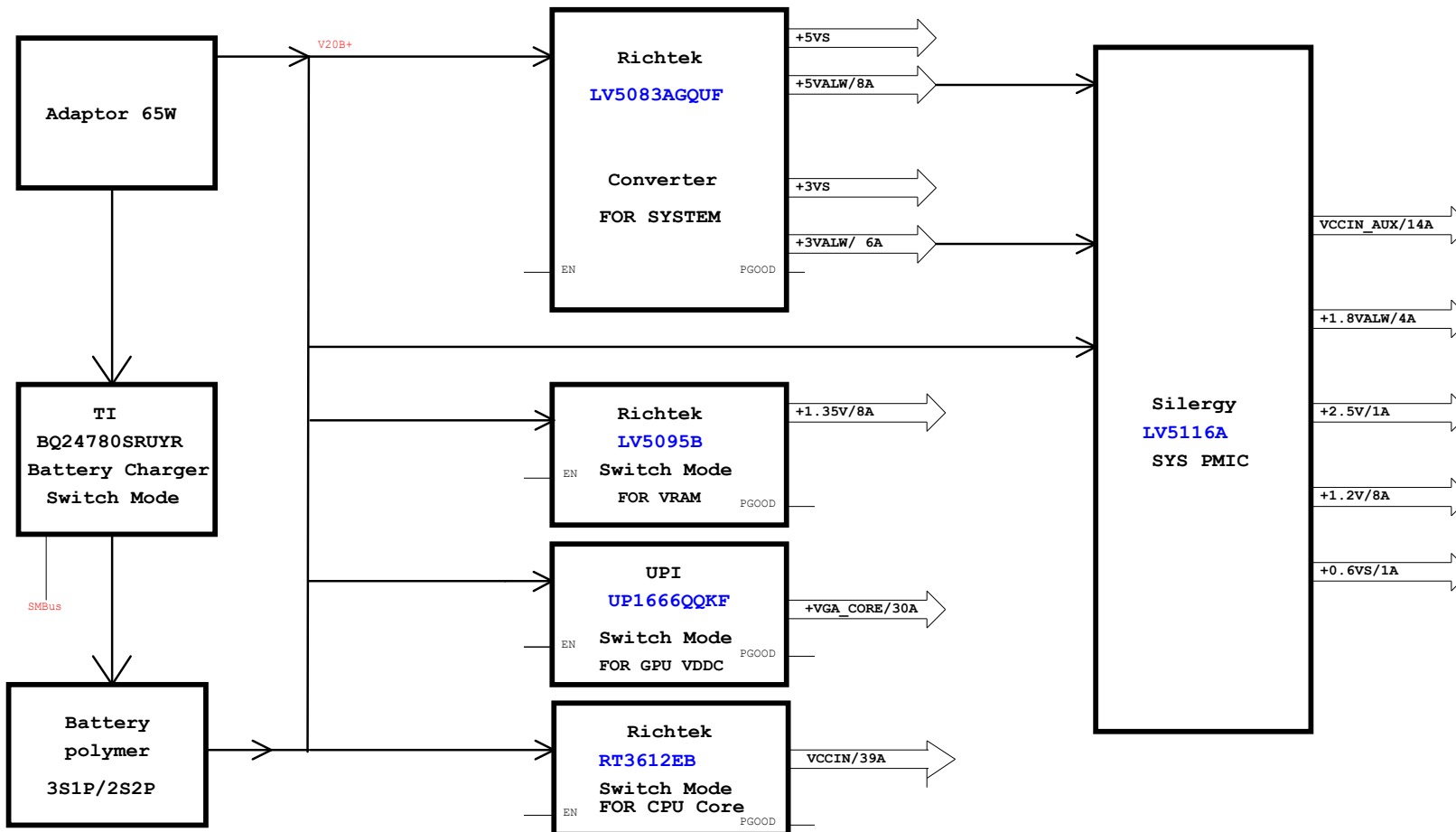
MD Shielding

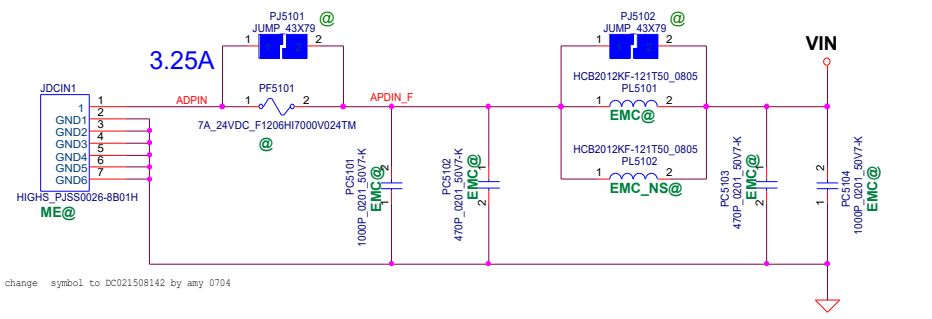


SODIMM Shielding

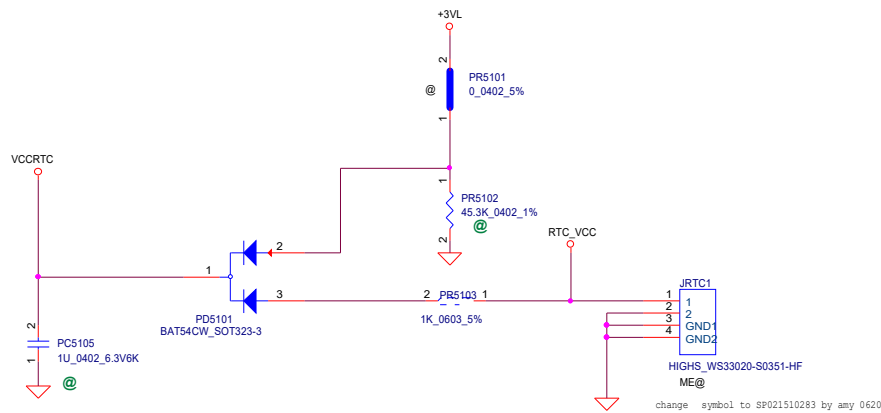


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				B	GS44D/GS54D	0.1
				Date:	Friday, December 06, 2019	Sheet 49 of 60



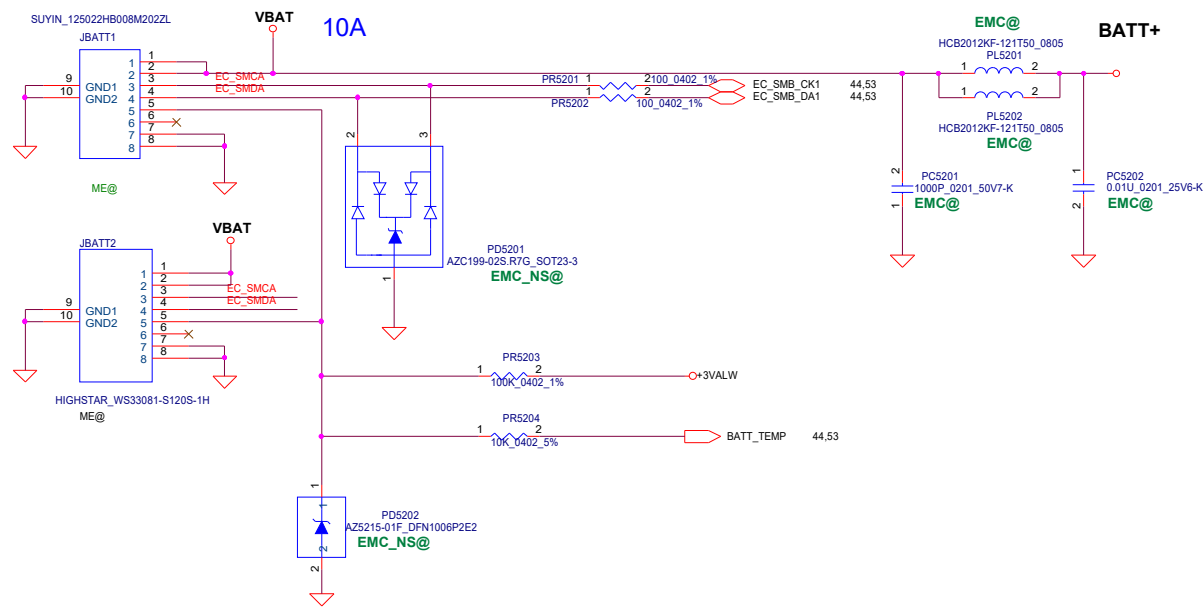


change symbol to DC021508142 by amy 0704

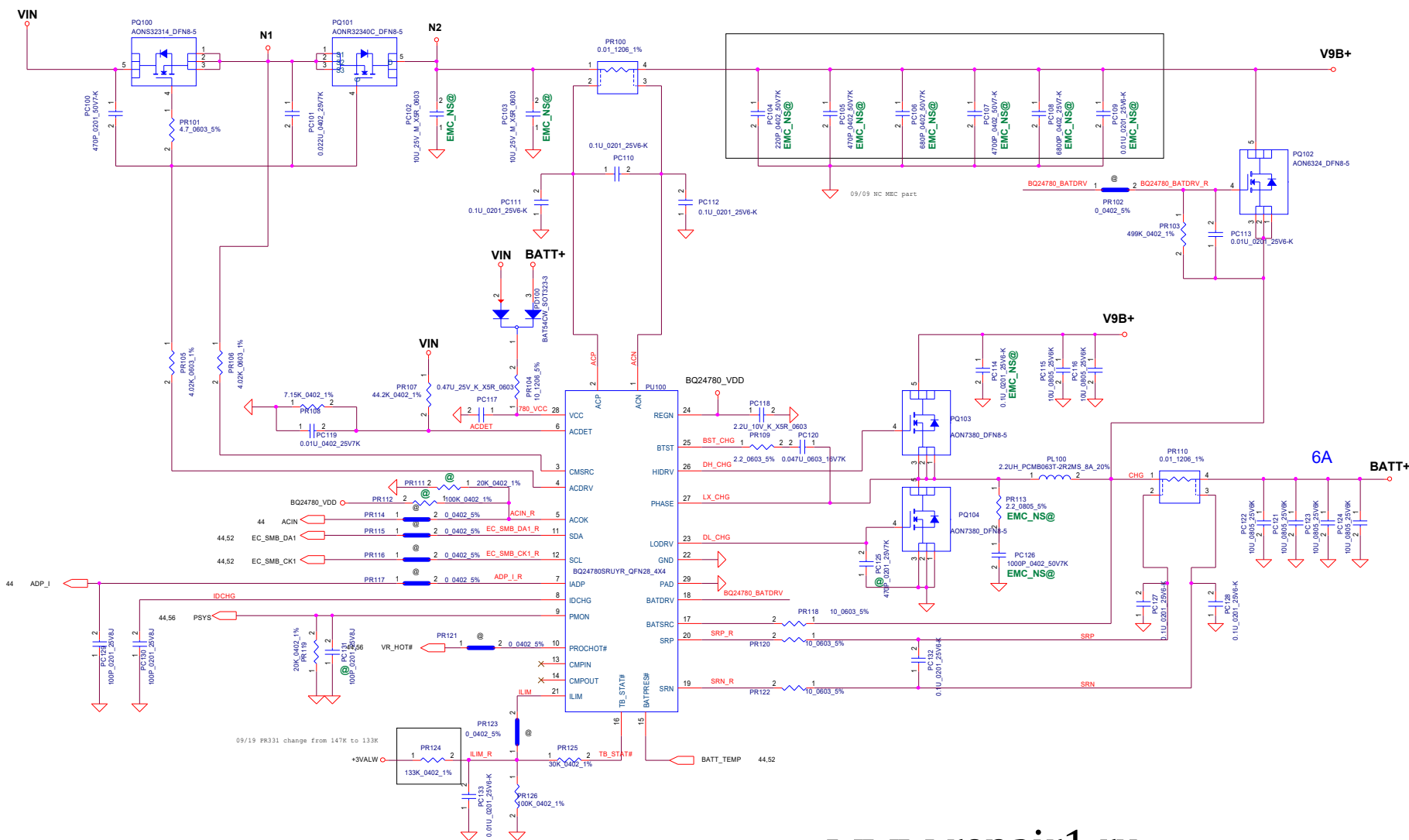


change symbol to SP021510283 by amy 0620

RTC_VCC 20MIL
+3VL 20MIL
VCCRTC 20MIL

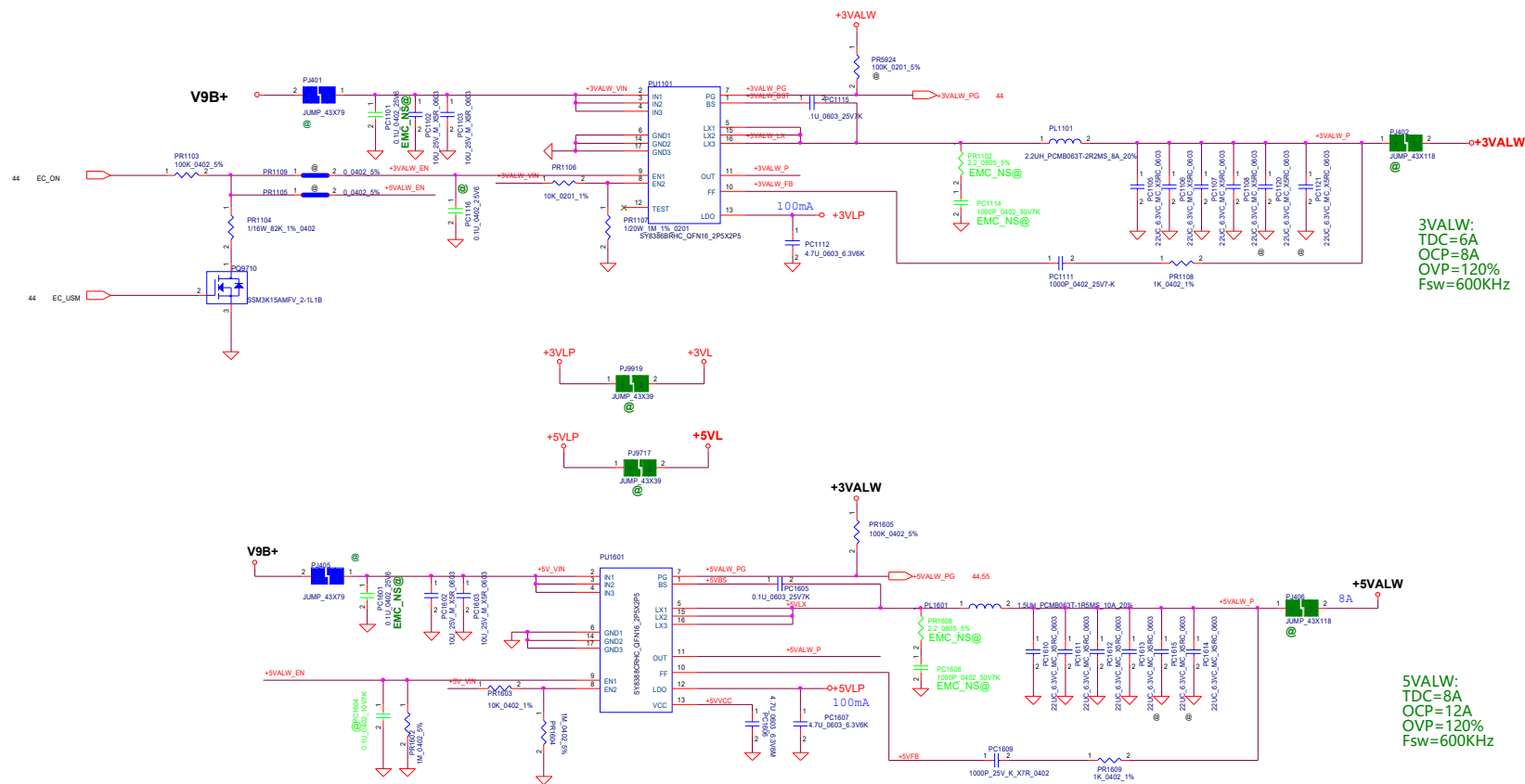


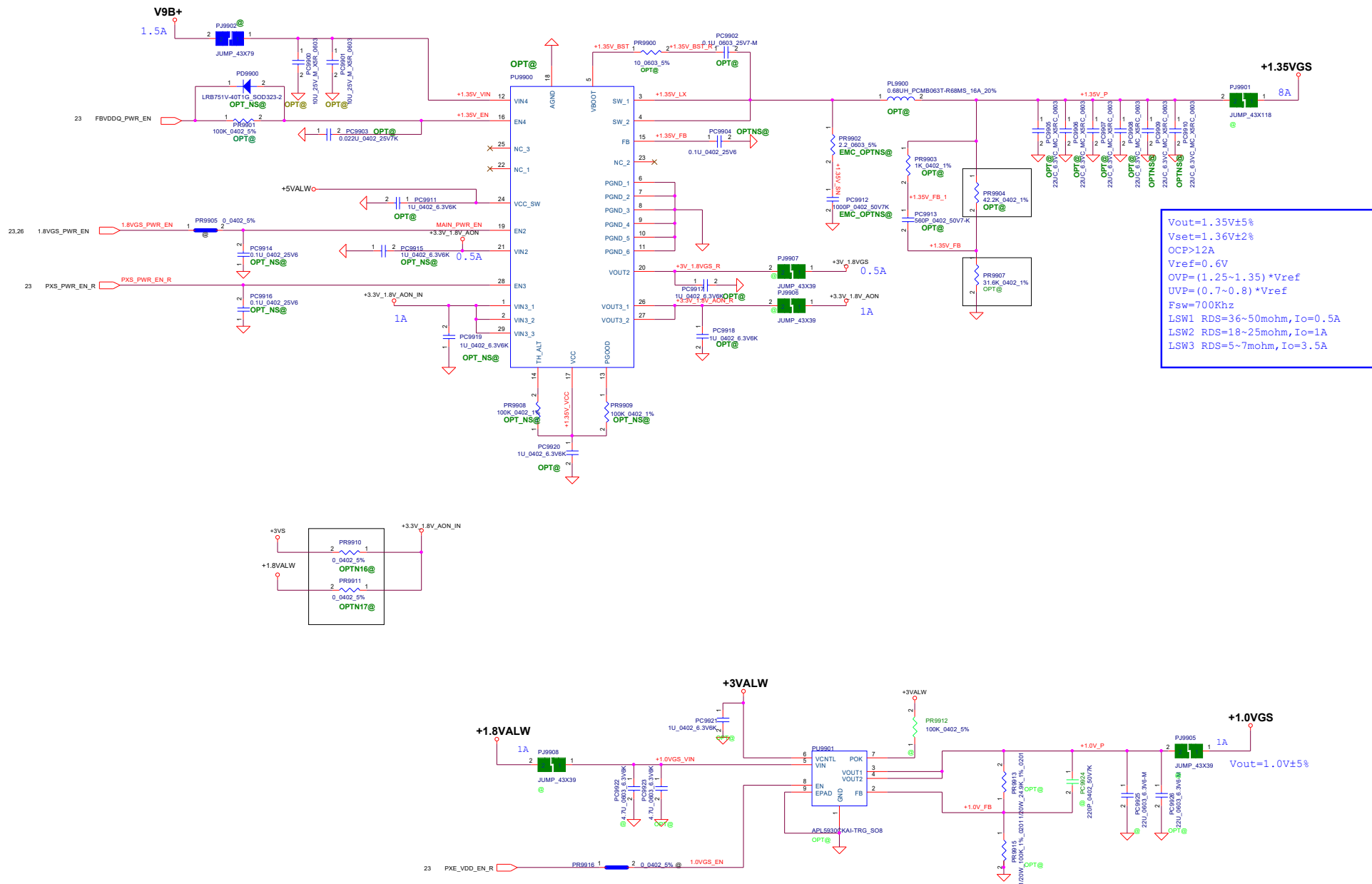
2S1P polymer battery
voltage level: +5.5V ~
8.8 V



ACDECT setting 17.2V
 Charge current limit HW=7A
 DC discharge limit =26A
 Discharge current limit HW=9A during Turbo boost

www.repair1.ru





RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM

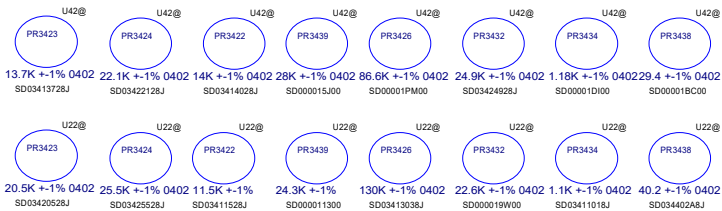
PR816,PR812,PR815,PR813,PR818,PC826 BOM structure control for N16 or N17

Component Value		N17	N16
R1 (K Ω)	PR7017	6.19	20
R2 (K Ω)	PR7011	20.5	20
R3 (K Ω)	PR7016	4.32	2
R4 (K Ω)	PR7013	16.5	18
R5 (K Ω)	PR7019	0.309	0
C (nF)	PC7028	4.7	2.7

UPI_OPT@ : for UP1666
RT_OPT@ : for RT8816A

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				Date	Friday, December 05, 2019
				Sheet	58 of 4

POWER



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C									
B									
A									
								</	