

Compal Confidential

AIWZ0/AIWZ1 DIS M/B Schematics Document

Intel Boardwell U Processor with DDR3L
AMD Meso XT / Tropo XT2

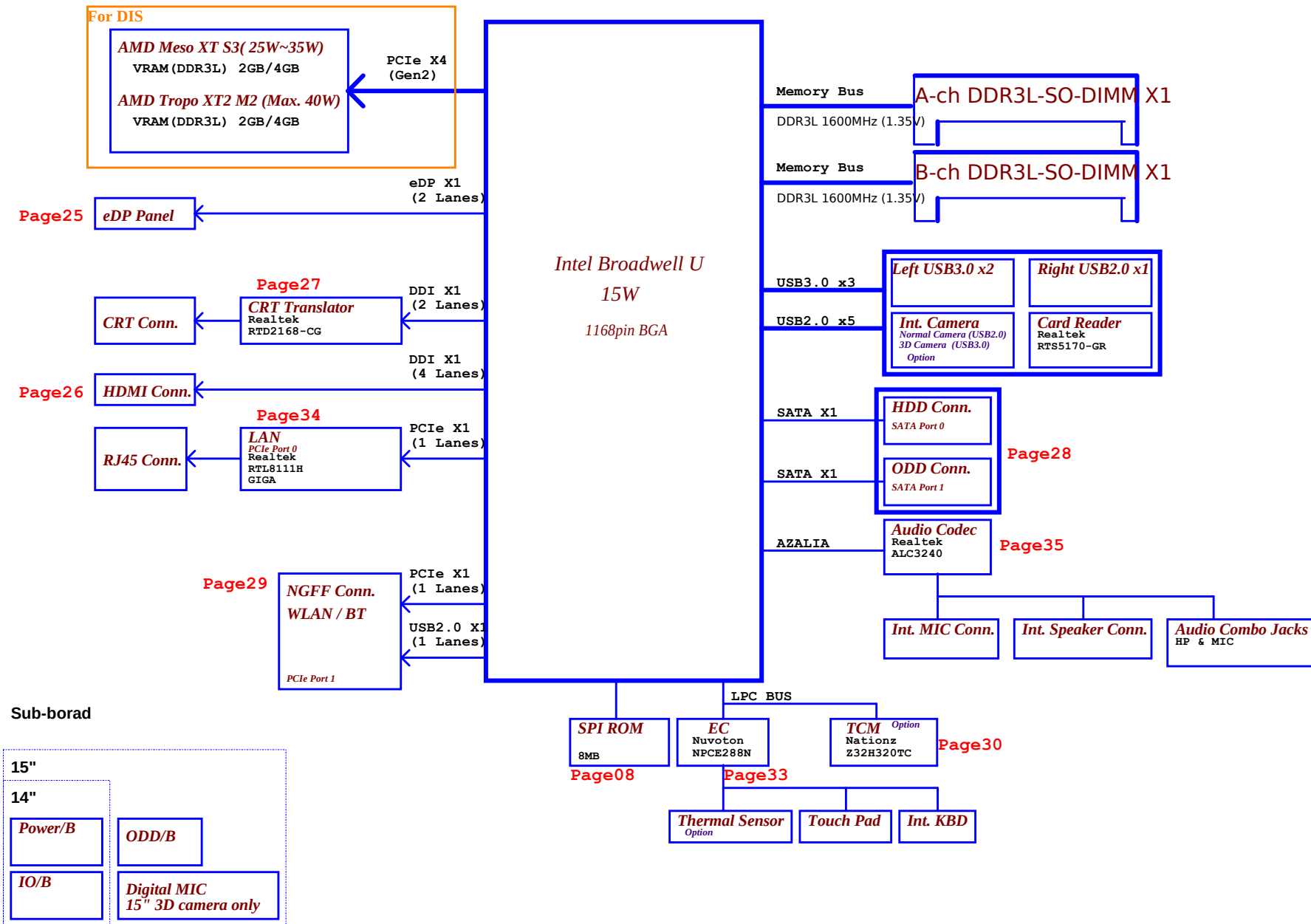
2015-02-02

LA-C281P

REV: : 1.0

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Voltage Rails

<div>power plane</div> <div>State</div>	B+	+5VALW +3VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS +VCC_CORE +VGA_CORE +1.8VS +0.675VS +1.05VS
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011x	Thermal Sensor	0100 1100

PCH SM Bus address

Device	Address	Device	Address
DDR_JDIMM1	1010 000x A0h	Internal thermal sensor	0100 0001 41h
DDR_JDIMM2	1010 010x A4h		

EC SM Bus2 address

AMD-GPU SM Bus address

SMBUS Control Table

<div></div>	SOURCE	CRT	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
EC_SMB_CK1 EC_SMB_DA1	NPCE288 +3VALW	✗	✓ +3VALW	✗	✗	✗	✗	✗
EC_SMB_CK2 EC_SMB_DA2	NPCE288 +3VS	✓ +3VS	✗	✗	✗	✗	✓ +3VS	✓ +3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	✗	✗	✗	✓ +3VS	✗	✗	✗
PCH_SML0CLK PCH_SML0DATA	PCH +3VALW	✗	✗	✗	✗	✗	✗	✗
SML1CLK SML1DATA	PCH +3VALW	✓ +3VS	✗	✓ +3VS	✗	✗	✓ +3VGS	✗

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Sub Board
		3	CardReader
		4	Touch Screen
	UHCI2	5	Camera
		6	Bluetooth (NGFF)
EHCI1	UHCI3	7	
		8	
	UHCI4	9	
		10	
	UHCI5	11	
		12	
	UHCI6	13	

BDW_CPU

UC1
SA000089A60 17-5500U
S IC FH8065801620004 SR23W F0 2.4G C38!
17_5500@

UC1
SA000089970 15-5200U
S IC FH8065801620204 SR23Y F0 2.2G C38!
15_5200@

UC1
SA000089880 13-5010U
S IC FH8065801620406 SR23Z F0 2.1G C38!
13_5010@

UC1
SA000083EH0 13-5005U
S IC FH8065801884006 SR244 F0 2G C38!
13_5005@

PCB

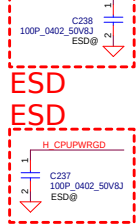
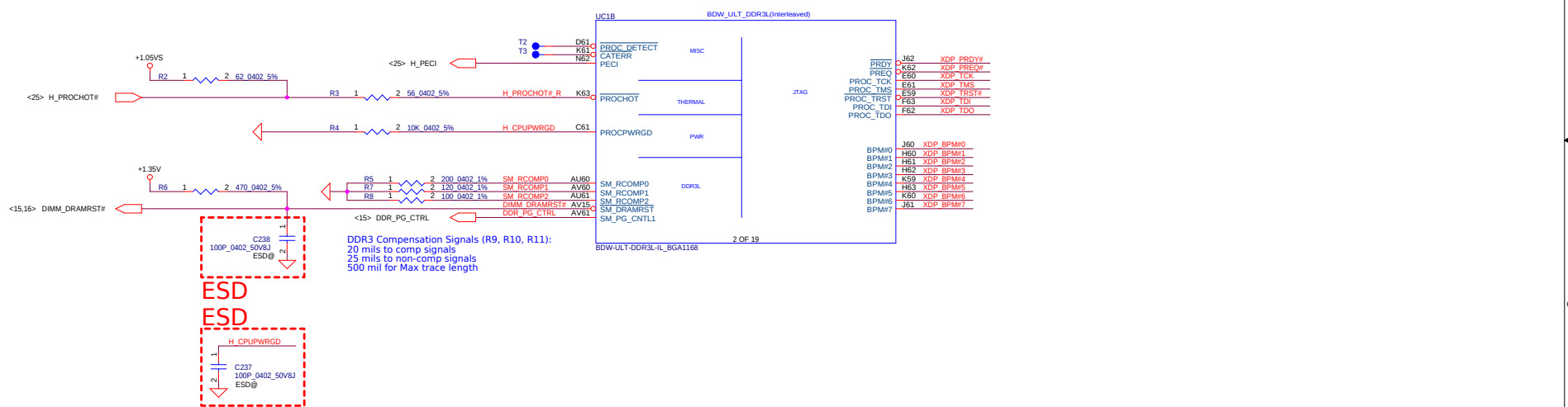
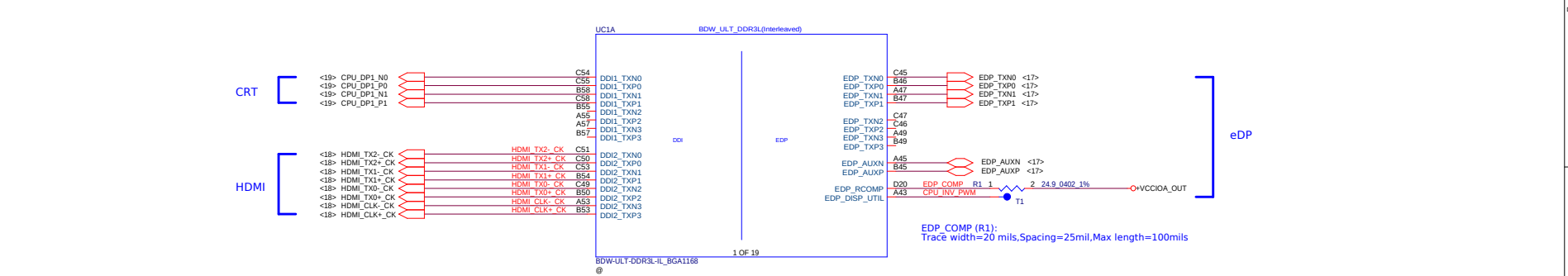
ZZZ
DA218J00101
PCB AIWZ0 LA-C281P L.S-C281P/C282P 02
Z14@
PCB AIWZ0 LA-C281P L.S-C281P/C282P 02

ZZZ
DA218J00101
PCB AIWZ1 LA-C281P L.S-C281P/C282P/C283P/C285P/C286P 02
Z15@
PCB AIWZ1 LA-C281P L.S-C281P/C282P/C283P/C285P/C286P 02

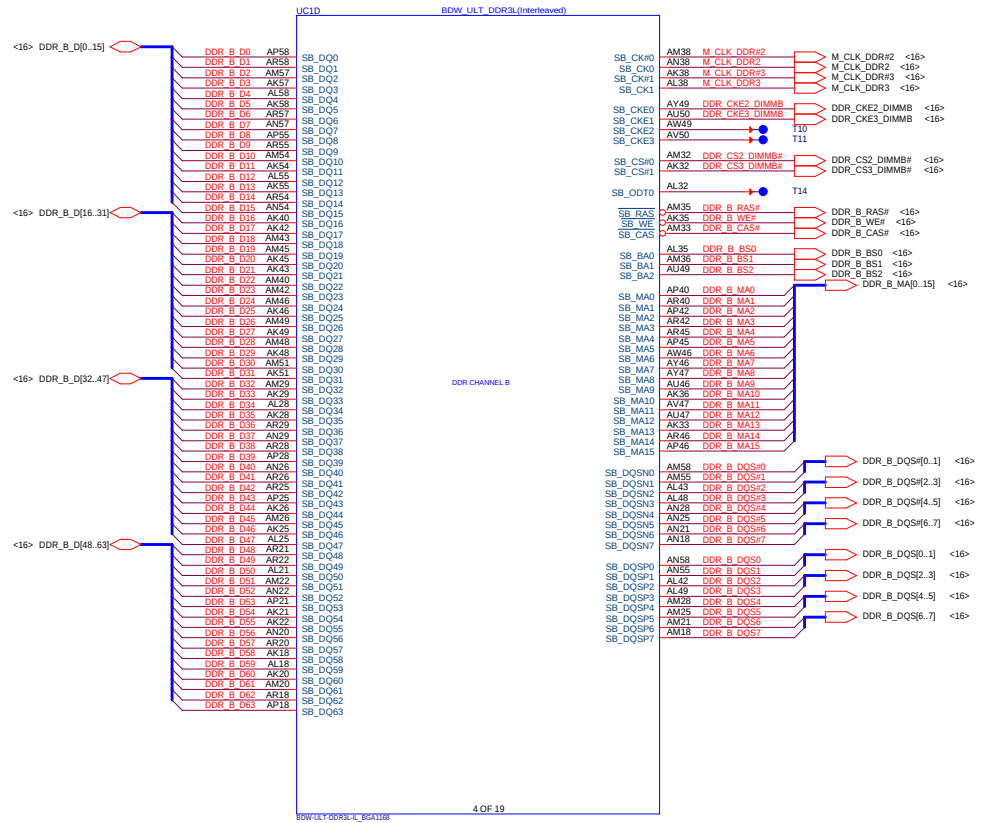
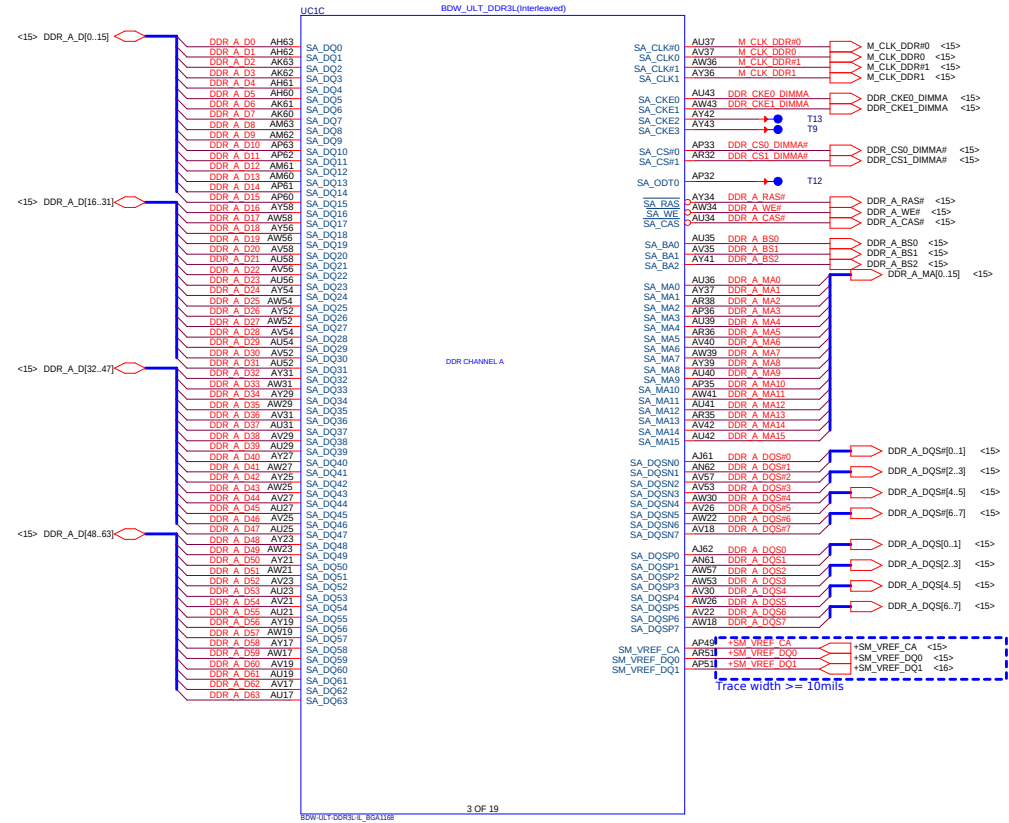
BOM Structure Table

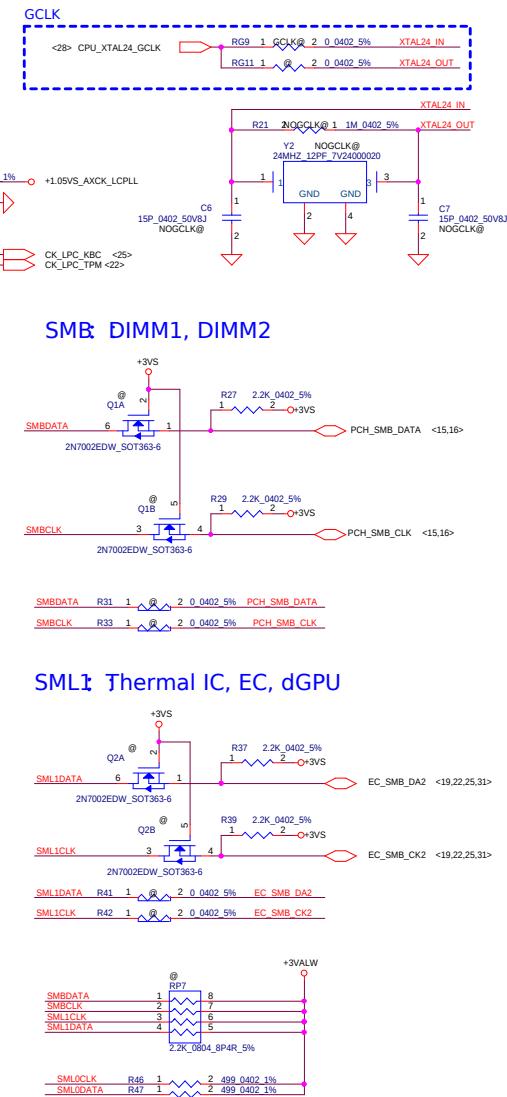
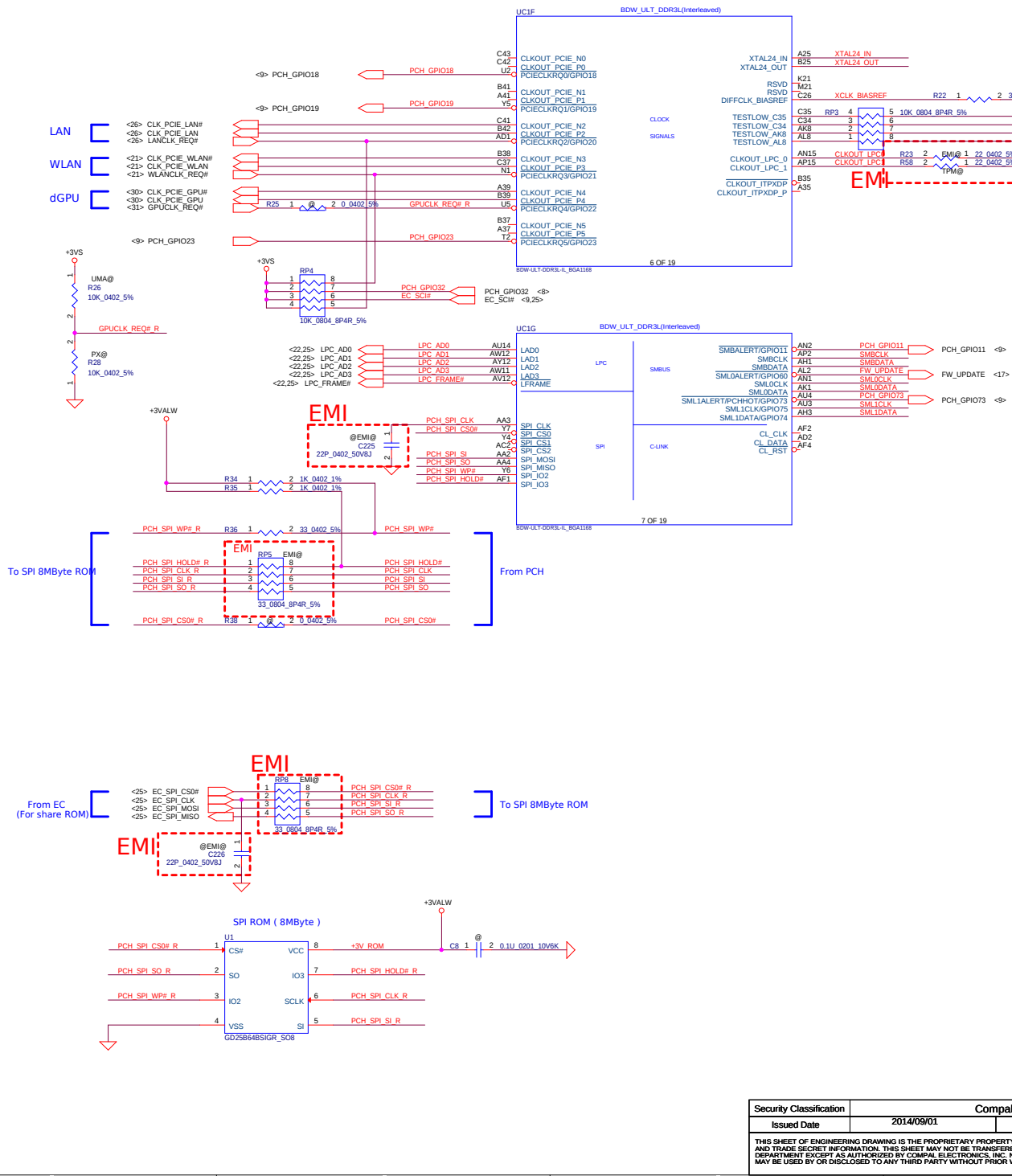
Item	BOM Structure
AIWZ0 (14")	Z14@
AIWZ1 (15")	Z15@
AIWZ0 (17")	Z17@
LAN Switch mode	SWITCH@
LAN RTL8111GS-CG	8111GLDO@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NOISCT@
For Green CLK	GCLK@
For No Green CLK	NOGCLK@
Green CLK IC For DIS	GCLKDIS@
Green CLK IC For UMA	GCLKUMA@
For system DIS	PX@
For TROPO DIS pop	DIS@
For TROPO DIS unpop	@DIS@
For UMA	UMA@
3D Camera	3DCMOS@
Camera	CMOS@
HDMI	HDMI@
NO keyboard backlight	NOKBL@
Keyboard backlight	KBL@
HDMI Royalty	45@
Connector	ME@
Un-pop component for EMI	@EMI@
Un-pop component for ESD	@ESD@
pop component for EMI	EMI@
pop component for ESD	ESD@
Un-pop for TPM	TPM@
pop for TFM	NOTPM@
VRAM indentify	X76@
For TROPO function	TROPO@
ADB function	ADB@
NO ADB function	NOADB@
CPU_SA000083E30	QGZ3@
CPU_SA000083C10	QH17@
CPU_SA00007AM00	QFSY@
CPU_SA000083A10	QH15@
CPU_SA000083D30	QH18@
CPU_SA00007UG00	QGHA@
CPU_SA00007UH00	QGHB@
CPU_SA00007U900	QGH9@

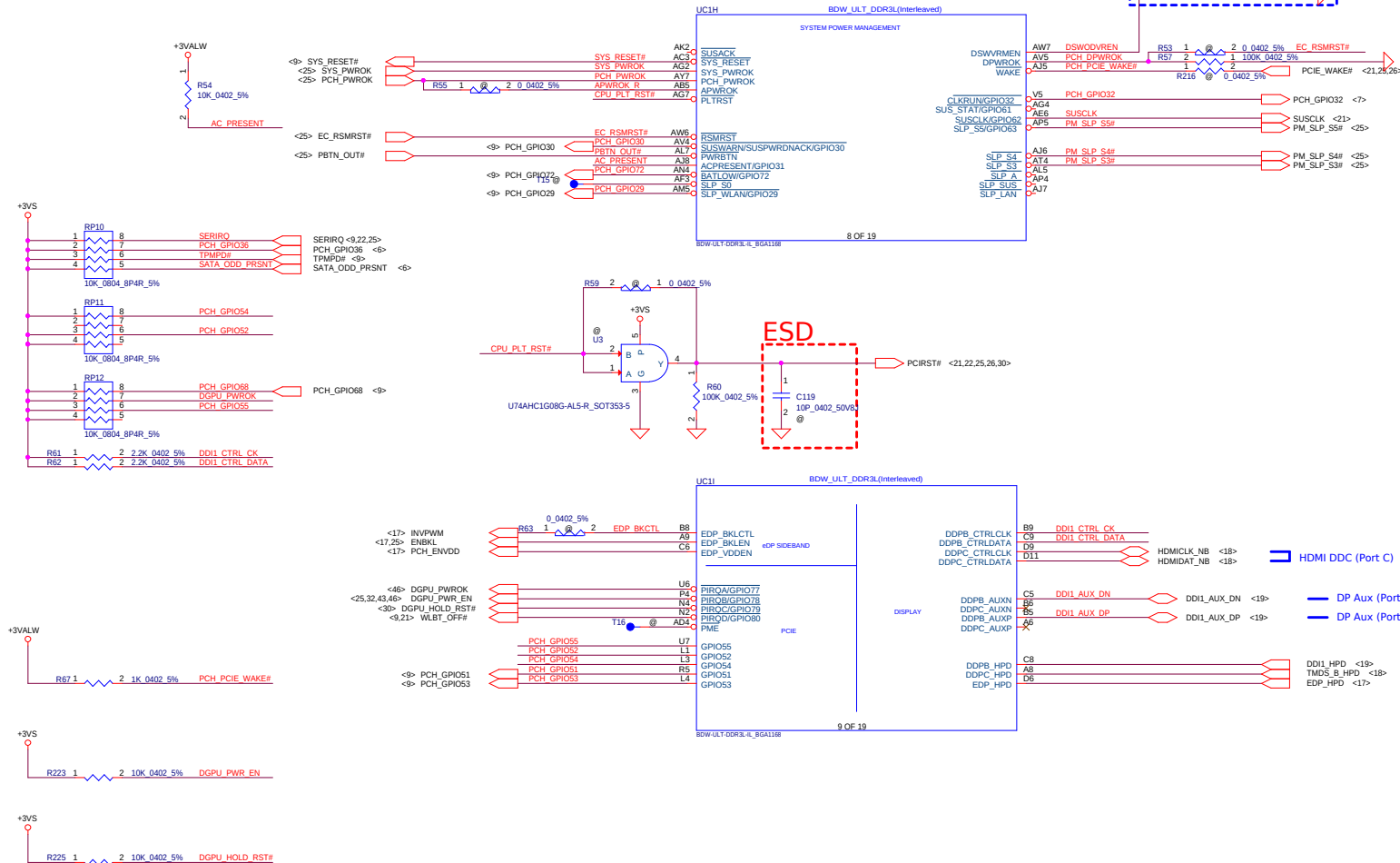
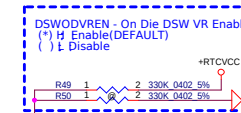
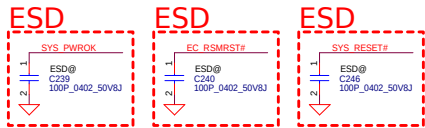
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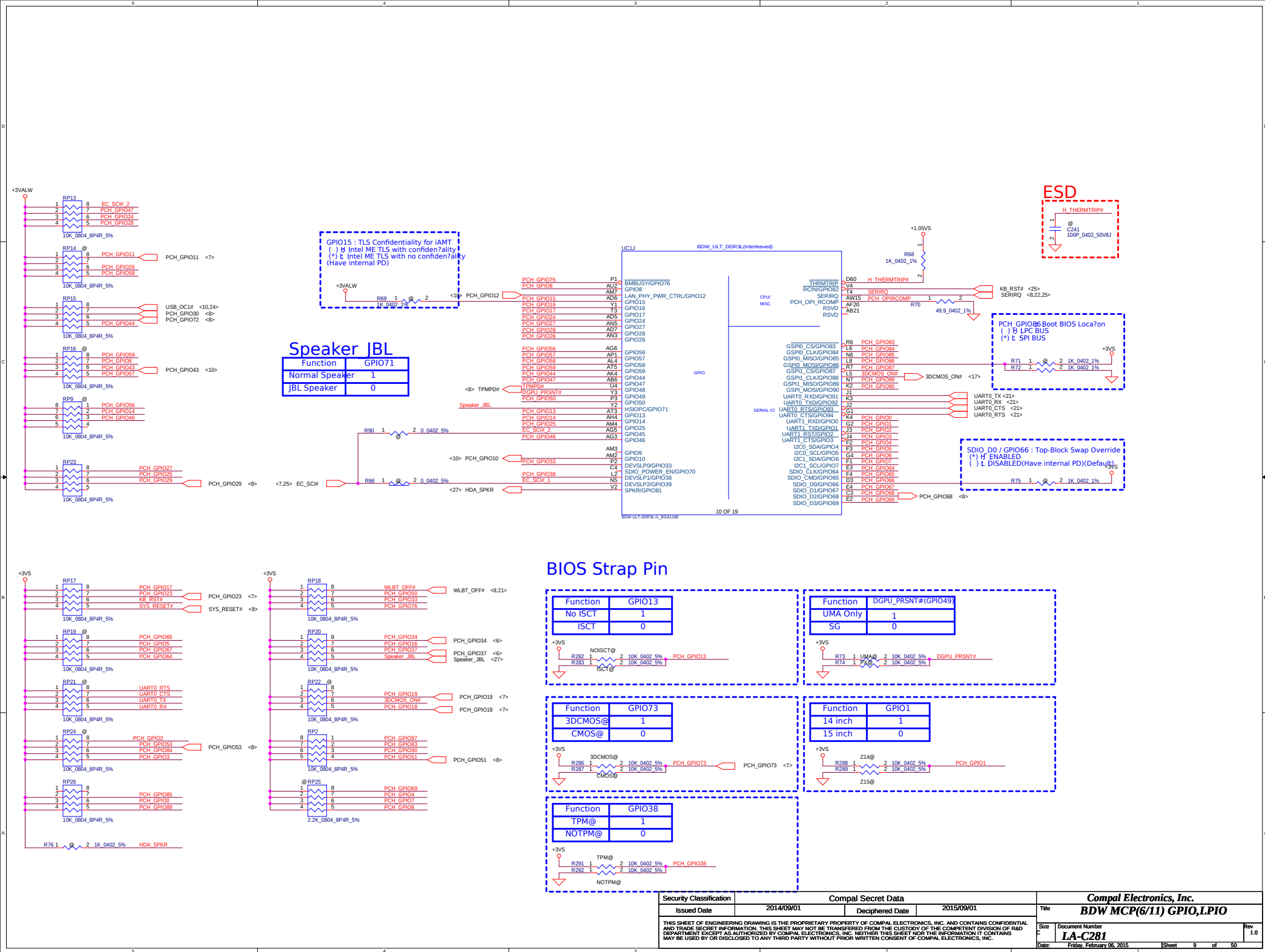
Interleaved Memory

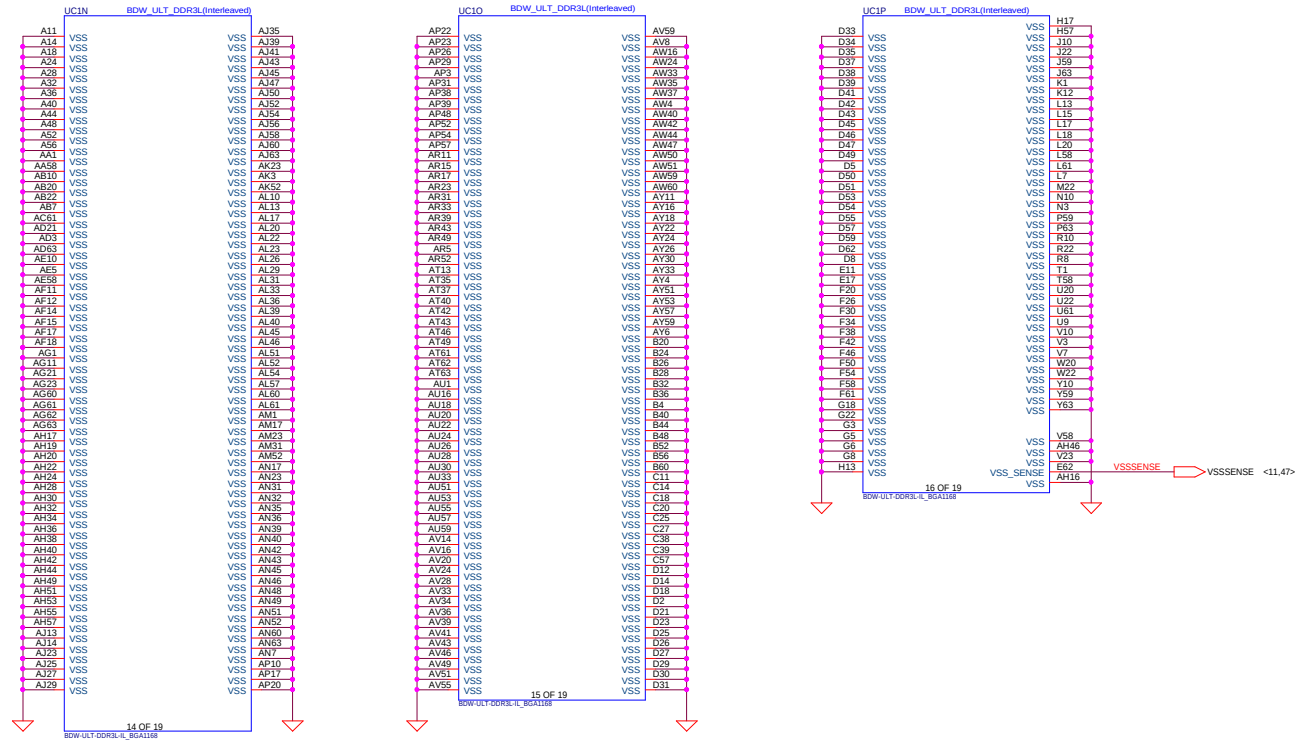


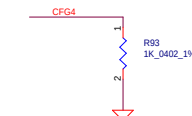
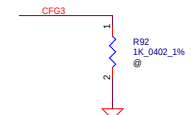




Security Classification	Compal Secret Data			Compal Electronics, Inc.	
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Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

Display Port Presence Strap	
CFG4	<p>1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>

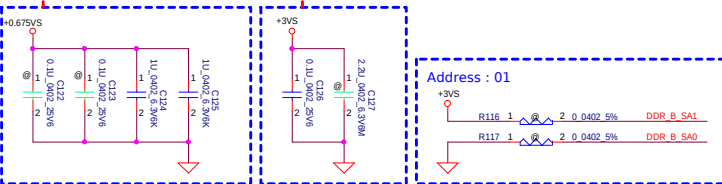
The diagram illustrates the connection of various signals between the CPU and the DQ070000. The signals are organized into four main categories, each with a dashed blue border:

- D/Q Signals link to CPU:**
 - << DDR_B_D[0..63] connects to DQ070000.DQ[0..63]
 - << DDR_B_DQS[0..7] connects to DQ070000.DQS[0..7]
 - << DDR_B_DQS[0..7] connects to DQ070000.DQS[0..7]
 - << DDR_B_MA[0..15] connects to DQ070000.DMA[0..15]
- CMD Signals from CPU:**
 - << DDR_B_BS0 connects to DQ070000.DBS0
 - << DDR_B_BS1 connects to DQ070000.DBS1
 - << DDR_B_BS2 connects to DQ070000.DBS2
 - << DDR_B_RAS# connects to DQ070000.DRAS#
 - << DDR_B_WE# connects to DQ070000.DWE#
 - << DDR_B_CAS# connects to DQ070000.DCAS#
- Clock Signals from CPU:**
 - << M_CLK_DDR0 connects to DQ070000.M_CLK_DDR0
 - << M_CLK_DDR2 connects to DQ070000.M_CLK_DDR2
 - << M_CLK_DDR3 connects to DQ070000.M_CLK_DDR3
 - << M_CLK_DDR3 connects to DQ070000.M_CLK_DDR3
- CTL Signals from CPU:**
 - << DDR_CKE2_DIMM connects to DQ070000.DCKE2_DIMM
 - << DDR_CKE3_DIMM connects to DQ070000.DCKE3_DIMM
 - << DDR_CS2_DIMMH connects to DQ070000.DCS2_DIMMH
 - << DDR_CS2_DIMML connects to DQ070000.DCS2_DIMML
 - << DDR_CS3_DIMMH connects to DQ070000.DCS3_DIMMH
 - << DDR_CS3_DIMML connects to DQ070000.DCS3_DIMML
- SMBUS Signals link to CPU:**
 - <<715> PCH_SMB_DATA connects to DQ070000.PCH_SMB_DATA
 - <<715> PCH_SMB_CLK connects to DQ070000.PCH_SMB_CLK



The top diagram shows a +1.35V supply connected to a parallel combination of four capacitors: C105, C106, C107, and C108. Each capacitor is labeled with its value, 100.0002 8.376V. The bottom diagram shows a +1.35V supply connected to a parallel combination of eight capacitors: C111, C112, C113, C114, C115, C116, C117, and C118. Each capacitor is labeled with its value, 100.0002 8.376V.

Layout Note:
Place near JDIMM2.199

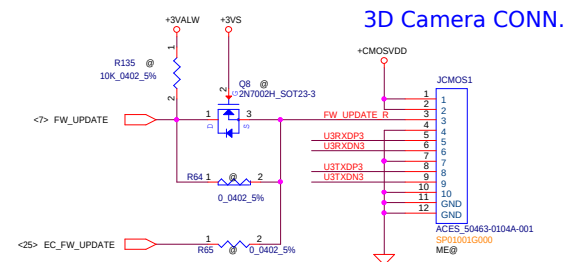
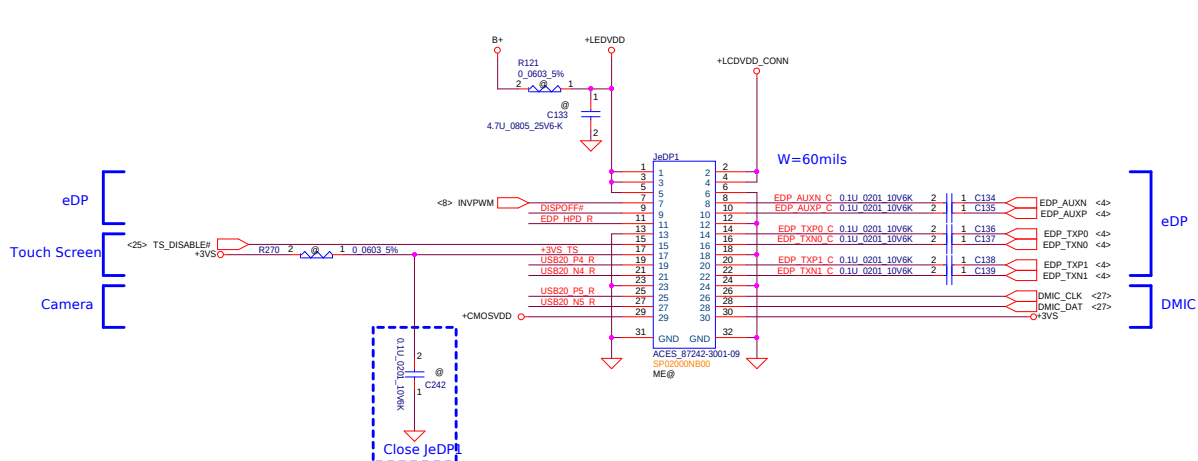
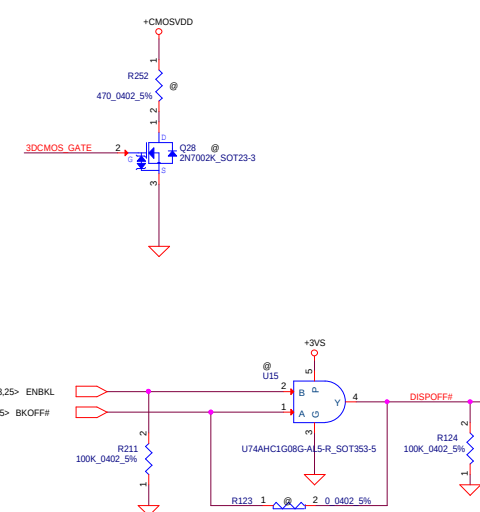


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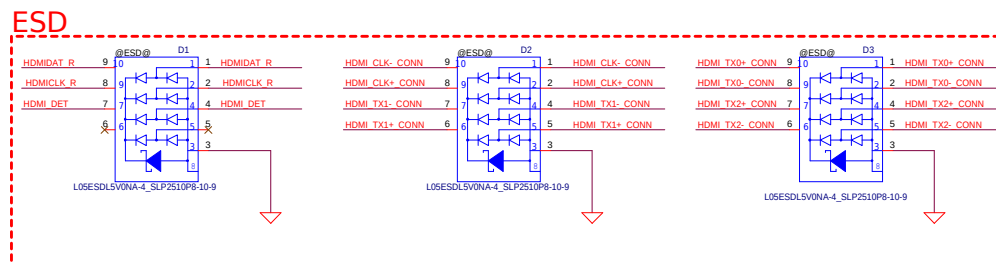
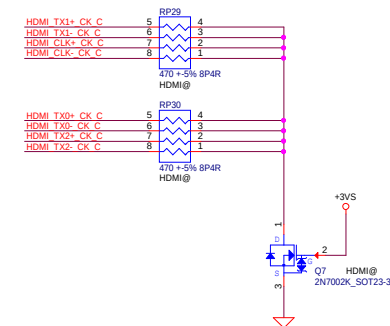
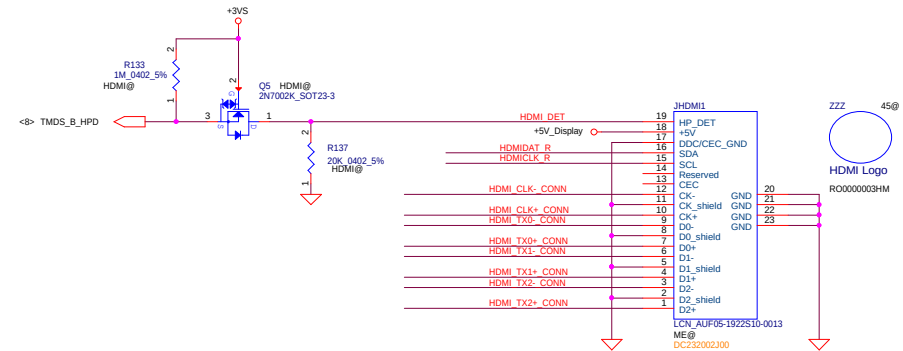
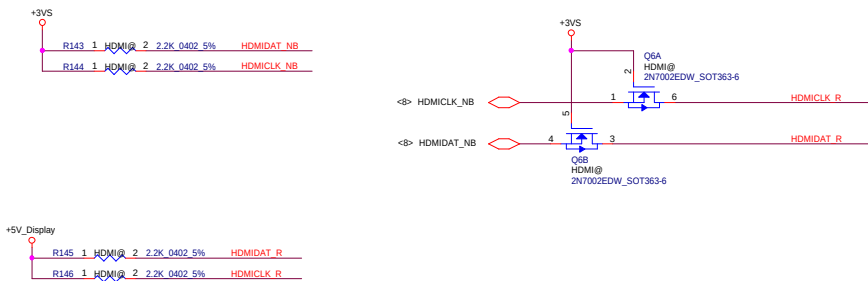
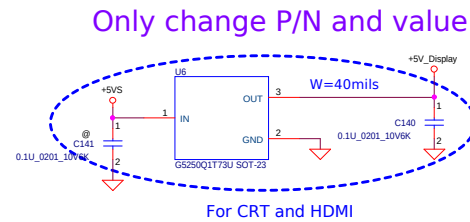
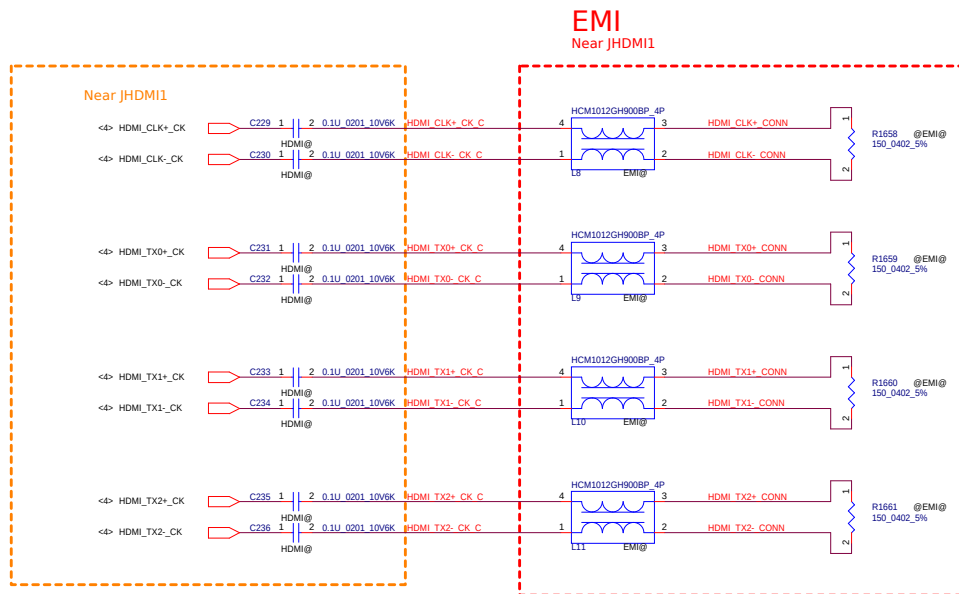
R116 1 2 0 0402 5% DDR_B SA1

R117 1 2 0 0402 5% DDR_B SA0

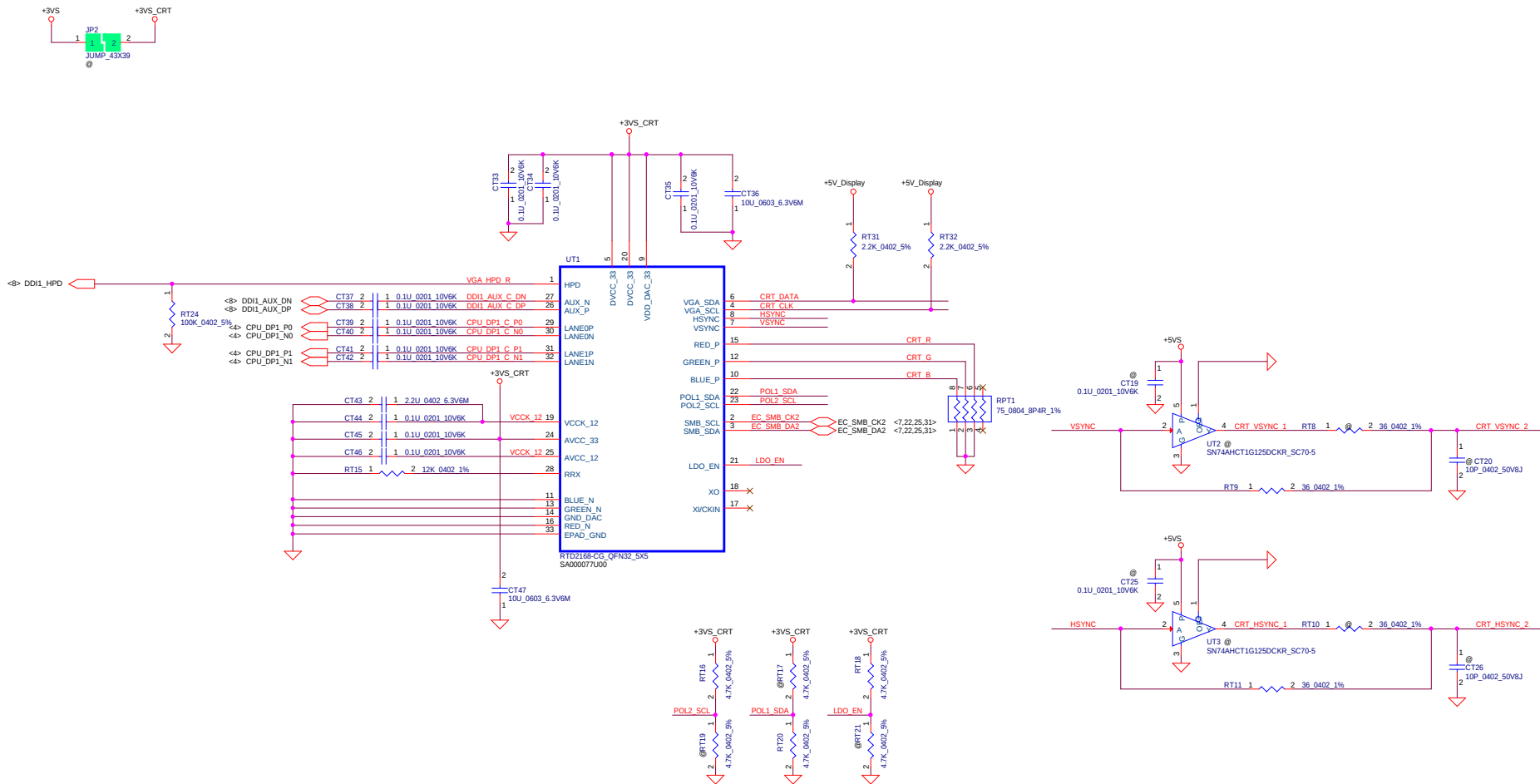
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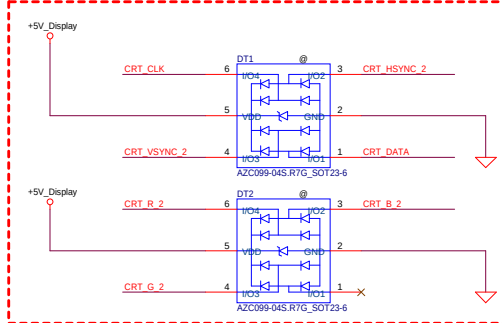
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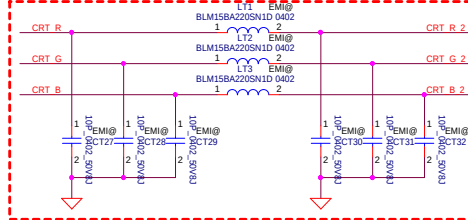
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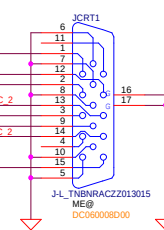
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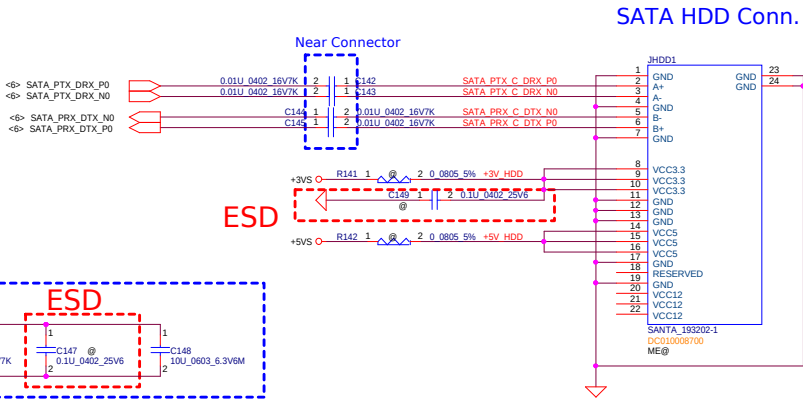


CRT

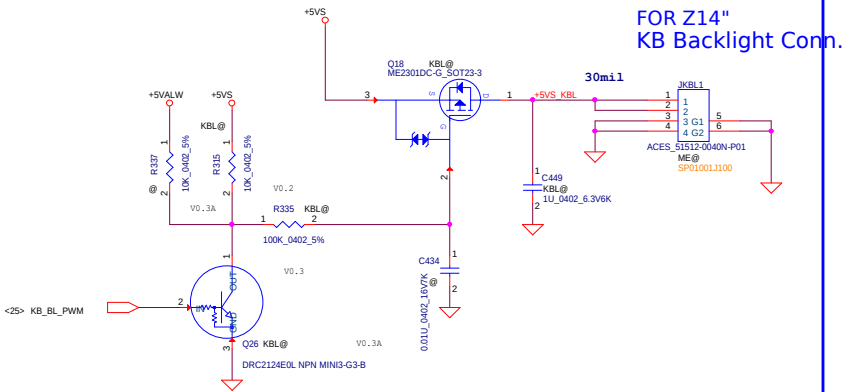


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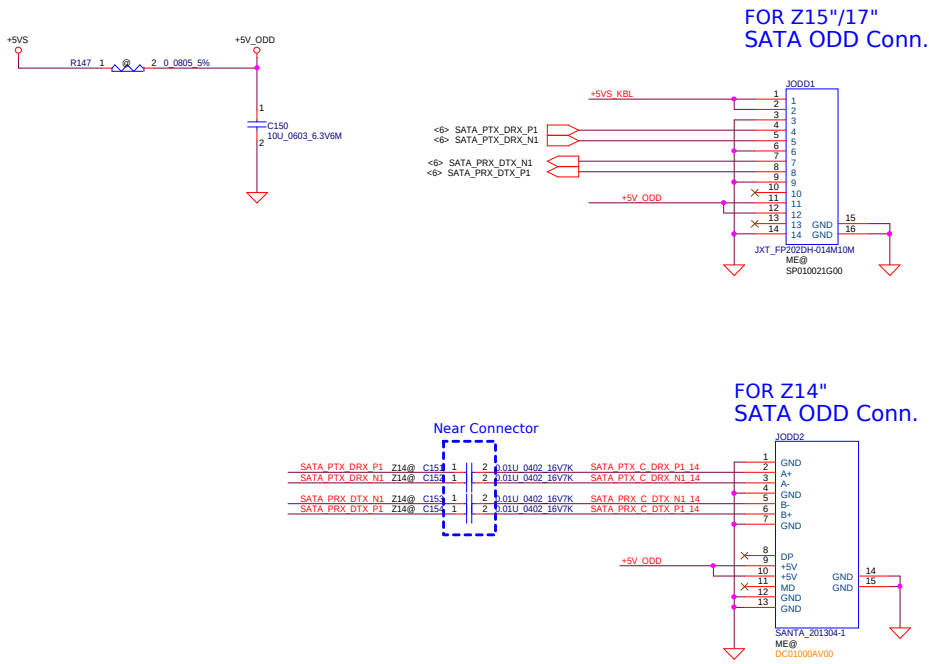
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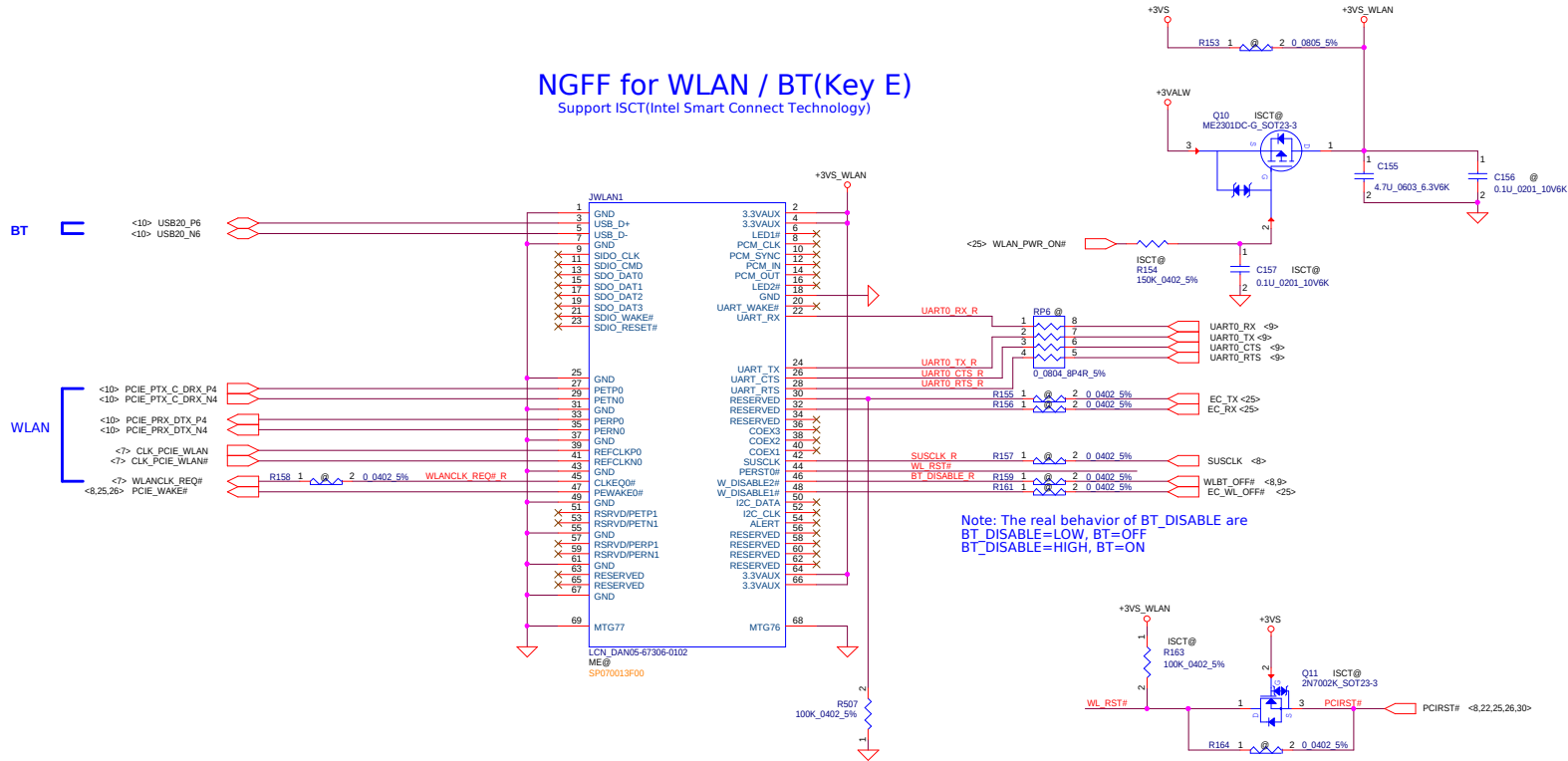
KB Backlight



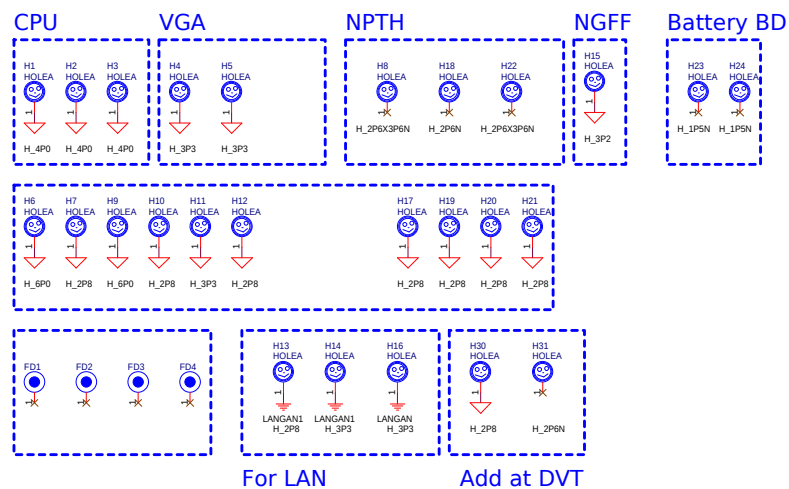
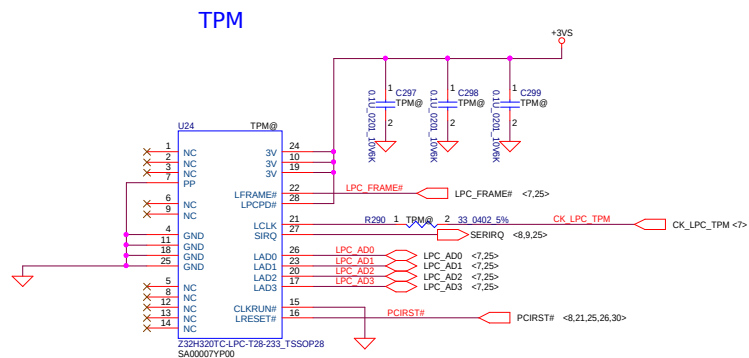
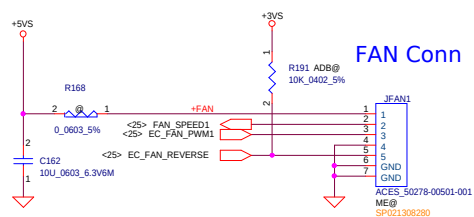
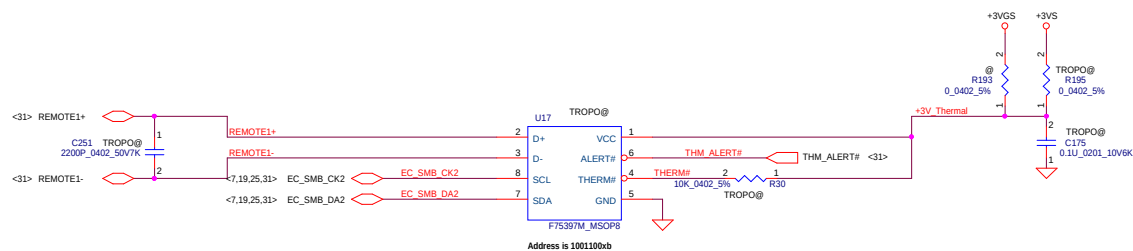
ODD



NGFF for WLAN / BT(Key E) Support ISCT(Intel Smart Connect Technology)

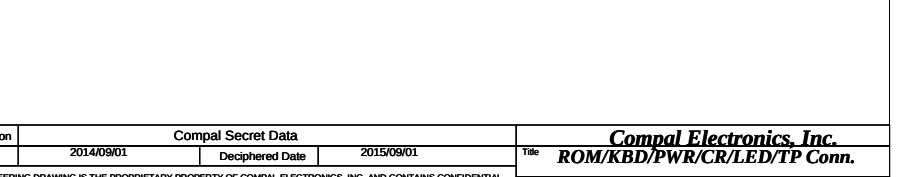
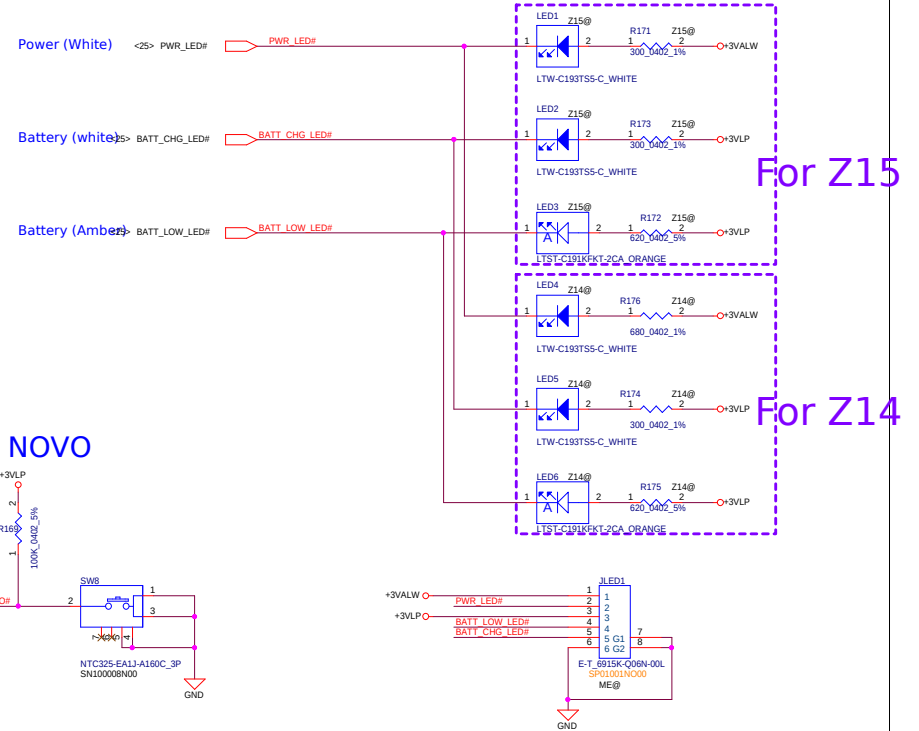
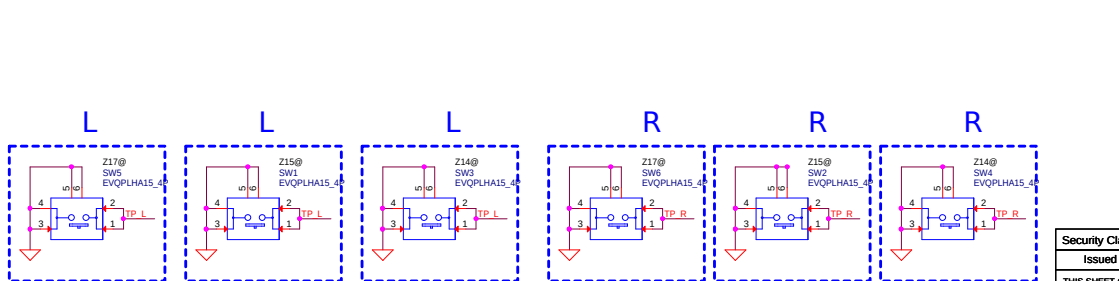
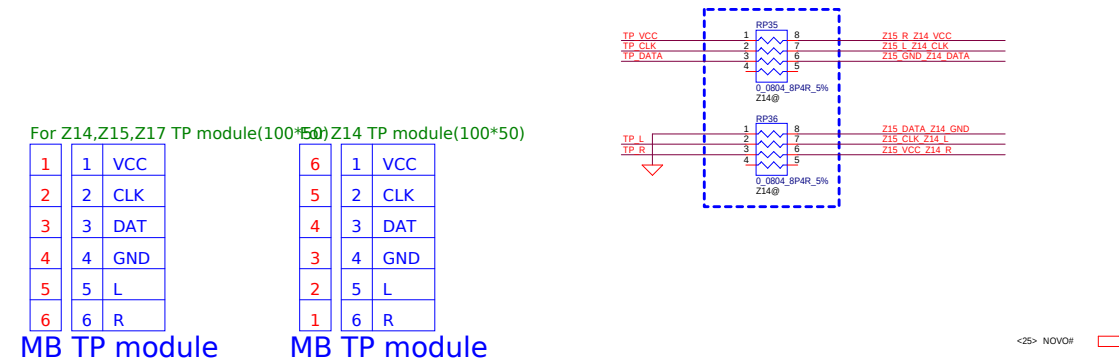
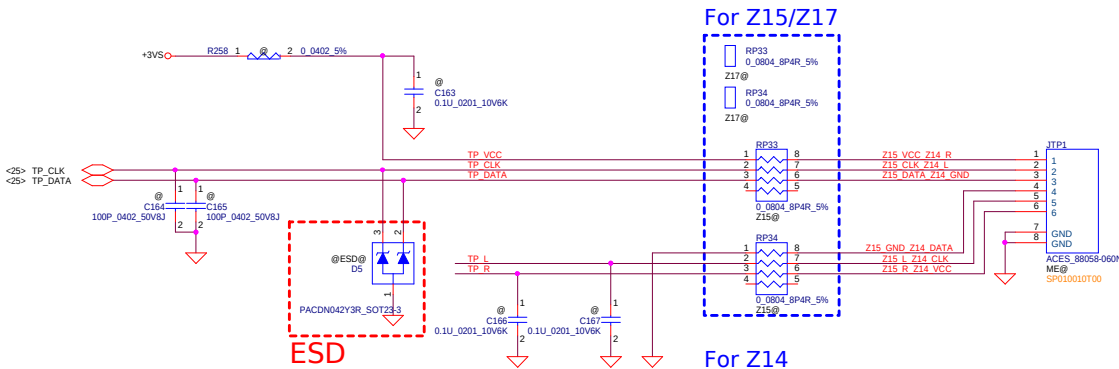
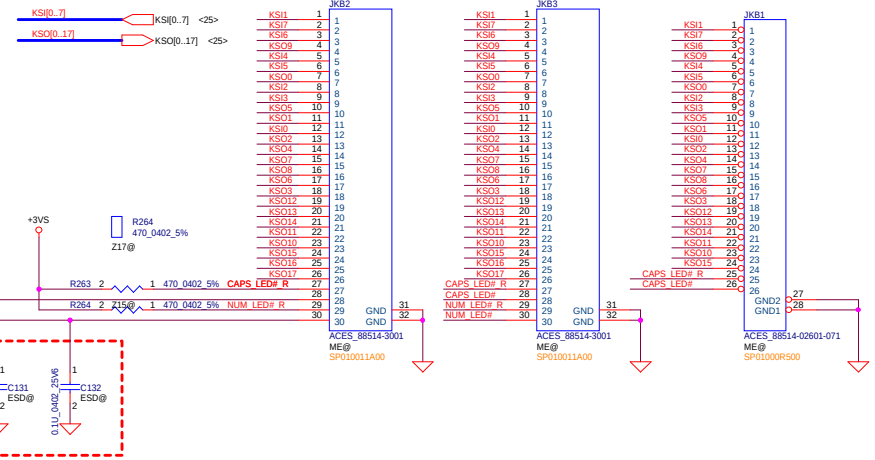
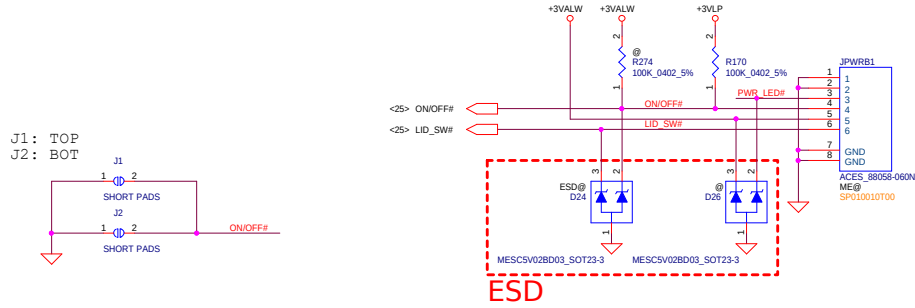


2 Channel



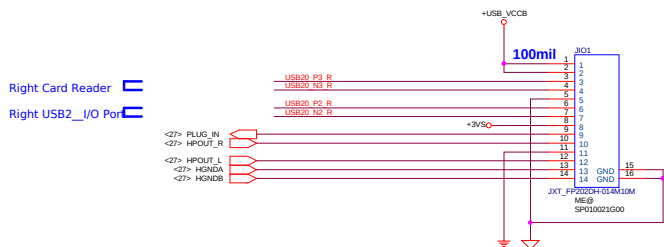
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				Date: Friday, February 06, 2015	Sheet 22 of 50

KB For Z15 KB For Z17 KB For Z14



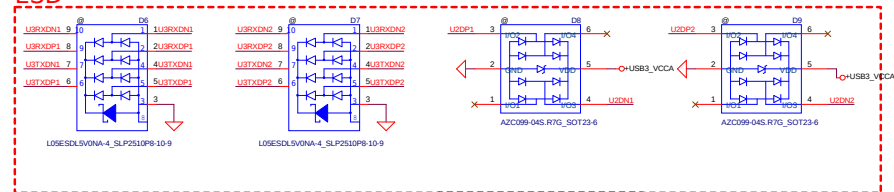
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Issued Date	2014/09/01	Deciphered Date	2015/09/01
Title		Compal Electronics, Inc. ROM/KB/PWR/CR/LED/TP Conn.	
Size	C	Document Number	LA-C281
Date:	Friday, February 06, 2015	ISheet	23 of 50

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[illegible]

Right Card Reader ☐

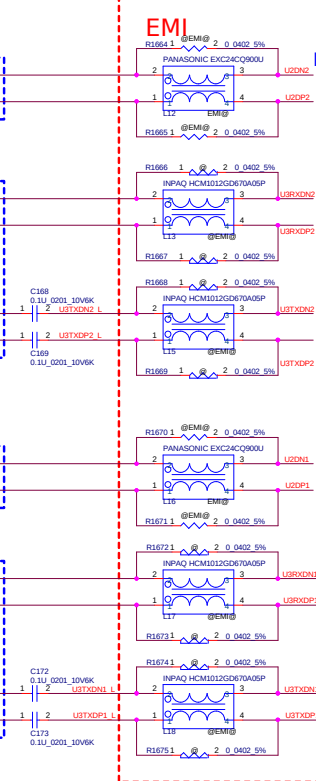
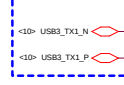
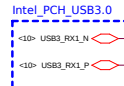
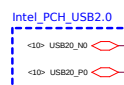
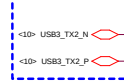
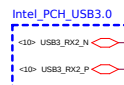
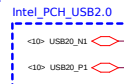
Right USB2 I/O Port ☐



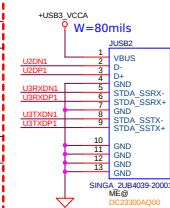
Intel PCH USB2.0

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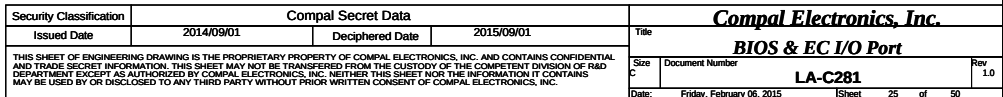
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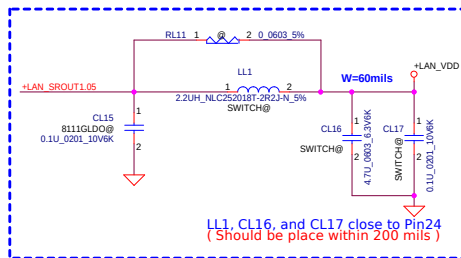
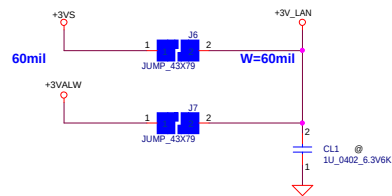


Left USB CONN

[illegible]

Security Classification	Compul Secret Data		Title		Compul Electronics, Inc.	
Issued Date	20140901	Deciphered Date	20150901	USB3.0/Left USB Ports		
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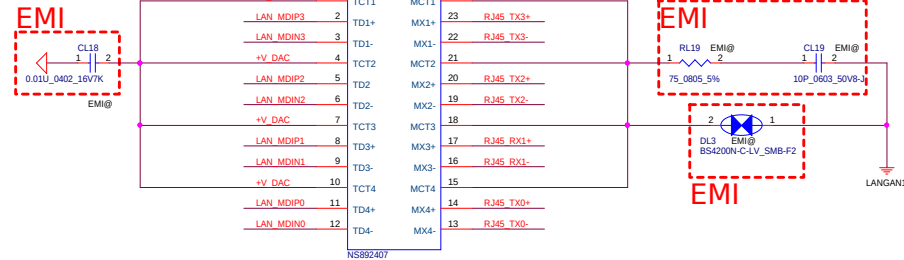
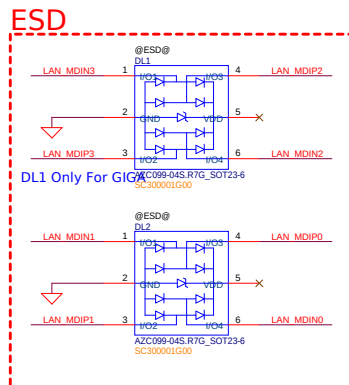
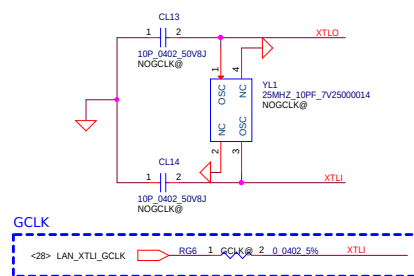
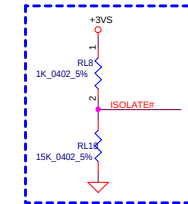
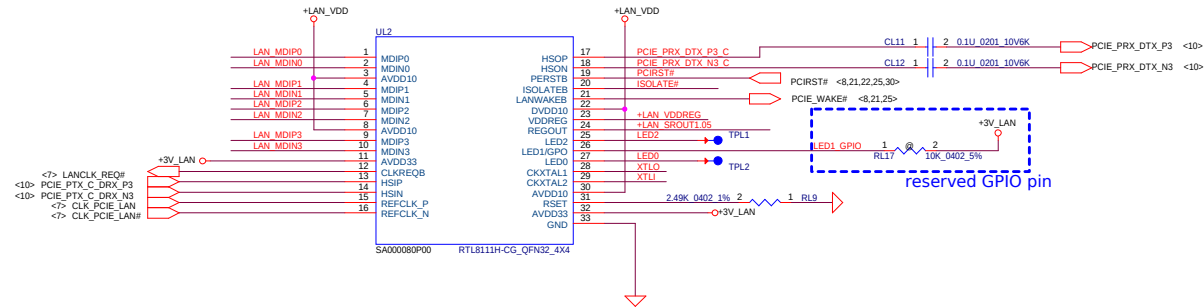
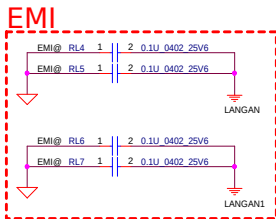
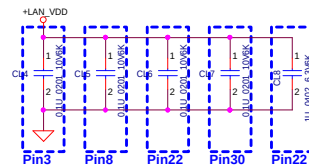
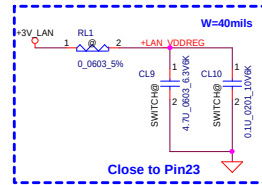
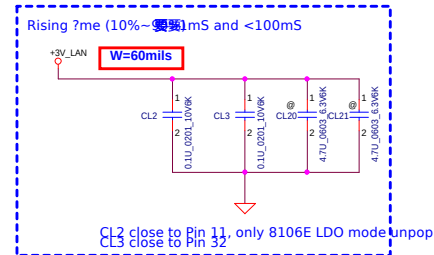
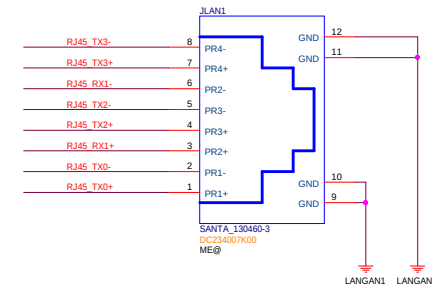
SA00005V700

SA00005V700

Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.

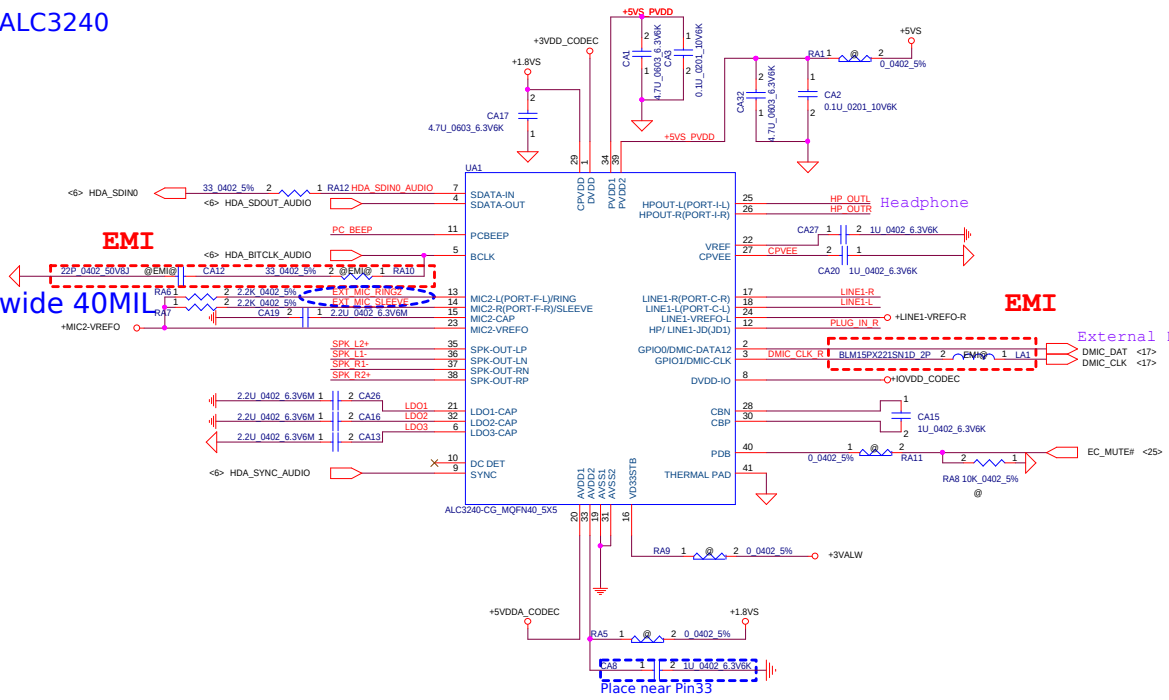
	1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
RTL8111G	LDO	X	X	X	O	O
RTL8111G	External	X	X	X	X	O
RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
RTL8106E	LDO	X	X	X	X	X

RJ-45 CONN.

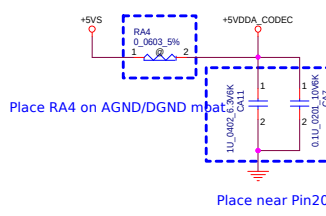


Security Classification	Compal Secret Data	Compal Electronics, Inc.
Issued Date	2014/09/01	Deciphered Date
Deciphered Date	2015/09/01	Size
Size	Document Number	LAN RTL8111/8106
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of	50	

ALC3240



+5VS → +5VDDA_CODEC



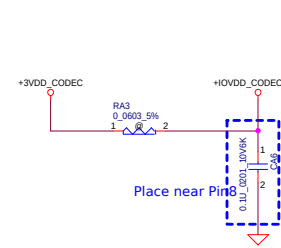
Each PlaTorm Power Net Support:List

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
AMD Carrizo	V	V	V	V	V
AMD Carrizo-L	V	V	V	V	V
Intel Broadwell	V	V	V	V	V
Intel Braswell	V	V	V	V	V
Intel Skylake	V	V	V	V	V
Intel Bay trail-M	V	V	V	V	V

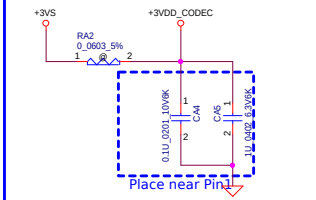
Each PlaTorm HDA Link Voltage Support (Pin 8)

	3.3V	1.5V
AMD Carrizo		V
AMD Carrizo-L		V
Intel Broadwell	V	V
Intel Braswell		V
Intel Skylake	V	V
Intel Bay trail-M		V

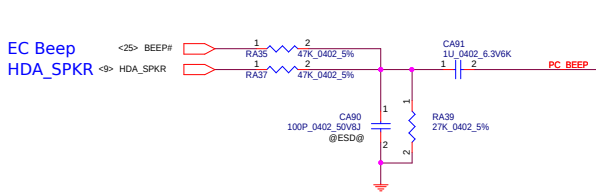
+3VDD_CODEC → +IOVDD_CODEC



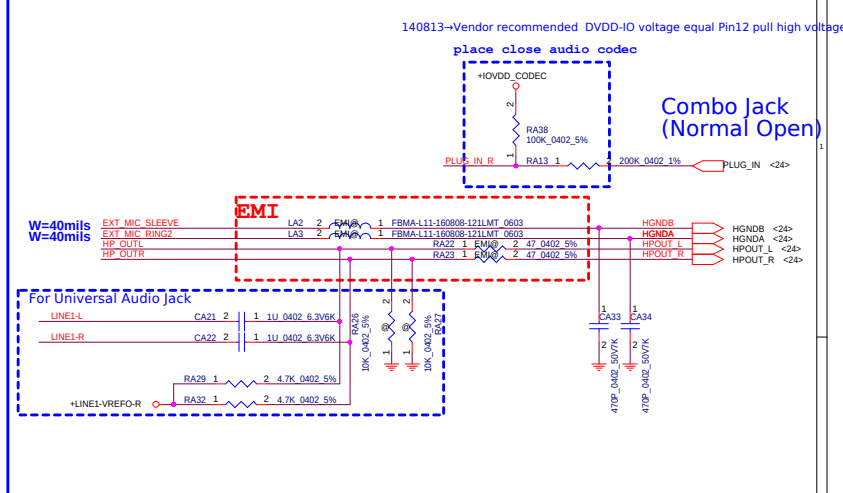
+3VS → +3VDD_CODEC



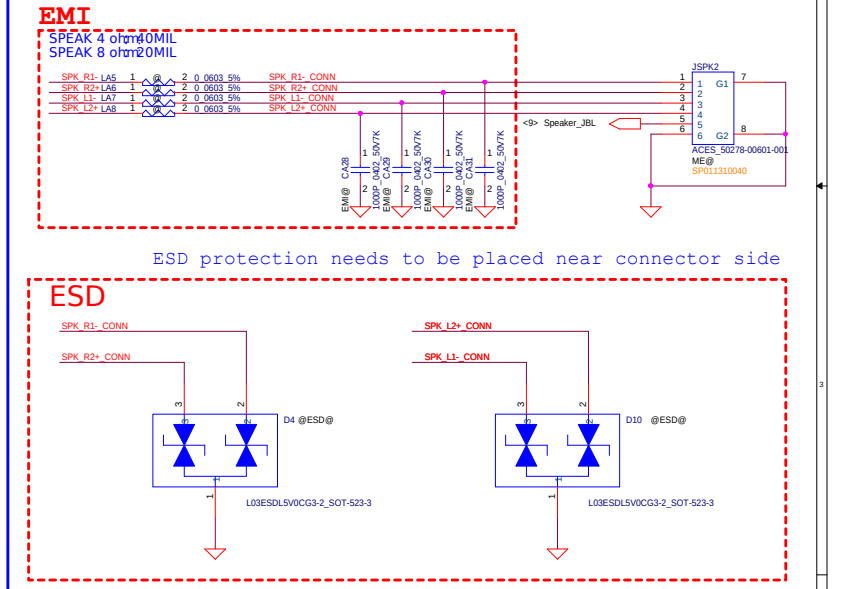
PC Beep



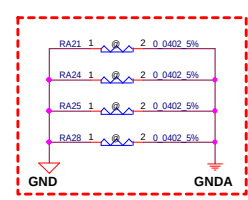
Input

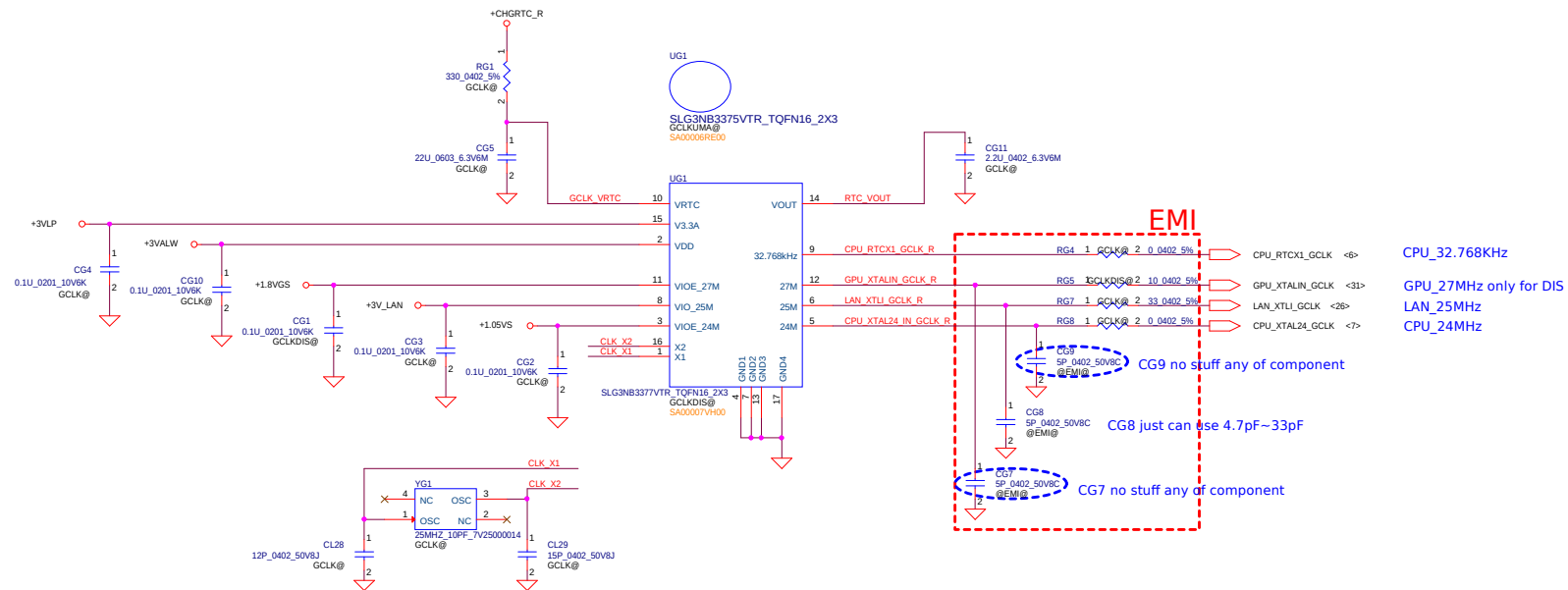


Output

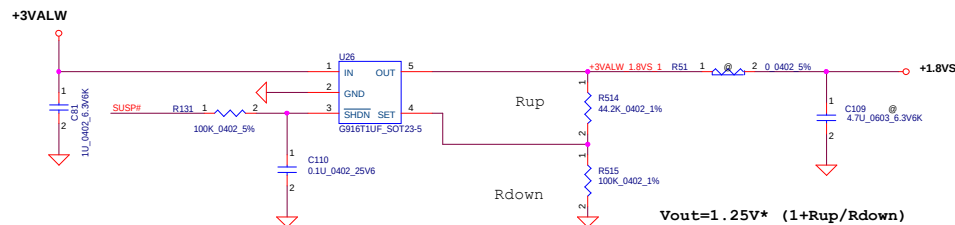
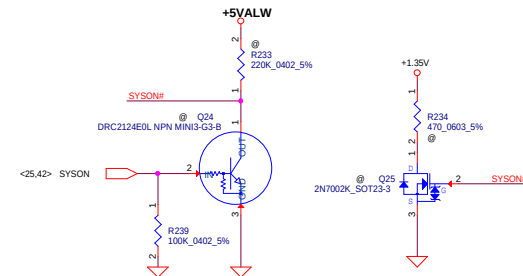
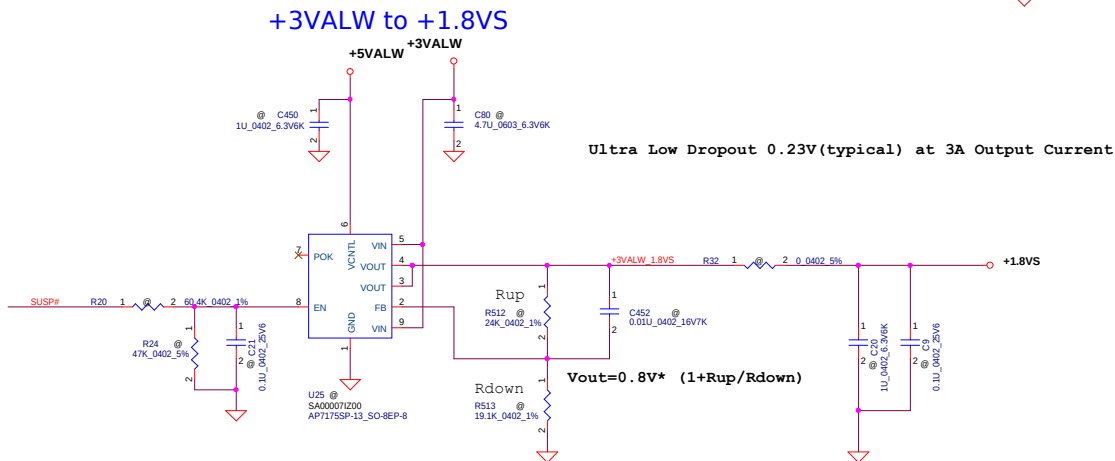
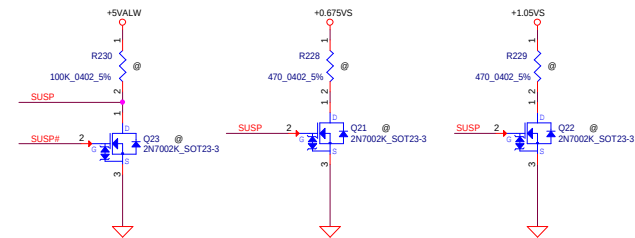
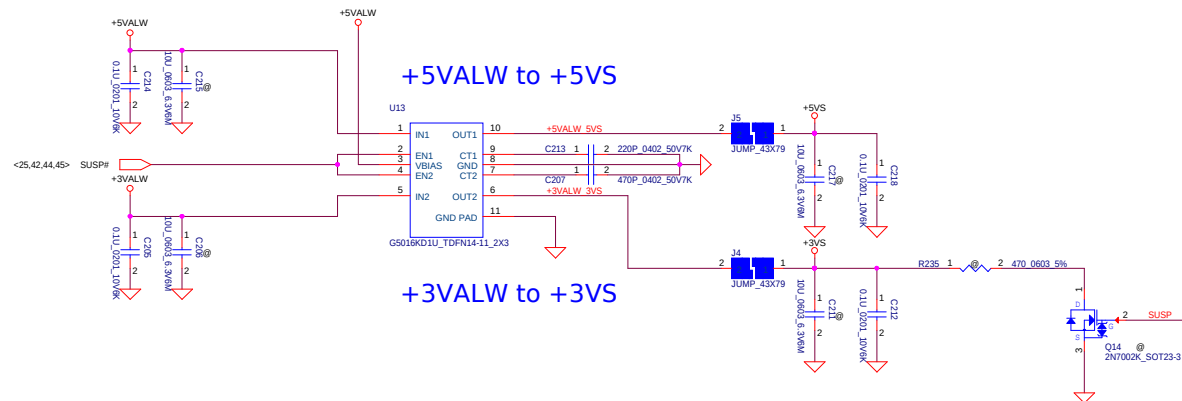


EMI

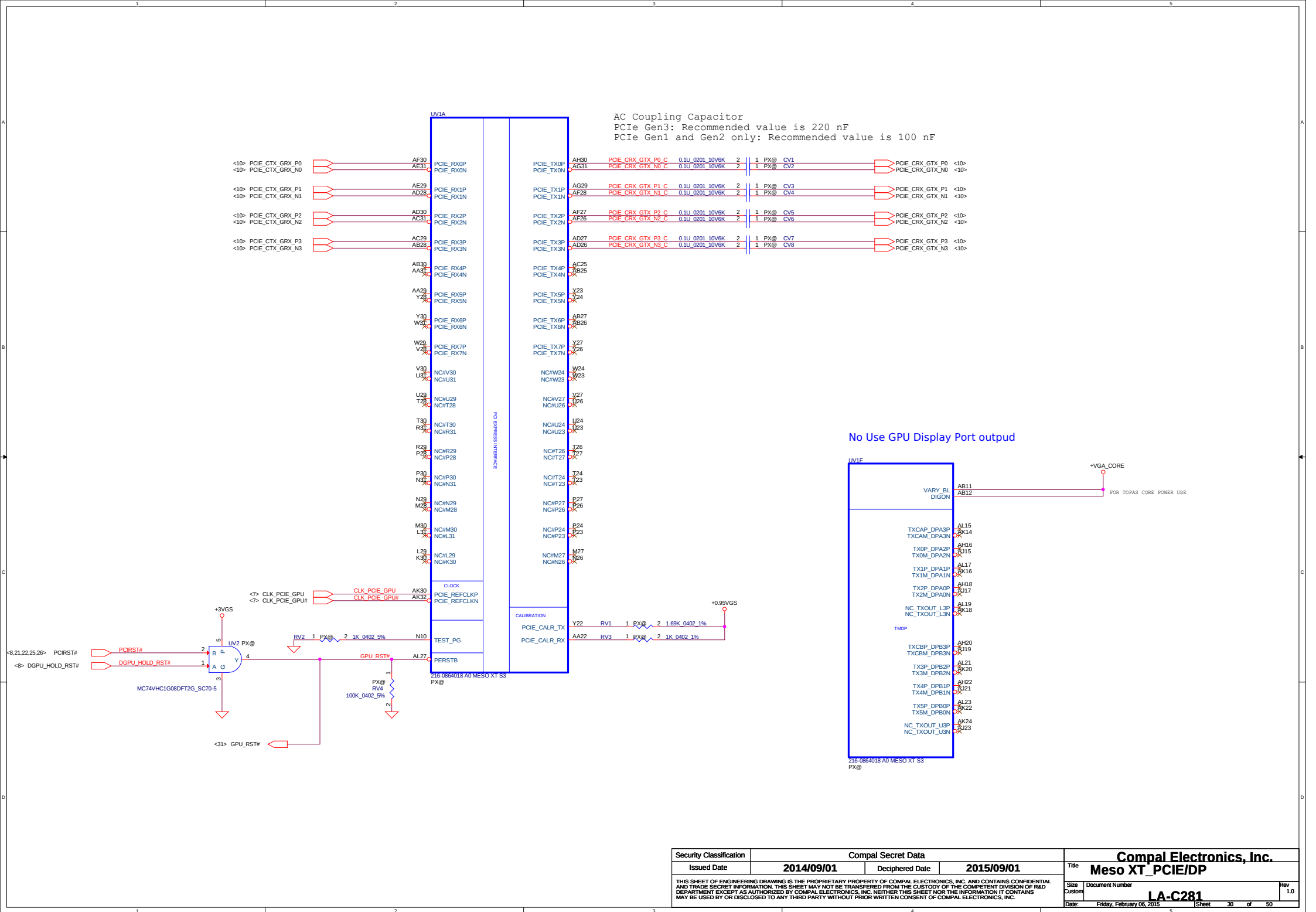




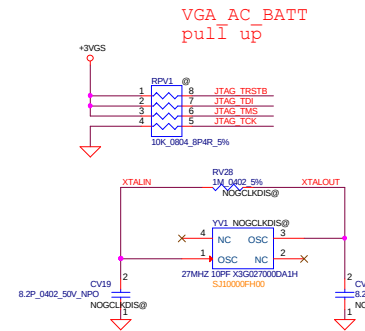
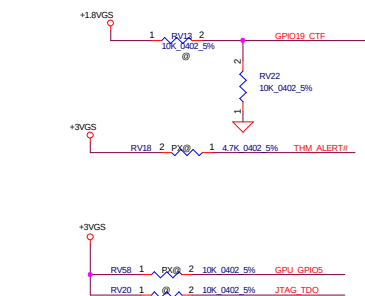
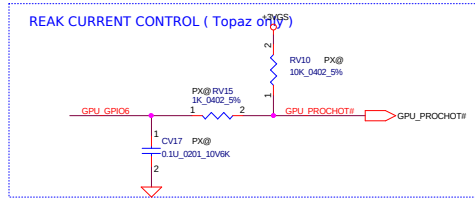
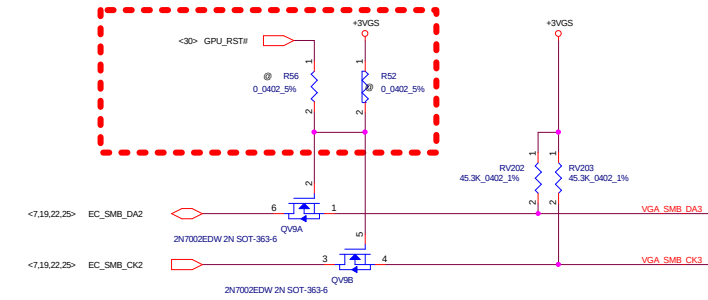
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/09/01	Deciphered Date	2015/09/01	Title	GCLK
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				Rev	1.0



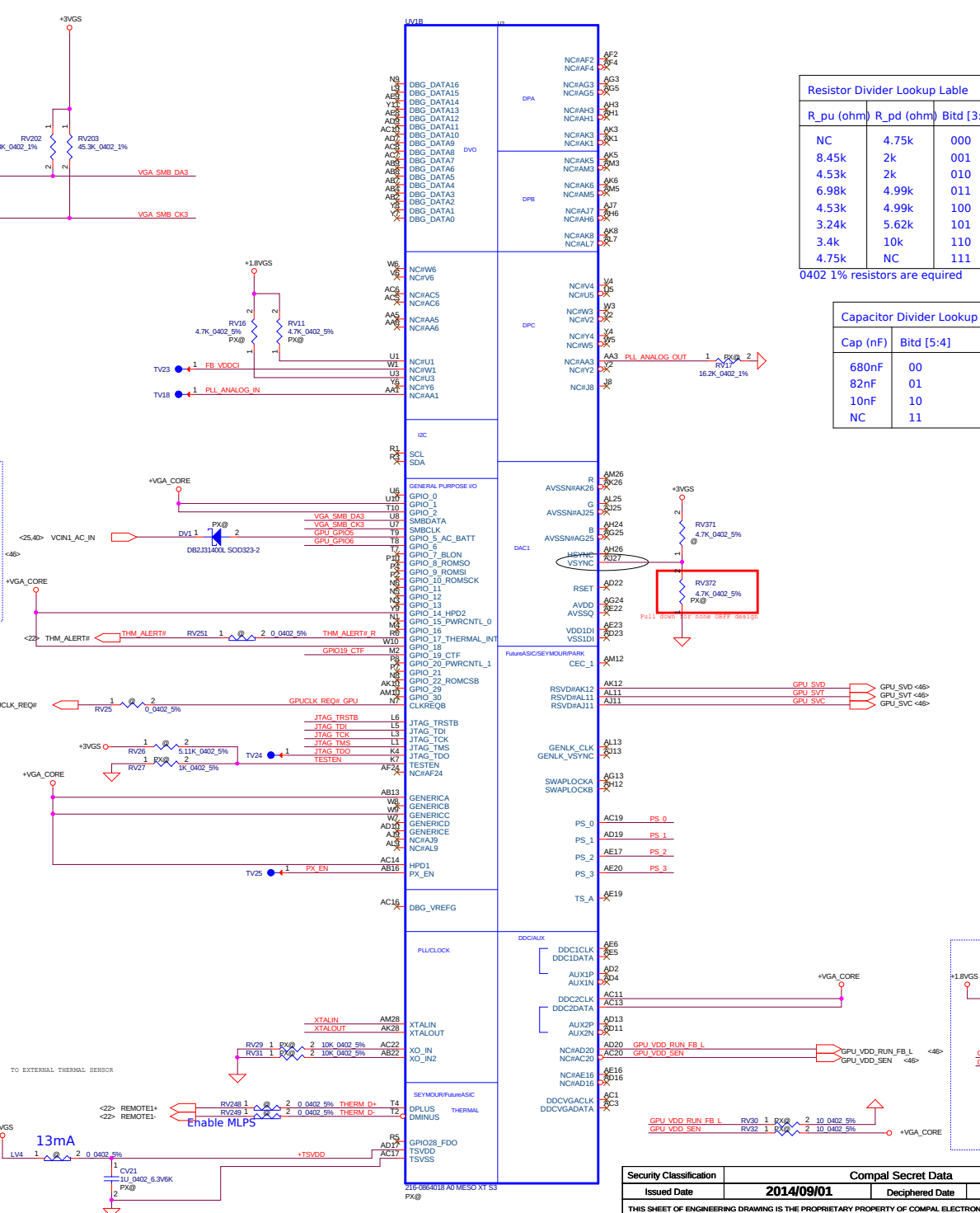
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/09/01	Deciphered Date	2015/09/01	Title		
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Size	C	Document Number	LA-C281	Rev	1.0	
Date:	Friday, February 06, 2015	Sheet	29	of	50	



for GPU tempture issue



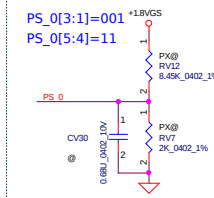
<2B> GPU_XTALIN_GCLK <GPU_XTALIN_GCLK RV253 2 0.0402_5% XTALIN



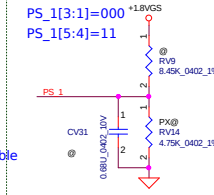
Resistor Divider Lookup Table		
R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are required

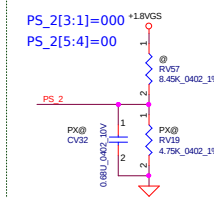
Capacitor Divider Lookup Table	
Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11



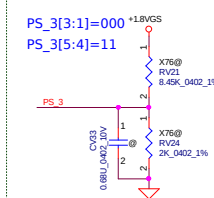
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]



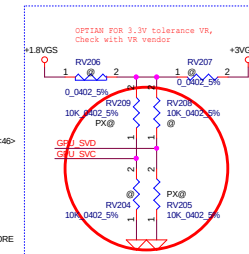
Strap Name :
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWIN
PS_1[5] STRAP_TX_DEEMPH_EN



Strap Name :
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A



Strap Name :
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]



+1.35VS to +1.35VGS (6.234A)

+1.05VS to +0.95VGS

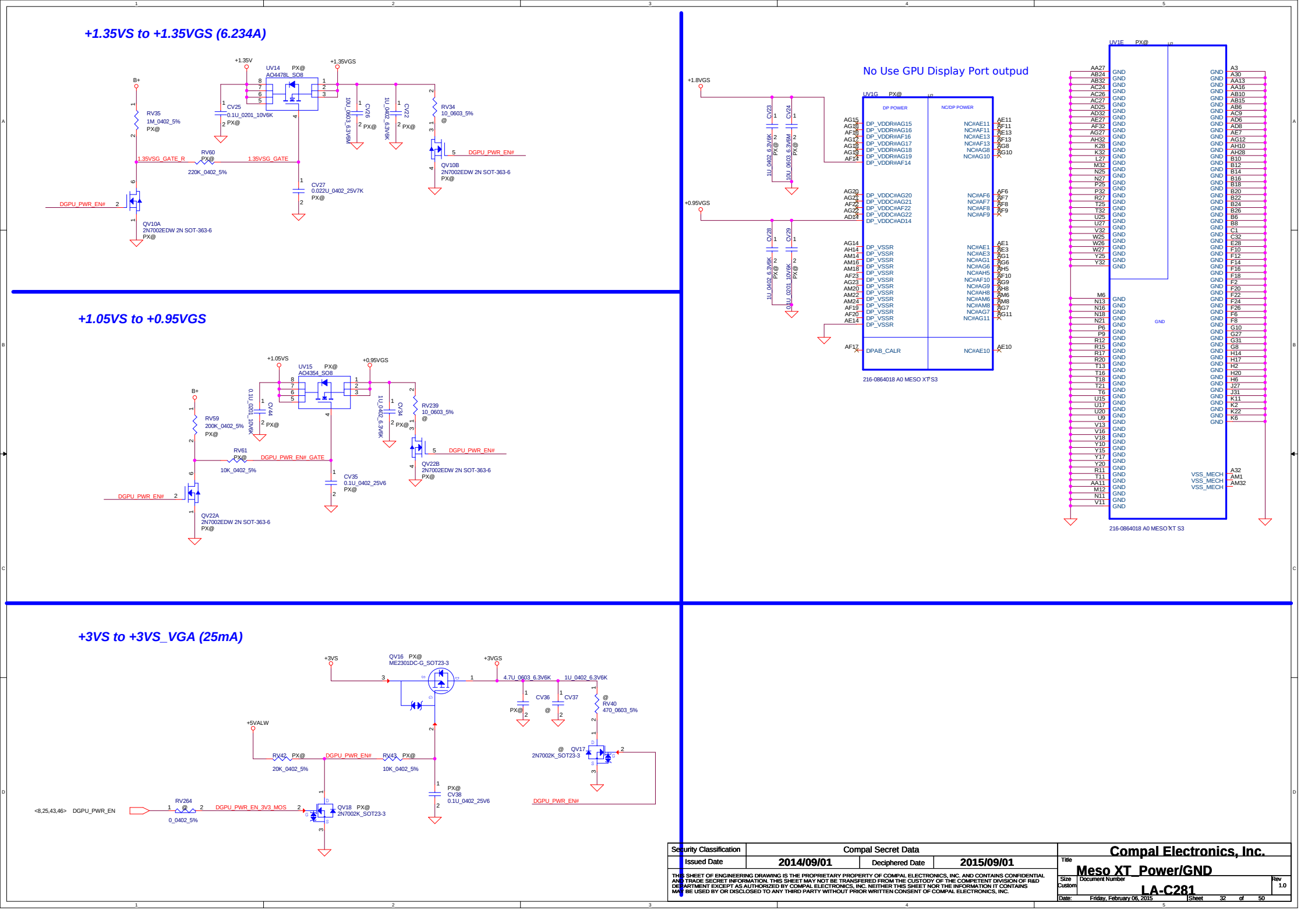
+3VS to +3VGS_VGA (25mA)

No Use GPU Display Port output

216-0864018 A0 MESO XT'S3

216-0864018 A0 MESO XT'S3

Security Classification	Compal Secret Data		Title	
Issued Date	2014/09/01	Deciphered Date	2015/09/01	Meso XT Power/GND
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Size	Custom	Document Number	LA-C281	Rev 1.0
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+1.35VS to +1.35VGS (6.234A)

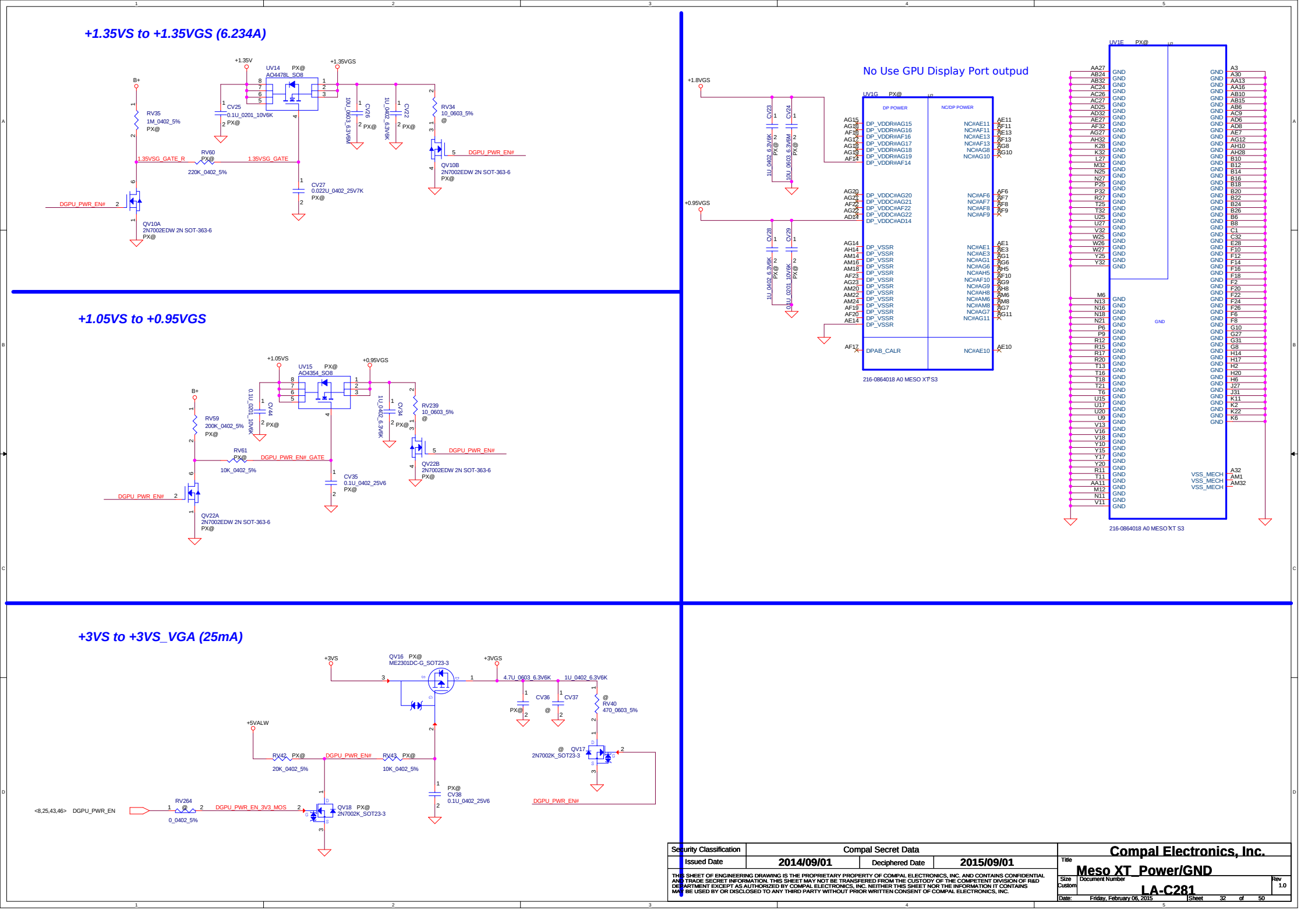
+1.8VGS to +0.95VGS

+1.05VS to +0.95VGS

+3VS to +3VS_VGA (25mA)

216-0864018 A0 MESO XT'S3

AA27	GND	A3	GND
AB24	GND	AA13	GND
AC24	GND	AA16	GND
AC26	GND	AB10	GND
AC27	GND	AB15	GND
AD25	GND	AB6	GND
AD32	GND	AC9	GND
AE27	GND	AD8	GND
AF32	GND	AE7	GND
AG27	GND	AG12	GND
AH32	GND	AH10	GND
K28	GND	B10	GND
K32	GND	B12	GND
L27	GND	B14	GND
M32	GND	B16	GND
N25	GND	B18	GND
N27	GND	B20	GND
P25	GND	B22	GND
P32	GND	B24	GND
R27	GND	B26	GND
T25	GND	B6	GND
T32	GND	B8	GND
U25	GND	B12	GND
U27	GND	B14	GND
V32	GND	B16	GND
W25	GND	B18	GND
W26	GND	B20	GND
W27	GND	B22	GND
Y25	GND	B24	GND
Y32	GND	B26	GND
		B6	GND
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		B16	GND
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		B22	GND



+1.35VS to +1.35VGS (6.234A)

+1.05VS to +0.95VGS

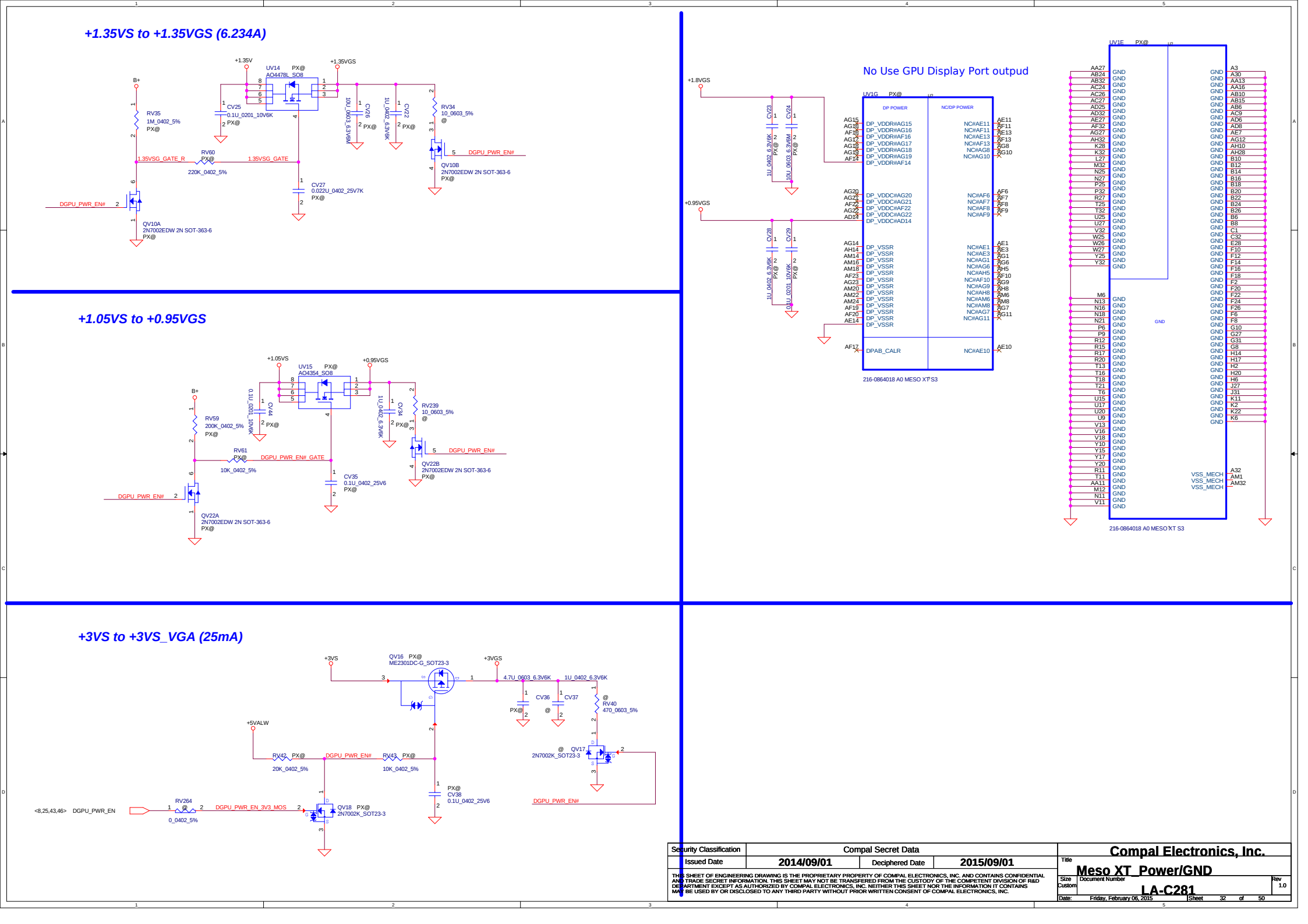
+3VS to +3VS_VGA (25mA)

No Use GPU Display Port output

216-0864018 A0 MESO XT S3

216-0864018 A0 MESO XT S3

Security Classification	Compal Secret Data		Title	
Issued Date	2014/09/01	Deciphered Date	2015/09/01	Meso XT Power/GND
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Size	Custom	Document Number	LA-C281	Rev 1.0
Date	Friday, February 06, 2015	Sheet	32	of 50



+1.35VS to +1.35VGS (6.234A)

+1.05VS to +0.95VGS

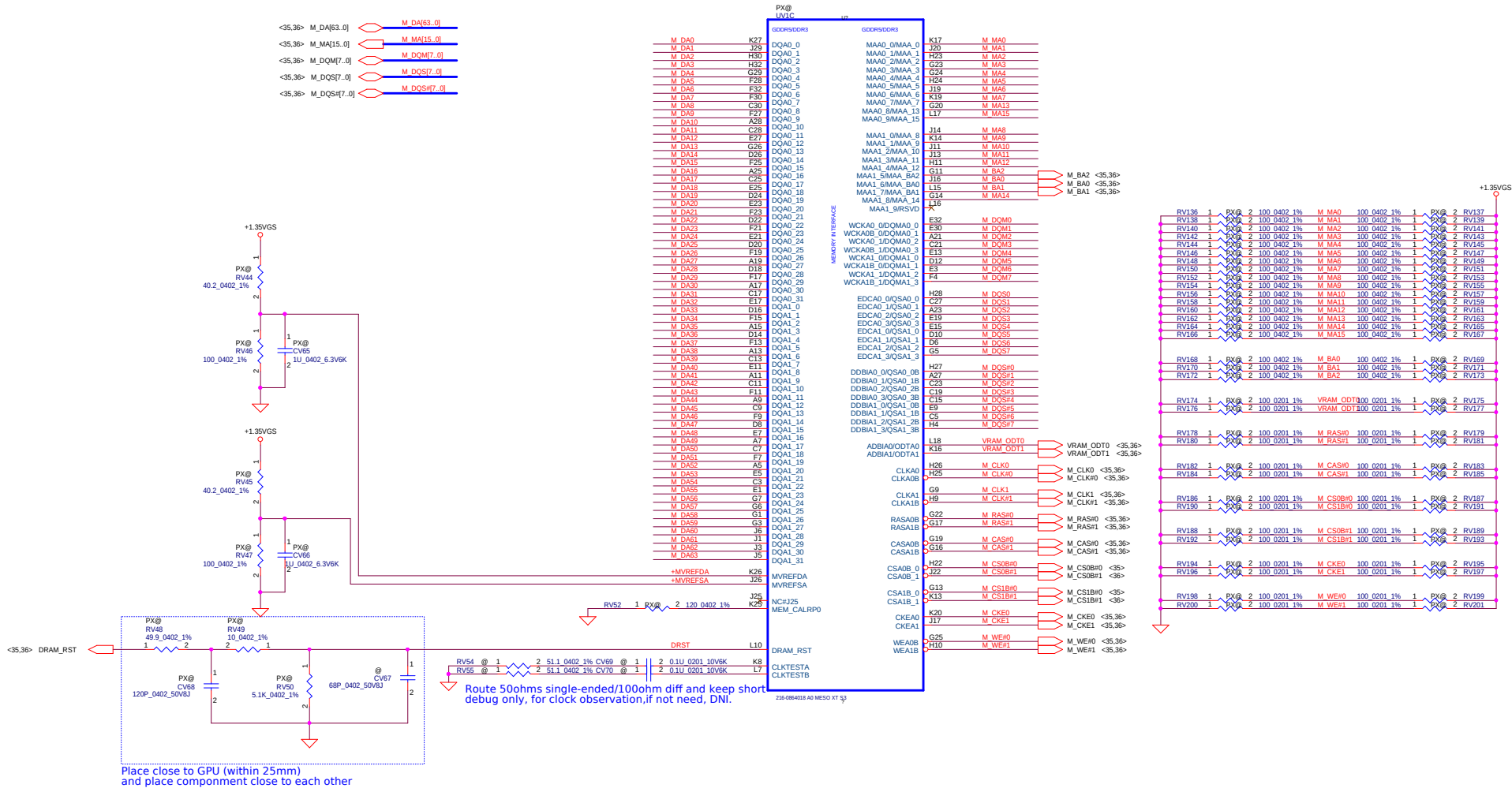
+3VS to +3VGS_VGA (25mA)

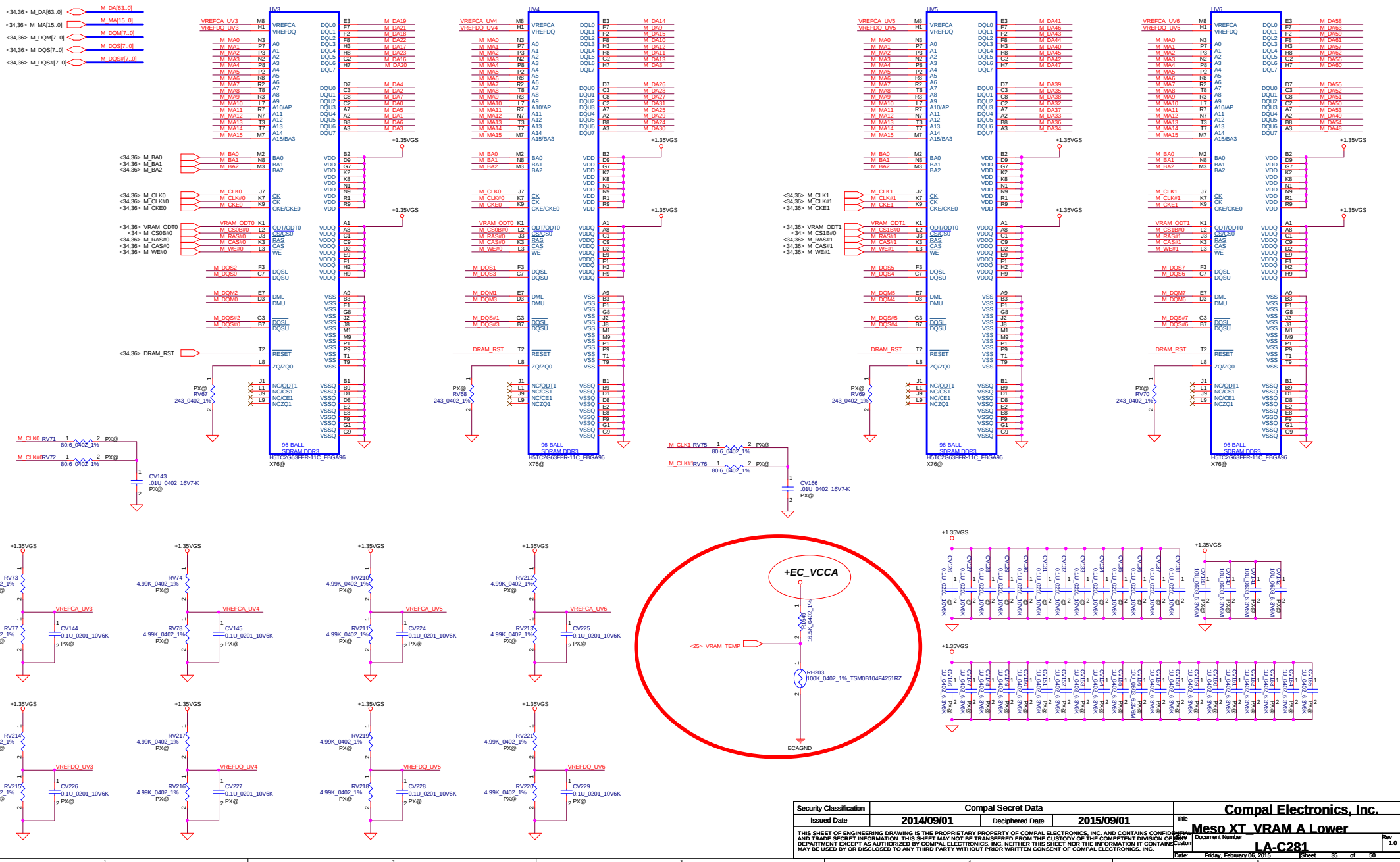
No Use GPU Display Port output

216-0864018 A0 MESO XT'S3

216-0864018 A0 MESO XT'S3

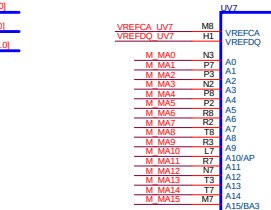
Security Classification	Compal Secret Data		Title	
Issued Date	2014/09/01	Deciphered Date	2015/09/01	Meso XT Power/GND
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Size	Custom	Document Number	LA-C281	Rev 1.0
Date	Friday, February 06, 2015	Sheet	32	of 50





Security Classification		Compal Secret Data		Title	
Issued Date		2014/09/01	Deciphered Date	2015/09/01	Meso XT VRAM A Lower
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Date		Friday, February 06, 2015	Sheet	35	of 90

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<34.35> M_DQM[7..0] M_DQM[7..0]
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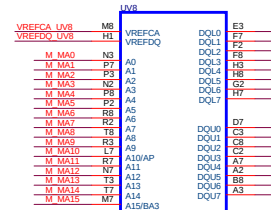
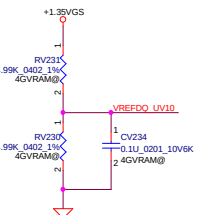
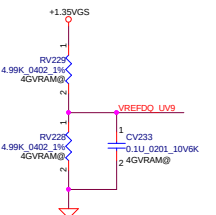
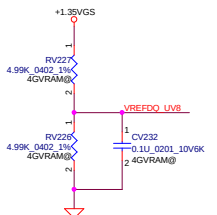
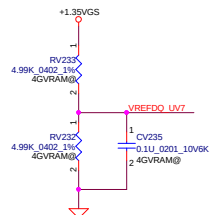
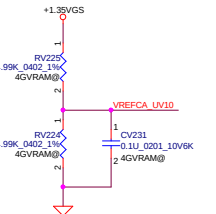
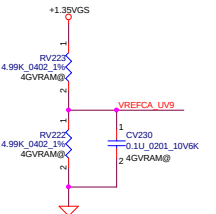
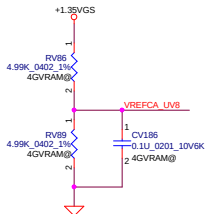
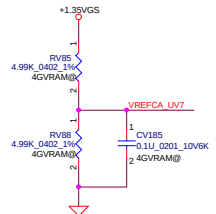
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RESET RESET

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243_0402_1% 243_0402_1%

M_CLK0 RV83 1 2 PX@
80.6_0402_1% 80.6_0402_1%

M_CLK[0] RV84 1 2 PX@
80.6_0402_1% 80.6_0402_1%

CV183 01U_0402_16V7-K
PX@ PX@



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M_DQS2 M_DQS2
M_DQS3 M_DQS3

M_DQM2 M_DQM2
M_DQM3 M_DQM3

M_DQS[0] M_DQS[0]
M_DQS[0] M_DQS[0]

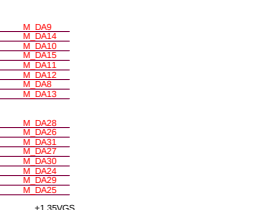
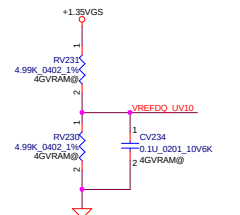
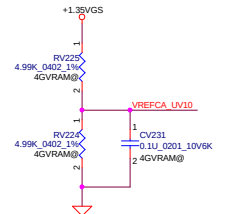
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RESET RESET

4GVRAM@ 4GVRAM@
243_0402_1% 243_0402_1%

M_CLK1 RV87 1 2 PX@
80.6_0402_1% 80.6_0402_1%

M_CLK[1] RV90 1 2 PX@
80.6_0402_1% 80.6_0402_1%

CV187 01U_0402_16V7-K
PX@ PX@



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<34.35> M_CAS[1] M_CAS[1]
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M_DQS6 M_DQS6

M_DQM5 M_DQM5
M_DQM6 M_DQM6

M_DQS[1] M_DQS[1]
M_DQS[1] M_DQS[1]

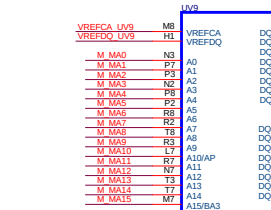
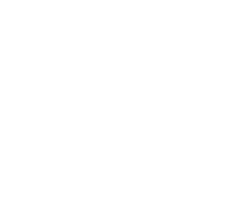
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RESET RESET

4GVRAM@ 4GVRAM@
243_0402_1% 243_0402_1%

M_CLK1 RV87 1 2 PX@
80.6_0402_1% 80.6_0402_1%

M_CLK[1] RV90 1 2 PX@
80.6_0402_1% 80.6_0402_1%

CV187 01U_0402_16V7-K
PX@ PX@



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<34.35> M_CAS[1] M_CAS[1]
<34.35> M_WE[1] M_WE[1]

M_DQS5 M_DQS5
M_DQS6 M_DQS6

M_DQM5 M_DQM5
M_DQM6 M_DQM6

M_DQS[1] M_DQS[1]
M_DQS[1] M_DQS[1]

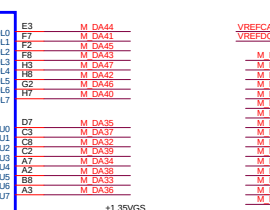
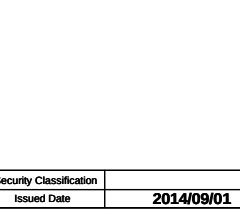
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4GVRAM@ 4GVRAM@
243_0402_1% 243_0402_1%

M_CLK1 RV87 1 2 PX@
80.6_0402_1% 80.6_0402_1%

M_CLK[1] RV90 1 2 PX@
80.6_0402_1% 80.6_0402_1%

CV187 01U_0402_16V7-K
PX@ PX@



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M_DQS5 M_DQS5
M_DQS6 M_DQS6

M_DQM5 M_DQM5
M_DQM6 M_DQM6

M_DQS[1] M_DQS[1]
M_DQS[1] M_DQS[1]

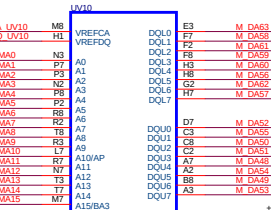
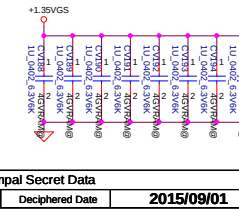
<34.35> DRAM_RST DRAM_RST
RESET RESET

4GVRAM@ 4GVRAM@
243_0402_1% 243_0402_1%

M_CLK1 RV87 1 2 PX@
80.6_0402_1% 80.6_0402_1%

M_CLK[1] RV90 1 2 PX@
80.6_0402_1% 80.6_0402_1%

CV187 01U_0402_16V7-K
PX@ PX@



<34.35> M_BA0 M_BA0
<34.35> M_BA1 M_BA1
<34.35> M_BA2 M_BA2

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<34.35> M_CAS[1] M_CAS[1]
<34.35> M_CAS[1] M_CAS[1]
<34.35> M_WE[1] M_WE[1]

M_DQS5 M_DQS5
M_DQS6 M_DQS6

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M_DQM6 M_DQM6

M_DQS[1] M_DQS[1]
M_DQS[1] M_DQS[1]

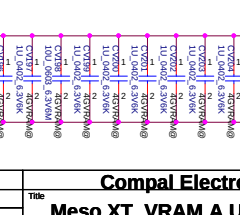
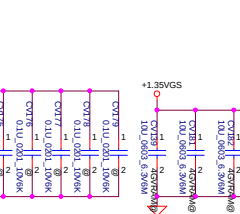
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RESET RESET

4GVRAM@ 4GVRAM@
243_0402_1% 243_0402_1%

M_CLK1 RV87 1 2 PX@
80.6_0402_1% 80.6_0402_1%

M_CLK[1] RV90 1 2 PX@
80.6_0402_1% 80.6_0402_1%

CV187 01U_0402_16V7-K
PX@ PX@



Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2014/09/01	Deciphered Date	2015/09/01	Title	
				Meso XT VRAM A Upper	
				Documents Number	
				LA-C281	
				Rev	
				1.0	
				Date	
				Friday, February 06, 2015	
				Sheet	
				36 of 90	

Meso XT_VRAM_STRAP

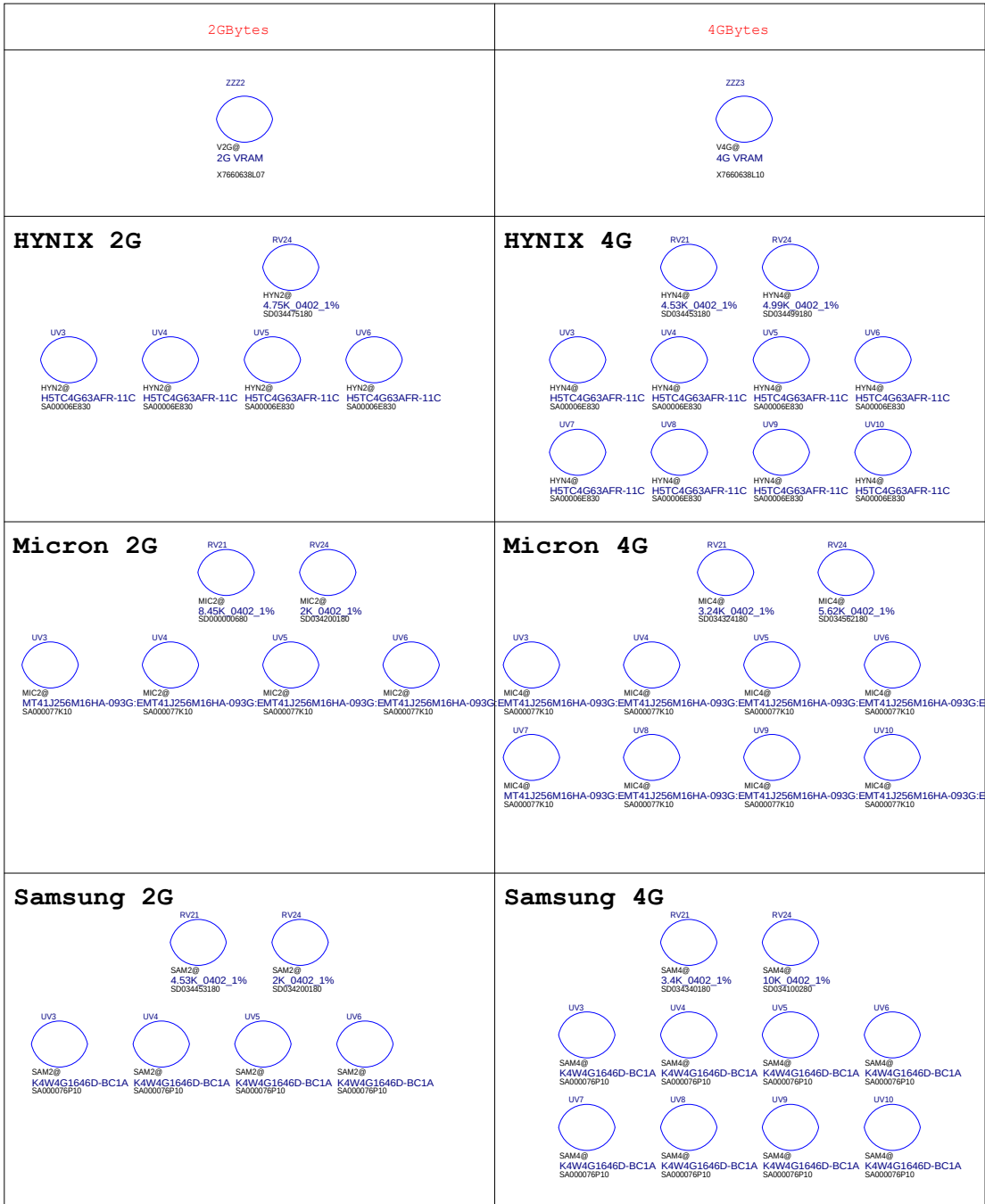
X76@

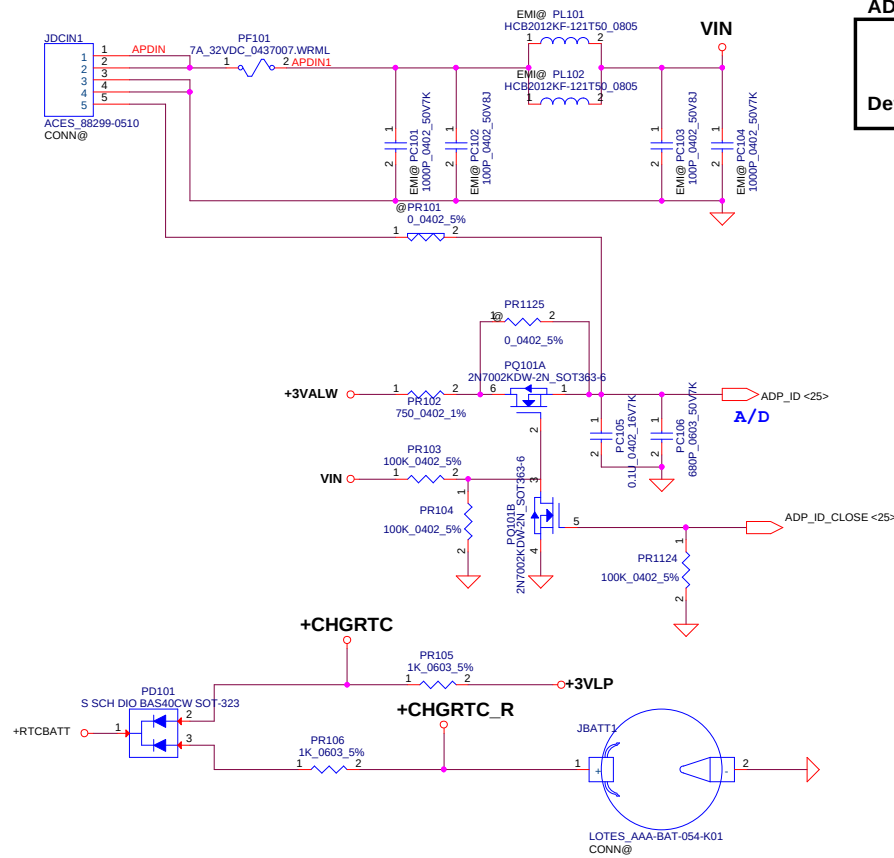
X76@

	Vendor	ID	PS_3[3]	PS_3[2]	PS_3[1]	R_pu	R_pd
						RV21	RV24
2GBytes	HYN2@ Hynix 2G SA00006E830 256Mx16 H5TC4G63AFR-11C	0	0	0	0	NC	4.75K
2GBytes	MIC2@ Micron 2G SA000077K10 256Mx16 MT41J256M16HA-093G:E	1	0	0	1	8.45K	2K
2GBytes	SAM2@ Samsung 2G SA000076P10 256Mx16 K4W4G1646D-BC1A	2	0	1	0	4.53K	2K
		3	0	1	1	6.98K	4.99K
4GBytes	HYN4@ Hynix 4G SA00006E830 256Mx16 H5TC4G63AFR-11C	4	1	0	0	4.53K	4.99K
4GBytes	MIC4@ Micron 4G SA000077K10 256Mx16 MT41J256M16HA-093G:E	5	1	0	1	3.24K	5.62K
4GBytes	SAM4@ Samsung 4G SA000076P10 256Mx16 K4W4G1646D-BC1A	6	1	1	0	3.4K	10K
		7	1	1	1	4.75K	NC

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

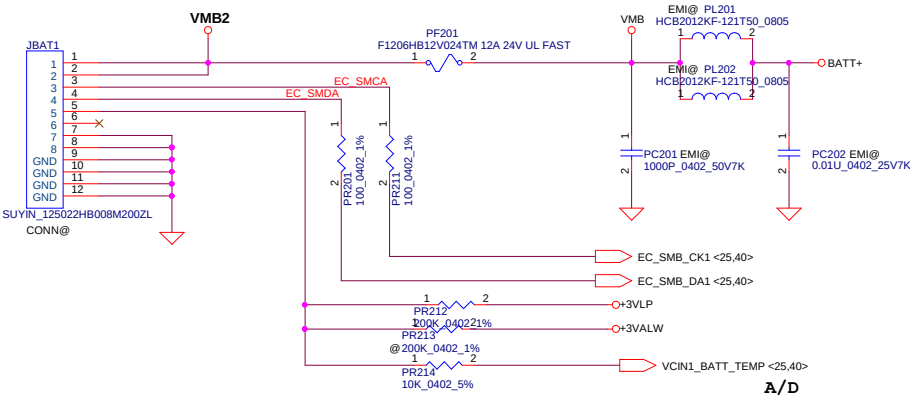




ADP_ID		
AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

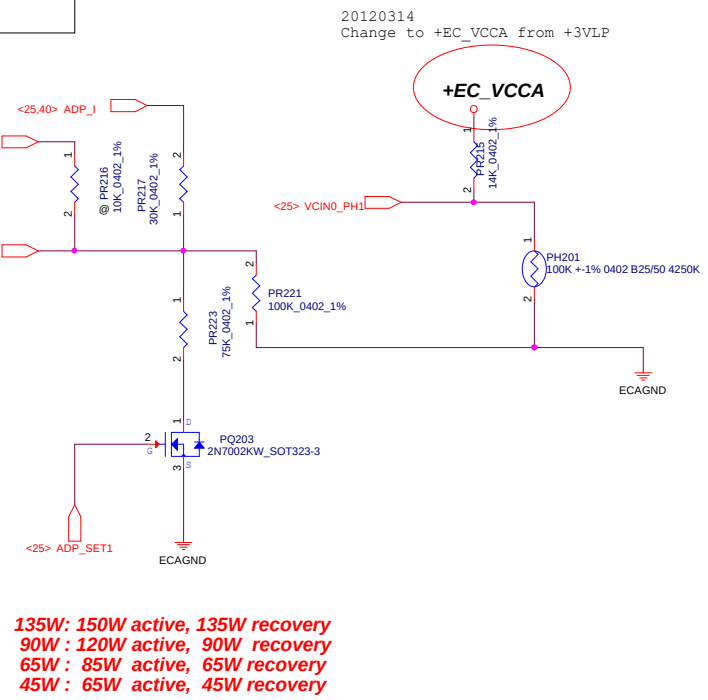
RTC Battery

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	PWR DCIN / RTC Battery
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				Date: Friday, February 06, 2015	Rev 1.0
				Sheet 38 of 50	

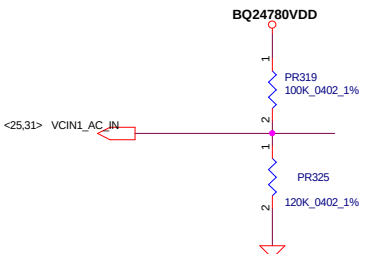
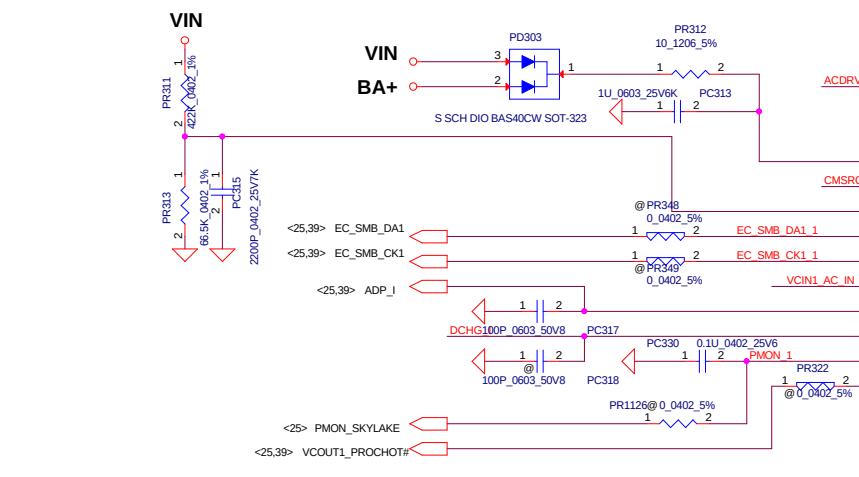
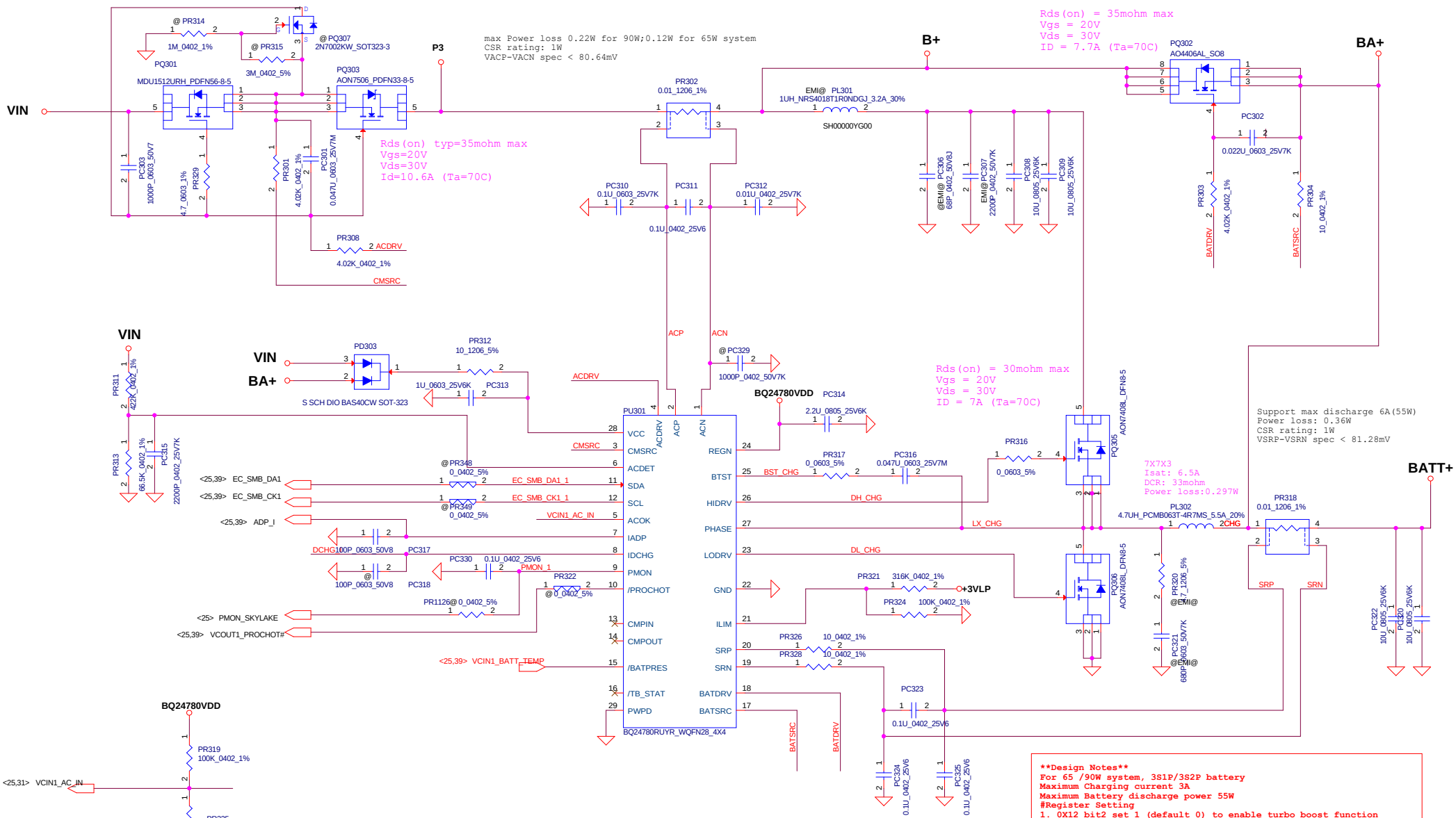


PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

	ADP_SET1	ADP_SET2
45W adapter	0	0
65W adapter	1	0
90W adapter	0	1
135W adapter	1	1



135W: 150W active, 135W recovery
90W : 120W active, 90W recovery
65W : 85W active, 65W recovery
45W : 65W active, 45W recovery



Vin Detector			
	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rs
ILIM = 3.3*100/(316+100)/20/0.01
= 3.966 A

Rds(on) = 35mohm max
Vgs = 20V
Vds = 30V
ID = 7.7A (Ta=70C)

Rds(on) = 30mohm max
Vgs = 20V
Vds = 30V
ID = 7A (Ta=70C)

Support max discharge 6A(55W)
Power loss: 0.36W
CSR rating: 1W
VSRP-VSRN spec < 81.28mV

- **Design Notes****
- For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3A
Maximum Battery discharge power 55W
- #Register Setting**
- 0X12 bit2 set 1 (default 0) to enable turbo boost function
 - Disable turbo when AC only
- #Circuit Design**
- ILIM pull high voltage need base on 3/5V enable control
 - Use 7X7 choke and 3X3 H/L side MOSFET
- Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
- #Protect function**
- ACOVF : VCC voltage > 24V
 - Charger timeout : No communication within 175s(default)
 - ACOC : 3.33 X Input current DAC setting (default:Disable)
 - CHGOCF : based on charge current setting
 - BATOVF : 103-106%
 - BATLOWV : 2.6V
 - TSHUT : 155C
 - IFAUULT HI : 750mV (default:Disable)
 - IFAUULT LOW : 230mV (default)

Security Classification		Compal Secret Data		2015/11/05		Compal Electronics, Inc.	
Issued Date	2013/11/05	Deciphered Date	2015/11/05	Title	BQ24780	Rev	1.0
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				Date	Friday, February 06, 2015	Sheet	40 of 50

SY8208B_V2.mdd

Change 3V5V_EN to 3VALW_EN

ENLDO_3V5V



SY8208C_V2.mdd

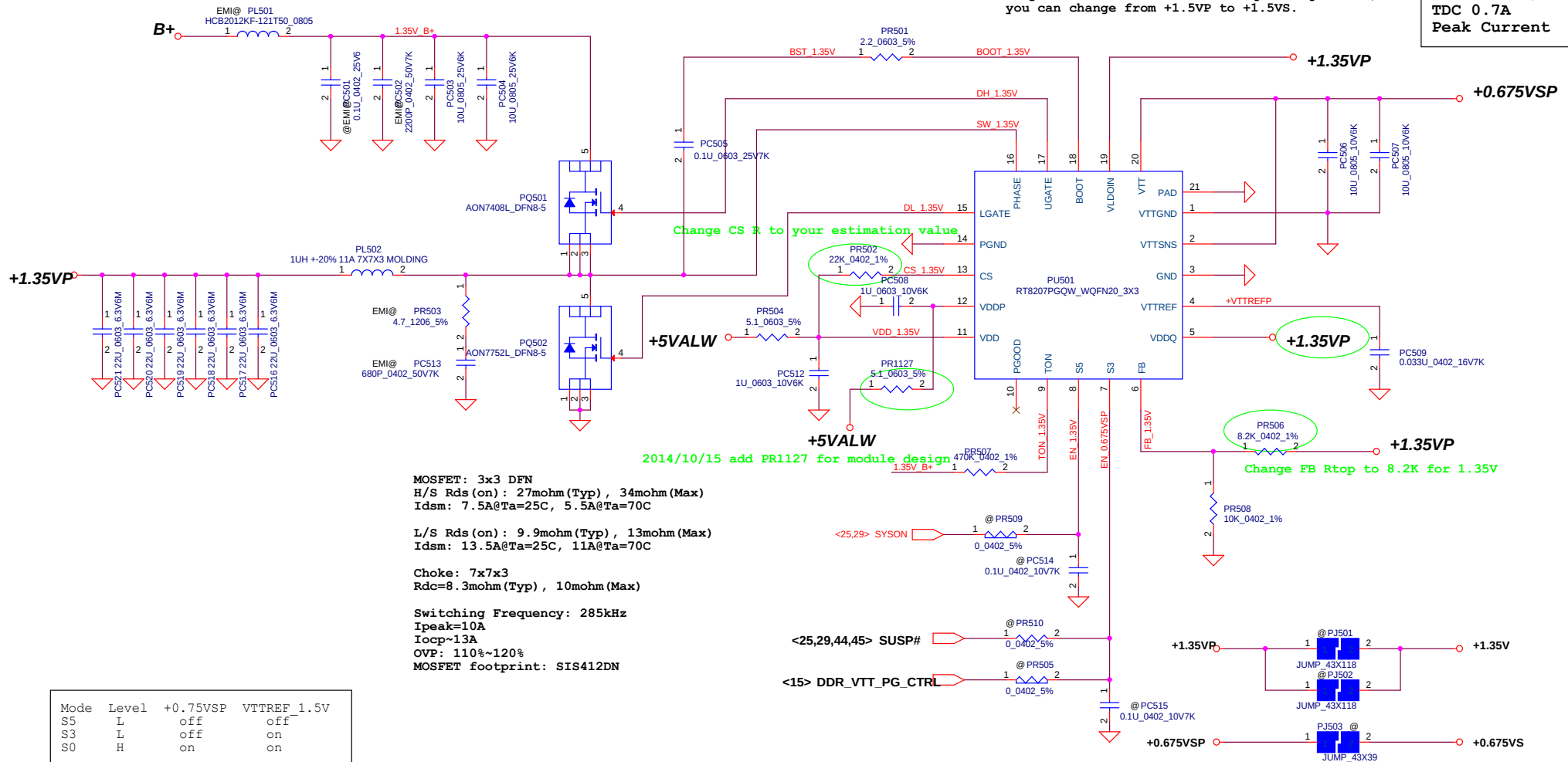
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Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title	
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RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A

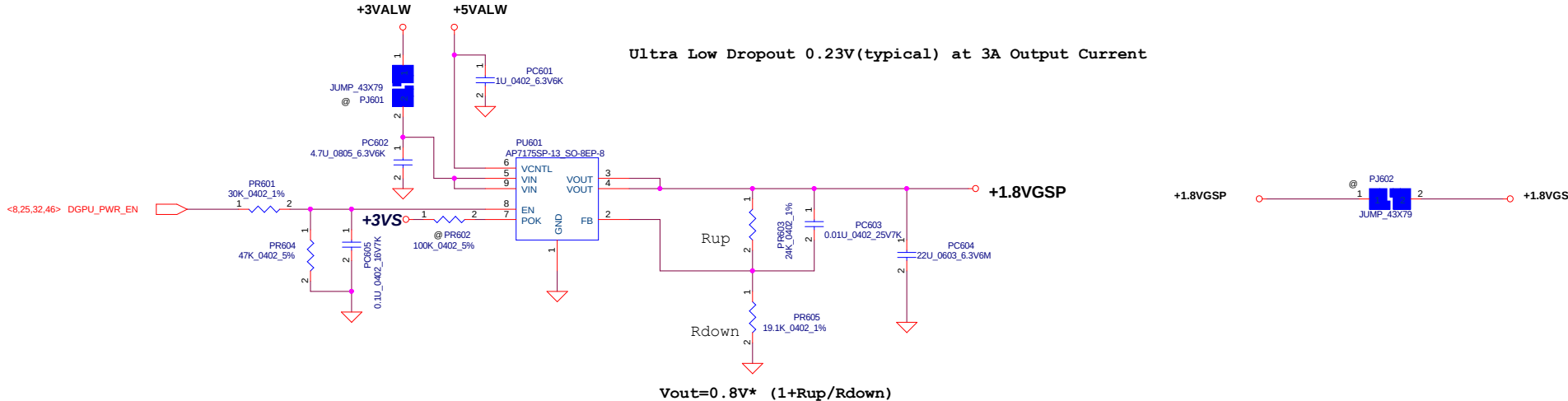


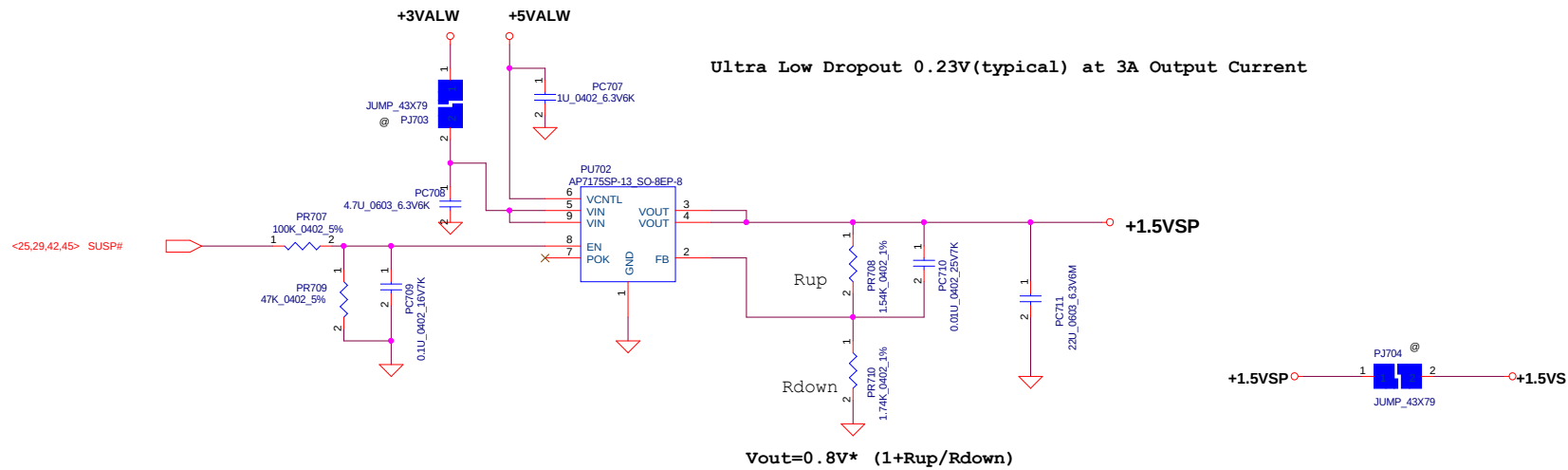
Mode	Level	+0.75VSP	VTTREF 1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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				Document Number	1.0
				Z BDW	
Date:	Friday, February 06, 2015	Sheet	42	of	50

Module model information
APL5930_V1.mdd

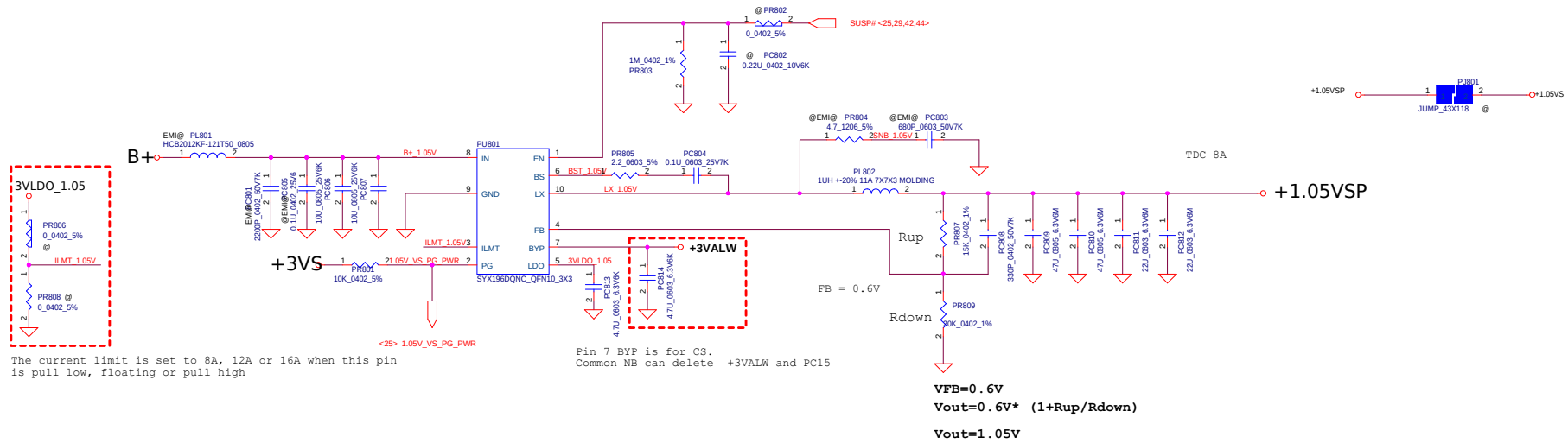




Module model information

SV8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



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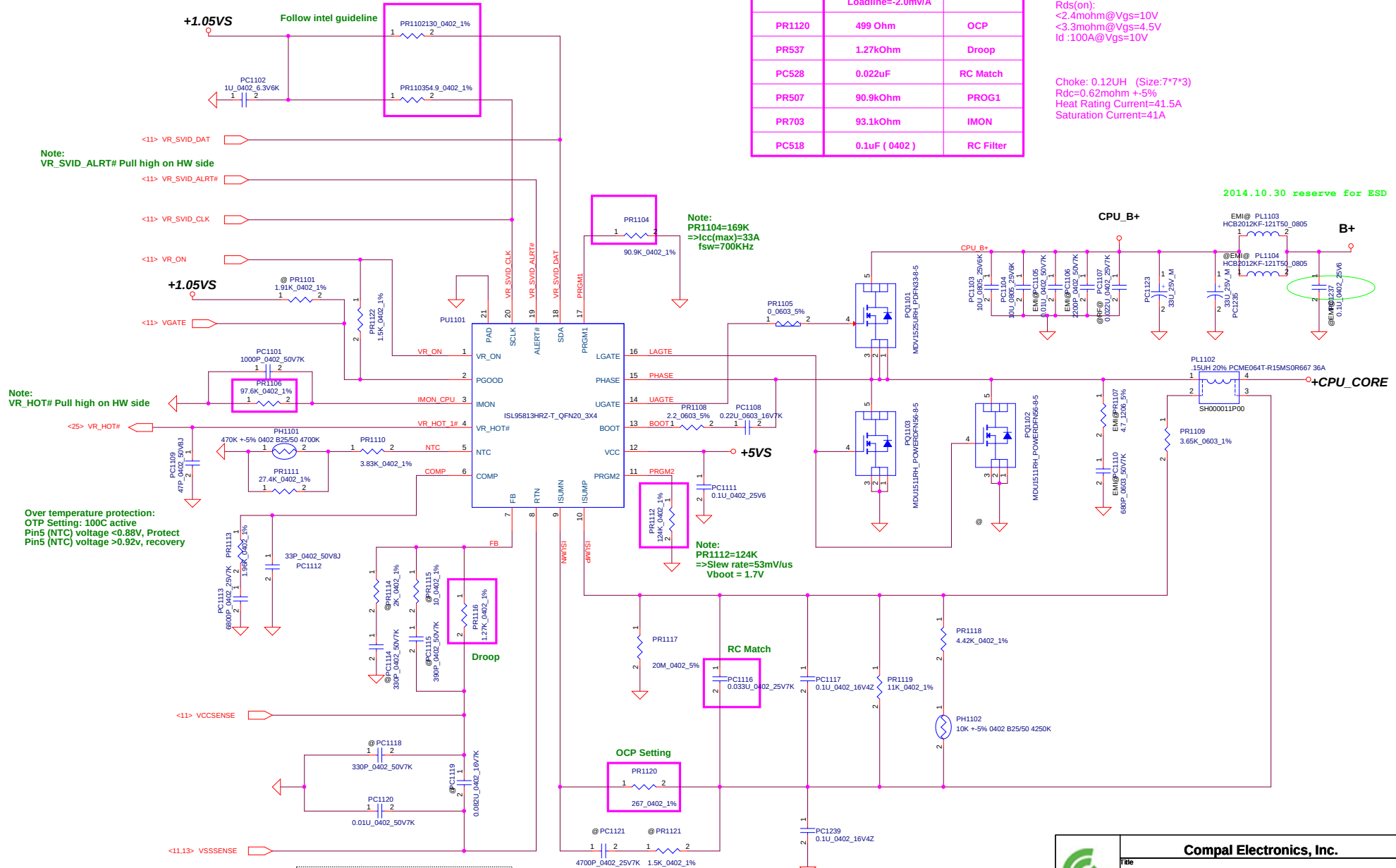
Module model information:
ISL95813 (for 15W & 28W CPU)

Base on BDW PDDG Rev_0_73		
Location	15W	Note
	TDC 14A	
	MAX 32A	
	OCp 39A	
	Loadline=-2.0mv/A	
PR1120	499 Ohm	OCp
PR537	1.27kOhm	Droop
PC528	0.022uF	RC Match
PR507	90.9kOhm	PROG1
PR703	93.1kOhm	IMON
PC518	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.12UH (Size:7*7*3)
Rdc=0.62mohm +-5%
Heat Rating Current=41.5A
Saturation Current=41A



Local sense put on HW site



Compal Electronics, Inc.

ISL95813 for BDW-Y&U(15W/28W) CPU

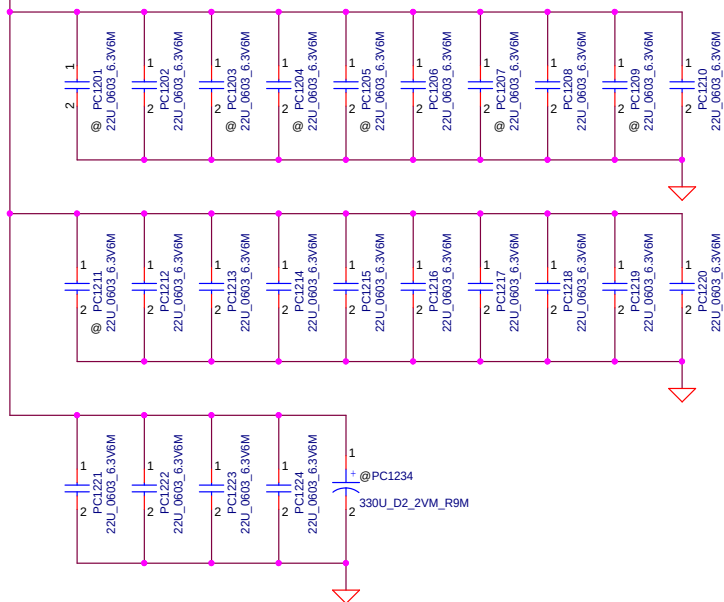
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Rev
1.0

+CPU_CORE

24 X 22u/0603



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			Z BDW		1.0
Date:		Friday, February 06, 2015		Sheet	48 of 50

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	reserve VGA_CORE RC delay	P46	add PC1236	2014.10.15	SIV
2	reserve 0.1uF for ESD	P41/P47	add PC1237,PC1238	2014.10.30	SIV
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Version change list (P.I.R. List)			Page 1 of 1 for HW		
Item	Reason for change	PG#	Modify List		Phase
1	Reserve clean CMOS circuit	P06	reserve R80,Q27	2014.10.28	SIV
2	HDMI Design	P18	add R1650,R1651,R1652,R1653,R1654,R1655,R1656,R1657,R1658,R1659,R1660,R1661	2014.10.28	SIV
3	USB2.0 design for EMI request	P24	add R1676 and R1677	2014.10.28	SIV
4	Change commom chock symbol for EMI request	P24	change L12~L18	2014.10.28	SIV
5	Add FAN_ID for EC request	P25	add R516 and R517	2014.10.29	SIV
6	Audio design for EMI request	P36	add CA28,CA29,CA30,CA31	2014.10.29	SIV
7	Audio design for EMI request	P36	change from RA19,RA20 to LA2,LA3	2014.10.29	SIV
8	Audio design for EMI request	P36	add LA1	2014.10.29	SIV
9	+1.35V design for EMI request	P15	add C320~C324	2014.10.29	SIV
10	modify +MEM_GFX power sequence	P32	change C901 from 0.01uF to 0.1uF	2014.10.30	SIV
11	LAN design change for wake on lan	P26	delete RL18, add J6,J7	2014.11.13	SIT
12	Change pcb foot print by DFX request	P20,P24	change J1O1,JODD1,JHDMI pcb footprint	2014.12.08	SIT
13	Change for VGA power sequence	P32	change CV35 value	2014.12.08	SIT
14	Change Audio PCBEEP SCH by verdor suggestion	P27	add RA35,RA37,CA90,CA91,RA39 / DELETE CA23,CA24,RA36,RA34,CA25	2014.12.15	SIT
15	Modify LED BOM setting	P27	modify LED1,LED2,LED3,LED4,LED5,LED6 BOM setting	2014.12.15	SIT
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