

01 -- COVER SHEET  
02 -- SYSTEM BLOCK DIAGRAM  
03 -- CLOCK MAP  
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05 -- POWER SEQUENCY DIAGRAM  
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08 -- RESET SIGNAL MAP  
09 -- Calpella (DMI,PEG,FDI)  
10 -- Calpella (CLK,MISC,JTAG)  
11 -- Calpella (DDR3)  
12 -- Calpella (POWER/GND)  
13 -- Calpella (GRAPHIC POWER)  
14 -- PCH (HDA,JTAG,SATA)  
15 -- PCH (PCI-E,SMBUS,CLK)  
16 -- PCH (DMI,FDI,GPIO,LVDS)  
17 -- PCH (PCI,USB,NVRAM,GPIO)  
18 -- PCH (POWER)  
19 -- DDR3(SO-DIMM 0&1)  
20 -- VGA (PCI-E/STRAP) 1/5

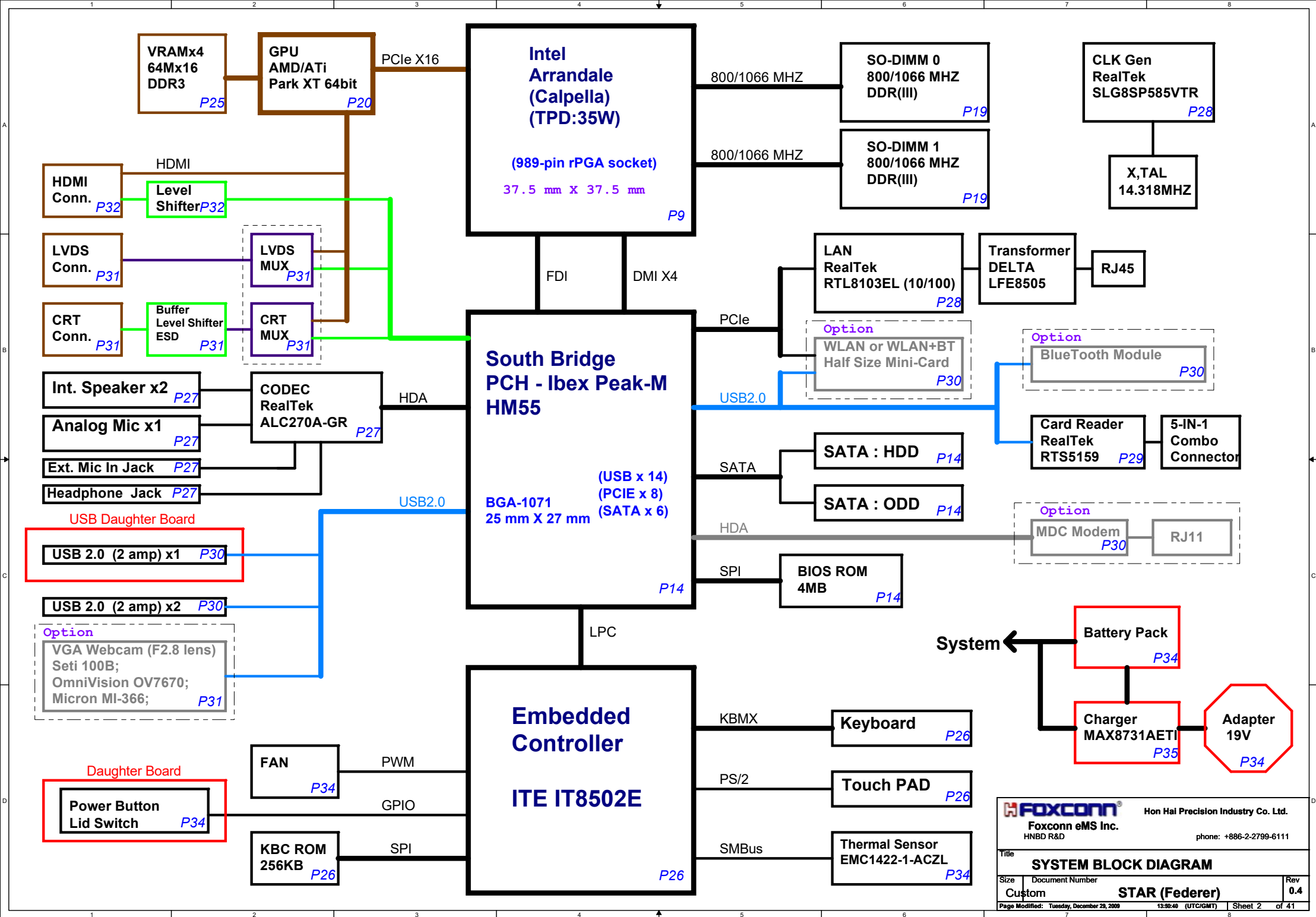
21 -- VGA\_S3 (IO) 2/5  
22 -- VGA\_S3 (DDR3) 3/5  
23 -- VGA\_S3 (DP) 4/5  
24 -- VGA\_S3 (POWER) 5/5  
25 -- VRAM (DDR3)  
26 -- EC+KBC (IT8502E)  
27 -- CODEC/JACK/SPEAKER/MIC  
28 -- LAN (RTL8103EL)/CLOCK GEN  
29 -- Card Reader  
30 -- WLAN/BT/MDC/USB/MOUNTING  
31 -- LVDS/CRT/Webcam  
32 -- HDMI  
33 -- DCIN/Battery/OCP/FAN  
34 -- PWR\_Charger MAX8731AETI  
35 -- 5V/3.3V SN0608098RHBT  
36 -- Vcore MAX17030  
37 -- 1.1V VTT/+V1.05RUN  
38 -- 1.5VDDR3+0.75V+V1.8RUN  
39 -- PWR\_Others power plane  
40 -- CPU VREG & Decoupling  
41 -- ATVDD/+VPCIE

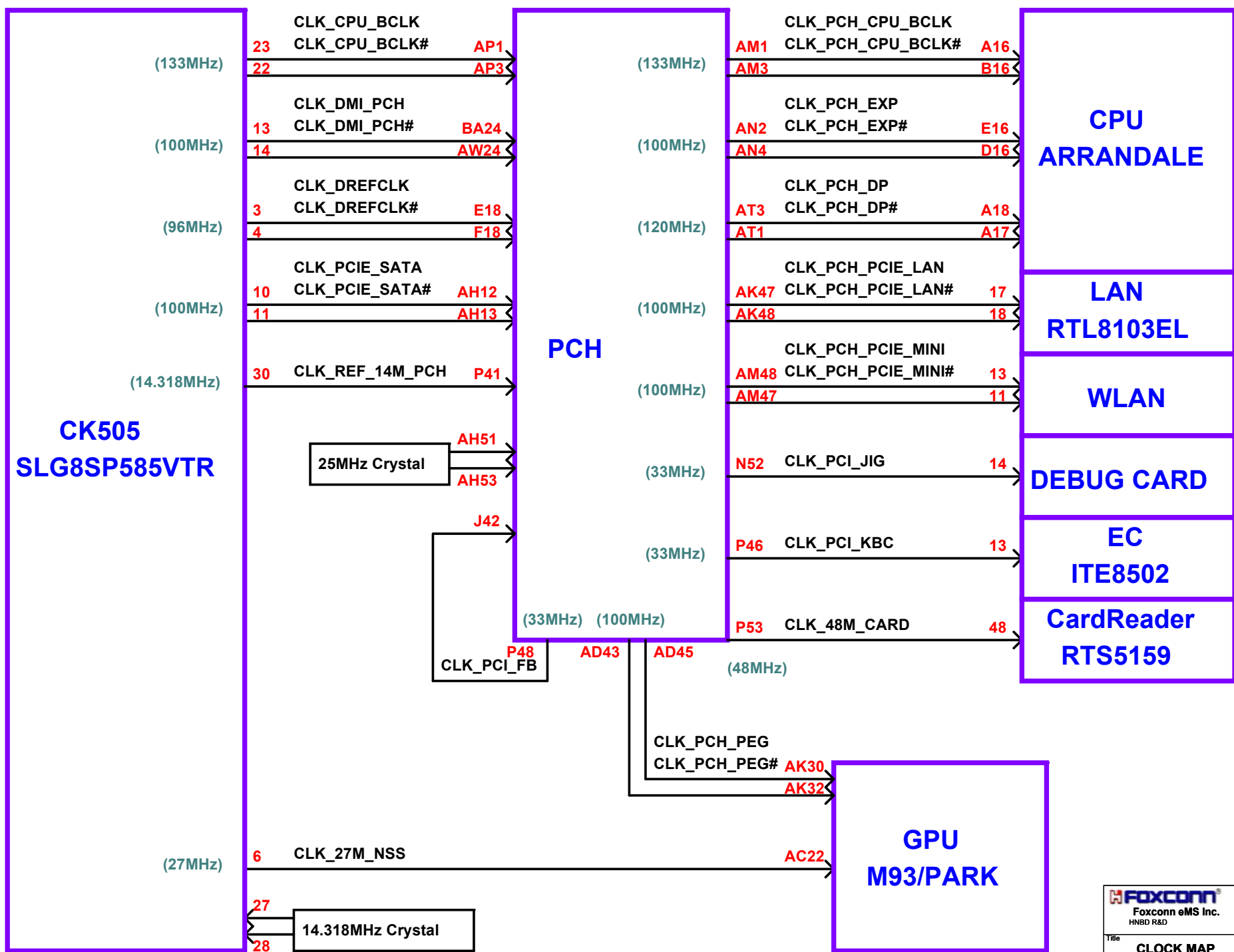
P. Leader	Check by	Design by



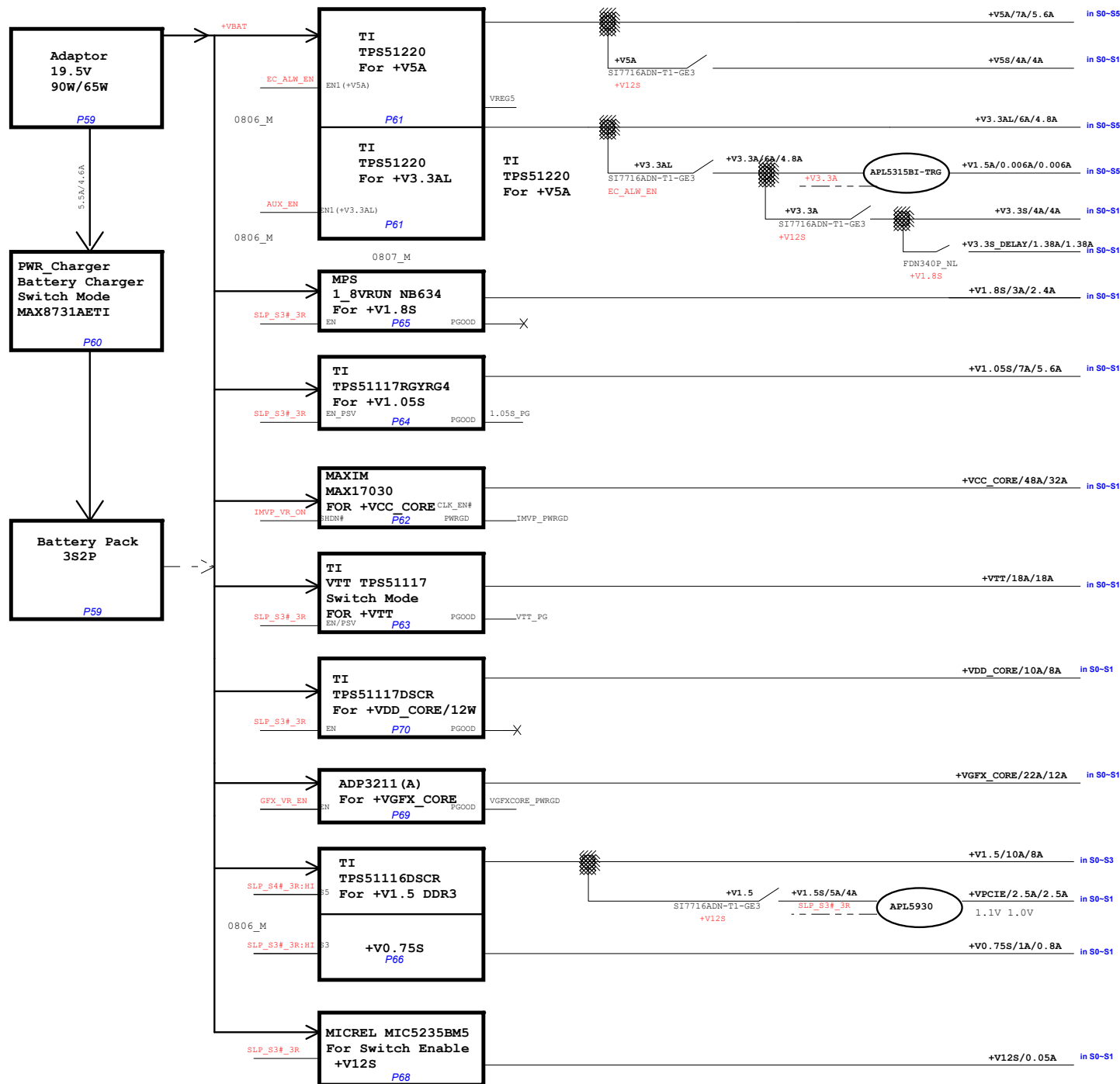
Hon Hai Precision Industry Co. Ltd.  
phone: +886-2-2799-6111

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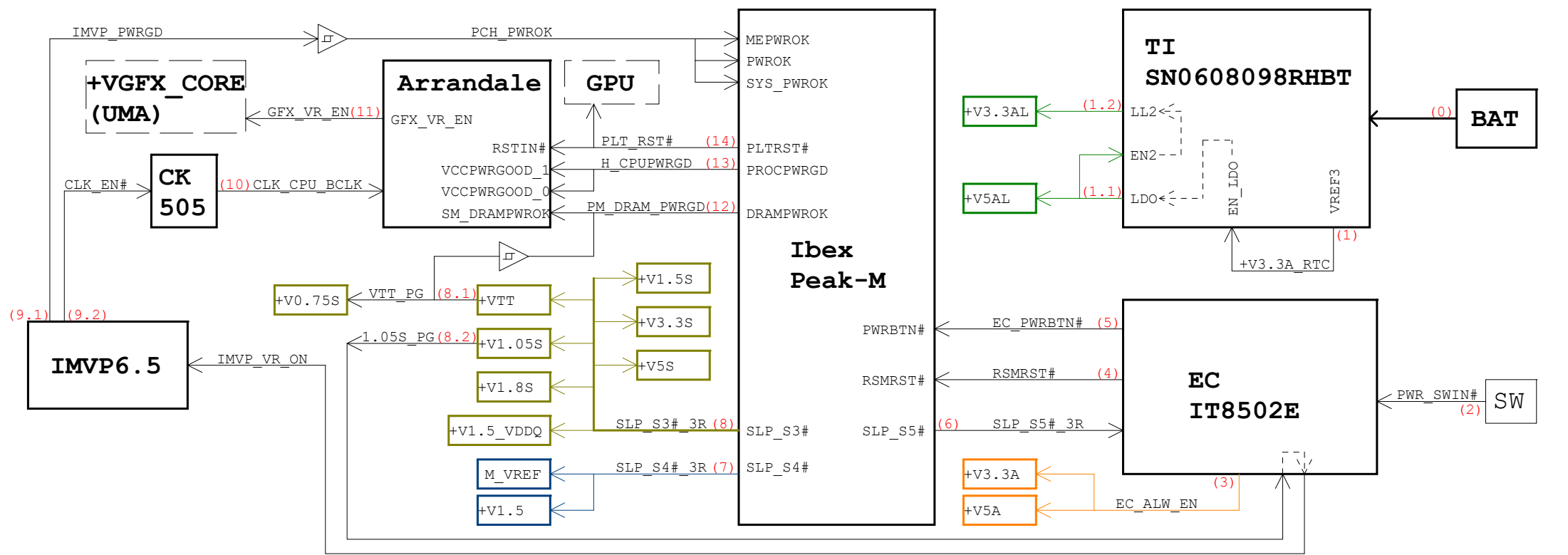




ADAPT\_OC\_IINP to IT8520  
ACTIN\_EC to IT8520



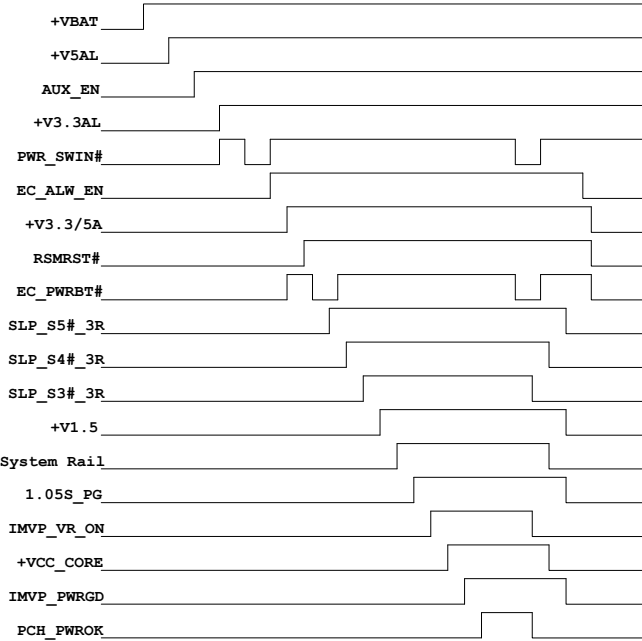
POWER SEQUENCY DIAGRAM



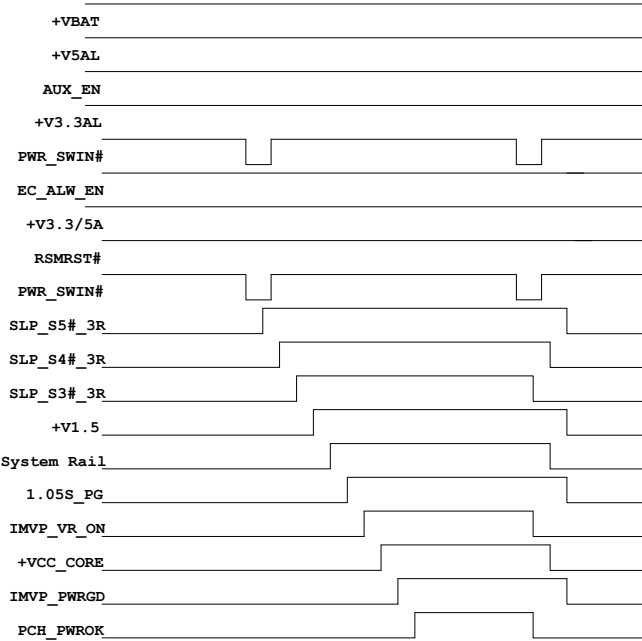
	Source Rail	EN	PG	Power Status				Remark
				S0	S3	AC S4/S5	DC S4/S5	
+VBAT				V	V	V	V	
+V5AL	+VBAT	+V3.3A_RTC		V	V	V	V	
+V3.3AL	+VBAT	+V5AL		V	V	V	V	
+V5A	+VBAT	EC_ALW_EN		V	V	V		
+V3.3A	+V3.3AL	EC_ALW_EN		V	V	V		
+V1.5	+VBAT	SLP_S4#_3R		V	V			
+V0.75S	+V1.5	VTT_PG		V				
+V1.5S	+V1.5	RUN_ON_LOAD		V				
+V1.5_VDDQ	+V1.5	RUN_ON_LOAD		V				
+VCC_CORE	+VBAT	IMVP_VR_ON	IMVP_PWRGD	V				
+VTT	+VBAT	SLP_S3#_3R	VTT_PG	V				
+VGFX_CORE	+VBAT	GFX_VR_EN		V				
+V1.8S	+VBAT	SLP_S3#_3R		V				
+V1.05S	+VBAT	SLP_S3#_3R	1.05S_PG	V				
+V5S	+V5A	RUN_ON_LOAD		V				
+V3.3S	+V3.3A	RUN_ON_LOAD		V				
+VDD_CORE	+VBAT	SLP_S3#_3R		V				
+V3.3S_Delay	+V3.3S	+V1.8S		V				
+VPCIE	+V1.5S	SLP_S3#_3R		V				

POWER SEQUENCE TIMING

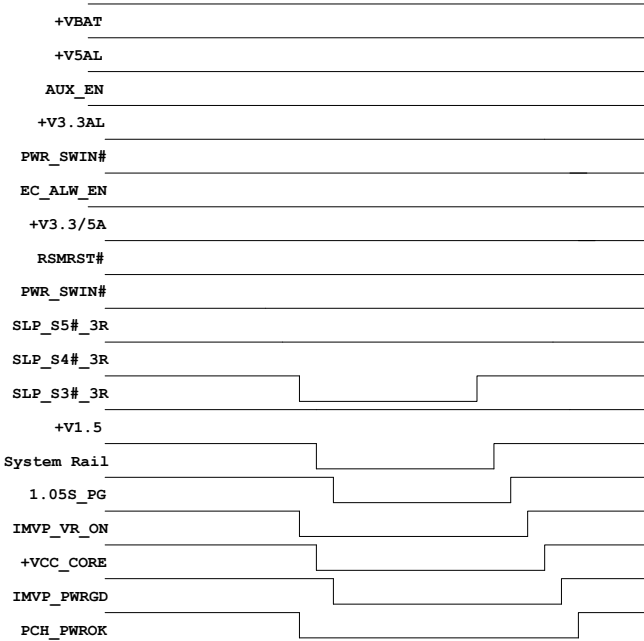
G3(OFF)->S0->S5



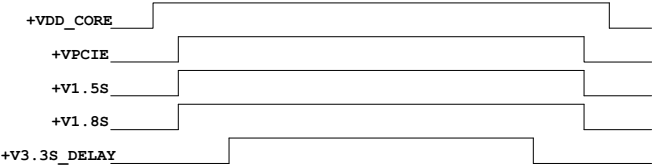
S5->S0->S5



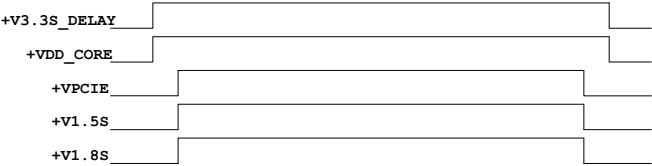
S0->S3->S0



M93 Sequence




Park Sequence



## Discrete GPU



# RESET SIGNAL MAP



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HNBD R&D

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Title

RESET SIGNAL MAP

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0.4

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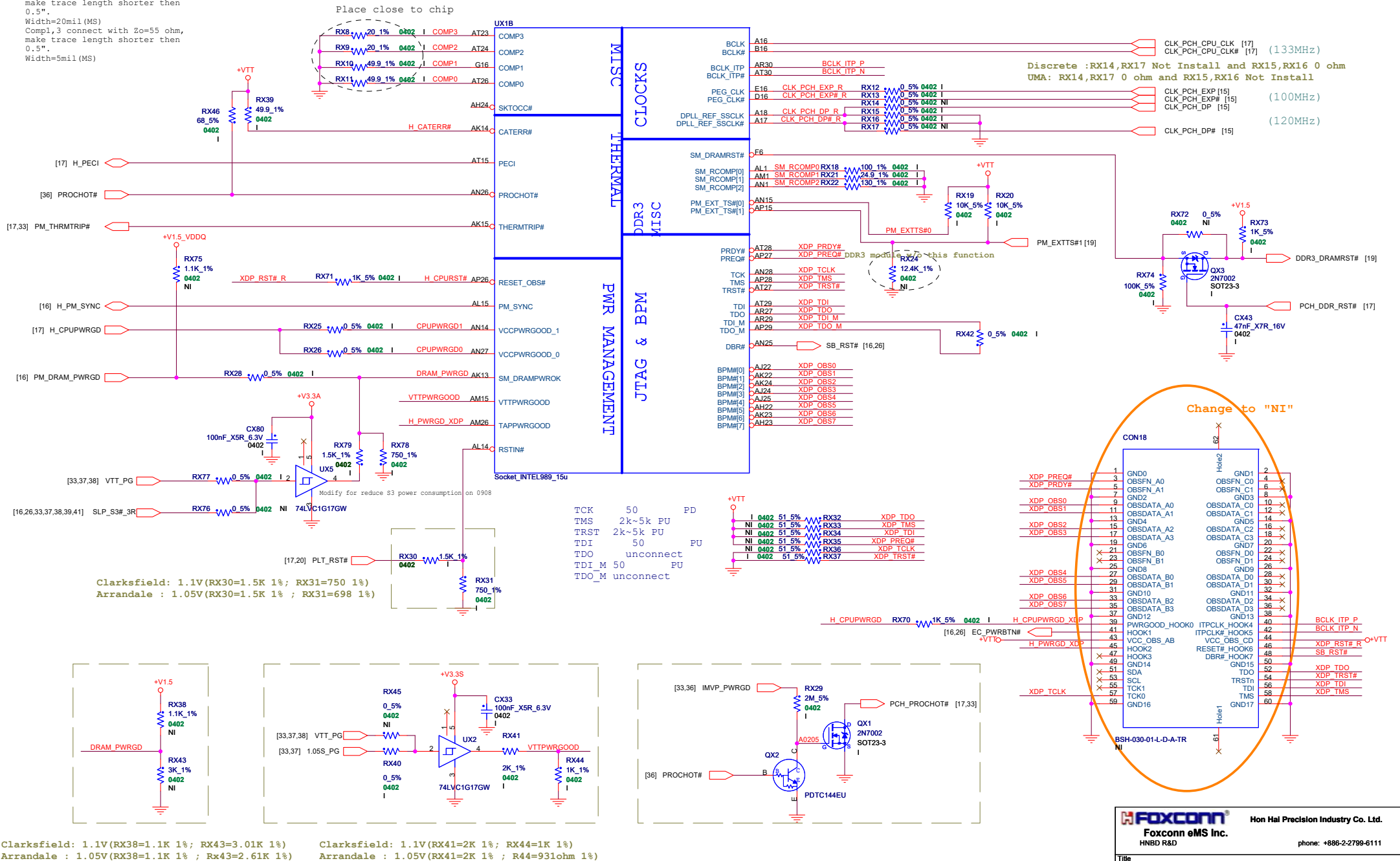
13:30:41 (UTC/GMT)

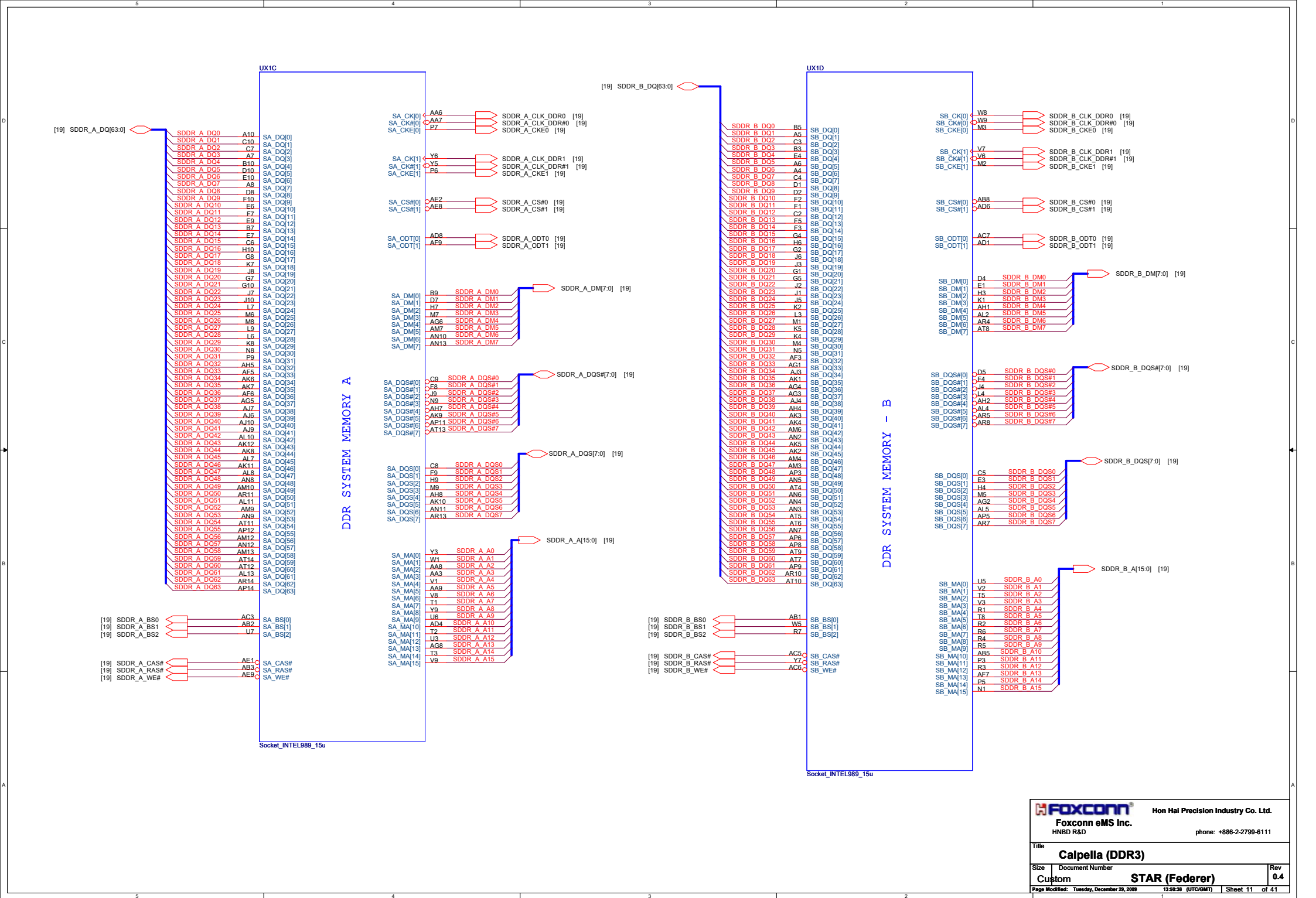
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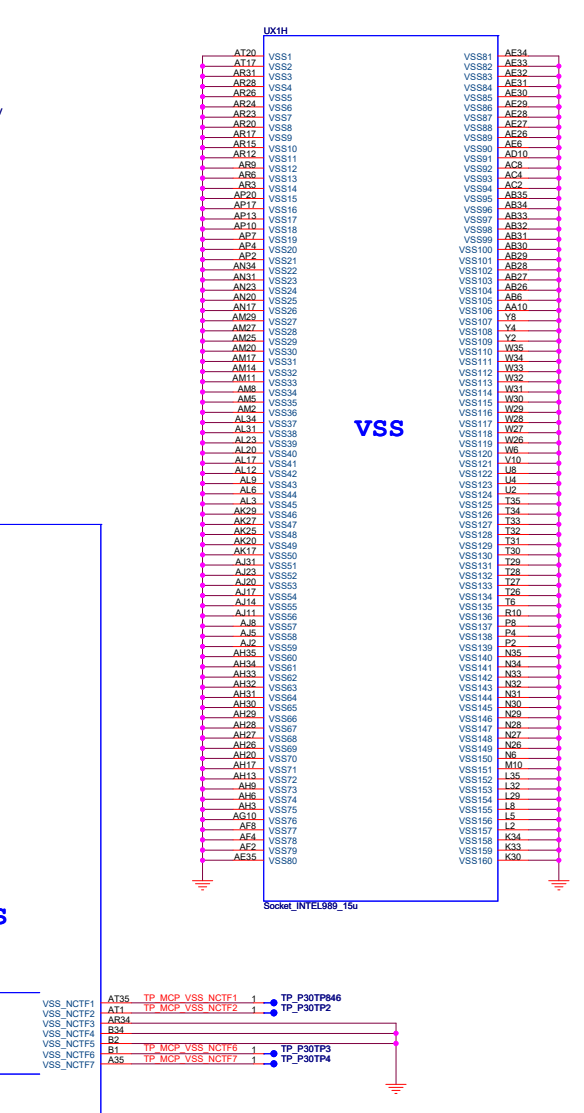
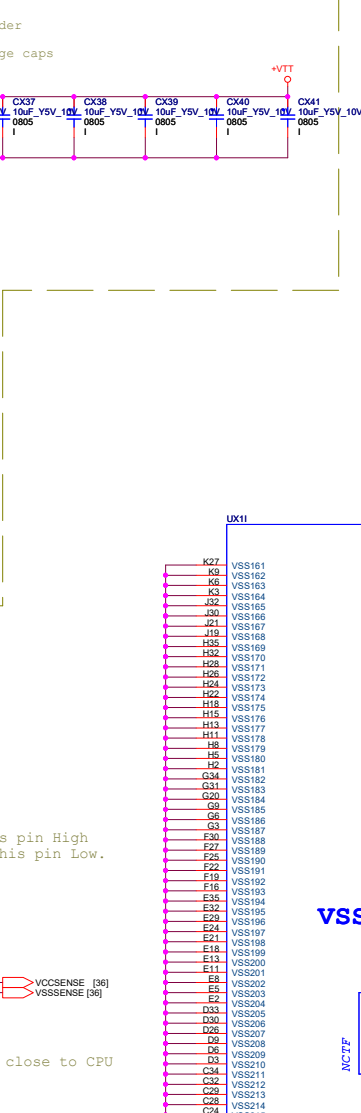
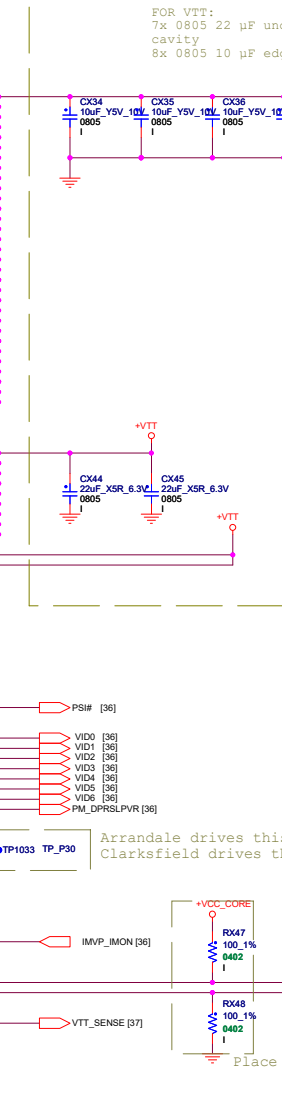
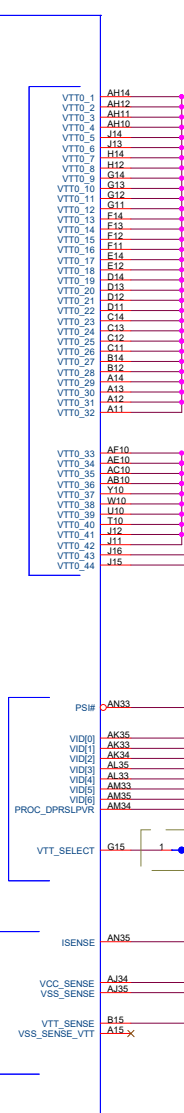
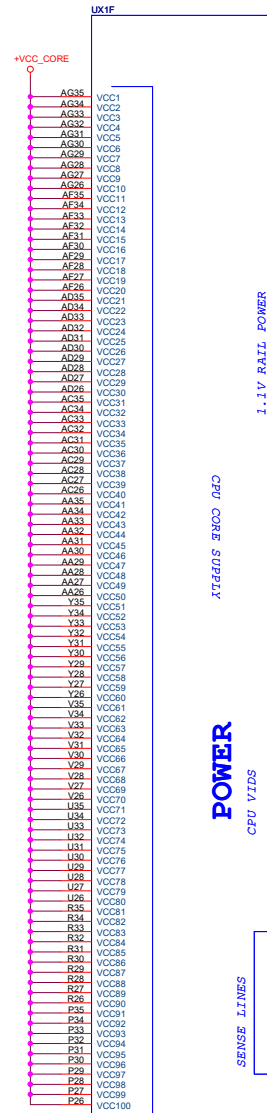
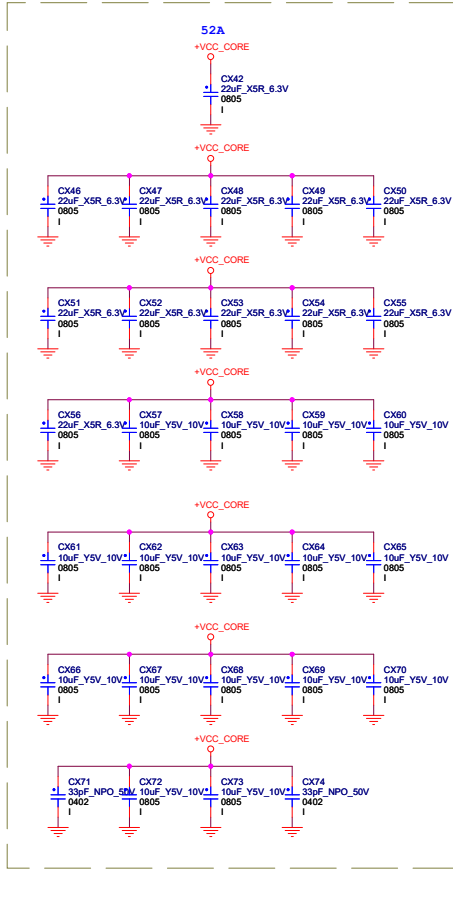


Layout Note:  
Comp0,2 connect with  $Z_0=27.4$  ohm,  
make trace length shorter then  
0.5".  
Width=20mil(MS)  
Comp1,3 connect with  $Z_0=55$  ohm,  
make trace length shorter then  
0.5".  
Width=5mil(MS)





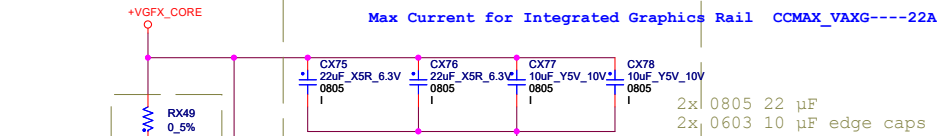
FOR VCC:  
12x 0805 22  $\mu$ F inside cavity,  
7x 0805 10  $\mu$ F under cavity and 9 x 0805 10  $\mu$ F  
between inductor and socket on top layer



+VTT to +VTT [10,13,17,18,28,36,37,40]  
+VCC\_CORE to +VCC\_CORE [36]

Arrandale drives this pin High  
Clarkfield drives this pin Low.

Place close to CPU

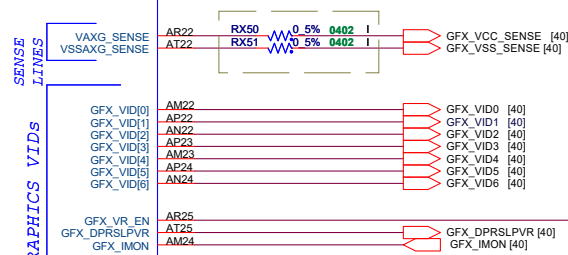


Discrete GPU: Not Install  
UMA: Install

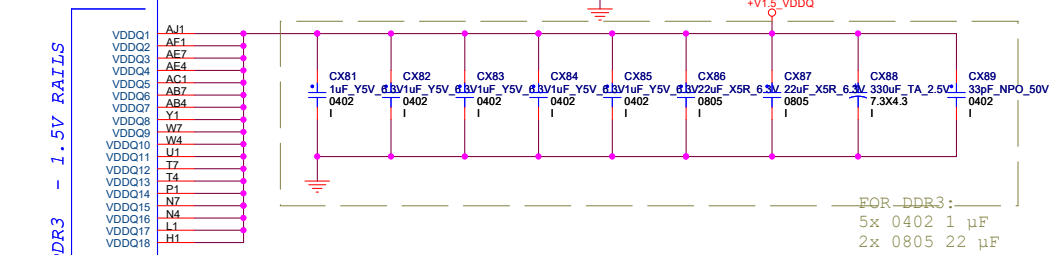


Discrete GPU: Not Install  
UMA: Install

Discrete GPU: Install  
UMA: Not Install



Discrete GPU: Not Install  
UMA: Install



## POWER

DDR3 - 1.5V RAILS

1.1V

1.8V

PEG & DMI

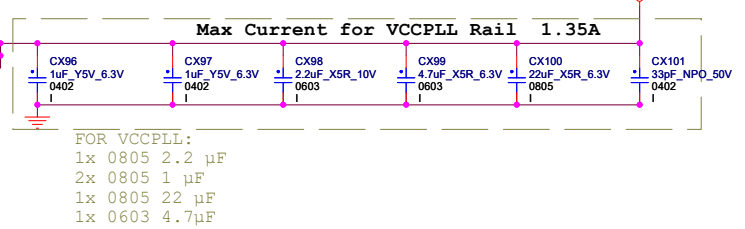
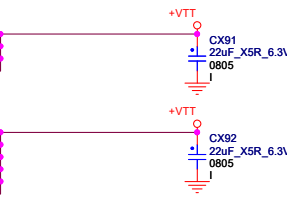
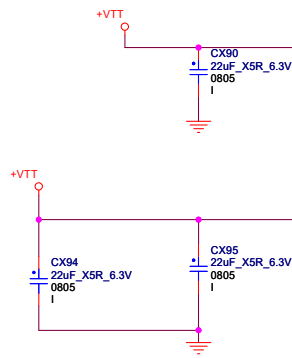
GRAPHICS

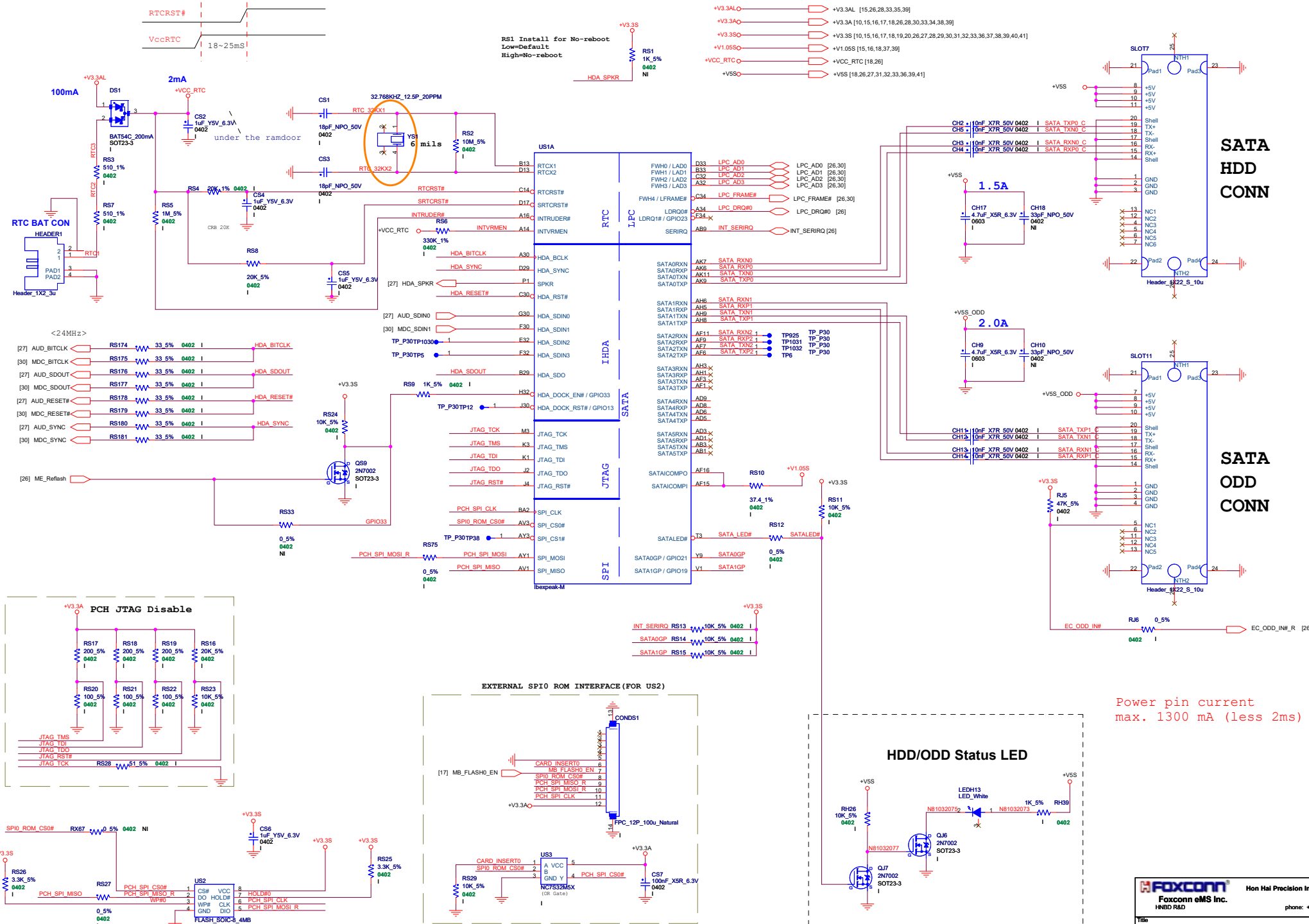
SENSE LINES

GRAPHICS VIDS

UX1G

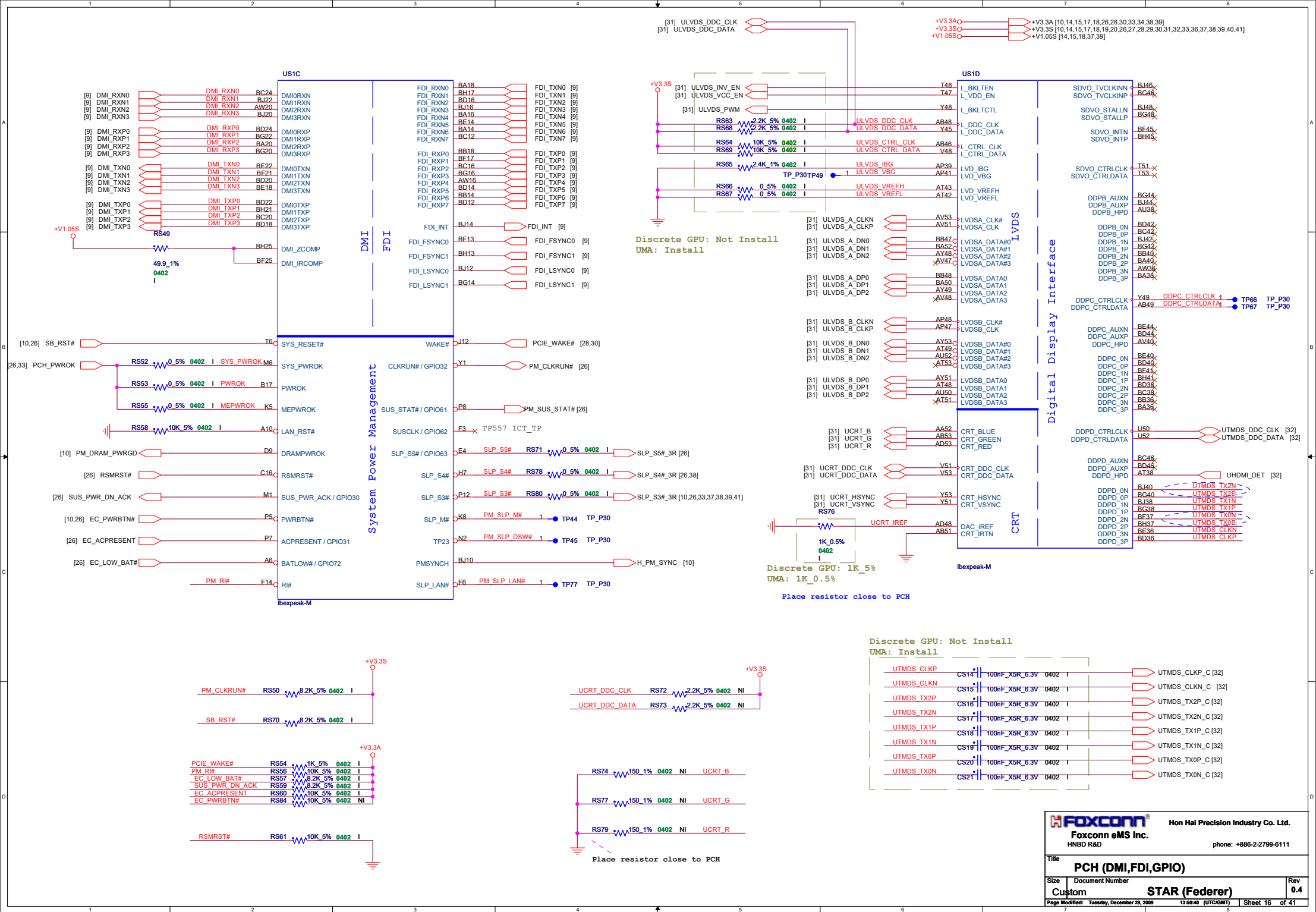
Socket\_INTEL989\_15u



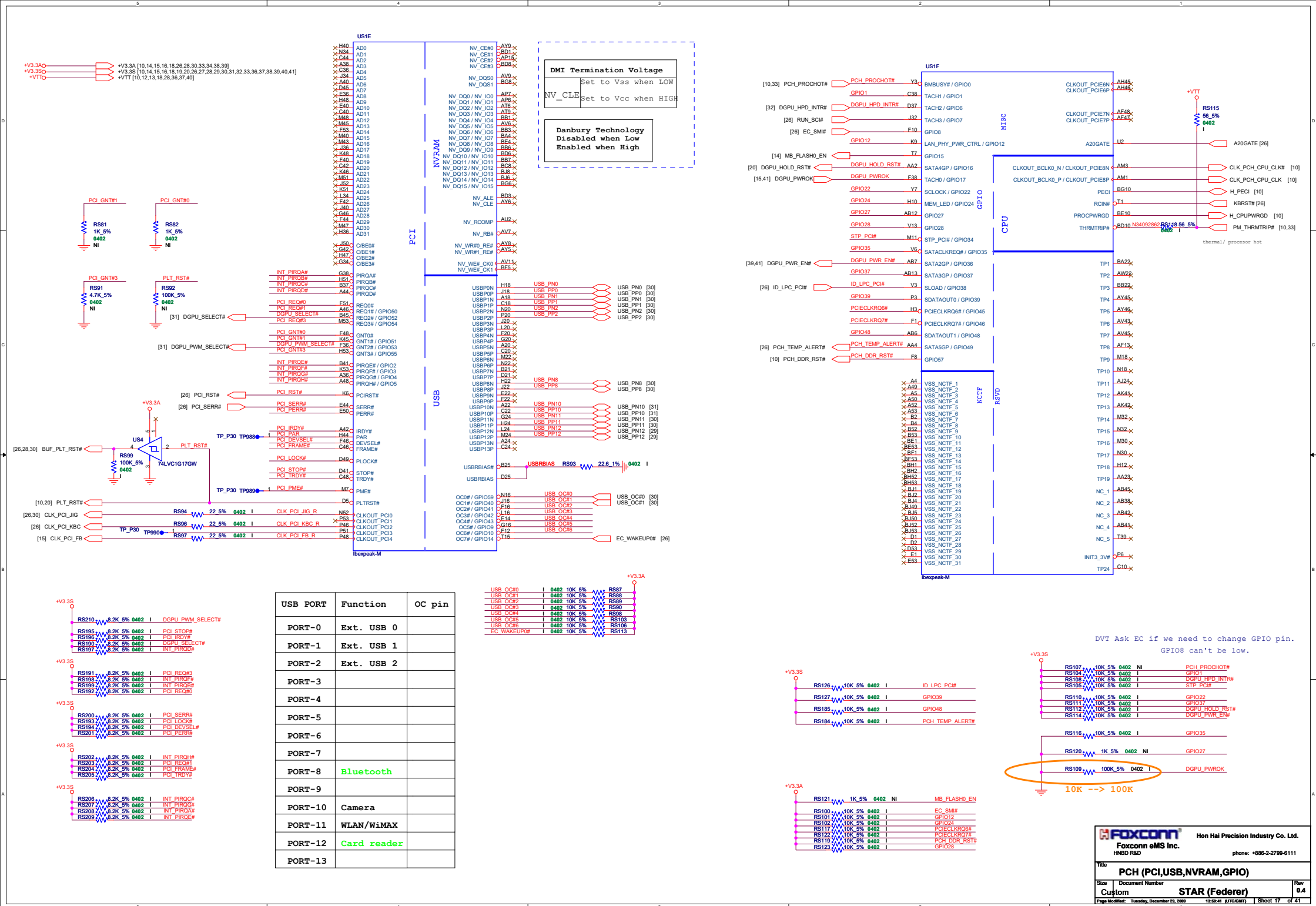


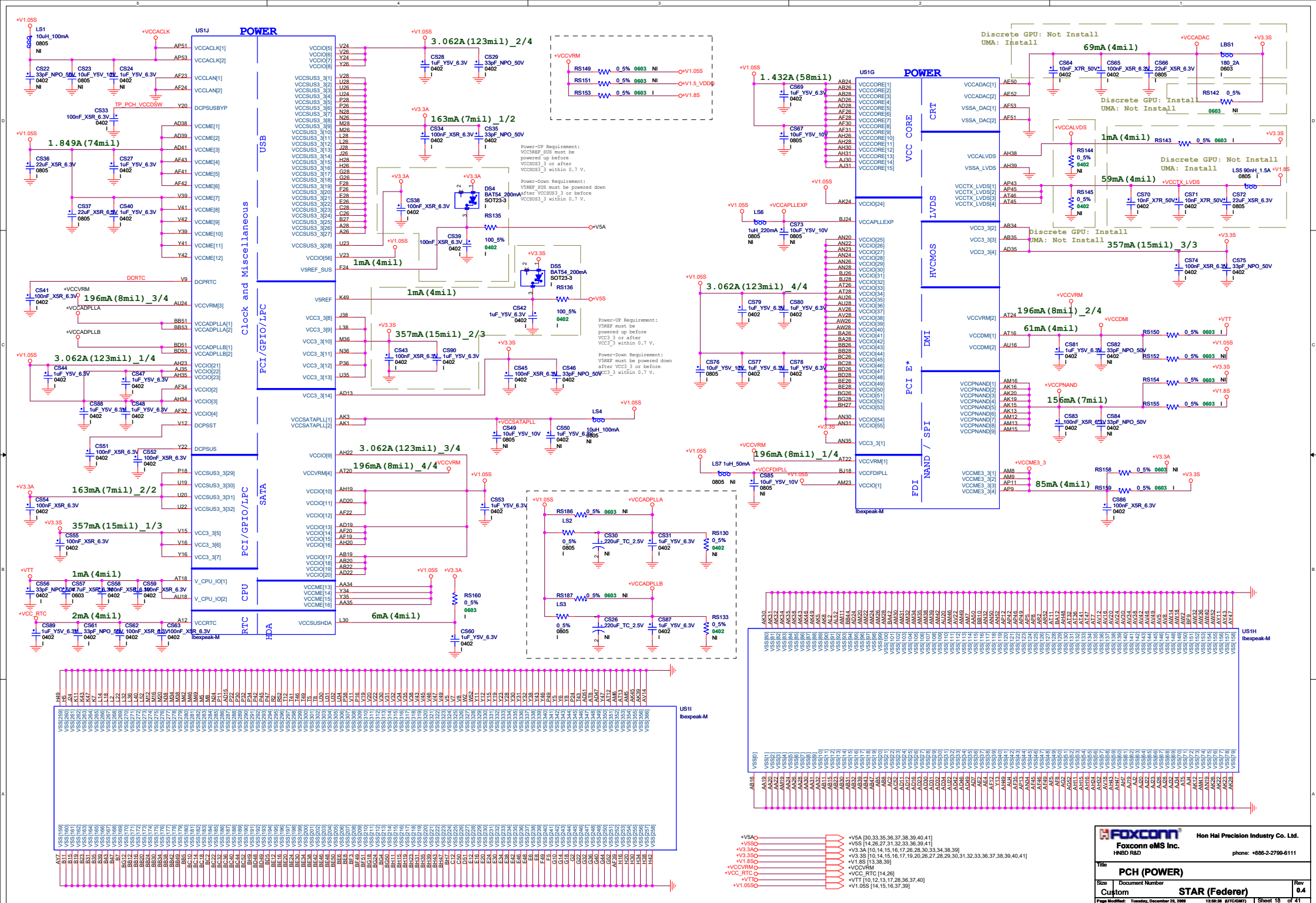


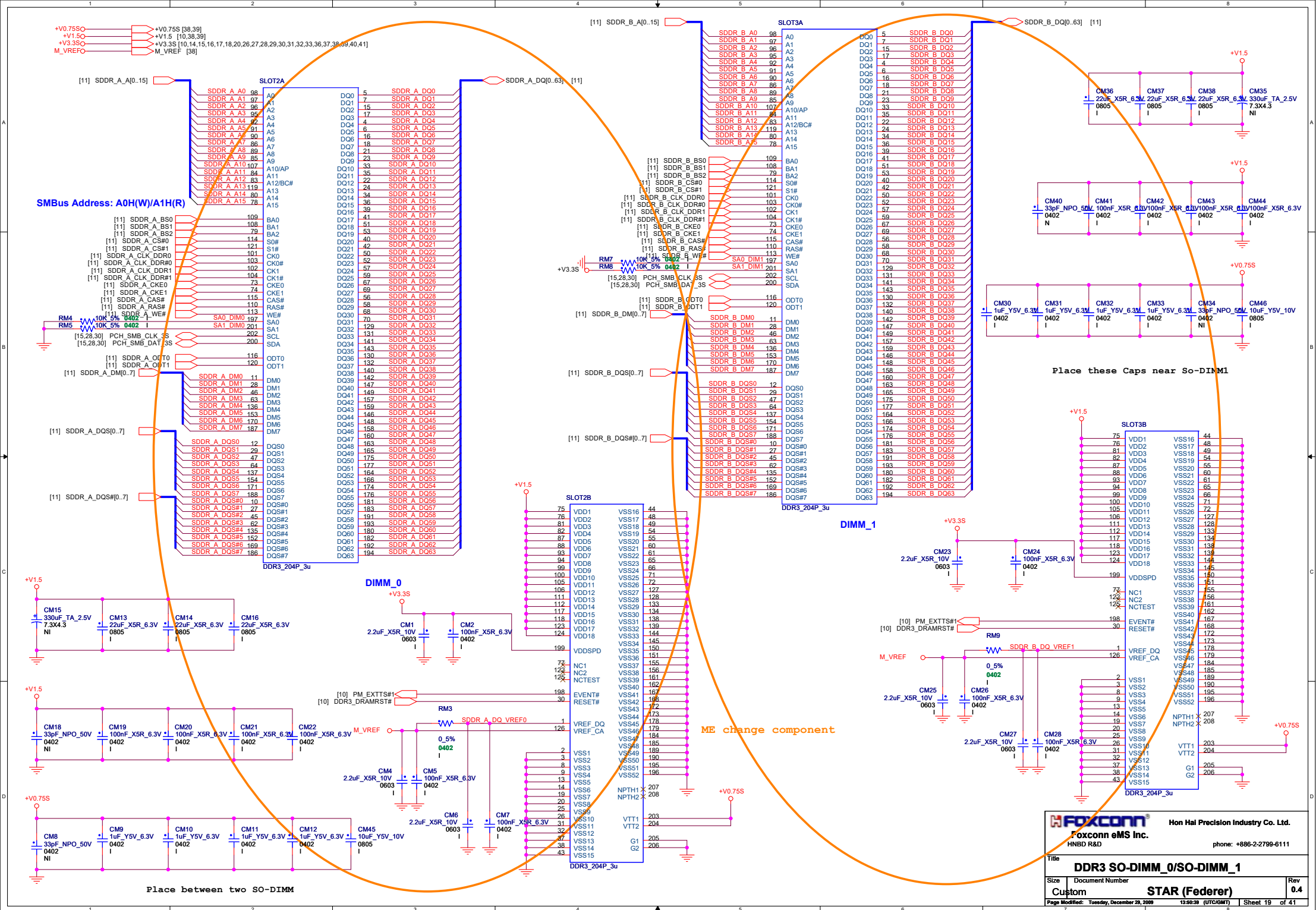


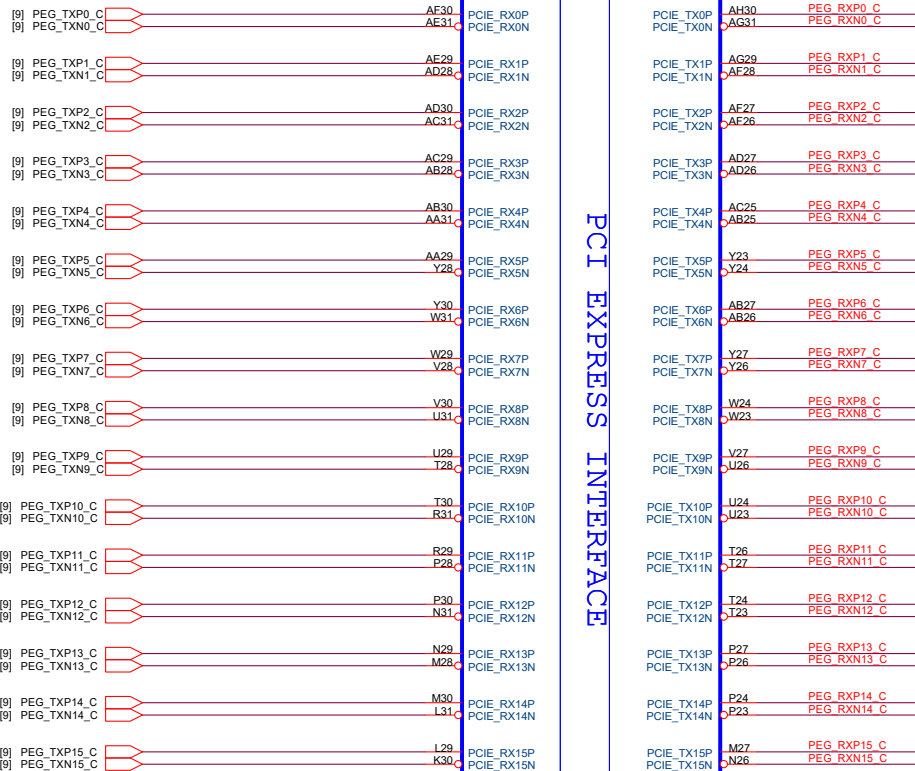






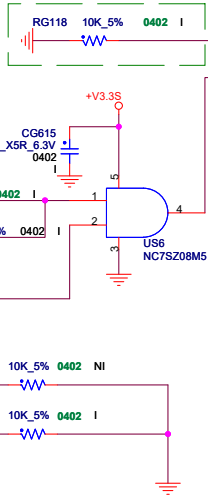






PCI EXPRESS INTERFACE

M93-S3 Not Install  
PARK-S3 Install 10K ohm



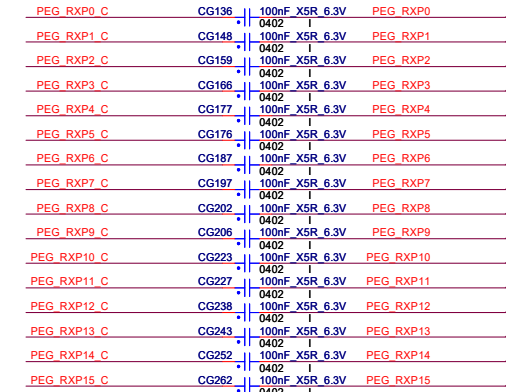
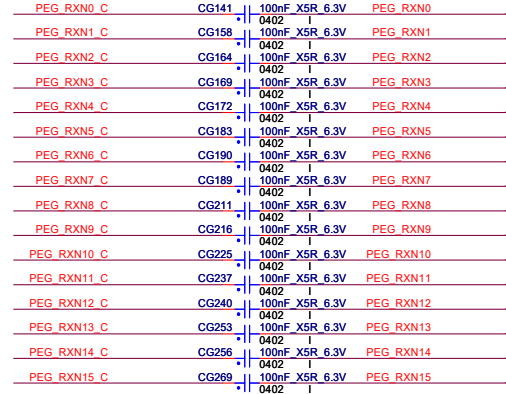
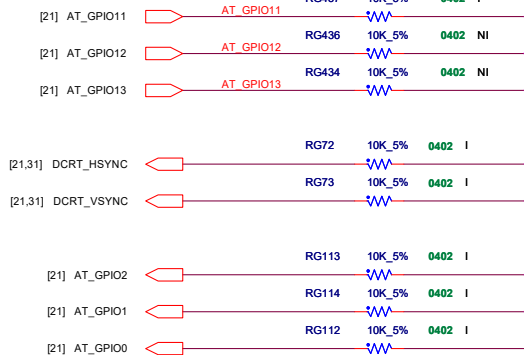
If no ROM attached, GPIO[13:12:11] ;  
CONFIG(2:0)  
controls the memory aperture size.

Reserved 011  
512MB 001

HSYNC , VSYNC  
AUD[1] , AUD[0]

0,0 No audio function  
0,1 Audio for DisplayPort and HDMI if dongle is detected  
1,0 Audio for DisplayPort only  
1,1 Audio for both DisplayPort and HDMI

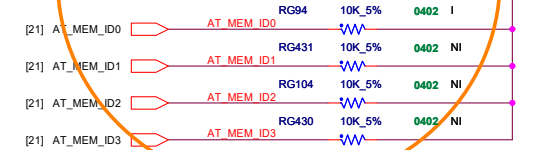
GPIO 0 : PCIE FULL TX OUTPUT SWING  
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED  
GPIO 2 : PCIE GEN2 ENABLED



Modify setting by different VRAM vendor

Strap for DDR3  
AT\_MEM\_ID (3:2:1:0)

0000	64Mx16	Samsung (K4W1G1646E-HC12)	512MB
0001	64Mx16	Hynix (H5TQ1G63BFR-12C)	512MB
0010	128Mx16	Samsung (K4W2G1646B-HC12)	1GB
0100	128Mx16	Samsung (K4W2G1646C-HCxx)	1GB
1000	128Mx16	Hynix (H5TQ2G63BFR-12C)	1GB
1001	128Mx16	Micron (MT41J128M16HA-12)	1GB

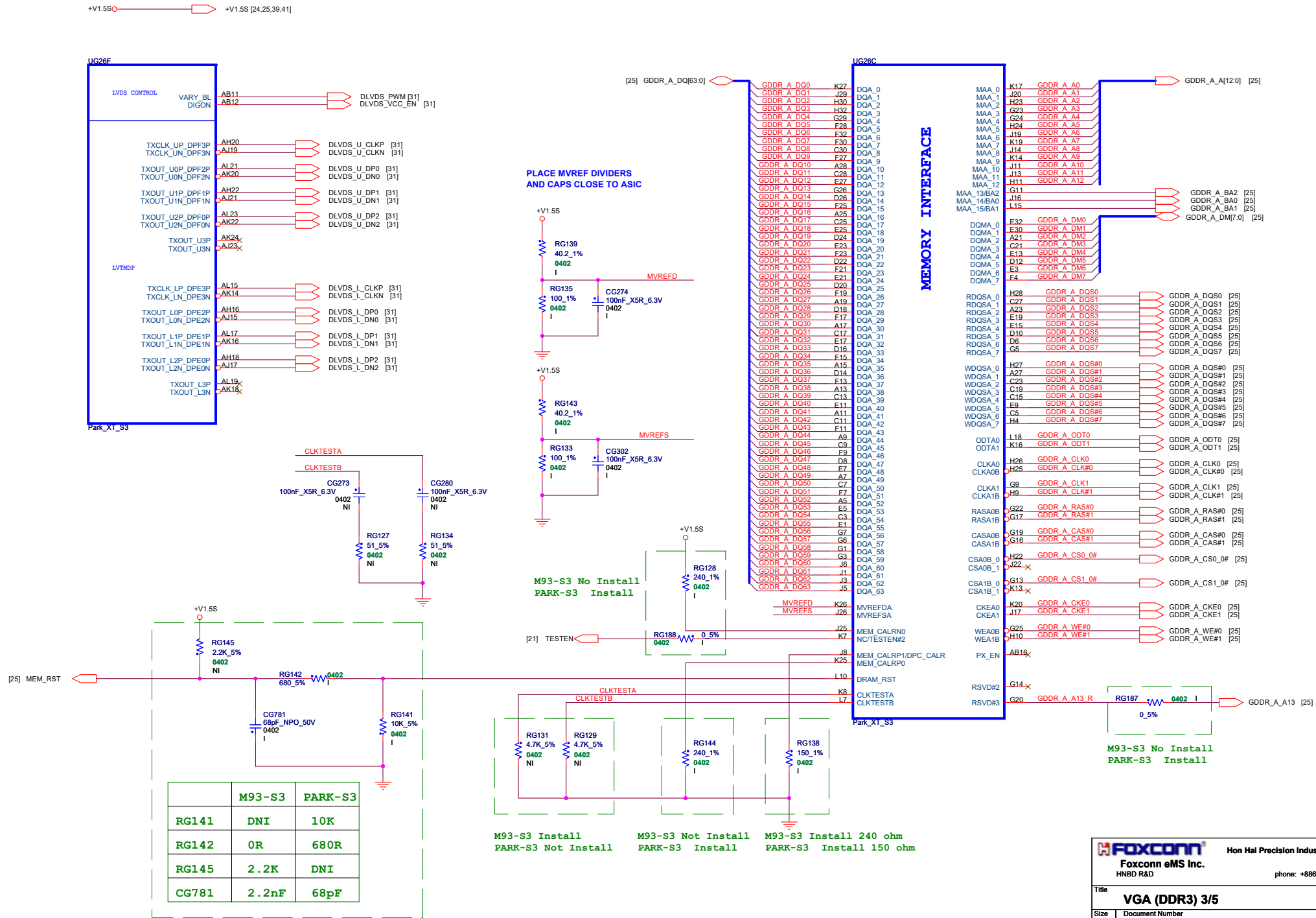




M93-S3:Not Install  
PARK-S3:Install

Del NorFlash parts

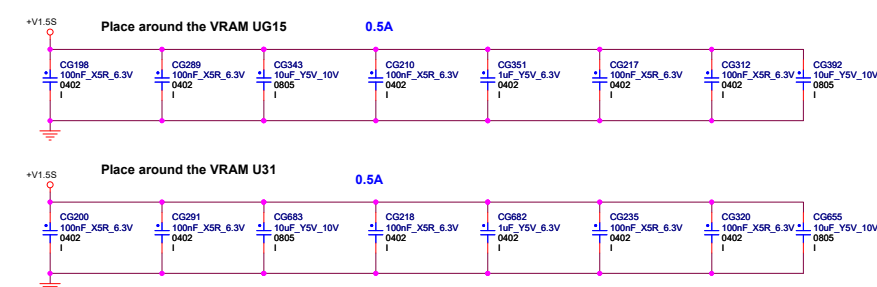
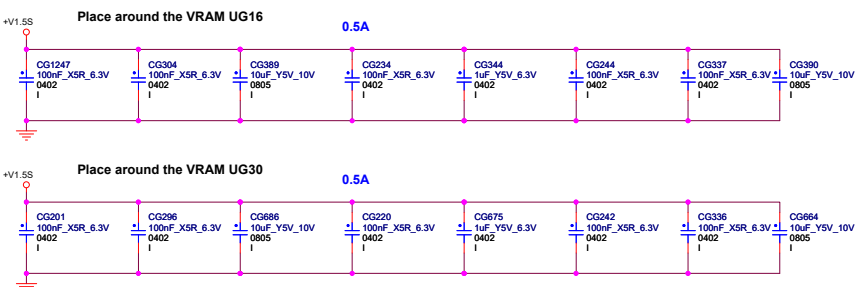
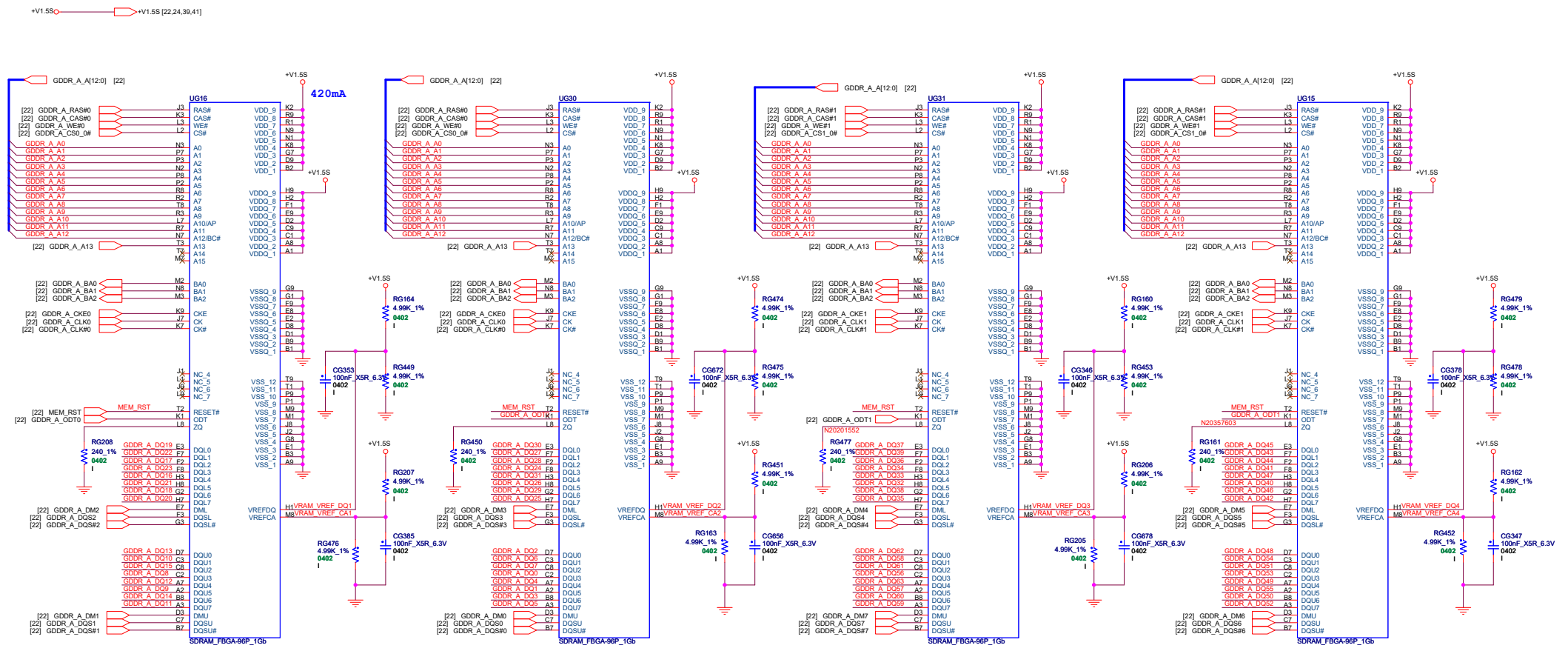
clock source change to clock gen.

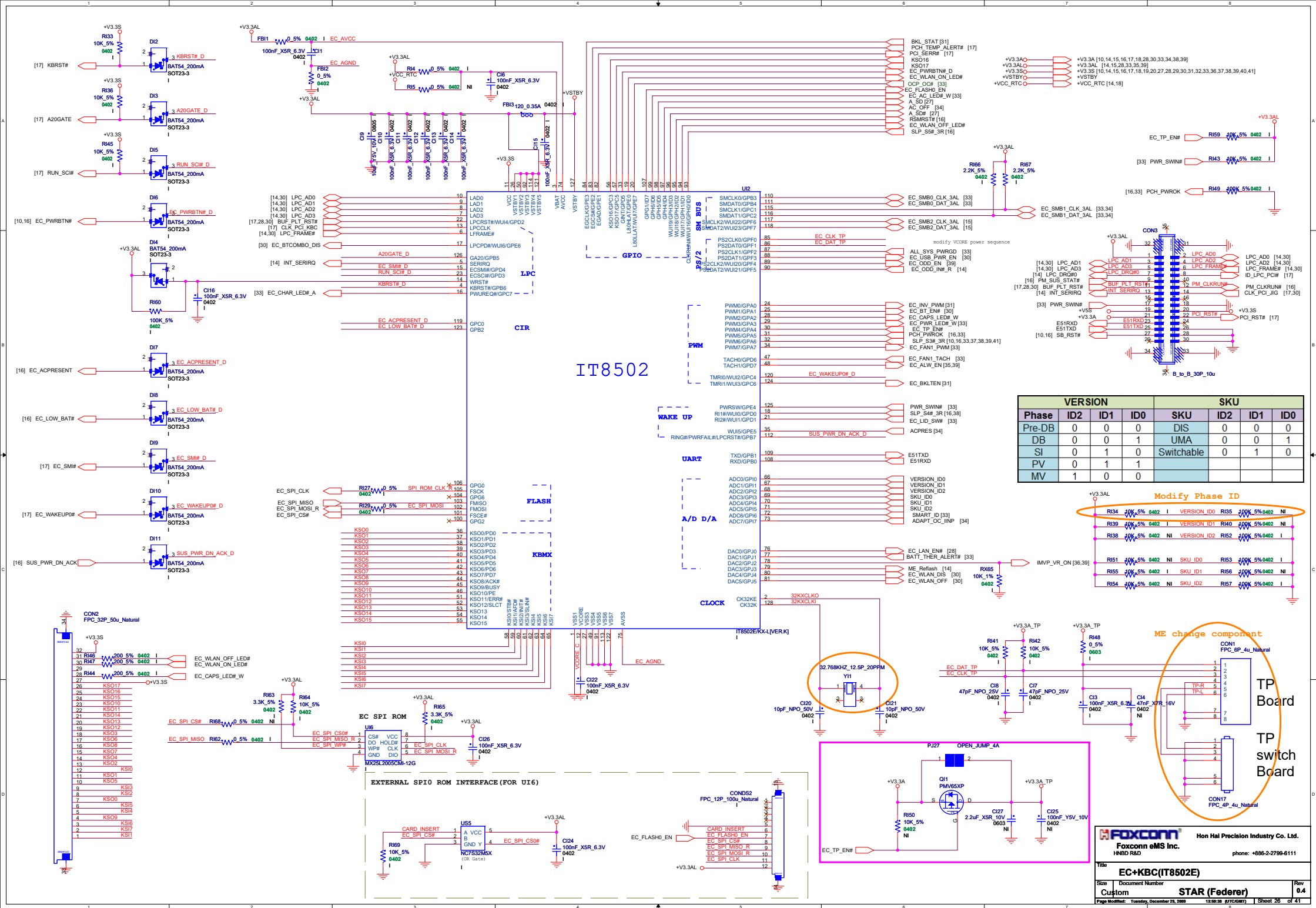


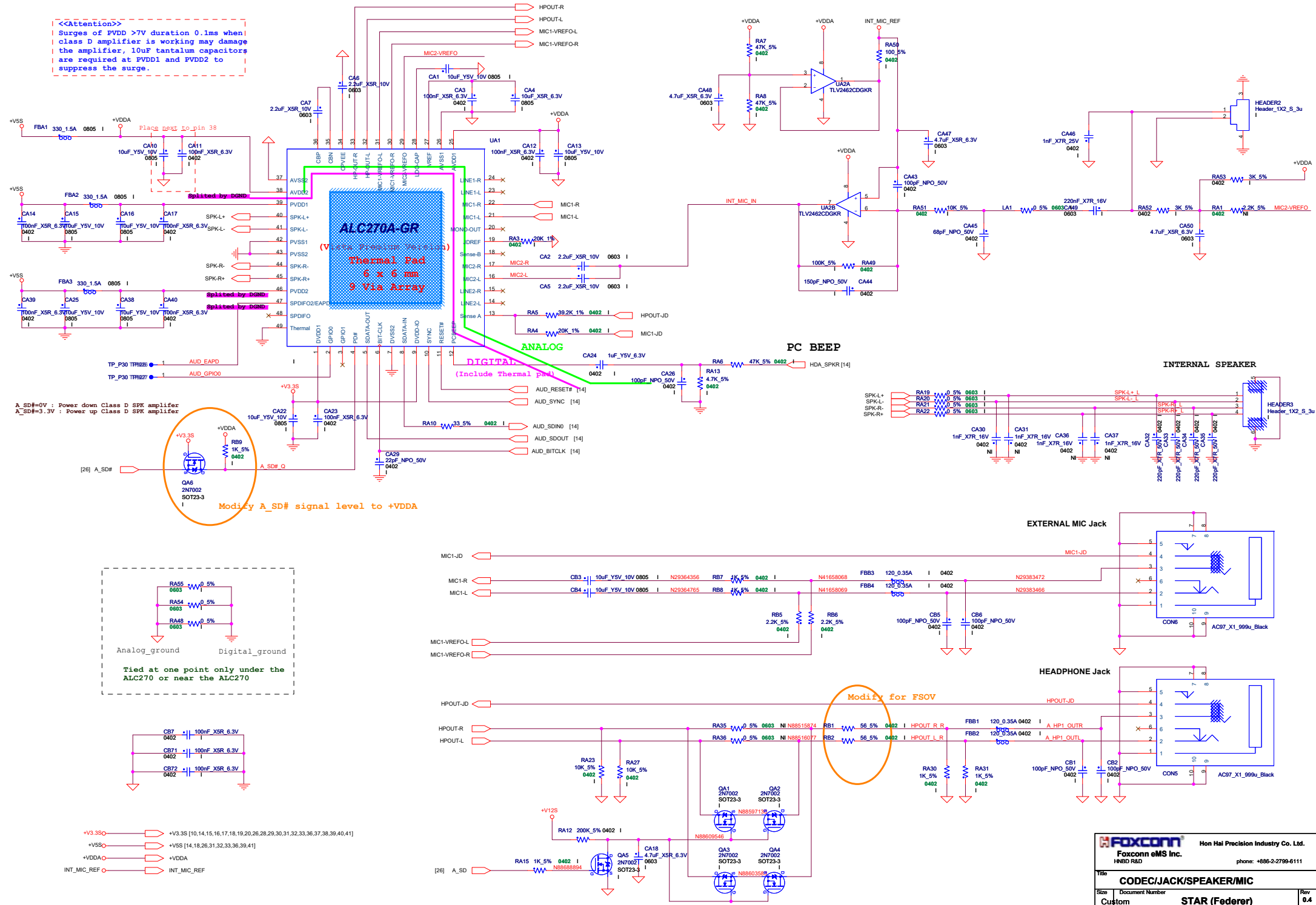


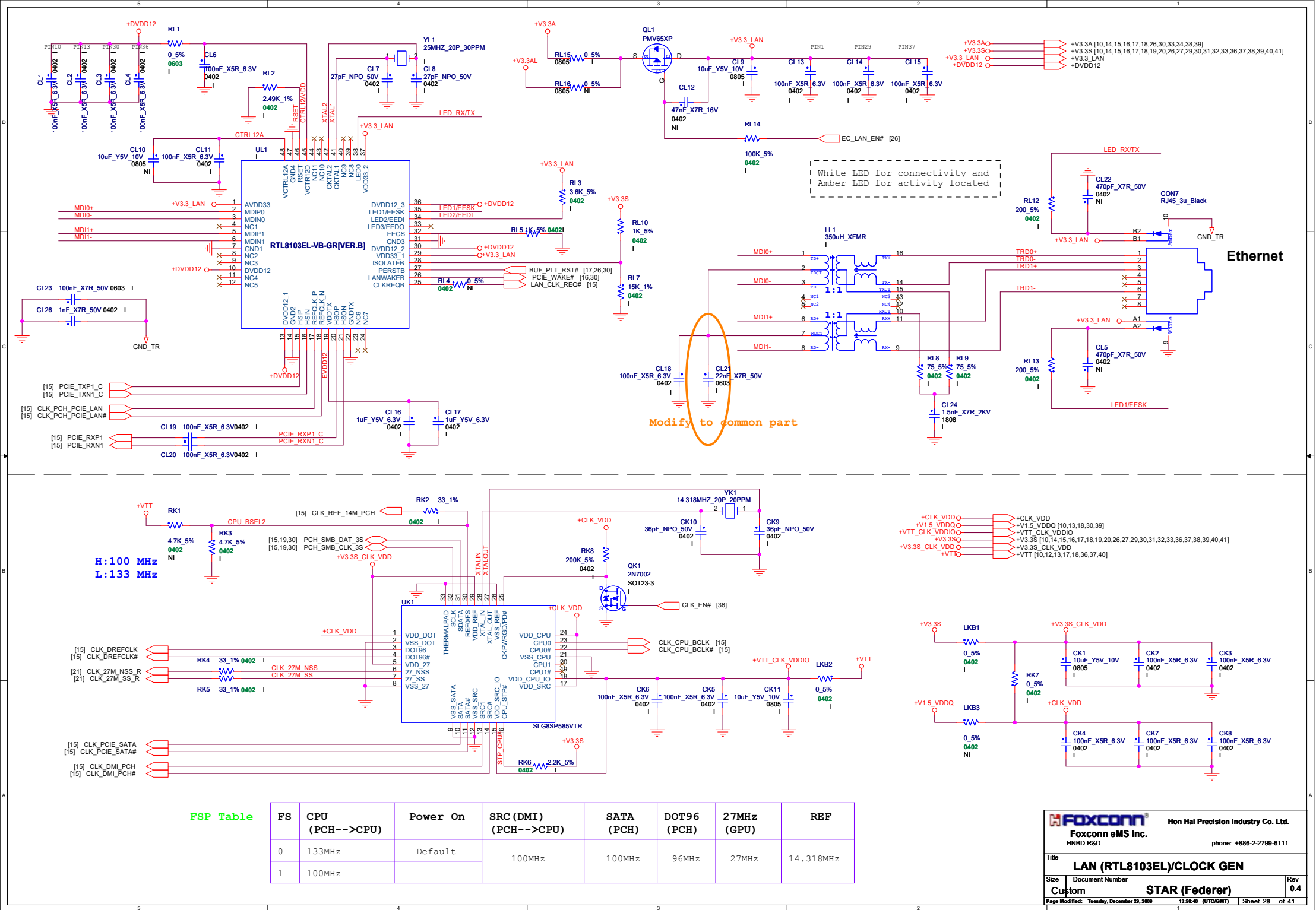


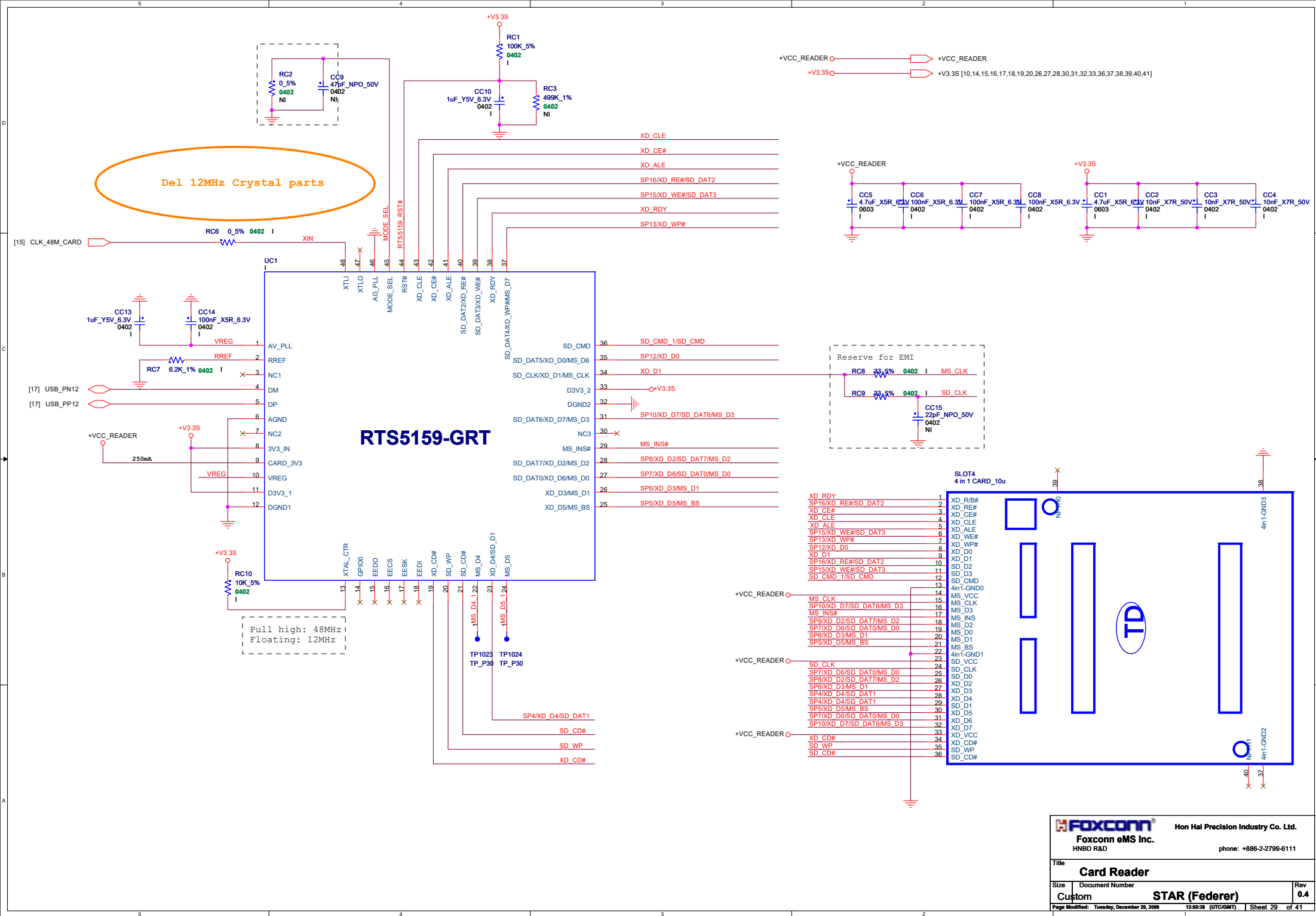




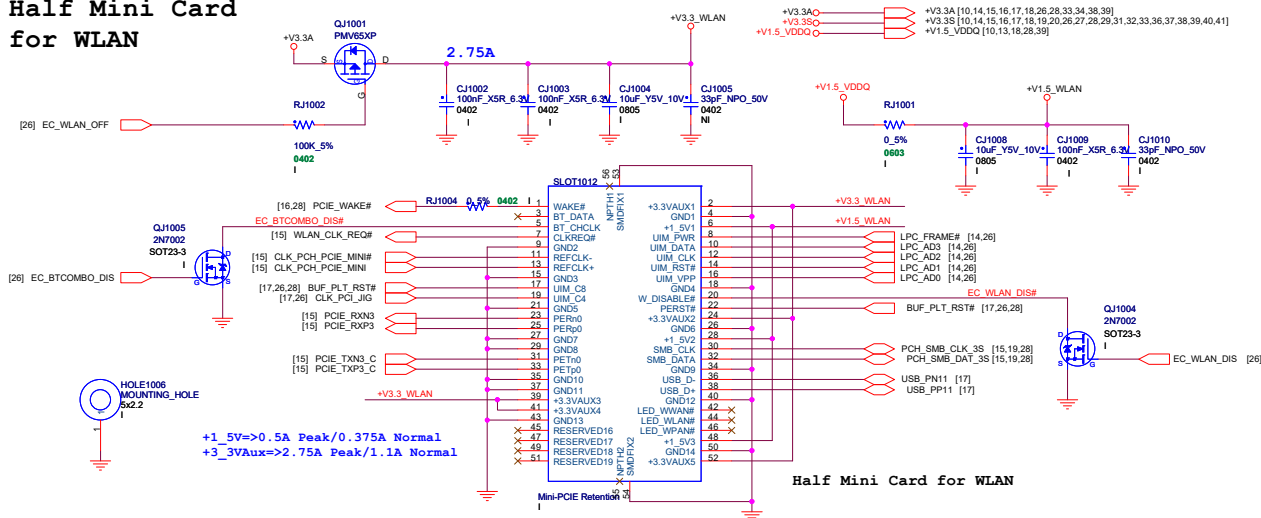




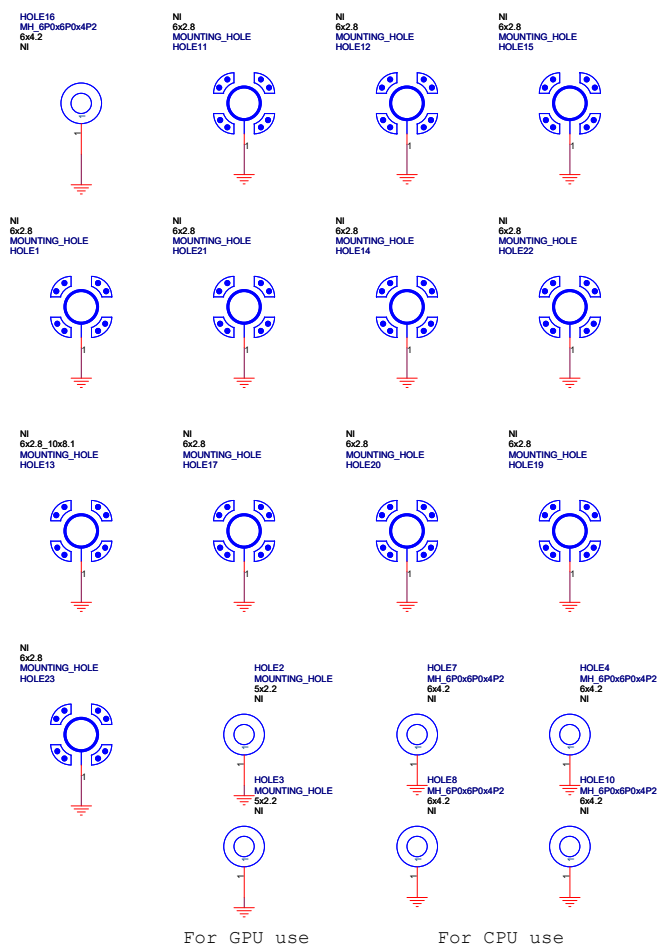




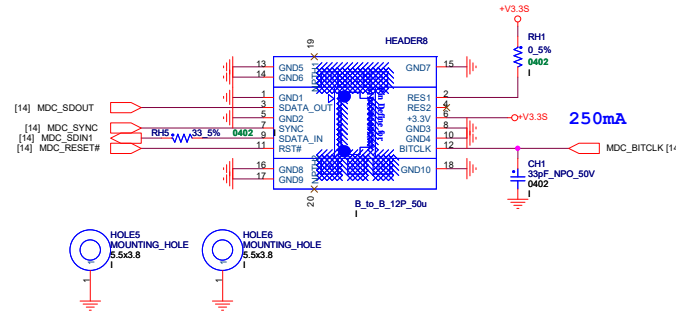
# Half Mini Card for WLAN



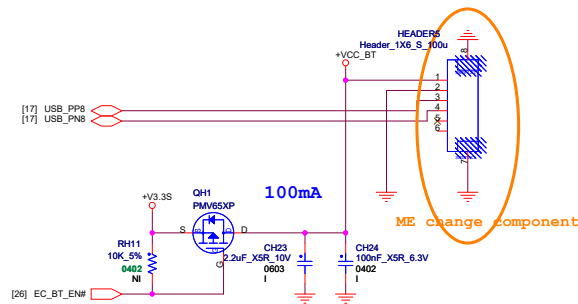
# MOUNTING HOLE



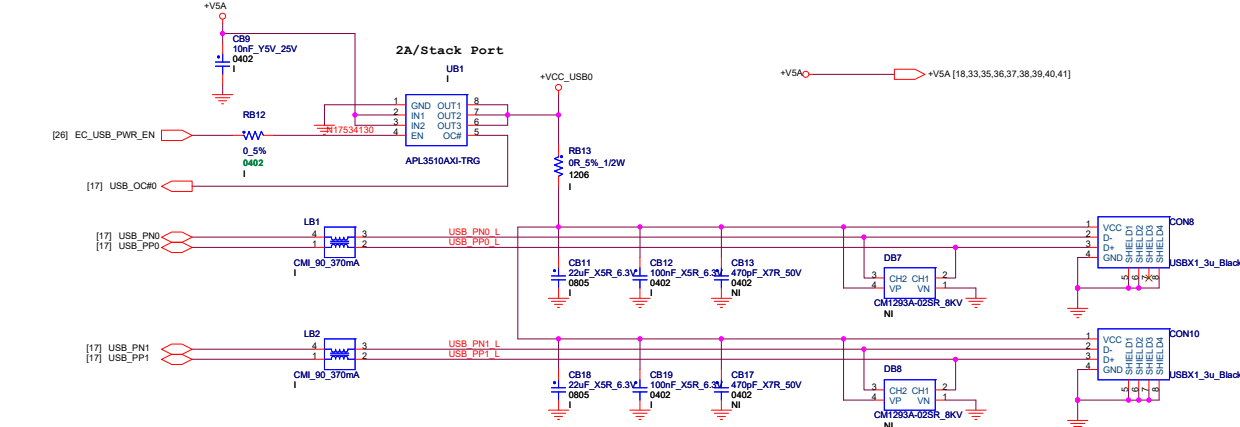
# MDC CONN.



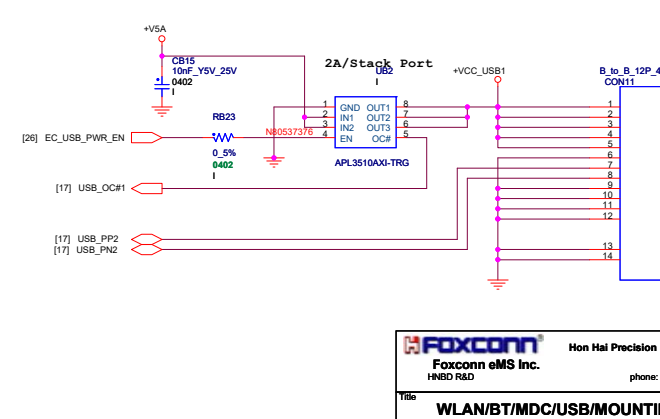
# Bluetooth CONN.



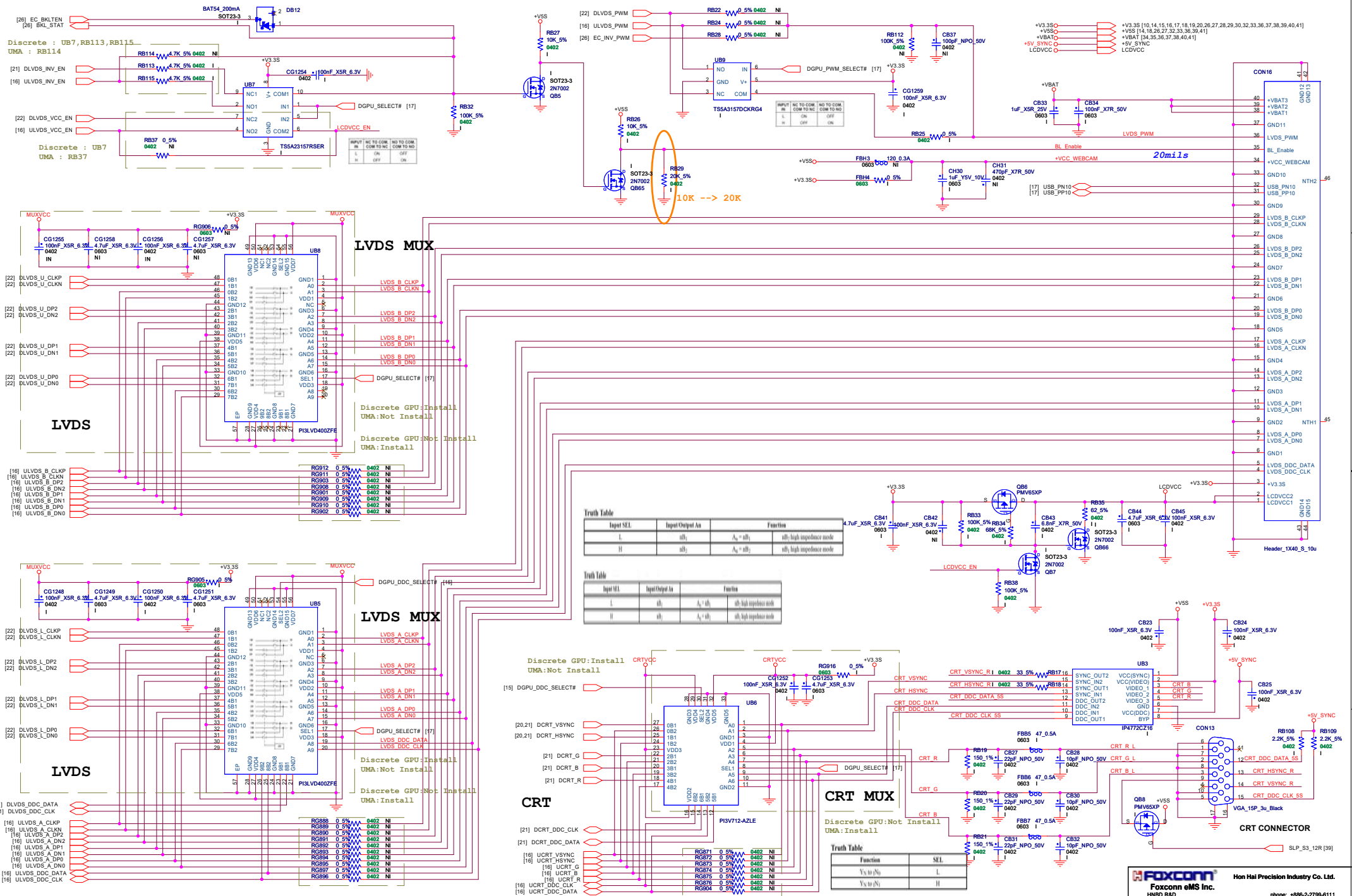
# USBX2 CONN.



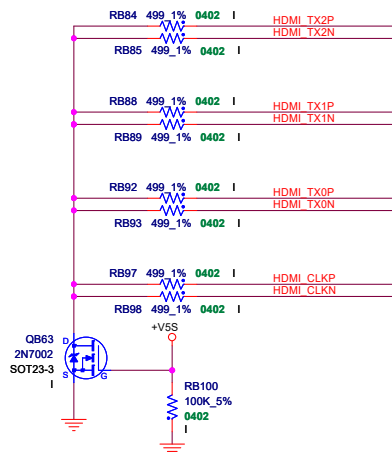
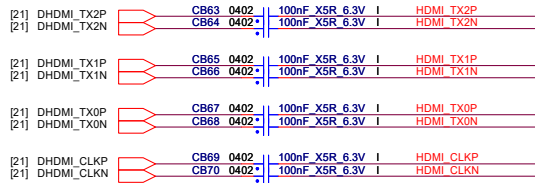
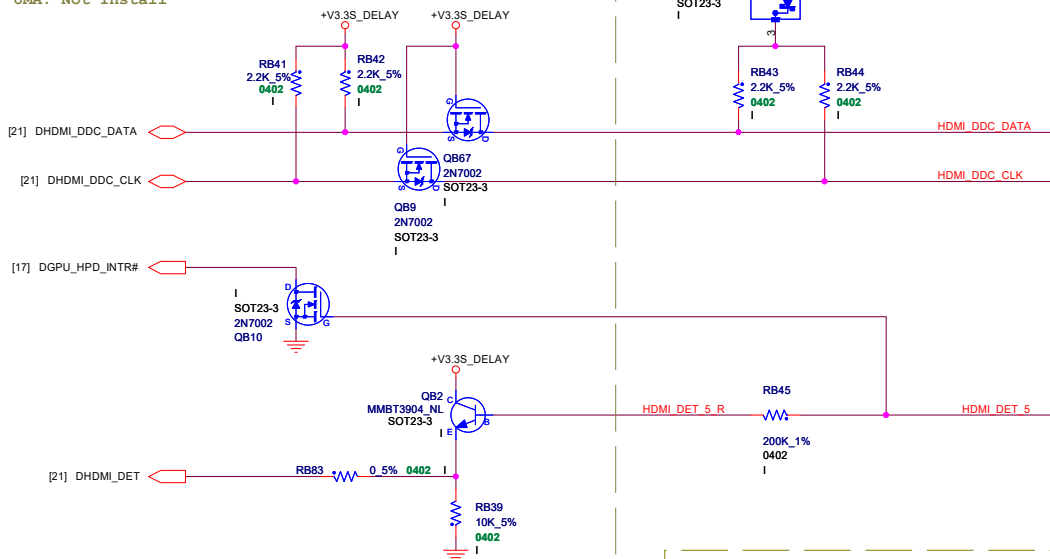
# USBX1 CONN.



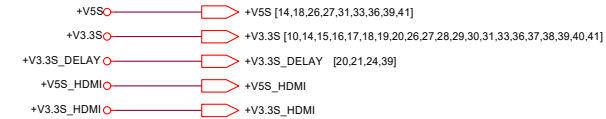
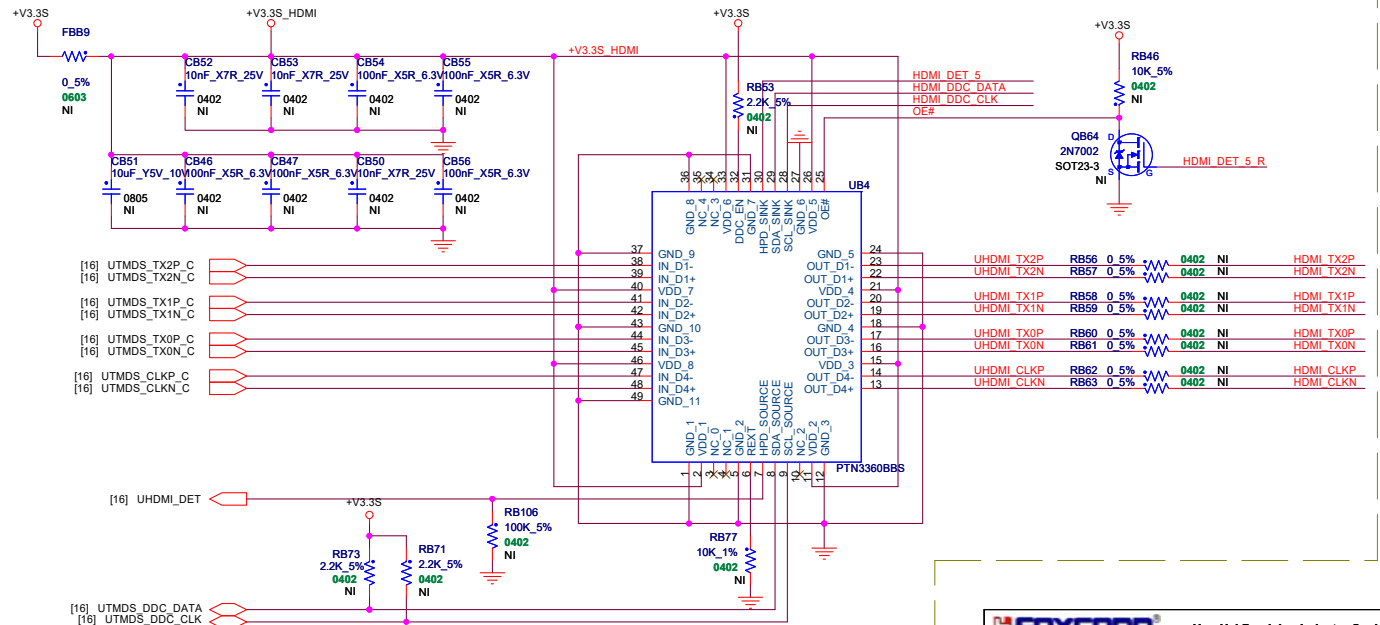




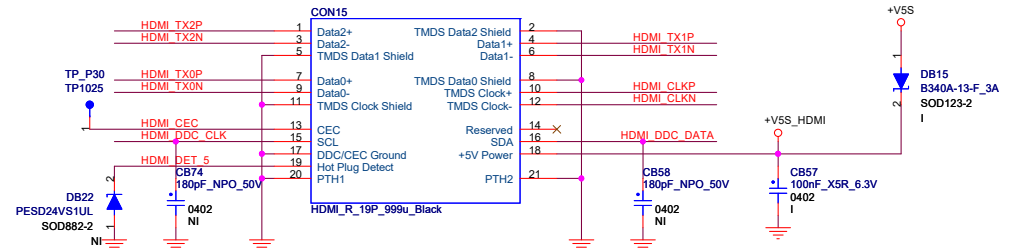
Discrete GPU: Install  
UMA: Not Install



Discrete GPU:Not Install  
UMA:Install

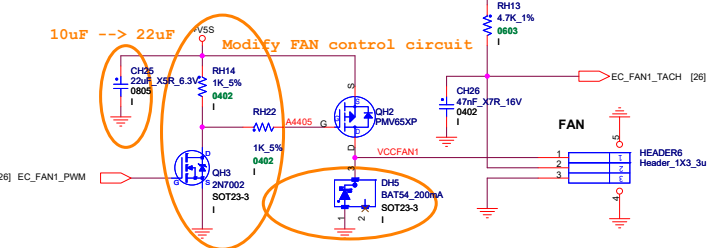


HDMI spec: +5V:4.7V min , 55mA max.

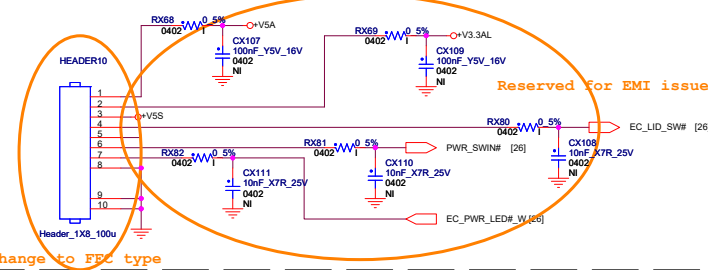




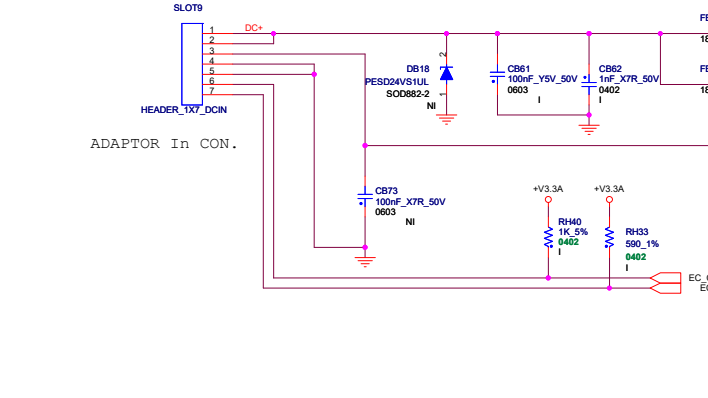
## FAN CONNECTOR



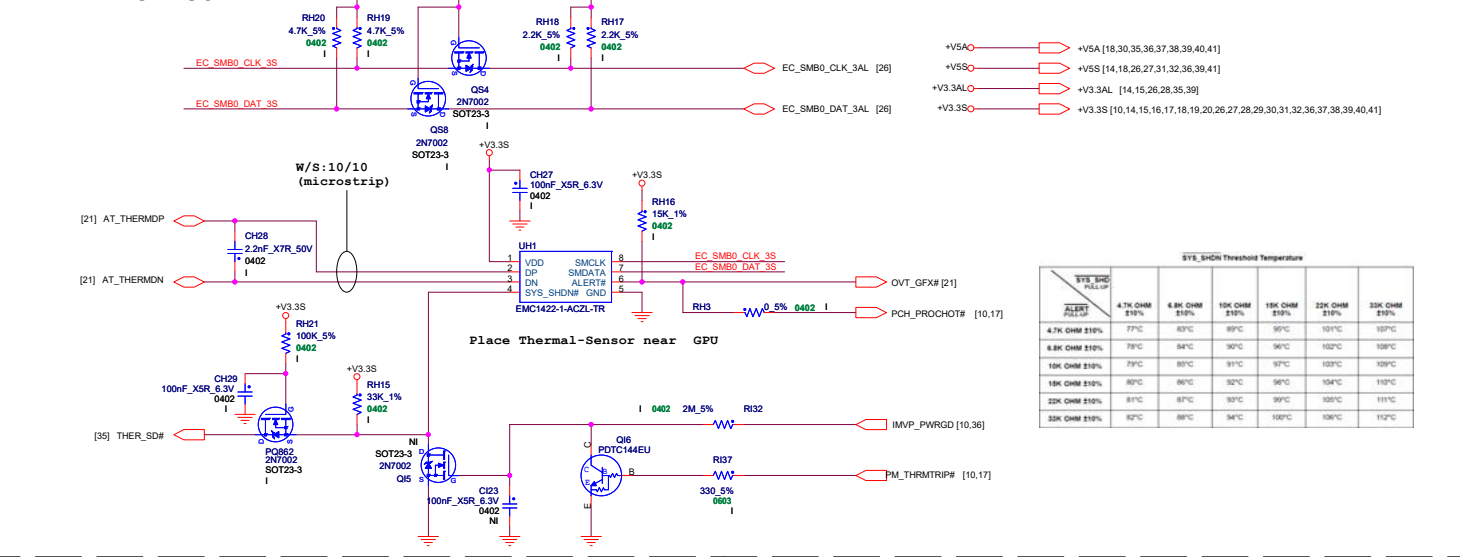
## POWER BUTTON BOARD CONNECTOR



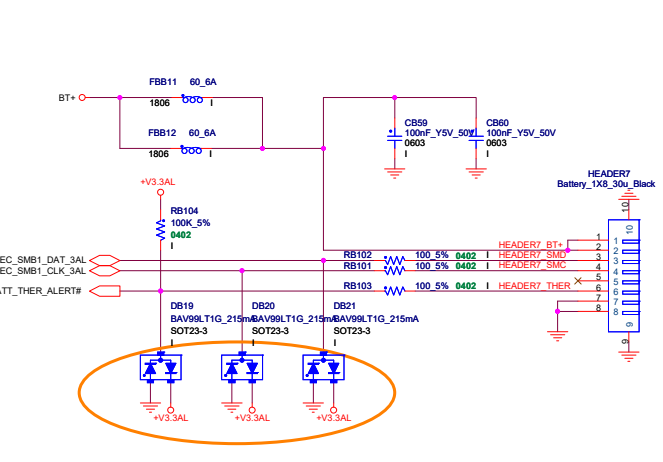
DC\_JACK  
Wire to Board  
CONNECTOR



## THERMAL SENSOR

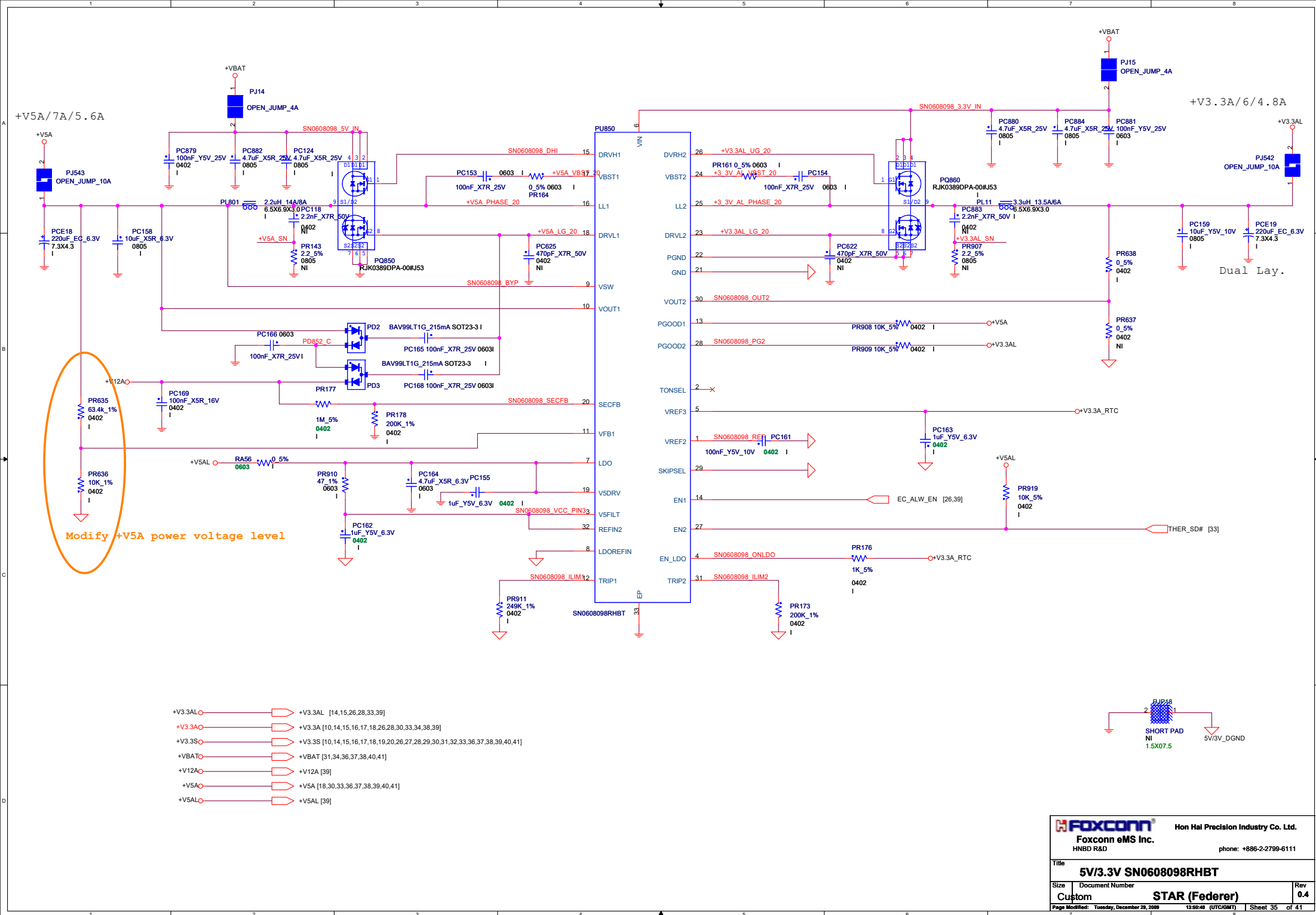


## BATTERY CONNECTOR



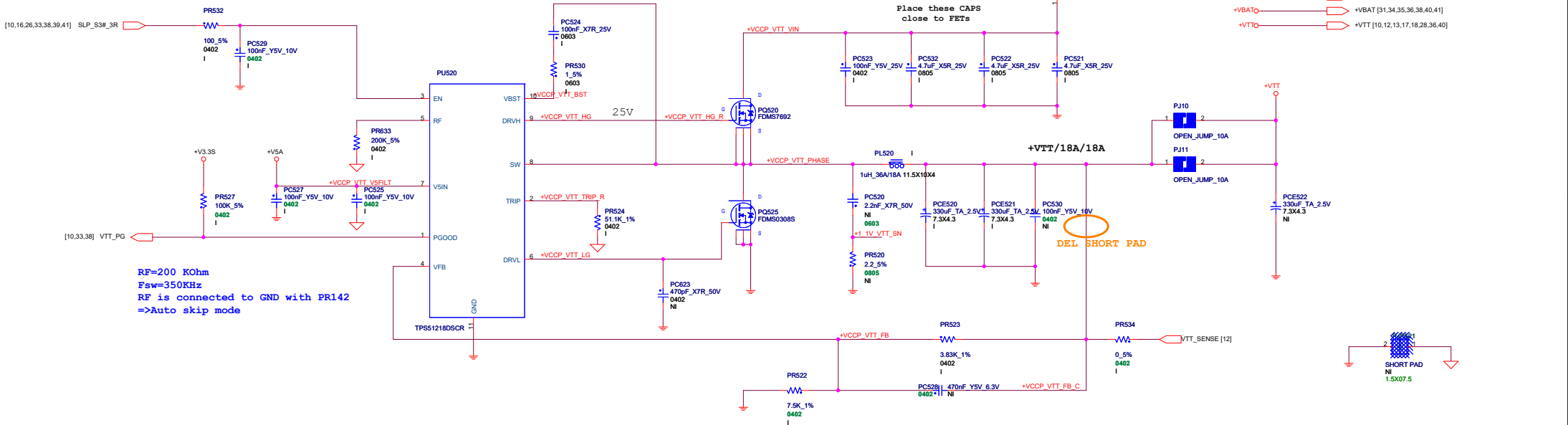
Pin No.	Symbol	Comments
1	BATT+	Batt+, Battery Positive Terminal
2	BATT+	Batt+, Battery Positive Terminal
3	SMD	SMbus data interface I/O pin.
4	SMC	SMbus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal



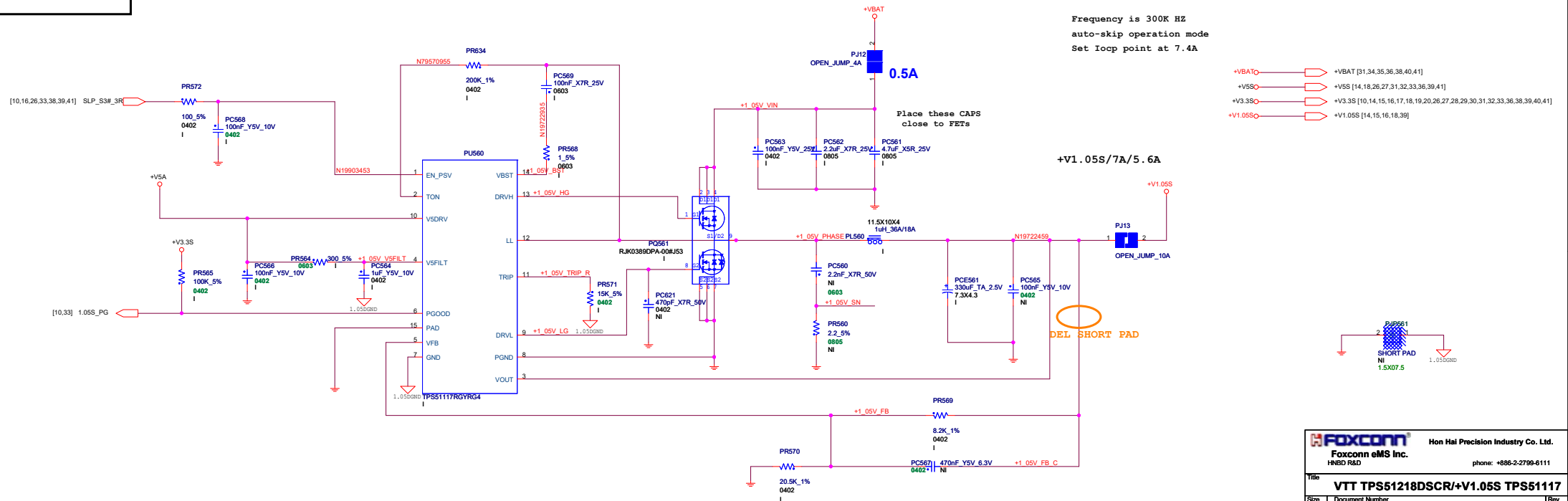




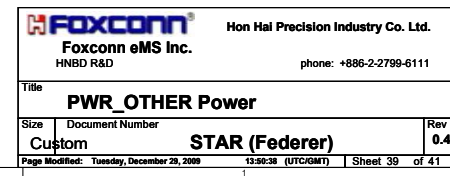
## +VTT TPS51218



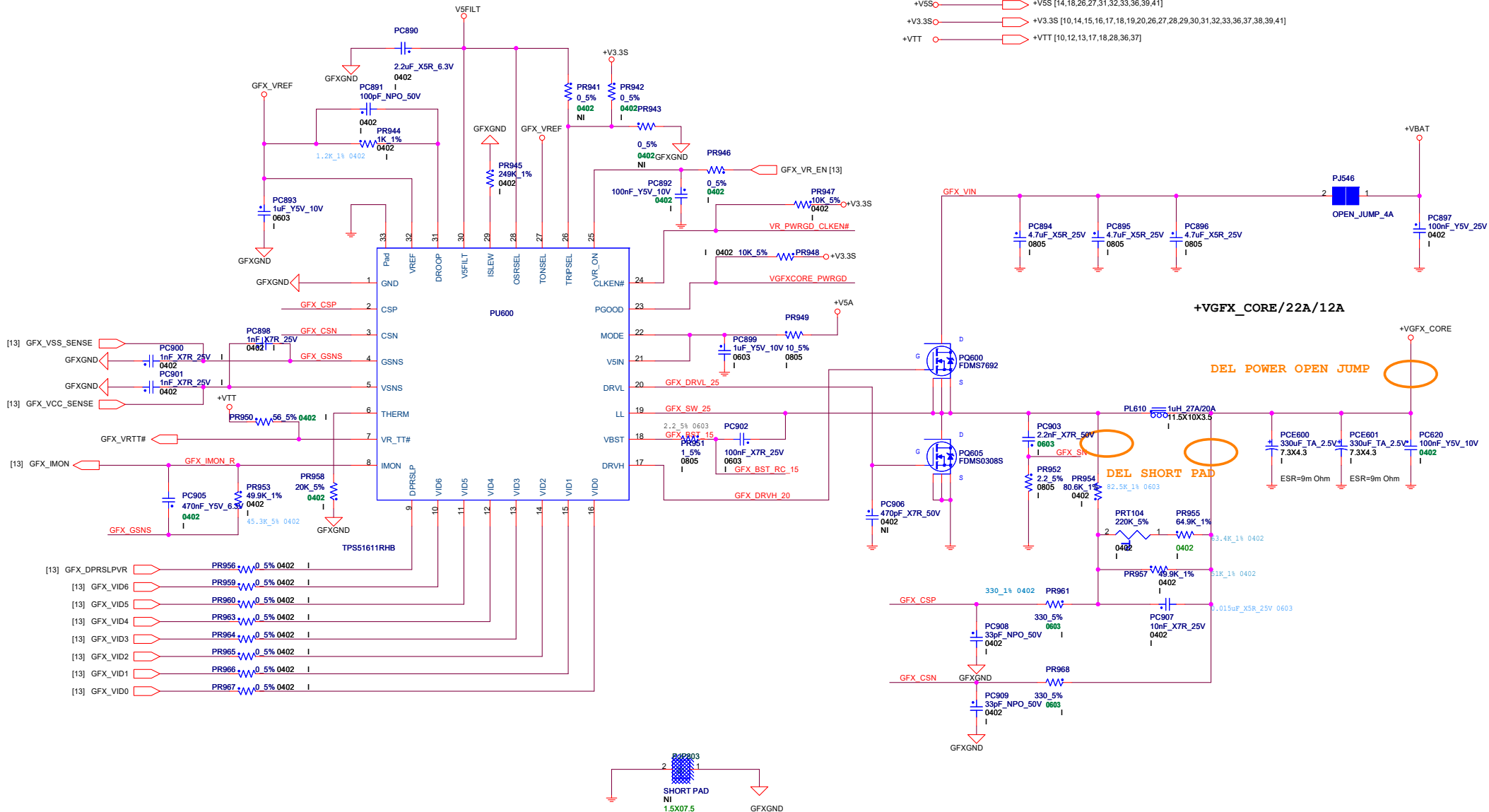
## +V1.05S TPS51117



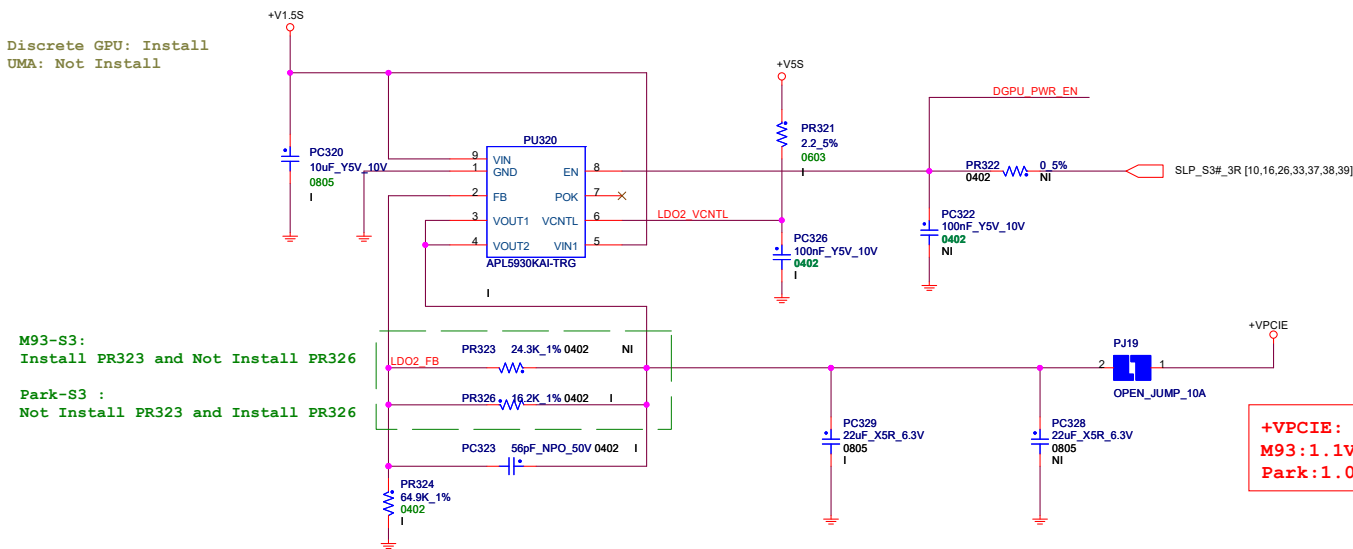
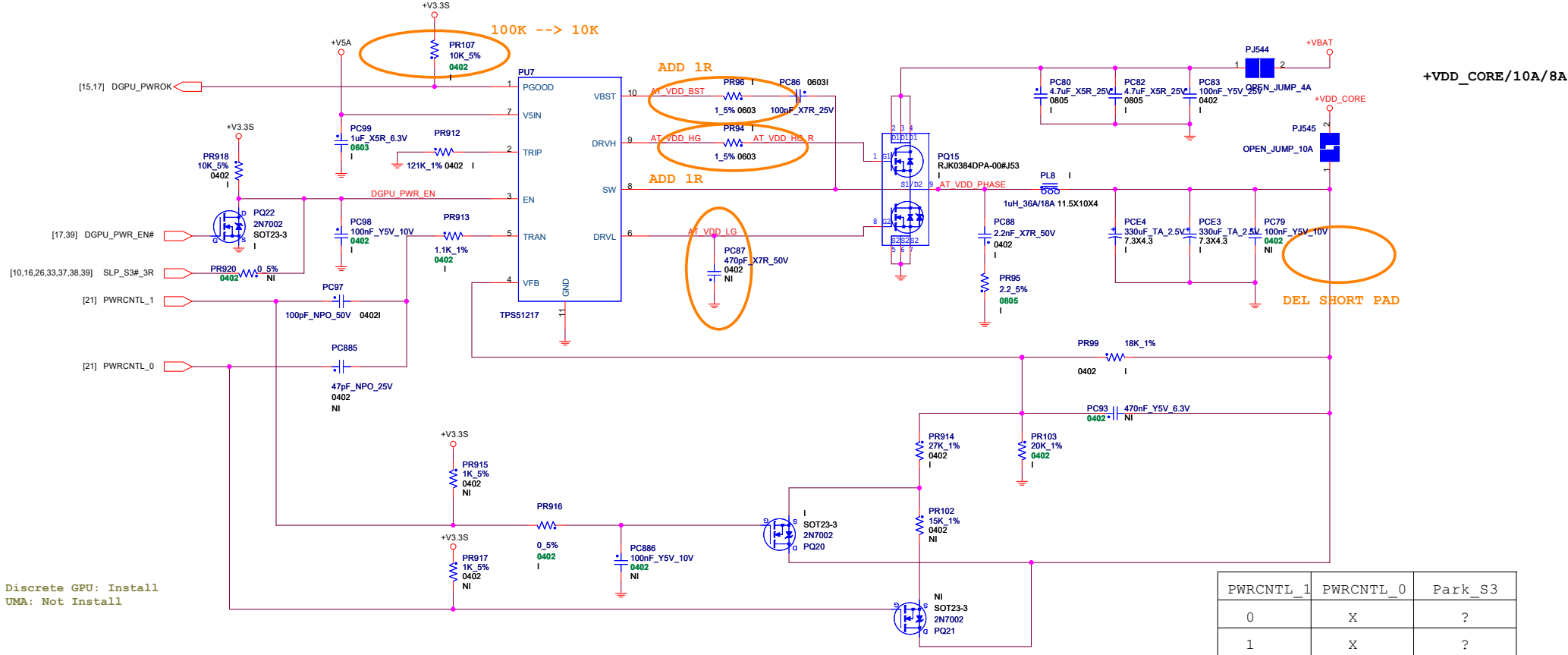




+VGFXCORE







+VBAT	+VBAT [31,34,35,36,37,38,40]
+V5A	+V5A [18,30,33,35,36,37,38,39,40]
+V5S	+V5S [14,18,26,27,31,32,33,36,39]
+V3.3S	+V3.3S [10,14,15,16,17,18,19,20,26,27,28,29,30,31,32,33,36,37,38,39,40]
+V1.5S	+V1.5S [22,24,25,39]
+VDD_CORE	+VDD_CORE [24]
+VPCIE	+VPCIE [20,21,23,24]