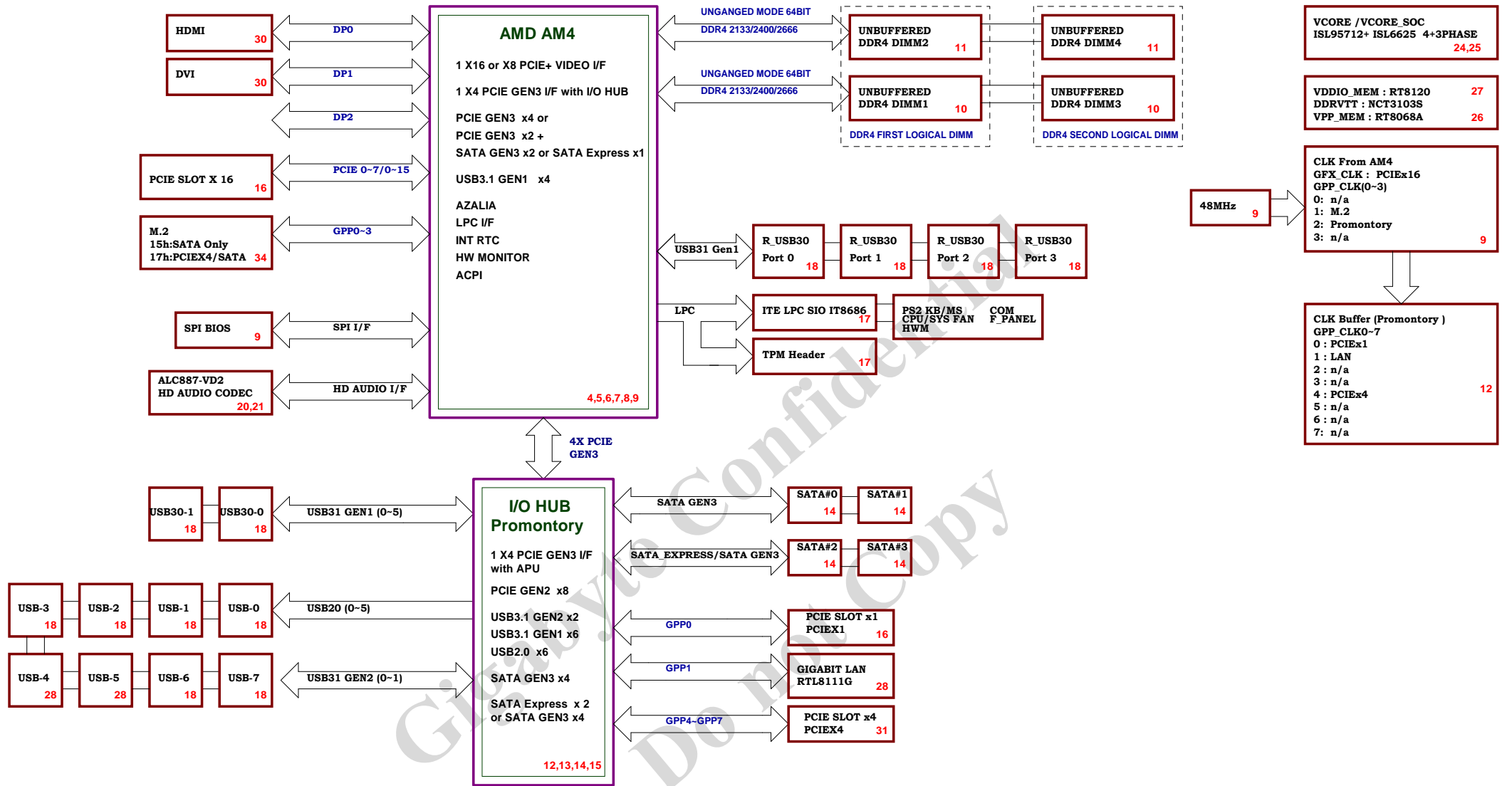
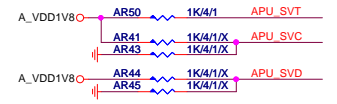
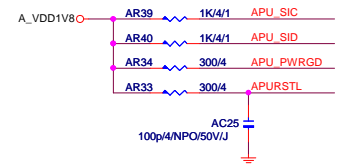
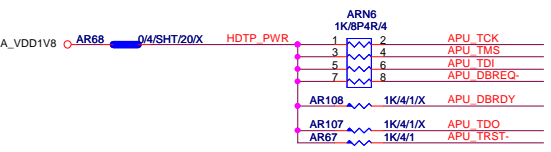
			
Title			
BOM & PCB HISTORY			
Size	Document Number		Rev
Custom	B450M DS3H		1.01
Date:	Monday, October 01, 2018	Sheet	2 of 35



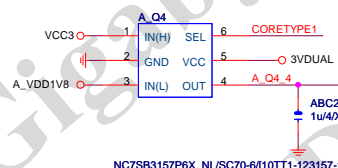
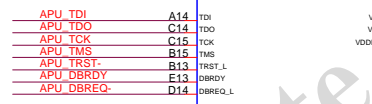


SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

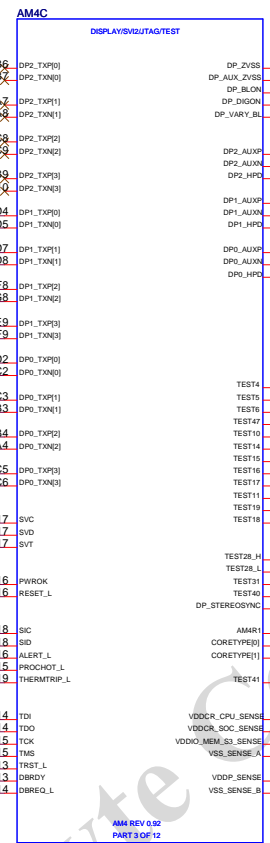


DVI

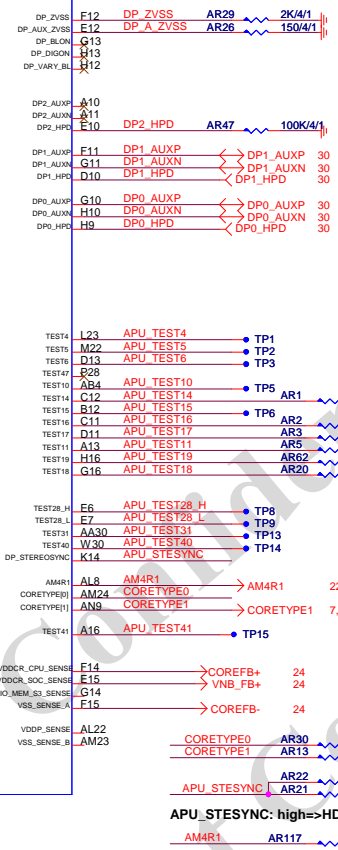
HDMI



NC7SB3157P6X_NL/SC70-6[10T11-123157-10R]



Placed within 1500 mils from APU



THERMTRIP- AR36 0/4/SHT/20/X THERMTRIP0 THERMTRIP0 17

CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h- 6 Fh	TYPE 0
0	1	Reserved	TYPE 1
1 ST	0	Family 17 h / Models 00 h- 0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h- 1 Fh	TYPE 3

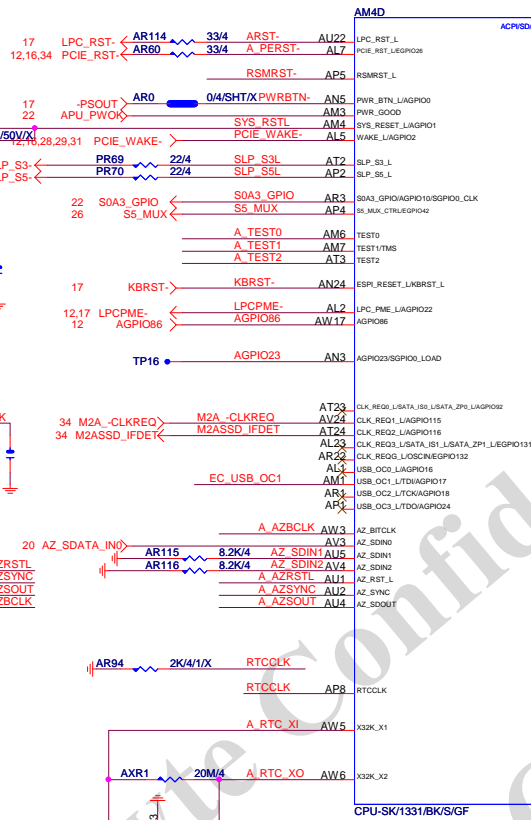
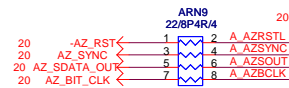
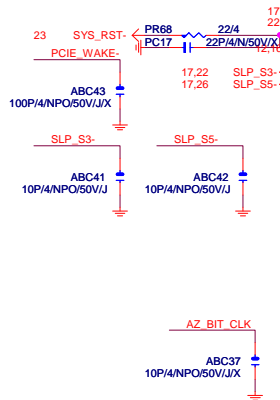
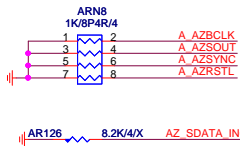
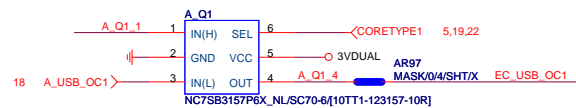
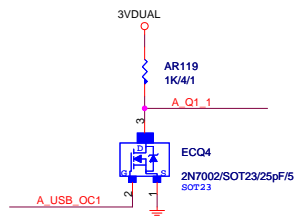
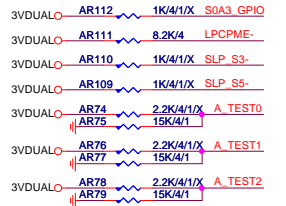
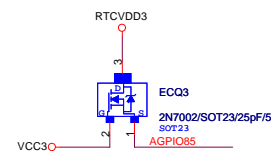
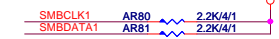
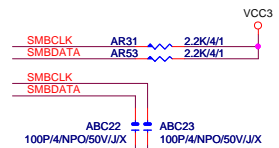
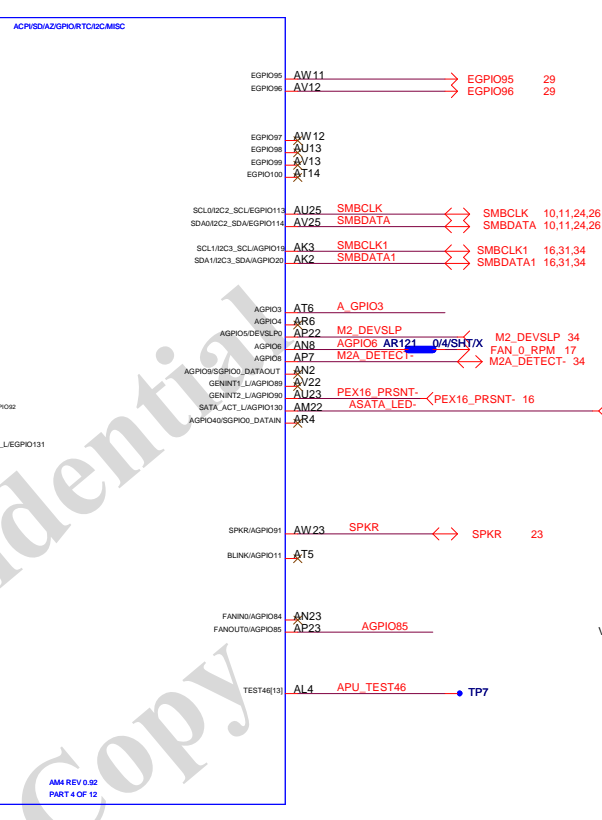
GIGABYTE™

TitleCPU DDI, CONTROL

SizeCustomDocument NumberB450M DS3HRev1.01

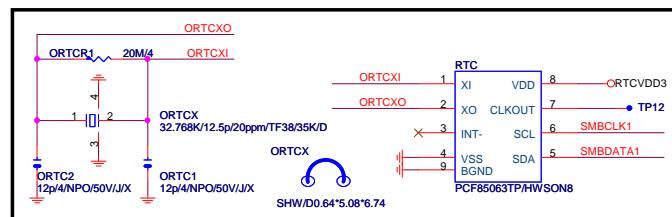
Date:Monday, October 01, 2018Sheet5 of 35

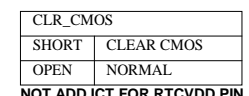
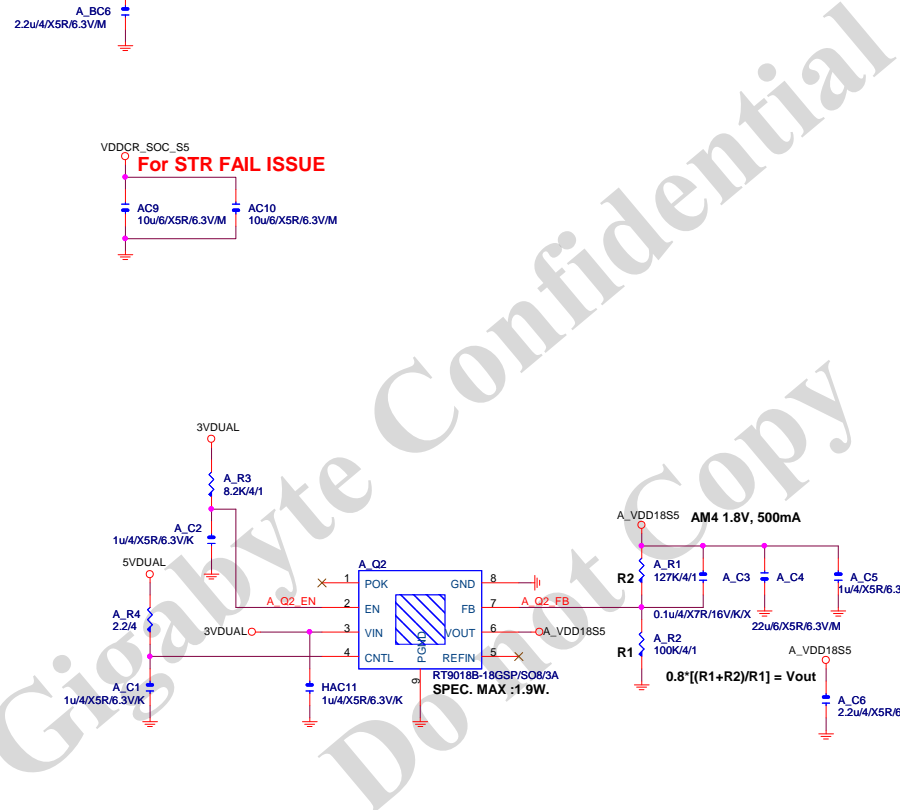
F. PANEL 已 PU

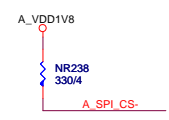
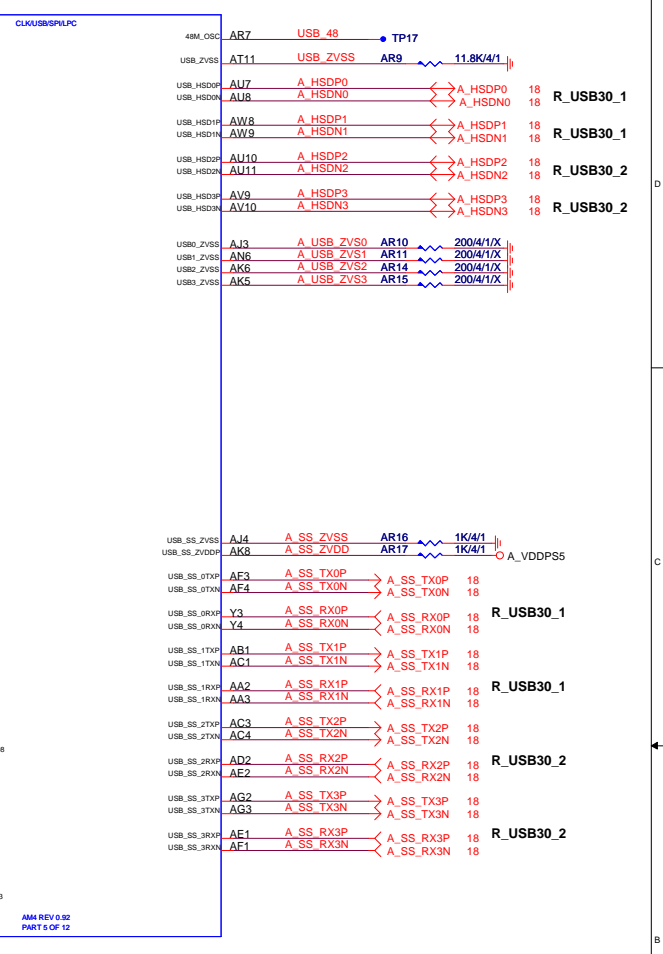
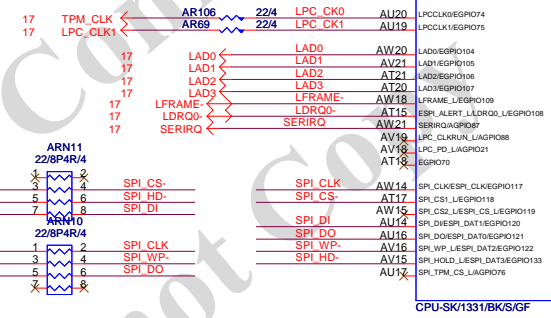
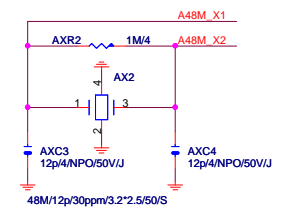
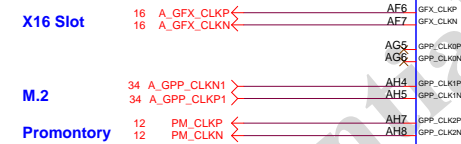
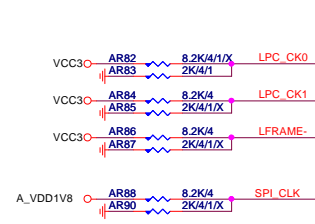
AM4 REV.0.92
PART 4 OF 12

Internal Debug Only

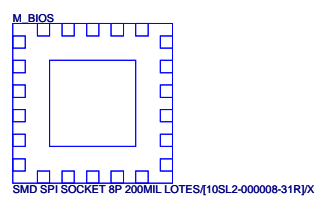
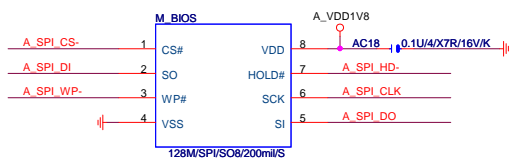
TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



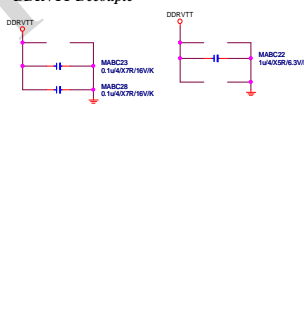
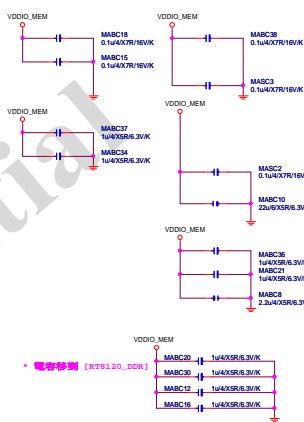
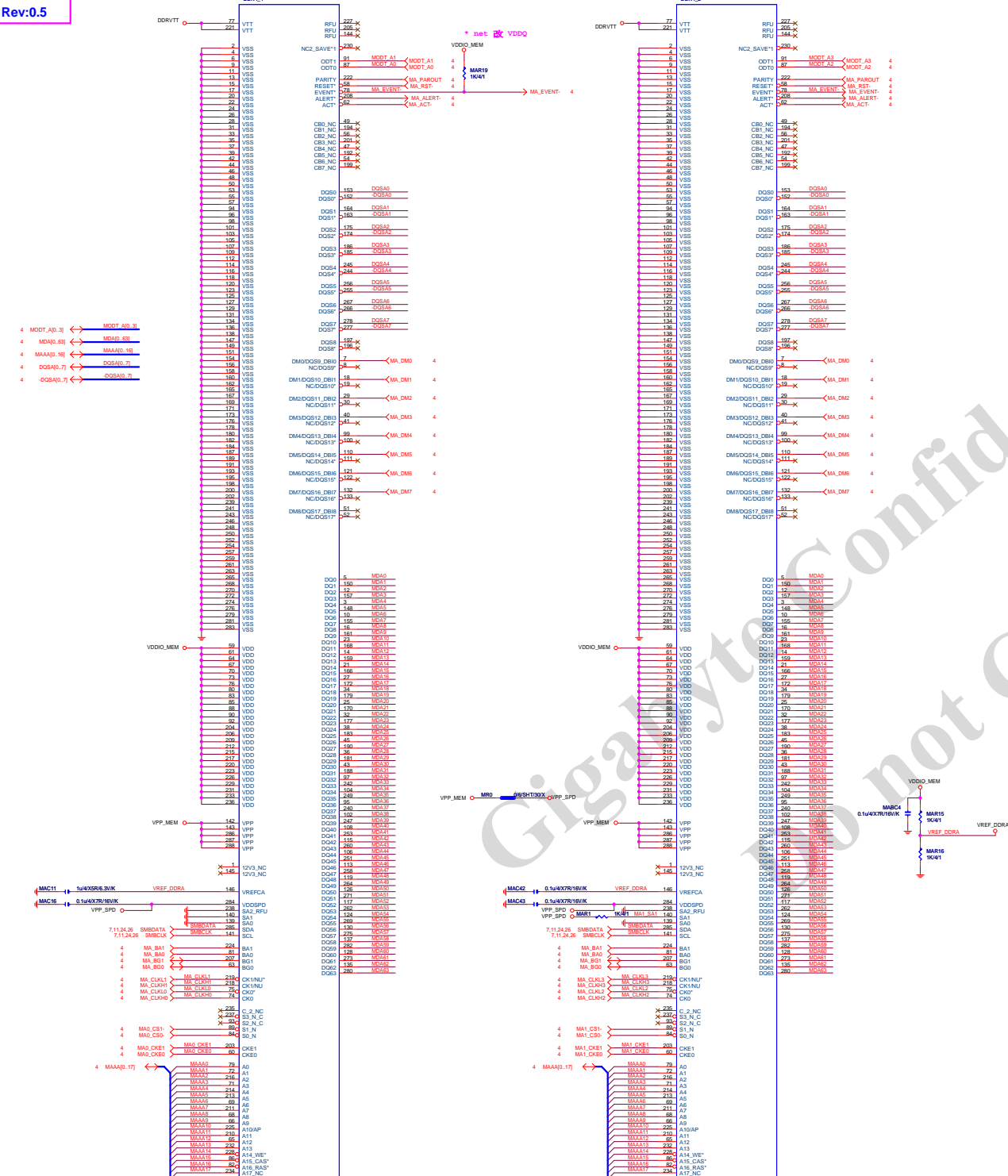


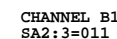
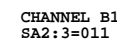


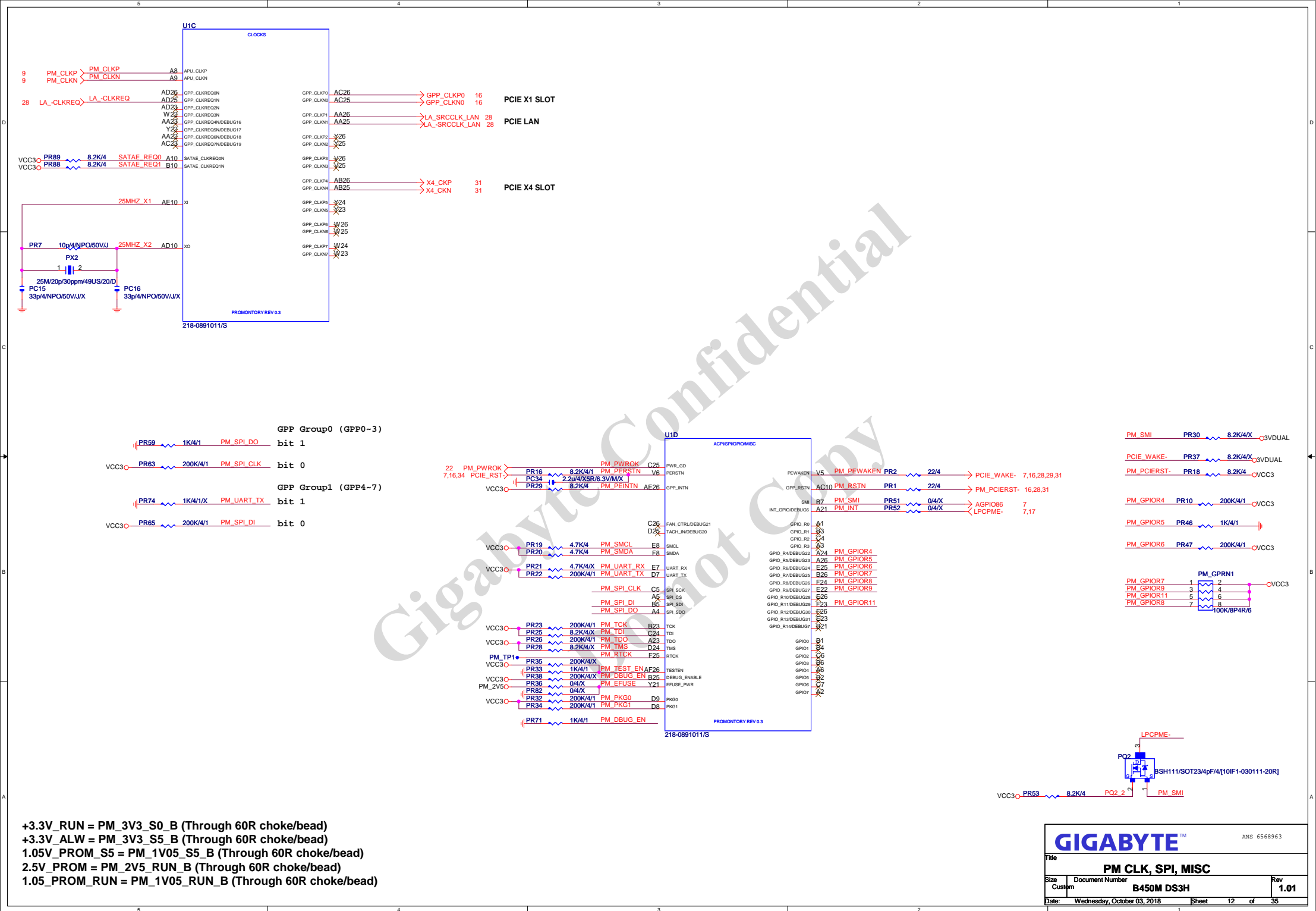
128Mb: 128M/SPI/SO8/200mil/S
256Mb: 256M/WSON8/200MIL/S
Footprint: IC8WSON-BIOS-COLAY



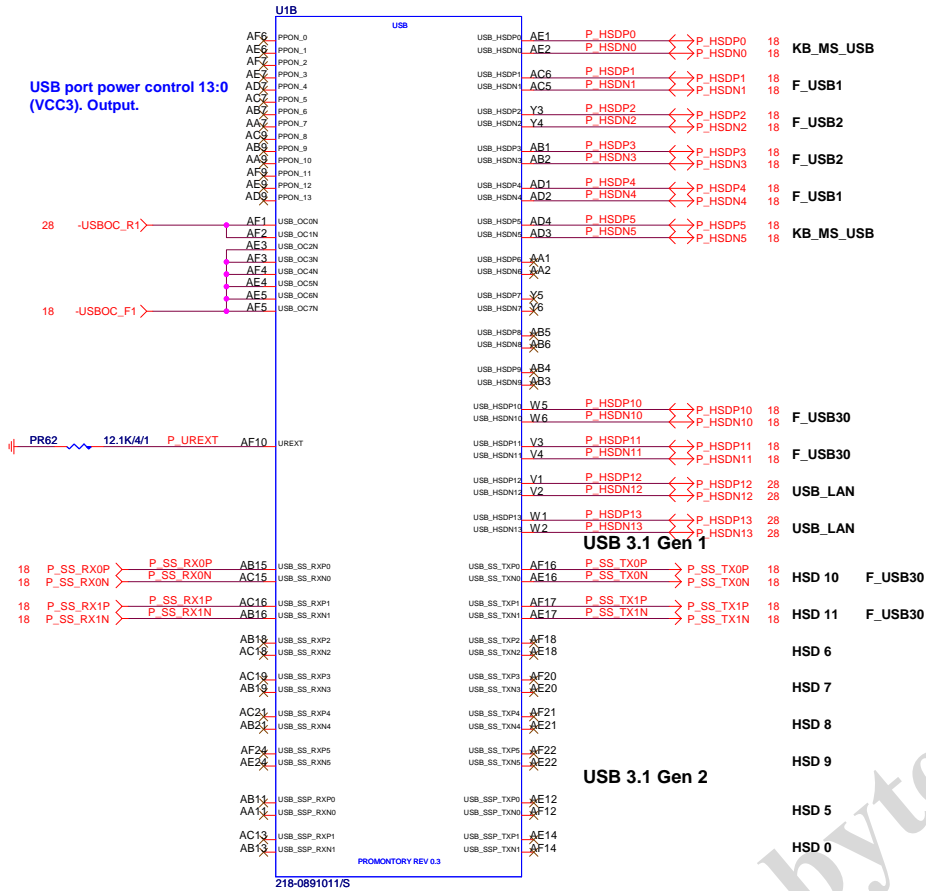
GIGABYTE™
Title **CPU USB3, SPI**
Size Custom Document Number **B450M DS3H** Rev **1.01**
Date: Wednesday, August 29, 2018 Sheet 9 of 35





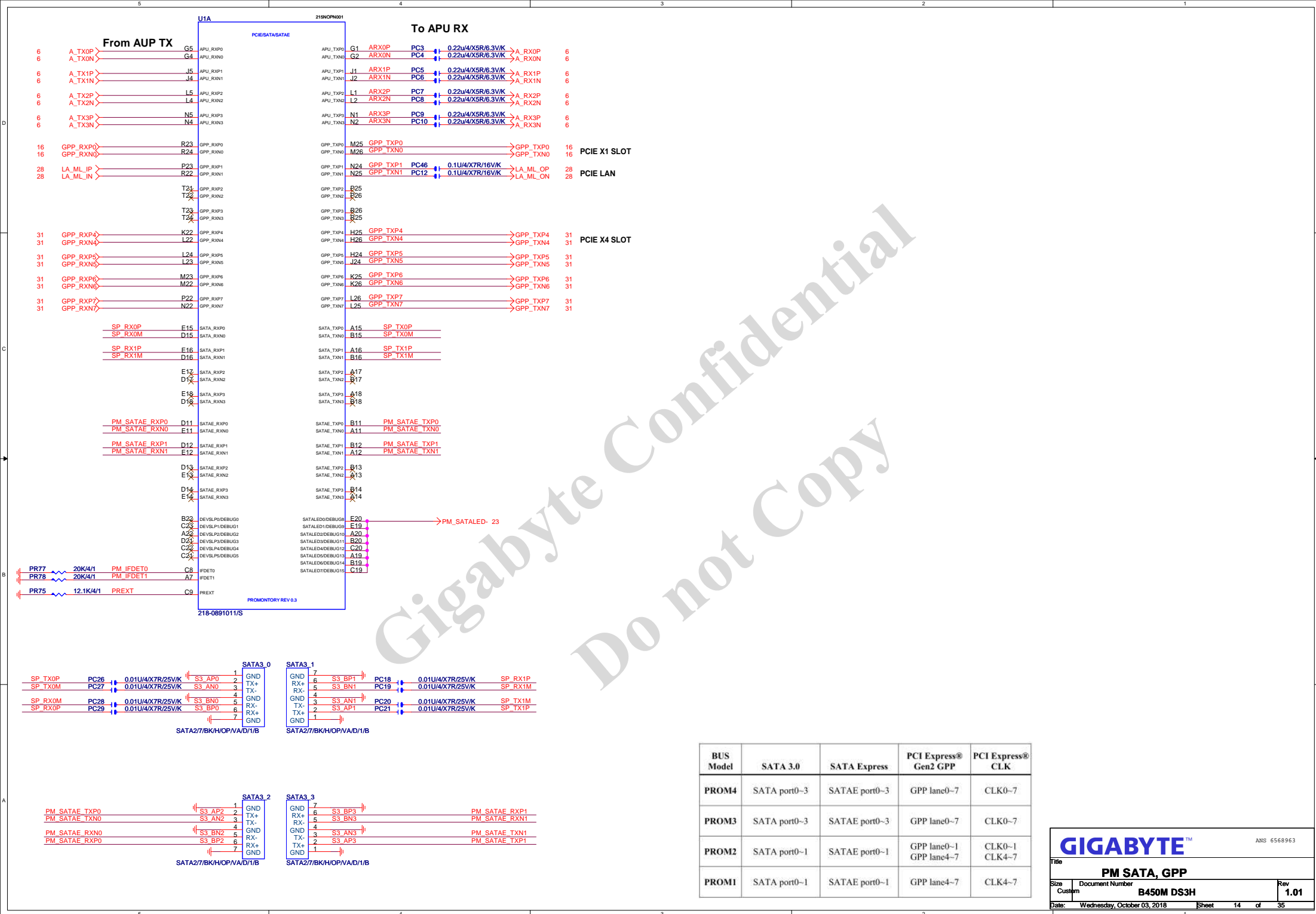


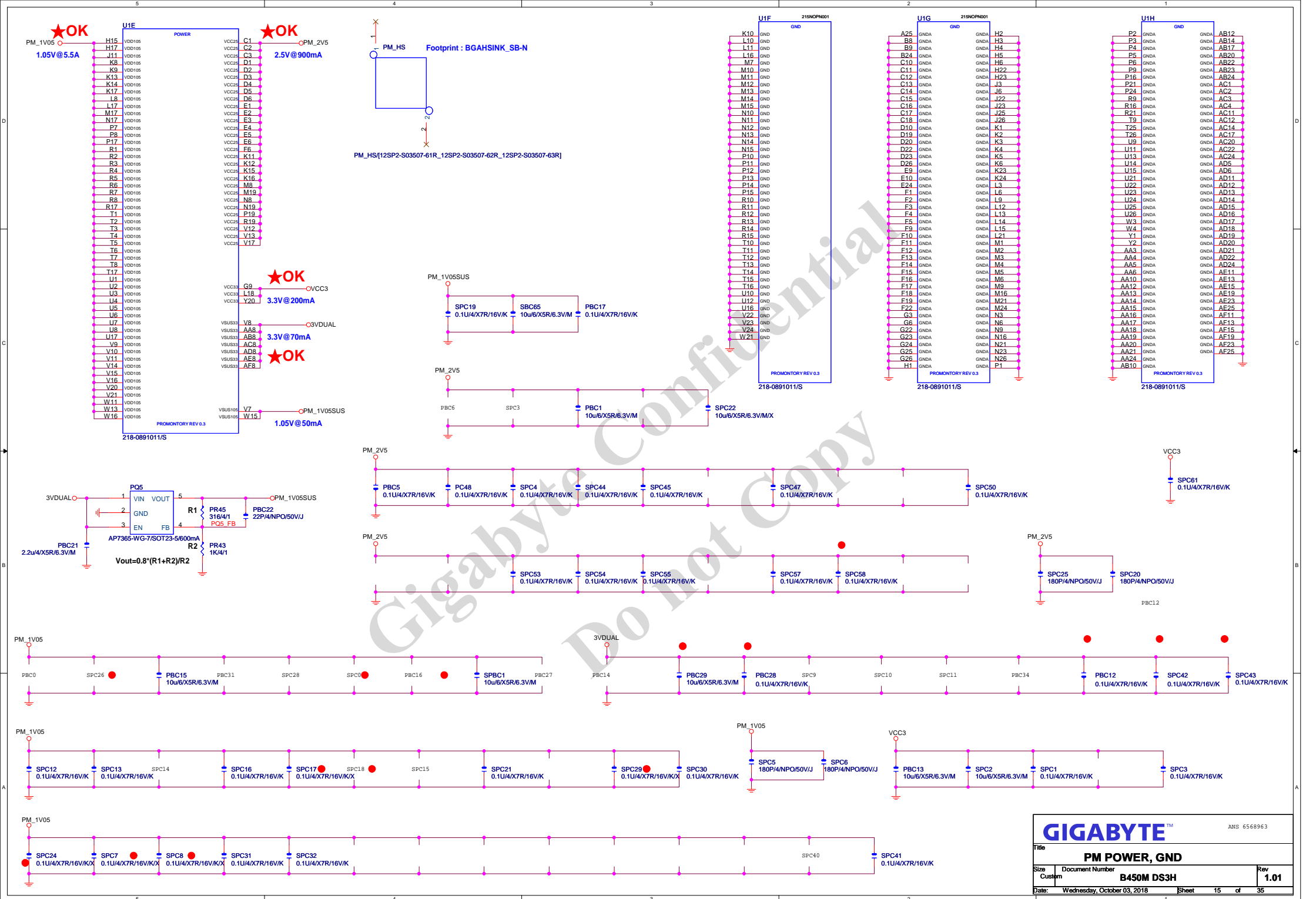
USB port power control 13:0
(VCC3). Output.

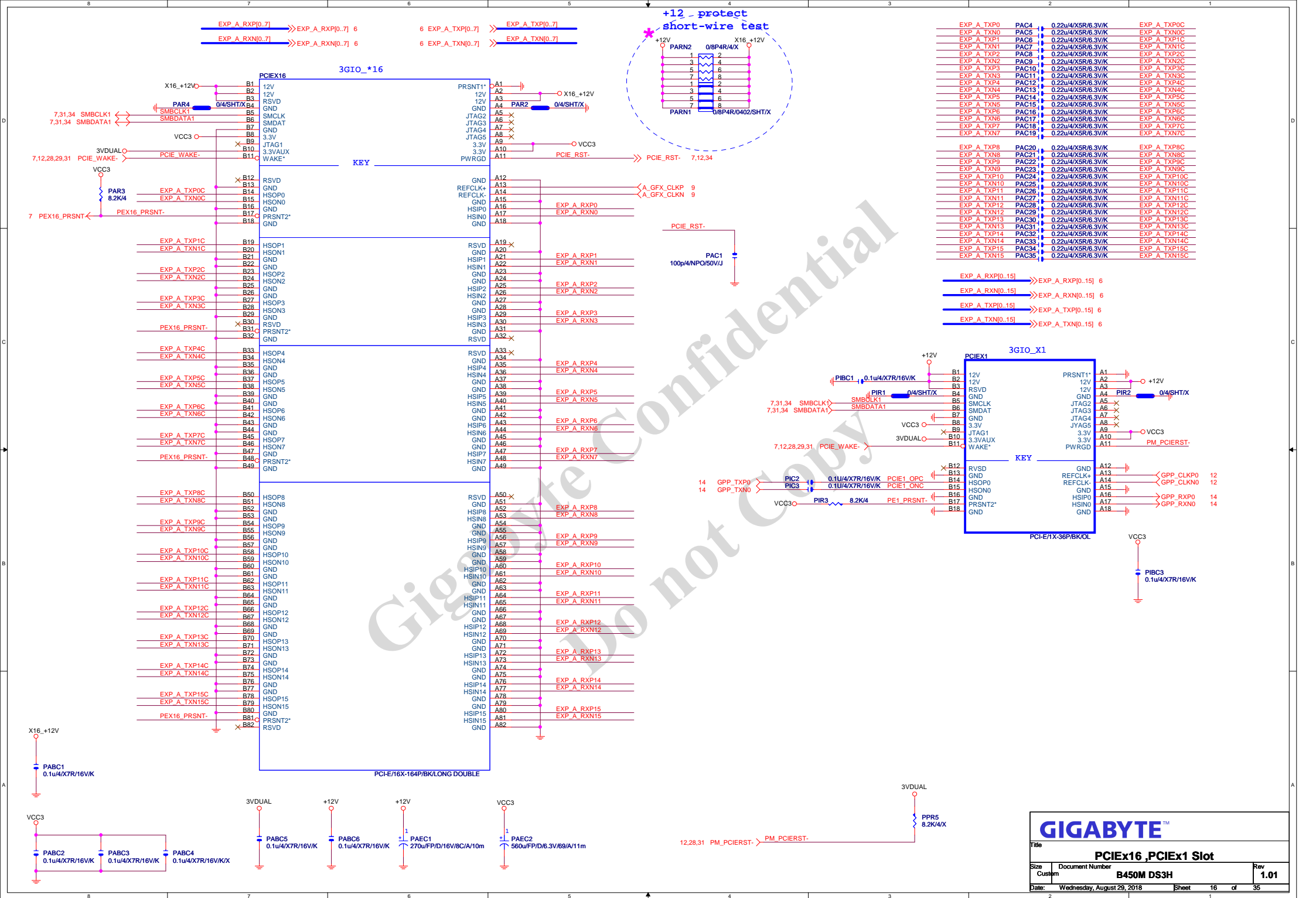


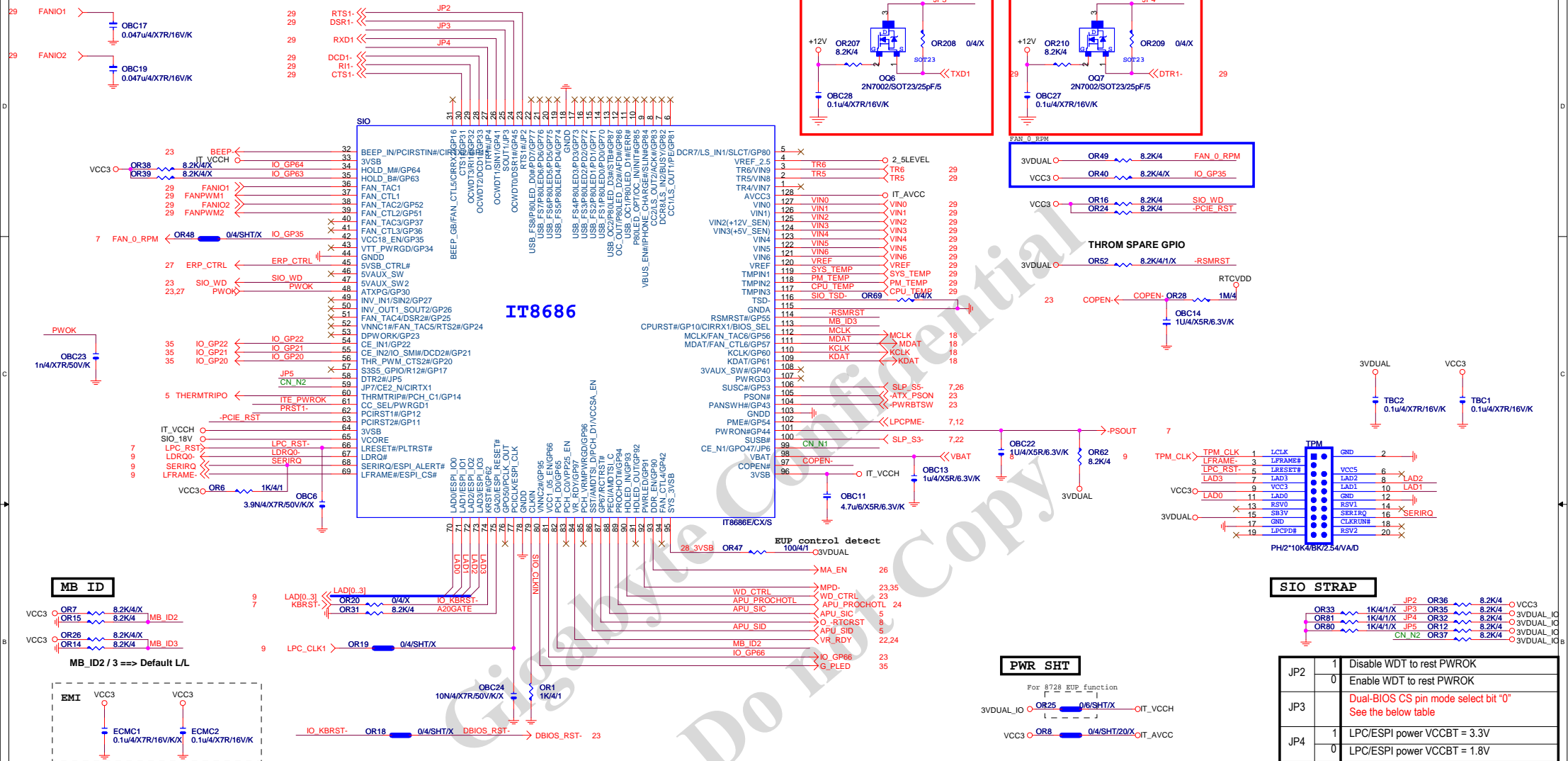
USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[11]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM3	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0







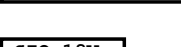


FAN TABLE		
	CPU_FAN	FAN_CTL1 FAN_TAC1
	SYS_FAN1	FAN_CTL2 FAN_TAC2
	SYS_FAN2	FAN_CTL3 FAN_TAC3
	SYS_FAN3	FAN_CTL4 FAN_TAC4
	OPT_FAN OR SYS_FAN4	FAN_CTL5 FAN_TAC5
	THRMTRIP	PIN56
	PROCHOT	PIN89

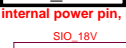
DUAL BIOS OPT STRAP



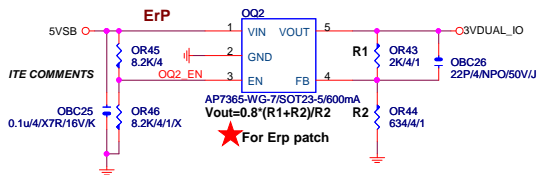
Power leakage



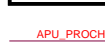
SIO_18V



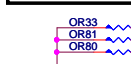
SIO CAP



SIO PU



SIO STRAP

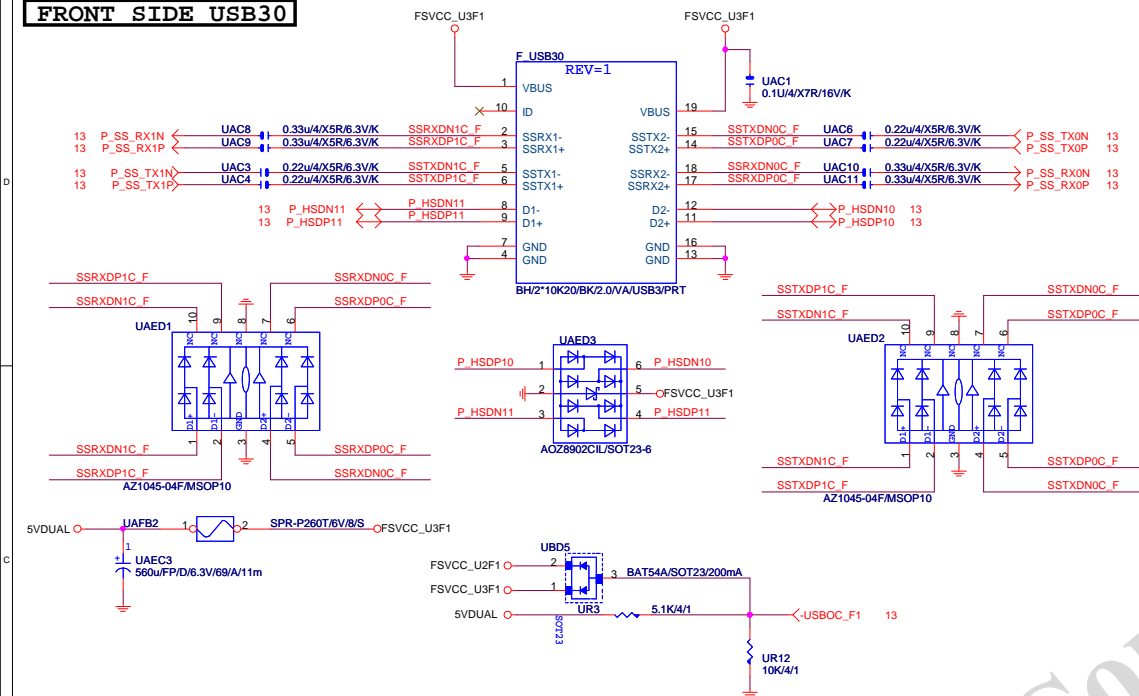


JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
JP3	0 1	CE mode 2
	0 0	CE mode 3

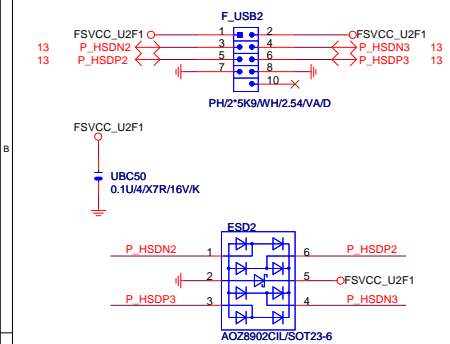
GIGABYTE™

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ITE 8686 LPC IO			
Size	Document Number	Rev	
Custom	B450M DS3H	1.01	
Date:	Wednesday, August 29, 2018	Sheet	17 of 35

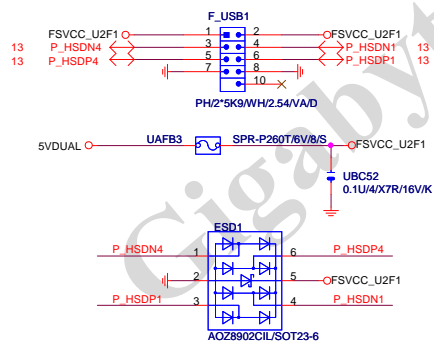
FRONT SIDE USB30



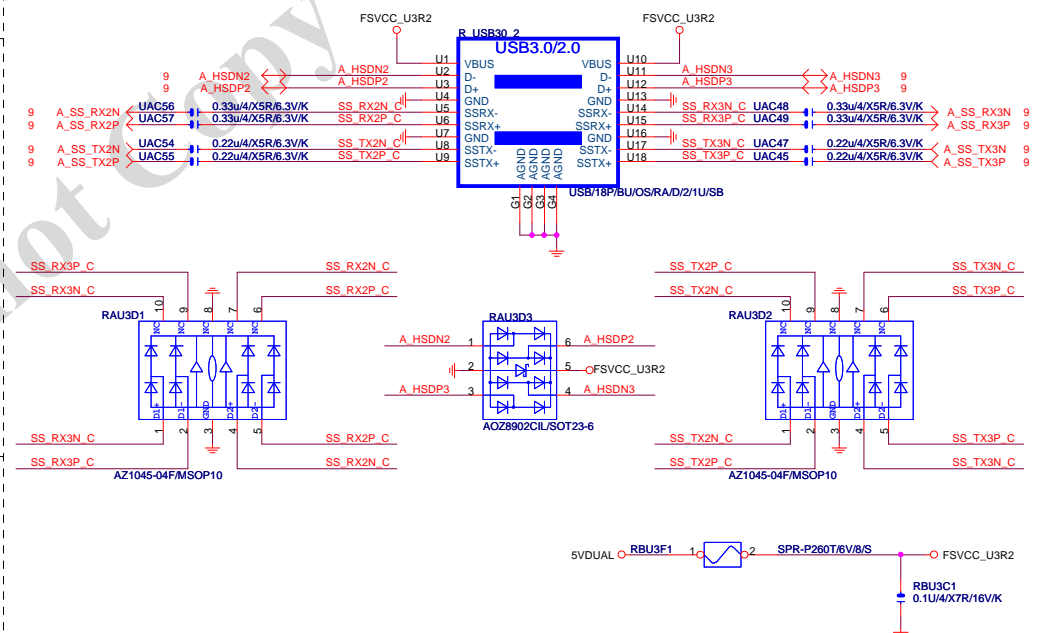
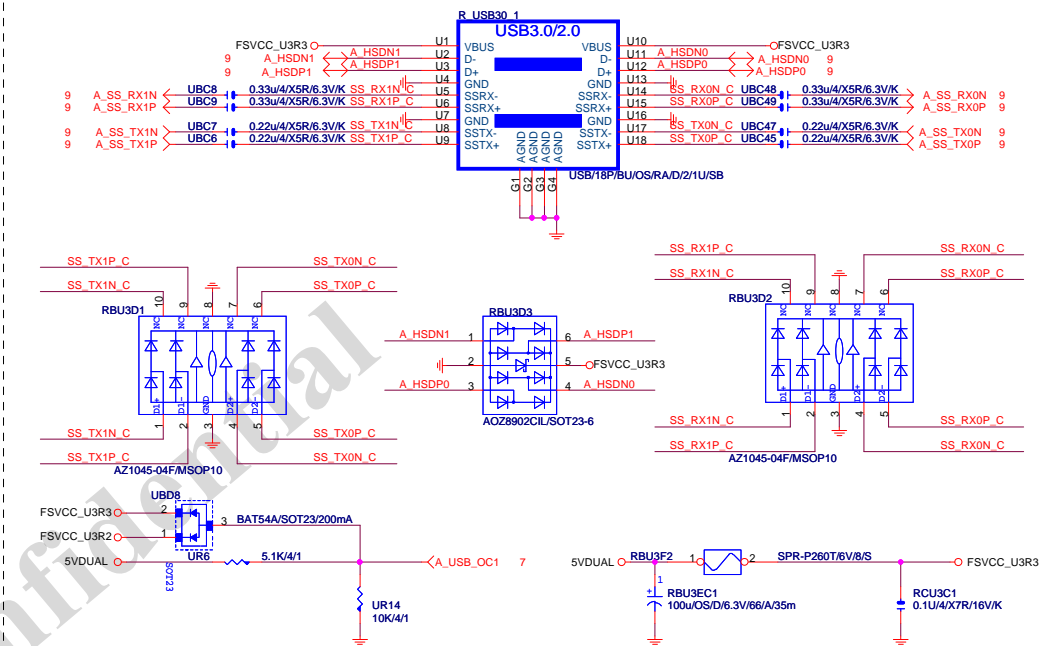
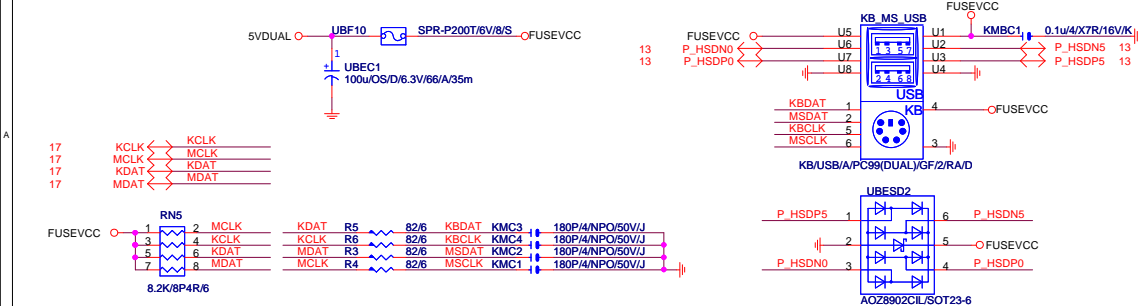
FRONT SIDE USB2



FRONT SIDE USB1



KB/MS & USB



GIGABYTE™

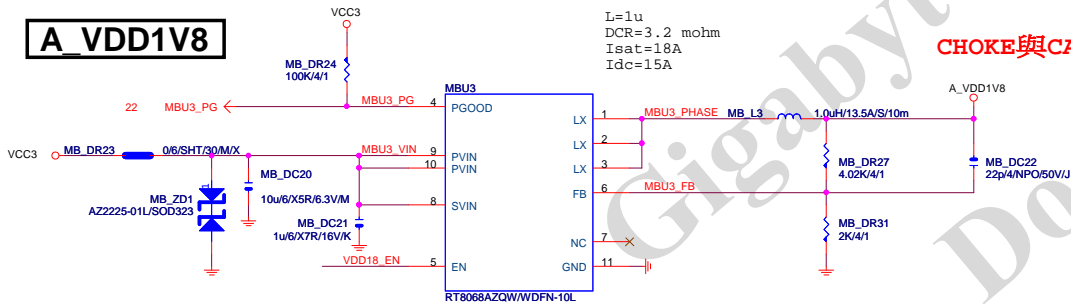
Title	F_USB ,F_USB30 ,R_USB30 , KB_MS_USB
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Size	Document Number	Rev
Custom	B450M DS3H	1.01

Date: Wednesday, August 29, 2018 Sheet 18 of 35

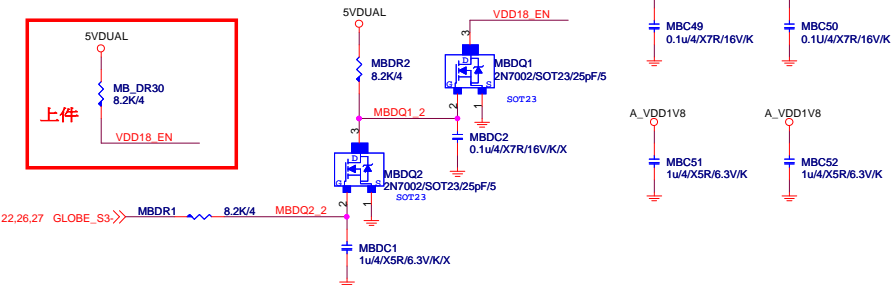
REV:0.4

A_VDD1V8



PWR_SEQ

* 刪 MA_DR32

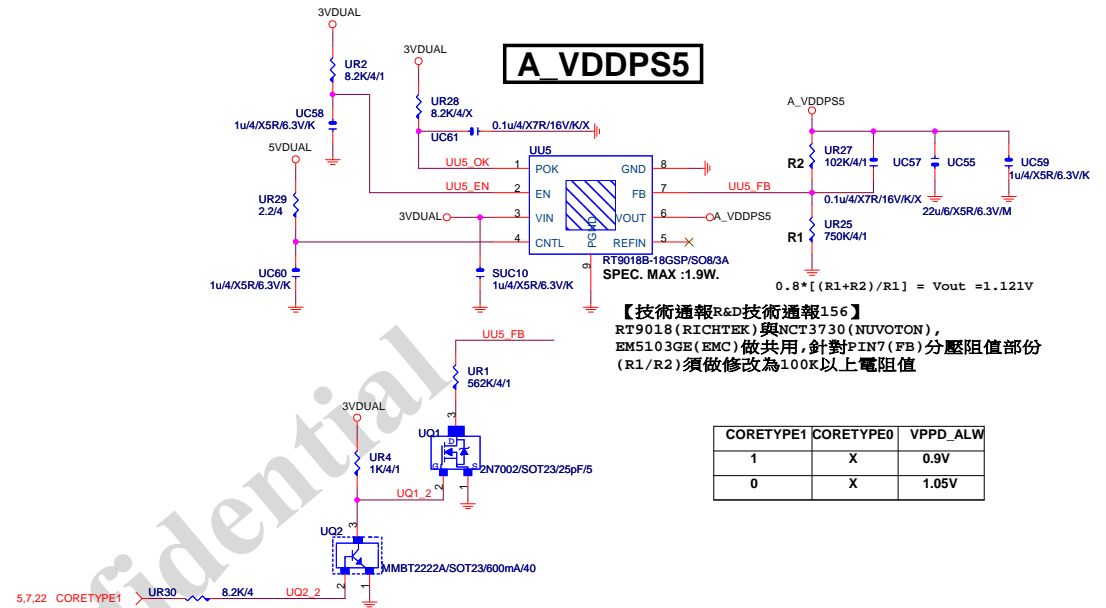


VPP CAP

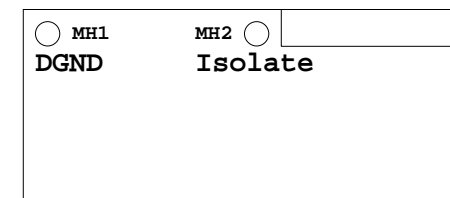
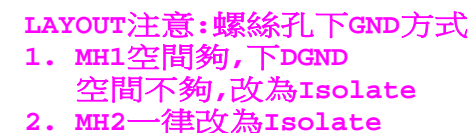
* 大電容 >0

47u*1PCS

A_VDDPS5



CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V




GND切割線

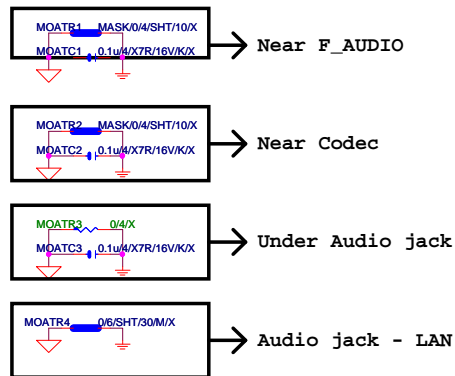


音效區域印刷



				
Title				
ALC887 CODEC				
Size	Document Number			Rev
Custom	B450M DS3H			1.01
Date:	Wednesday, August 29, 2018	Sheet	20	of 35

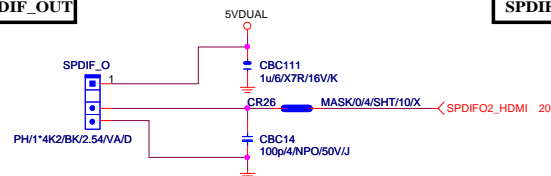
Rev 3.1



*量産前,0ohm改short pad

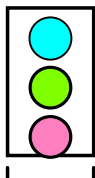
SPDIF_OUT

SPDIF_IN



For HDMI SPDIF (依SPEC保留或移除)

AZALIA JACK

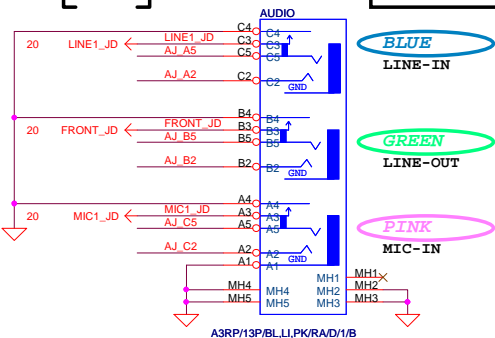


AZALIA JACK

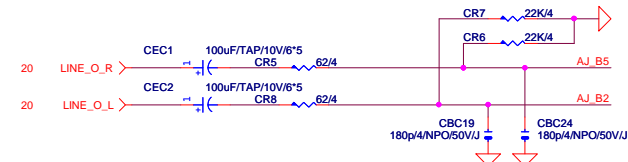
BLUE
LINE-IN

GREEN
LINE-OUT

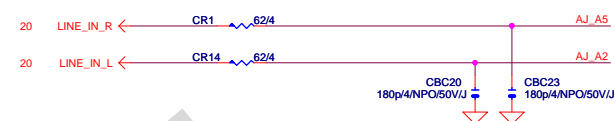
PINK
MIC-IN



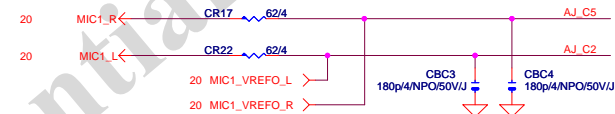
LINE-OUT



LINE-IN



MIC-IN

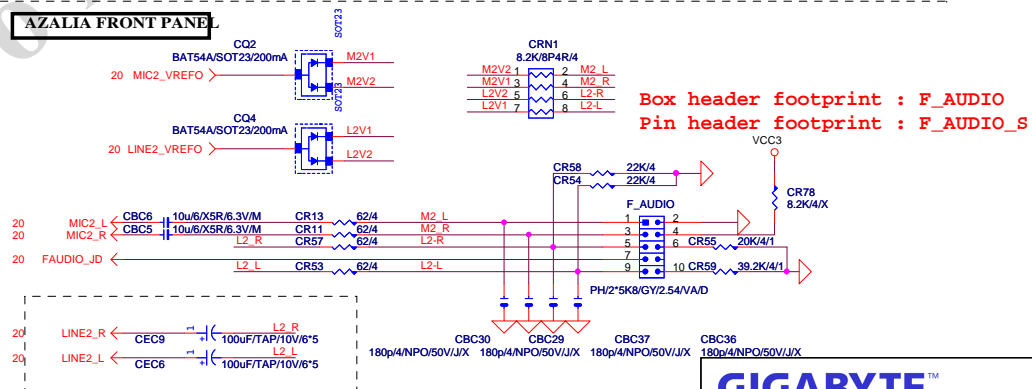


SURROUND

CEN/LFE

SURR BACK

AZALIA FRONT PANEL



Box header footprint : F_AUDIO
Pin header footprint : F_AUDIO_S

GIGABYTE

Title		
AUDIO JACK		
Size	Document Number	Rev
Custom	B450M DS3H	1.01
Date:	Wednesday, August 29, 2018	Sheet 21 of 35

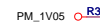


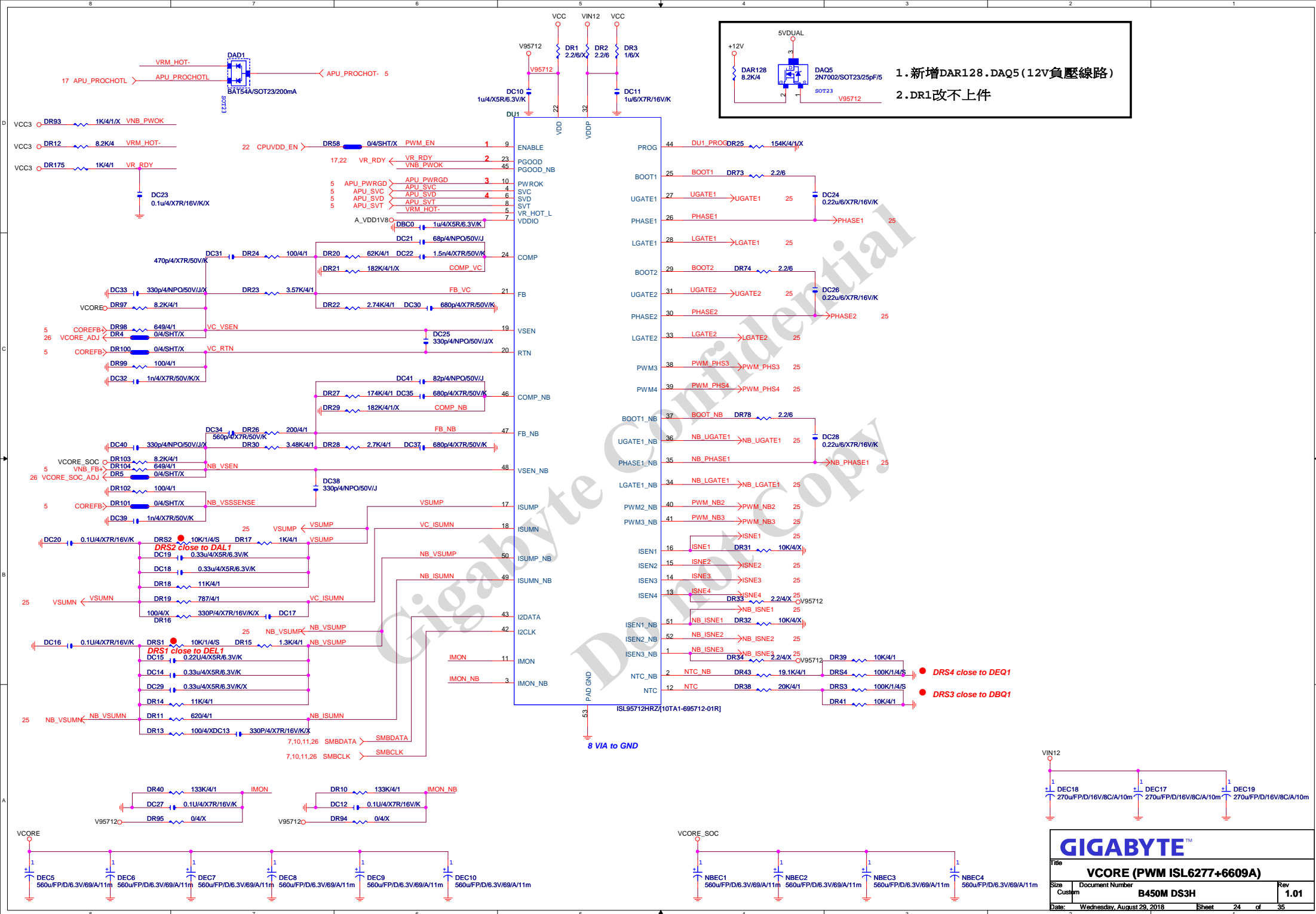
19 MBU3_PG) NPR18 0/4/SHT/X AVDDP_EN

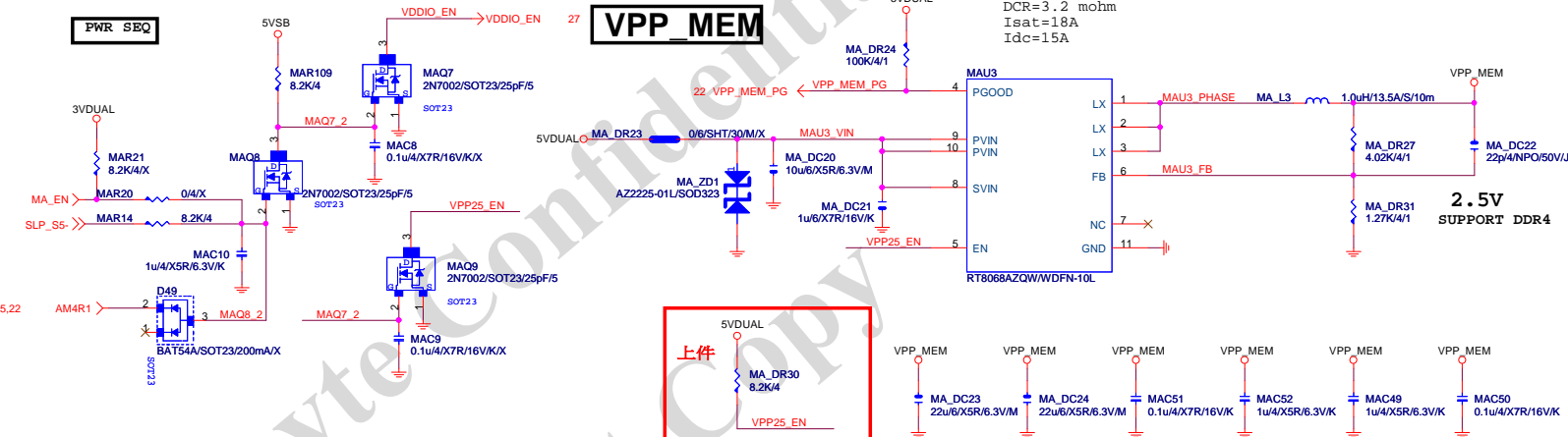
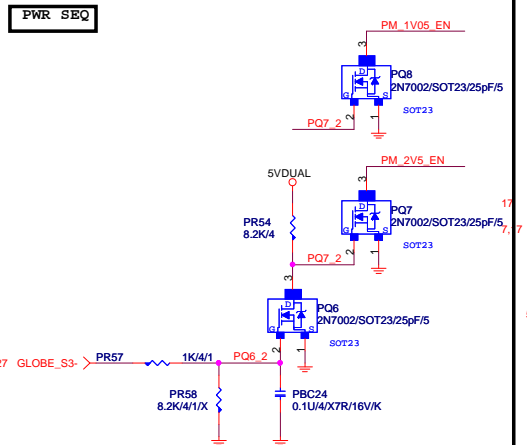
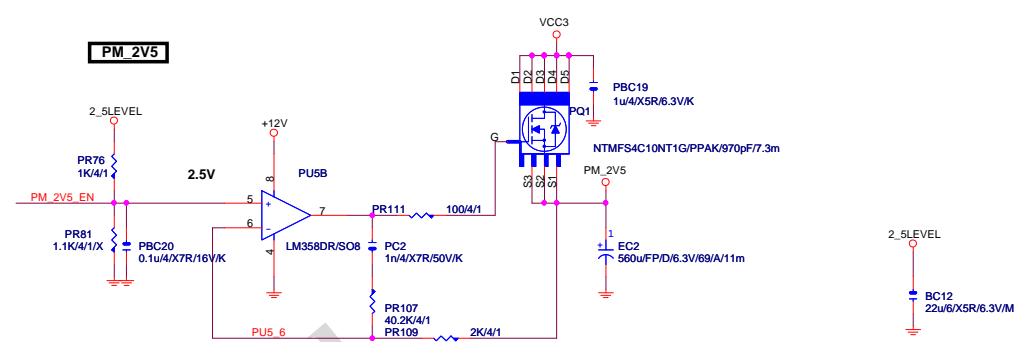
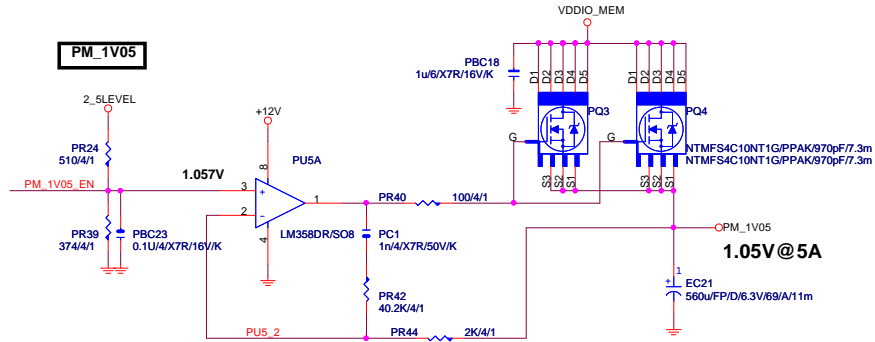


UGATE_A NPR2 2.2/6 G NPQ1

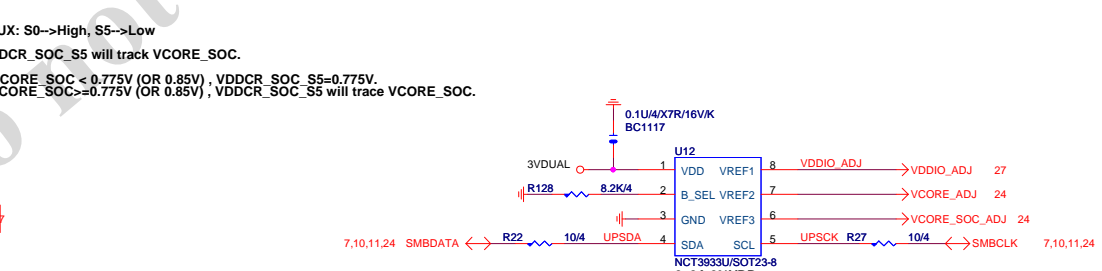
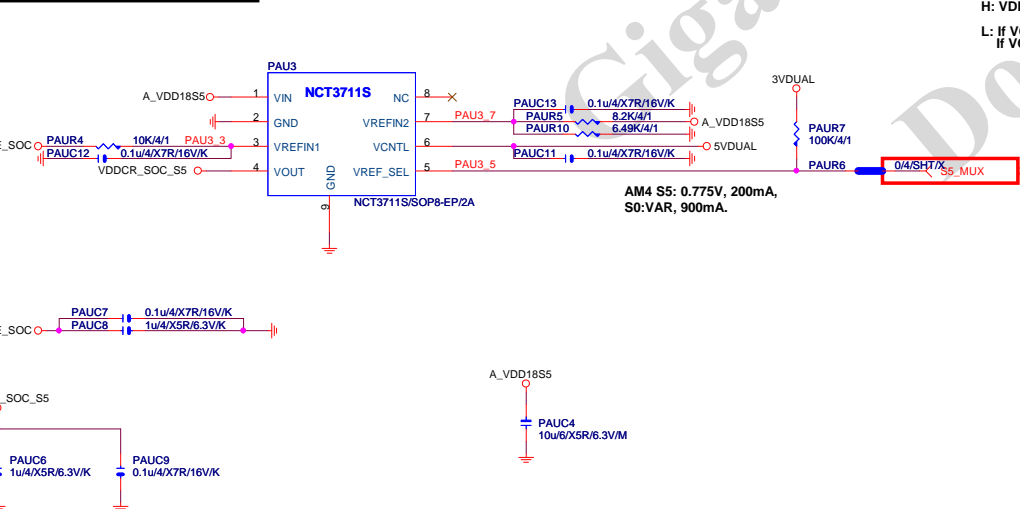
CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

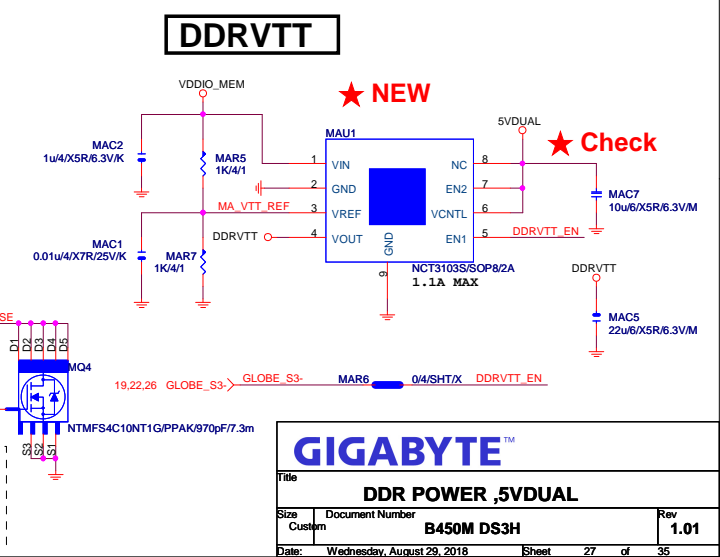
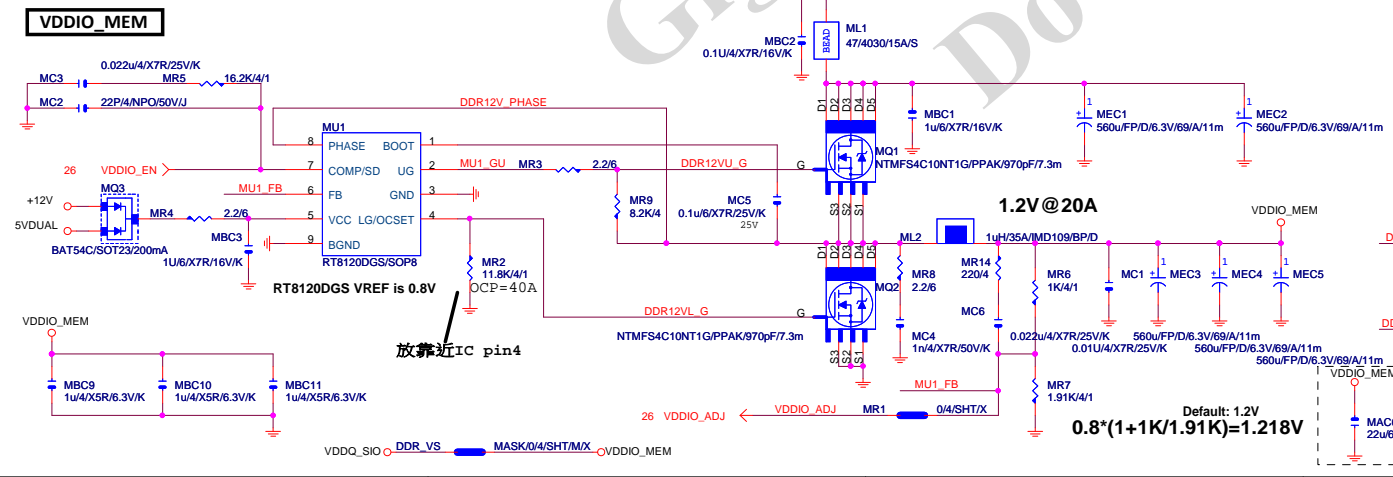
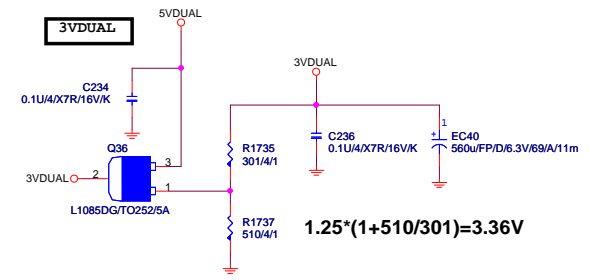
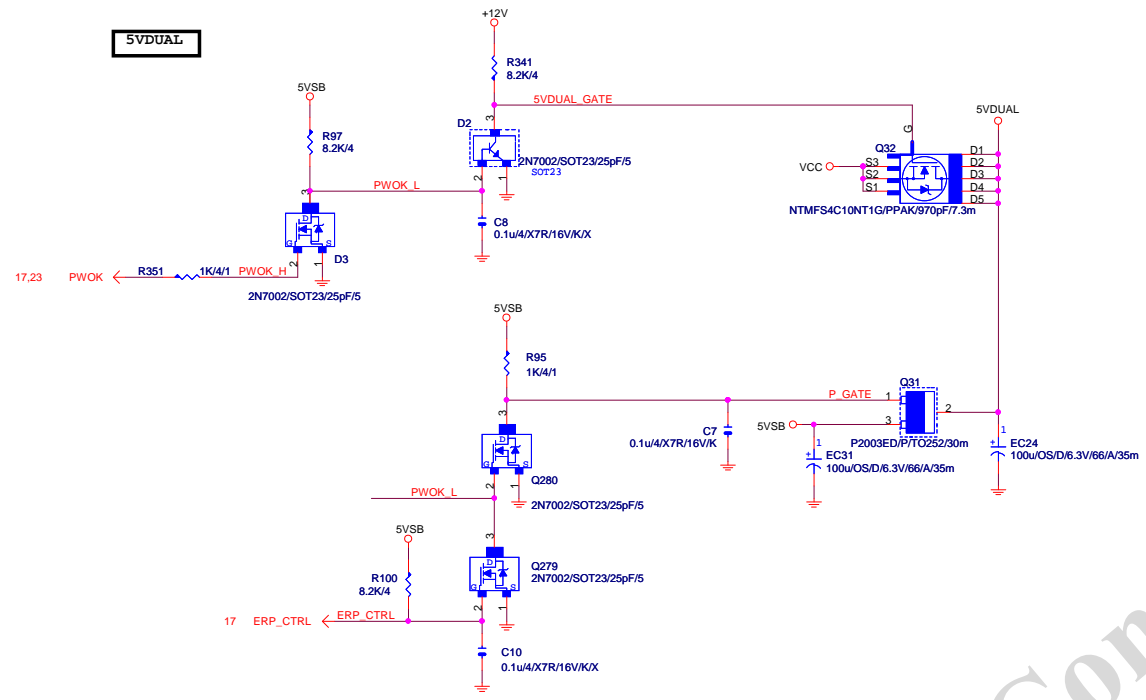






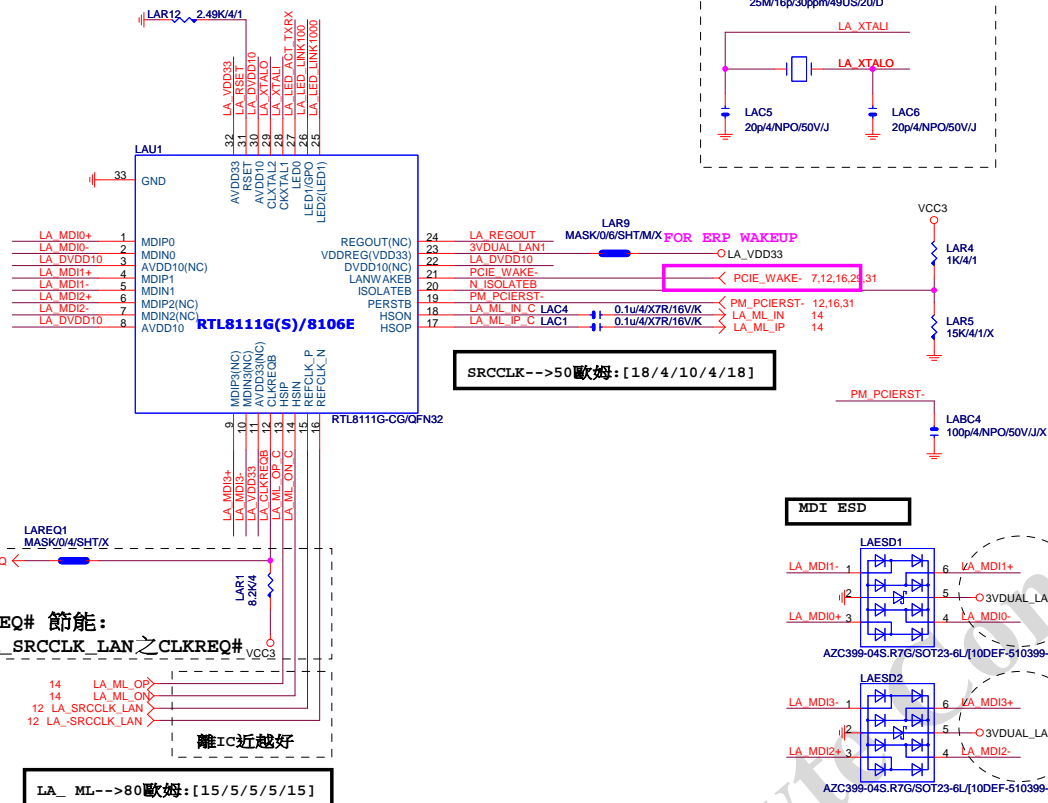
VDDCR SOC S5





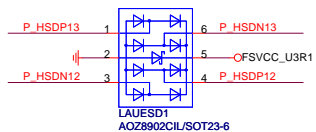
GIGABYTE™		
Title DDR POWER ,5VDUAL		
Size Custom	Document Number B450M DS3H	Rev 1.01
Date: Wednesday, August 29, 2018	Sheet 27	of 35

LAN:RTL8111G	R2.03
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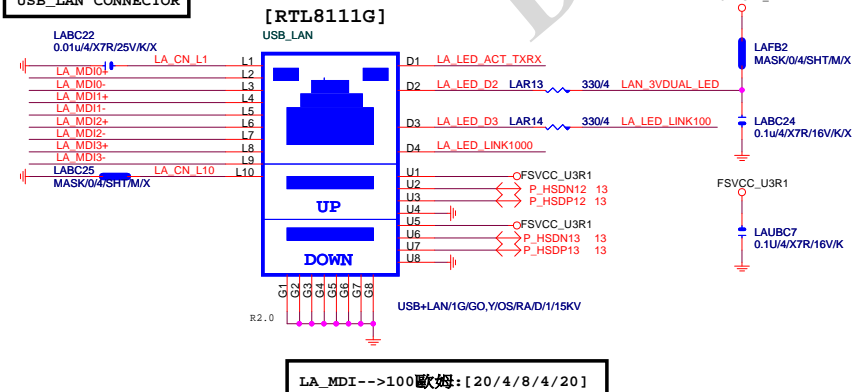


USB_LAN CONNECTOR	R2.03
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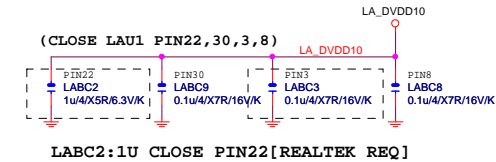
RMA ESD PROTECT



USB_LAN CONNECTOR

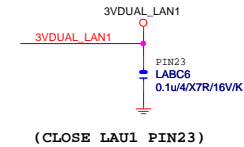


LAN POWER

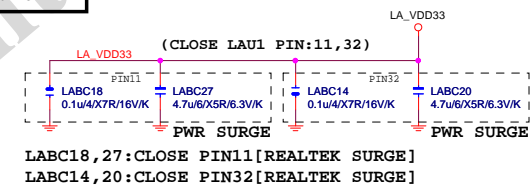


LAN POWER

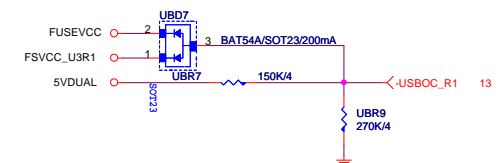
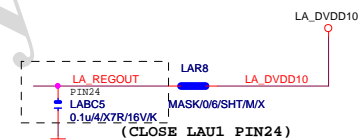
note: lan power連接及電流



LAN POWER



LAN POWER



USB POWER



Close to connector
USB_LAN 2-Port 2.0A
FUSE-0805

LAN POWER

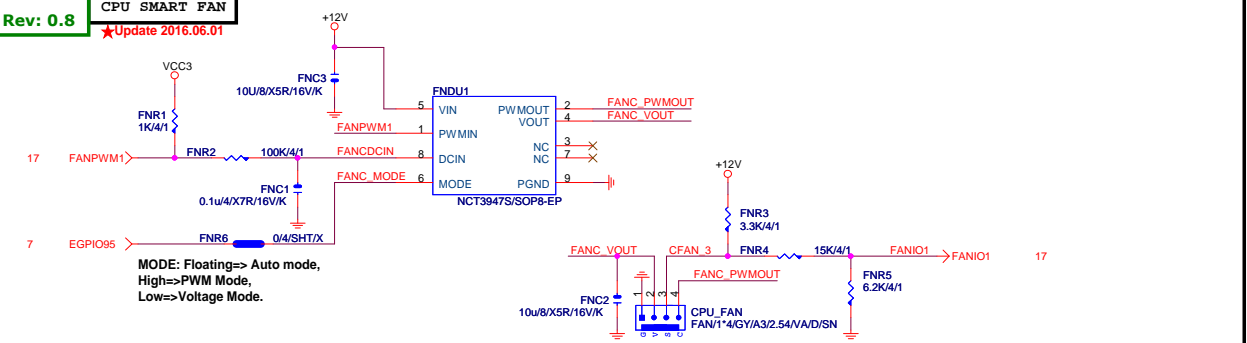


EMI

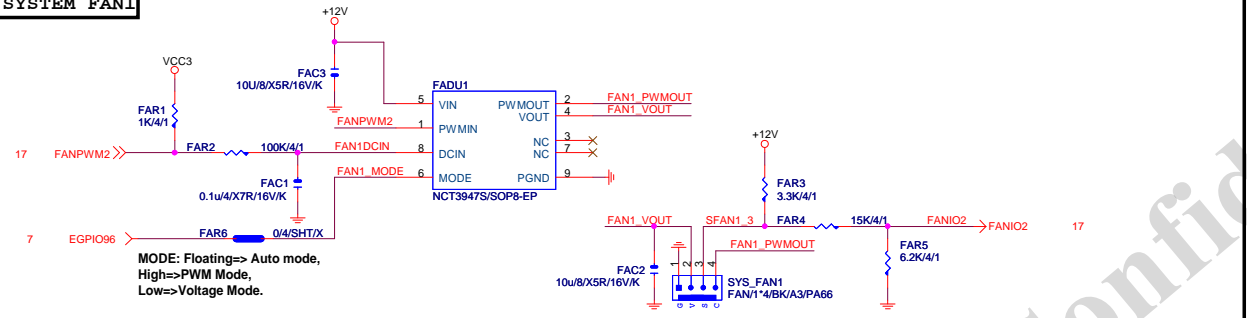
LAN AGND change GND
Remove Short Pad

GIGABYTE™

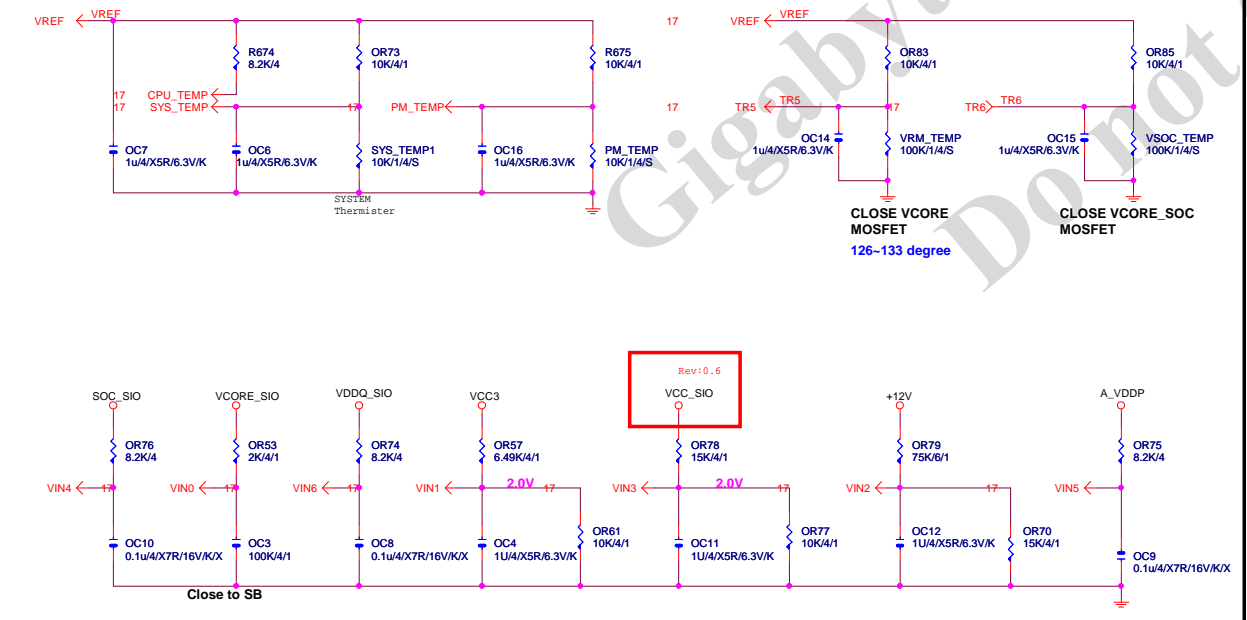
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Size	Document Number	Rev	
Custom	B450M DS3H	1.01	
Date:	Wednesday, August 29, 2018	Sheet	28 of 35



SYSTEM FAN1

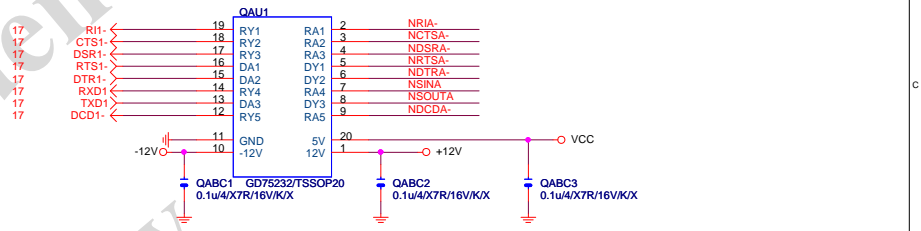


Hardware Monitor circuits

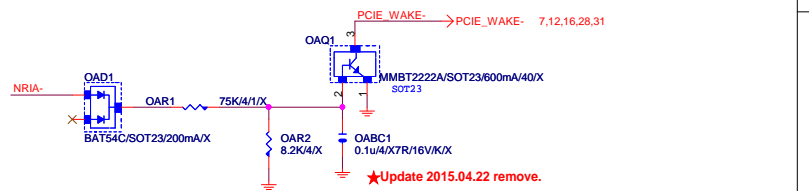
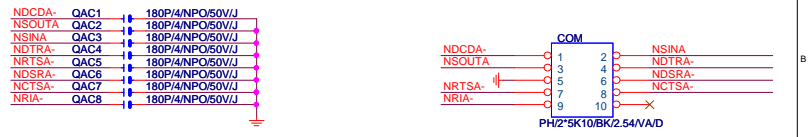


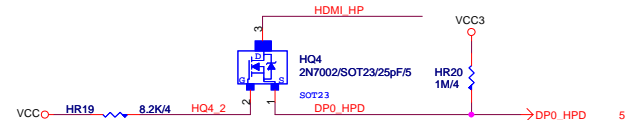
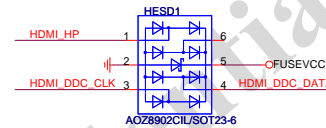
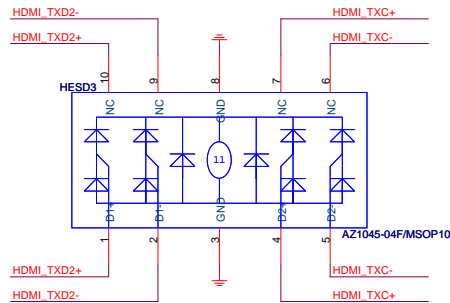
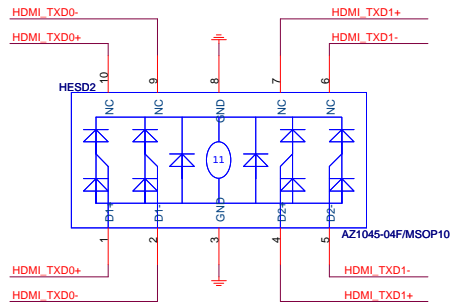
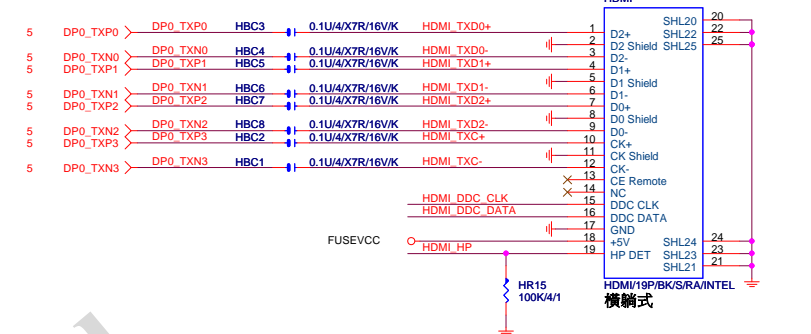
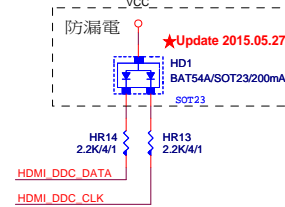
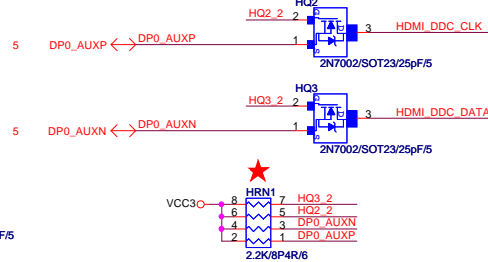
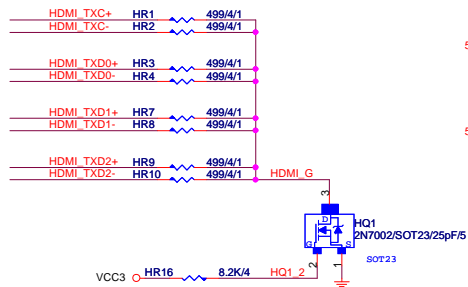
LPT PORT

COM PORT



R&D技術通報151 有使用PRINT PORT的
MODEL，需使用新料號:10HP2-118728-72R。(CHIP IT8728F/EX (GB) ITE/SMD
QFP128 PRINTPORT SORTING)料件。串電阻33 ohm改為68 ohm。

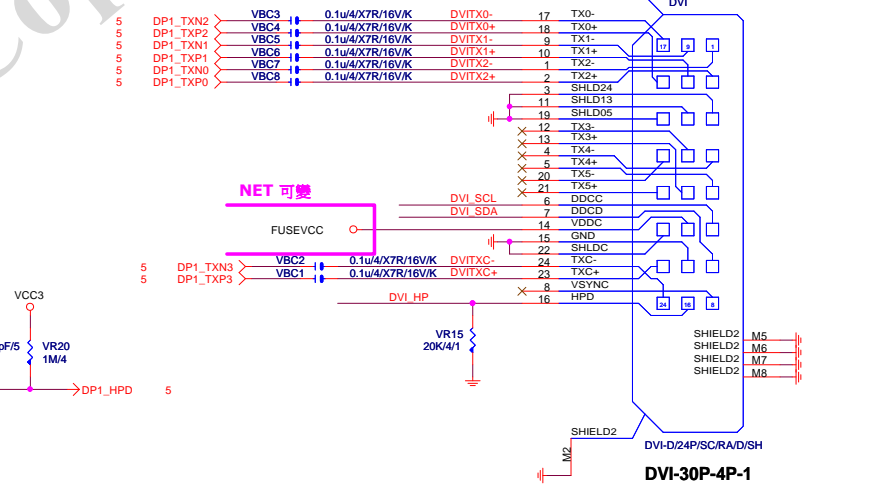
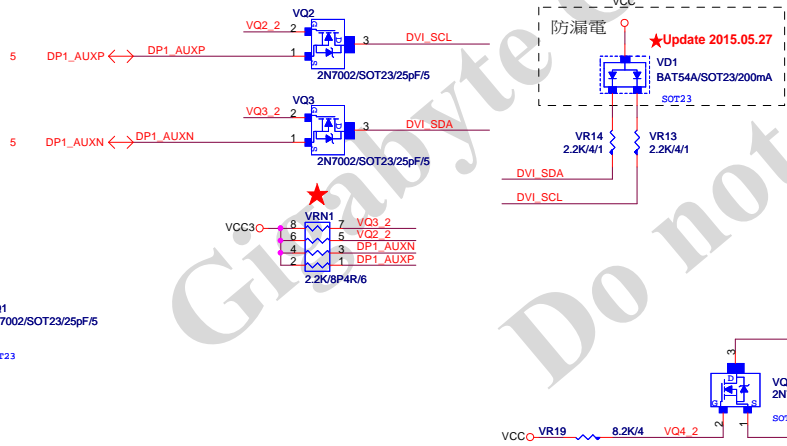
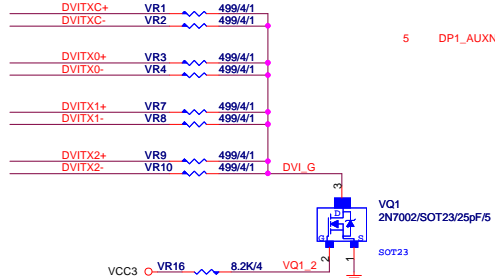




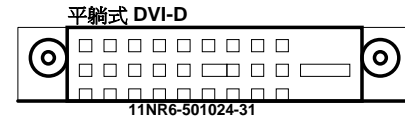
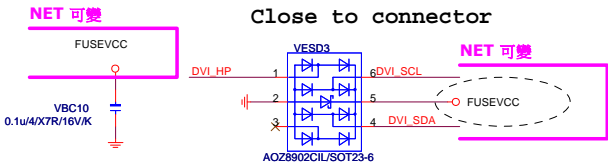
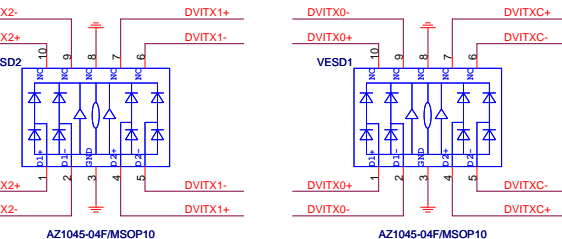
Rev: 0.73

DVI CONN

DVI: 20/4/6/4/20
Impedance=85 +- 17.5%



Close to connector



GIGABYTE

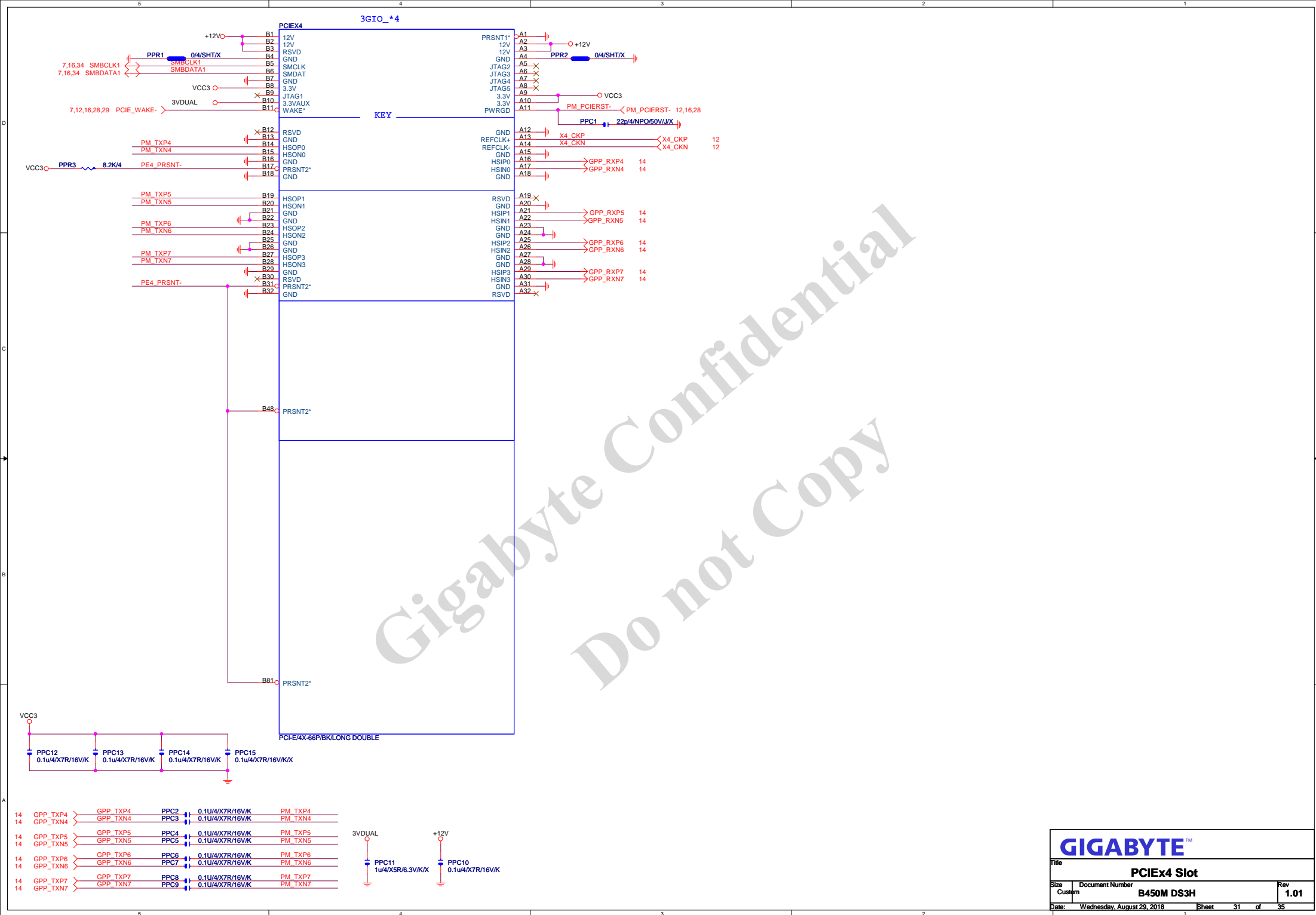
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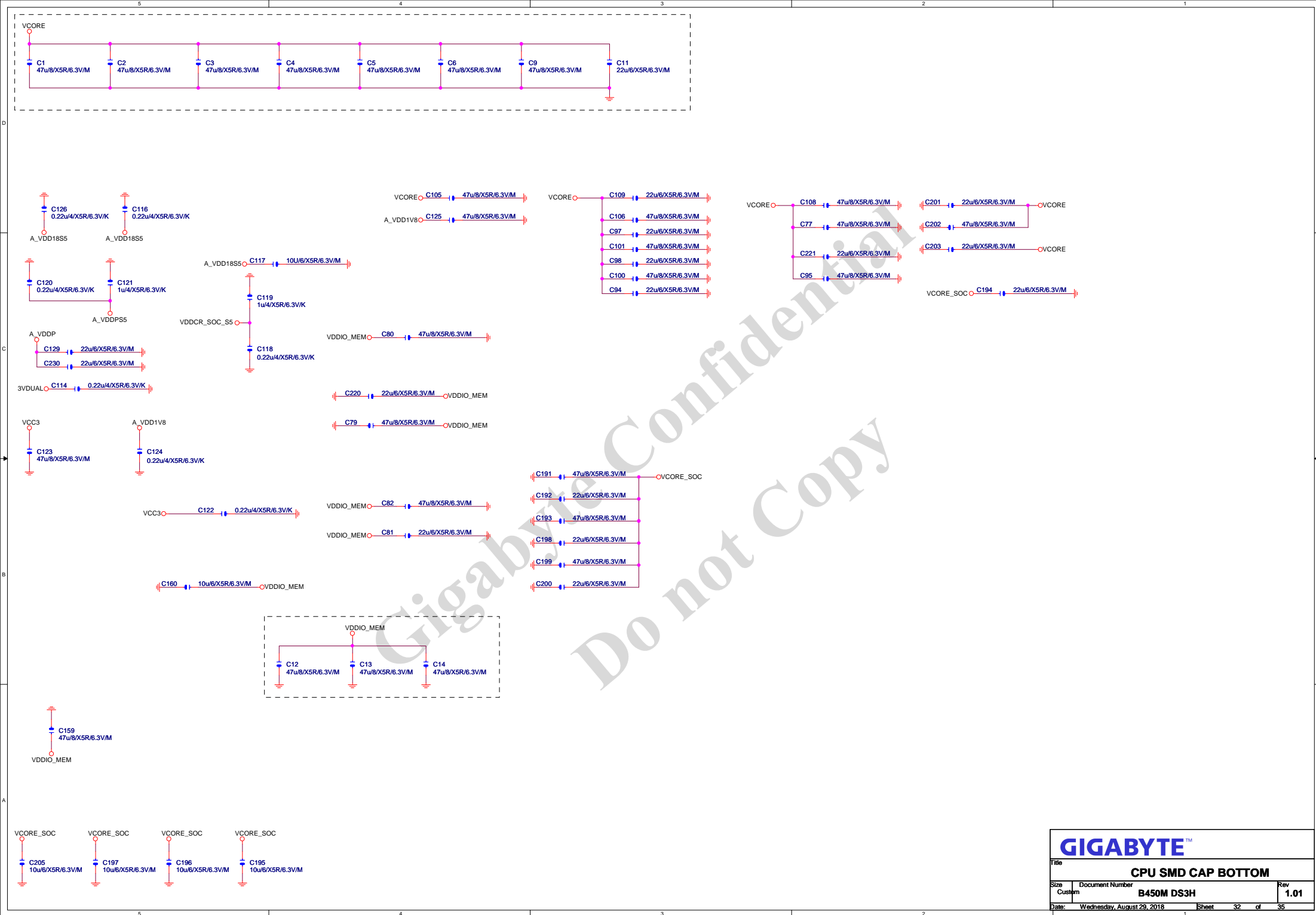
Size: **B450M DS3H**

Date: **Wednesday, August 29, 2018**

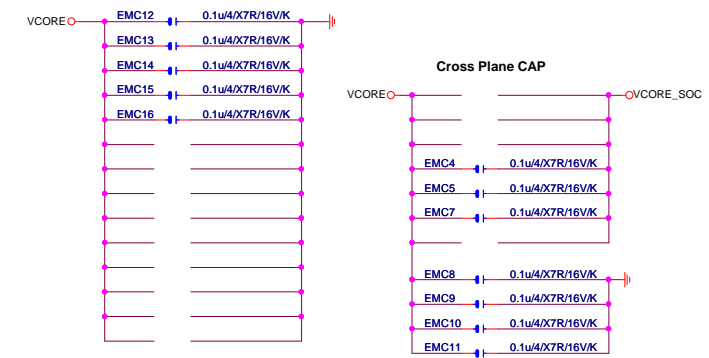
Sheet: **30** of **35**

Rev: **1.01**

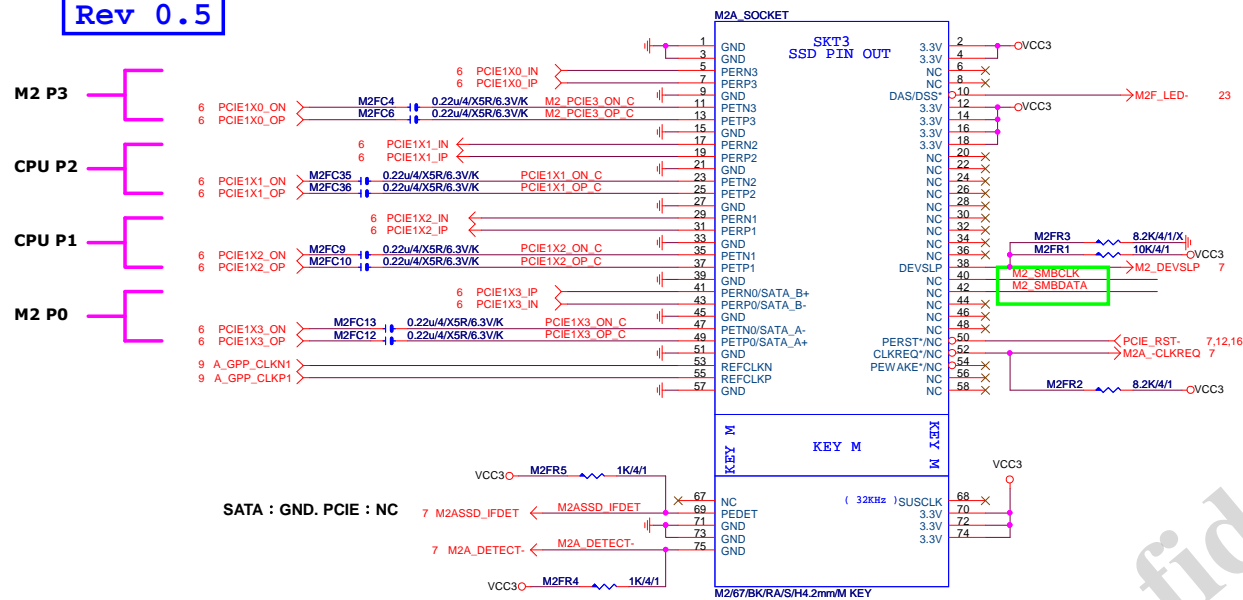




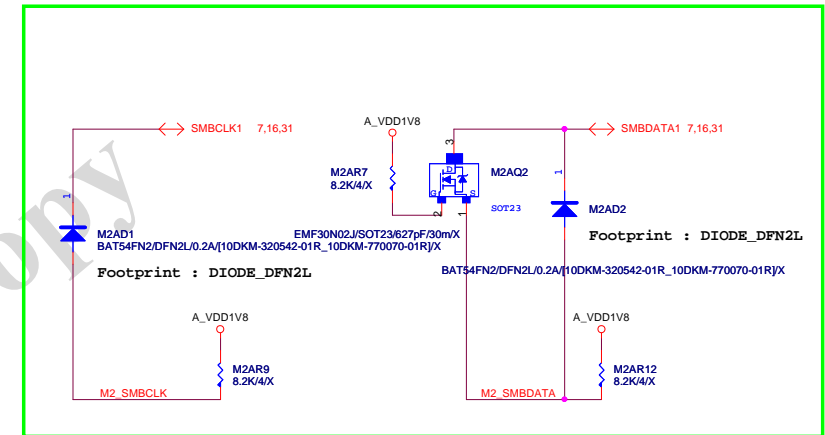
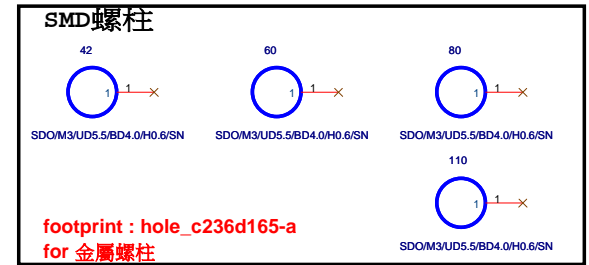
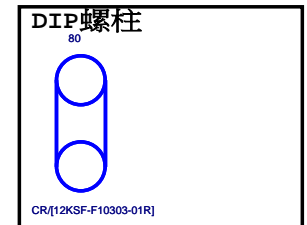
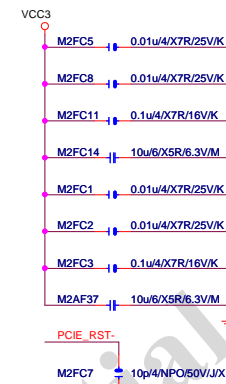
CPU TOP CAVITY

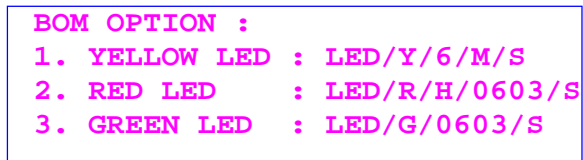


Rev 0.5



footprint : NGFF-M-75P-11CM-09MM-SMD





	IO_GP95	IO_GP91
Still Mode	H	L
OFF Mode	L	L
Pluse Mode	H	BREATH

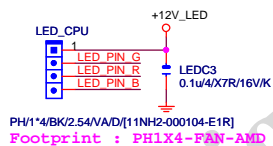
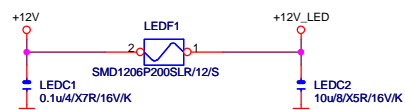
17 IO_GP22

LED PIN_R

17 IO_GP20

LED PIN_G

17 IO_GP21

[illegible]