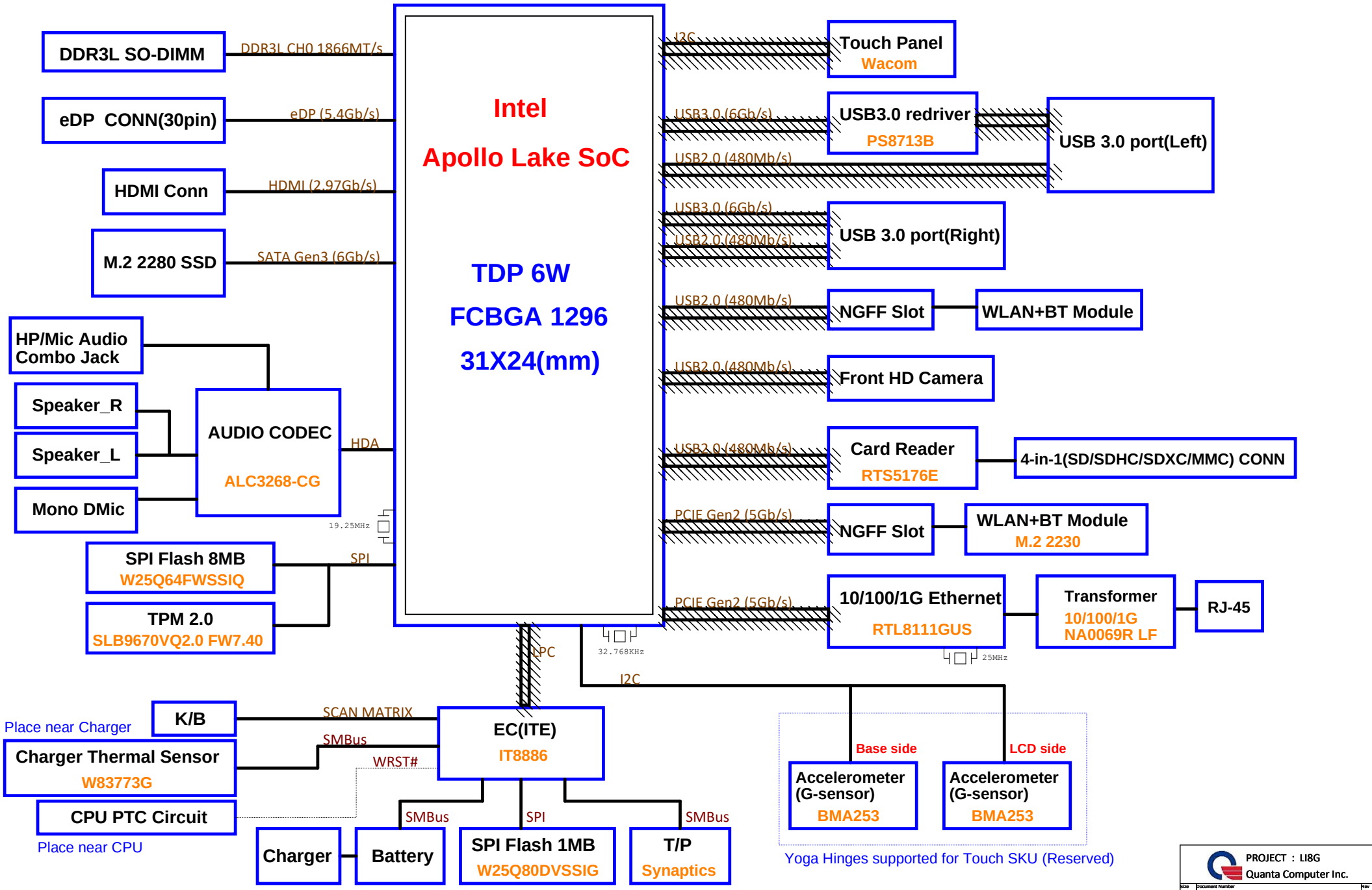
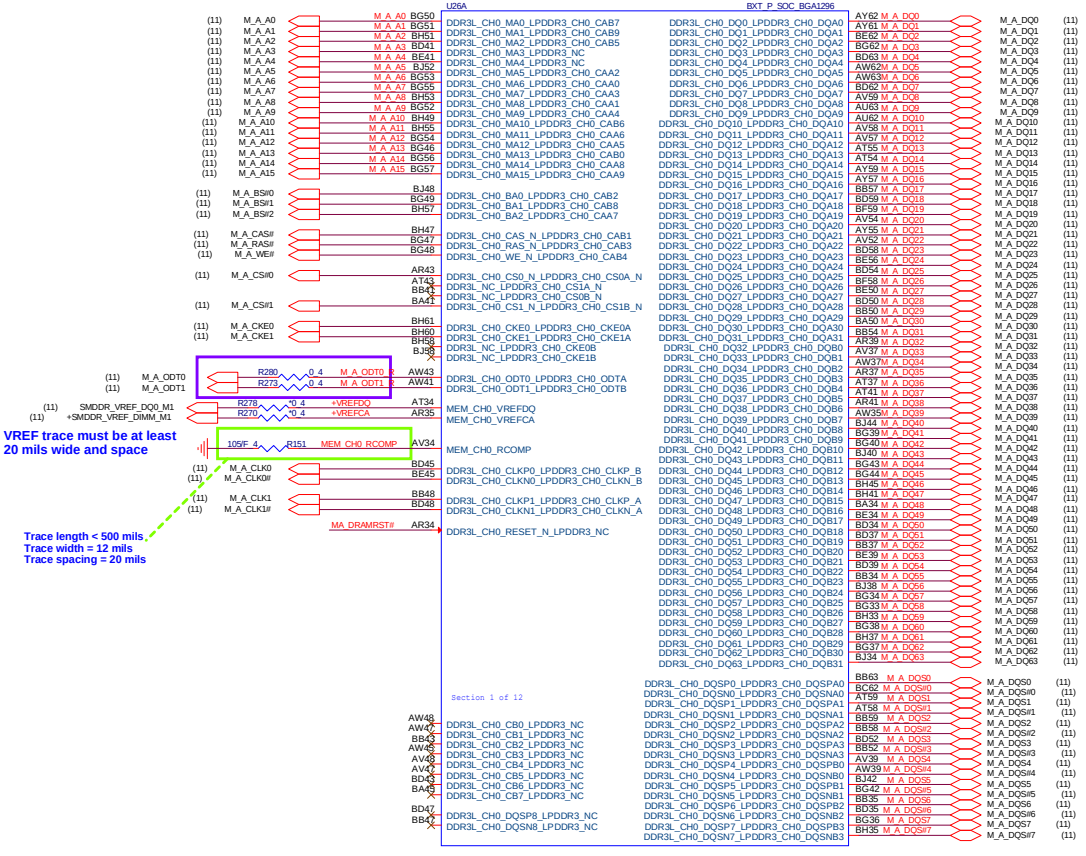
Newton II Intel APL Platform UMA Block Diagram (Windows)

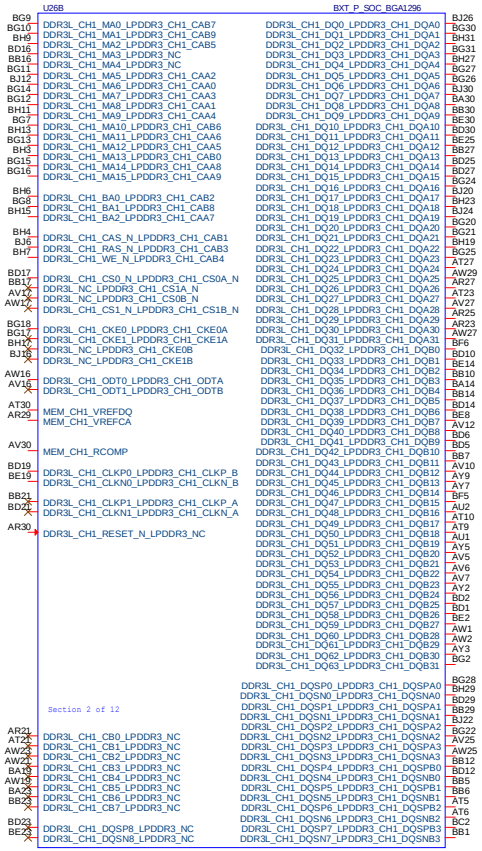


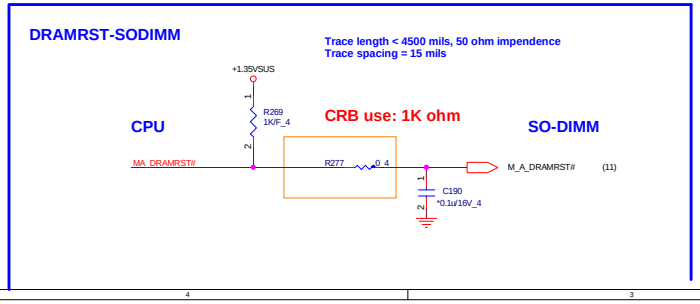
PROJECT : LI8G
Quanta Computer Inc.
LI8G Block Diagram

APL ULT (DDR3L)

(7,11,28,35) +1.35VSUS







PROJECT : LI8G

Quanta Computer Inc.

Size	Document Number	Rev
	BXTP (MEMORY)	1A

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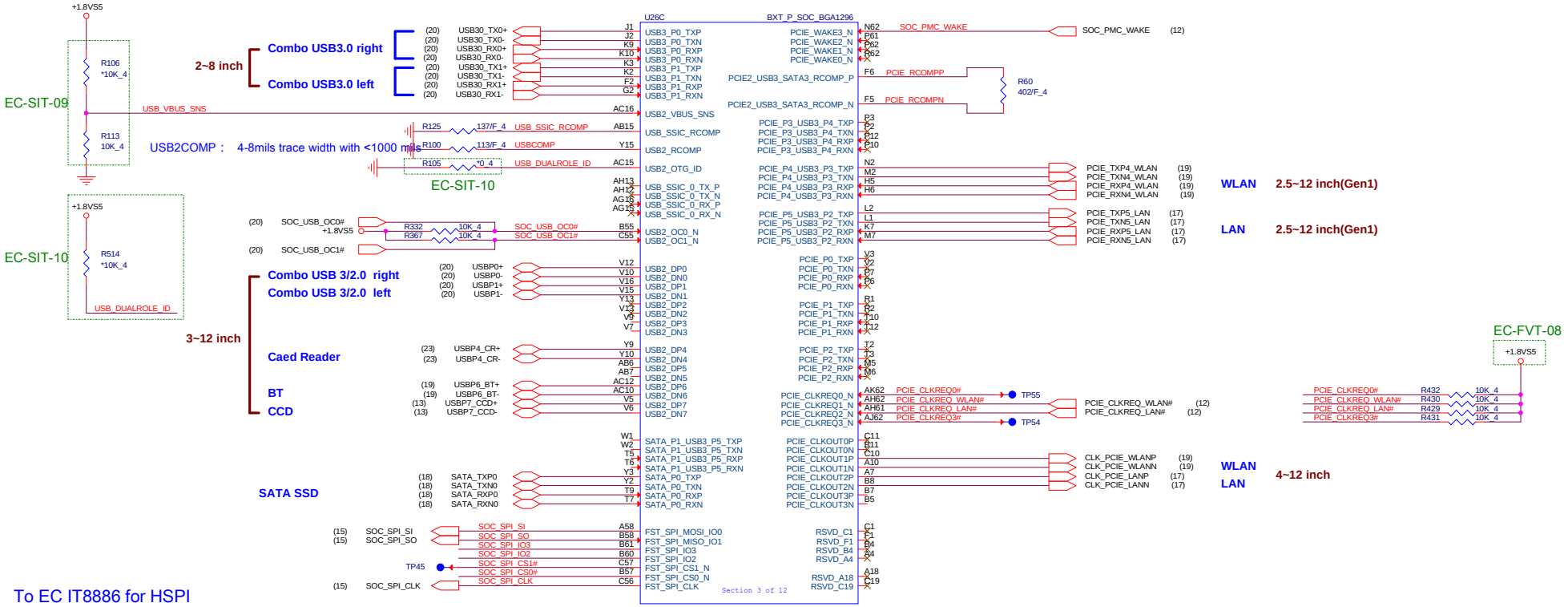
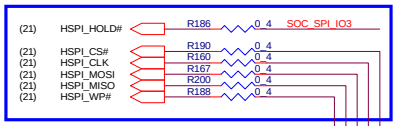
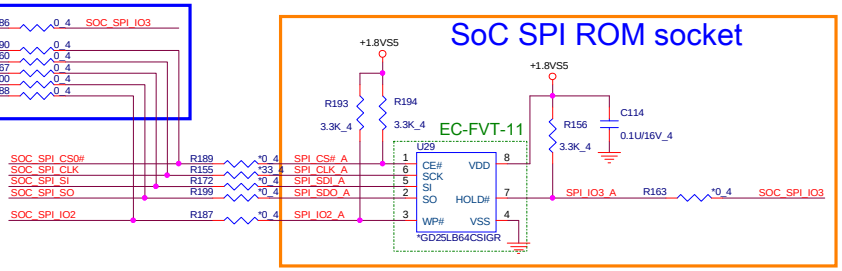
Apollo lake (SATA , ODD, CLK ,USB,PCIE)

03

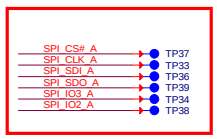
(4,5,6,7,9,10,12,14,15,21,29,31,33,35) +1.8VS5

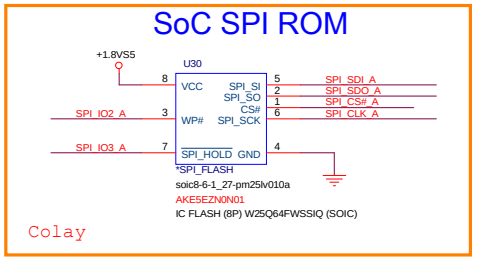






SPI socket P/N: DFHS08FS023 only for A-TEST





SPI ROM	Vender	Size	Quanta P/N	Vender P/N
1.8V	WND	8MB	AKE5EZN0N01	W25Q64FWSSIQ

PROJECT : LI8G

Quanta Computer Inc.

Size	Document Number	Rev
	BXTP (PCIE/USB/SATA/SPI)	1A

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Apollolake (DISPLAY,eDP)

(3,5,6,7,9,10,12,14,15,21,29,31,33,35) +1.8VS5
(6,12,13,14,18,21,33) +1.8V
(6,11,12,13,14,15,16,17,18,19,20,21,22,23,24,26,28,29,32,33) +3.3V

+1.8VS5

EDP_PANEL_EN R355 *100K/F_4
EDP_BKLT_EN R368 *100K/F_4
EDP_BKLTCTL R44 *100K/F_4

eDP PWM

+1.8V
EDP_BKLTCTL
Q9 RUC002N05GZT116
R47 4.7K_4 +3.3V
PCH_DPST_PWM (13)
R45 *0_4
R39 100K_4
GND

Max 7.5 inch

HDMI

(14) IN_D2
(14) IN_D2#
(14) IN_D1
(14) IN_D1#
(14) IN_D0
(14) IN_D0#
(14) IN_CLK
(14) IN_CLK#

DDI0_HPD (14) HDMI_HPD_DC#
TP8
DDI1_HPD

eDP Panel

(13) INT_EDP_TXP0
(13) INT_EDP_TXN0
(13) INT_EDP_AUXP
(13) INT_EDP_AUXN

<10000 mil

(14) SDVO_DATA
(14) SDVO_CLK

(12) EDP_PANEL_EN
(12) EDP_BKLT_EN

U26D BXT_P_SOC_BGA1296

DDI1_TXP_0 AF2
DDI1_TXN_0 AF3
DDI1_TXP_1 AD3
DDI1_TXN_1 AD2
DDI1_TXP_2 AC1
DDI1_TXN_2 AC2
DDI1_TXP_3 AB3
DDI1_TXN_3 AB2
DDI1_AUXP AK16
DDI1_AUXN AK15
MIPI_I2C_SDA B51
MIPI_I2C_SCL C51
DDI0_TXP_0 AK3
DDI0_TXN_0 AK2
DDI0_TXP_1 AM3
DDI0_TXN_1 AM2
DDI0_TXP_2 AH3
DDI0_TXN_2 AH2
DDI0_TXP_3 AL2
DDI0_TXN_3 AL1
DDI0_AUXP AM16
DDI0_AUXN AM15
DDI0_RCOMP_P AG1
DDI0_RCOMP_N AG2
GPIO_200 C50
GPIO_199 A50
EDP_TXP_0 AG7
EDP_TXN_0 AG9
EDP_TXP_1 AG12
EDP_TXN_1 AG10
EDP_TXP_2 AC6
EDP_TXN_2 AC5
EDP_TXP_3 AC7
EDP_TXN_3 AC9
EDP_RCOMP_P AG6
EDP_RCOMP_N AG5
EDP_AUXP AH10
EDP_AUXN AH9
DDI1_DDC_SDA C54
DDI1_DDC_SCL A54
DDI0_DDC_SDA C49
DDI0_DDC_SCL B49
PNL1_VDDEN C52
PNL1_BKLTEN B53
PNL1_BKLTCTL C53
PNL0_VDDEN C47
PNL0_BKLTEN B47
PNL0_BKLTCTL C46
OSC_CLK_OUT_0 AG62
OSC_CLK_OUT_1 AF61
OSC_CLK_OUT_2 AG63
OSC_CLK_OUT_3 AE60
OSC_CLK_OUT_4 AF62
OSCOUT P29
OSCIN R27
MDSI_RCOMP AP7
MDSI_C_DP_0 AK7
MDSI_C_DN_0 AK6
MDSI_C_DP_1 AM5
MDSI_C_DN_1 AM6
MDSI_C_DP_2 AM12
MDSI_C_DN_2 AM10
MDSI_C_DP_3 AK13
MDSI_C_DN_3 AM13
MDSI_C_CLKP AM9
MDSI_C_CLKN AM7
MDSI_A_DP_0 AP12
MDSI_A_DN_0 AP10
MDSI_A_DP_1 AR2
MDSI_A_DN_1 AR1
MDSI_A_DP_2 AP15
MDSI_A_DN_2 AP13
MDSI_A_DP_3 AP6
MDSI_A_DN_3 AP5
MDSI_A_CLKP AP2
MDSI_A_CLKN AP3
MCSI_RX_DATA0_P M23
MCSI_RX_DATA0_N P23
MCSI_RX_CLK0_P L23
MCSI_RX_CLK0_N J23
MCSI_RX_DATA1_P J21
MCSI_RX_DATA1_N H21
MCSI_RX_DATA2_P M25
MCSI_RX_DATA2_N L25
MCSI_RX_CLK1_P F25
MCSI_RX_CLK1_N E25
MCSI_RX_DATA3_P H25
MCSI_RX_DATA3_N J25
MCSI_DP_0 P17
MCSI_DN_0 M17
MCSI_DP_1 P21
MCSI_DN_1 R21
MCSI_DP_2 L17
MCSI_DN_2 J17
MCSI_DP_3 F17
MCSI_DN_3 E17
MCSI_CLKP_0 M19
MCSI_CLKN_0 H19
MCSI_CLKP_2 L19
MCSI_CLKN_2 F19
GP_CAMERASB0 L37
GP_CAMERASB1 P34
GP_CAMERASB2 J34
GP_CAMERASB3 H30
GP_CAMERASB4 M37
GP_CAMERASB5 F30
GP_CAMERASB6 R35
GP_CAMERASB7 L34
GP_CAMERASB8 M34
GP_CAMERASB9 M35
GP_CAMERASB10 R34
GP_CAMERASB11 E30
MDSI_A_TE M45
MDSI_C_TE M43
Section 4 of 12

R419 402/F_4 DDI0_RCOMP_P
R112 402/F_4 EDP_RCOMP_P
R428 150F_4 MDSI_RCOMP
MCSI_DPHY1.2_RCOMP F27
R57 150F_4 MCSI_DPHY1.2_RCOMP
MCSI_DPHY1.1_RCOMP H27
R58 150F_4 MCSI_DPHY1.1_RCOMP

CCD_EN (13)
LCD_BK_OFF (13)
TOUCH_PANEL_EN (13)

C229 15P/50V_4
C228 15P/50V_4
XTAL192_OUT
XTAL192_IN
Y2
19.2MHZ +-30PPM
R378 200K/F_4

<1000 mil

PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	BXTP (HDMI/eDP)	1A
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Apollolake (EMMC/LPC/I2C)

05

Refer to EDS, need change to Function 3 for pin H52

use for SPI TPM chip select

(15) SOC_SPI_CS2#_TPM → SOC_SPI_CS2#_TPM

U26E BXT_P_SOC_BGA1296

EMMC_D0 EMMC_D1 EMMC_D2 EMMC_D3 EMMC_D4 EMMC_D5 EMMC_D6 EMMC_D7 EMMC_RCLK EMMC_CMD EMMC_CLK

RSVD_V49

GPIO_RCOMP — R38 200/F_4

EMMC_RCOMP — R102 200/F_4

Pull low for normal platform operation (9) GPIO_104 → GPIO_104 → SIO_SPI_0_CLK
Pull low for normal platform operation (9) GPIO_105 → GPIO_105 → SIO_SPI_0_FS0
SOC_SPI_CS2#_TPM → SIO_SPI_0_FS1
SIO_SPI_0_RXD
SIO_SPI_0_TXD

LPC 1.8V/3.3V mode select (9) GPIO_110 — TP12 → GPIO_110

Boot BIOS Strap
Pull low for normal platform operation (9) GPIO_111 → GPIO_111 → SIO_SPI_1_CLK
Pull low for normal platform operation (9) GPIO_112 → GPIO_112 → SIO_SPI_1_FS0
Pull low for normal platform operation (9) GPIO_113 → GPIO_113 → SIO_SPI_1_FS1
SIO_SPI_1_RXD
Pull low for normal platform operation (9) GPIO_117 → GPIO_117 → SIO_SPI_1_TXD

SOC_OVRIDE → SIO_SPI_2_CLK

Top swap override (9) GPIO_120 — TP43 → GPIO_120 → SIO_SPI_2_FS0
Pull low for normal platform operation (9) GPIO_121 → GPIO_121 → SIO_SPI_2_FS1
SIO_SPI_2_FS2
Pull high for normal platform operation (9) GPIO_123 → GPIO_123 → SIO_SPI_2_RXD
SIO_SPI_2_TXD

EC_LPCCLK — C263 *18P/50V_4

LPC set 3.3V

(19,21) LPC_LAD0 — R402 22_4 — LPC_LAD0_R → LPC_AD0
(19,21) LPC_LAD1 — R403 22_4 — LPC_LAD1_R → LPC_AD1
(19,21) LPC_LAD2 — R400 22_4 — LPC_LAD2_R → LPC_AD2
(19,21) LPC_LAD3 — R401 22_4 — LPC_LAD3_R → LPC_AD3

DEBUG_LPCCLK — C264 *18P/50V_4

(21) EC_LPCCLK — R411 22_4 — LPC_CLKOUT0 → LPC_CLKOUT0
(19) DEBUG_LPCCLK — R412 22_4 — LPC_CLKOUT1 → LPC_CLKOUT1

(21) LPC_CLKRUN# — R399 22_4 — LPC_CLKRUN# → LPC_CLKRUN_N
(19,21) LPC_LFRAME# — R388 22_4 — LPC_LFRAME# → LPC_FRAME_N
(21) EC_IRQ_SERIRQ — R410 22_4 — SOC_SERIRQ → LPC_SERIRQ

Section 5 of 12

Enable CSE(TXE3.0) ROM Bypass (9) GPIO_39 — TP6 → GPIO_39 → LPSS_UART0_TXD
RTC Clock Timer Bypass (9) GPIO_40 — TP4 → GPIO_40 → LPSS_UART0_RXD
LPSS_UART0_RTS_N
LPSS_UART0_CTS_N

Allow eMMC as a boot source (9,10) GPIO_43 → GPIO_43 → LPSS_UART1_TXD
Allow SPI as a boot source (10) GPIO_42 → GPIO_42 → LPSS_UART1_RXD
(9) GPIO_44 → GPIO_44 → LPSS_UART1_RTS_N
LPSS_UART1_CTS_N

Force DNX FW Load (9) GPIO_47 — TP3 → GPIO_47 → LPSS_UART2_TXD
Pull low for normal platform operation (9) GPIO_48 — TP11 → GPIO_48 → LPSS_UART2_RXD
(12) SOC_KBC_SMI → LPSS_UART2_RTS_N
LPSS_UART2_CTS_N

C21 *0.1U/16V_4

SDIO_PWR_DWN_N
SDIO_D0 SDIO_D1 SDIO_D2 SDIO_D3 SDIO_CMD SDIO_CLK

SDCARD_LVL_WP SDCARD_D0 SDCARD_D1 SDCARD_D2 SDCARD_D3 SDCARD_CMD SDCARD_CLK SDCARD_CD_N

GPIO_0 BID0 — BID0 (10)
GPIO_1 BID1 — BID1 (10)
GPIO_2 BID2 — BID2 (10)
GPIO_3 BID3 — BID3 (10)
GPIO_4 BID4 — BID4 (10)
GPIO_5 BID5 — BID5 (10)
GPIO_6 — ACCEL_INTH# (10)
GPIO_7 — GPIO_7 (10)
GPIO_8 — GPIO_8 (10)
GPIO_9 — GPIO_9 (10)

GPIO_10 — R380 0_4 / R376 *0_4 — SOC_KBC_SCI (12)

3/28 add Res option

GPIO_11 E39
GPIO_12 C30
GPIO_13 C38 — LED_MIC_MUTE# (24)
GPIO_14 F39 — TOUCH_PANEL_RST#_SOC (12)
GPIO_15 C36 — SIM_DET — TPM_INT# (15)
GPIO_16 C35 — NGFF_PRE

EC-SIT-01

GPIO_17 J39
GPIO_18 C33
GPIO_19 B27 — IERR — R328 *0_4 — SOC_PCI_SERR#
GPIO_20 C26 — SOC_TCH_INT# (12)
GPIO_21 A26 — SATA_GP0 — TP44
GPIO_22 B25 — SATA_GP1 — TP5
GPIO_23 C25 — SATA_DEVSLP — SOC_DEVSLP (12)
GPIO_24 C27 — LED_SPK_MUTE# (24)
GPIO_25 C31 — LED_FN_KEY# (24)
GPIO_26 C29

EC-SIT-19

EC-SIT-01

GPIO_27 B37
GPIO_28 B35
GPIO_29 C37
GPIO_30 D34
GPIO_31 F35
GPIO_32 F34
GPIO_33

ISH_GPIO_0 AM48 — HDA_BCLK_R — R451 33_4 — ACZ_BCLK_AUDIO (16)
ISH_GPIO_1 AK58 — HDA_SYNC_R — R147 33_4 — ACZ_SYNC_AUDIO (16)
ISH_GPIO_2 AK51 — ACZ_SDIN0 (16)
ISH_GPIO_3 AM54 — HDA_SDO_R — R150 33_4 — ACZ_SDOUT_AUDIO (16)
ISH_GPIO_4 AM51 — TP26
ISH_GPIO_5 AM49 — RF_KILL#_R
ISH_GPIO_6 AM57 — TP31
ISH_GPIO_7 AM55 — TP29
ISH_GPIO_8 AM52 — SOC_BT_OFF# — SOC_BT_OFF# (12)
ISH_GPIO_9 AK57 — ACZ_SPKR (16)

HDA

LPSS_I2C0_SDA AR62 — SOC_TCH_PNL_SDA — SOC_TCH_PNL_SDA (12)
LPSS_I2C0_SCL AR63 — SOC_TCH_PNL_SCL — SOC_TCH_PNL_SCL (12)

I2C to Touch

LPSS_I2C1_SDA AM62 — SOC_SENS_SDA — SOC_SENS_SDA (13,18)
LPSS_I2C1_SCL AM61 — SOC_SENS_SCL — SOC_SENS_SCL (13,18)

I2C to sensor

LPSS_I2C2_SDA AP59
LPSS_I2C2_SCL AP58
LPSS_I2C3_SDA AM62
LPSS_I2C3_SCL AL62
LPSS_I2C4_SDA AP52
LPSS_I2C4_SCL AP54
LPSS_I2C5_SDA AP49
LPSS_I2C5_SCL AP51
LPSS_I2C6_SDA AL63
LPSS_I2C6_SCL AK61
LPSS_I2C7_SDA AP62
LPSS_I2C7_SCL AP61

EC-SIT-01

(3,4,6,7,9,10,12,14,15,21,29,31,33,35) +1.8VS5
(4,6,12,13,14,18,21,33) +1.8V

+1.8VS5

SOC_PCI_SERR# R329 *10K_4
ACCEL_INTH# R377 10K_4
SOC_KBC_SCI R366 10K_4
SOC_KBC_SMI R41 10K_4

SOC_BT_OFF# R433 4.7K/F_4

NGFF_PRE R375 10K_4
SIM_DET R374 10K_4
RF_KILL#_R R128 10K_4

ACZ_BCLK_AUDIO — C296 *33p/50V_4

SOC_PCI_SERR# — EC-SIT-19

(21) EC_IERR# — Q27 RK7002BM

APL Doc.560733(HDA SDI I/O pin issue
Remove these circuit for QS sample

EC-FVT-18

HDA_SYNC_R R140 *249/F_4 — HDA_SDIN0_AUDIO (16)
R146 *510/F_4

+1.8VS5

SOC_TCH_PNL_SCL R460 2.2K_4
SOC_TCH_PNL_SDA R457 2.2K_4
SOC_SENS_SCL R454 2.2K_4
SOC_SENS_SDA R450 2.2K_4

I2C standard/fast mode:
I2C total lenght is about 4500 mils = 4.5inchs
Cb = 4.5*5pF +7pF = 29.5pF
PU resistor = 2K ohm

BOARD ID SETTING

EC-FVT-13 EC-SIT-25

+1.8VS5

R326 *10K_4 BID0 — R343 10K_4
R327 10K_4 BID1 — R344 *10K_4
R324 *10K_4 BID2 — R341 10K_4
R325 10K_4 BID3 — R342 *10K_4

SKU	BID_0	BID_1	BID_2	BID_3
SDV Non-Touch	0	0	0	0
SDV Touch	1	0	0	0
FVT Non-Touch	0	0	0	1
FVT Touch	1	0	0	1
SIT Non-Touch	0	0	1	0
SIT Touch	1	0	1	0
SVT Non-Touch				
SVT Touch				

Override

Flash Descriptor Override (SOC_OVRIDE)
0 = Normal Override(Normal operation)
1 = Override

+1.8VS5

R372 100K_4

R359 4.7K_4 — SOC_OVRIDE

GPIO_118 HW Strap

(21) EN_OVERRIDE# — Q37 RUC002N05GZT116

PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	BXTP (GPIO/LPC/I2C/HDA)	1A
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Apollolake (PMU/PMIC/HDA)

06

PMU set to 3.3V

EC-FVT-16

check list use 20k

EC-SIT-21

Pin AG55 is EMMC_PWR_EN_N (CRB 1.0)

SMBUS set to 3.3V

SMBus 1.8V/3.3V mode select

PMU 1.8V/3.3V mode select

Apollo EDS pin腳有錯誤 SMBus No Re-Boot

Pull low for normal platform operation

Folllow APL MOW31 ::
un-stuff 51 ohm pull down resistor on TRST_N pin

RTC Clock 32.768KHz (CPU)

Trace length < 1000 mils

CH01006JB08 -> 10p
CH01506JB06 -> 15p
CH-6806TB01 -> 6.8p

EC-SIT-16

*SSM6N43FU

AC_PRESENT

eDP HPD

RTC Circuitry (RTC)

+3V_RTC
Trace width = 20 mils

Trace width = 20 mils

20MIL

EC reset RTC

EC-SIT-17

SMBus

SoC

APL S5

S0

DDR3L
Click Pad

PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	BXTP (PMU/PMIC/SMB/RTC)	1A

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BOT side cap

TOP side cap

Apollolake (POWER)

07

(6,12,13,15,16,17,19,20,21,24,27,31,32,33,35) +3VS5
(31,35) +1.24VS5
(3,4,5,6,9,10,12,14,15,21,29,31,33,35) +1.8VS5
(6) +3V_RTC

(29,30) +VNN
(29,30) +VCC_VCGI
(6,29,32,35) +1.05V
(2,11,28,35) +1.35VSUS

+VNN Output Decoupling Recommendations

1uFx3	0402	BOT, inside socket cavity
22uFx4	0603	TOP, inside socket cavity

VDD2_1P24_GLML Output Decoupling Recommendations

1uFx3	0402	TOP*1 / BOT*3, inside socket cavity
22uFx1	0603	TOP, inside socket cavity

VDD2_1P24_DSI_CSI Output Decoupling Recommendations

1uFx2	0402	TOP*1 / BOT*1, inside socket cavity
22uFx1	0603	TOP, inside socket cavity

VDD2_1P24_AUD_ISH_PLL Output Decoupling Recommendations

1uFx2	0402	TOP*1 / BOT*1, inside socket cavity
22uFx1	0603	TOP, inside socket cavity

VDD2_1P24_MPHY Output Decoupling Recommendations

1uFx3	0402	TOP*1 / BOT*2, inside socket cavity
22uFx1	0603	TOP, inside socket cavity

VCCRAM_1P05_IO_3PHASEIO Output Decoupling Recommendations

1uFx4	0402	TOP*2 / BOT*2, inside socket cavity
22uFx1	0603	TOP, inside socket cavity

+VCCDDQ Output Decoupling Recommendations

1uFx2	0402	BOT, inside socket cavity
22uFx8	0603	TOP, inside socket cavity

+VCC_VCCGI Output Decoupling Recommendations

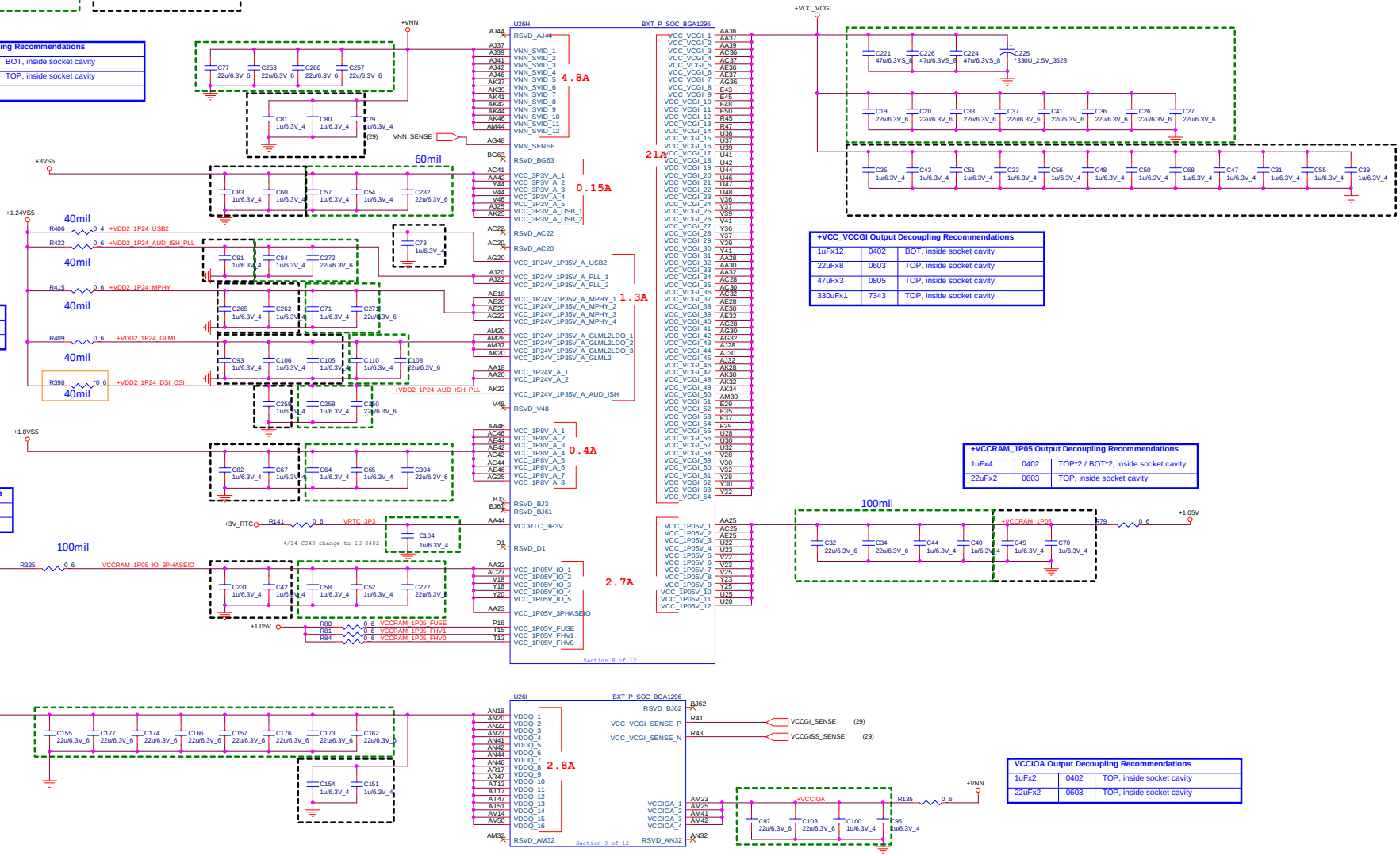
1uFx12	0402	BOT, inside socket cavity
22uFx8	0603	TOP, inside socket cavity
47uFx3	0805	TOP, inside socket cavity
330uFx1	7343	TOP, inside socket cavity

+VCCRAM_1P05 Output Decoupling Recommendations

1uFx4	0402	TOP*2 / BOT*2, inside socket cavity
22uFx2	0603	TOP, inside socket cavity

VCCIOA Output Decoupling Recommendations

1uFx2	0402	TOP, inside socket cavity
22uFx2	0603	TOP, inside socket cavity



PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	BXTP (POWER)	1A

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Apollolake ULT (GND)

U26J BXT_P_SOC_BGA1296

R29	VSS_1	VSS_82	AH58
A12	VSS_2	VSS_83	AH59
A16	VSS_3	VSS_84	AH6
A20	VSS_4	VSS_85	AH7
A24	VSS_5	VSS_86	AJ1
A28	VSS_6	VSS_87	AJ18
A32	VSS_7	VSS_88	AJ2
A36	VSS_8	VSS_89	AJ23
A40	VSS_9	VSS_90	AJ27
A44	VSS_10	VSS_91	AJ34
A48	VSS_11	VSS_92	AJ36
A5	VSS_12	VSS_93	AJ63
A52	VSS_13	VSS_94	AK10
A56	VSS_14	VSS_95	AK12
A62	VSS_15	VSS_96	AK18
A9	VSS_16	VSS_97	AK23
AA1	VSS_17	VSS_98	AK27
AA2	VSS_18	VSS_99	AK36
AA27	VSS_19	VSS_100	AK48
AA34	VSS_20	VSS_101	AK5
AA41	VSS_21	VSS_102	AK52
AA63	VSS_22	VSS_103	AK59
AB10	VSS_23	VSS_104	AK9
AB12	VSS_24	VSS_105	AM18
AB16	VSS_25	VSS_106	AM22
AB48	VSS_26	VSS_107	AM27
AB5	VSS_27	VSS_108	AM34
AB52	VSS_28	VSS_109	AM36
AB57	VSS_29	VSS_110	AM39
AB59	VSS_30	VSS_111	AM46
AB9	VSS_31	VSS_112	AN1
AC18	VSS_32	VSS_113	AN10
AC27	VSS_33	VSS_114	AN11
AC34	VSS_34	VSS_115	AN13
AC39	VSS_35	VSS_116	AN14
AE1	VSS_36	VSS_117	AN16
AE10	VSS_37	VSS_118	AN17
AE11	VSS_38	VSS_119	AN2
AE13	VSS_39	VSS_120	AN25
AE14	VSS_40	VSS_121	AN27
AE16	VSS_41	VSS_122	AN28
AE17	VSS_42	VSS_123	AN30
AE2	VSS_43	VSS_124	AN34
AE23	VSS_44	VSS_125	AN36
AE27	VSS_45	VSS_126	AN37
AE34	VSS_46	VSS_127	AN39
AE39	VSS_47	VSS_128	AN47
AE4	VSS_48	VSS_129	AN48
AE41	VSS_49	VSS_130	AN5
AE47	VSS_50	VSS_131	AN50
AE48	VSS_51	VSS_132	AN51
AE5	VSS_52	VSS_133	AN53
AE50	VSS_53	VSS_134	AN54
AE51	VSS_54	VSS_135	AN56
AE53	VSS_55	VSS_136	AN57
AE54	VSS_56	VSS_137	AN59
AE56	VSS_57	VSS_138	AN63
AE57	VSS_58	VSS_139	AN7
AE59	VSS_59	VSS_140	AN8
AE63	VSS_60	VSS_141	AP55
AE7	VSS_61	VSS_142	AP9
AE8	VSS_62	VSS_143	AR19
AG13	VSS_63	VSS_144	AR32
AG18	VSS_64	VSS_145	AR45
AG23	VSS_65	VSS_146	AT12
AG27	VSS_66	VSS_147	AT16
AG34	VSS_67	VSS_148	AT19
AG37	VSS_68	VSS_149	AT2
AG39	VSS_69	VSS_150	AT25
AG41	VSS_70	VSS_151	AT29
AG42	VSS_71	VSS_152	AT3
AG44	VSS_72	VSS_153	AT35
AG46	VSS_73	VSS_154	AT39
AH15	VSS_74	VSS_155	AT45
AH16	VSS_75	VSS_156	AT48
AH48	VSS_76	VSS_157	AT52
AH5	VSS_77	VSS_158	AT57
AH52	VSS_78	VSS_159	AT61
AH54	VSS_79	VSS_160	AT62
AH55	VSS_80	VSS_161	AT7
AH57	VSS_81	VSS_162	AU32

Section 10 of 12

U26K BXT_P_SOC_BGA1296

AV19	VSS_163	VSS_244	BG29
AV2	VSS_164	VSS_245	BG32
AV21	VSS_165	VSS_246	BG35
AV23	VSS_166	VSS_247	BG41
AV29	VSS_167	VSS_248	BG45
AV3	VSS_168	VSS_249	BH1
AV32	VSS_169	VSS_250	BH2
AV35	VSS_170	VSS_251	BH21
AV41	VSS_171	VSS_252	BH25
AV43	VSS_172	VSS_253	BH39
AV45	VSS_173	VSS_254	BH43
AV55	VSS_174	VSS_255	BH62
AV61	VSS_175	VSS_256	BH63
AV62	VSS_176	VSS_257	BJ10
AV9	VSS_177	VSS_258	BJ14
AW14	VSS_178	VSS_259	BJ18
AW30	VSS_179	VSS_260	BJ28
AW34	VSS_180	VSS_261	BJ32
AW50	VSS_181	VSS_262	BJ36
AY10	VSS_182	VSS_263	BJ4
AY32	VSS_183	VSS_264	BJ46
AY54	VSS_184	VSS_265	BJ50
AY58	VSS_185	VSS_266	BJ54
AY6	VSS_186	VSS_267	BJ56
B2	VSS_187	VSS_268	BJ60
B3	VSS_188	VSS_269	BJ8
B62	VSS_189	VSS_270	C12
B63	VSS_190	VSS_271	C16
B9	VSS_191	VSS_272	C28
BA1	VSS_192	VSS_273	C32
BA12	VSS_193	VSS_274	C40
BA16	VSS_194	VSS_275	C48
BA17	VSS_195	VSS_276	D32
BA2	VSS_196	VSS_277	D58
BA21	VSS_197	VSS_278	D6
BA25	VSS_198	VSS_279	E12
BA27	VSS_199	VSS_280	E14
BA29	VSS_200	VSS_281	E19
BA32	VSS_201	VSS_282	E27
BA35	VSS_202	VSS_283	E4
BA37	VSS_203	VSS_284	E54
BA39	VSS_204	VSS_285	F10
BA43	VSS_205	VSS_286	F21
BA47	VSS_206	VSS_287	F3
BA48	VSS_207	VSS_288	F32
BA52	VSS_208	VSS_289	F37
BA62	VSS_209	VSS_290	F43
BA63	VSS_210	VSS_291	F45
BB19	VSS_211	VSS_292	F50
BB25	VSS_212	VSS_293	F56
BB3	VSS_213	VSS_294	F59
BB39	VSS_214	VSS_295	F63
BB45	VSS_215	VSS_296	G1
BB61	VSS_216	VSS_297	G32
BC32	VSS_217	VSS_298	H17
BD3	VSS_218	VSS_299	H23
BD32	VSS_219	VSS_300	H29
BD56	VSS_220	VSS_301	H3
BD61	VSS_221	VSS_302	H37
BD8	VSS_222	VSS_303	H47
BE1	VSS_223	VSS_304	H61
BE10	VSS_224	VSS_305	H7
BE12	VSS_225	VSS_306	J12
BE16	VSS_226	VSS_307	J14
BE17	VSS_227	VSS_308	J19
BE21	VSS_228	VSS_309	J27
BE27	VSS_229	VSS_310	J30
BE29	VSS_230	VSS_311	J32
BE35	VSS_231	VSS_312	J35
BE37	VSS_232	VSS_313	J37
BE43	VSS_233	VSS_314	J48
BE47	VSS_234	VSS_315	J63
BE48	VSS_235	VSS_316	K32
BE52	VSS_236	VSS_317	K5
BE54	VSS_237	VSS_318	K54
BE63	VSS_238	VSS_319	K57
BF3	VSS_239	VSS_320	K6
BF32	VSS_240	VSS_321	L21
BF61	VSS_241	VSS_322	L27
BG19	VSS_242	VSS_323	L29
BG23	VSS_243	VSS_324	L35

Section 11 of 12

U26L BXT_P_SOC_BGA1296

L43	VSS_325	VSS_361	U2
L45	VSS_326	VSS_362	U27
L50	VSS_327	VSS_363	U34
M14	VSS_328	VSS_364	U5
M21	VSS_329	VSS_365	U50
M27	VSS_330	VSS_366	U51
M3	VSS_331	VSS_367	U53
M32	VSS_332	VSS_368	U54
M50	VSS_333	VSS_369	U56
M59	VSS_334	VSS_370	U57
M9	VSS_335	VSS_371	U59
N1	VSS_336	VSS_372	U62
N32	VSS_337	VSS_373	U63
N63	VSS_338	VSS_374	U7
P13	VSS_339	VSS_375	U8
P19	VSS_340	VSS_376	V20
P35	VSS_341	VSS_377	V27
P37	VSS_342	VSS_378	V34
P41	VSS_343	VSS_379	V42
P43	VSS_344	VSS_380	Y12
P45	VSS_345	VSS_381	Y16
P5	VSS_346	VSS_382	Y22
P55	VSS_347	VSS_383	Y27
P59	VSS_348	VSS_384	Y34
P9	VSS_349	VSS_385	Y42
R23	VSS_350	VSS_386	Y46
R32	VSS_351	VSS_387	Y48
T49	VSS_352	VSS_388	Y5
U1	VSS_353	VSS_389	Y52
U10	VSS_354	VSS_390	Y54
U11	VSS_355	VSS_391	Y55
U13	VSS_356	VSS_392	Y57
U14	VSS_357	VSS_393	Y59
U16	VSS_358	VSS_394	Y6
U17	VSS_359	VSS_395	Y7
U18	VSS_360		

Sect 12/12

U26G BXT_P_SOC_BGA1296

B13	SPARE_9	NOCONNECT_16	M12
C13	SPARE_8	NOCONNECT_17	C15
L16	SPARE_7	NOCONNECT_18	F16
M16	SPARE_6	NOCONNECT_19	J16
E23	SPARE_5	NOCONNECT_20	D8
F23	SPARE_4	NOCONNECT_21	E8
R25	SPARE_3	NOCONNECT_22	H16
AB49	SPARE_2	NOCONNECT_23	C9
AC13	SPARE_11	NOCONNECT_24	F8
AB13	SPARE_10	NOCONNECT_25	E10
AM59	SPARE_1	NOCONNECT_26	E16
AM58	SPARE_0	NOCONNECT_27	F14
		NOCONNECT_28	F12
T51	NOCONNECT_1	NOCONNECT_29	H10
L14	NOCONNECT_2	NOCONNECT_30	H14
R19	NOCONNECT_3	NOCONNECT_31	H12
E6	NOCONNECT_4	NOCONNECT_32	A14
R17	NOCONNECT_5	NOCONNECT_33	C14
E3	NOCONNECT_6	NOCONNECT_34	M39
D4	NOCONNECT_7	NOCONNECT_35	P39
A60	NOCONNECT_8	NOCONNECT_36	R39
A61	NOCONNECT_9	NOCONNECT_37	R37
BJ2	NOCONNECT_10	NOCONNECT_38	C2
BG1	NOCONNECT_11	NOCONNECT_39	J29
P27	NOCONNECT_12	NOCONNECT_40	P25
A3	NOCONNECT_13	NOCONNECT_41	R30
M10	NOCONNECT_14	NOCONNECT_42	C63
B15	NOCONNECT_15	NOCONNECT_43	E63
		NOCONNECT_44	D2
		NOCONNECT_45	AP57

Section 7 of 12

R119 0_4 VNNSS_SENSE (29)

R7193, please close Ball AE47.

PROJECT : LI8G

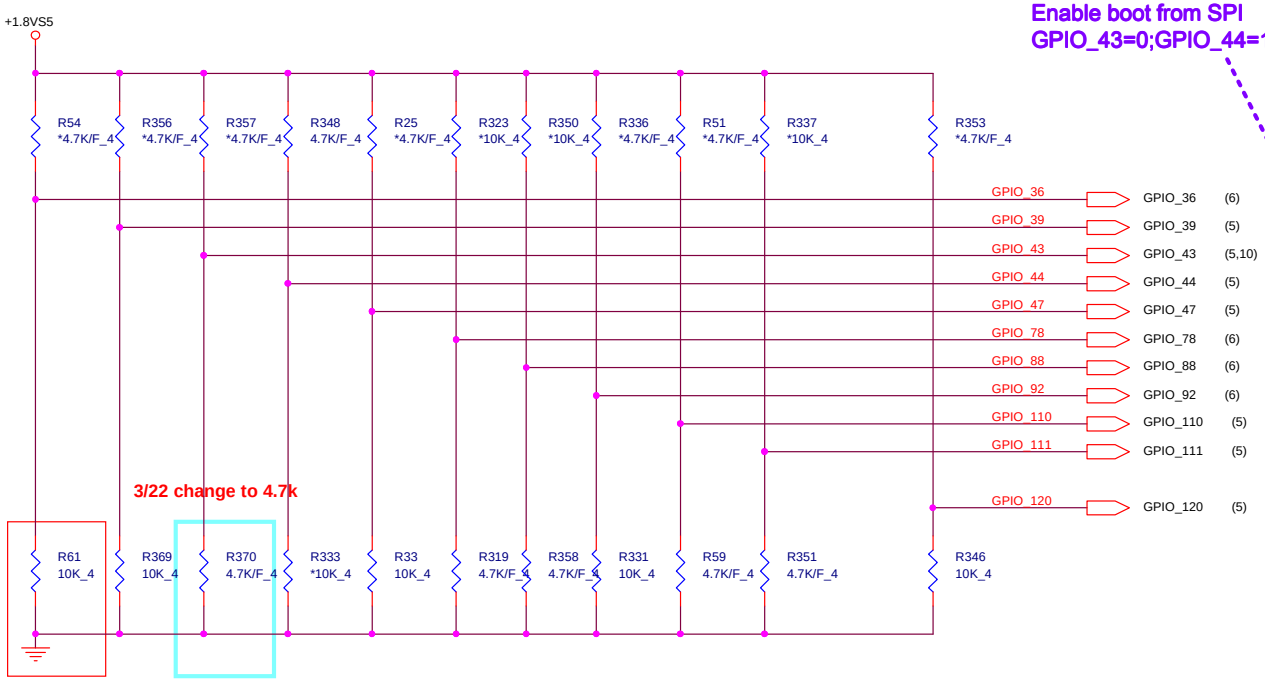
Quanta Computer Inc.

Size	Document Number	Rev
	BXTP (GND)	1A
Date: Thursday, September 08, 2016	Sheet 8 of 40	

HARDWARE STRAPS

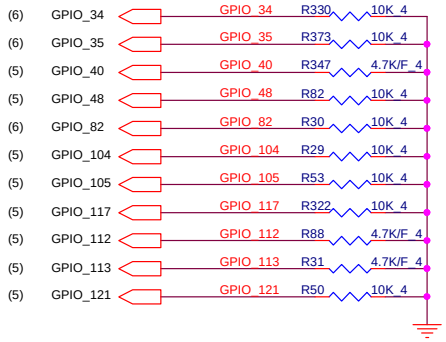
(3,4,5,6,7,10,12,14,15,21,29,31,33,35) +1.8VS5

Follow APL WoW36 ::
Enable boot from SPI
GPIO_43=0;GPIO_44=1



This rail must be 1.24V for A0 step.
Starting B-step, this rail can be 1.24V or 1.35V

Hardware Strap	Strap Description	Value
GPIO_36	VCC_1P24V_1P35V_A voltage select 0 = 1.24V 1 = 1.35V	0
GPIO_39	Enable CSE(TXE3.0) ROM Bypass 0 = Disable bypass 1 = Enable Bypass	0
GPIO_43	Allow eMMC as a boot source 0 = Disable 1 = Enable	0
GPIO_44	Allow SPI as a boot source 0 = Disable 1 = Enable	1
GPIO_47	Force DNX FW Load 0 = Do not force 1 = Force	0
GPIO_78	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V	0
GPIO_88	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
GPIO_92	SMBus No Re-Boot 0 = Disable (default) 1 = Enable	0
GPIO_110	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
GPIO_111	Boot BIOS Strap 0 = Boot from SPI 1 = Do not boot from SPI	0
GPIO_120	Top swap override 0 = Disable 1 = Enable	0

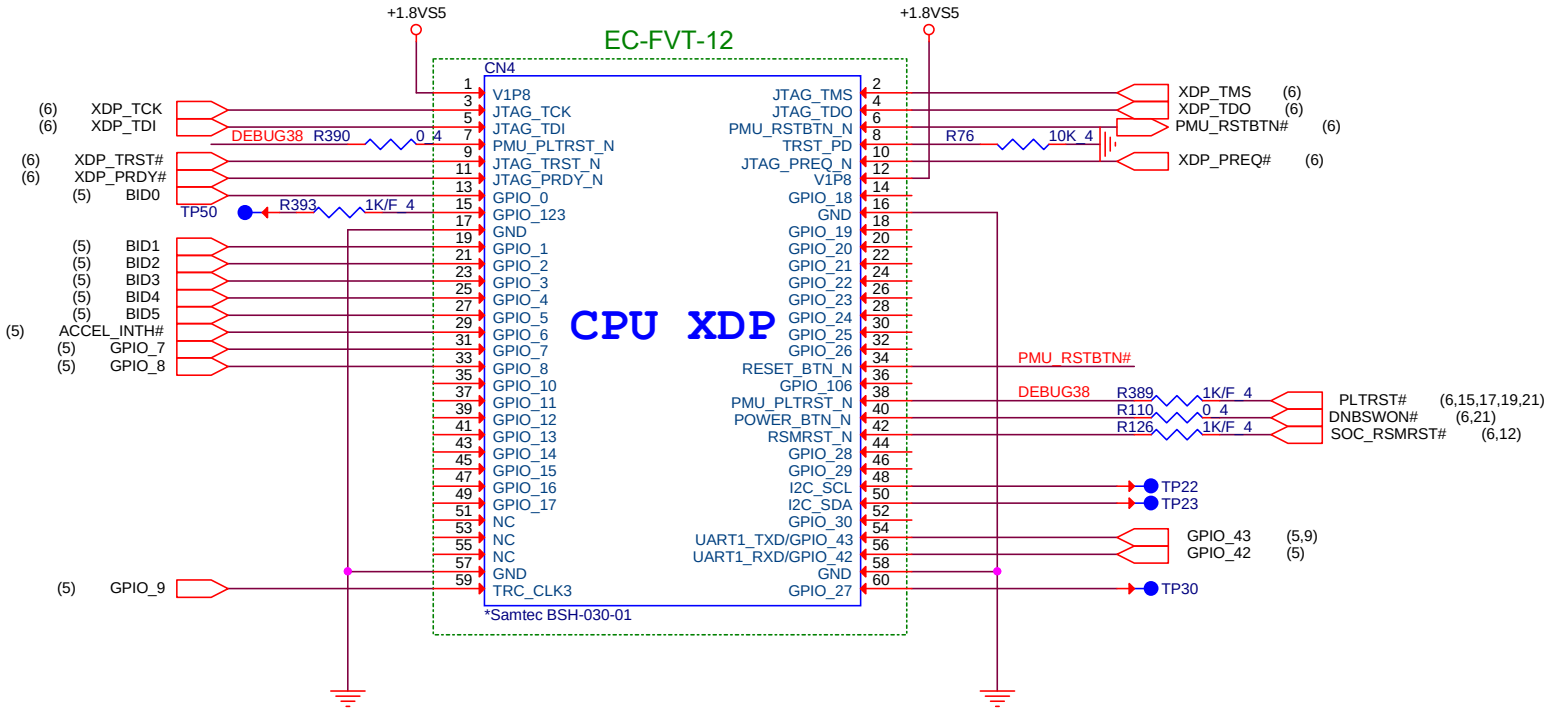


Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_40/GPIO_48/GPIO_104/GPIO_105/GPIO_112/GPIO_113/GPIO_117/GPIO_121 PD
GPIO_106/GPIO_123 PU

PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	HARDWARE STRAPS	1A
Date: Thursday, September 08, 2016	Sheet 9 of 40	

(3,4,5,6,7,9,12,14,15,21,29,31,33,35) +1.8VS5

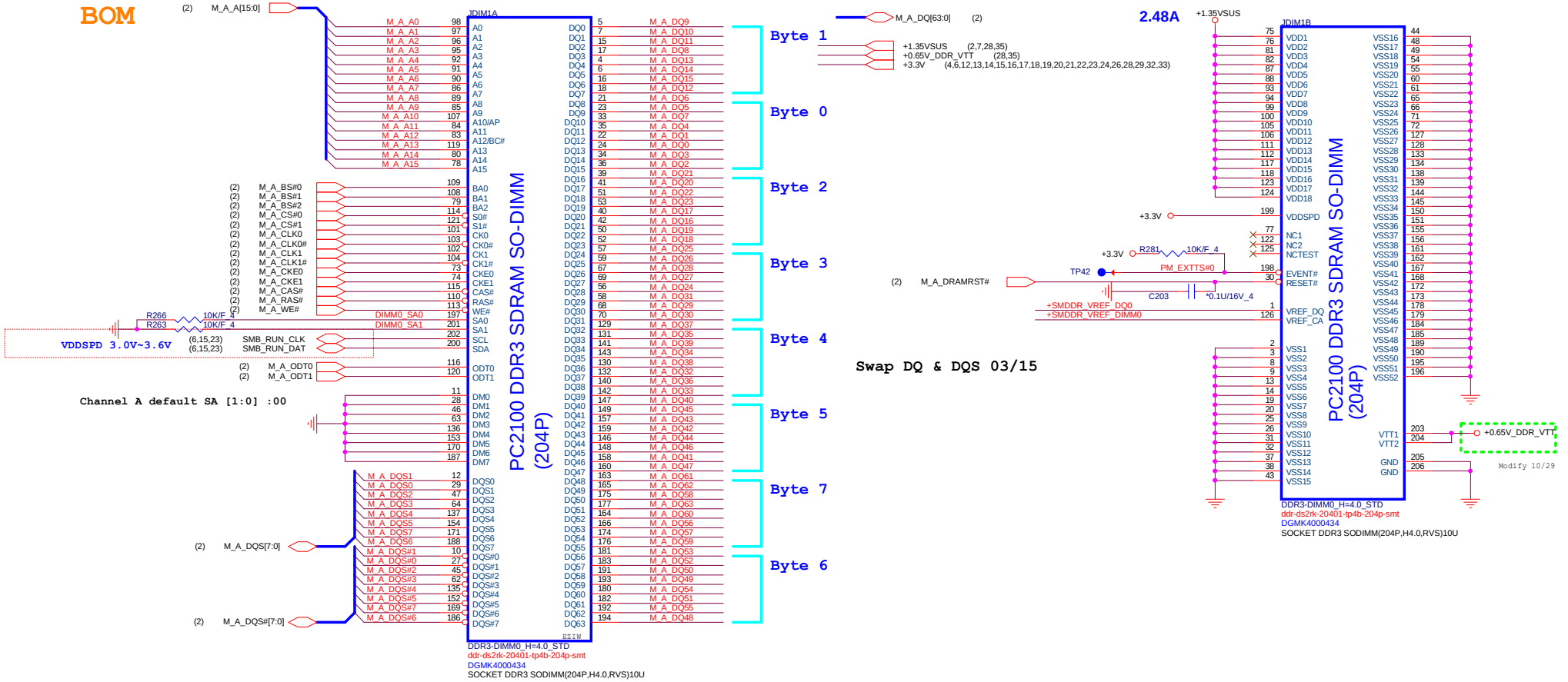


PROJECT : LI8G

Quanta Computer Inc.

Size	Document Number	Rev
	APL XDP	1A
Date: Thursday, September 08, 2016	Sheet 10 of 40	

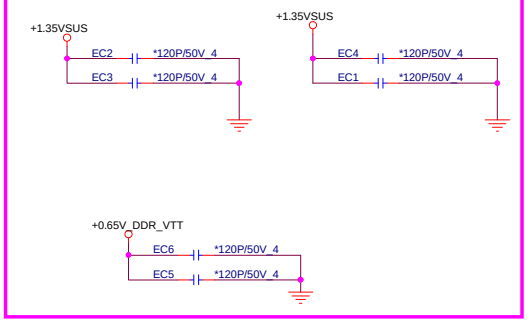
BOM



2.48A

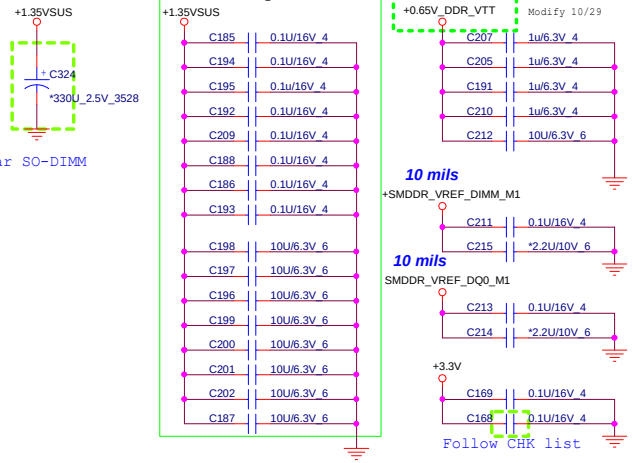
Swap DQ & DQS 03/15

For EMI RESERVE

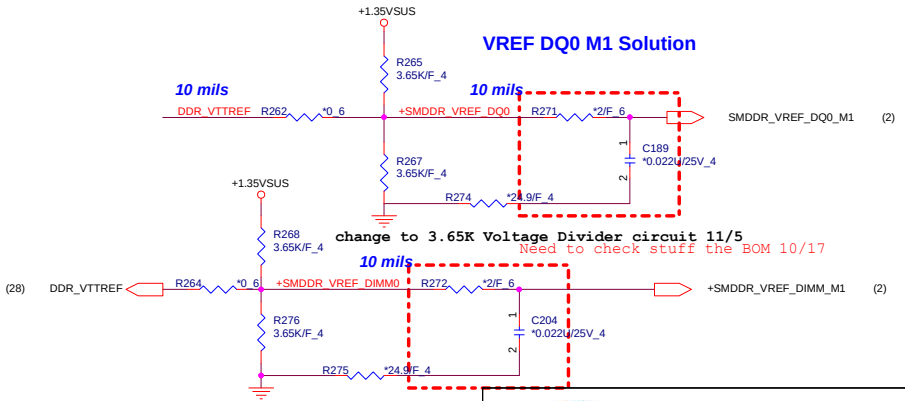


Place these Caps near So-Dimm0.

0.1uF/10uF 4pcs on each side of connector



VREF DQ0 M1 Solution

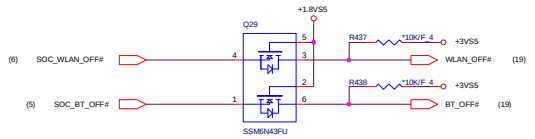


Correct CHA VREF_DQ/CA net name 10/29

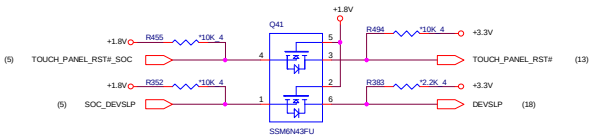
PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3L DIMM0-RVS(4.0H)CH-A	1A
Date: Thursday, September 08, 2016	Sheet 11 of 40	

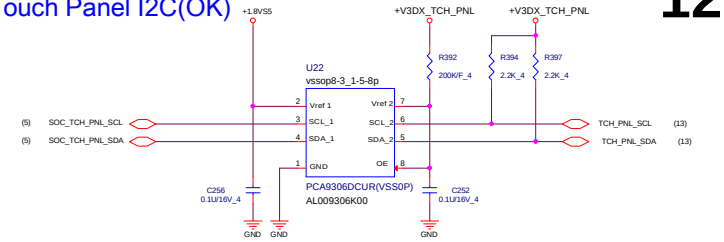
RF OFF#



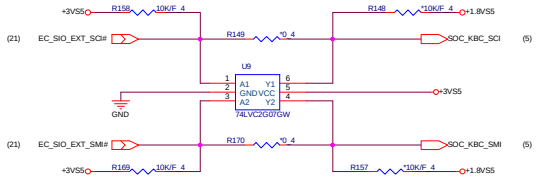
TCH_RST#/DEVSLP



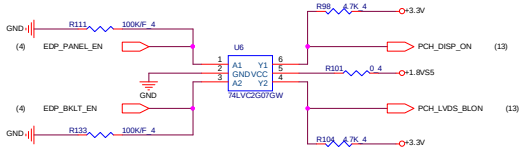
Touch Panel I2C(OK)



SCI#/SMI#(OK)

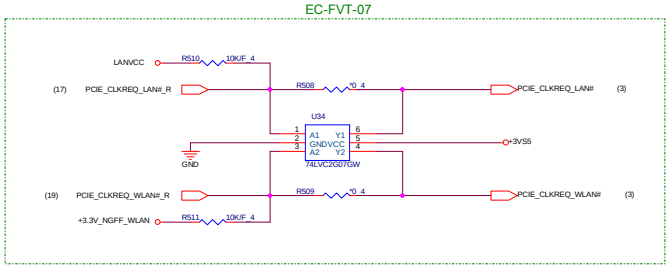


Disp ON/BL ON(OK)

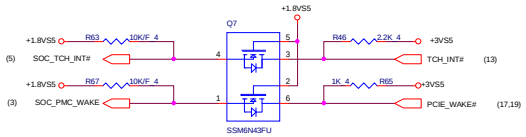


CLKREQ#

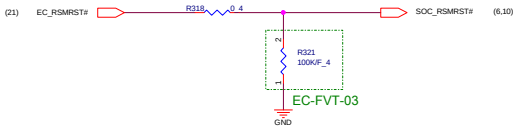
EC-FVT-07



INT



RSMRST#(OK)



PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	Level shift/Thermistor	1A

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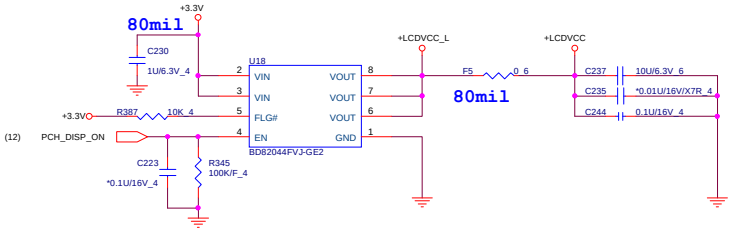
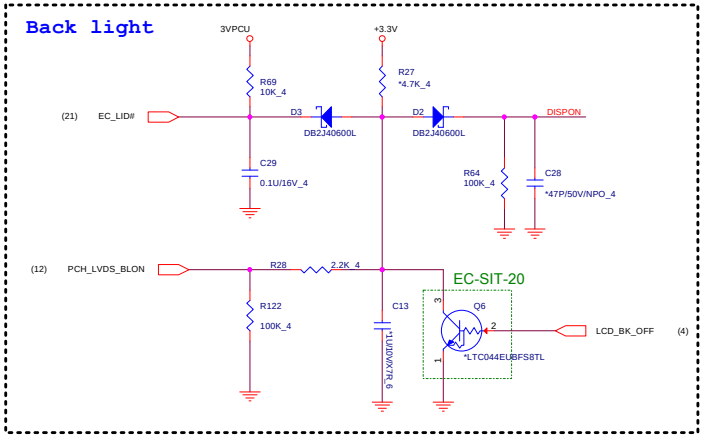
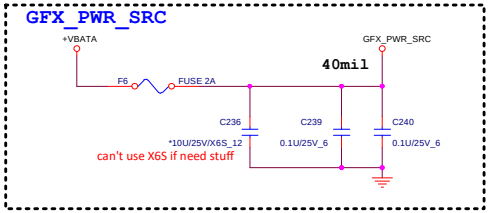
LCDVCC

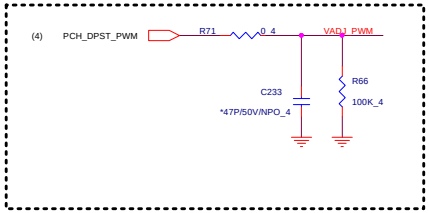


Back light

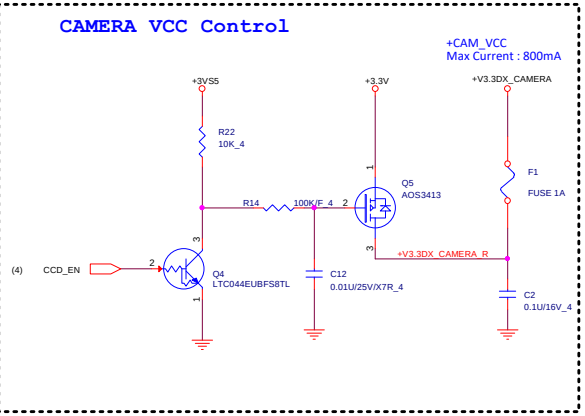


GFX_PWR_SRC

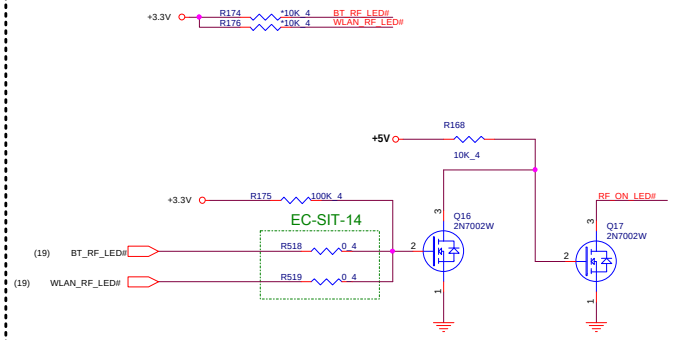




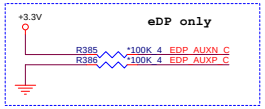
CAMERA VCC Control



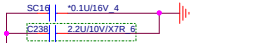
CCD+MIC+LOGO+WLAN LED CONN



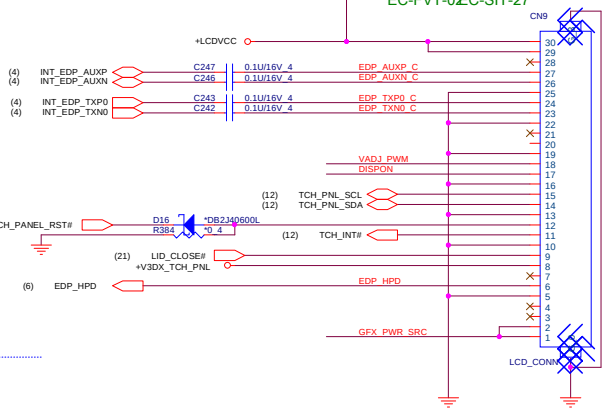
eDP only



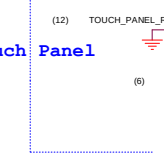
For ESD



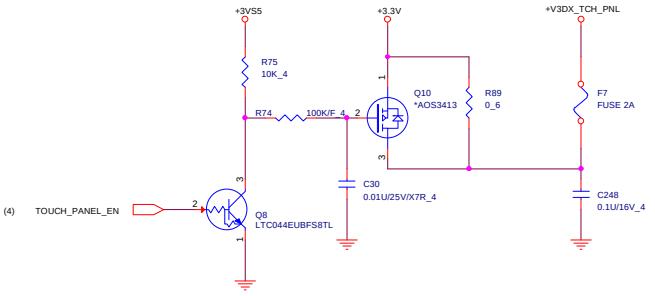
EC-FVT-02 EC-SIT-27

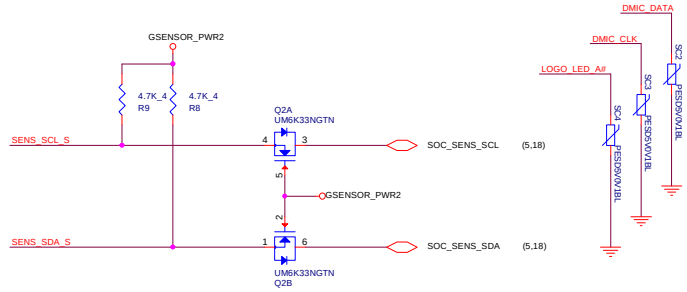


Touch Panel

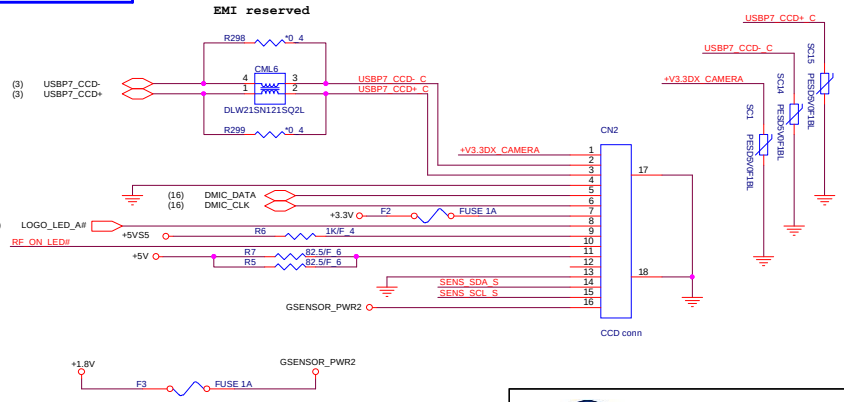


Touch Panel VCC Control





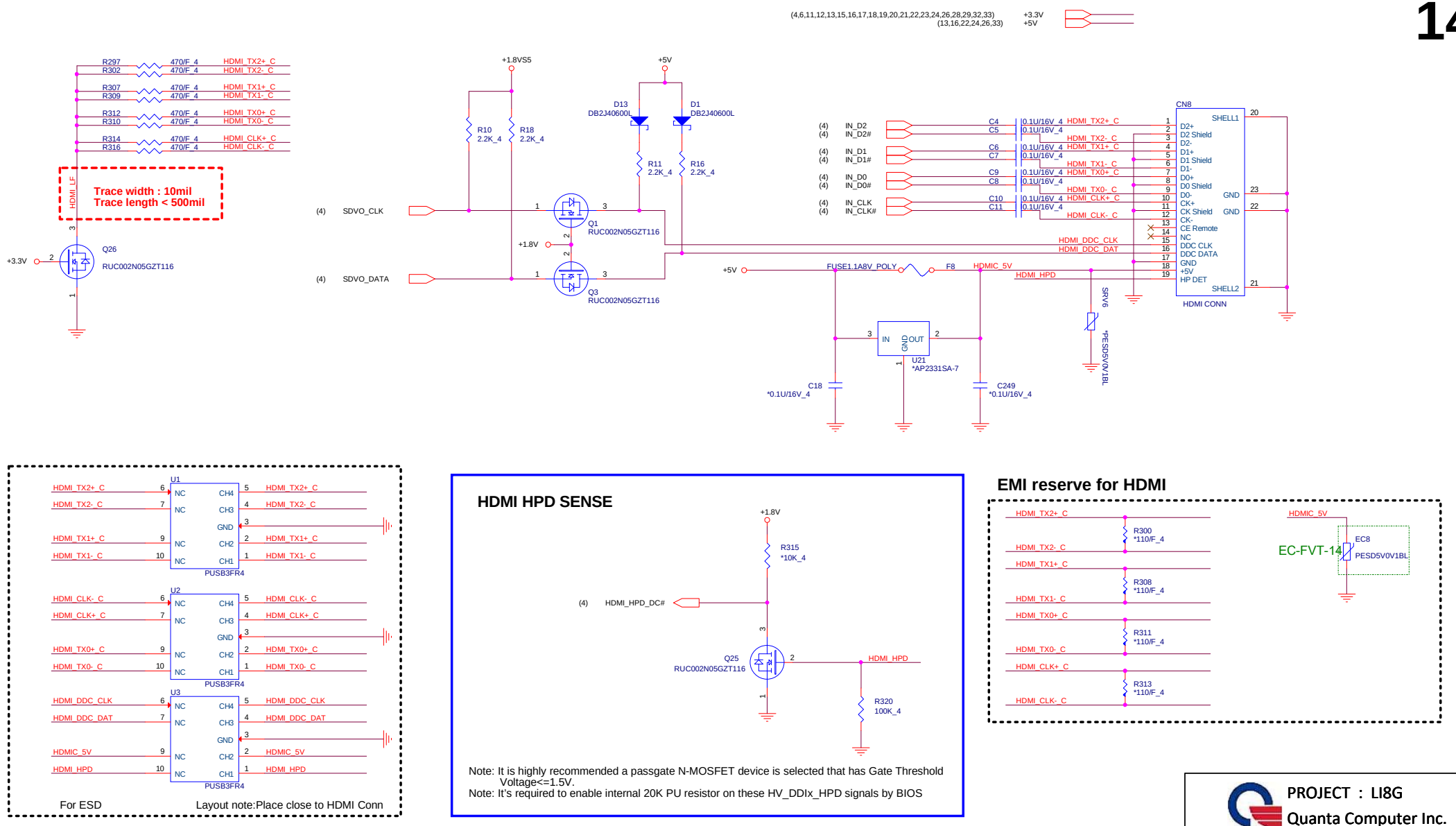
EMI reserved



PROJECT : LI8G

Quanta Computer Inc.

Size	Document Number	Rev
	LCD/CCD/Touch Panel/MIC	1A
Date: Monday, September 12, 2016	Sheet 13 of 40	



HDMI HPD SENSE

Note: It is highly recommended a passgate N-MOSFET device is selected that has Gate Threshold Voltage<=1.5V.
Note: It's required to enable internal 20K PU resistor on these HV_DDIx_HPD signals by BIOS

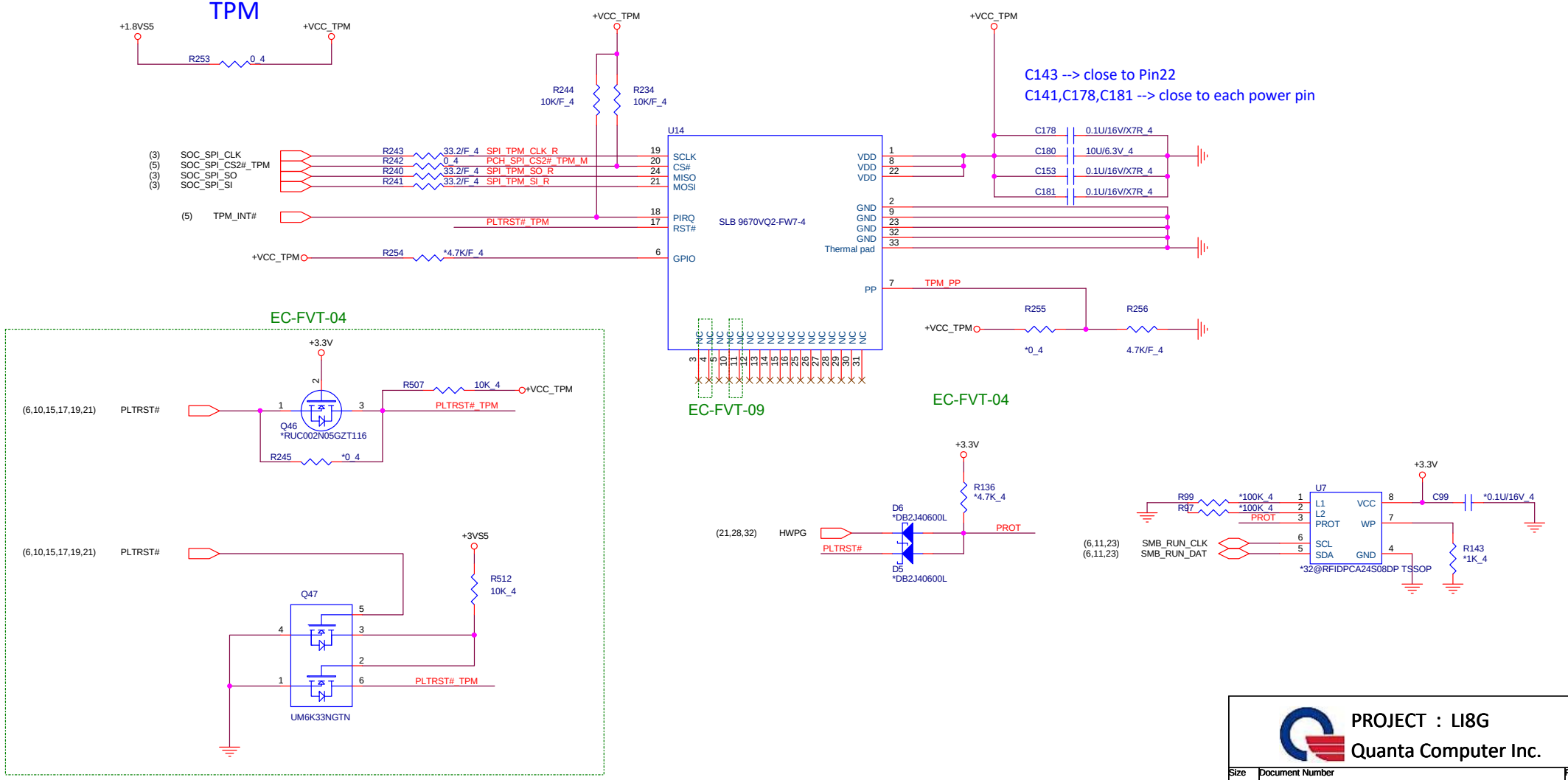
EMI reserve for HDMI

PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI CONN	1A
Date: Thursday, September 08, 2016	Sheet 14 of 40	

HDMI CONN

TPM

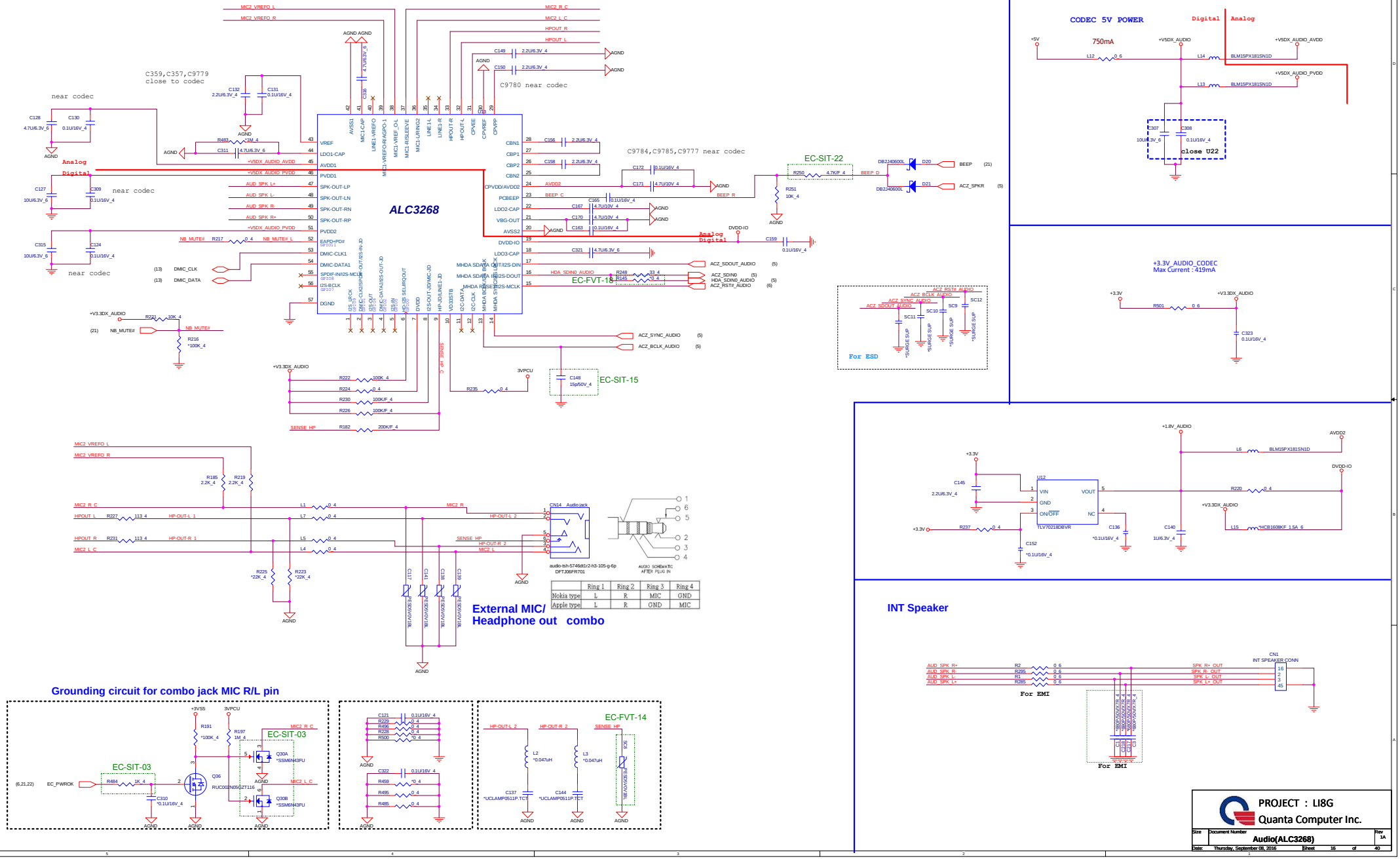


PROJECT : LI8G

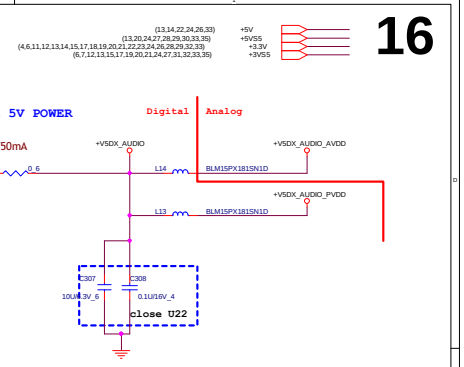
Quanta Computer Inc.

Size	Document Number	Rev
	TPM/RFID	1A
Date: Thursday, September 08, 2016	Sheet 15 of 40	

ALC3268

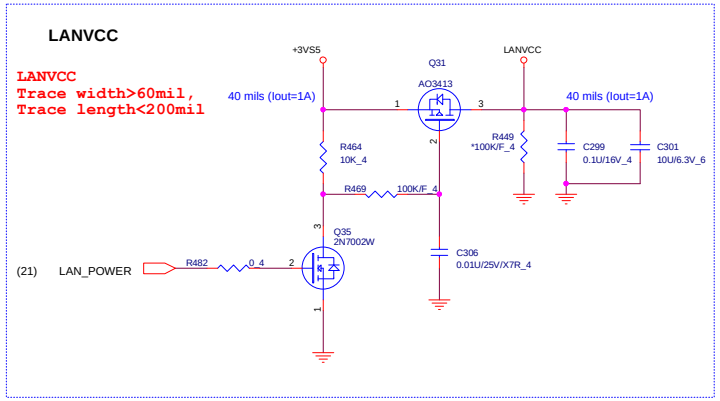


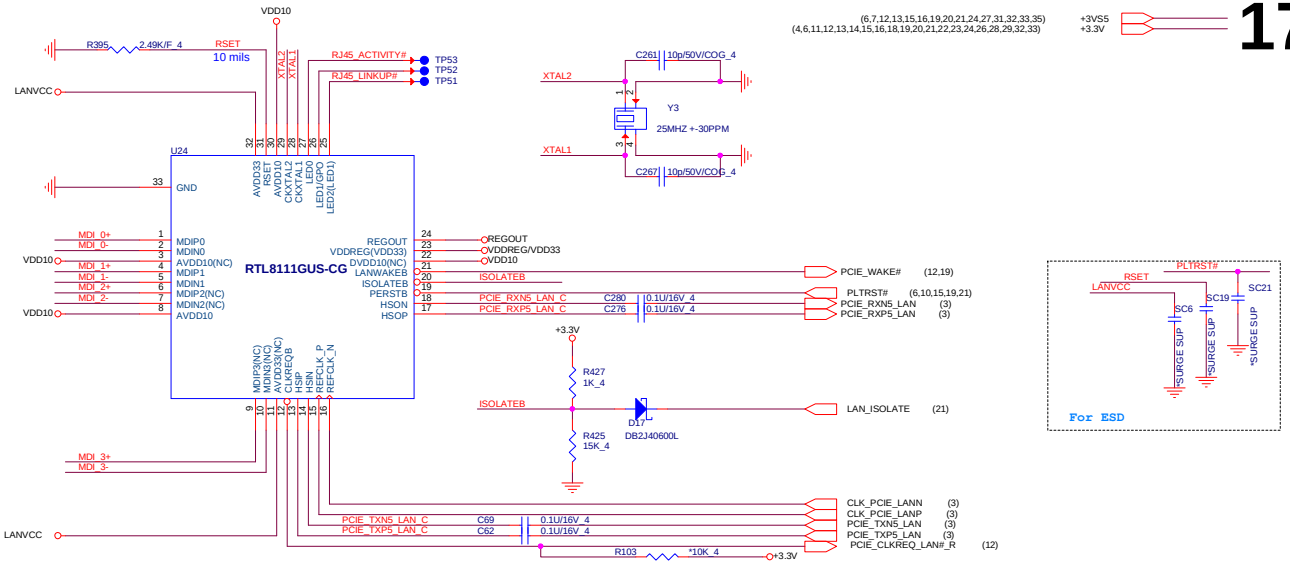
	Ring 1	Ring 2	Ring 3	Ring 4
Nokia type	L	R	MIC	GND
Apple type	L	R	GND	MIC

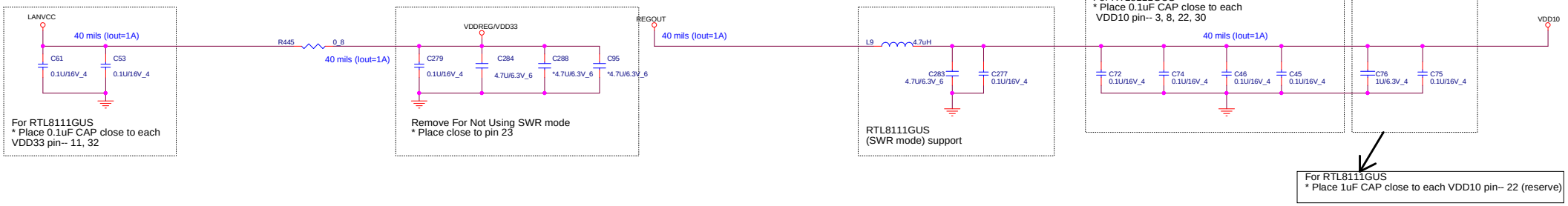


Quanta Computer Inc.	PROJECT : LI8G
Size	Document Number: Audio(ALC3268)
Rev	1A
Date: Thursday, September 08, 2016	Sheet 16 of 40

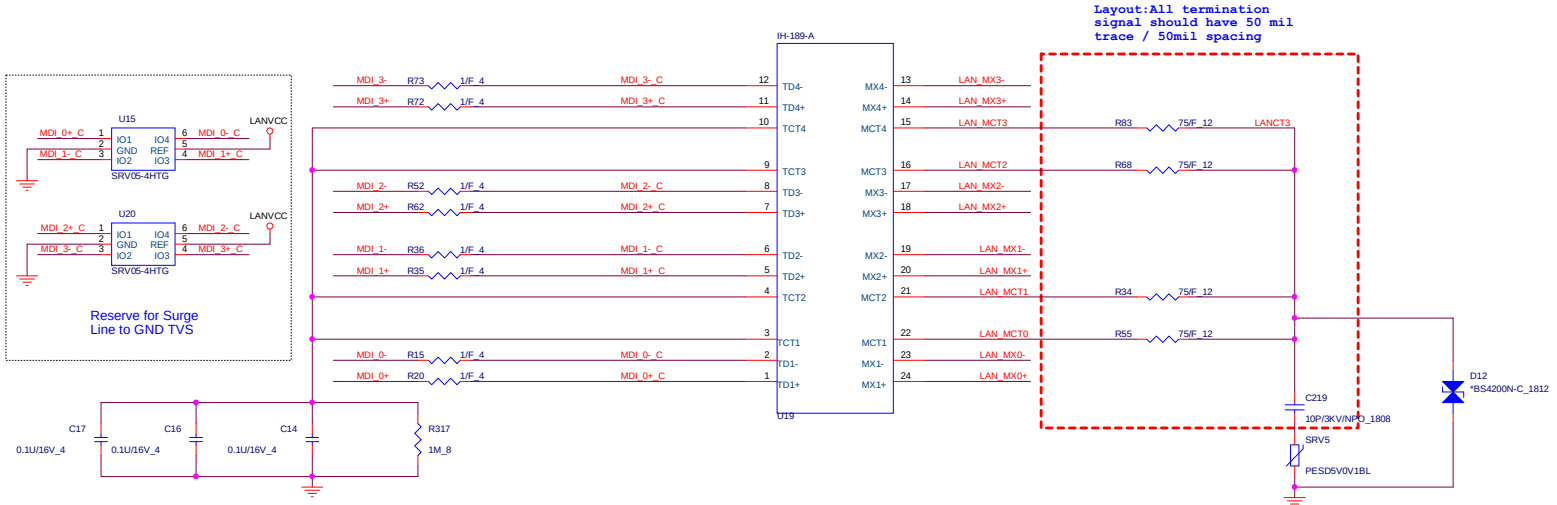
16



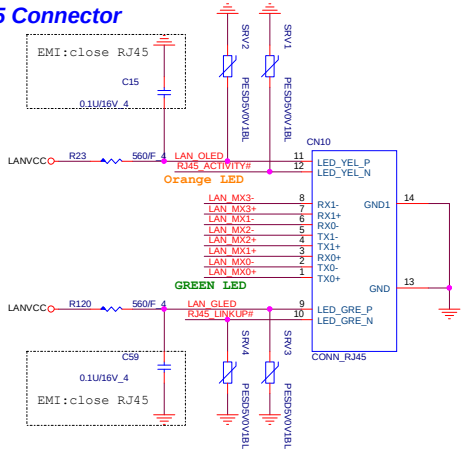




Tramsformer



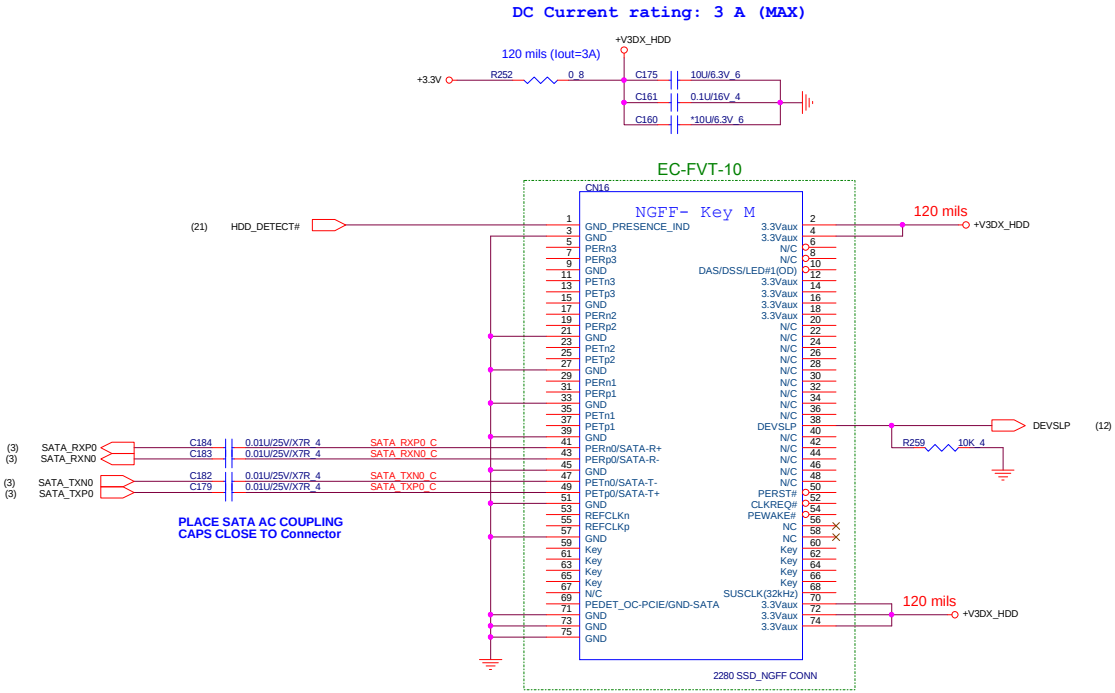
RJ45 Connector



PROJECT : LI8G
Quanta Computer Inc.

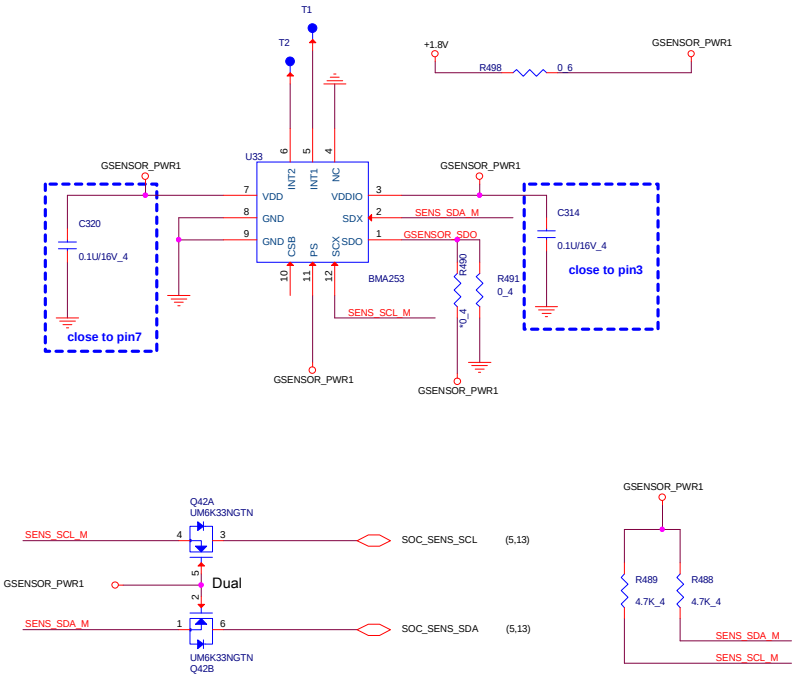
Size	Document Number	Rev
	LAN(RTL8111GUS)	1A
Date: Thursday, September 08, 2016	Sheet 17 of 40	

M.2 2280 SSD



(4,6,11,12,13,14,15,16,17,19,20,21,22,23,24,26,28,29,32,33) +3.3V

G-SENSOR For Yoga



PROJECT : LI8G

Quanta Computer Inc.

Size	Document Number	Rev
	M.2 2280/G-SENSOR	1A
Date: Thursday, September 08, 2016	Sheet 18 of 40	

(4,6,11,12,13,14,15,16,17,18,20,21,22,23,24,26,28,29,32,33) +3.3V
(6,7,12,13,15,16,17,20,21,24,27,31,32,33,35) +3VS5

NGFF WiFi/BT connector
M.2 2230

CN13

NGFF Slot-A SD

1	GND	3.3Vaux	2
3	USB_D+	3.3Vaux	4
5	USB_D-	LED#1 (OD)	6
7	GND	PCM_CLK (0/1.8V)	8
9	SDIO CLK(O)(0/1.8V)	PCM_SYNC (0/1.8V)	10
11	SDIO CMD(IO)(0/1.8V)	PCM_IN (0/1.8V)	12
13	SDIO DAT0(IO)(0/1.8V)	PCM_OUT (0/1.8V)	14
15	SDIO DAT1(IO)(0/1.8V)	LED#2 (OD)	16
17	SDIO DAT2(IO)(0/1.8V)	GND	18
19	SDIO DAT3(IO)(0/1.8V)	UART Wake(0/3.3V)	20
21	SDIO Wake(I)(0/1.8V)	UART Rx (0/1.8V)	22
23	SDIO Reset(O)(0/1.8V)	Key	24
25	Key	Key	26
27	Key	Key	28
29	Key	Key	30
31	Key	UART Tx (0/1.8V)	32
33	GND	UART CTS (0/1.8V)	34
35	PETp0	UART RTS (0/1.8V)	36
37	PETn0	RESERVED	38
39	GND	RESERVED	40
41	PERp0	RESERVED	42
43	PERn0	COEX3(?)(0/1.8V)	44
45	GND	COEX2(?)(0/1.8V)	46
47	REFCLKP0	COEX1(?)(0/1.8V)	48
49	REFCLKN0	SUSCLK(32kHz)(0/3.3V)	50
51	GND	PERST0#(0/3.3V)	52
53	CLKREQ0#(0/3.3V)	W_Disable#2(0/3.3V)	54
55	PEWake0#(0/3.3V)	W_Disable#1(0/3.3V)	56
57	GND	I2C DATA(0/3.3)	58
59	Reserved/PETp1	I2C CLK(0/3.3)	60
61	Reserved/PETn1	ALERT(0/3.3)	62
63	GND	RESERVED	64
65	Reserved/PERp1	RESERVED	66
67	Reserved/PERn1	RESERVED	68
69	GND	RESERVED	70
71	RESERVED	3.3Vaux	72
73	RESERVED	3.3Vaux	74
75	GND		

WiFi/BT_NGFF CONN

(3) USBP6_BT+
(3) USBP6_BT-

(3) PCIE_TXP4_WLAN — C115 0.1U/16V_4 — PCIE_TXP4_WLAN_C
(3) PCIE_TXN4_WLAN — C116 0.1U/16V_4 — PCIE_TXN4_WLAN_C
(3) PCIE_RXP4_WLAN
(3) PCIE_RXN4_WLAN
(3) CLK_PCIE_WLANP
(3) CLK_PCIE_WLANN
(12) PCIE_CLKREQ_WLAN#_R — R207 0_4 — MINICARD_PME#
(5) DEBUG_LPCCLK — R204 0_4
(5,21) LPC_LFRAME# — R206 0_4

+3.3V_NGFF_WLAN

EC-SIT-14

R171 *10K_4 — +3.3V_NGFF_WLAN — WLAN_RF_LED# (13)
R173 *10K_4 — +3.3V_NGFF_WLAN — BT_RF_LED# (13)

BT_OFF_R# — PLTRST# (6,10,15,17,21)
WLAN_OFF_R#

R218 0_4 — LPC_LAD0 (5,21)
R209 0_4 — LPC_LAD1 (5,21)
R205 0_4 — LPC_LAD2 (5,21)
R203 0_4 — LPC_LAD3 (5,21)

+3.3V_NGFF_WLAN
C98 0.1U/16V_4
C118 0.047U/10V_4
C135 0.1U/16V_4
C134 0.047U/10V_4
C113 4.7U/6.3V_6

Place caps close to connector.

+3.3V_NGFF_WLAN — +3.3V_NGFF_WLAN — R152 10K_4
Q18 LTC044EUBFS8TL
(12,17) PCIE_WAKE# — R161 0_4 — MINICARD_PME#
(21) SIO_WAKE_SCI# — R162 *0_4 — R153 *0_4

(12) WLAN_OFF# — D8 DB2J40600L — R131 10K_4 — +3.3V_NGFF_WLAN — WLAN_OFF_R#
(12) BT_OFF# — D7 DB2J40600L — R118 10K_4 — BT_OFF_R#

40 mils (Iout=1A)

EC-SIT-13

+3VS5
+3.3V — F10 FUSE 2A — +3.3V_NGFF_WLAN
F4 *FUSE 2A
40 mils (Iout=1A)

Q13 AOS3413
R109 10K_4
R117 100K/F_4
C78 0.01U/25V/X7R_4
Q14 2N7002W
(21) EC_WLAN_EN

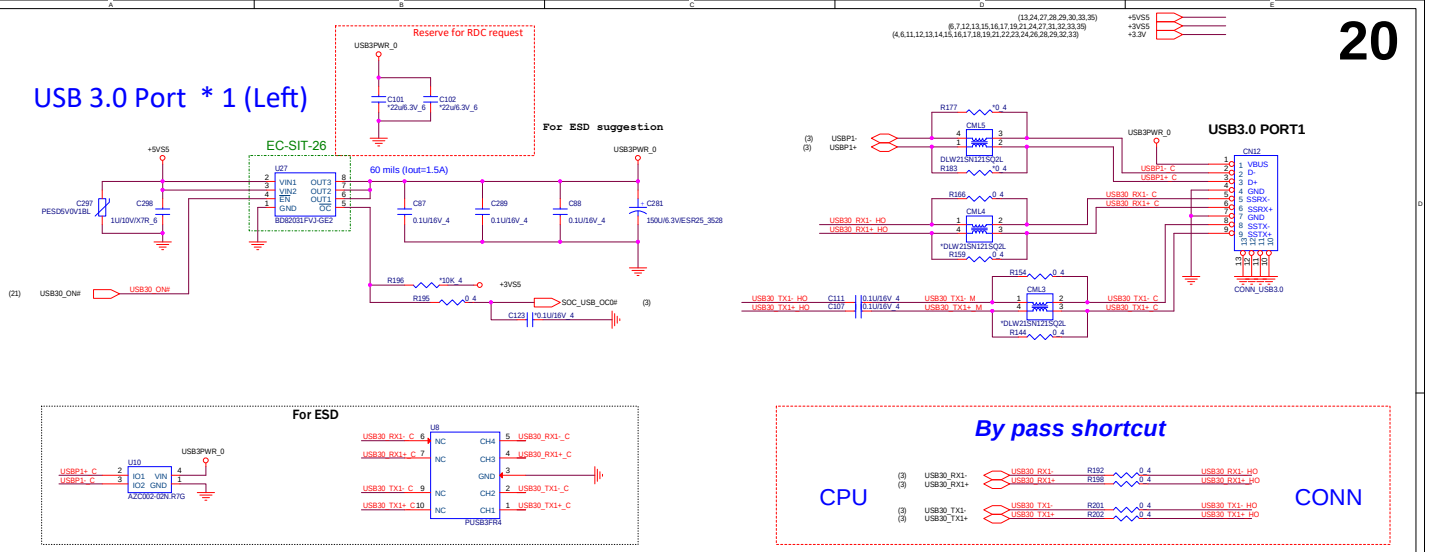
+3.3V_ NGFF_WLAN
Max Current : 1000mA

R142 *100K/F_4
C109 0.1U/16V_4

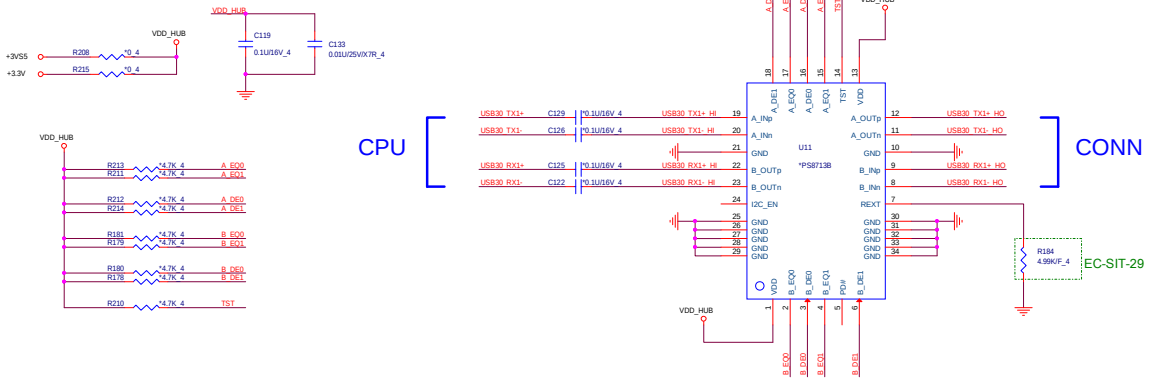
PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	Wifi/BT NGFF	1A
Date: Thursday, September 08, 2016	Sheet 19 of 40	

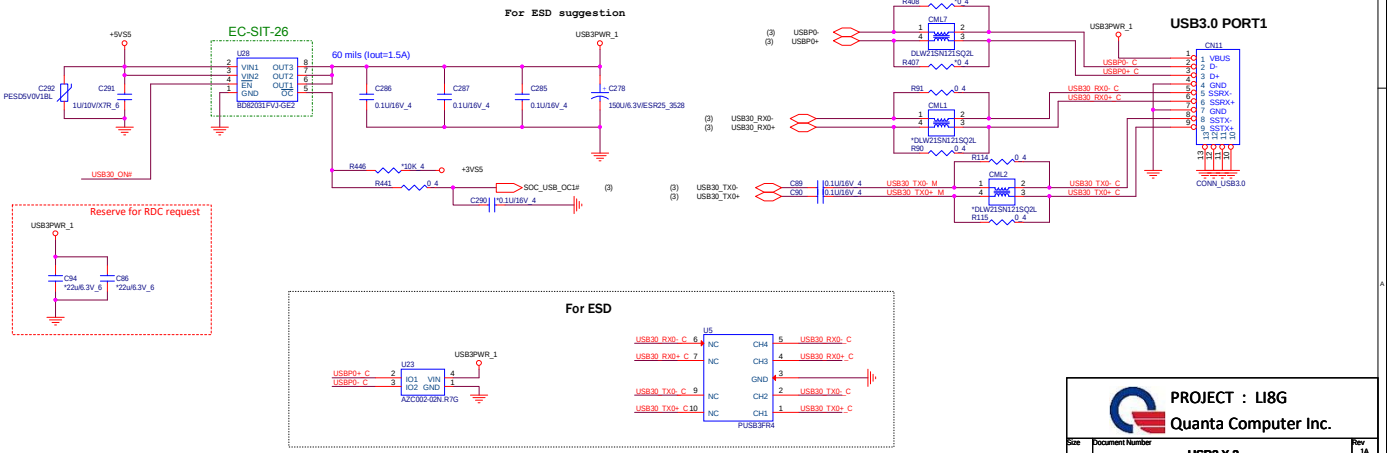
USB 3.0 Port * 1 (Left)



USB 3.0 Redriver (Reserved)

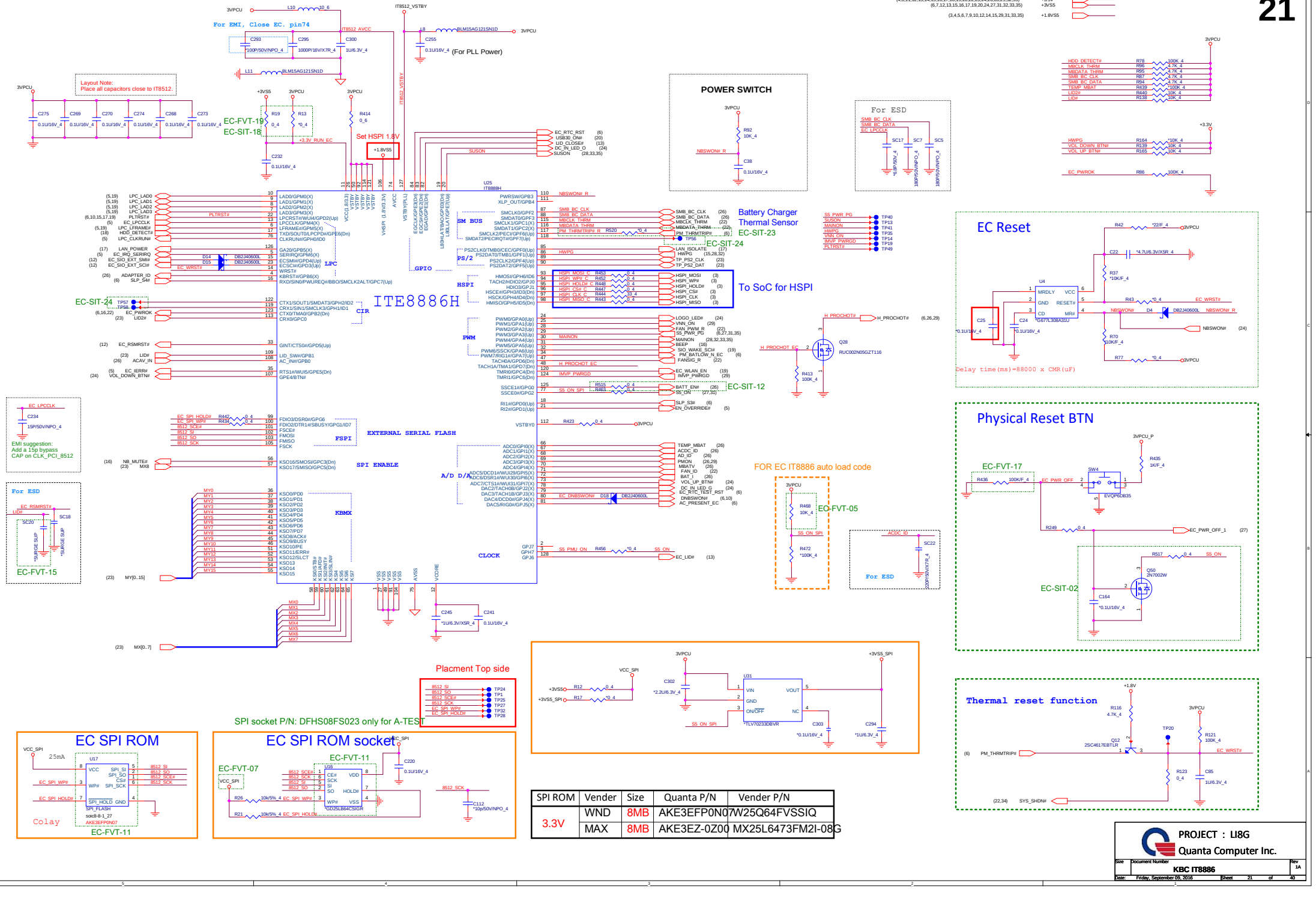


USB 3.0 Port * 1 (Right)



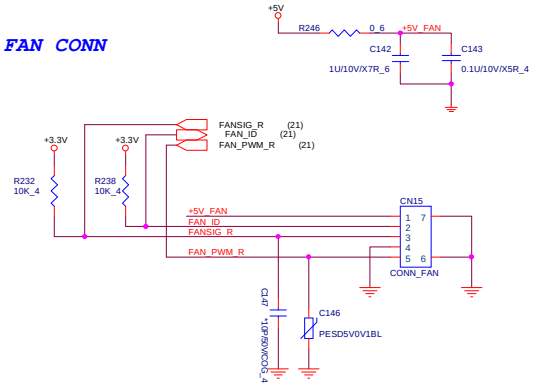
PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	USB3 X 2	1A
Date: Monday, September 12, 2016	Sheet 20 of 40	

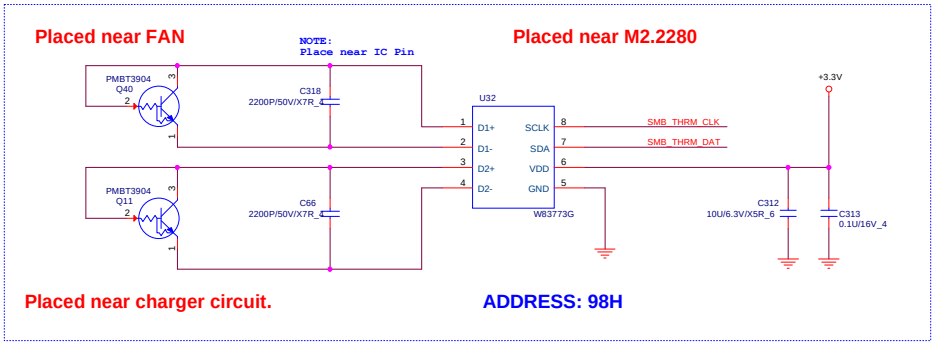


SPI ROM	Vender	Size	Quanta P/N	Vender P/N
3.3V	WND	8MB	AKE3EFP0N07	W25Q64FVSSIQ
	MAX	8MB	AKE3EZ-0Z00	MX25L6473FM2I-08G

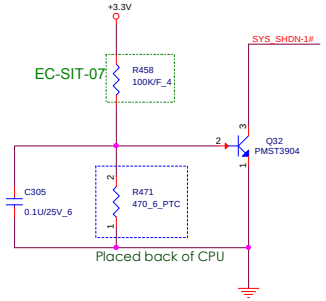
FAN CONN

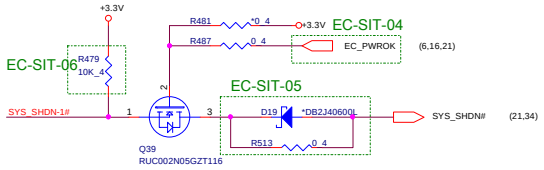


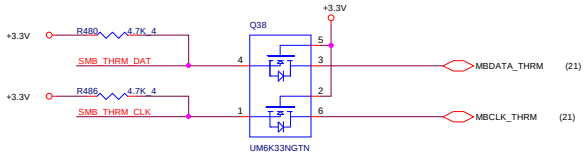
Thermal Sensor



CPU PTC circuit







To EC

PROJECT : LI8G

Quanta Computer Inc.

Size	Document Number	Rev
	FAN/Thermal	1A

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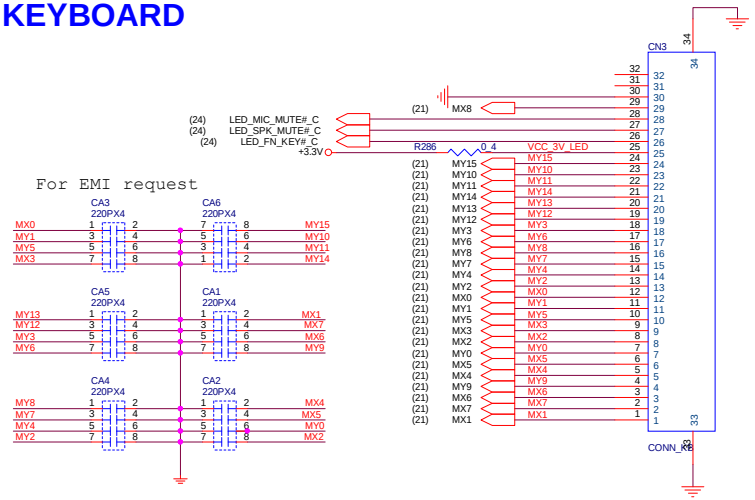
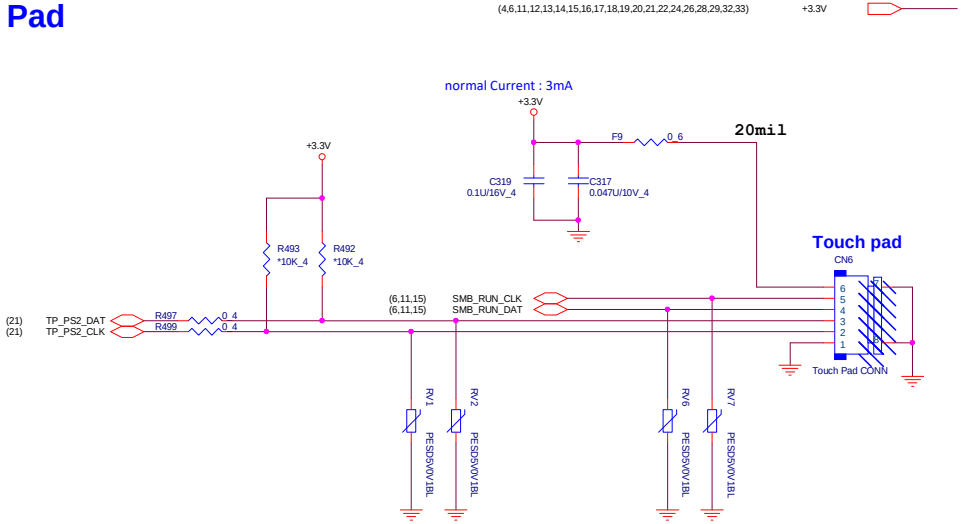
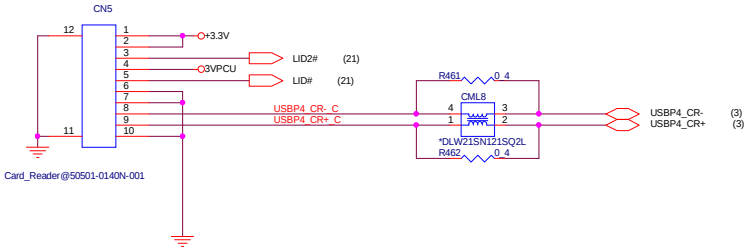
KEYBOARD



Click Pad



To Card Reader Board



PROJECT : LI8G

Quanta Computer Inc.

Size	Document Number	Rev
	KB/TP/DB	1A

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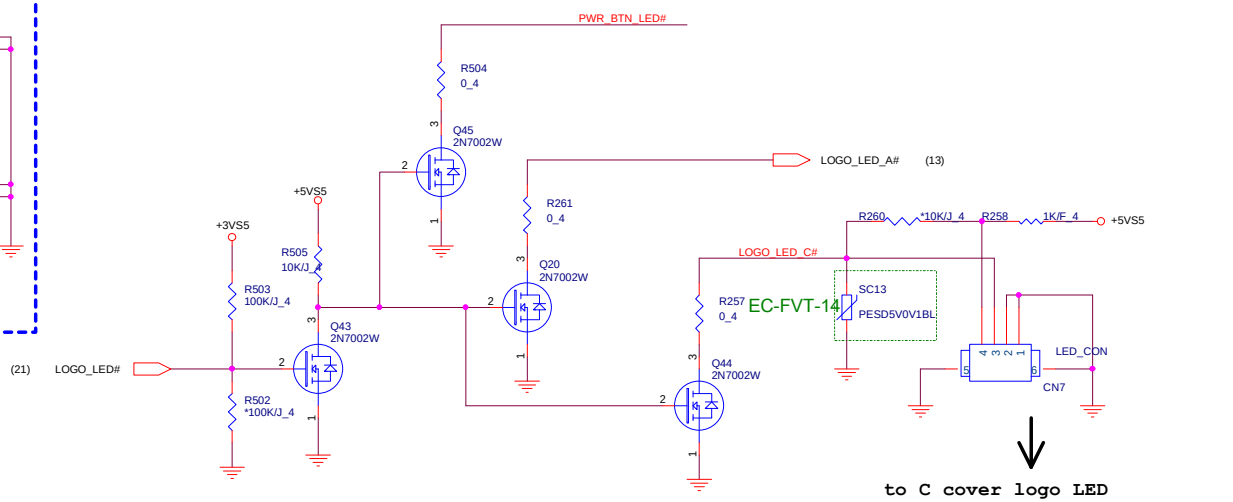
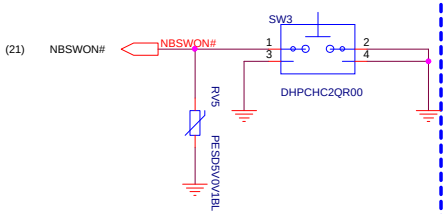
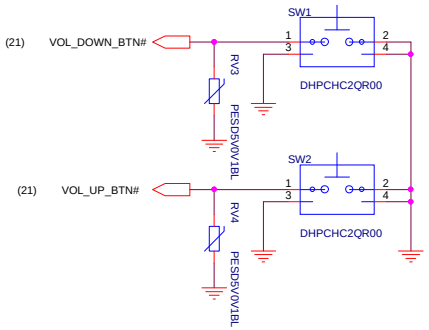
A/C cover & power button LED



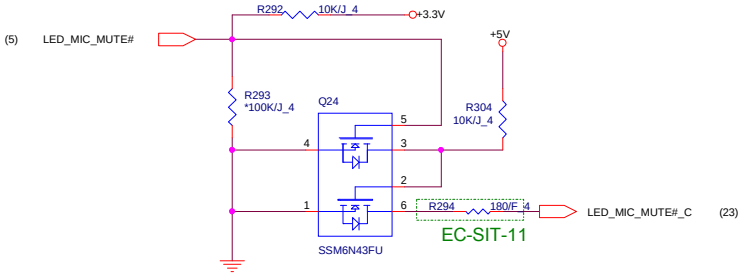
Power Switch



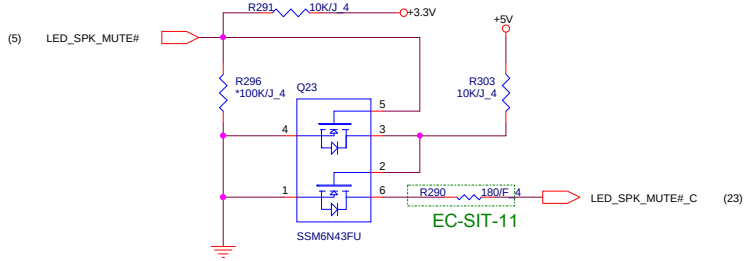
Volume up/down Switch



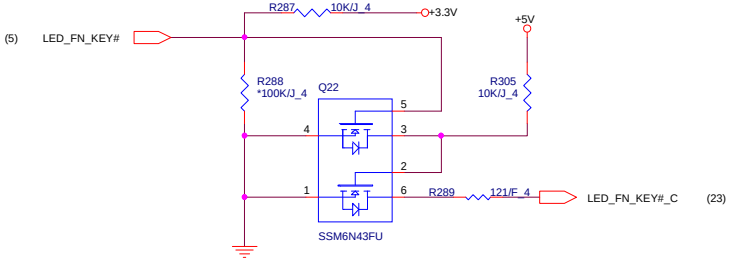
Mute LED

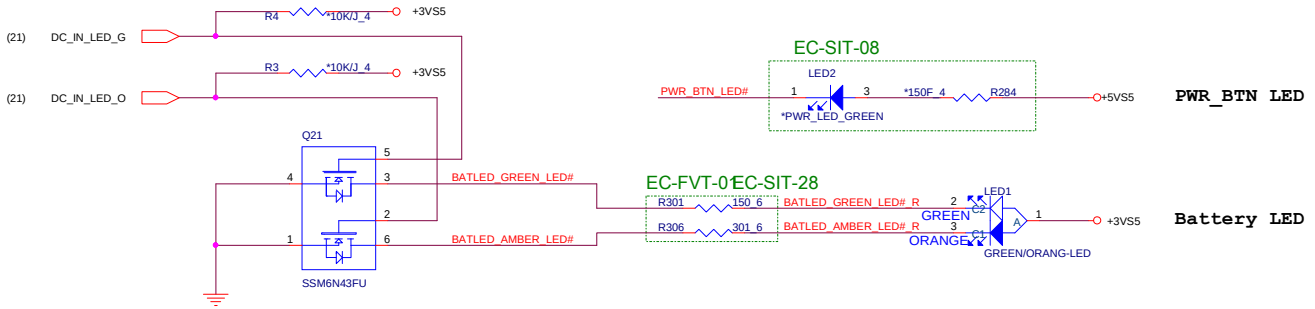


Speaker LED



Fn key LED

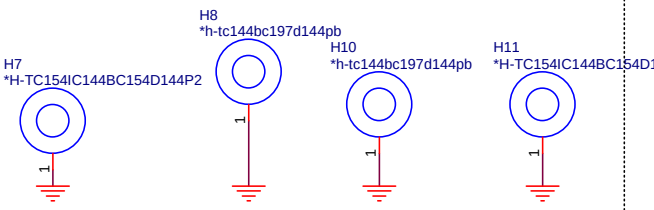




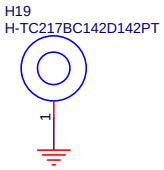
PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/SW	1A
Date: Monday, September 12, 2016	Sheet 24 of 40	

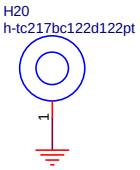
Hole For CPU bracket



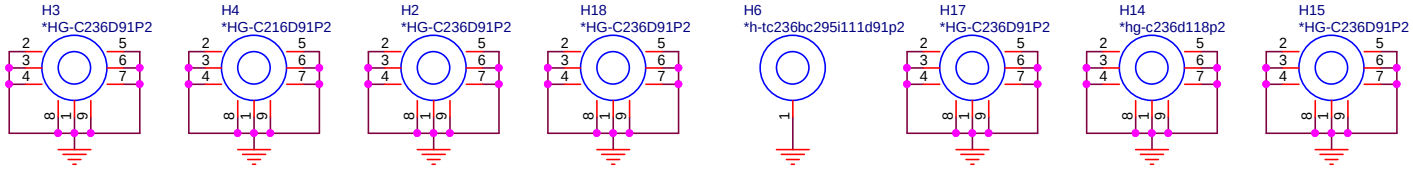
NGFF WLAN



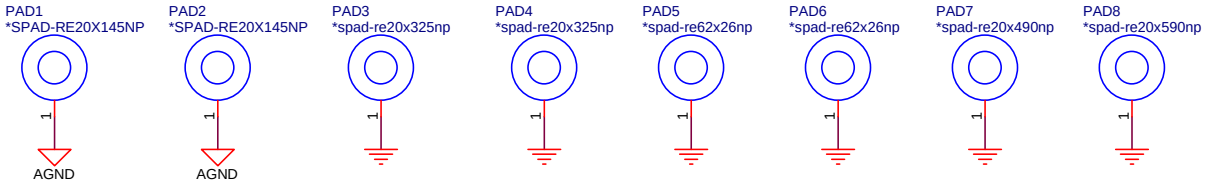
NGFF M.2 2280



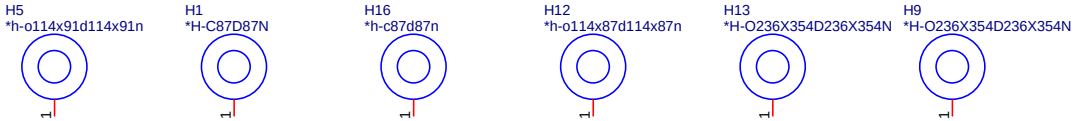
Boundary Hole



PAD



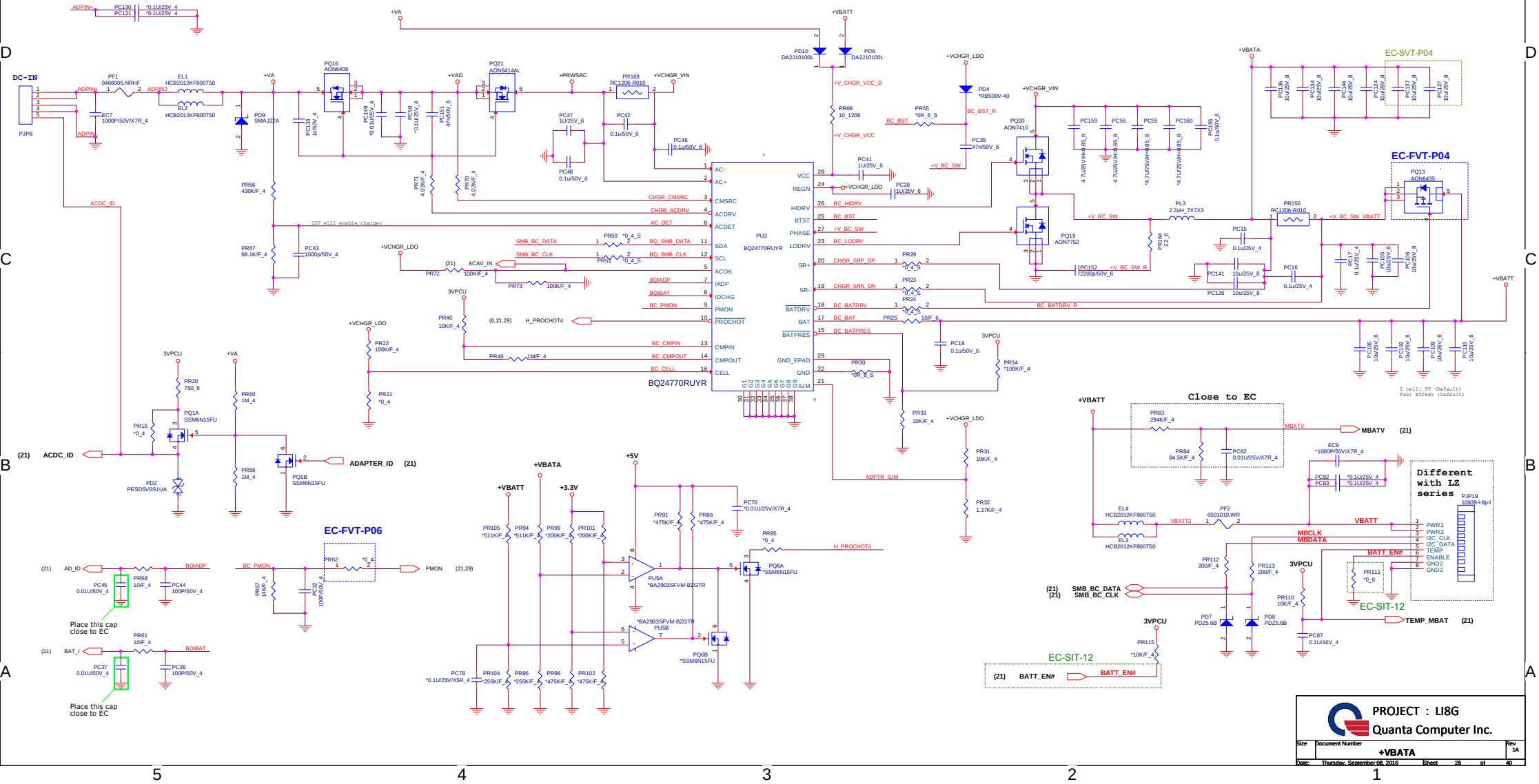
Non-PTH Hole



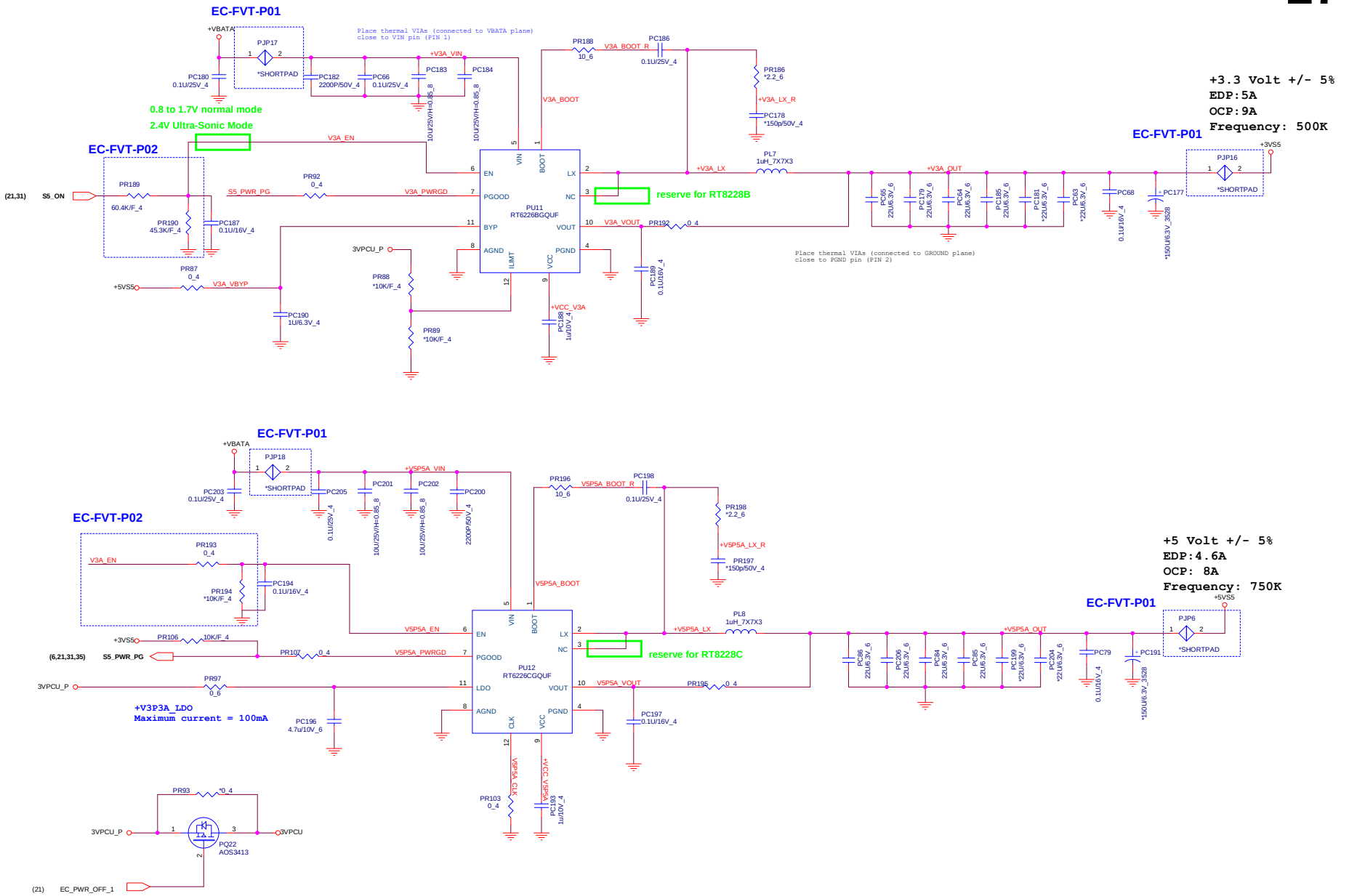
PROJECT : LI8G

Quanta Computer Inc.

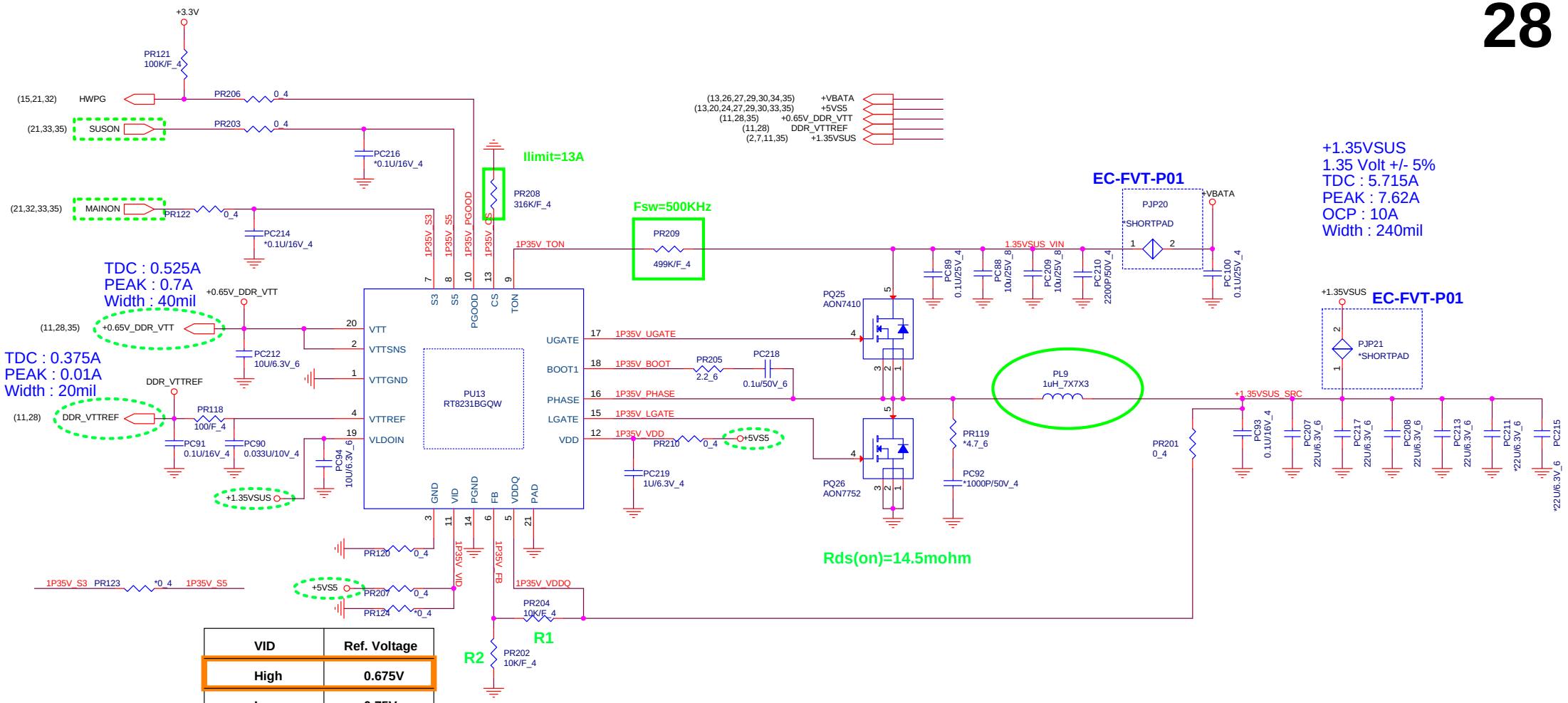
Size	Document Number	Rev
	Screw Hole	1A
Date: Thursday, September 08, 2016	Sheet 25 of 40	


DC-IN
PJP8
BQ24770RUYR
EC-FVT-P06
EC-FVT-P04
EC-SVT-P04
EC-SIT-12
Close to EC
Different with LZ series
Place this cap close to EC
Place this cap close to EC
PROJECT : LI8G
Quanta Computer Inc.
+VBATA
Thursday, September 08, 2016

VR PAGE: +V5A & +V3P3A



PROJECT : LI8G			
Quanta Computer Inc.			
Size	Document Number		Rev
	3/5VS5 - RT6226B/RT6226C		1A
Date: Thursday, September 08, 2016	Sheet 27	of	40



VID	Ref. Voltage
High	0.675V
Low	0.75V

Vout=Vref(0.675)X(1+(R1/R2))

OCP=10A
L ripple current
=(19-1.35)*1.35/(1u*500k*19)
=2.508A
Vtrip=10-(2.508/2)*14.5mohm
=126.817mV
Rlimit=126.817mV/5uA*10=253.63Kohm

DDR=1.35V
PR2032=10K/F_4
PR2033=10K/F_4

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	DDR(RT8231BGQW)	1A
Date: Thursday, September 08, 2016	Sheet 28 of 40	

Change pull up to +1.05V_S5

SVID_CLK : UP:85 ohm Series:95 ohm
SVID_ALERT : UP:68 ohm Series:220 ohm
SVID_DATA : UP:170 ohm Series:20 ohm

IMVP8 VR Controller

Rail A (1(phase)) +VCCGI
Rail C (1(phase)) +VNN

Add S5_ON for VNN sequence
Check VR Sequence

Double Check Rail B Non-Usage Pin

EC-FVT-P03
PU1
ISL95859AHRTZ-T

Rail C
Rail A

Close to VNN Choke
Close to VCCGI Choke
Close to VCCGI MOS

EC-SIT-P02

10/20 Modify VNN sense resistor
10/23 Modify VNN sense resistor
10/27 Modify VNN sense resistor
10/20 Modify VCCGI sense resistor

20160526
20160526

APL VR (1+1 Phase)

+VCCGI	+VNN
Icc Max: 21A	Icc Max: 4.8A
Icc TDC: 18A	Icc TDC: N/A
Vboot: 0V	Vboot: 1.05V
OCP: 25A	OCP: 8A
Fsw: 750KHZ	Fsw: 750KHZ

VCCGI L/L: :
R_DC_LL: 6mV/A
R_AC_LL: 6mV/A

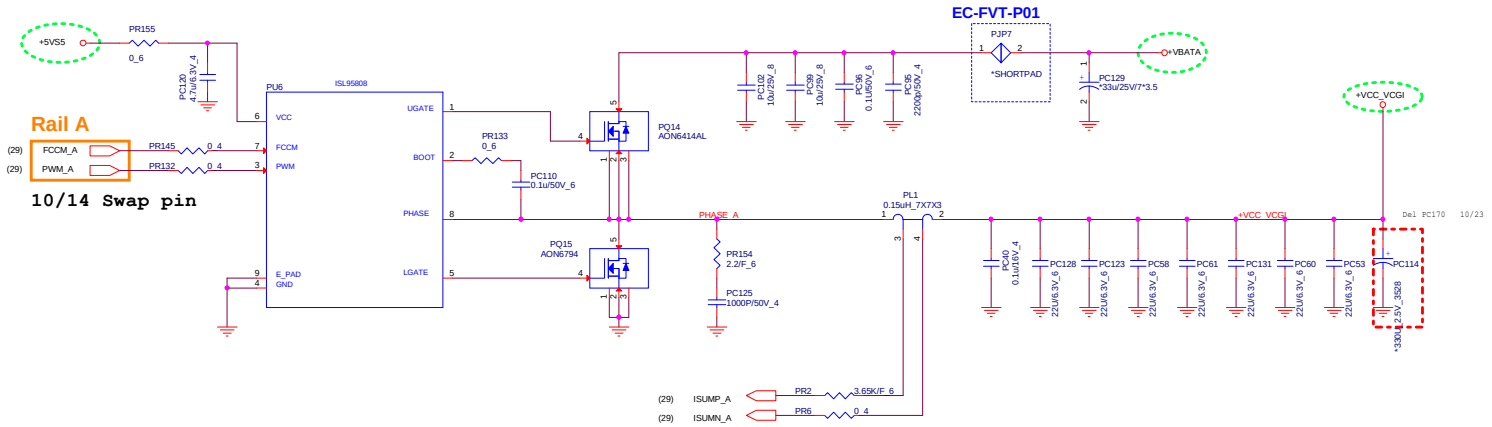
PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	CPU_CORE (ISL95859)	1A

Date: Monday, September 12, 2016 Sheet 29 of 40

(13,26,27,28,29,34,35) +VBATA
(7,29) +VCC_VCGI
(7,29) +VNN
(13,20,24,27,28,29,33,35) +5VS5

VCCGI



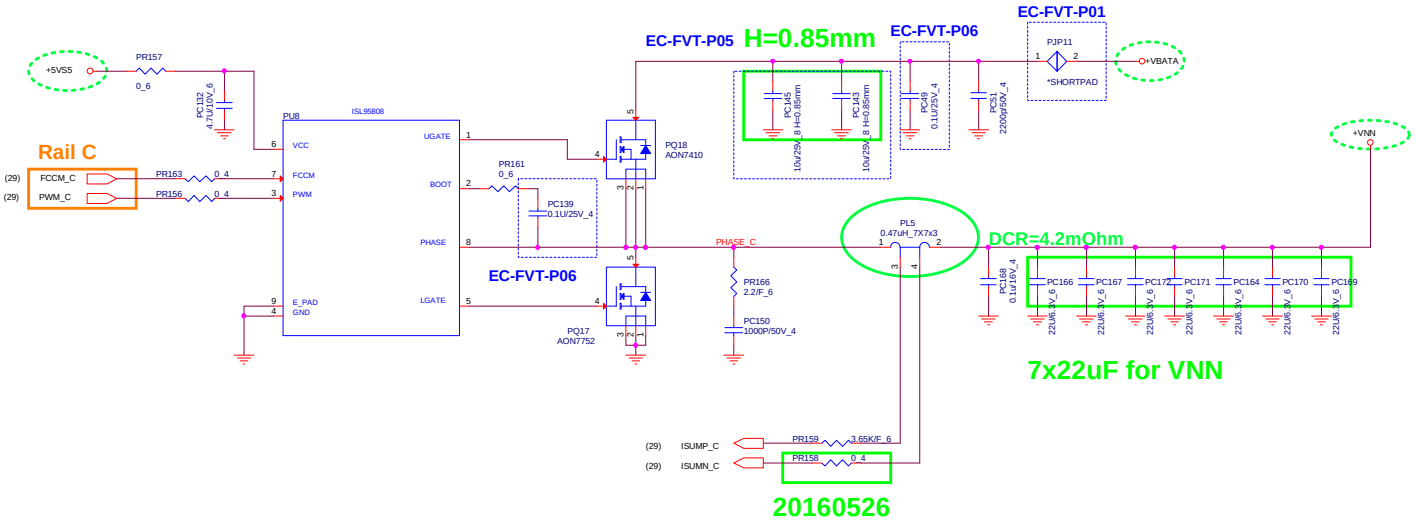
+VCCGI

Icc Max: 21A
Icc TDC: 18A
Vboot: 0V
OCP: 25A
Fsw: 750KHZ

VCCGI L/L: :

R_DC_LL: 6mV/A
R_AC_LL: 6mV/A

VNN



+VNN

Icc Max: 4.8A
Icc TDC: N/A
Vboot: 1.05V
OCP: 8A
Fsw: 750KHZ

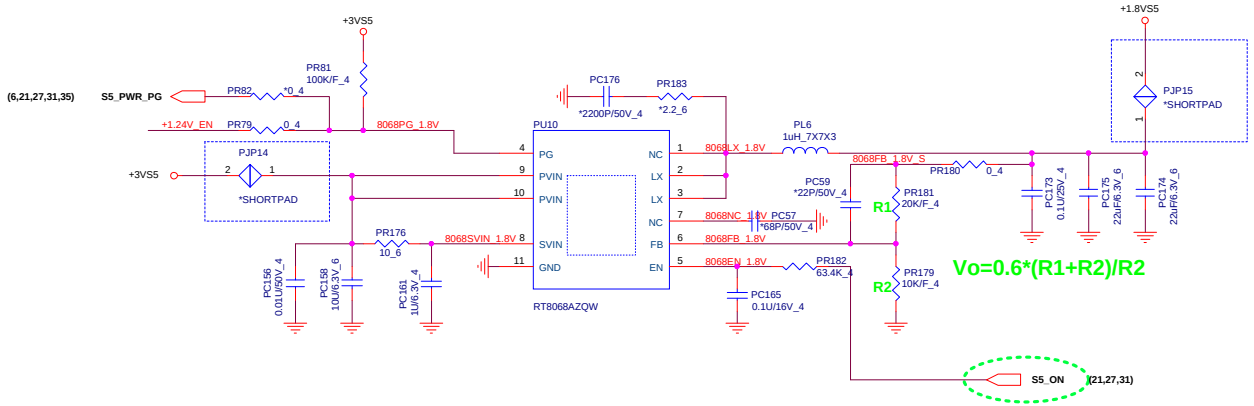
PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	+VCCGI / +VNN	1A

Date: Friday, September 09, 2016 Sheet 30 of 40

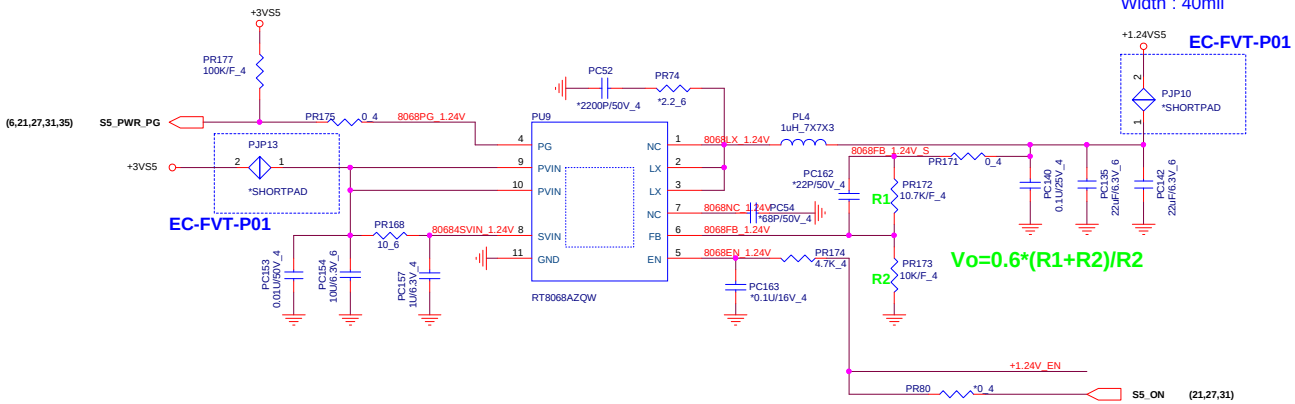
+1.8V_S5
1.8Volt +/- 5%
TDC : 0.315A
PEAK : 0.42A
Width : 20mil

Modify +1.8V_S5 PG pull up to +3V_S5 10/29



+1.24V_S5
1.24Volt +/- 5%
TDC : 0.975A
PEAK : 1.3A
Width : 40mil

Modify +1.24V_S5 PG pull up to +3V_S5 12/24



Change +1.24VSUS EN for Apollo Lake power sequence
10/29

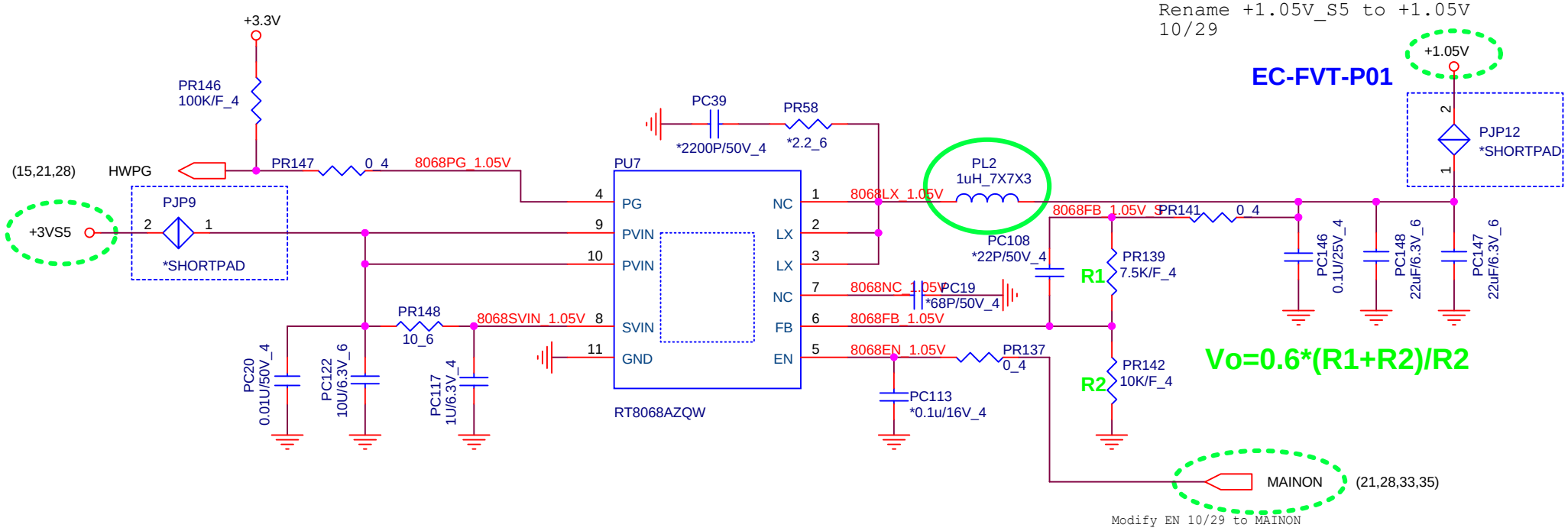
PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	+1.8VS5 /+1.24VS5	1A
Date: Thursday, September 08, 2016	Sheet 31 of 40	

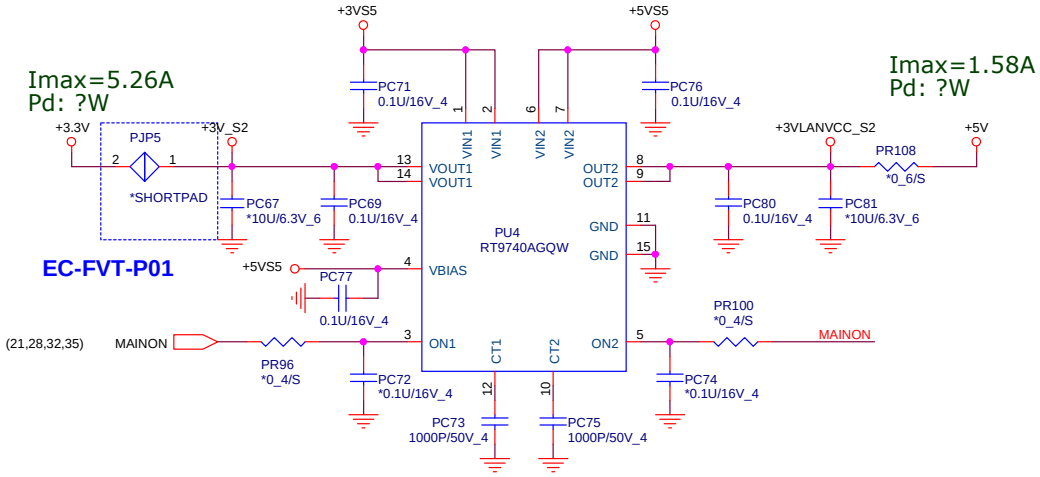
+1.05V_S5
1.05Volt +/- 5%
TDC : 2.025A
PEAK : 2.7A
Width : 100mil

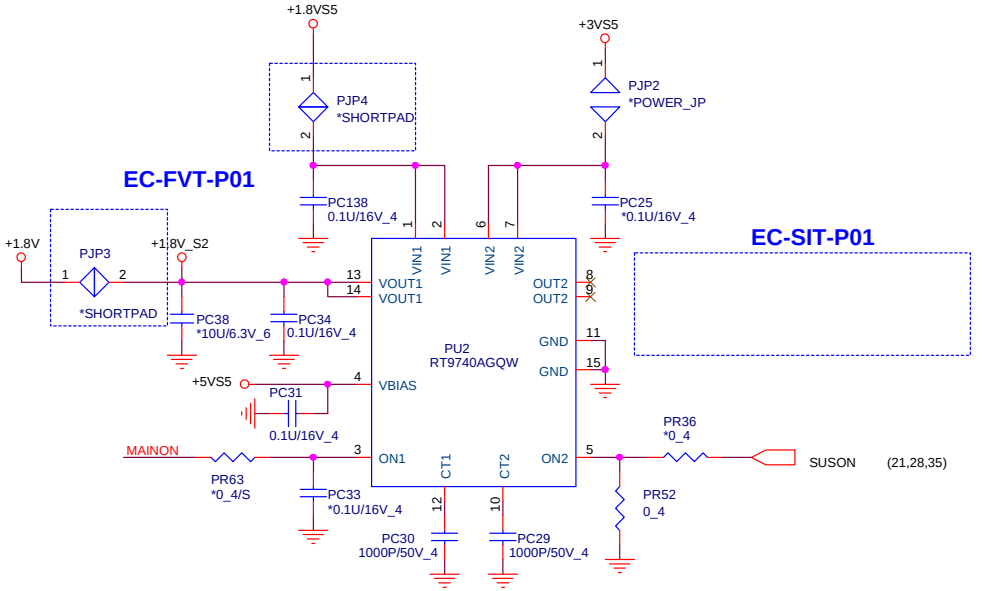
Rename +1.05V_S5 to +1.05V
10/29

EC-FVT-P01



PROJECT : LI8G		
Quanta Computer Inc.		
Size	Document Number: +1.05V (RT8068AZQW)	Rev 1A
Date: Thursday, September 08, 2016	Sheet 32 of 40	

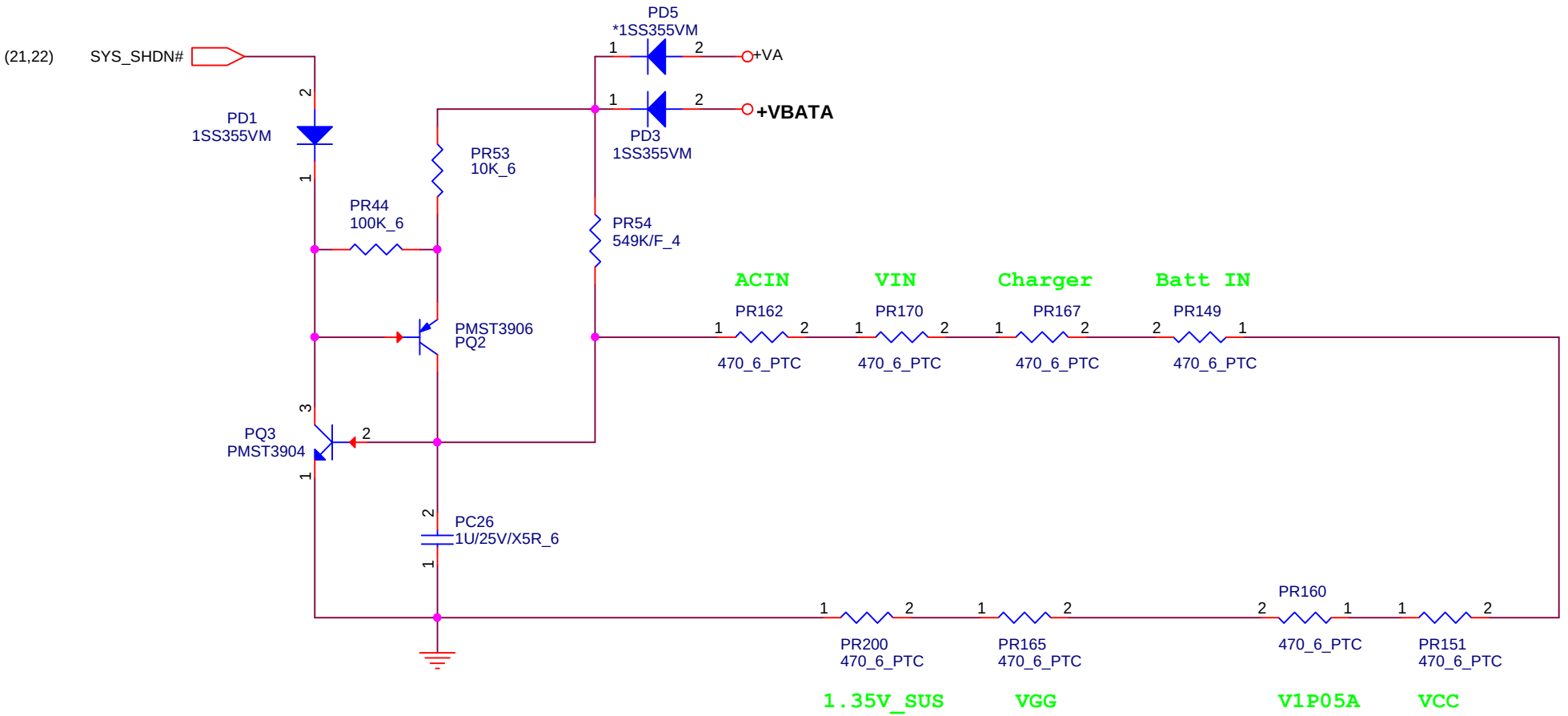




PROJECT : LI8G

Quanta Computer Inc.

Size	Document Number	Rev
	Load SW	1A
Date: Thursday, September 08, 2016	Sheet 33 of 40	



PROJECT : LI8G

Quanta Computer Inc.

Size	Document Number	Rev
	PTC Circuit	1A
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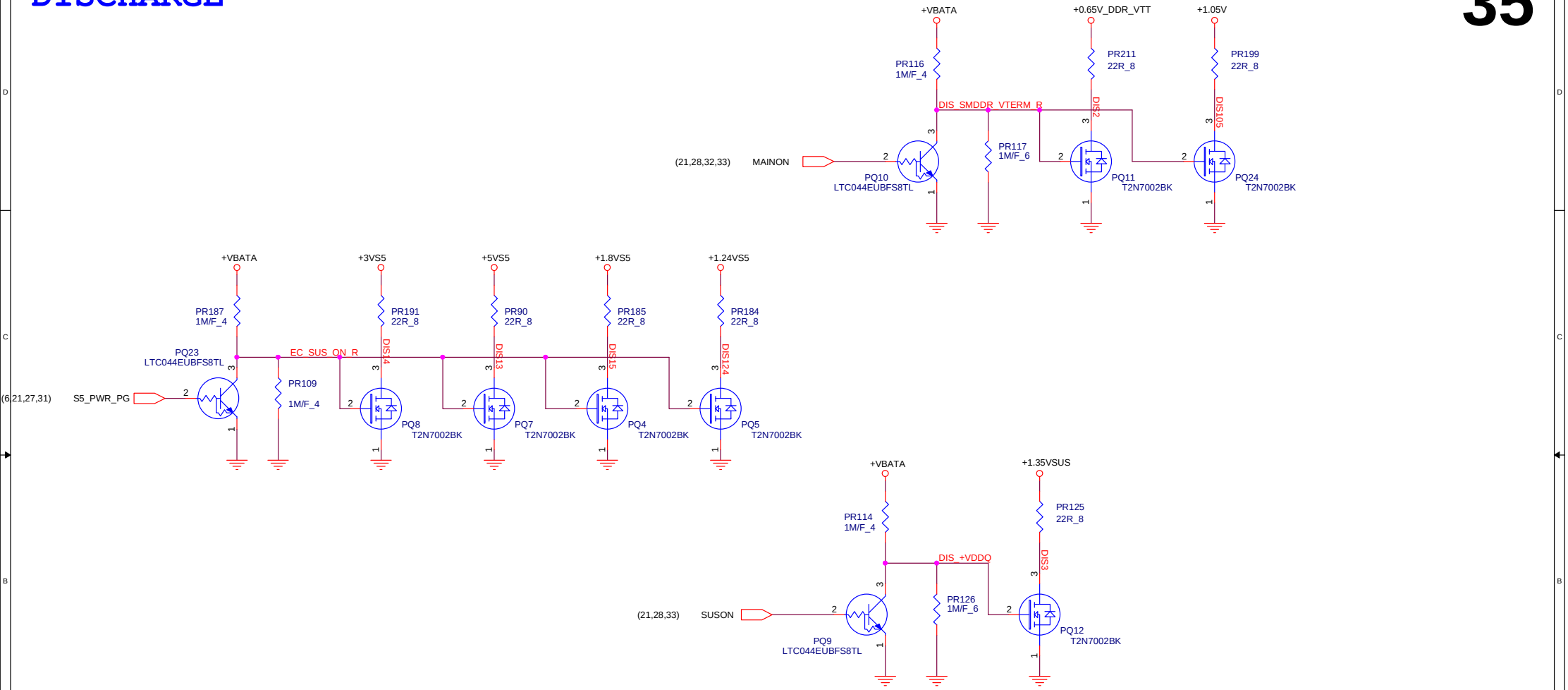
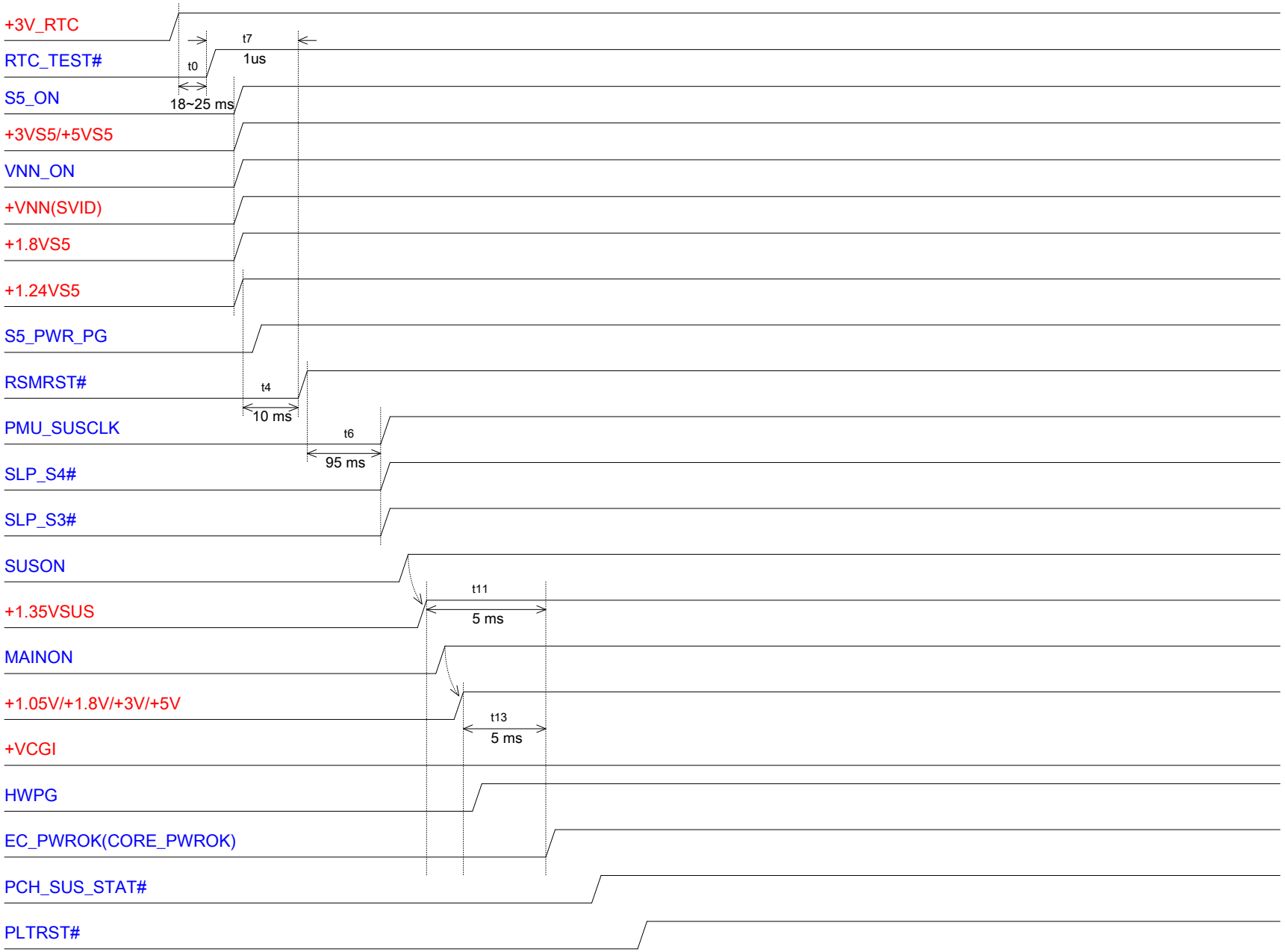
DISCHARGE



PROJECT : LI8G

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge	1A
Date: Thursday, September 08, 2016	Sheet 35 of 40	



PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	Power sequence	1A
Date: Thursday, September 08, 2016	Sheet 36 of 40	

LI8 EE Schematic EC Tracking Record A to B version(SDV/FVT Planar)

EC #	Page	Description	Part Affected
EC-FVT-01	24	Modify LED limited circuit resistor value the same as Newton 1.	R301,R306
EC-FVT-02	13	Buyer request change CAP PN due to EOD issue.	C238
EC-FVT-03	12	Stuff 100K to keep RSMRST# low after S5_ON ramped.	R321
EC-FVT-04	15	Add level shift for TPM reset pin.	Add Q47,R512,R507 Reserve Q46,R245
EC-FVT-05	21	S5_ON PU RES change to 10K to solve can't power on issue.	R468
EC-FVT-06	21	Modify R26/R21 PU power rail to solve can't power on issue.	
EC-FVT-07	12	Add CLKREQ# level shift circuit	Add U34,R510,R511 Reserve R508,R509
EC-FVT-08	3	Modify CLKREQ# PU power rail to +1.8VS5	
EC-FVT-09	15	Modify TPM footprint for pin4/pin11	U14
EC-FVT-10	18	RDC request to modify SSD CONN footprint	CN16
EC-FVT-11	3	Un-stuff BIOS ROM socket	Delete U29,U16 Add U17
EC-FVT-12	10	Un-stuff XDP CONN	Delete CN4
EC-FVT-13	5	Modify BID for FVT stage	Un-stuff R325; Stuff R342
EC-FVT-14	16,24,14	Follow ESD team request to modify ESD component P/N	SC8,SC13 Add EC8
EC-FVT-15	21	Un-stuff ESD component	Delete SC20
EC-FVT-16	6	Intel recommand to un-stuff RSMRST# & CORE_PWROK PU RES	Delete R391,R396
EC-FVT-17	21	Change RES value	R436
EC-FVT-18	5,16	Delete components which is workaround for ES sample CPU	Delete R145,R140,R146
EC-FVT-19	21	Modify EC pin11 VCC power rail to fix 3VPCU can't drop to 0V while press reset button	Add R13 Delete R19

LI8G Power Schematic EC Tracking Record A to B version

EC #	Page	Description	Part Affected
EC-FVT-P01	27, 28, 30, 31 32, 33	Change short pad	PJP3,PJP4,PJP5,PJP6,PJP7,PJP9,PJP10,PJP11,PJP12,PJP13,PJP14 PJP15,PJP16,PJP17,PJP18,PJP20,PJP21
EC-FVT-P02	27	modify 3V/5V enable voltage	PR189 change to 60.4K,PR190 change to 45.3K,PR193 change to 0 ohm Remove PR194
EC-FVT-P03	29	Change PU1 P/N	PU1
EC-FVT-P04	26	Change PQ13 P/N(FOR SMT PROGRAM)	PQ13
EC-FVT-P05	30	Change PC145,PC143 P/N(FOR HIGH LIMIT)	PC145,PC143
EC-FVT-P06	30	Change PC49,PC139 FOOTPRINT(FOR HIGH LIMIT)	PC139,PC49
EC-FVT-P07	26	BOM error	Un-stuff PR62

PROJECT : LI8G
Quanta Computer Inc.

Size	Document Number	Rev
	PWR A to B EC History	1A
Date: Thursday, September 08, 2016	Sheet 38 of 40	

LI8G EE Schematic EC Tracking Record B to C version(FVT -> SIT Planar)

EC #	Page	Description	Part Affected
EC-SIT-01	5	Modify KB LED GPIO to fix LED always on issue	
EC-SIT-02	21	Add MOS to turn off S5_ON while press EC reset button	Add Q50,R517
EC-SIT-03	16	Un-stuff Q30 to fix external MIC no function issue	Delete Q30 ; Add R484
EC-SIT-04	22	Modify MOS enable pin to fix press 4s power button shut down can't power on issue	
EC-SIT-05	22	Un-stuff diode and replace it with 0ohm	Delete D19 ; Add R513
EC-SIT-06	22	Modify PU RES value to 10K	R479
EC-SIT-07	22	Modify PTC circuit RES value to 100K	R458
EC-SIT-08	24	Un-stuff power on LED due to light leakage issue	Delete LED2,R284
EC-SIT-09	3	Follow Intel DG to PD USB2_VBUS_SNS	Delete R106 ; Add R113
EC-SIT-10	3	Follow Intel DG to PD USB2_DUALROLE_ID oin and reserve PU RES	Delete R105
EC-SIT-11	24	Modify KB LED limited-current RES value to meet test criteria	R290,R294
EC-SIT-12	21,26	Connect battery enable pin to EC	Delete PR111 ; Add R515
EC-SIT-13	19	WLAN power connect to +3.3V directly	Delete F4 ; Add F10
EC-SIT-14	13,19	Delete diode & PU RES due to no leakage concern	Delete D9,D10,R171,R173 ; Add R518,R519
EC-SIT-15	16	Modify ACZ_BCLK_AUDIO CAP value to fix Jitter over Spec issue	C148
EC-SIT-16	6	Add diode to fix can't power on until plug RTC issue	Add D25
EC-SIT-17	6	Stuff RTC_RST circuit	Add R477,R478
EC-SIT-18	21	Modify power rail to fix S5 leakage issue	Delete R13 ; Add R19
EC-SIT-19	5	Reserve IERR function	Delete R328 ; Add Q27
EC-SIT-20	13	Delete MOS which is no used for LCD_BK_OFF function	Delete Q6
EC-SIT-21	6	Modify TP to larger one	TP17,TP21
EC-SIT-22	16	Modify RES value to fix BIOS beep no sound issue	R250
EC-SIT-23	21	Connect THRMTRIP# to EC GPIO pin directly(reserve)	
EC-SIT-24	21	Reserve test point	Add TP56,TP57,TP58
EC-SIT-25	5	Modify board ID for SIT stage	Delete R324,R342 ; Add R341,R325
EC-SIT-26	20	Change USB power switch PN to 1.5A	U27,U28
EC-SIT-27	13	PN EOD issue	C238
EC-SIT-28	24	Modify PN	R301
EC-SIT-29	20	PN EOD issue	R184

LI8G Power Schematic EC Tracking Record B to C version(FVT -> SIT Planar)

EC #	Page	Description	Part Affected
EC-SIT-P01	33	Remove +3VSUS net which is no used	
EC-SIT-P02	29	Change source	PR178,PR135,PR152