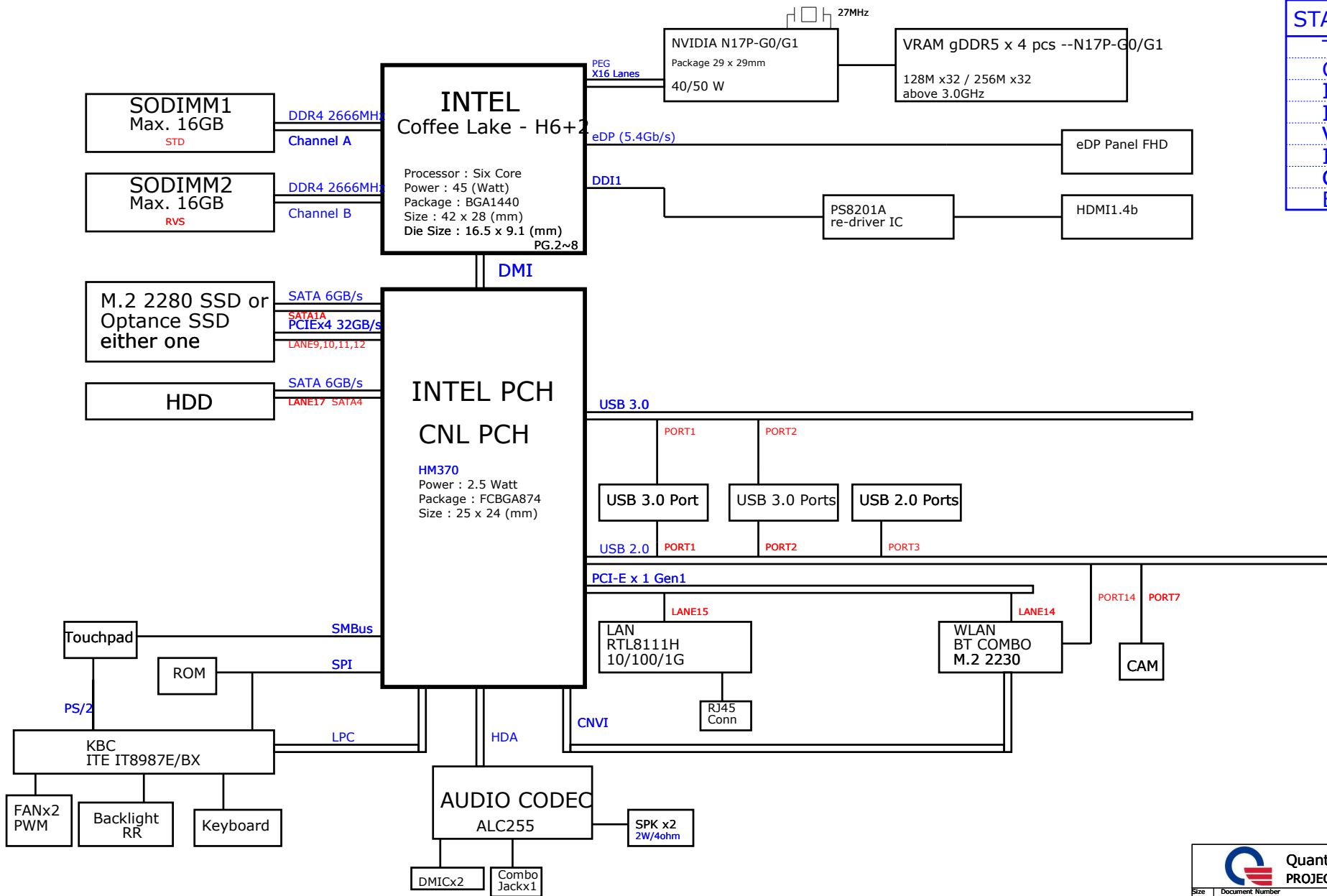


# Asus 15" FX504 GD/GE Block Diagram

01

STACKUP	
TOP	
GND	
IN1	
IN2	
VCC	
IN3	
GND	
BOT	





Model FX504GD FX504GE	REV	CHANGE LIST				
	ER	<p><b>1124 Change</b> Page 10 OC3#/OC4#/OC5#/OC6#/OC7# to PU +3V_S5 Page 15 Reserved R1202 to isolate +1.05V_S5 Page 53 ADD I2R66/I2R68 for HDMI Pre-emphasis setting</p> <p><b>1127 Change</b> Page 18 Reserved C221(DDR4_DRAMRST#) Page 19 Reserved C260(DDR4_DRAMRST#) Page 31 Modify HDD CONN CAP size to 0402 from 0201(C1234/C1235/C1232/C1233) Page 31 Modify HDD CONN FP for "DFHS22FR522" Page 32 Modify SSD CONN CAP size to 0402 from 0201(C318/C322/C323/C324/C325/C326/C327/C328) Page 32 Modify WIFI CONN CAP size to 0402 from 0201(C338/C339) Page 36 Modify "VPP_PG" to EC pin #126 from #19 Page 36 Modify "LED_CAP#" to EC pin #19 from #32 Page 36 Reserved EC pin #32 to TP(KTP51) Page 36 Swap EC pin #77 &amp; #76 signal "SPKER_ID" &amp; "WLAN_RF_ON" Page 23 Modify GPU timing(for GPU power sequence timing) Page 50 ADD KB backlight PWM control Page 13 Modify R1050 to 0ohm from 33ohm</p> <p><b>1101 Change</b> Page 13 Modify SML3ALERT#/SML2ALERT# PU to +3V_S5 from +3V Page 36 Modify SPI damping resistor to 33ohm from 15ohm Page 36 Modify MB ID Pin Define("MB_ID1"/"MB_ID2") Page 36 Modify SPK ID("SPK_ID0"/"SPK_ID1")</p> <p><b>1204 Change</b> Page 7 Add +1.2V_S0 to VCCPLL_OC1/VCCPLL_OC2/VCCPLL_OC3 Page 34 Mount C350/C351 ,Modify R942/R941 to 2.2kohm from 4.7kohm (for adjust the touch pad I2C signal quality ) Page 34 ADD level shiftt for touch pad I2C</p> <p><b>1205 Change</b> Page 16 ADD +1.2V_S0 &amp; +1.05V_VCCSTG control form C10_POWER signal(Currently set is RUN_ON) Page 20 ADD VC484(220pF) for DGPU_PWROK</p> <p><b>1206 Change</b> Page 22 ADD RC(VR160/VR161 &amp; VC480/VC481) for adjust the GPU I2C signal quality Page 30 Reserved ESD(SD41 &amp; SD42) component for USB_ON</p> <p><b>1124 Change</b> Page 10 OC3#/OC4#/OC5#/OC6#/OC7# to PU +3V_S5 Page 15 Reserved R1202 to isolate +1.05V_S5 Page 53 ADD I2R66/I2R68 for HDMI Pre-emphasis setting</p> <p><b>1127 Change</b> Page 18 Reserved C221(DDR4_DRAMRST#) Page 19 Reserved C260(DDR4_DRAMRST#) Page 31 Modify HDD CONN CAP size to 0402 from 0201(C1234/C1235/C1232/C1233) Page 31 Modify HDD CONN FP for "DFHS22FR522" Page 32 Modify SSD CONN CAP size to 0402 from 0201(C318/C322/C323/C324/C325/C326/C327/C328) Page 32 Modify WIFI CONN CAP size to 0402 from 0201(C338/C339) Page 36 Modify "VPP_PG" to EC pin #126 from #19 Page 36 Modify "LED_CAP#" to EC pin #19 from #32 Page 36 Reserved EC pin #32 to TP(KTP51) Page 36 Swap EC pin #77 &amp; #76 signal "SPKER_ID" &amp; "WLAN_RF_ON" Page 23 Modify GPU timing(for GPU power sequence timing) Page 50 ADD KB backlight PWM control Page 13 Modify R1050 to 0ohm from 33ohm</p> <p><b>1101 Change</b> Page 13 Modify SML3ALERT#/SML2ALERT# PU to +3V_S5 from +3V Page 36 Modify SPI damping resistor to 33ohm from 15ohm Page 36 Modify MB ID Pin Define("MB_ID1"/"MB_ID2") Page 36 Modify SPK ID("SPK_ID0"/"SPK_ID1")</p> <p><b>1204 Change</b> Page 7 Add +1.2V_S0 to VCCPLL_OC1/VCCPLL_OC2/VCCPLL_OC3 Page 34 Mount C350/C351 ,Modify R942/R941 to 2.2kohm from 4.7kohm (for adjust the touch pad I2C signal quality ) Page 34 ADD level shiftt for touch pad I2C</p> <p><b>1205 Change</b> Page 16 ADD +1.2V_S0 &amp; +1.05V_VCCSTG control form C10_POWER signal(Currently set is RUN_ON) Page 20 ADD VC484(220pF) for DGPU_PWROK</p> <p><b>1206 Change</b> Page 22 ADD RC(VR160/VR161 &amp; VC480/VC481) for adjust the GPU I2C signal quality Page 30 Reserved ESD(SD41 &amp; SD42) component for USB_ON</p>				
	PR	<p>Page 10 ADD TP220 &amp; TP221 Page 11 ADD RTC detect (R12475/R1216/Q50/R1217/R1218) for EC check . Page 10 ADD R12474/ R12473 for SML1CLK &amp; SML1DATA PU to +3V_S5. Page 13 Modify (R1050/R1201/R1053) to short pad from 0ohm. Page 14 Modify PR Board ID . Page 14 Reserve R1085 for DGPU_EVENT# PU Page 14 Reserve R1088 for SMBALERT# (Strapping) set to "0" Page 17 Reserve EMI CAP (EMC8/EMC9/EMC10/EMC11) Page 23 Modify VC479 size to 0402 from 0201 Page 23 Modify VR67 to 150Kohm from 100kohm Page 23 ADD VQ14/VR173/VC485(NVVDD_CORE1_EN)VQ15/VR174/VC486(1V8_MAIN_EN) for VGA power sequence. Page 32 Modify C320 size to 0402 from 0201 Page 34 Modify TR2 to 18.7kohm from 10kohm for set TU1 temperature 125deg. Page 34 Reserve TP device side PU R231 for TP_INTH#. Page 35 Modify (AR62/AR63/AR71) to short pad from 0ohm. Page 36 Modify KR164 to 18.7kohm from 10kohm for set TU1 temperature 125deg. Page 36 Reserve KC94 for PCH_SPI1_CLK_C Page 40 Modify PR453 to 18.7kohm from 100kohm for set TU2 temperature 110deg. Page 55 Modify ESD(LD7/LD8/LD10/LD9/LD1/LD2/LD5/LD6) P/N</p>				
DOC NO.		PROJECT MODEL :	BKLG/BKLH	APPROVED BY:		DATE: 2018/01/17
		PART NUMBER:		DRAWING BY:		REVISION: 1A



## Coffee Lake Processor (CLK,MISC,JTAG)

03

Please remove to CPU side

Host CLK:  
Trace length < 11000 mils  
Trace spacing = 15 / 20 mils, Impedence 85 ohm

Close to CPU

For DCI debug

## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX\_ENABLED BIT IN DEBUG  
1, Disable;

Mark eDP mode Enabled

Mark PCIe port reserved  
N17P used port 8~15

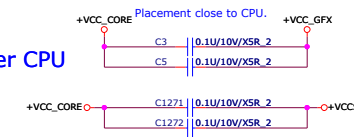
Design Note(CFG\_RCOMP):  
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.
CFG[0]	Stall reset sequence after PCU lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a Oxm board.
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS fro training

## CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A

## Under CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



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## ESD18/ESD19 Close to CPU



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## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



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## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU



## ESD18/ESD19 Close to CPU

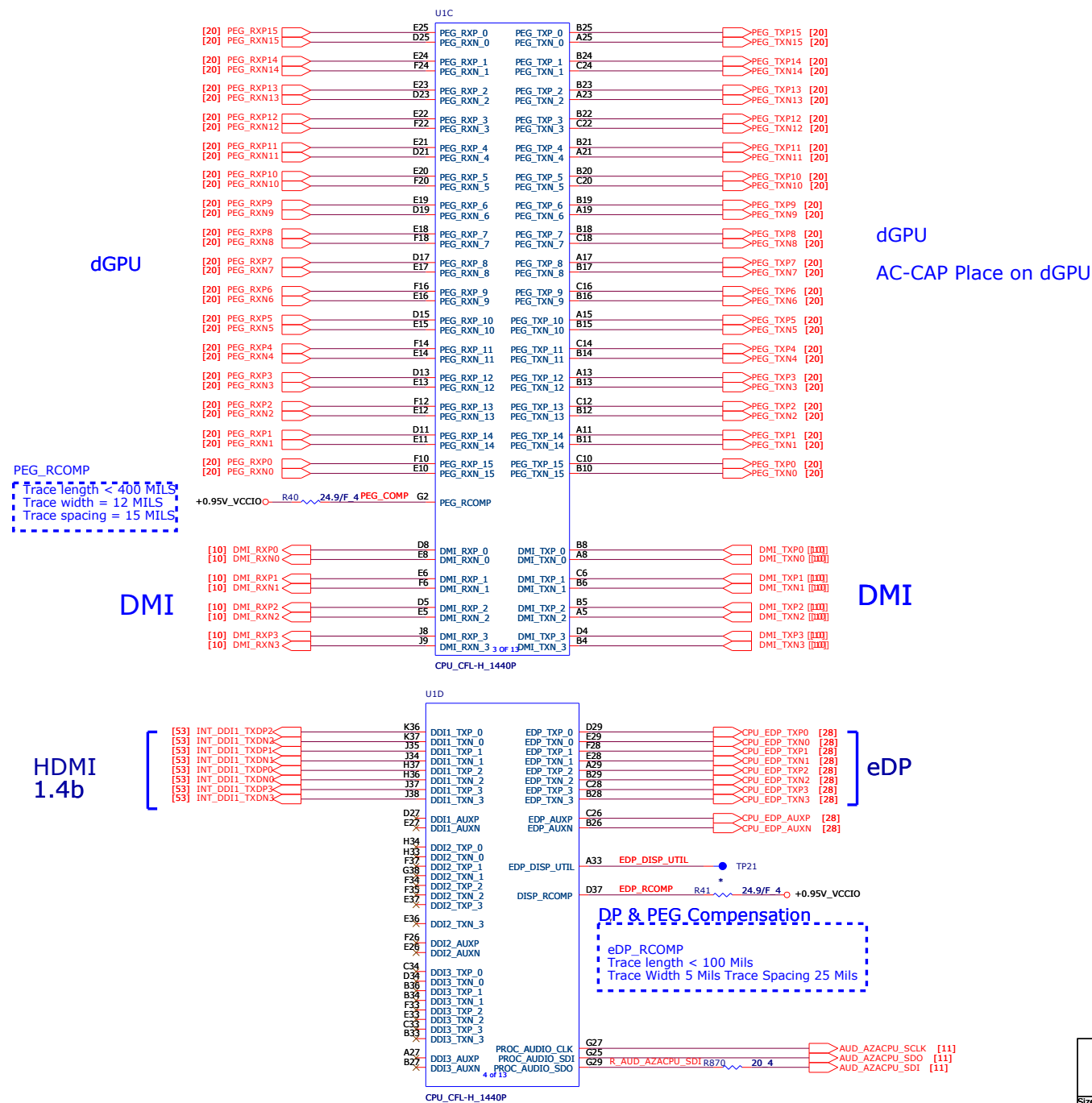


## ESD18/ESD19 Close to CPU



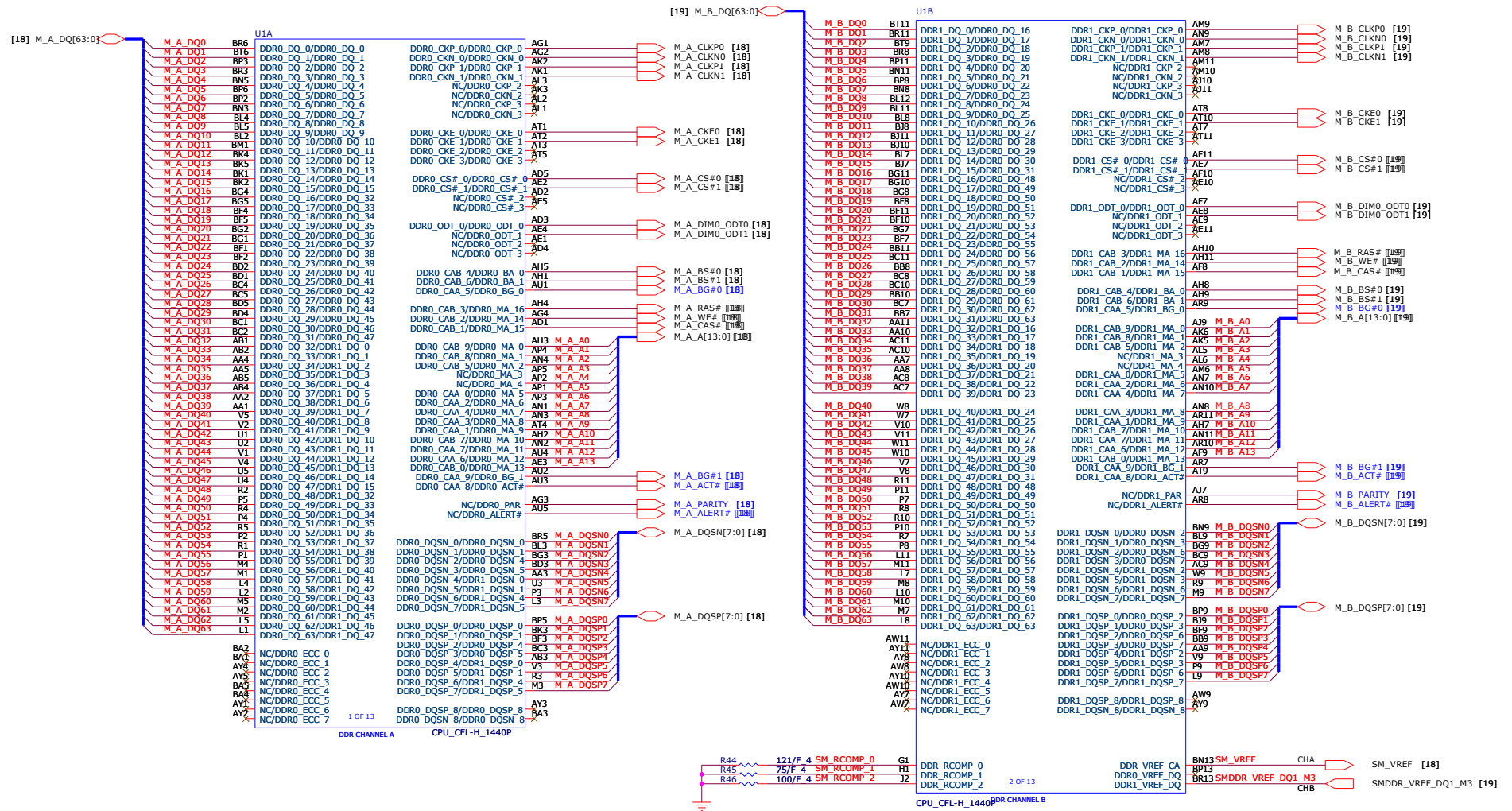
## ESD18/ESD19 Close to CPU



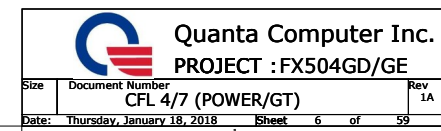




## Coffee Lake Processor (DDR4)



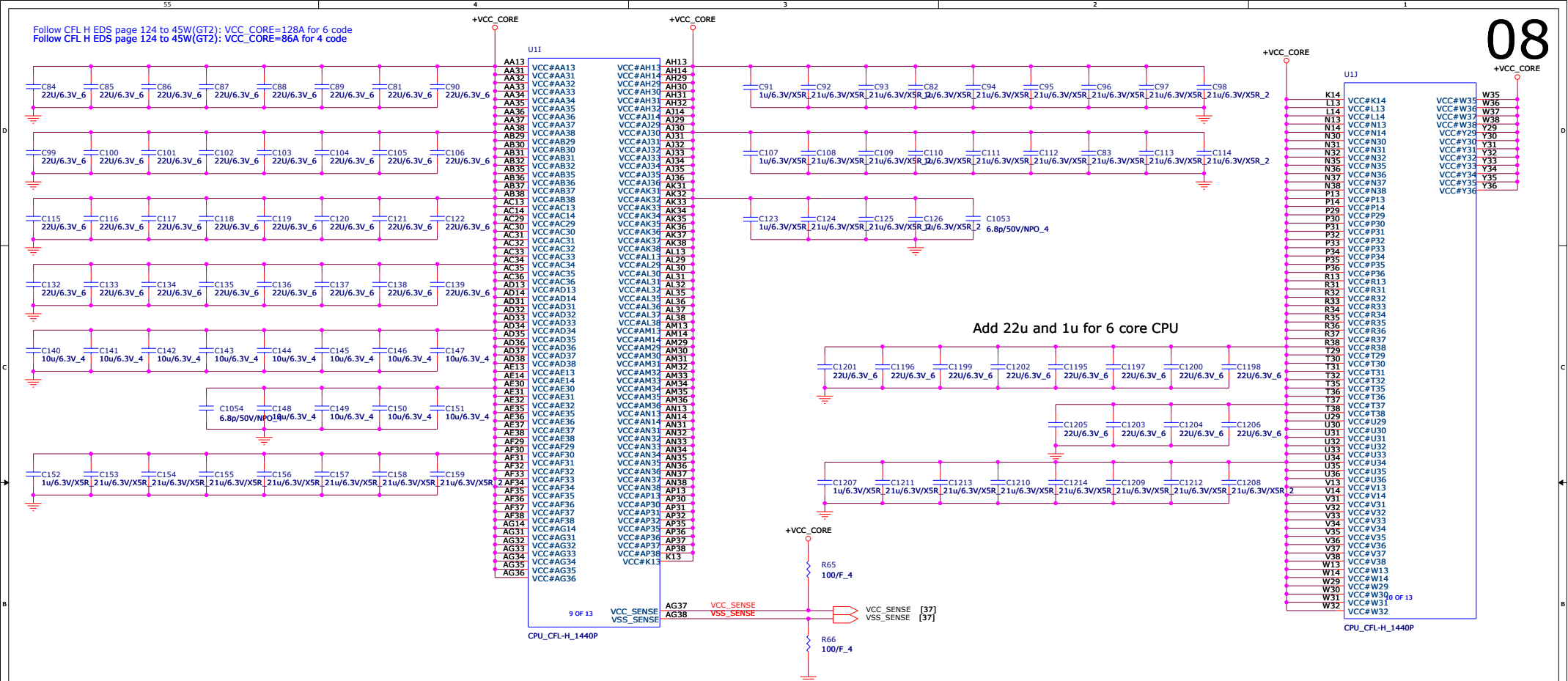








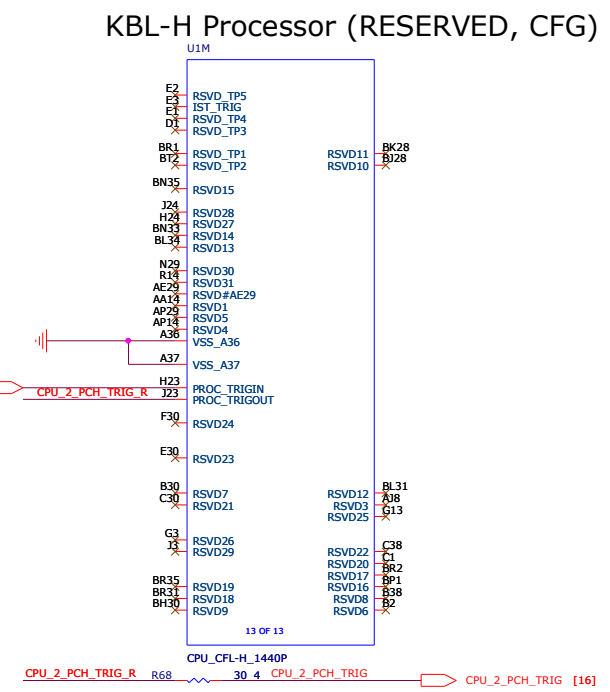
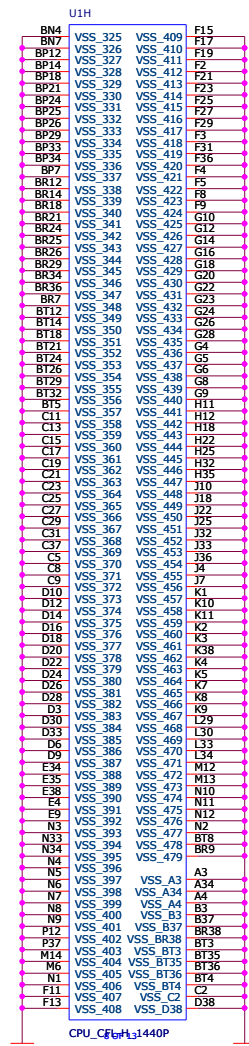
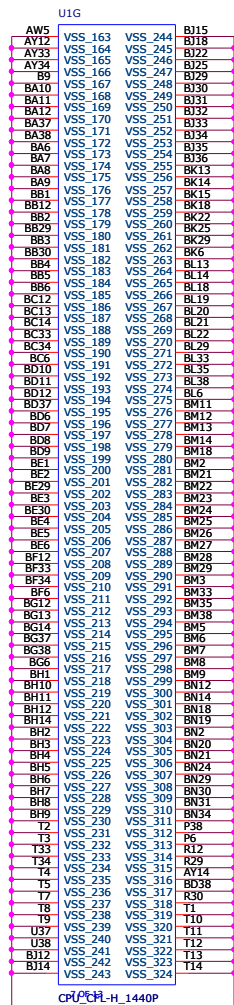
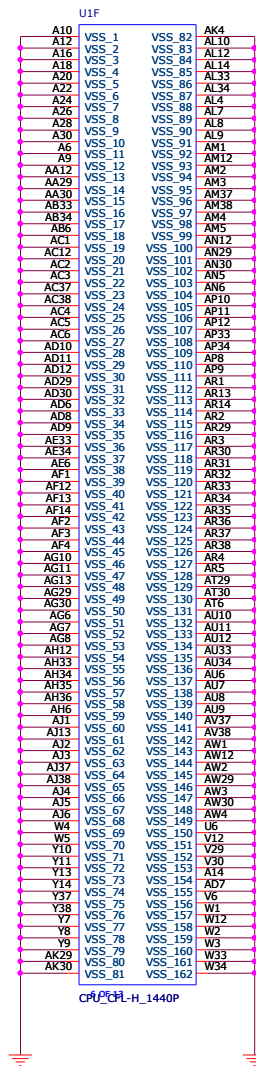




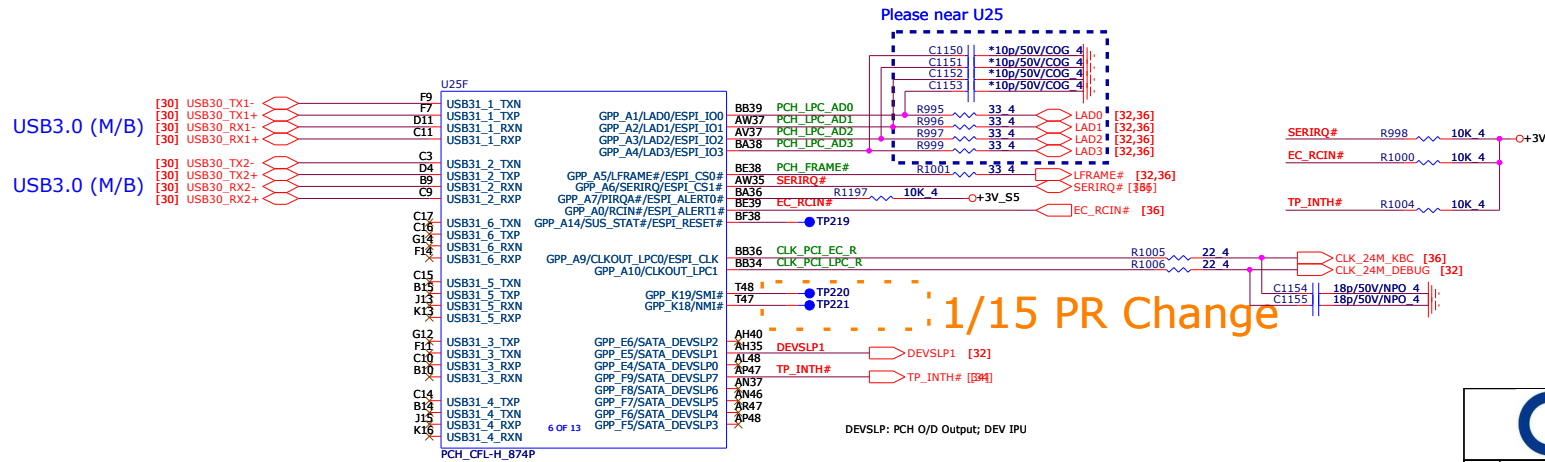
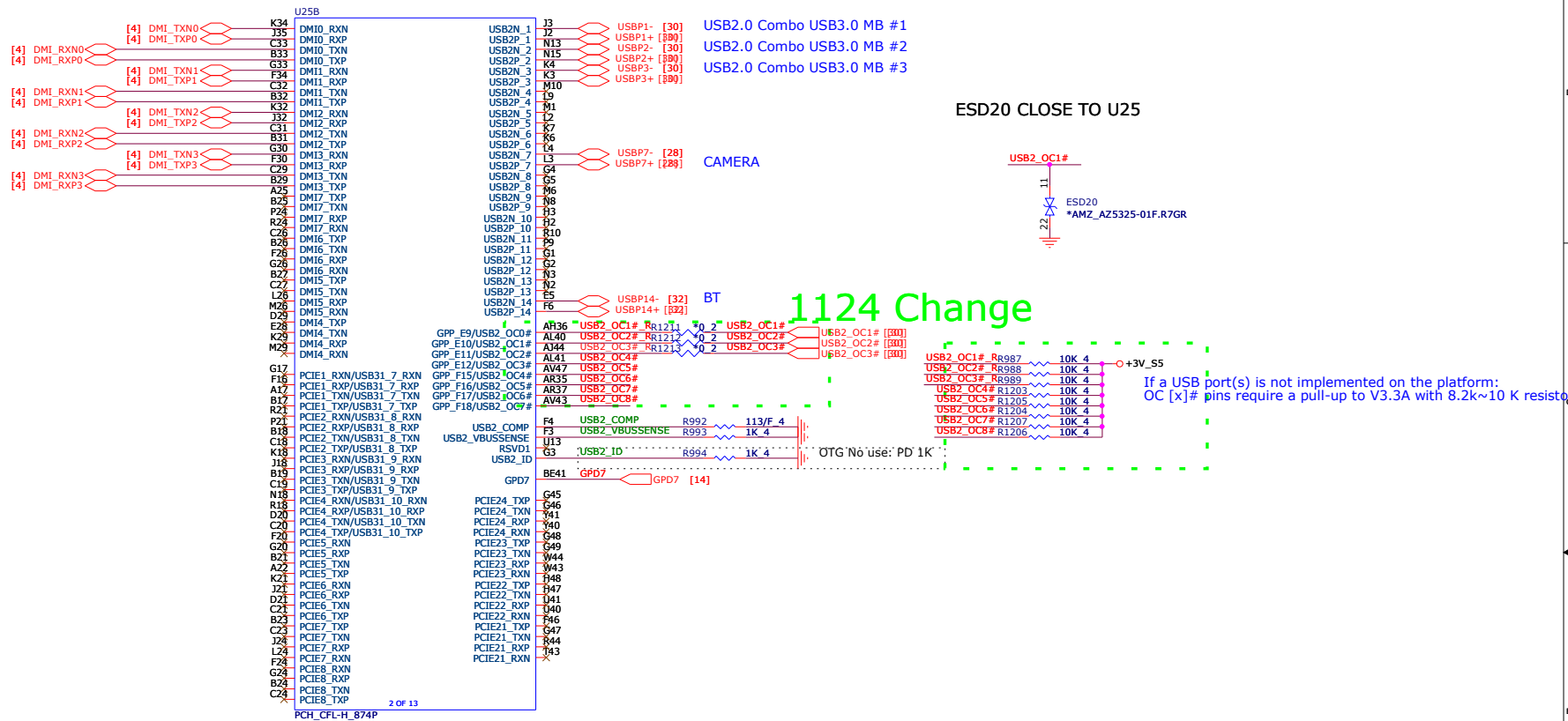
Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket  
Trace Impedance 50 ohm



### CFL-H Processor (GND)





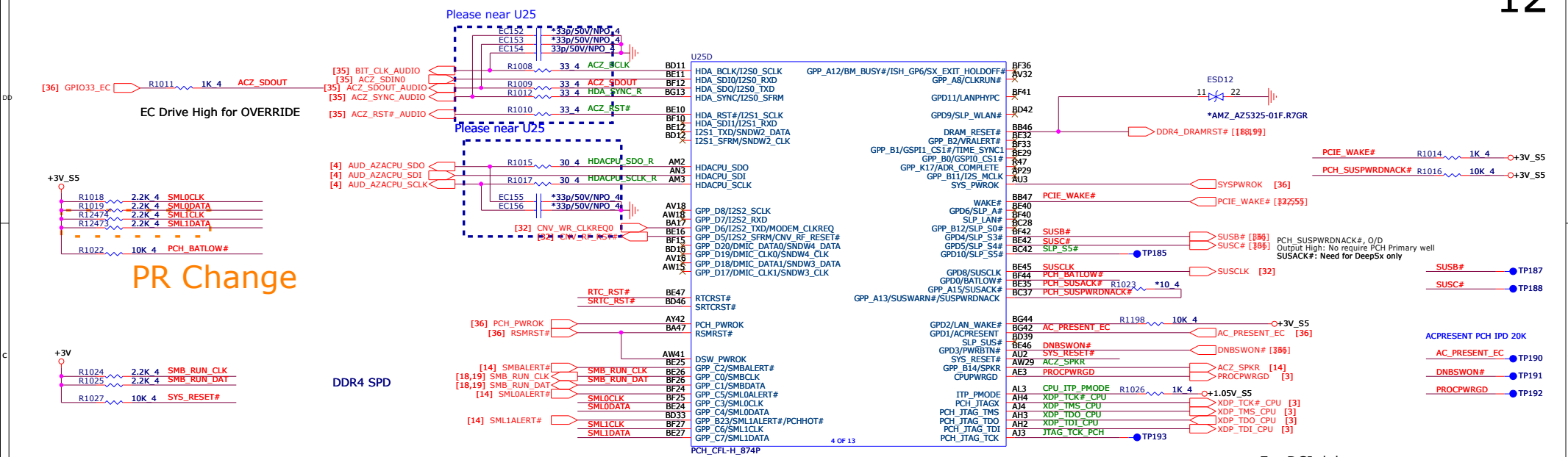


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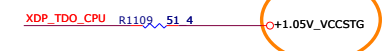
Size	Document Number	Rev
	PCH 1/7 (DMI/USB/PCIE)	1A

Date: Thursday, January 18, 2018 Sheet 10 of 59



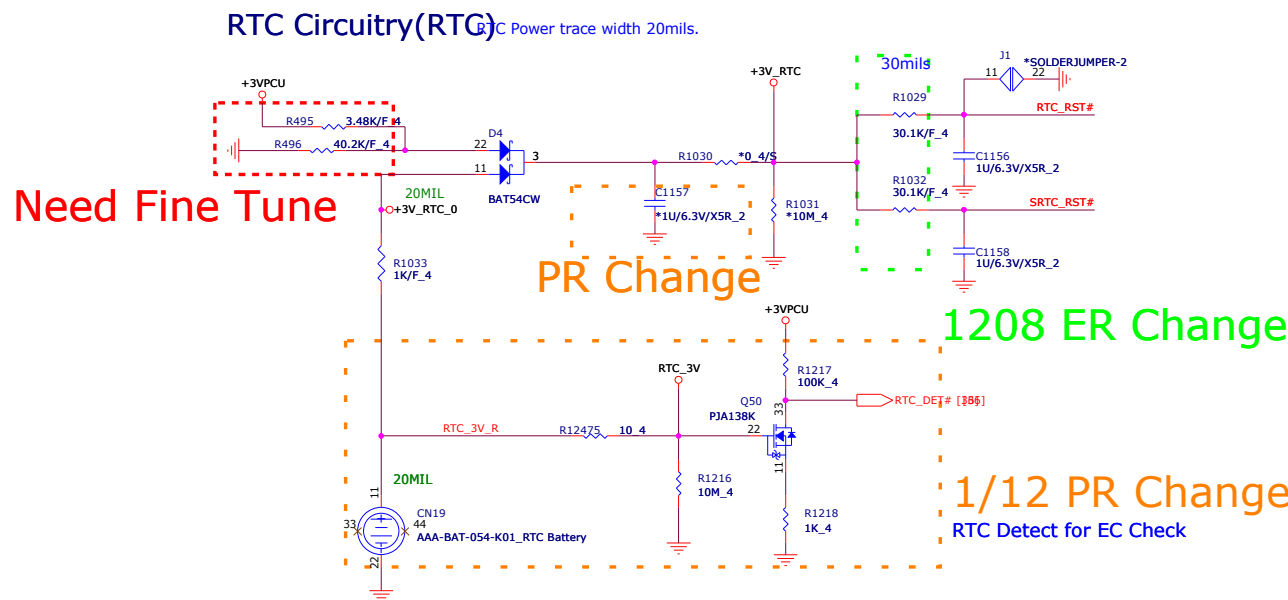



For DCI debug



Close to PCH

DIFF FX504 GE



 <div> <p><b>Quanta Computer Inc.</b></p> <p><b>PROJECT : FX504GD/GE</b></p> </div>		
Size	Document Number	Rev
	PCH 2/7 (HDA/SMBUS)	1A
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1129 Change

1101 Change

1/12 PR Change

1/12 PR Change

Place to BOT

PCH SPI ROM(CLG)

1/12 PR Change  
Put damping resistor close to CPU





	BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3
GE15 1050TI ID1 ROG	0	0	0	0
GE17 1050TI ID1 ROG	0	0	0	1
FX504 Single Mic	0	0	0	1
FX504 Dual Mic	0	0	1	1

Check again by KEVIN???



```

: HPD0 --> HDMI1.4
: HPD2 --> DP++
:
```

## 1/12 PR Change

## 0928 Change

PCH Strap: GPP\_J6 = M.2 CNVI STRAP

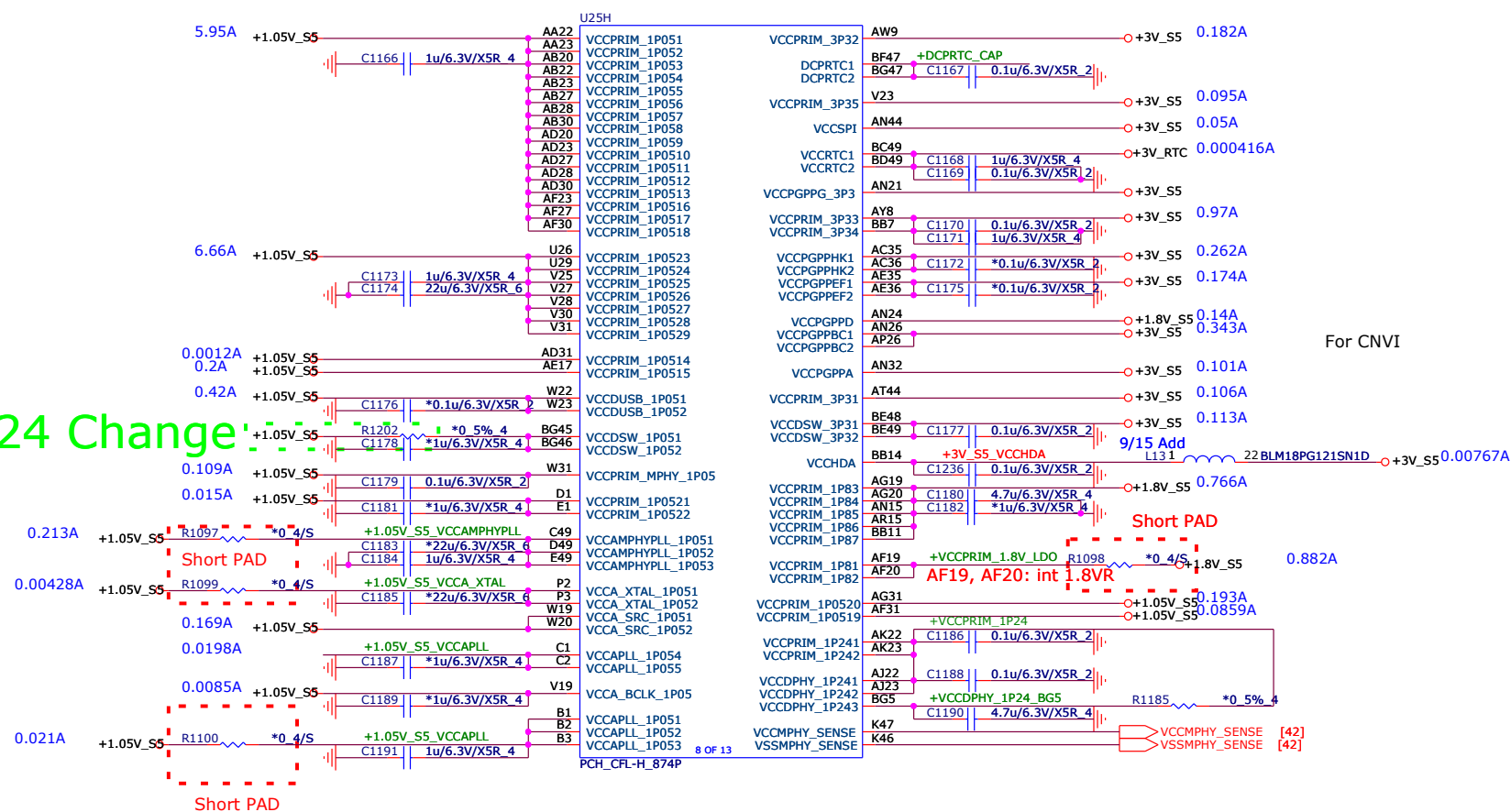
External pull-up is required. Recommend 100K.

+5V 55 R1096 100K 5% 4 GPD7 [10]



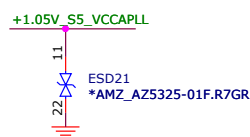
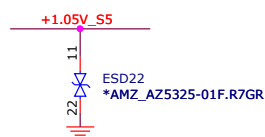
need to add +1.05V power rail

1124 Change:



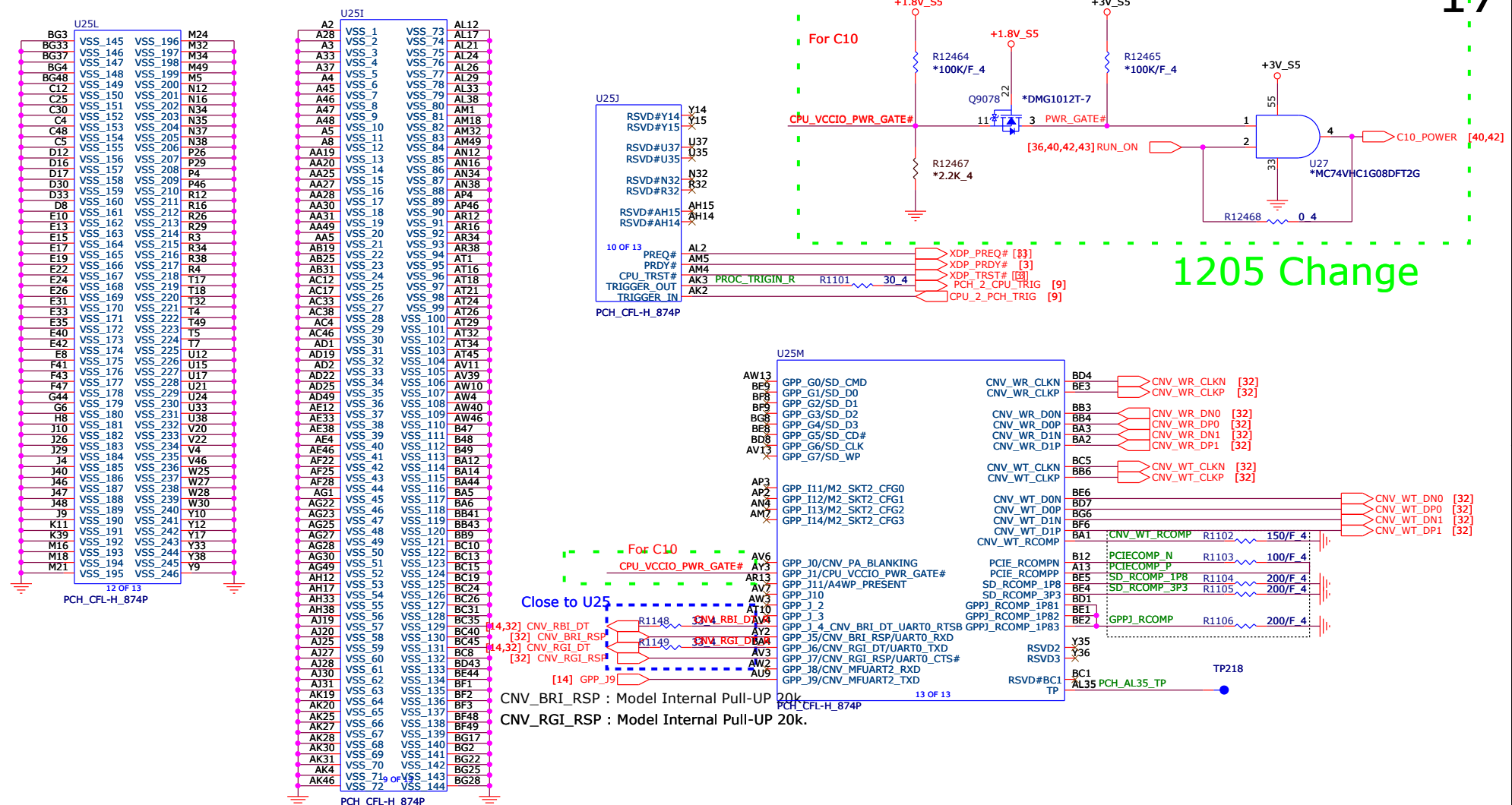
ESD22 CLOSE TO U25

ESD21 CLOSE TO U25.B2



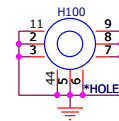
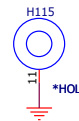
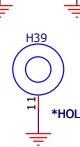
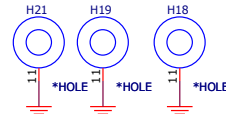
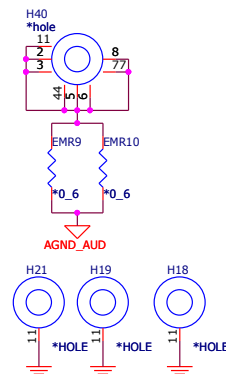
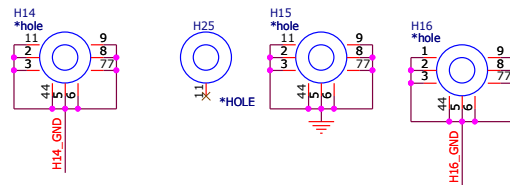
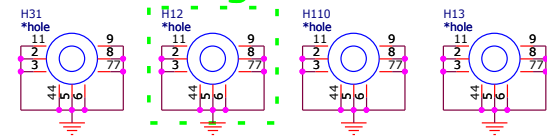
1.24V for CNVi logic = VCCDPHY\_1P24 & +VCCPRIM\_1P24  
This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC.  
Refer to the Platform Design Guide for implementation details.



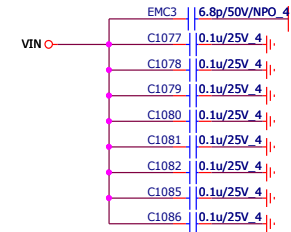




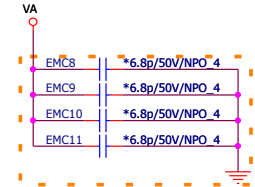
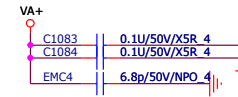
## 1207 Change



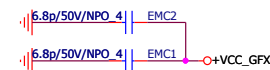
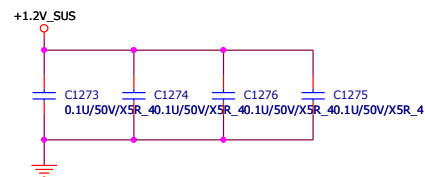
placement on TOP SIDE VIN Plane



placement on TOP SIDE VA+ Plane



PR Change



For Over place use



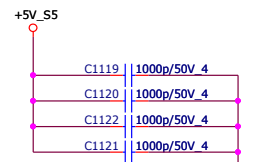
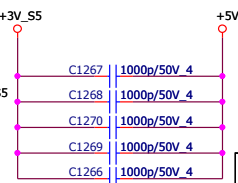
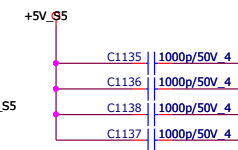
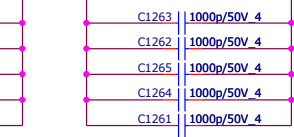
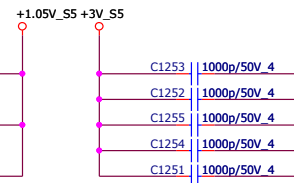
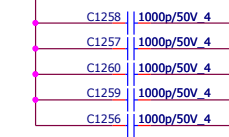
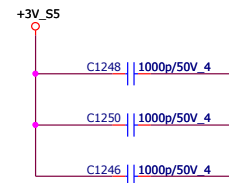
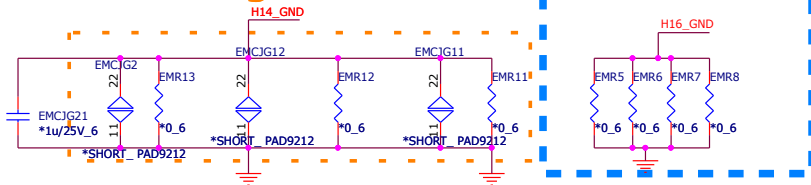
For EMC

For ESD request

Close to H14

Close to H16

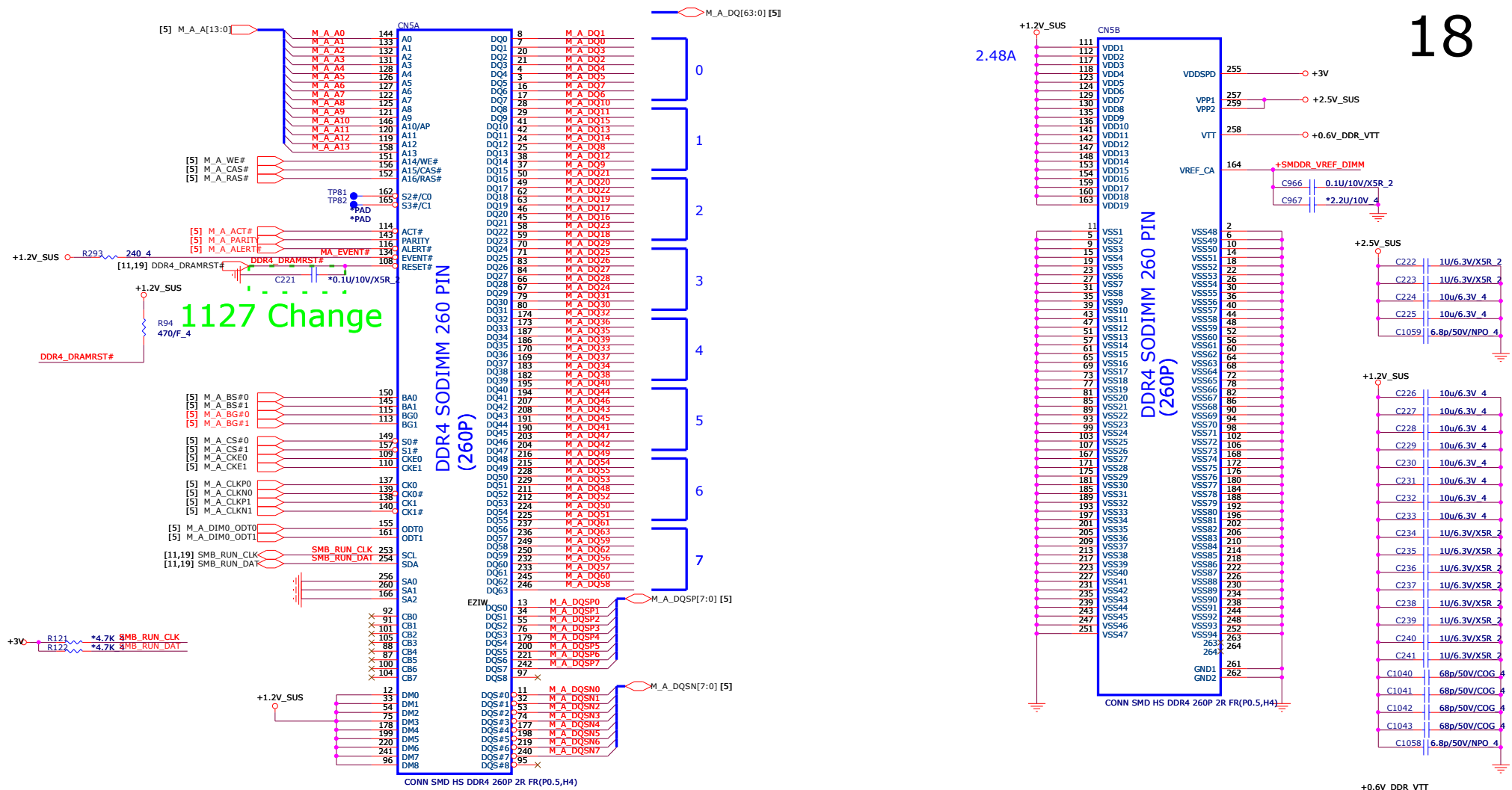
PR Change



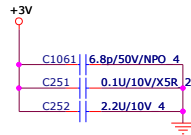
Quanta Computer Inc.  
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	HOLE	1A
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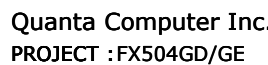
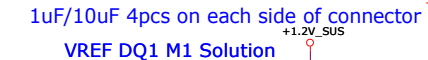
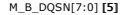
Place these Caps near So-Dimm0.



Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector















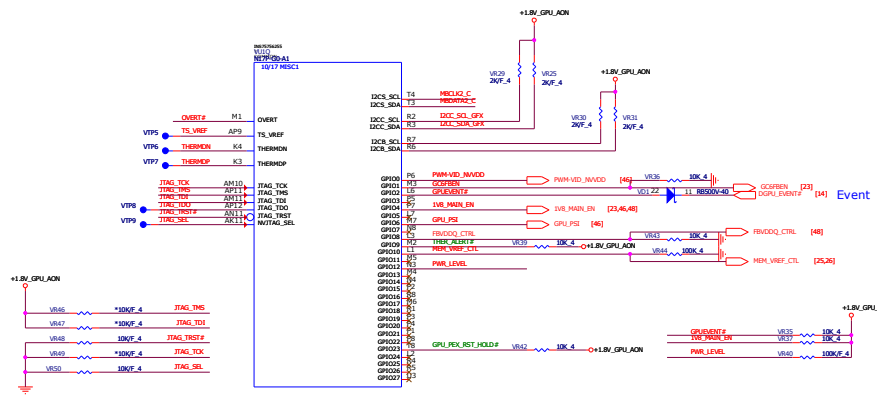
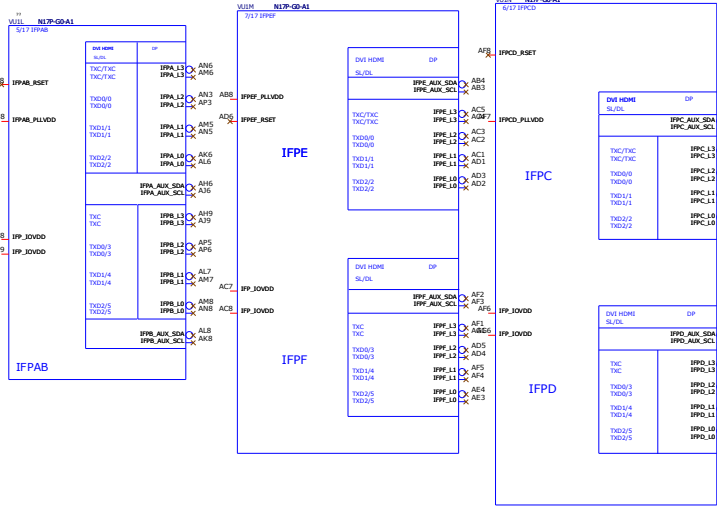


Table 14.2. GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	INVD0_PWM_VID	O	PWM Output to control INVD0	0 to 1V8 PWM output
GPIO1	GC6M_GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down
GPIO2	GC6M_GPU_EVENT#	I	GPU wake signal for GC6 2.1	10KΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	INVD0_STRAP_PWM	O	PWM output to control the STRAP power supply	0 to 1V8 output
GPIO4	GC6M1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to 1V8_AON
GPIO5	FRAM_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8AON

STRAP[2:0] VRAM Table for N17P-G0/G1 GDDR5 Recommended Memories

STRAP[2:0]	DESCRIPTION	Vendor	Vendor P/N	Quanta P/N	FBIDDQ
0x0	GD0RS 256Mx32 7 GHz	Samsung	K4G080325FB-HC28 (B-die)	AKGSGQ0191	1.5V/1.35V
0x1	GD0RS 256Mx32 7 GHz	Micron	MT51256H032HF-70-A (A-die)	AKGSGQUTL21	1.5V/1.35V
0x2	GD0RS 256Mx32 7 GHz	Hynix	H5GC8H24MJR-R0C (M-die)	AKGSGQUTW09	1.5V/1.35V
0x7	GD0RS 128Mx32 7 GHz	Samsung	K4G41325FE-HC28 (E-die)	AKGSGQUTL11	1.5V/1.35V
0x8	GD0RS 128Mx32 7 GHz	Micron	EDW4032BAG-70-F-D (A-die)	AKGSGQUTL15	1.5V/1.35V
0x6	GD0RS 128Mx32 7 GHz	Hynix	H5GC4H24AJR-R0C (A-die)	AKGSGQUTW29	1.5V/1.35V

Default

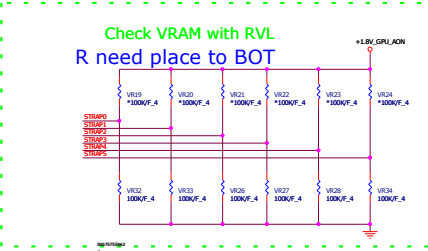
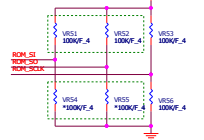


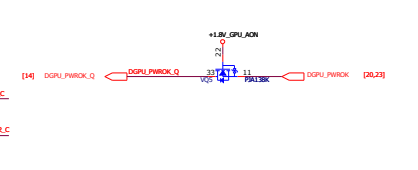
Table 5.3 RAMCFG

Strap Pins	see Note	RAMCFG Setting Number
STRAP2	STRAP1	STRAP0
L	L	L
L	L	H
L	H	L
L	H	H
H	L	L
H	L	H
H	H	L
H	H	H
L	M	L
L	M	H

R need place to BOT



1206 Change



Throttle



Overt shutdown



Table 14.2. GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	INVD0_PSI	O	Phase Shodding (see Section 14.3.3)	10 KΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 KΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the VDDQ2 power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 KΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 KΩ pull-down
GPIO11	LCD_VDD	O	Panel Power enable	100 KΩ pull-down
GPIO12	PWR_LEVEL	I	As power detect of power supply (drawn input)	100 KΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted Input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted Input. See Figure 14.5
GPIO16	GC6M_GPU_PEX_RST_NORM	O	System side PCIe reset monitor	10 KΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted Input. See Figure 14.5
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted Input. See Figure 14.5
GPIO19	3D_Vision	O	3D Vision L/R Signal	100 KΩ pull-down
GPIO20	GC6S_MODE	O		
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		

Table 14.2. GPIO Descriptions for GB4C-128 Packages (Continued)

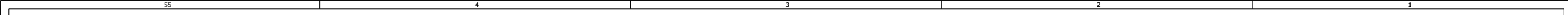
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO23	GC6M_GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	Open Drain 10 KΩ pull-up to a sated 3V3
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted Input. See Figure 14.5
GPIO25	UNUSED	I/O		
GPIO26	UNUSED	I/O		
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted Input. See Figure 14.5

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 KΩ pull-up to 3V3_AON











Channel 0  
<0~31>

MF=0 Non-mirrored

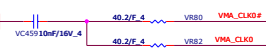


QD24~31

QD16~23

QD8~15

QD0~7



+FBVDDQ\_MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

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VMDQ-MEM

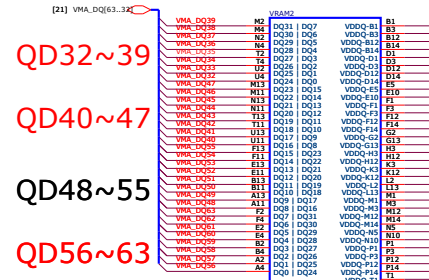
VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

Channel 1  
<32~63>

MF=1 mirrored

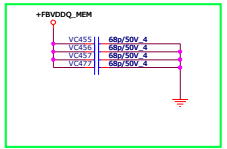


QD32~39

QD40~47

QD48~55

QD56~63



+FBVDDQ\_MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

VMDQ-MEM

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VMDQ-MEM

Table 9.4 GDDR5 Command Mapping (GB4C-128 &amp; GB2C-64 packages)

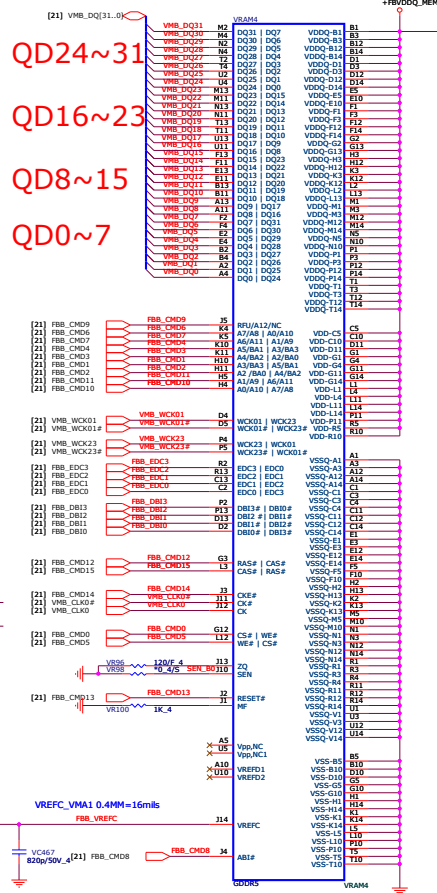
Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB1*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1



Channel 0  
<0-31>  
MF=0 Non-mirrored



Channel 1  
<32-63>

MF=1 mirrored

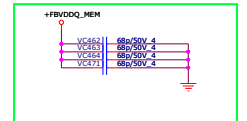
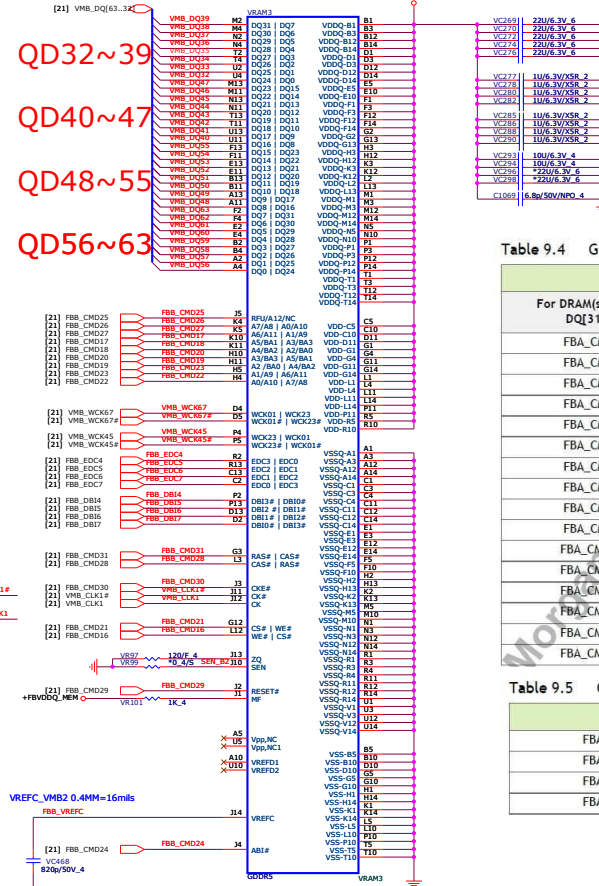


Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB1*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1



D  
C  
B  
A

D  
C  
B  
A


5

4

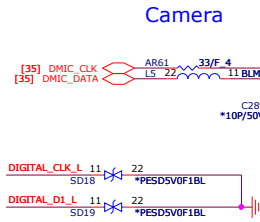
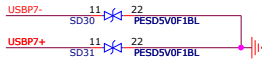
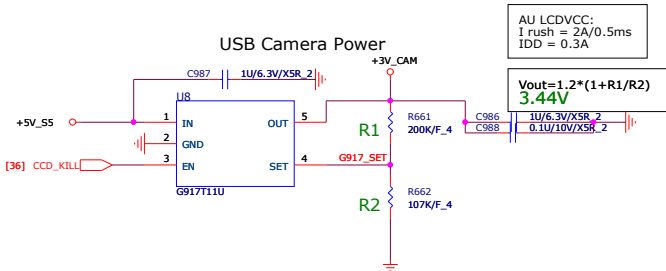
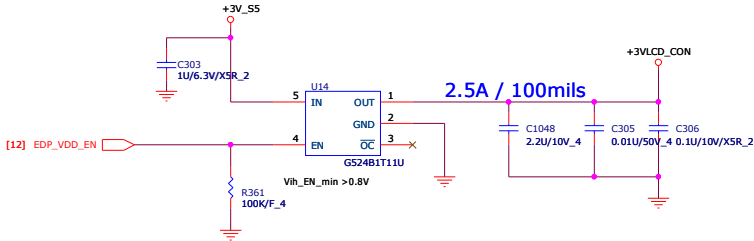
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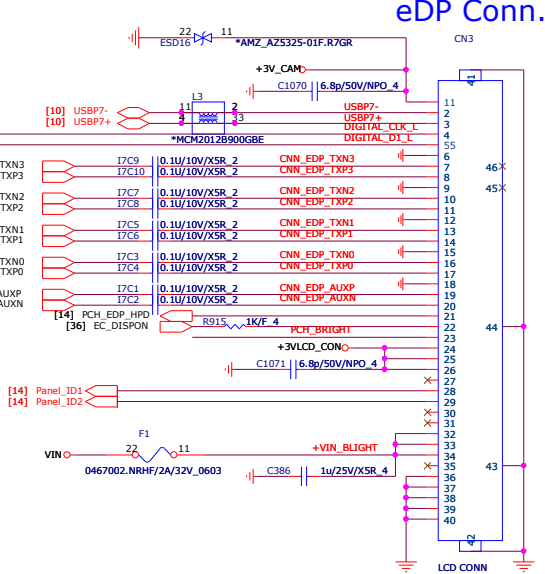
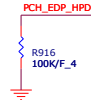
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Size	Document Number			Rev
	N17P-G1 (Reserved)			1A
Date:	Thursday, January 18, 2018		Sheet	27 of 59






	Panel ID1	Panel ID2
FHD	1	1
4K2K	1	0
HD	0	1





D  
C  
B  
A

D  
C  
B  
A

		<b>Quanta Computer Inc.</b>	
		<b>PROJECT : FX504GD/GE</b>	
Size	Document Number	Rev	
	NA	1A	
Date: Thursday, January 18, 2018		Sheet	29 of 59

5

4

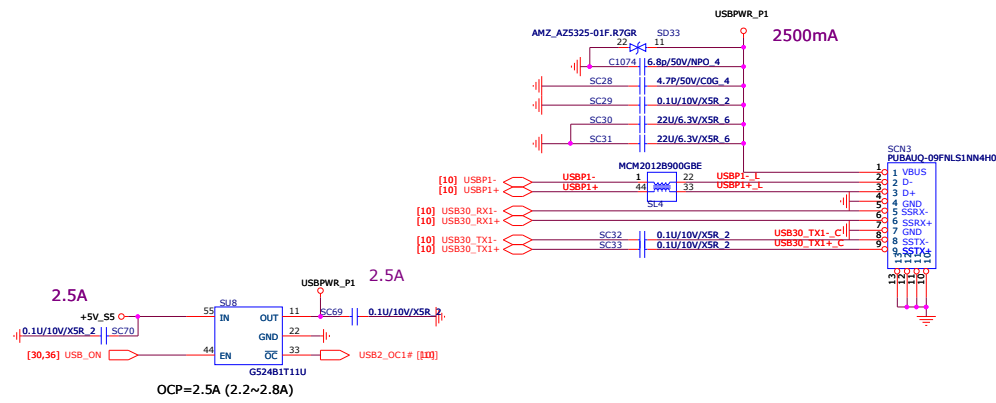
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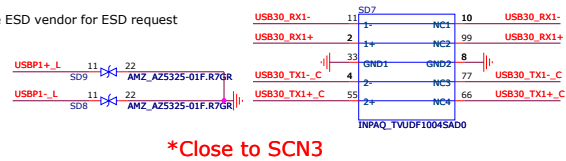
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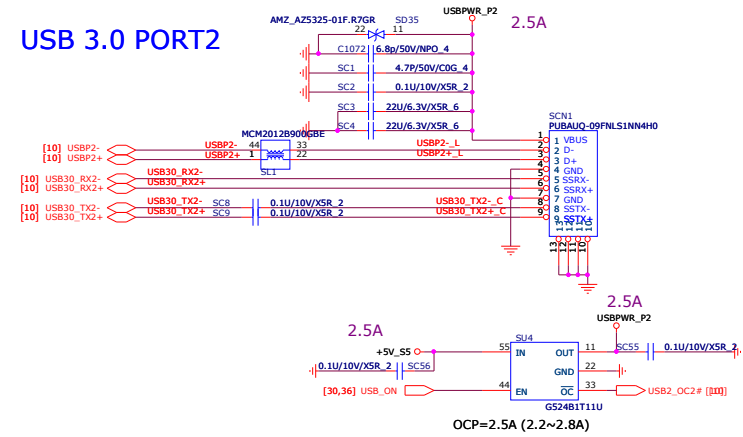
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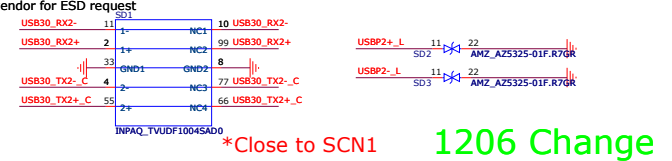
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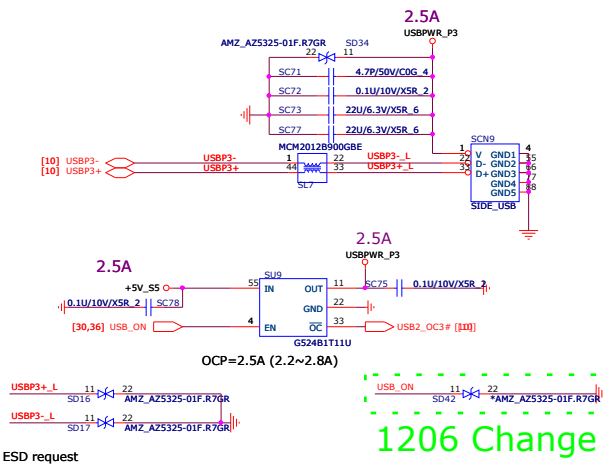
## USB 3.0 PORT2



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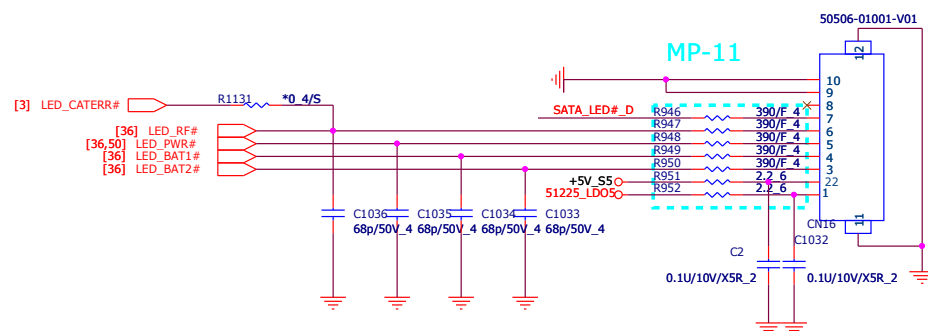
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1206 Change



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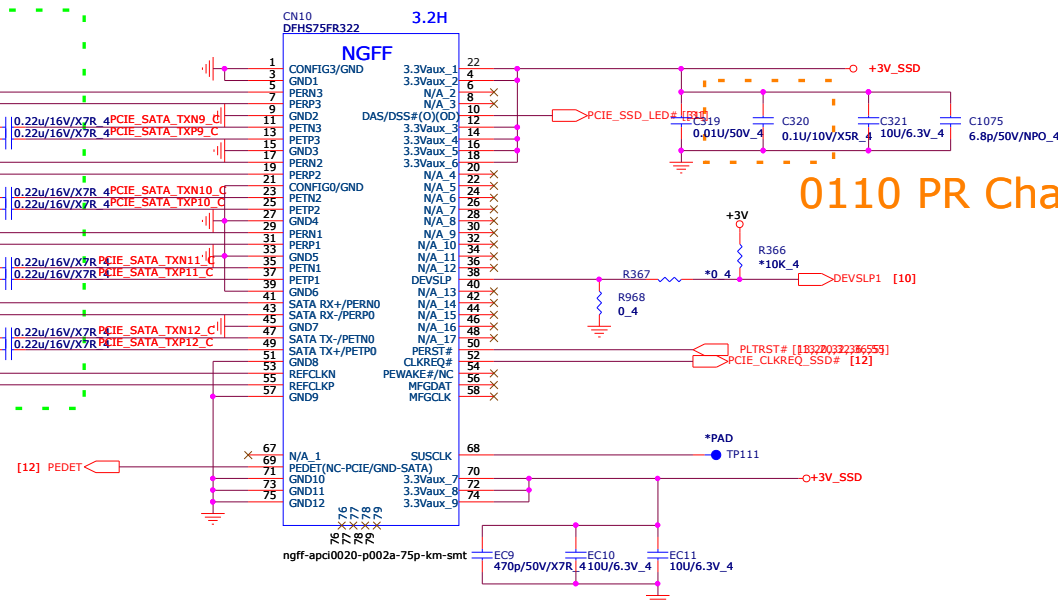
## 1127 Change



## SSD

## 1127 Change

Check again by Jay???



## WLAN/BT

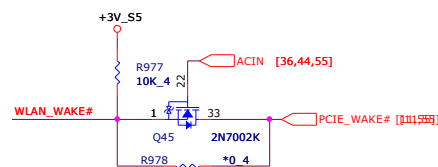
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DRE(12-0004-01) RDC STD  
DFHS75FR026

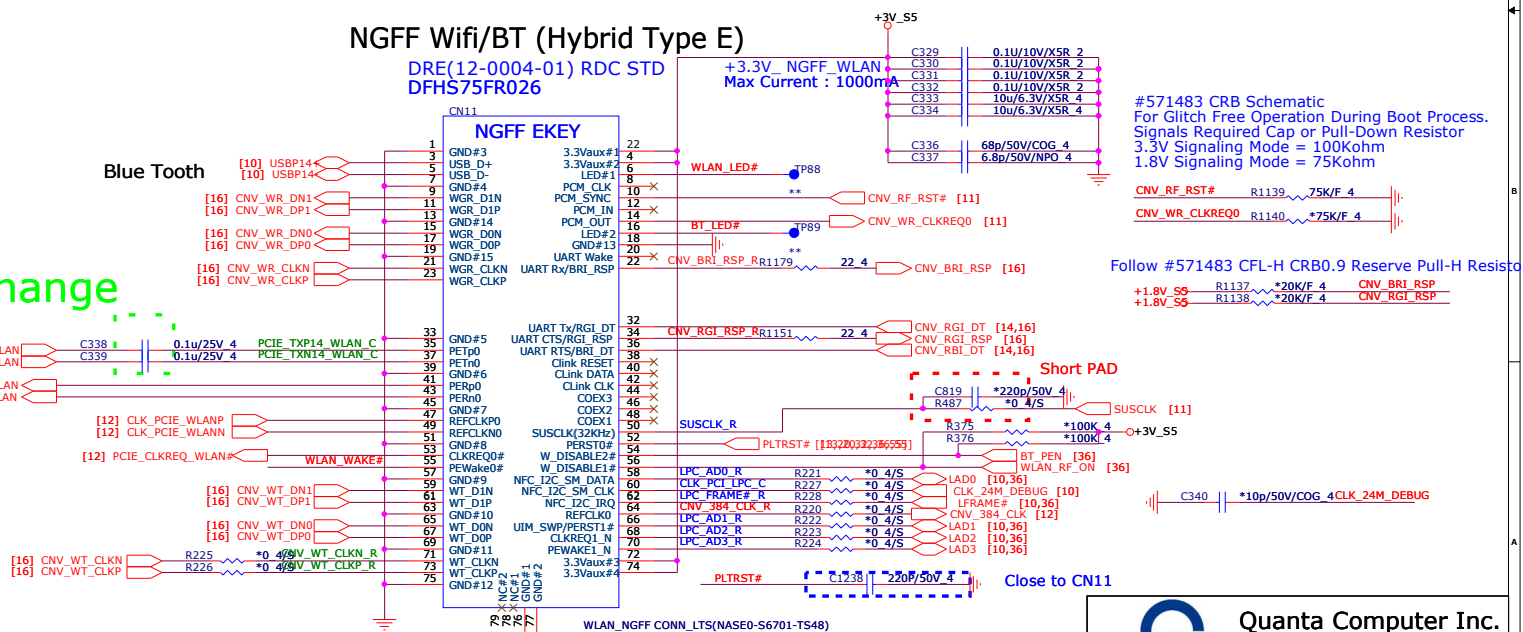
## Blue Tooth

## 1127 Change

WIFI



AC Mode : Support wakle on LAN
DC Mode : Don't support wake on LAN



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Size Document Number  
SSD/WLAN  
Date: Thursday, January 18, 2018 Sheet 32 of 59

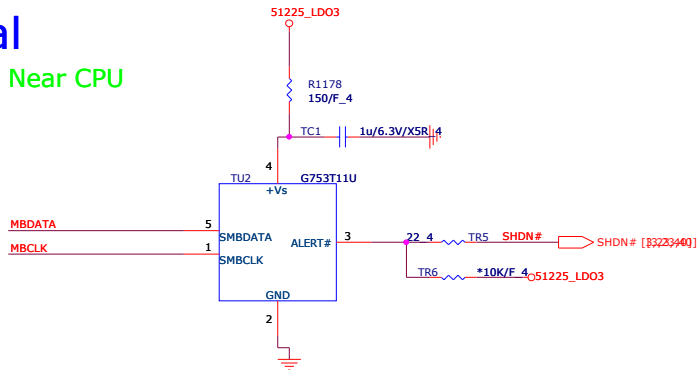




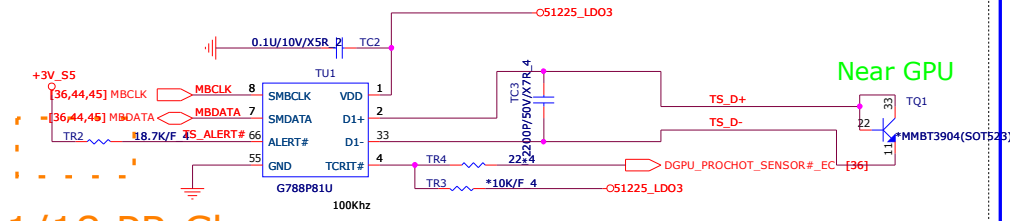


Thermal

Near CPU



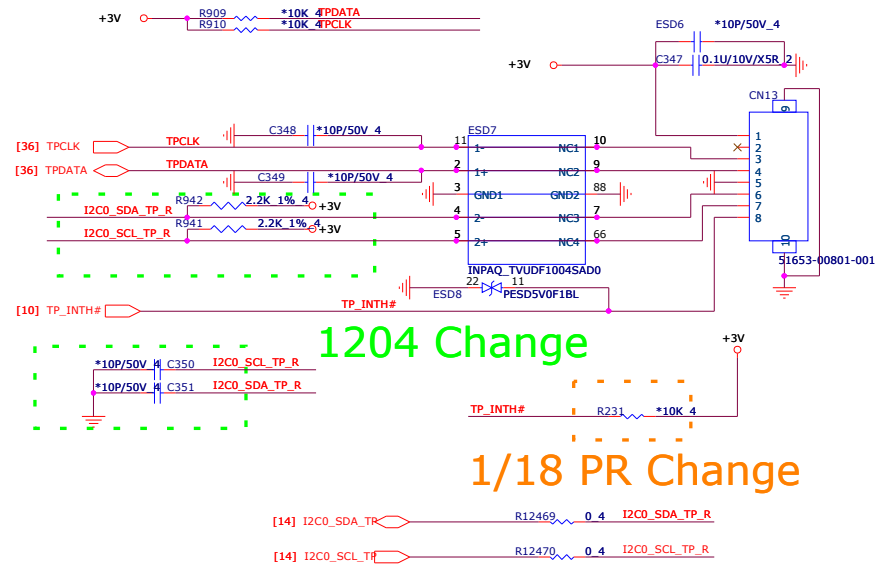
1/18 PR Change



Near GPU

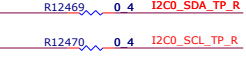
Touch Pad Connector AA type

34



1204 Change

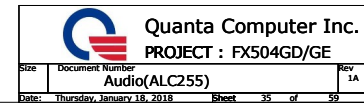
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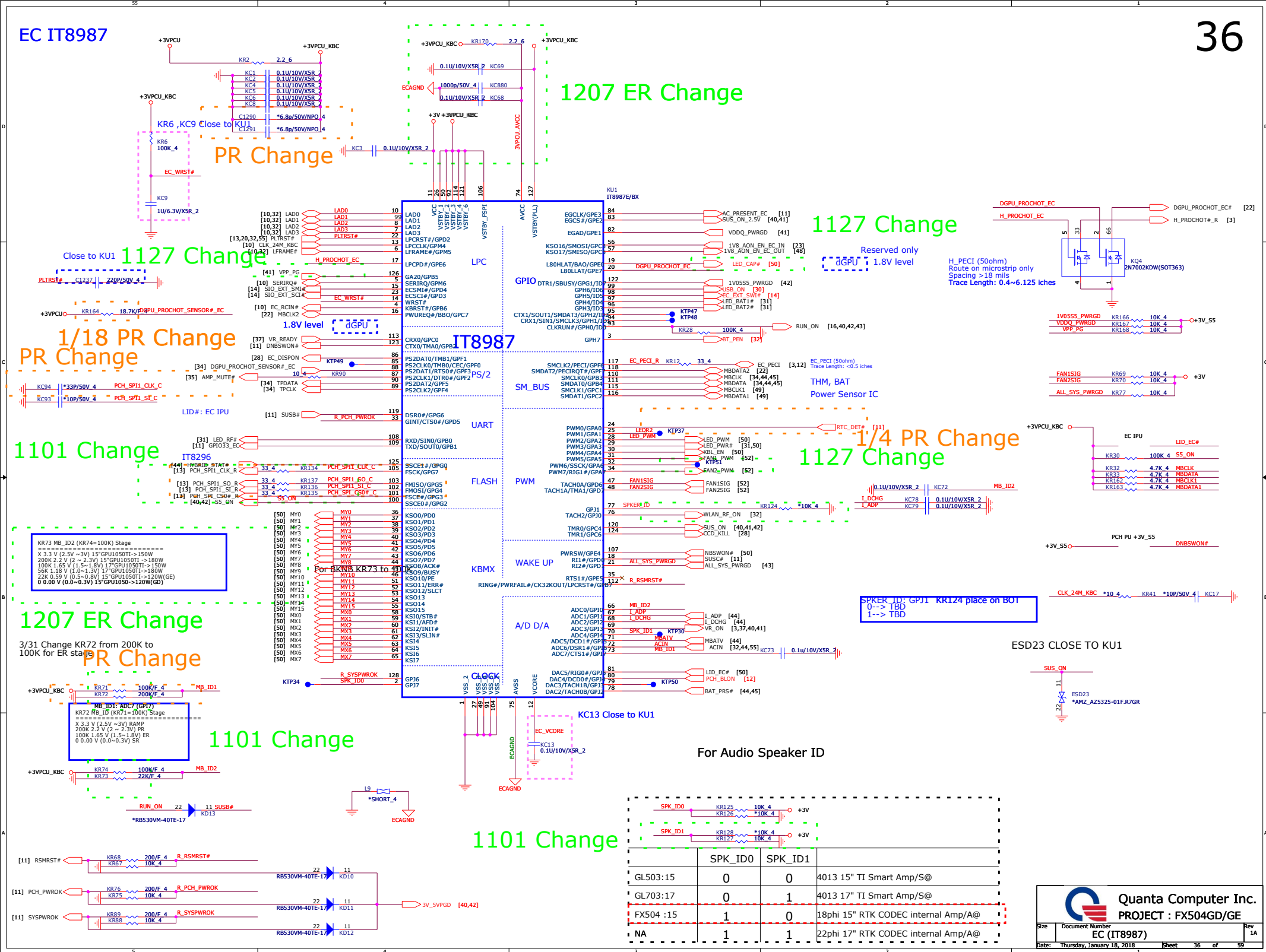
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Size	Document Number	Rev
	TP/Thermal	1A
Date:	Thursday, January 18, 2018	Sheet 34 of 59













45W H62: Max=11.1A, PL2=10A

22

7x3				
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PC  
22u/6[illegible]

10. *Journal of the American Academy of Religion*, 46 (1978), 1–24.

10. *Journal of the American Academy of Religion*, 46 (1978), 1–24.

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Quanta Computer Inc.

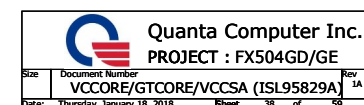
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Document Number  
VCCORE/GTCORE/VCCSA (ISL95829A) Rev 1

Monday, January 18, 2018 Sheet 37 of 59

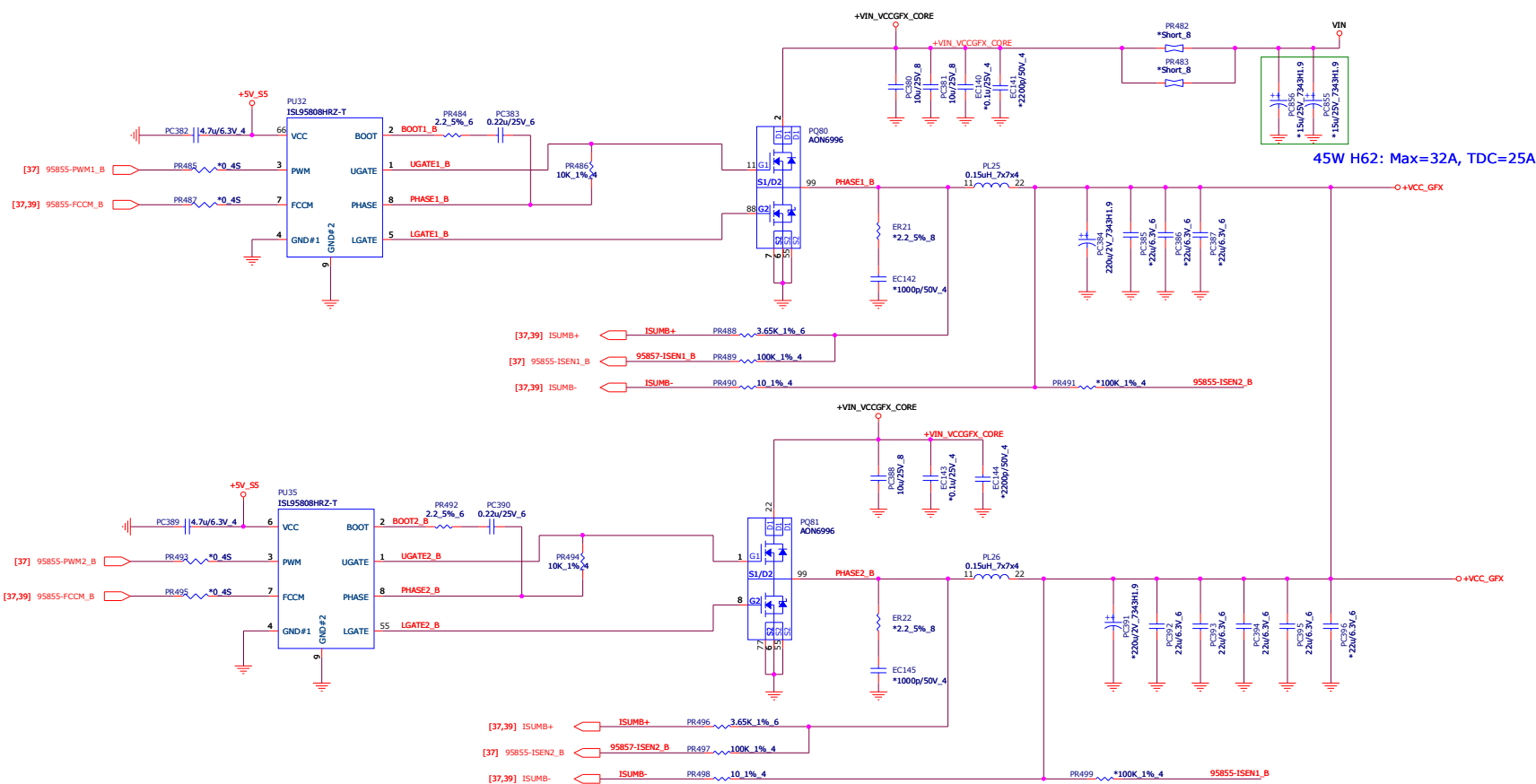
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## GFX\_CORE

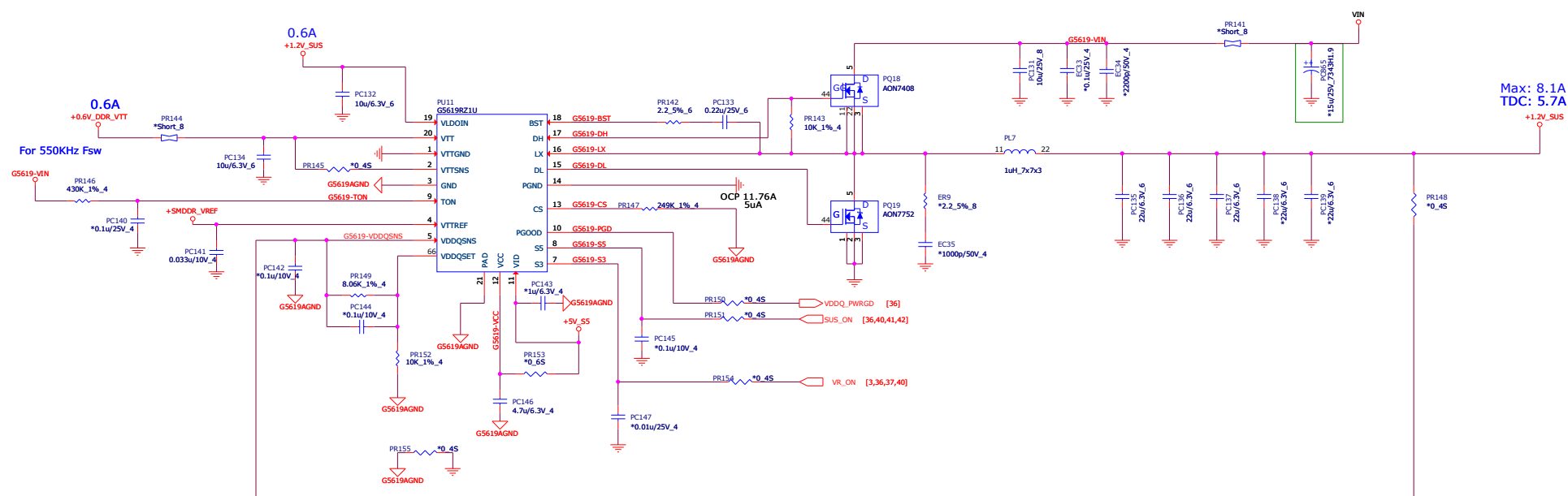




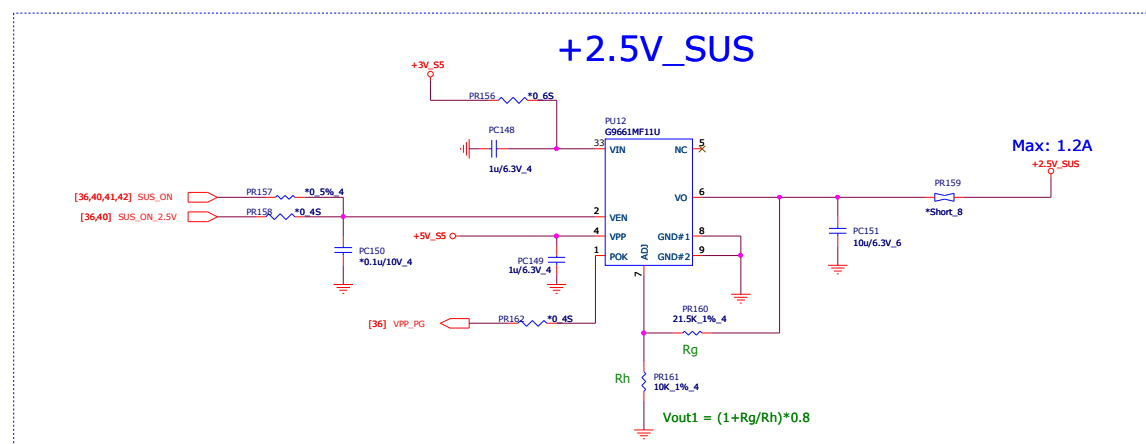




## 1.2VSUS &amp; VTT\_MEM

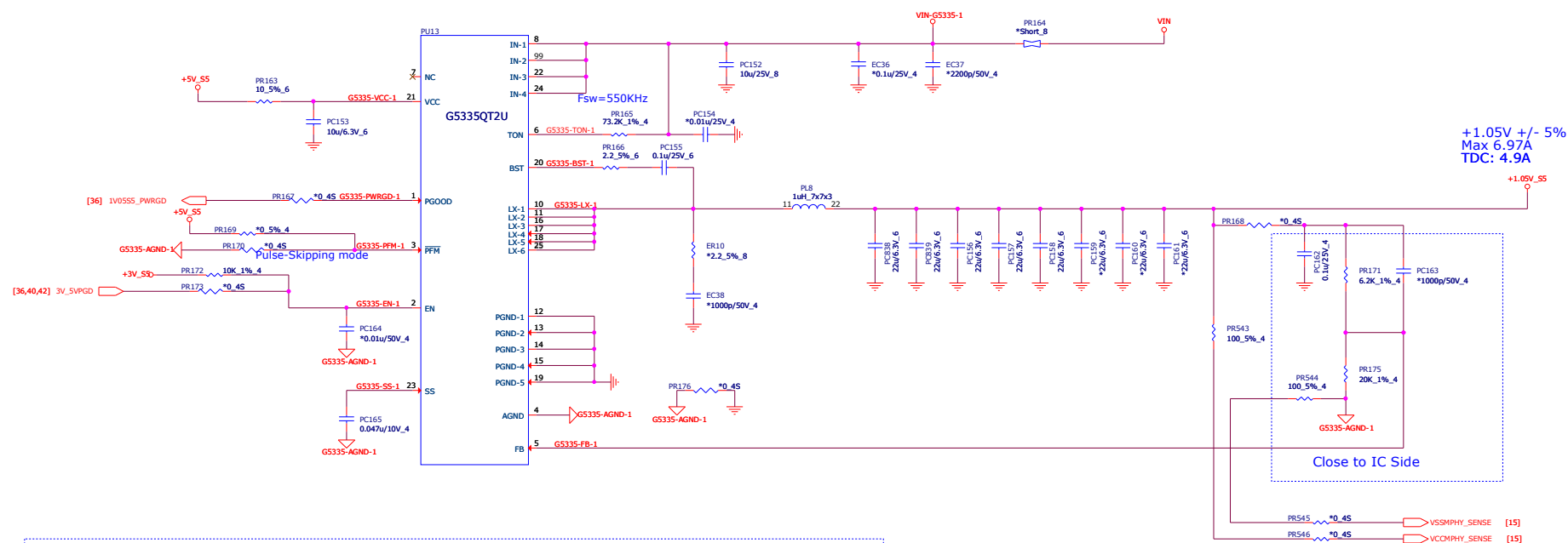


STATE	S3	S5	1.35VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off

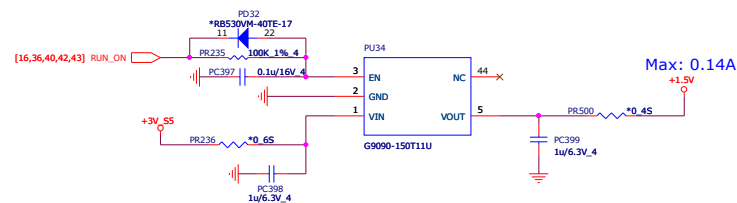




## +1.05V\_S5

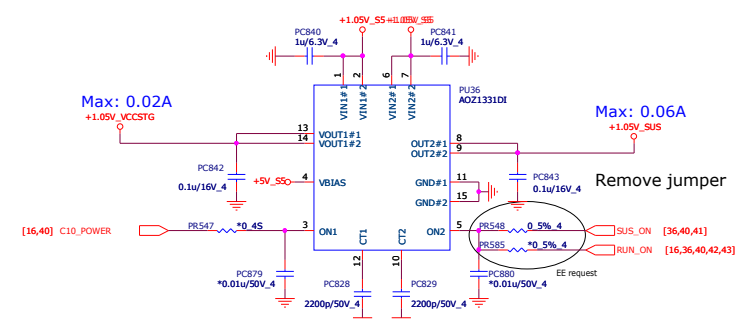
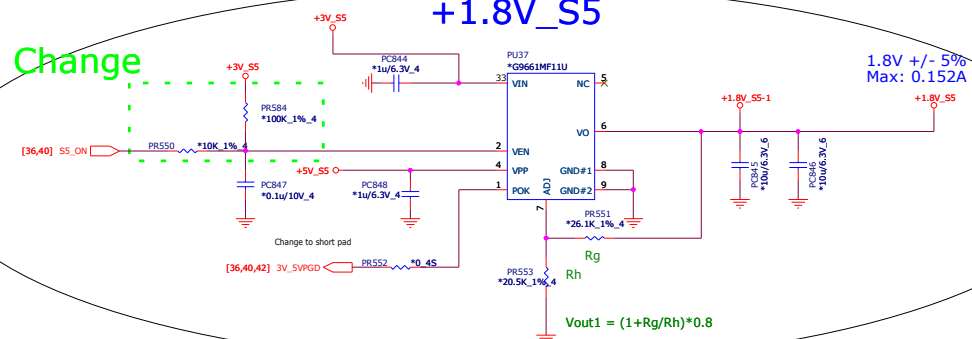


## +1.5V



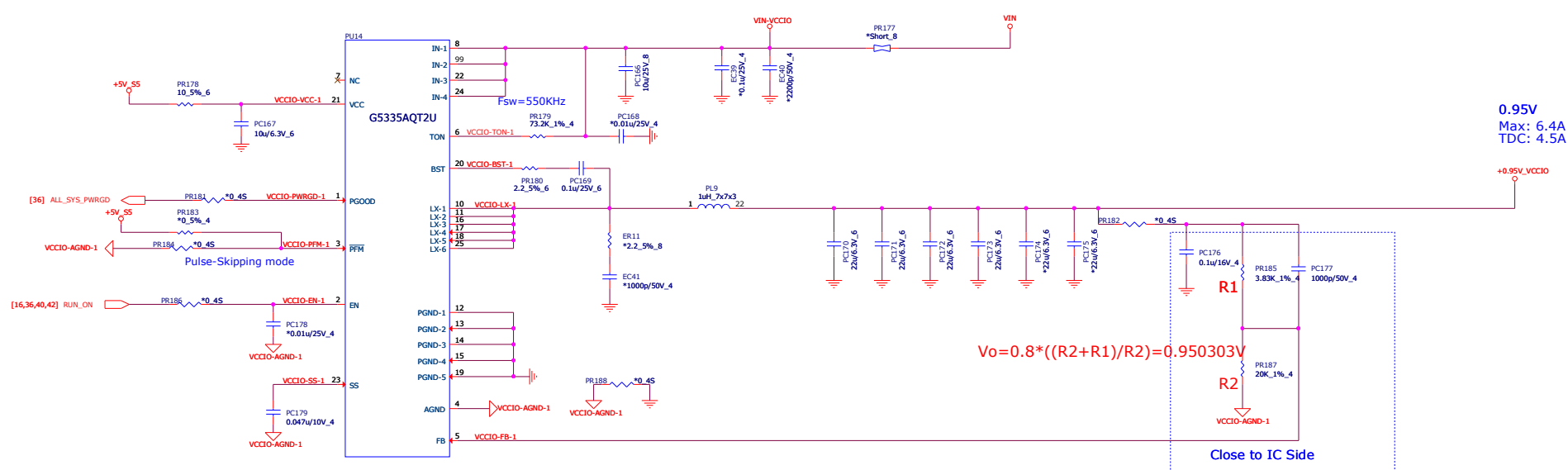
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1101 Change

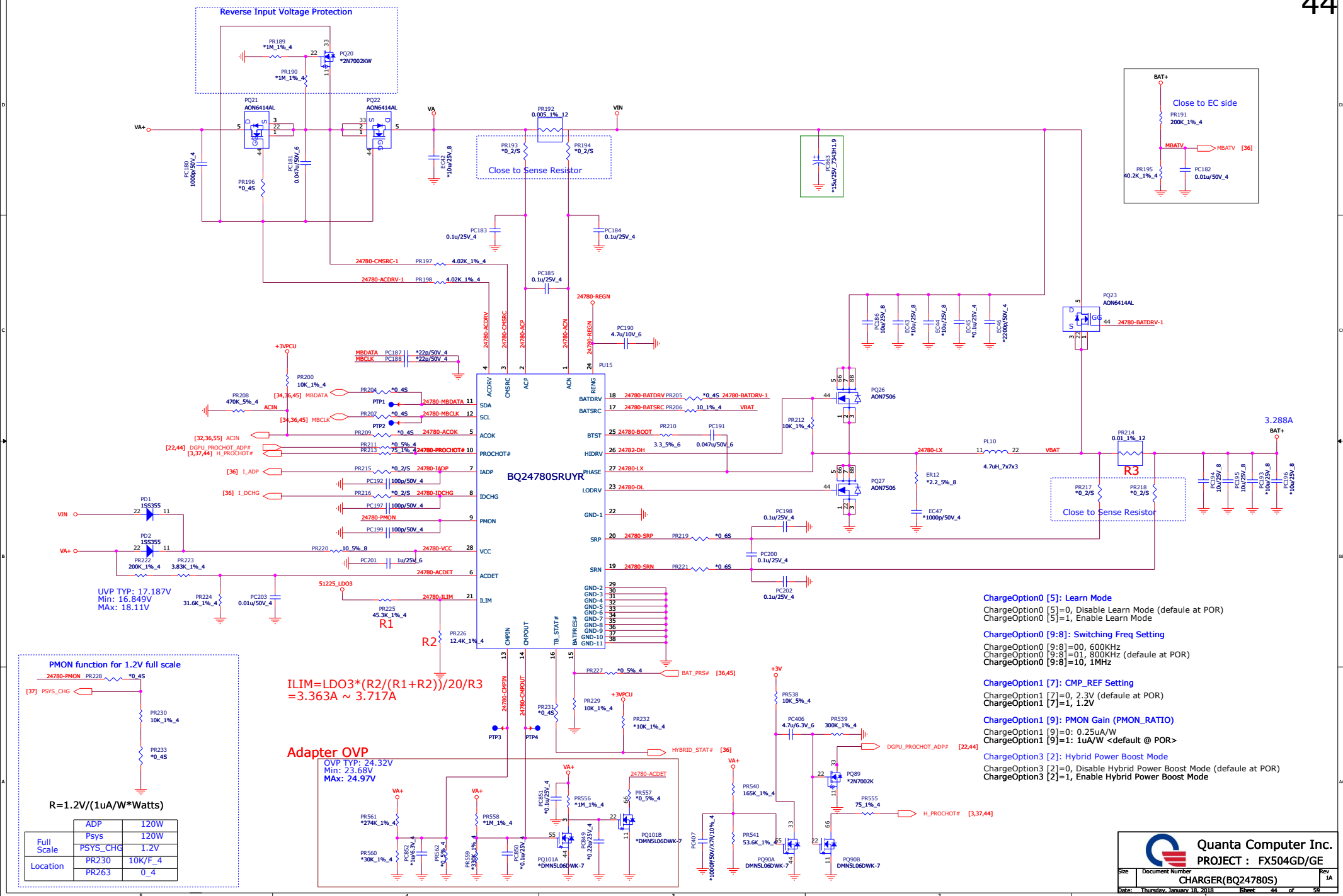




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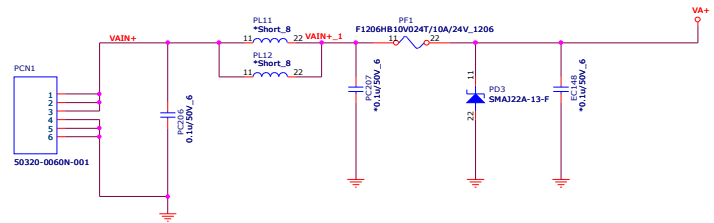




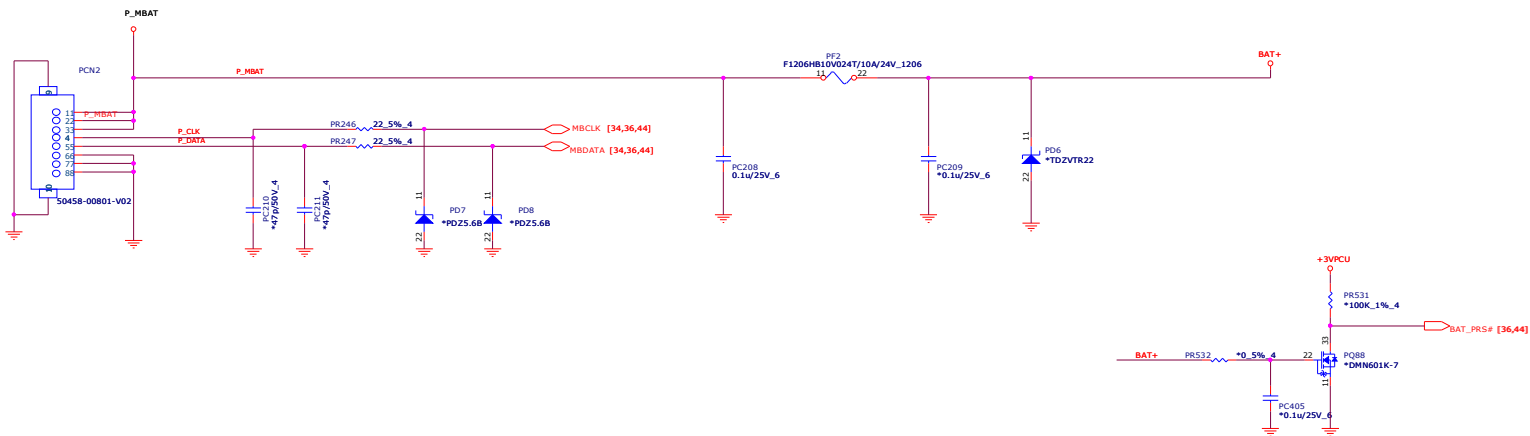


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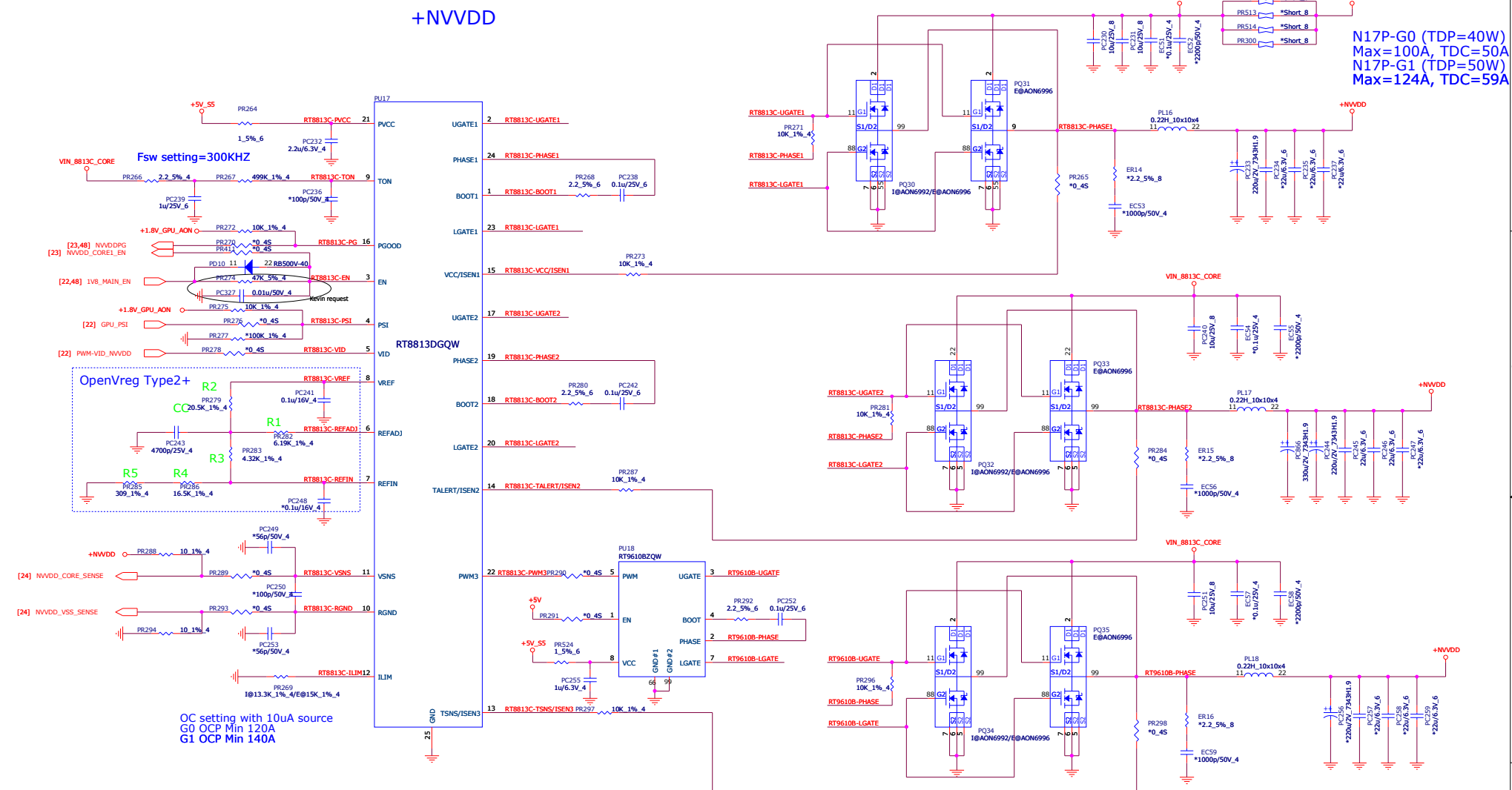
AC ADAPTOR IN CONN



# BAT IN

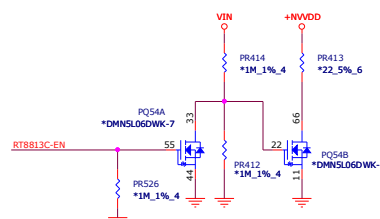




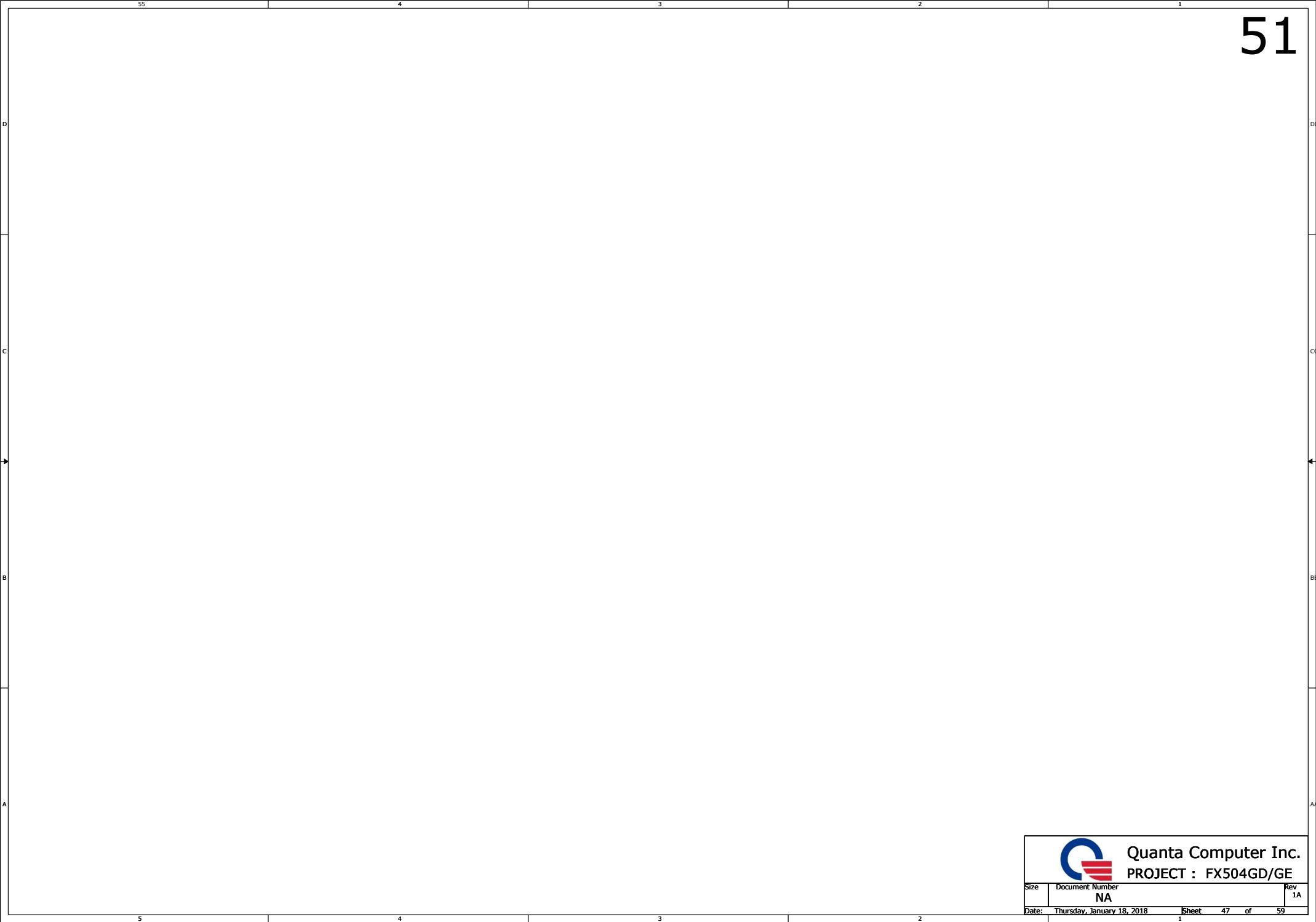



GPU\_PSI Status:

PSI Voltage	Operating Phase Number
0V~0.4V	1 phase with DEM
0.8V~1V	<b>1 phase with CCM</b>
1.4V~5.5V	Active phase with CCM (Only for 2 or 3 hases)



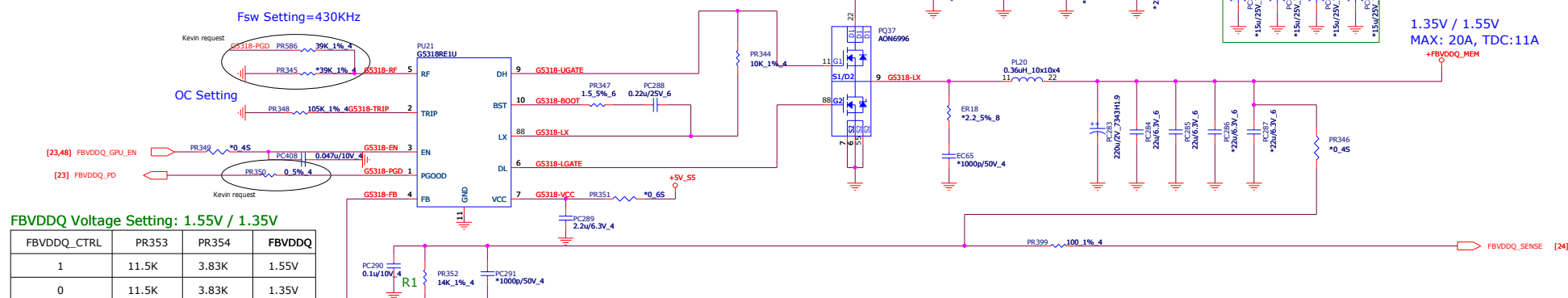




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		<b>PROJECT : FX504GD/GE</b>	
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	NA		1A
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FBVDDQ - 1.5V\_GPU



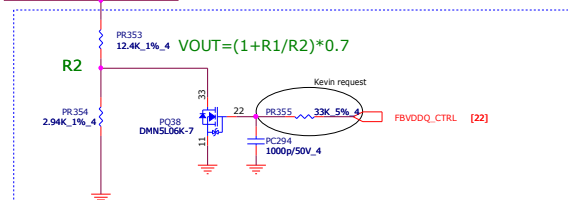
**FBVDDQ Voltage Setting: 1.55V / 1.35V**

FBVDDQ_CTRL	PR353	PR354	FBVDDQ
1	11.5K	3.83K	1.55V
0	11.5K	3.83K	1.35V

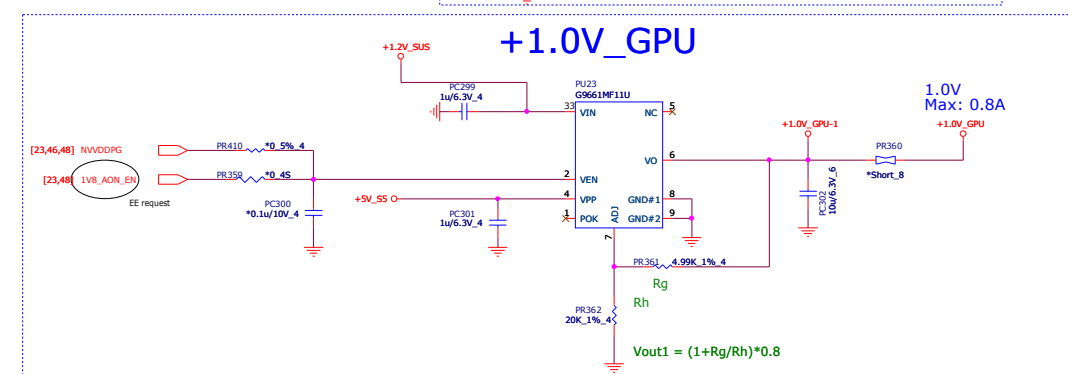
Adjust output to 1.55V/1.35V

FBVDDQ Voltage Setting: 1.50V / 1.35V

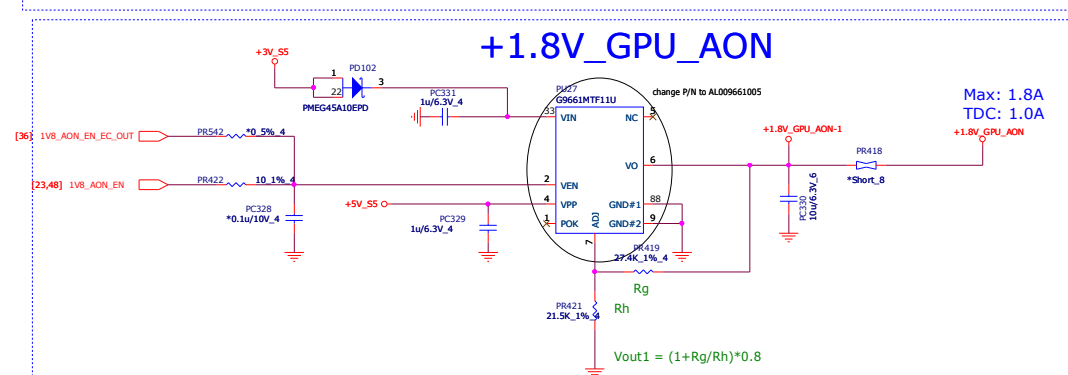
FBVDDQ_CTRL	PR353	PR354	FBVDDQ
1	12.4K	2.94K	1.50V
0	12.4K	2.94K	1.35V



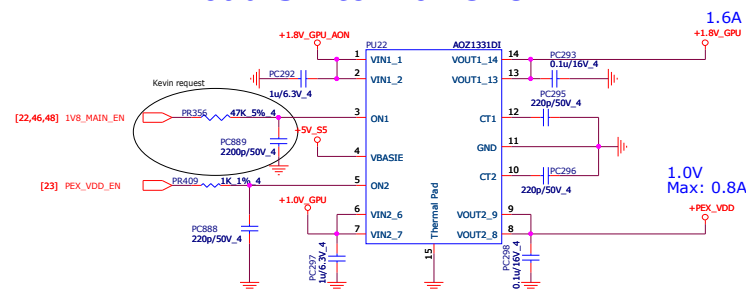
## +1.0V\_GPU



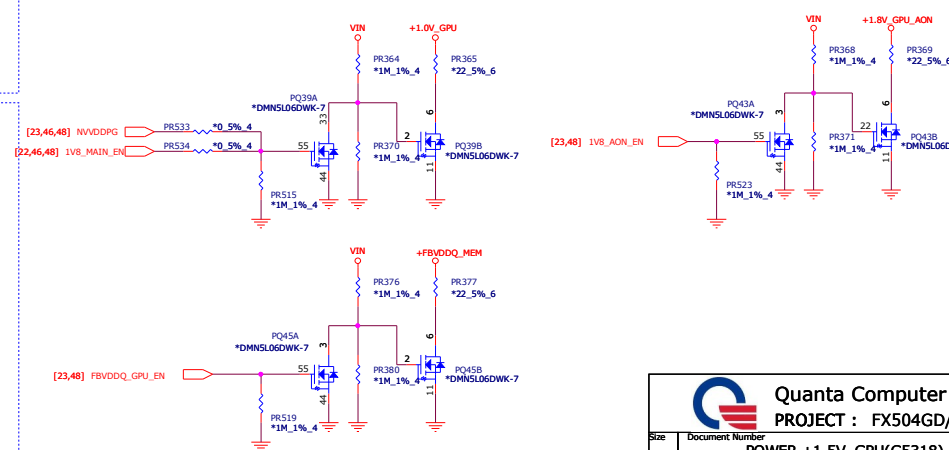
## +1.8V\_GPU\_AON



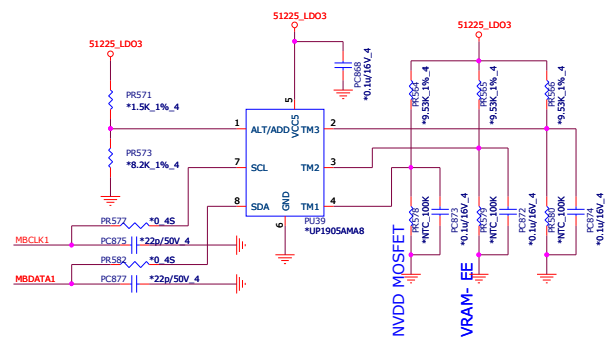
## Load Switch for GPU



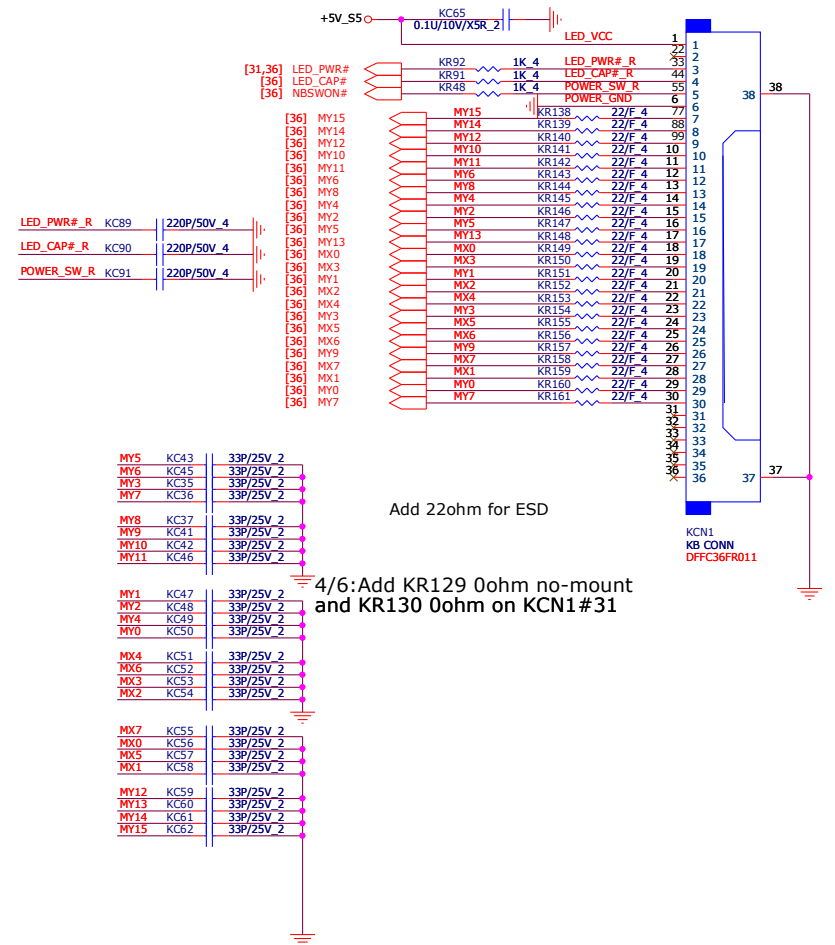
## Discharge



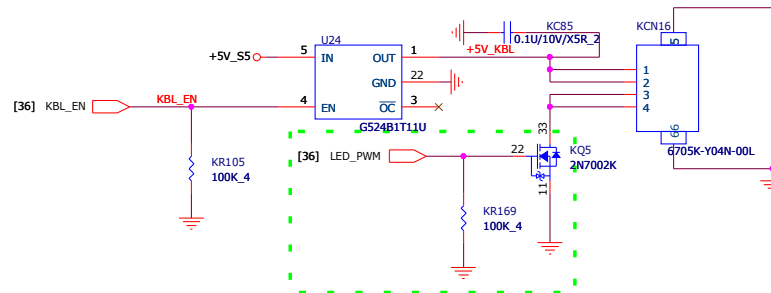






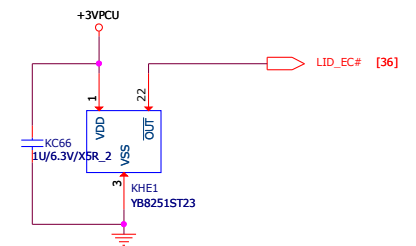
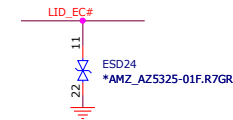


## KEYBOARD BACKLIGHT Con.




1127 Change

## ESD23 CLOSE TO KHE1







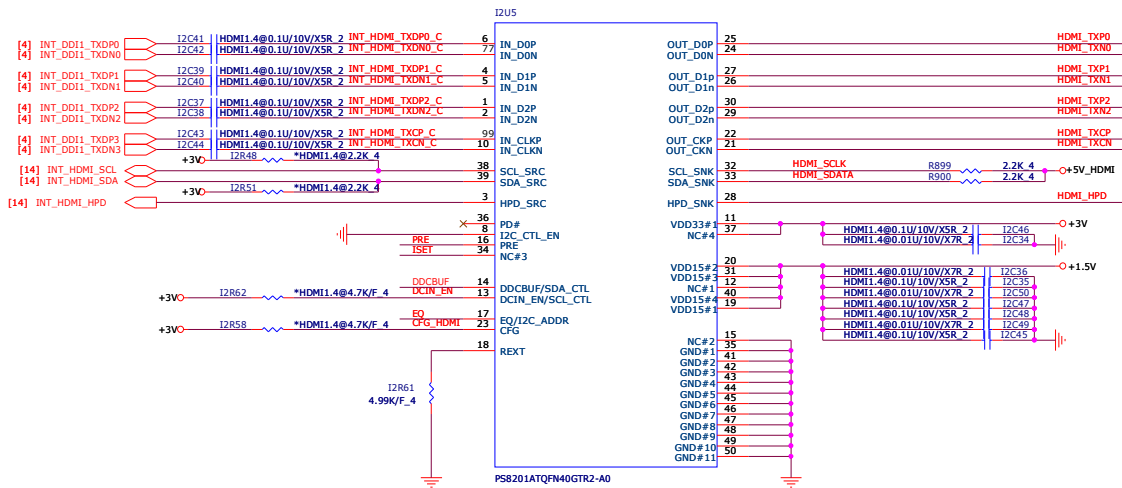
			<b>Quanta Computer Inc.</b>		
			<b>PROJECT : FX504GD/GE</b>		
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	N.A				1A
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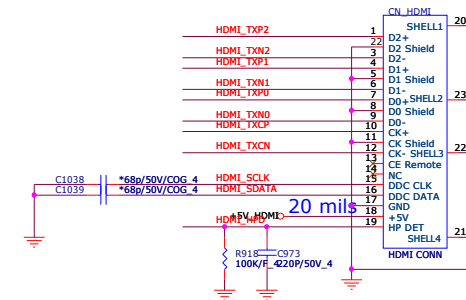
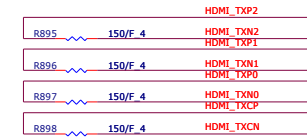




## HDMI 1.4 Re-Drive

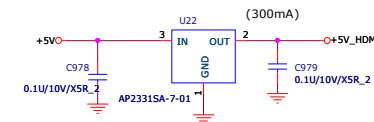


## EMI Solution



4/5:Change C1038,C1039 from mount 68P to no-mount for EA pass

4/5:Change I2R61 from 3.9K to 4.99K for EA



**ISET** For PS8407A only

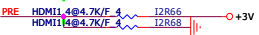
TMDS output swing adjustment; Internal pull down at ~150k $\Omega$ , 3.3V I/O  
 L: default  
 H: increase +13%  
 M: reduce -13%



CFG

Configuration pin, 3.3V IO, internal pull down at ~150kΩ. 3.3V I/O.  
L: HDMI ID disable  
H: HDMI ID enable

## 1124 Change



## PRE

Output pre-emphasis setting; Internal pull down at  $\sim 150\text{k}\Omega$ , 3.3V I/O.  
L: no pre-emphasis  
H: 1.6dB pre-emphasis  
M: 2.5dB pre-emphasis



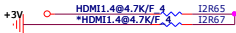
## DDCBUF

Enable active DDC buffer, Internal pull down 150Kohm+-20%, 3.3V I/O

L: Passive DDC pass-through (Default)

H: Active DDC buffer with default threshold

M: Active DDC buffer without internal pull up resistor

EQ

HDMI14@4.7K/F-4 12R04

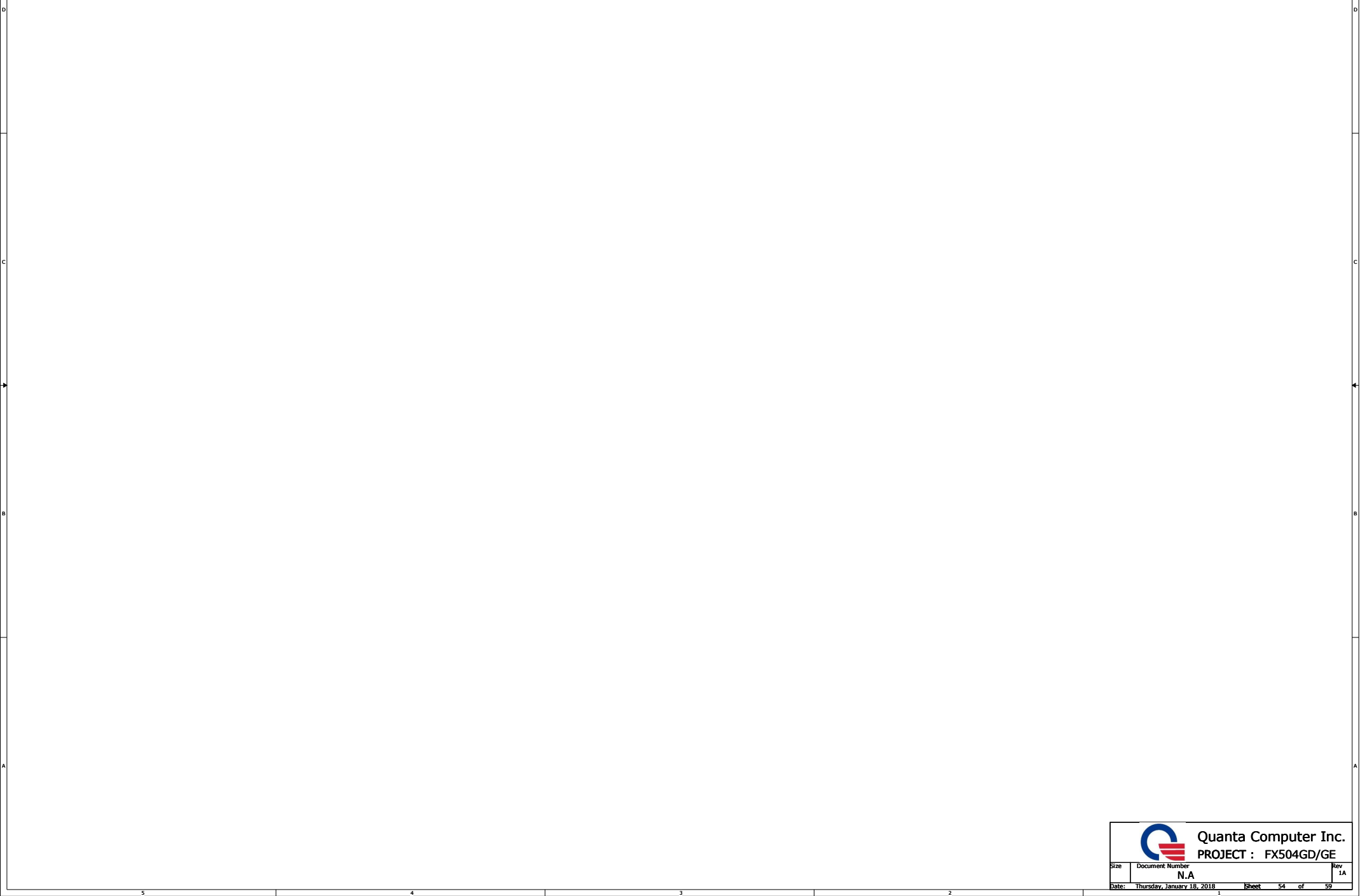


EQ

**For PS8407A**  
Receiver equalization setting; Internal pull down at  $\sim 150\text{k}\Omega$ , 3.3V I/O.  
L: programmable EQ for channel loss up to 12.4dB  
H: programmable EQ for channel loss up to 4.3dB  
M: programmable EQ for channel loss up to 8.6dB

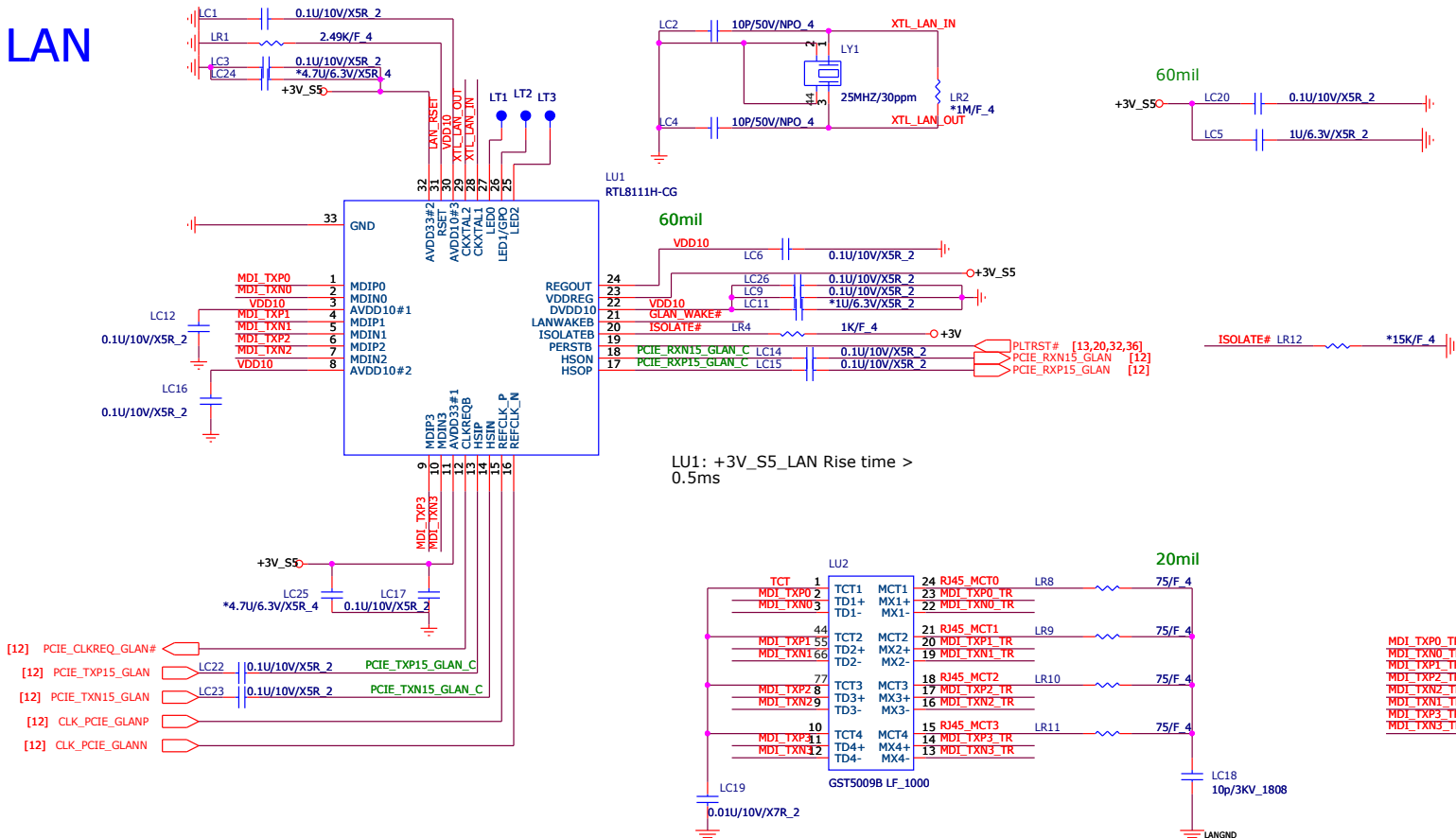
**For PS8201A**  
Receiver equalization setting; Internal pull down at  $\sim 150\text{k}\Omega$ , 3.3V I/O.  
L: programmable EQ for channel loss up to 6.5dB @ 3Gbps  
H: programmable EQ for channel loss up to 9.5dB @ 3Gbps  
M: programmable EQ for channel loss up to 3dB @ 3Gbps



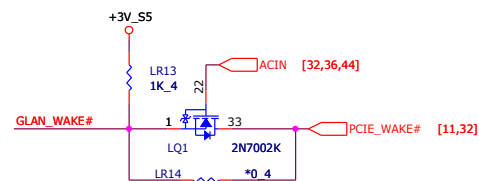
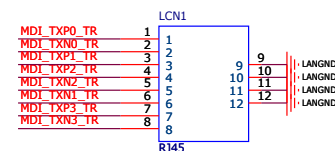
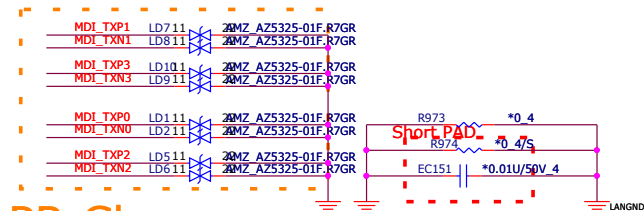
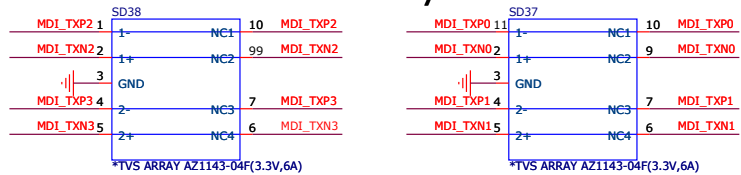




LAN

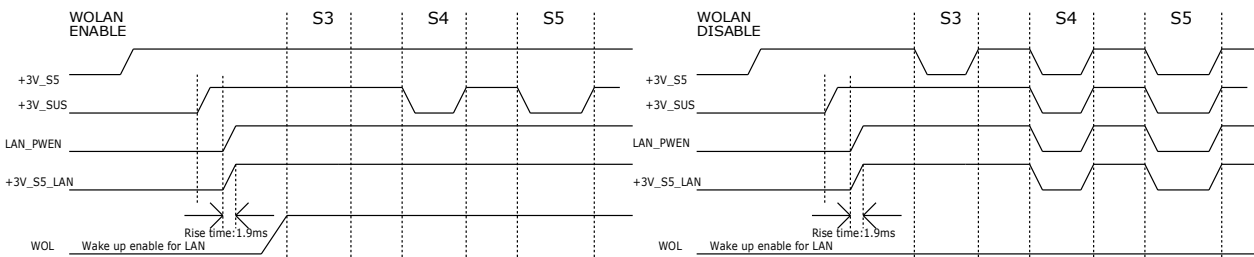


## ESD CO-Lay



AC Mode : Support wakle on LAN  
DC Mode : Don't support wake on LAN

## PR Change



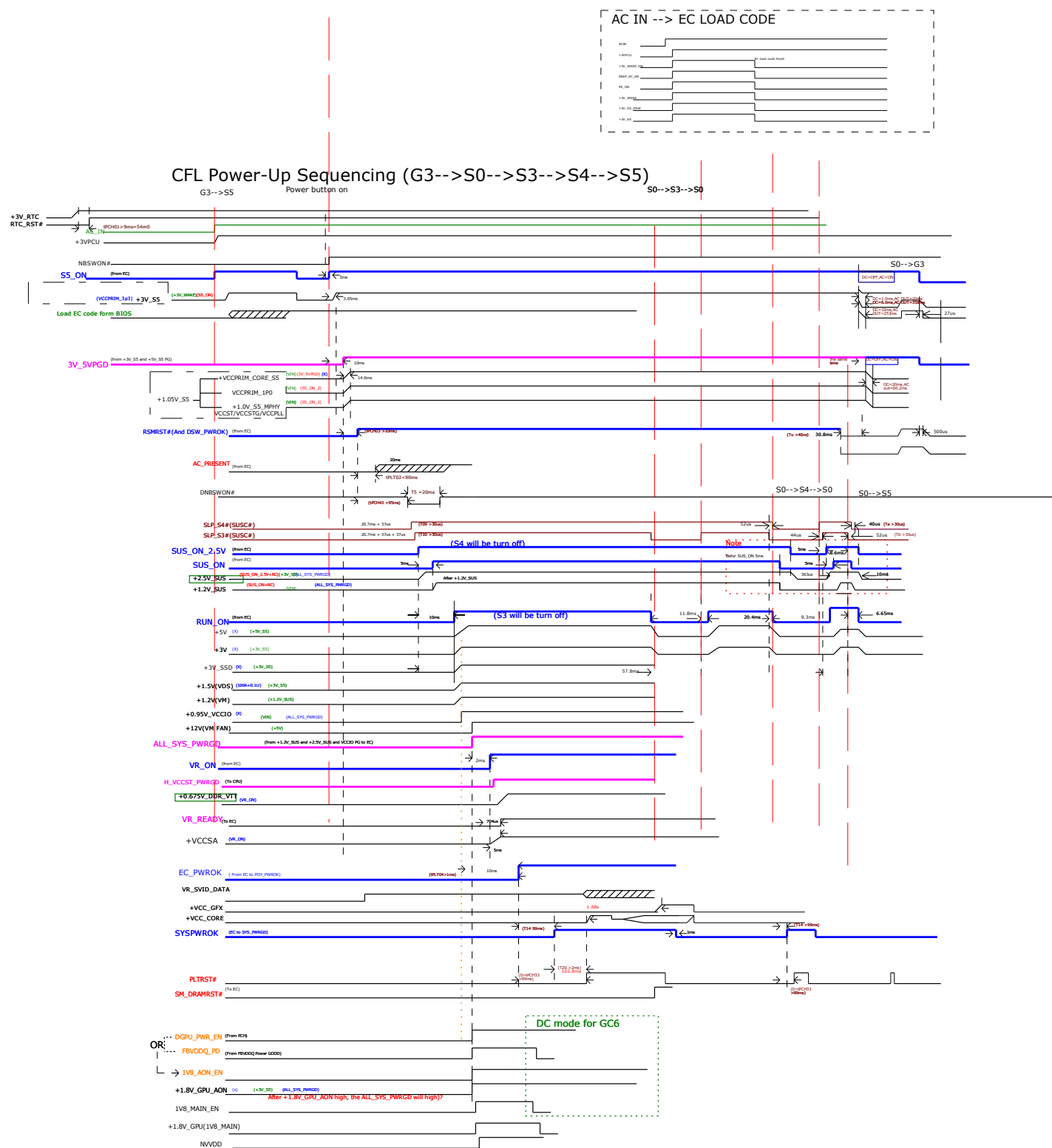
BIOS Setup	WOLAN DISABLE		WOLAN ENABLE	
	LAN_PWEN	WOL	LAN_PWEN	WOL
S3	H	H	H	H
S4	L	L	H	H
S5	L	L	H	H



Quanta Computer Inc.  
PROJECT : FX504GD/GE

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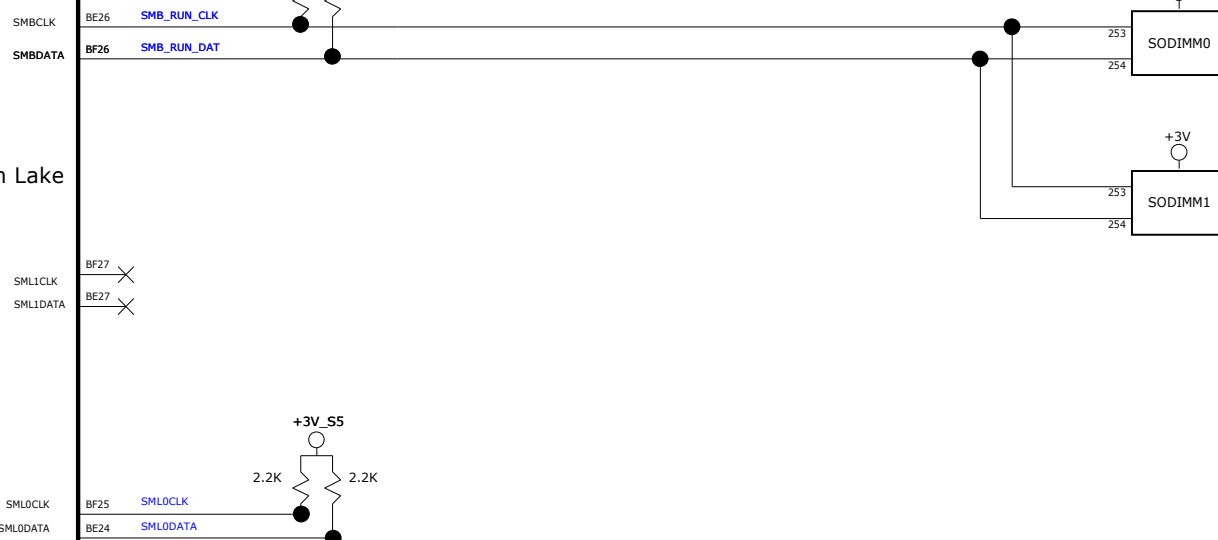




OS status	S0	S3		(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	
H/W status	S0	S3		S4 (Win10 off) RTC wake Enable WOLAN Enable	S4 (Win10 off) RTC wake Disable WOLAN Disable	S5 (Fast Startup "v")	S5 (Fast Startup "x")	
RUN_ON	H	L		L	L	L	L	
+3V	H	L		L	L	L	L	
+5V	H	L		L	L	L	L	
+0.675V_DDR_VTT	H	L		L	L	L	L	
+12V	H	L		L	L	L	L	
+3V_SSD/+3V_PCH_CARD/+1.5V	H	L		L	L	L	L	
+1.05V_VCCSTG	H	L		L	L	L	L	
+VCCSA	H	L		L	L	L	L	
+VCC_GFX	H	L		L	L	L	L	
+VCC_CORE	H	L		L	L	L	L	
+0.95V_VCCIO	H	L		L	L	L	L	
SUS_ON	H	H		L	L	L	L	
+1.05V_VCCPLL/+1.05V_VCCST	H	H		L	L	L	L	
+1.05V_SUS	H	H		L	L	L	L	
+1.2V_SUS	H	H		L	L	L	L	
SUS_ON_2.5V	H	H		L	L	L	L	
+2.5V_SUS	H	H		L	L	L	L	
S5_ON	H	H		HH	L	L	L	
+1.8V_S5	HH	H		H	L	L	L	
+1.05V_S5	H	HH		H	L	L	L	
S5_ON	H	HH		HH	L	HH	L	
+3V_S5	H	H		H	L	H	L	
+5V_S5	H	H		H	L	H	L	



# Cannon Lake PCH-H



# EC IT8987E

