


# B450 AORUS ELITE V2

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**2015.12.30--B.L**

<http://www.repair1.ru/>

			
Title			
<h2 style="margin: 0;">COVER SHEET</h2>			
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Customer			
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**Model Name:B450 AORUS ELITE V2**

### Component value change history


**Version: 1.01**

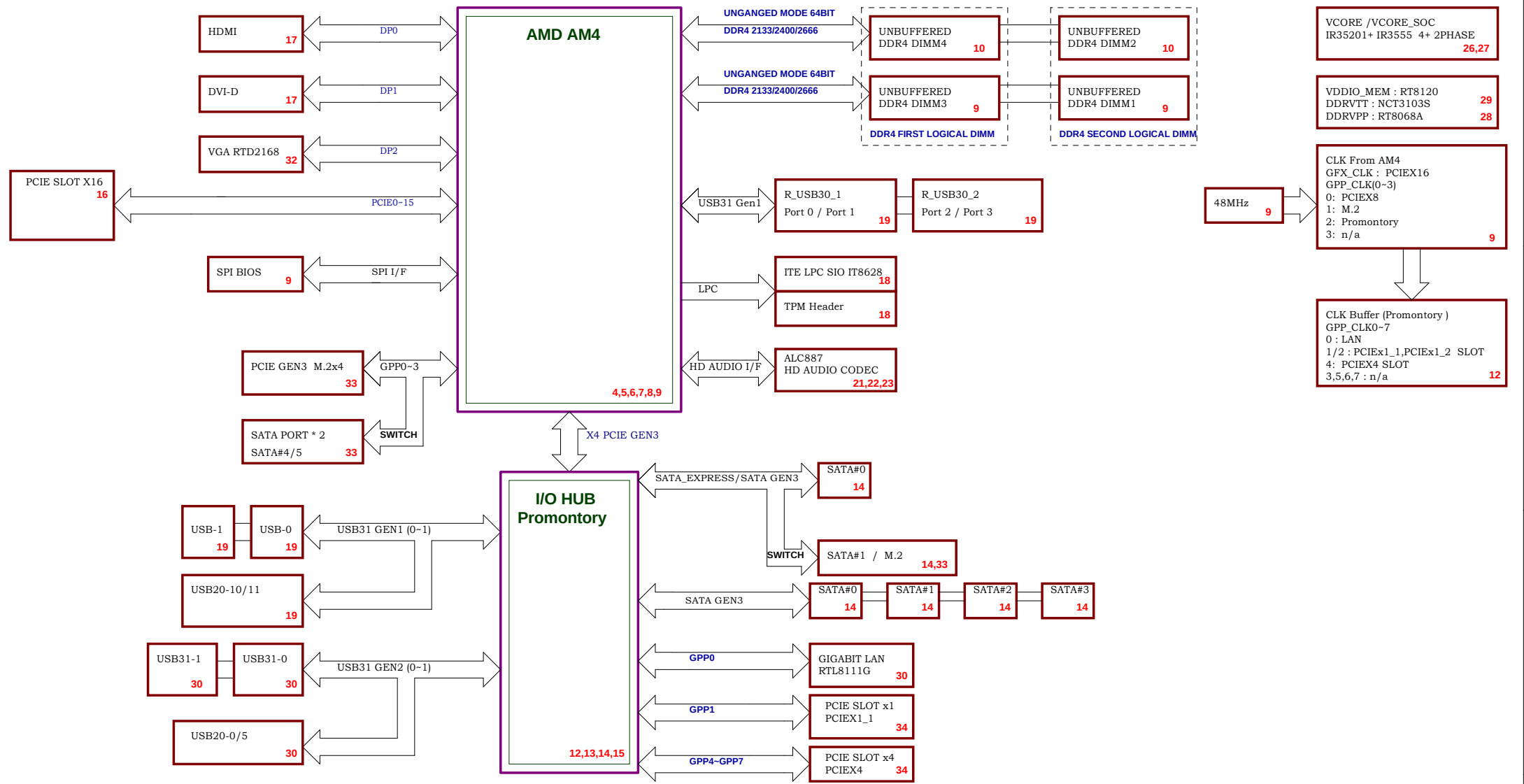
**P-Code: U98126-0**

### Circuit or PCB layout change for next version

[illegible]

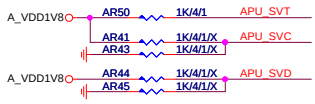
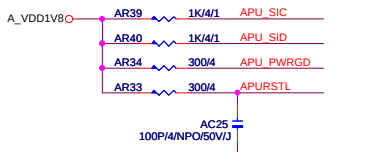
<http://www.repair1.ru/>

			
Title			
BOM & PCB HISTORY			
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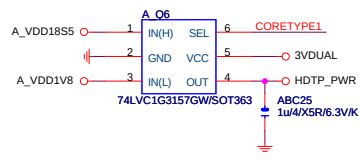
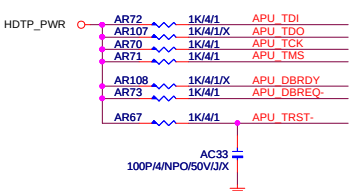


<http://www.repair1.ru/>



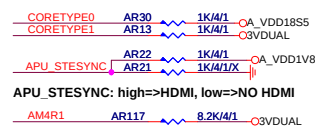
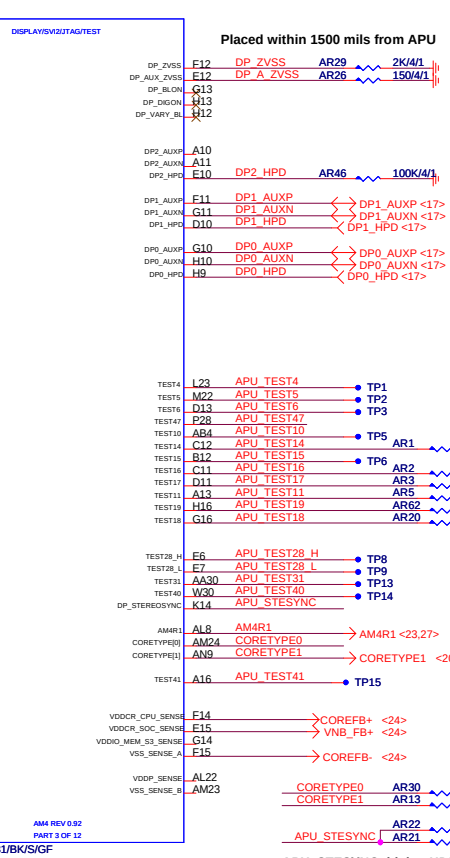
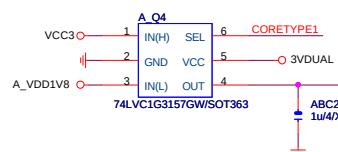
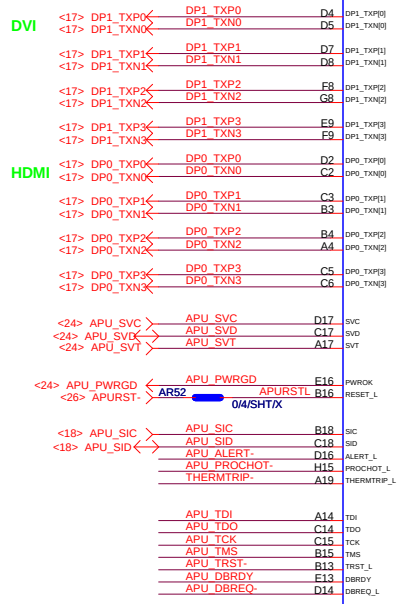


SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



DVI

HDMI



CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h-6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h-0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h-1 Fh	TYPE 3

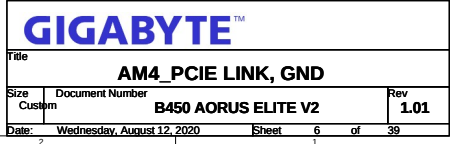
**GIGABYTE**™

Title: **CPU CONTROL**

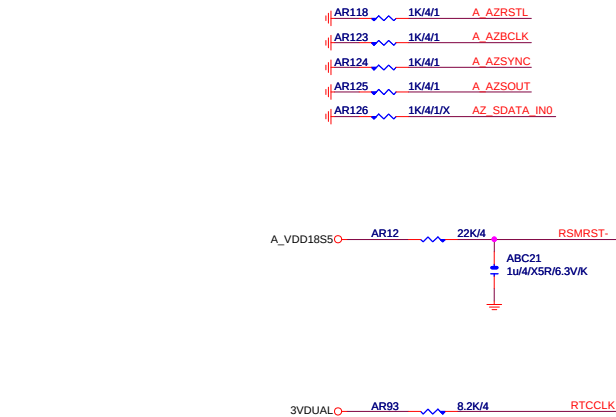
Size: Custom Document Number: **B450 AORUS ELITE V2** Rev: **1.01**

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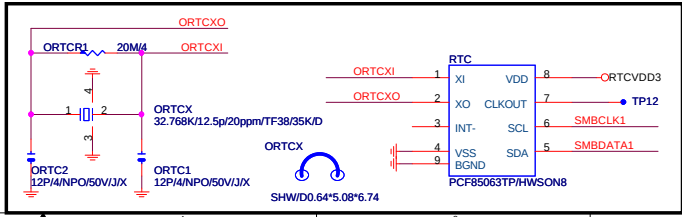
<http://www.repair1.ru/>



TEST0	TEST1	TEST2	Description
0	0	0	FCH JTAG accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH JTAG can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



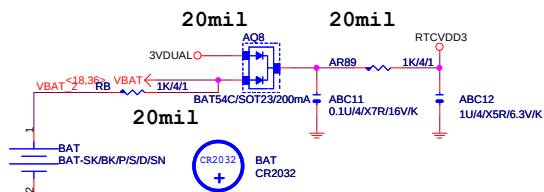
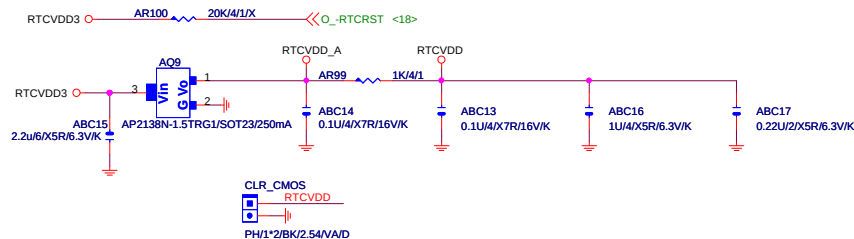
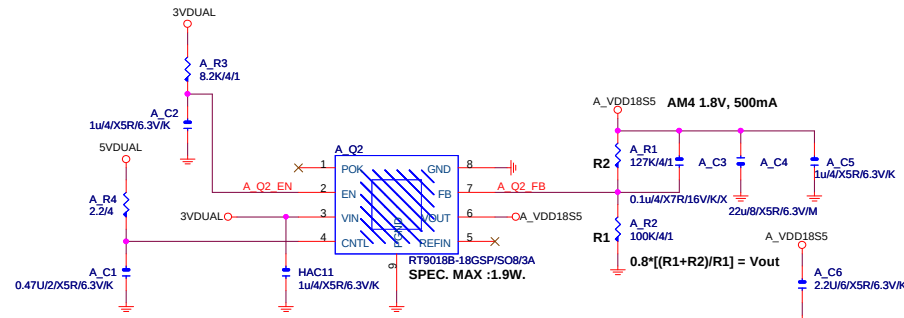
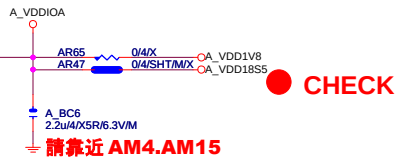
	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI_CLK (ZP)
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48KHz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)	Coin battery is on board. (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48KHz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100MHz PCIE clock as reference clock and generate internal clocks only	Default to traditional reset logic (DEFAULT)	Coin battery is not on board. (DEFAULT)	LPC ROM	short reset mode	Use 100MHz PCIE clock as reference clock and generate internal clocks only
	CZ/ST DIE ONLY						ZP DIE ONLY



GIGABYTE™			
AM4 MISC			
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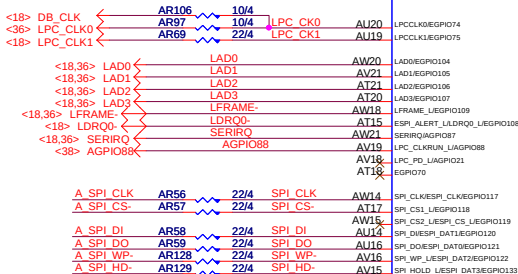
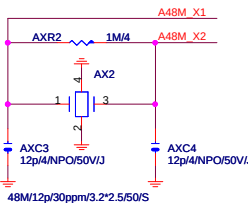
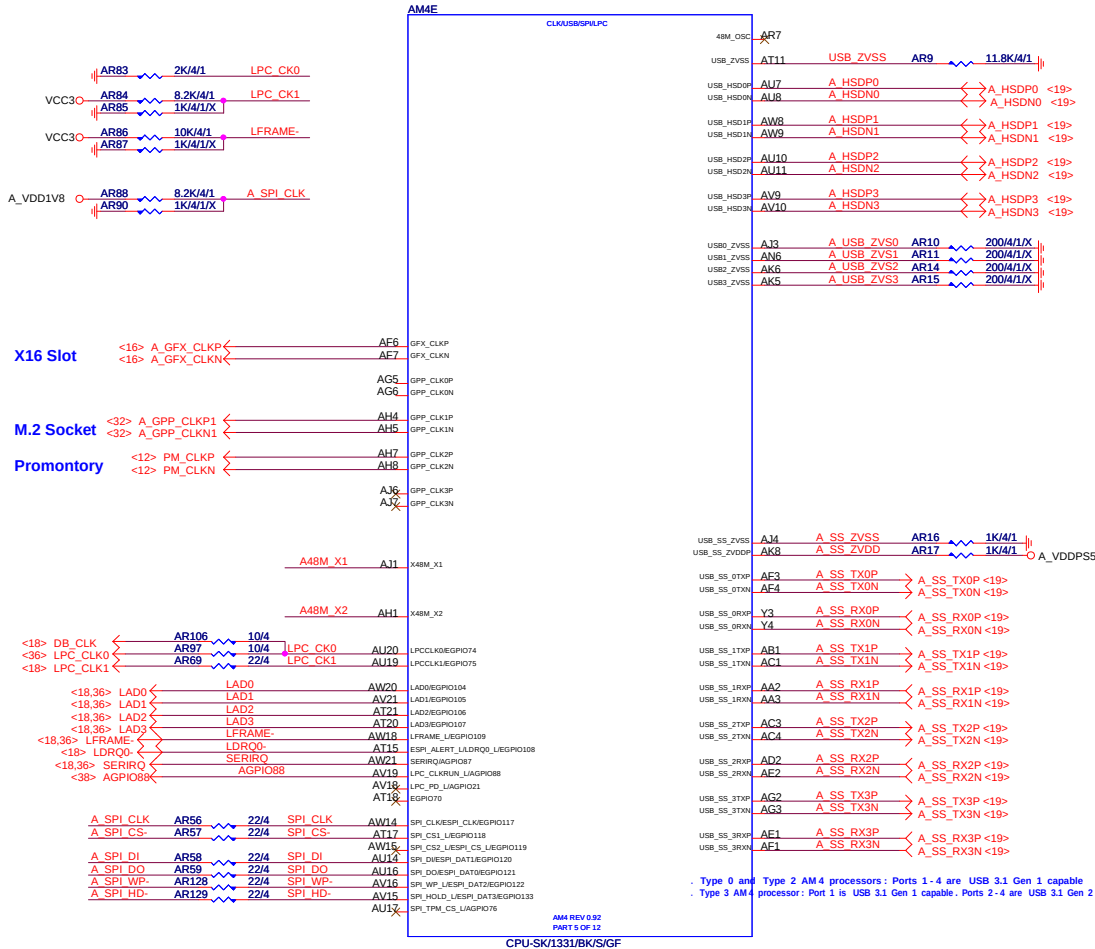
VCORE		VCORE_SOC	
Vcore EDC=125A	Vcore SOC EDC=75A	Vcore SOC EDC=75A	Vcore SOC EDC=75A
Vcore 0.75~1.5V	Vcore SOC 0.75~1.2V	Vcore SOC 0.75~1.2V	Vcore SOC 0.75~1.2V
VCORE	VCORE_SOC	VCORE_SOC	VCORE_SOC



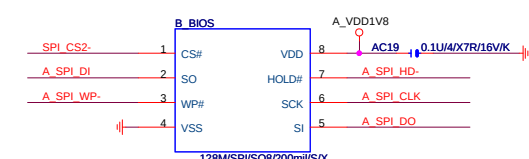
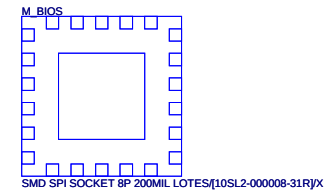
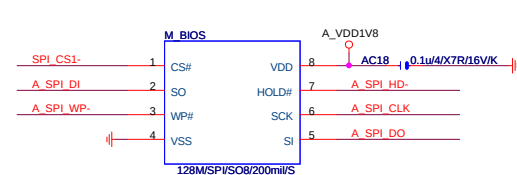
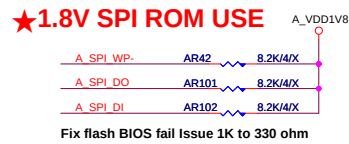
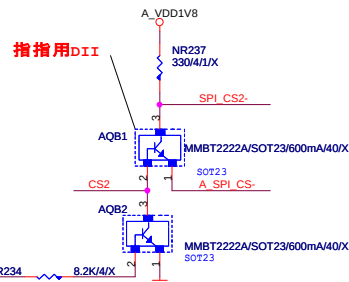
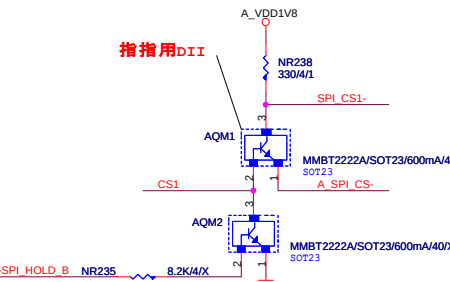
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

**NOT ADD ICT FOR RTCVDD PIN**

			
<b>Title</b> <b>CPU POWER &amp; GND</b>			
<b>Size</b> Custom	<b>Document Number</b> <b>B450 AORUS ELITE V2</b>		<b>Rev</b> <b>1.01</b>
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Type 0 and Type 2 AM4 processors: Ports 1-4 are USB 3.1 Gen 1 capable  
Type 3 AM4 processor: Port 1 is USB 3.1 Gen 1 capable, Ports 2-4 are USB 3.1 Gen 2 capable



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Title

APU USB, GPP

Size

Custom

Document Number

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Rev

1.01

Date

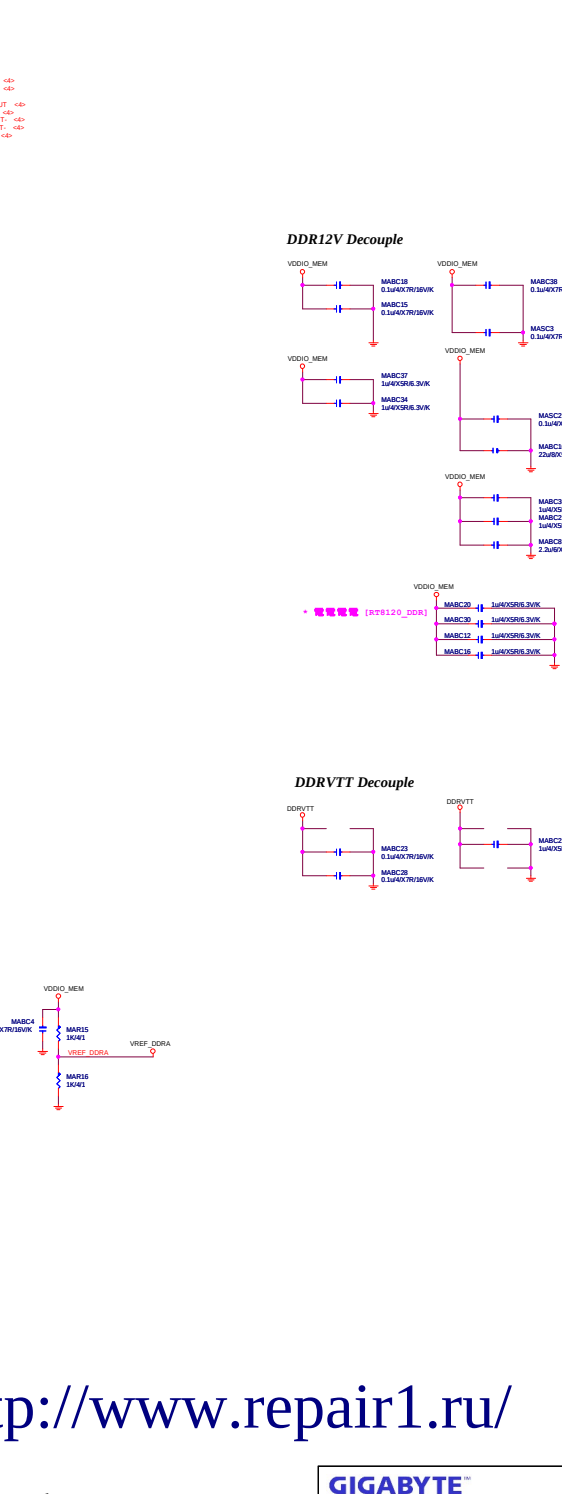
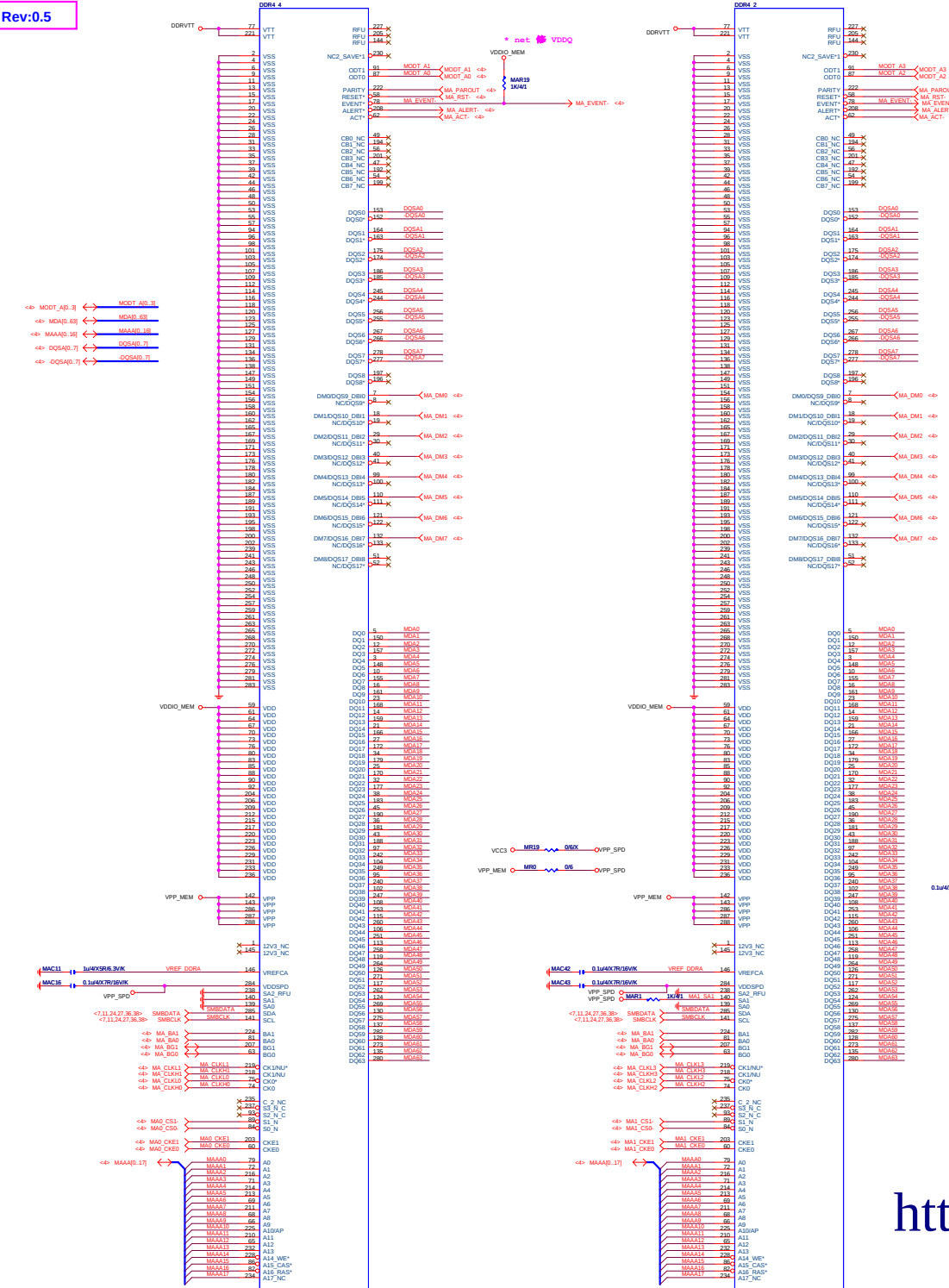
Friday, August 14, 2020

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DDR4 CHANNEL A		
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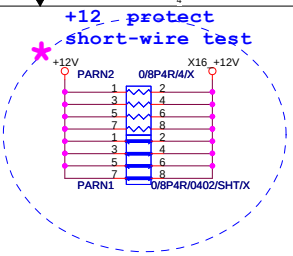
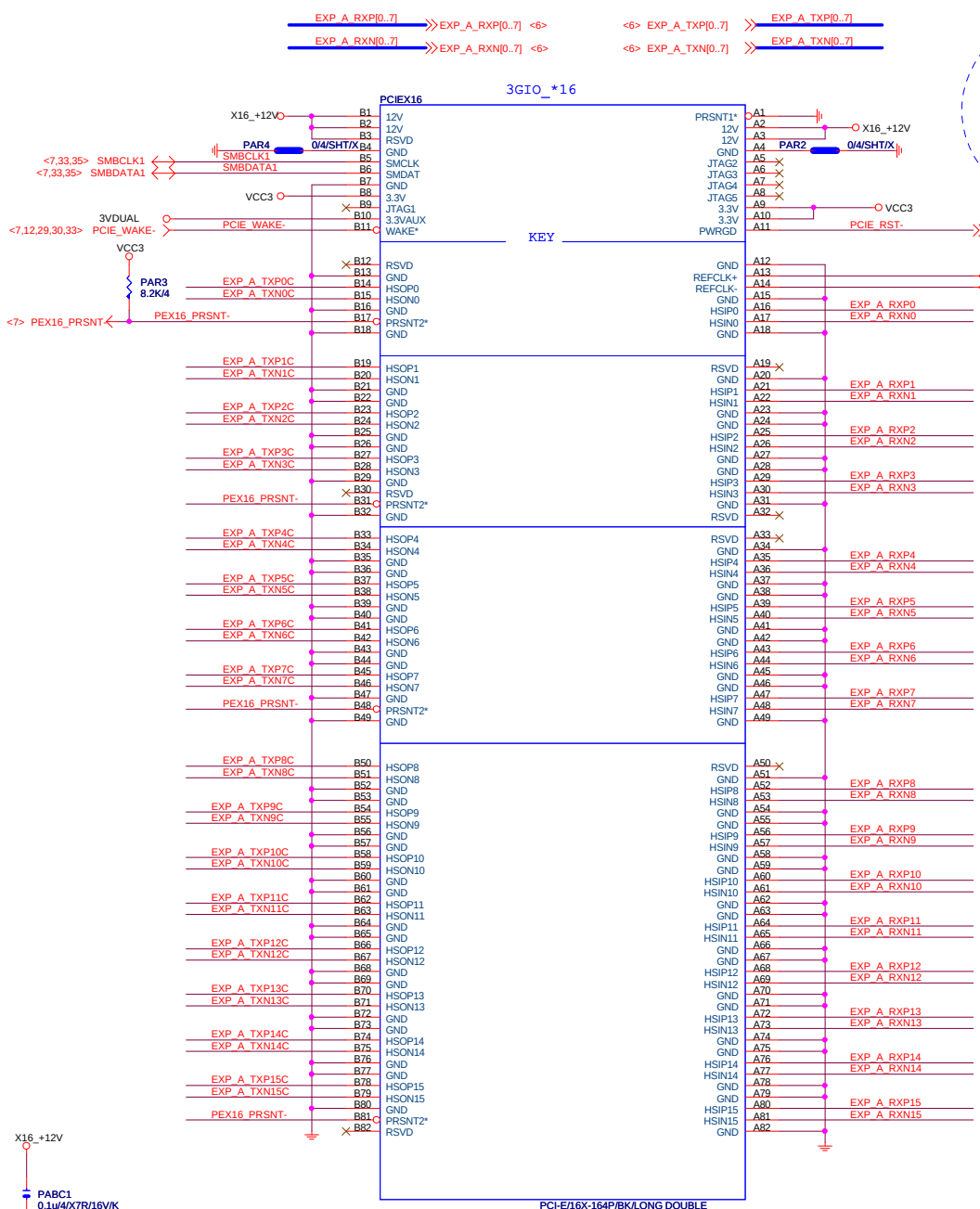






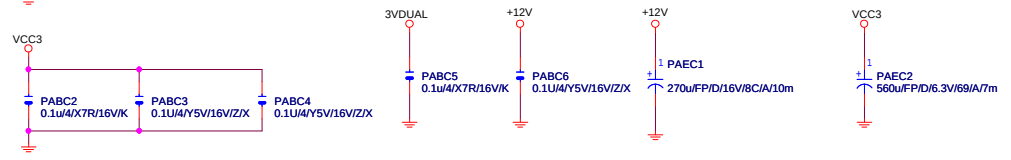




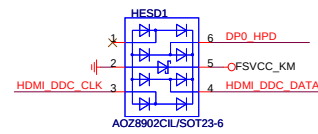
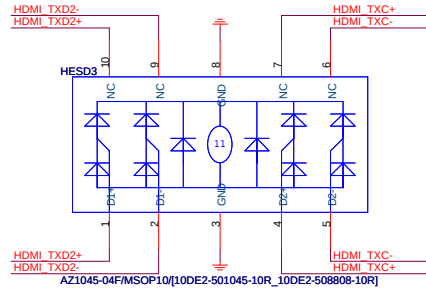
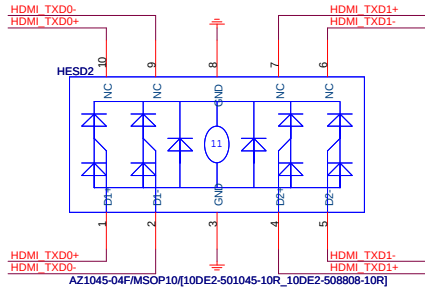
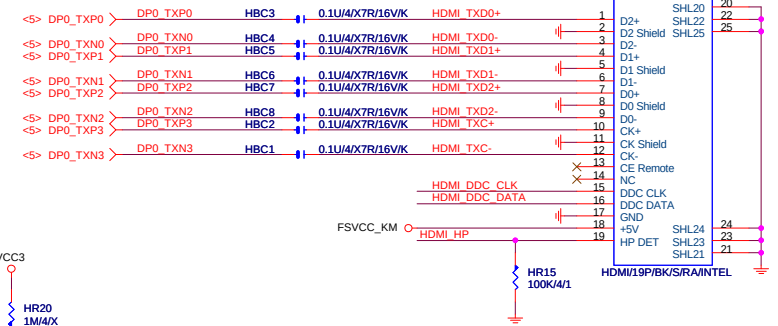
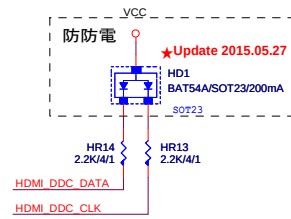
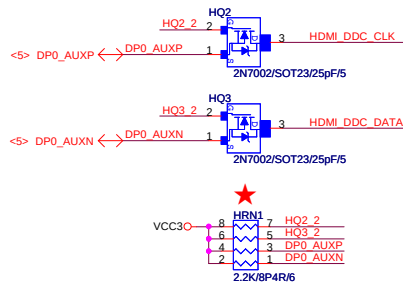
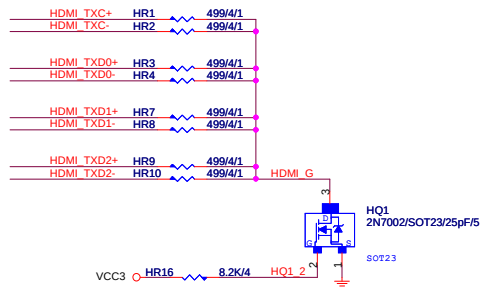


EXP A TXP0	PAC4	0.22U/2X5R6.3V/K	EXP A TXP0C
EXP A TXN0	PAC5	0.22U/2X5R6.3V/K	EXP A TXN0C
EXP A TXP1	PAC6	0.22U/2X5R6.3V/K	EXP A TXP1C
EXP A TXN1	PAC7	0.22U/2X5R6.3V/K	EXP A TXN1C
EXP A TXP2	PAC8	0.22U/2X5R6.3V/K	EXP A TXP2C
EXP A TXN2	PAC9	0.22U/2X5R6.3V/K	EXP A TXN2C
EXP A TXP3	PAC10	0.22U/2X5R6.3V/K	EXP A TXP3C
EXP A TXN3	PAC11	0.22U/2X5R6.3V/K	EXP A TXN3C
EXP A TXP4	PAC12	0.22U/2X5R6.3V/K	EXP A TXP4C
EXP A TXN4	PAC13	0.22U/2X5R6.3V/K	EXP A TXN4C
EXP A TXP5	PAC14	0.22U/2X5R6.3V/K	EXP A TXP5C
EXP A TXN5	PAC15	0.22U/2X5R6.3V/K	EXP A TXN5C
EXP A TXP6	PAC16	0.22U/2X5R6.3V/K	EXP A TXP6C
EXP A TXN6	PAC17	0.22U/2X5R6.3V/K	EXP A TXN6C
EXP A TXP7	PAC18	0.22U/2X5R6.3V/K	EXP A TXP7C
EXP A TXN7	PAC19	0.22U/2X5R6.3V/K	EXP A TXN7C

EXP A RXP[0..15]	>>>EXP_A_RXP[0..15]	<-6>
EXP A RXN[0..15]	>>>EXP_A_RXN[0..15]	<-6>
EXP A TXP[0..15]	>>>EXP_A_TXP[0..15]	<-6>
EXP A TXN[0..15]	>>>EXP_A_TXN[0..15]	<-6>



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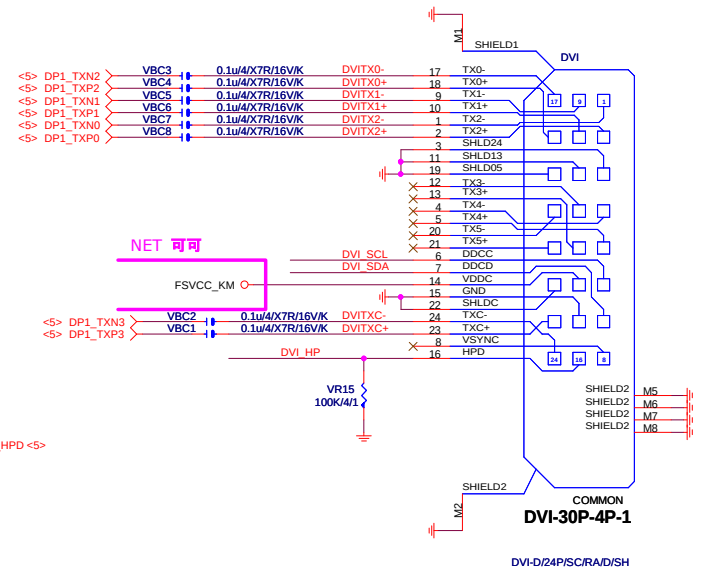
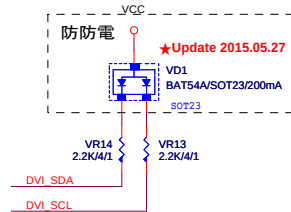
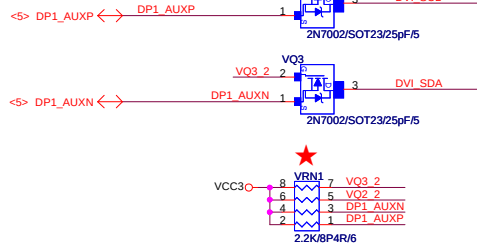
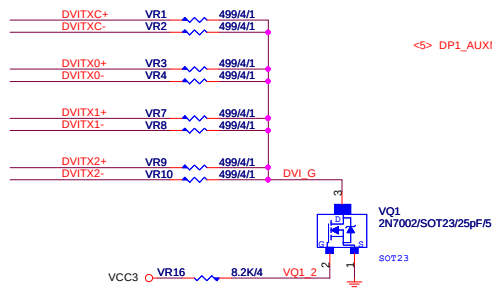


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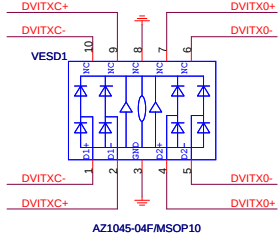
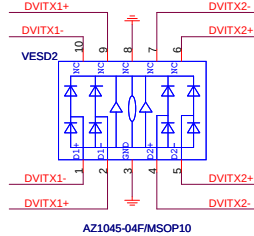
Rev: 0.73

DVI CONN

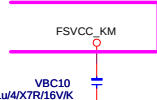
DVI: 20/4/6/4/20  
Impedance=85 +- 17.5%



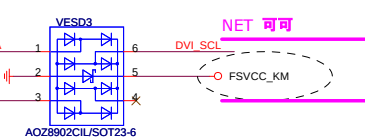
Close to connector



NET 可可



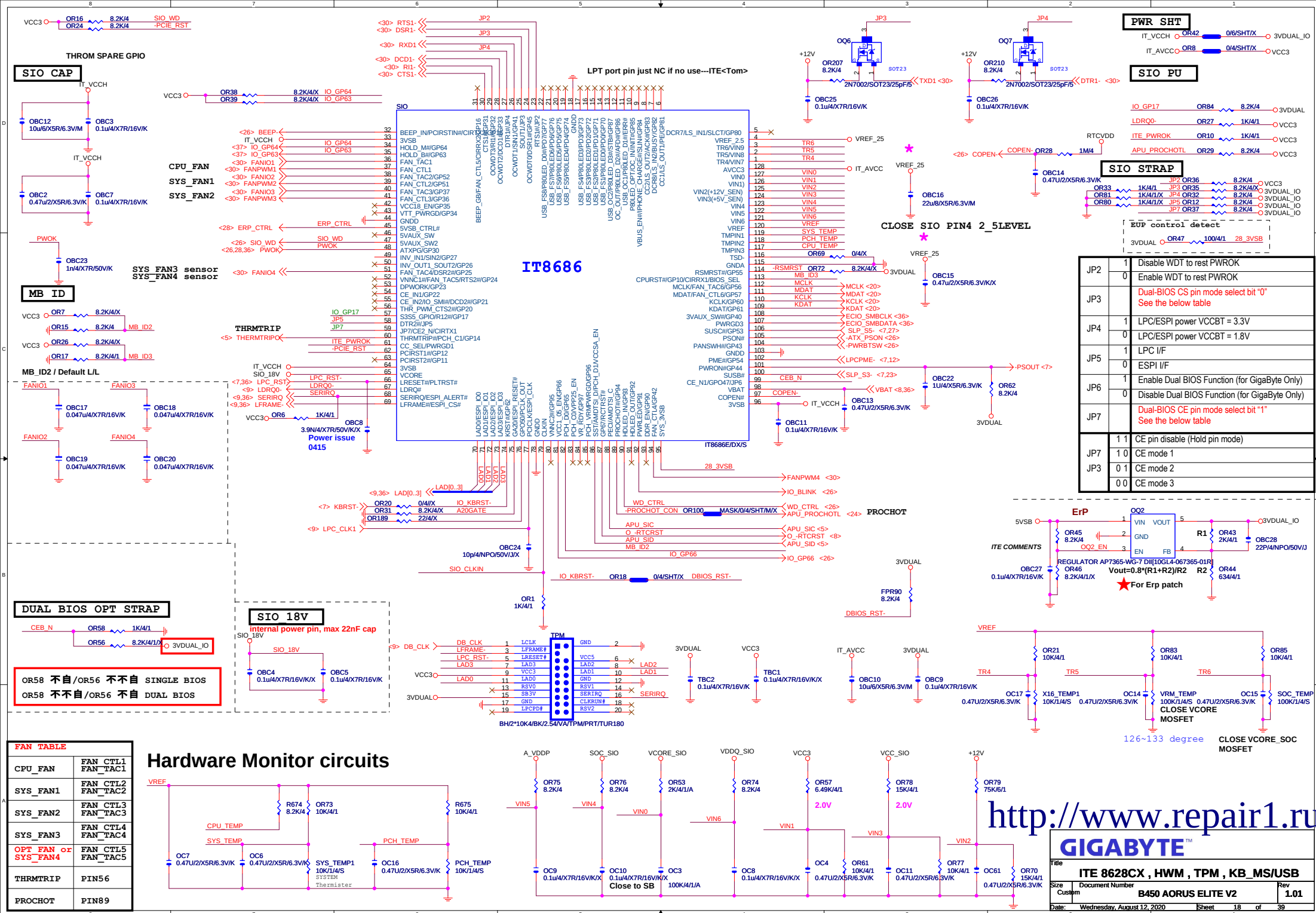
Close to connector



平平平 DVI-D



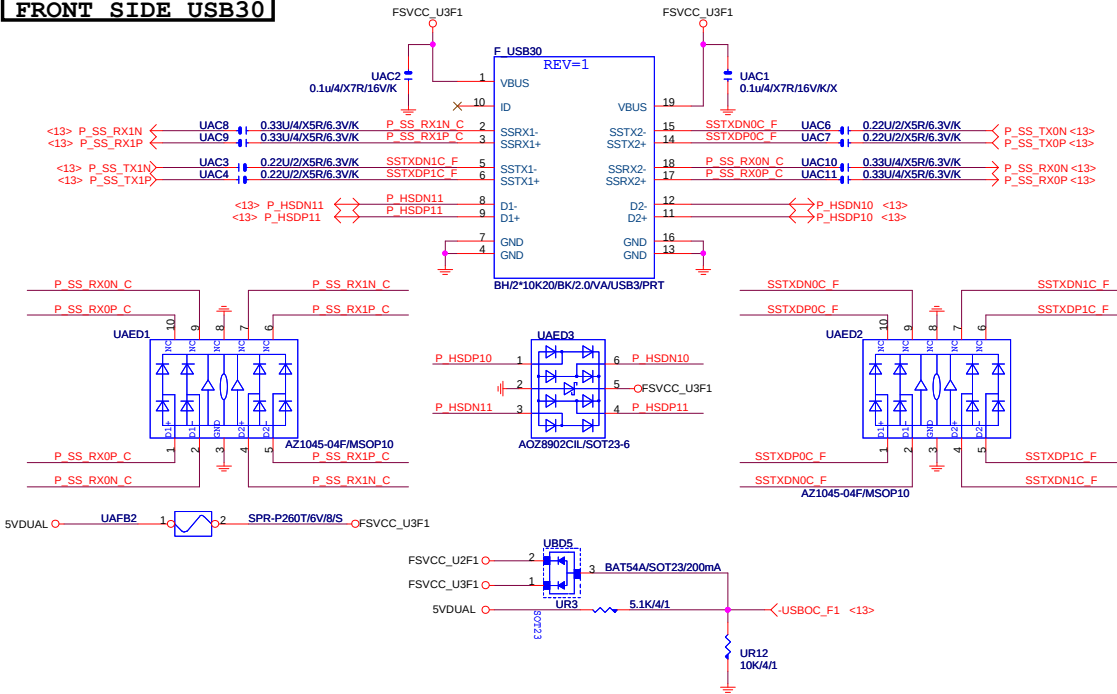
GIGABYTE™		
HDMI 2.0		
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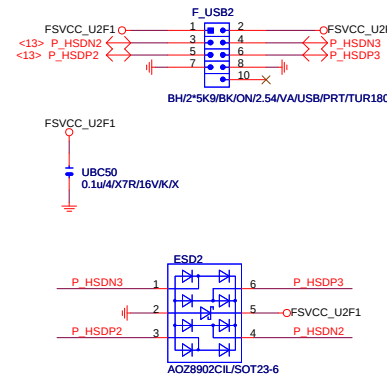
<http://www.repair1.ru/>

Title			
ITE 8628CX , HWM , TPM , KB_MS/USB			
Size	Document Number	Rev	
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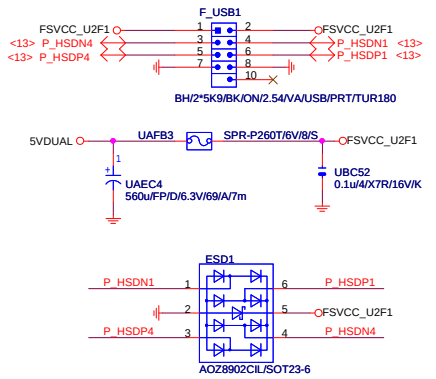
## FRONT SIDE USB30



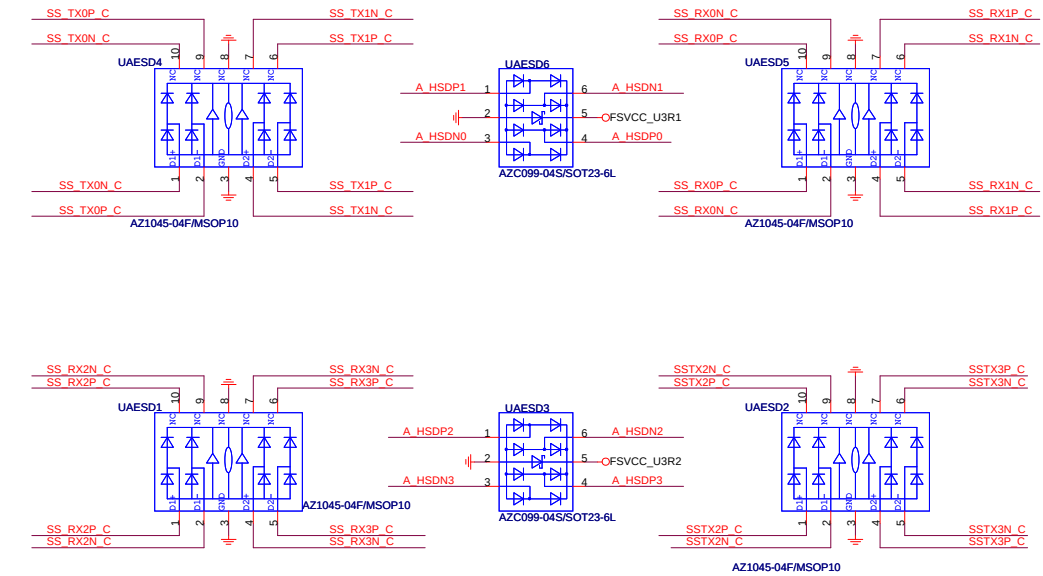
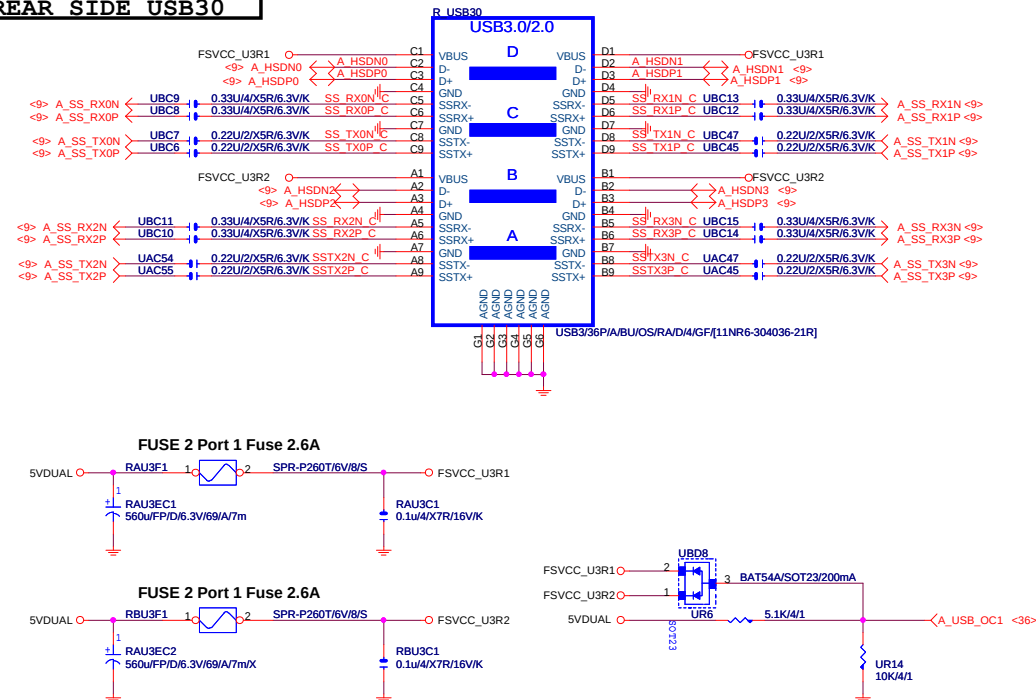
## FRONT SIDE USB2



## FRONT SIDE USB1



## REAR SIDE USB30

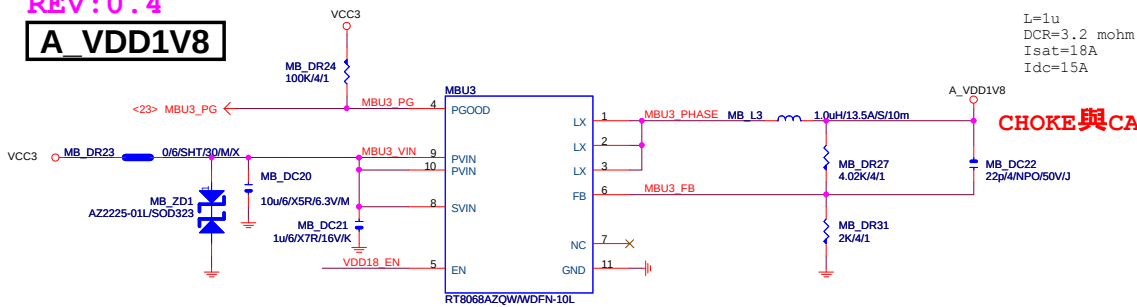


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GIGABYTE™			
Title			
F_USB, R_USB CONN			
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REV: 0.4

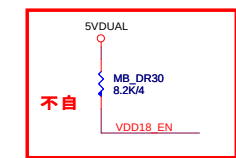
## A\_VDD1V8



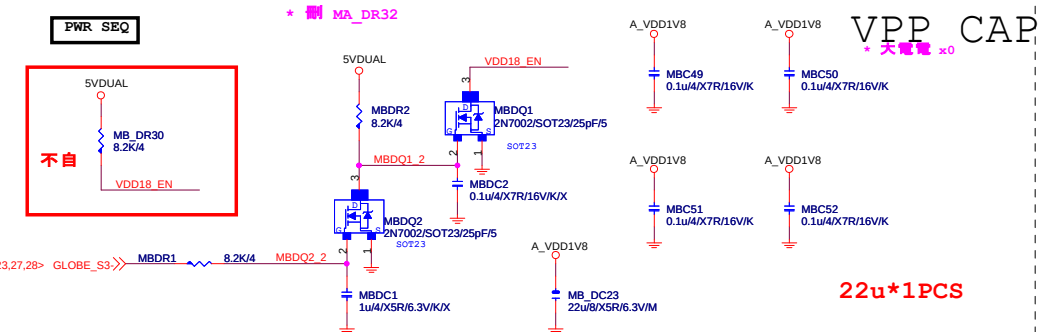
L=1u  
DCR=3.2 mohm  
Isat=18A  
Idc=15A

CHOKE與CAP用自可也

## PWR\_SEQ

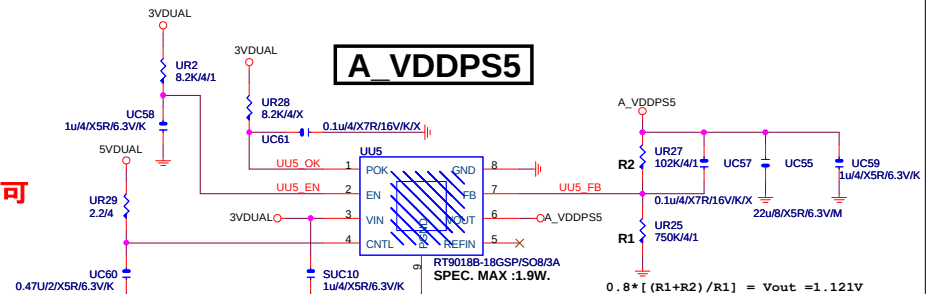


\* 刪 MA\_DR32



22u\*1PCS

## A\_VDDPS5



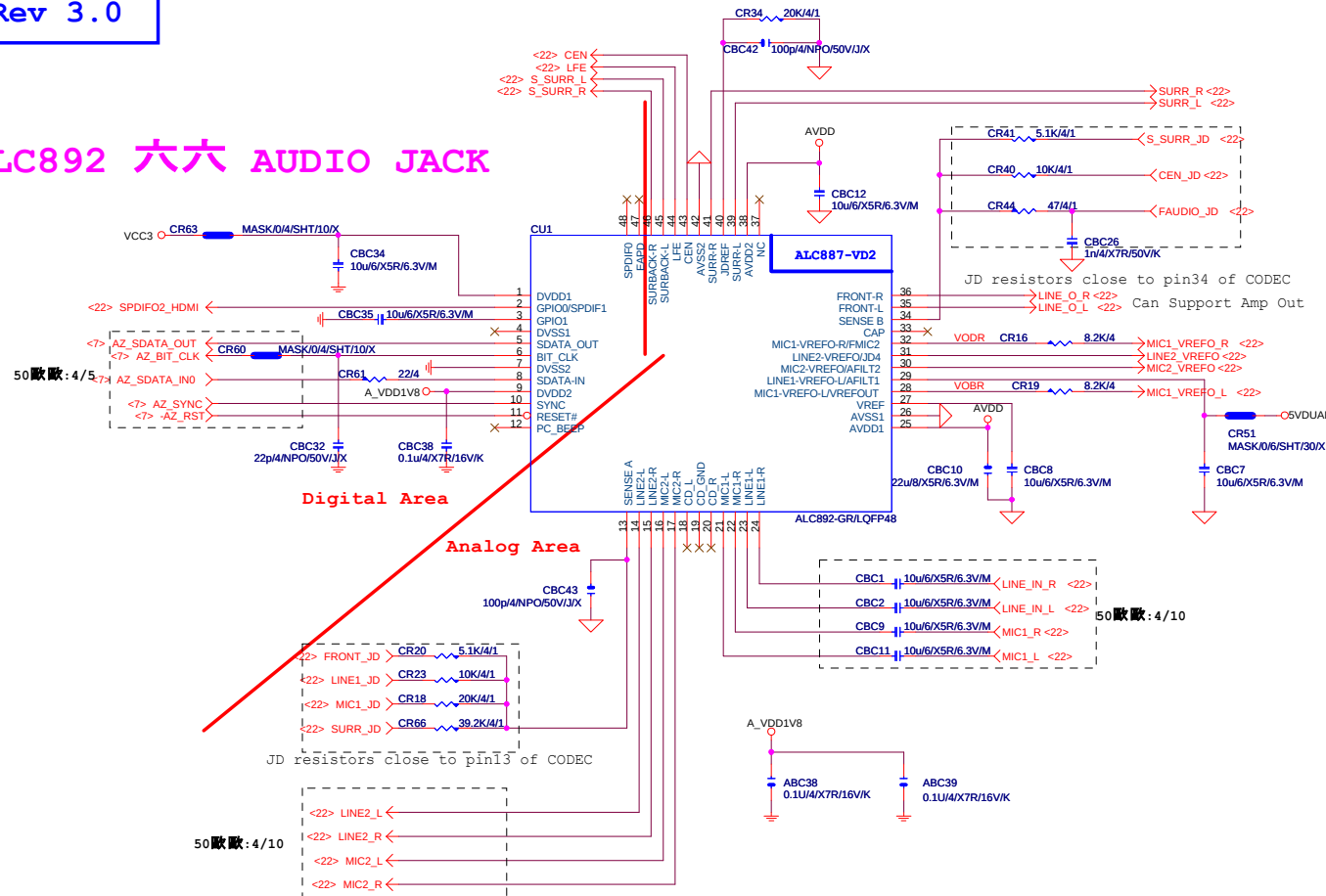
【技技技技 R&D技技技技156】  
RT9018 (RICHTEK) 與 NCT3730 (NUVOTON),  
EM5103GE (EMC) 做做用, 針針PIN7 (FB) 分分分分分分  
(R1/R2) 須做修修應100K以不電分

$$0.8 * [(R1+R2)/R1] = V_{out} = 1.121V$$

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

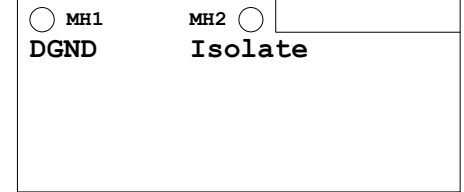
<http://www.repair1.ru/>

## ALC892 六六 AUDIO JACK



LAYOUT注注: 螺螺六螺GND方平

1. MH1空空空, 螺DGND  
空空空, 才修應Isolate
2. MH2統一修應Isolate
3. Codec螺方, 第第第第第第第第第第GND

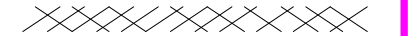


LAYOUT注注: 要加

GND切切切



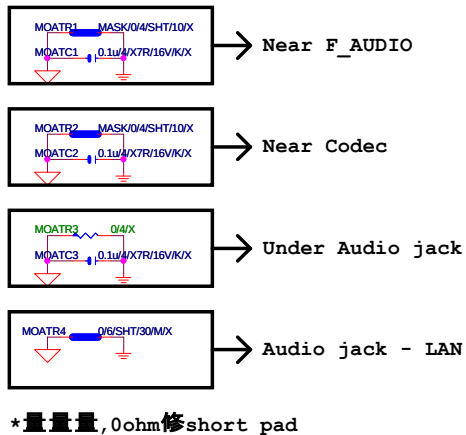
音音音音音音


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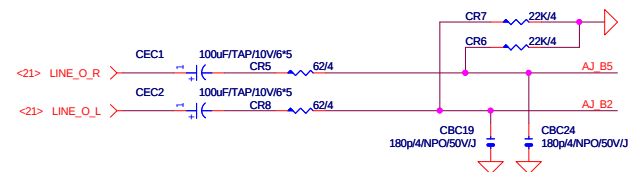
- BOM OPTION :
1. Chemicon 音音電電
  2. 金金金金 Reserve (LAYOUT 不自與上, 依依依Model spec)
  3. LED Reserve (不自與上上LED顏顏, 依依依Model spec)

GIGABYTE™			
Title	ALC1150 CODEC		
Size	Document Number	Rev	
Custom	B450 AORUS ELITE V2	1.01	
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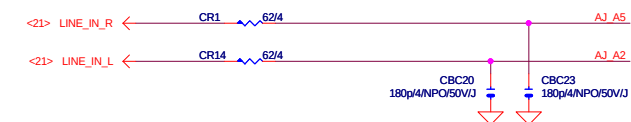
Rev 3.0



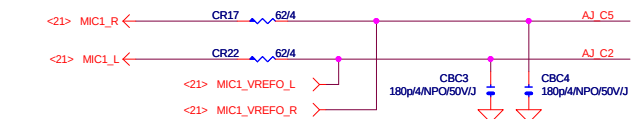
## LINE-OUT



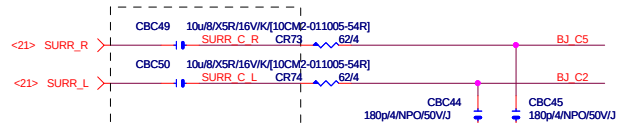
## LINE-IN



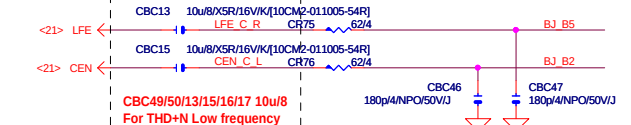
## MIC-IN



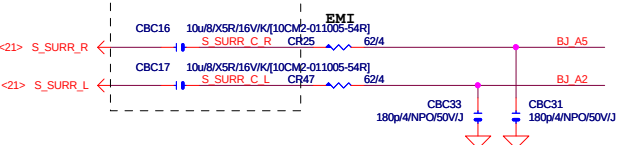
## SURROUND



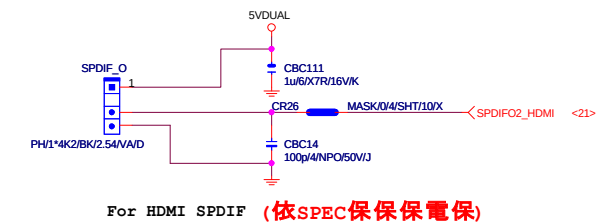
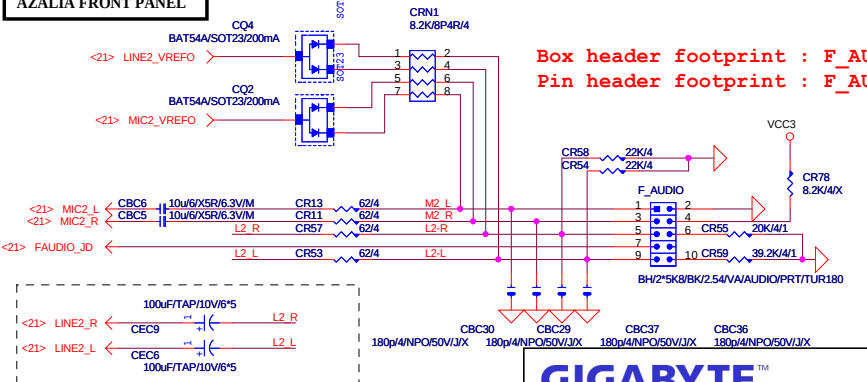
## CEN/LFE



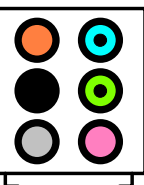
## SURR BACK



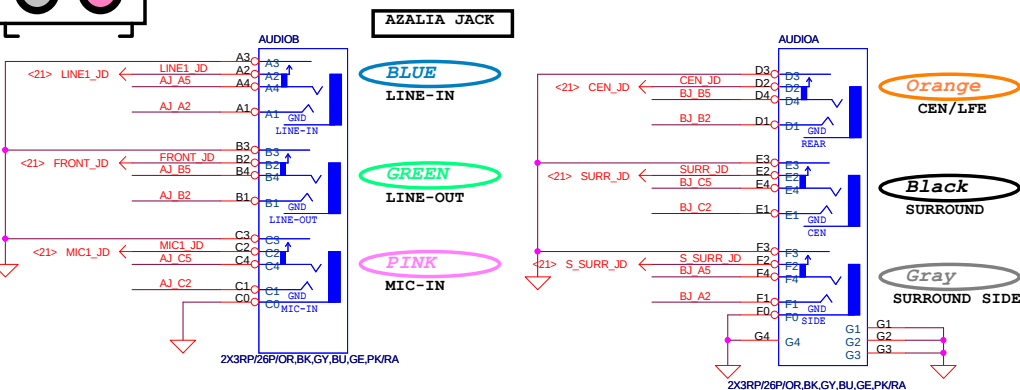
## AZALIA FRONT PANEL



## AZALIA JACK

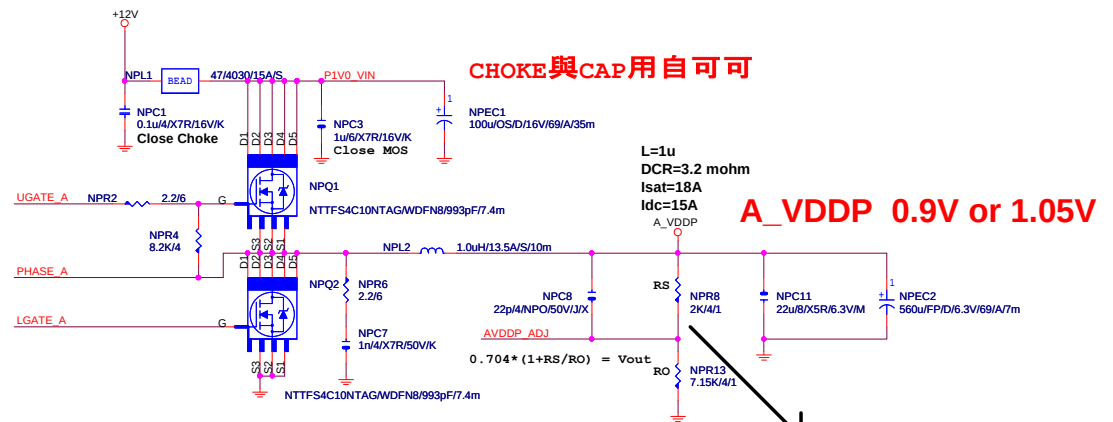
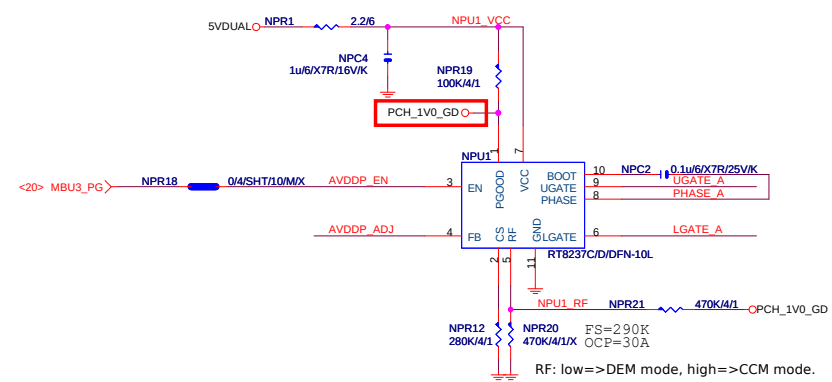


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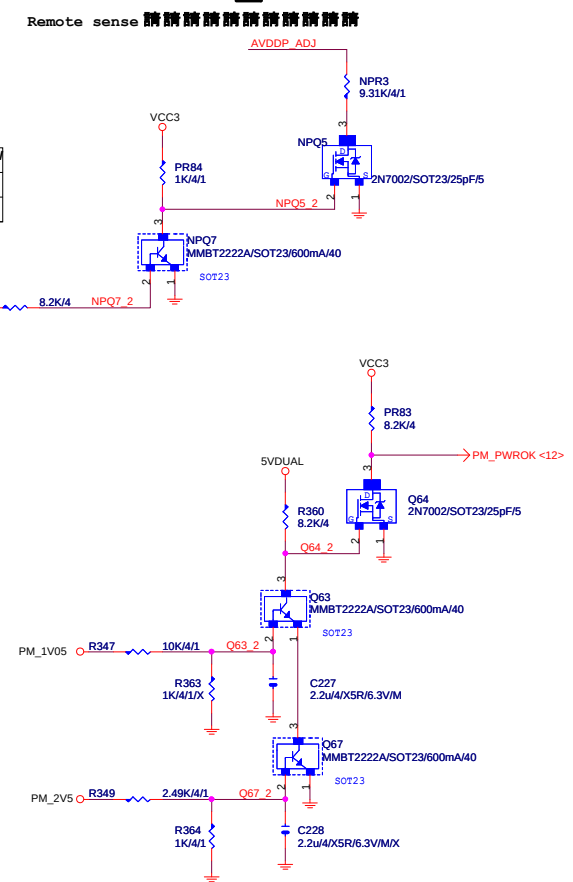
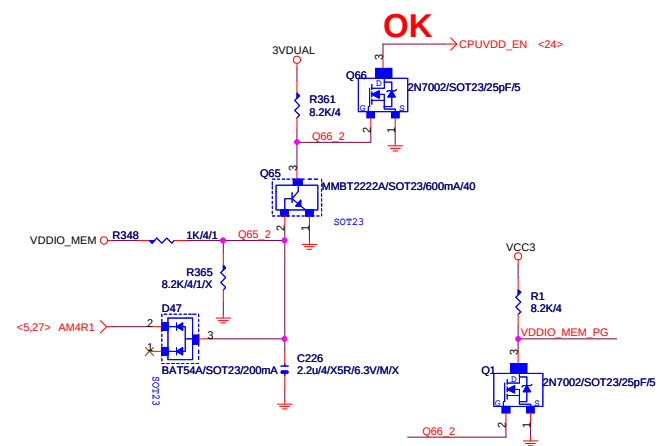
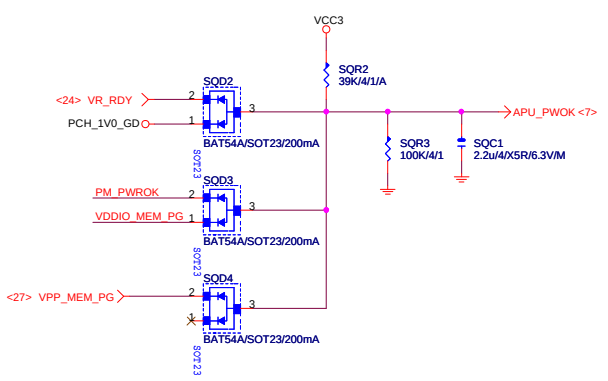
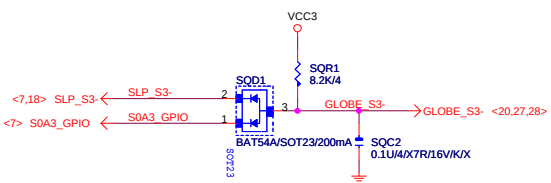
Title	AUDIO JACK	
Size	Custom	Document Number
		B450 AORUS ELITE V2
Rev	1.01	
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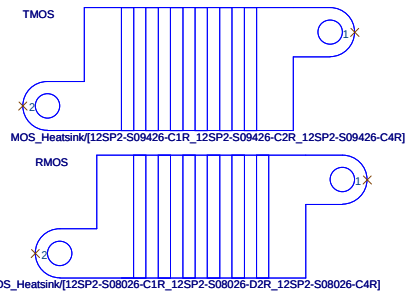
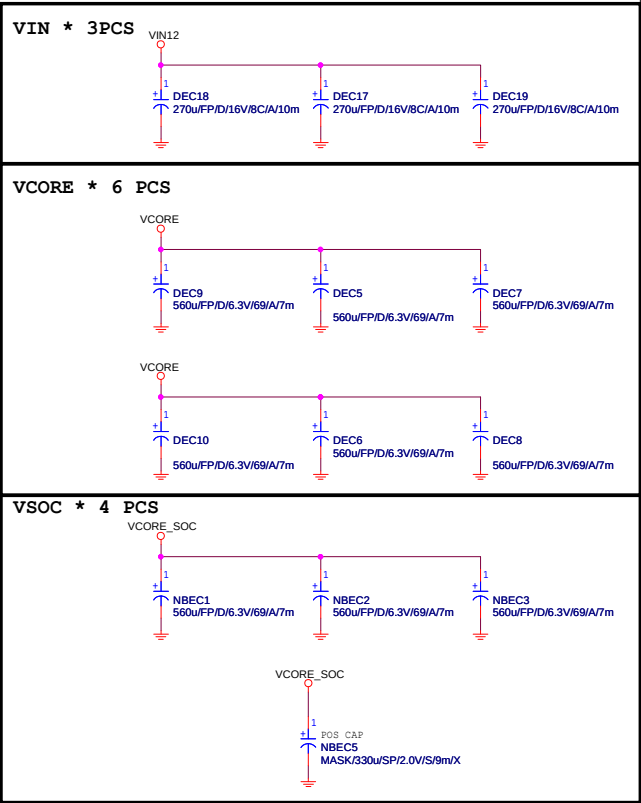
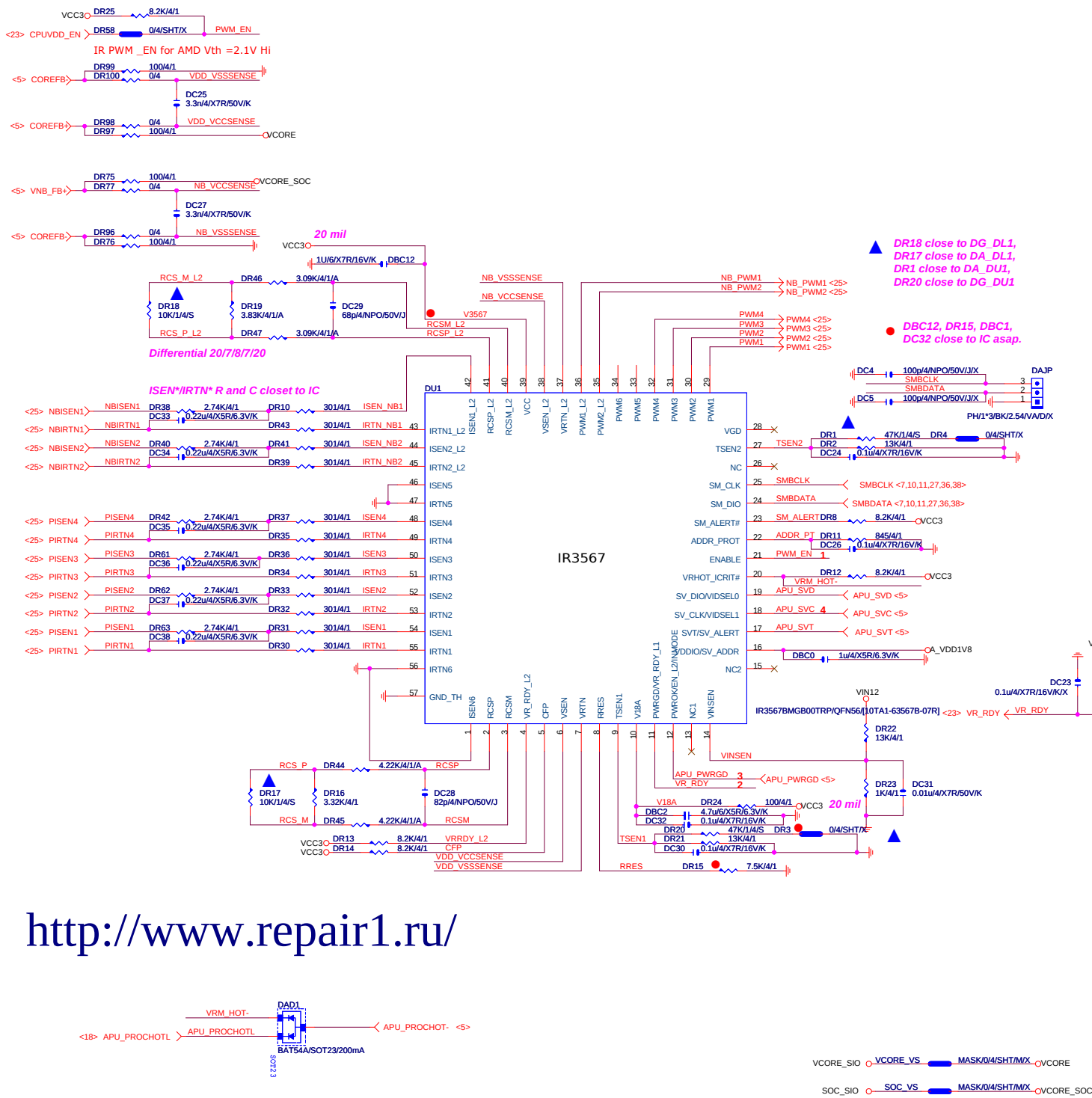


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請請位CHOKE統一請一方

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V





GIGABYTE			
Title			
VCORE (PWM ISL6277+6609A)			
Size	Document Number	Rev	
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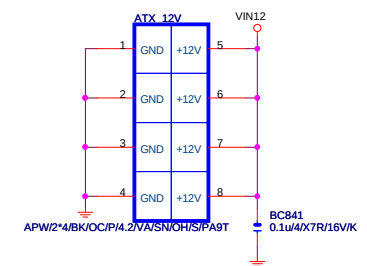
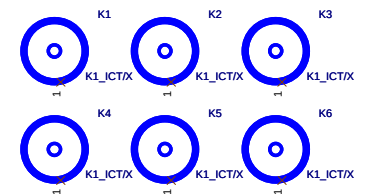
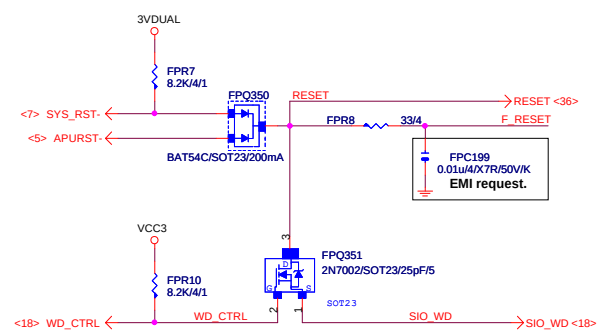
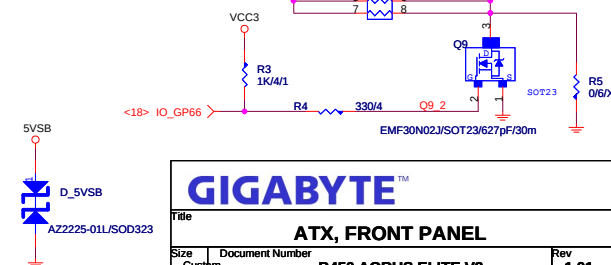
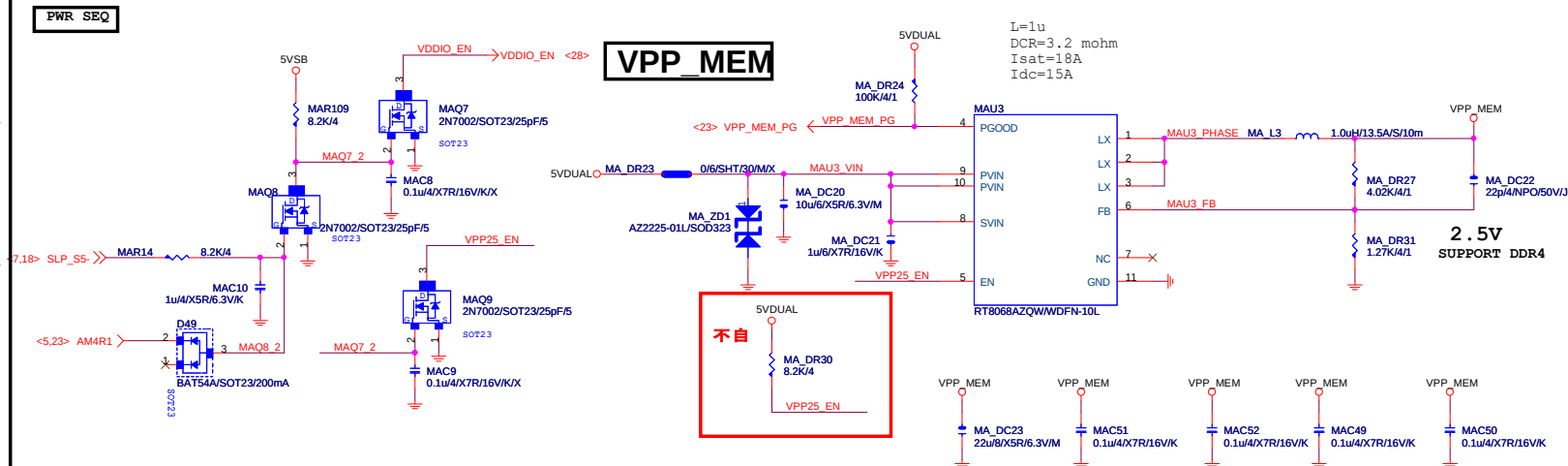
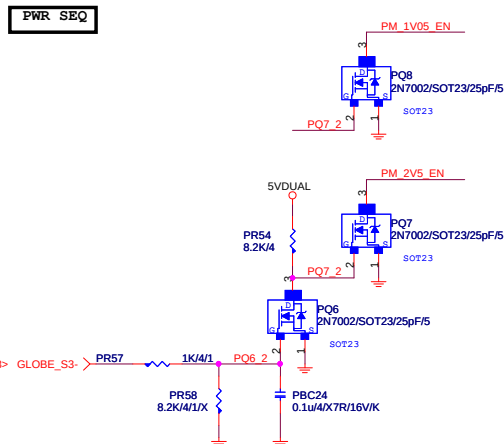
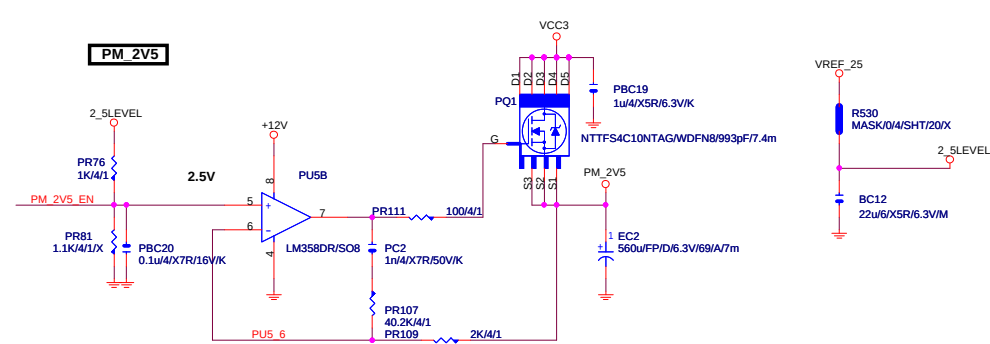
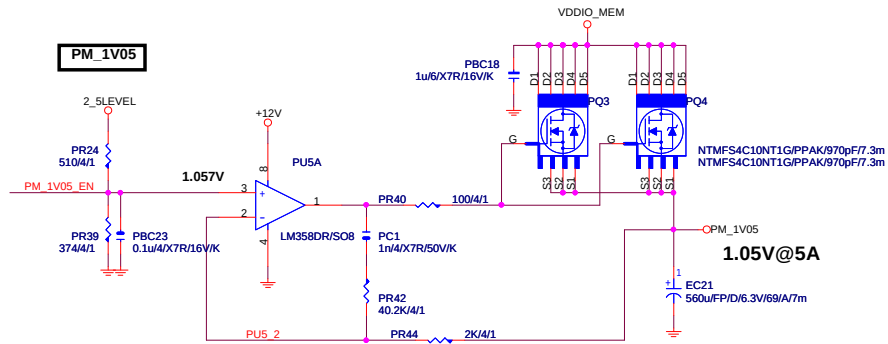


Diagram of a 5x8 LED matrix. The matrix is labeled with row numbers RN1 through RN5 and column numbers 1 through 8. A +12V supply is connected to the top-left corner (RN1, 1). The bottom row (RN5) is connected to ground.

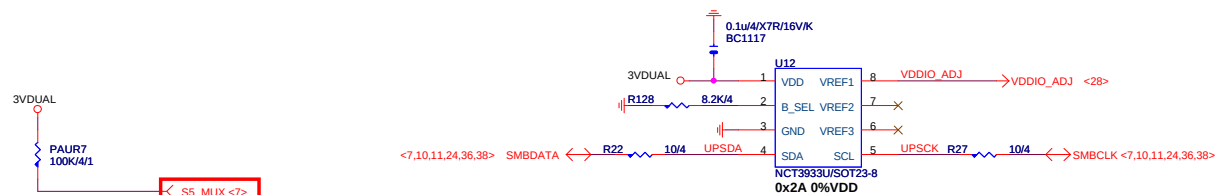
[illegible]



## VDDCR SOC S5

S5\_MUX: S0-->High, S5-->Low  
H: VDDCR\_SOC\_S5 will track VCORE\_SOC.  
L: If VCORE\_SOC < 0.775V (OR 0.85V), VDDCR\_SOC\_S5=0.775V.  
If VCORE\_SOC > 0.775V (OR 0.85V), VDDCR\_SOC\_S5 will trace VCORE\_SOC.

AM4 S5: 0.775V, 200mA,  
S0:VAR, 900mA.

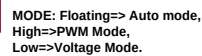


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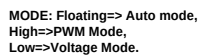
GIGABYTE™			
Title			
PM POWER			
Size	Document Number	Rev	
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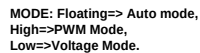




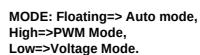
## SYSTEM FAN1



## SYSTEM FAN2



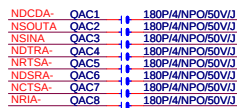
## SYSTEM FAN3



## COM PORT



## COMA



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## GIGABYTE

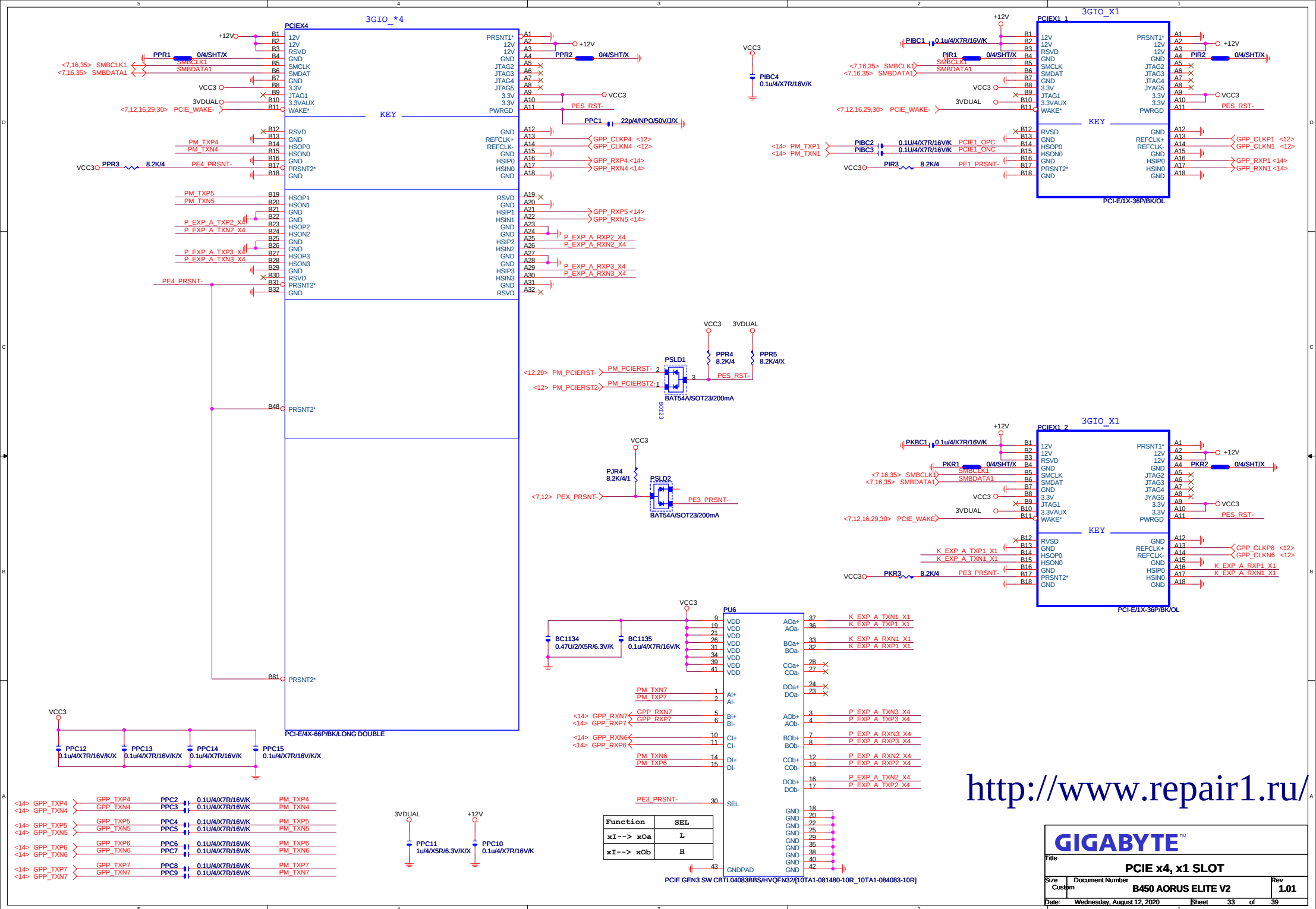
Title	PCIE X8, SWITCH
-------	-----------------

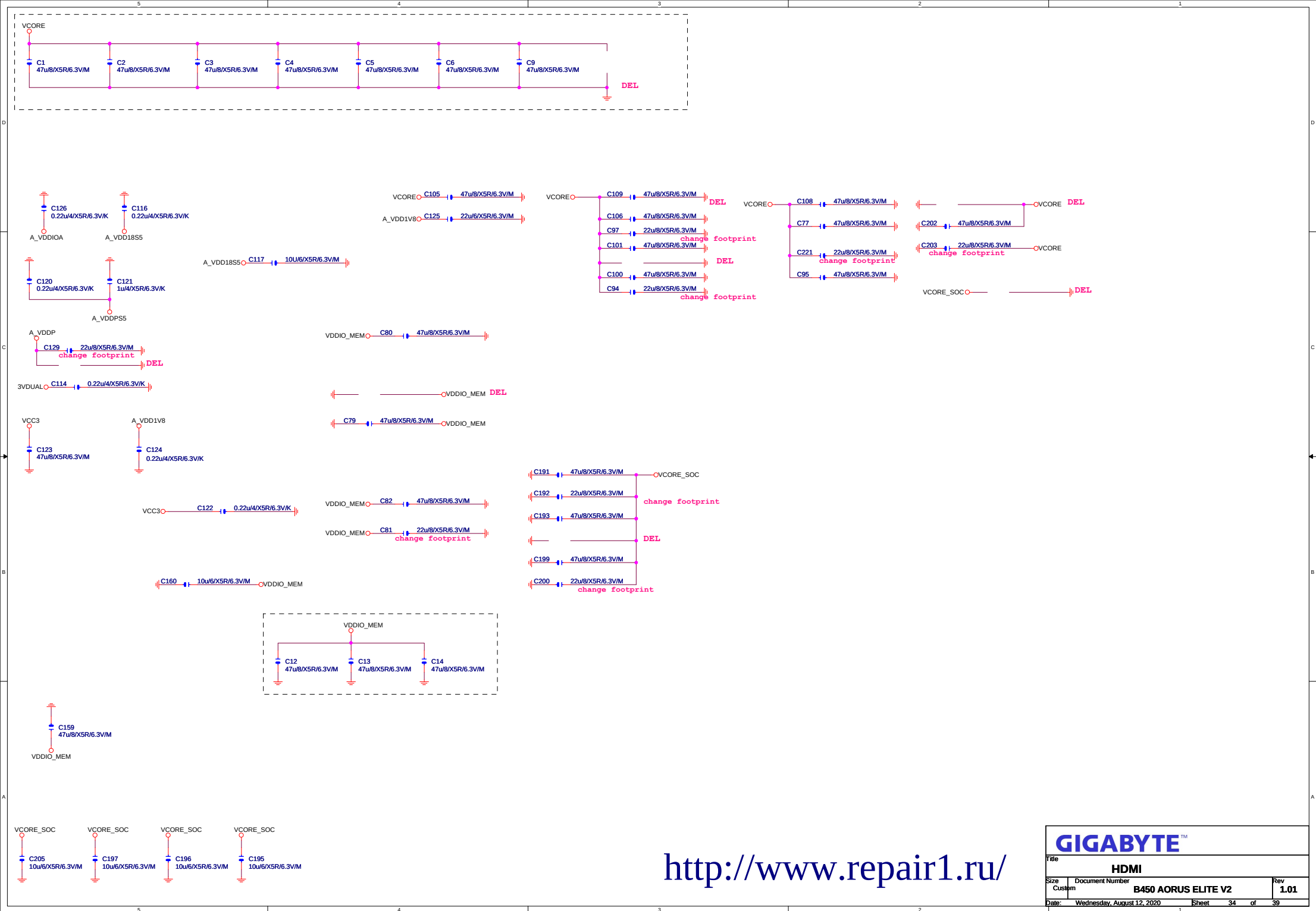
Size	Document Number	Rev
Custom	<b>B450 AORUS ELITE V2</b>	<b>1.01</b>

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<b>GIGABYTE</b> <sup>TM</sup>		
Title <b>DP to VGA</b>		
Size Custom	Document Number <b>B450 AORUS ELITE V2</b>	Rev <b>1.01</b>
Date: <b>Wednesday, August 12, 2020</b>	Sheet <b>31</b>	of <b>39</b>

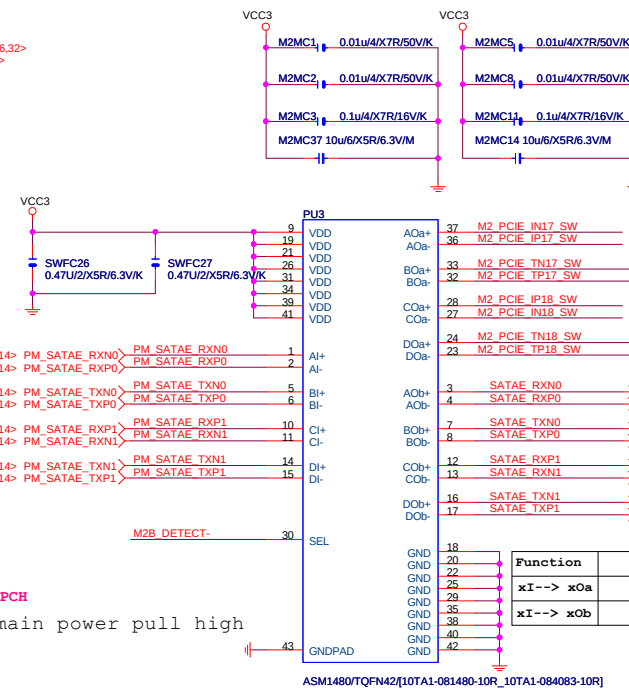
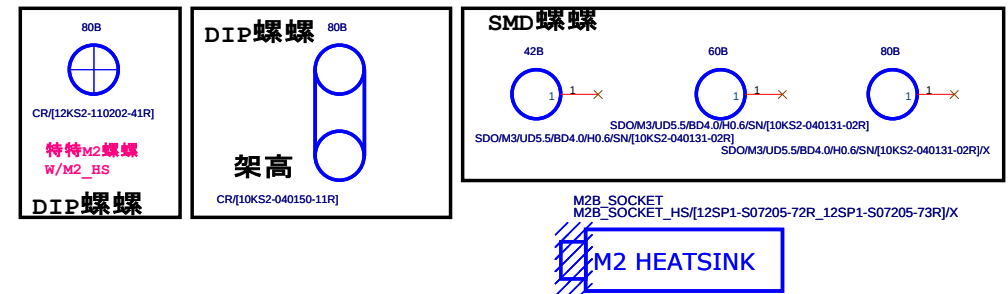
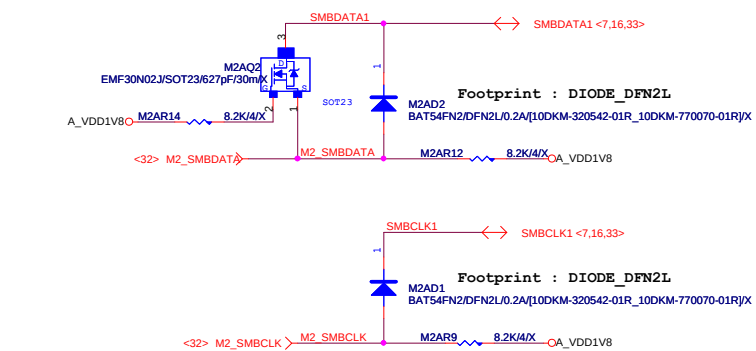
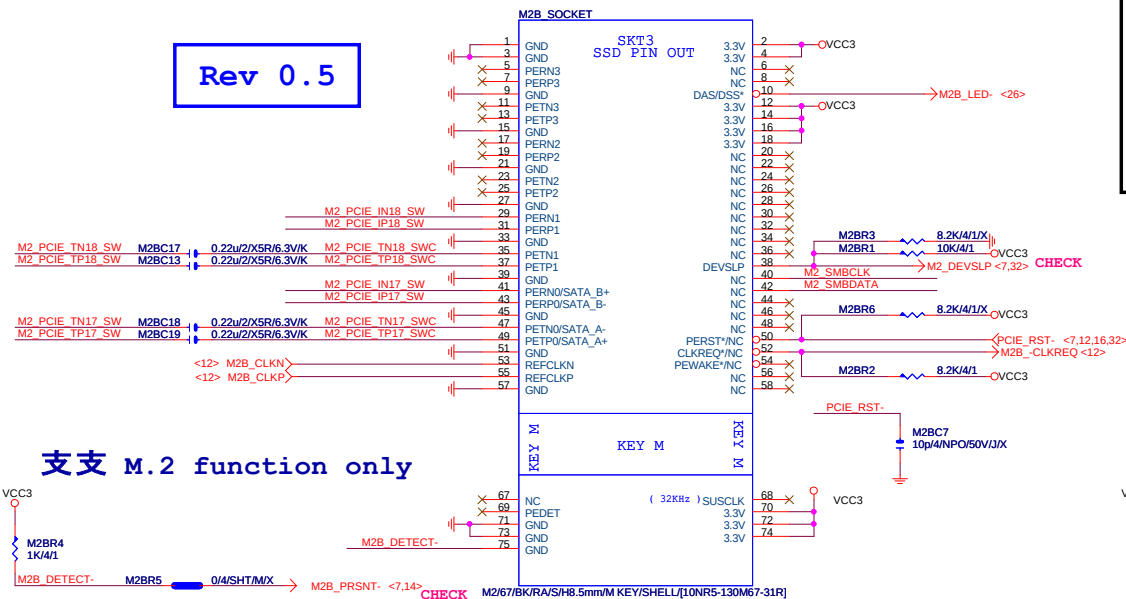
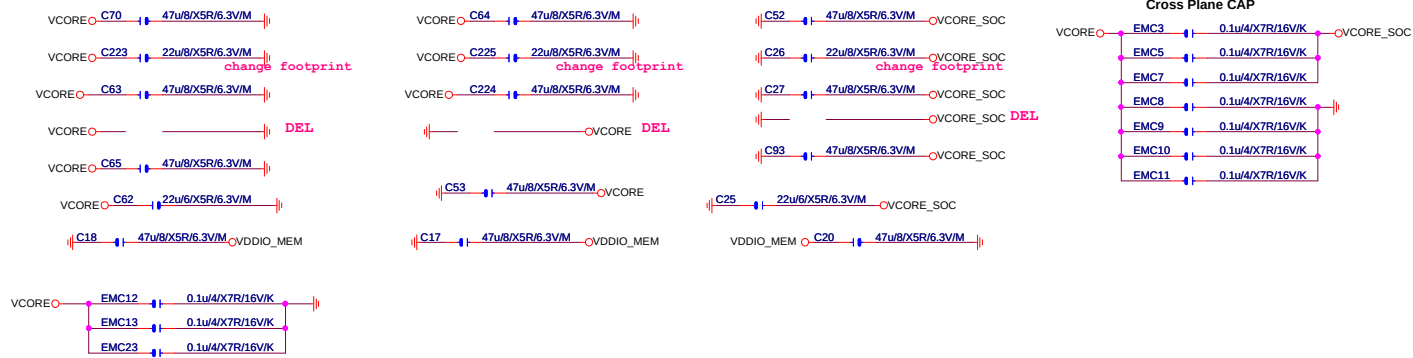






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## CPU TOP CAVITY



From PM SATAE

CONNECT TO PCH  
BIOS設應main power pull high

To M.2B PCIE Mode

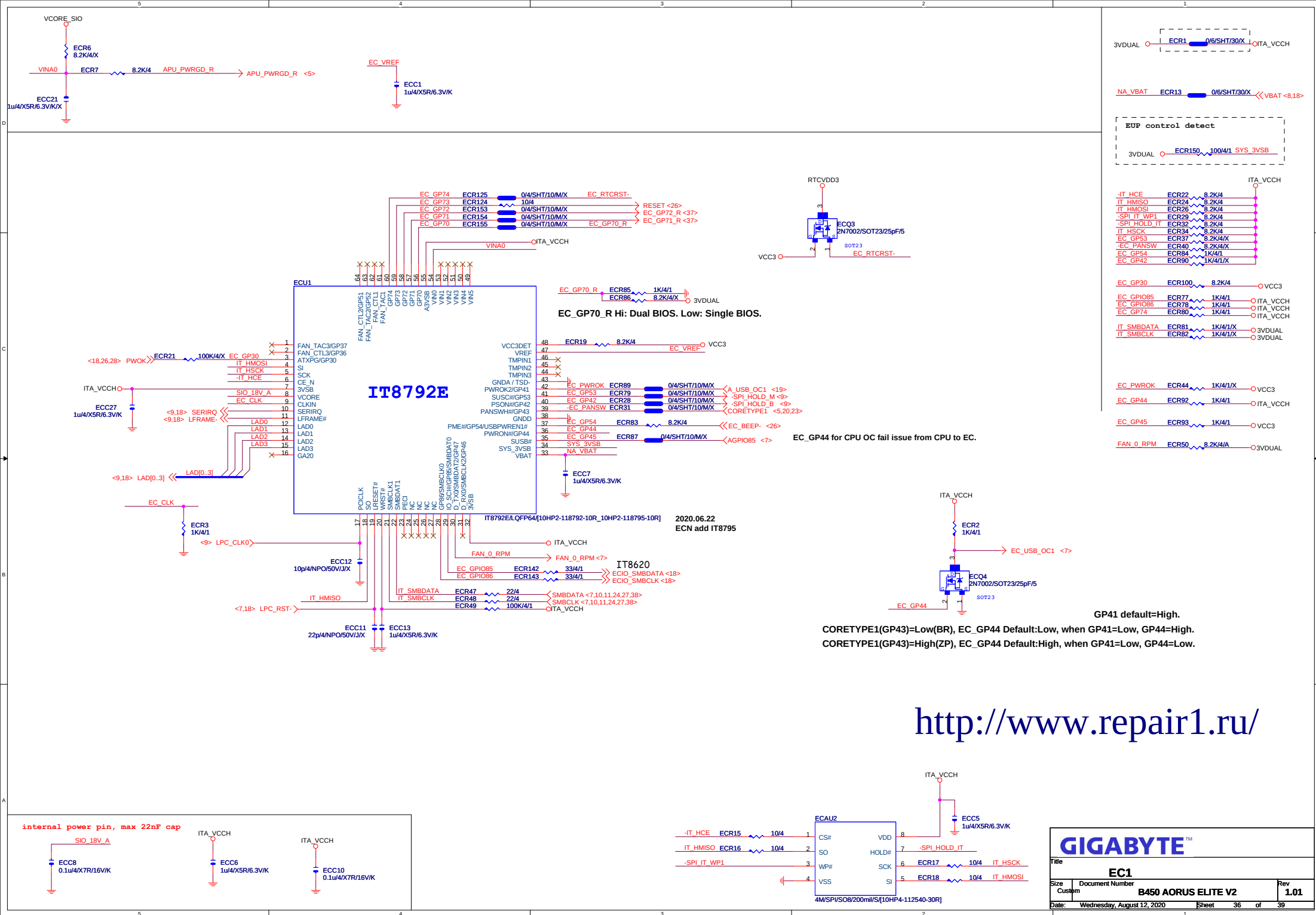
To SATA CONN

Function	SEL
xI--> x0a	L
xI--> x0b	H

**GIGABYTE™**

Title			
<b>HDMI</b>			
Size	Document Number	Rev	
Custom	<b>B450 AORUS ELITE V2</b>	<b>1.01</b>	
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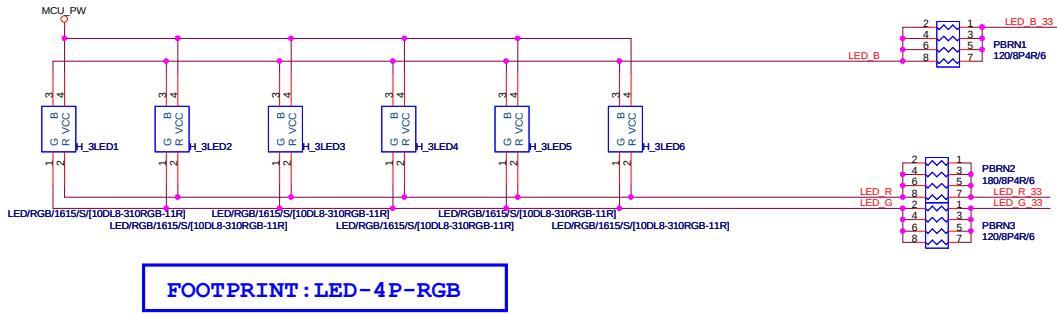
<http://www.repair1.ru/>





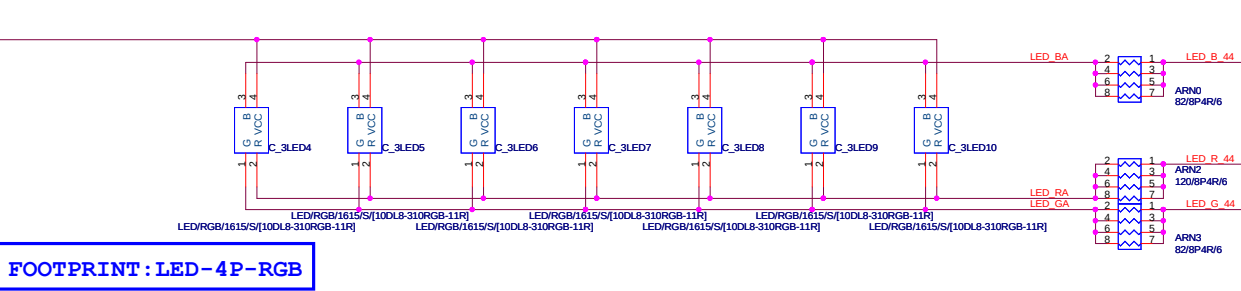
第第音 LED

FOR PCH 正正正 LED\*6 (位位在正左, 依依PCH\_HS設設位請)

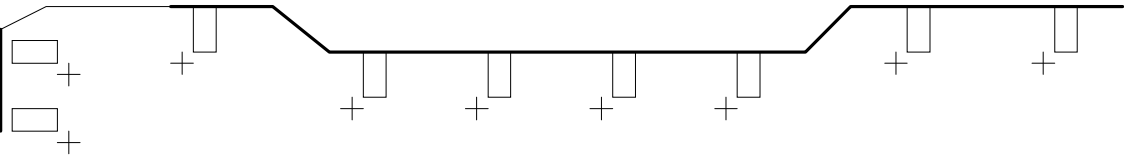


第第音 LED

FOR AUDIO 正正正 LED\*10 C\_3LED1~10)



Audio Ground切切切+背用 RGB LED

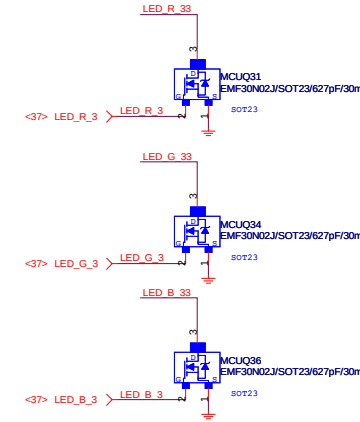


RGB LED LAYOUT 注注注注 :

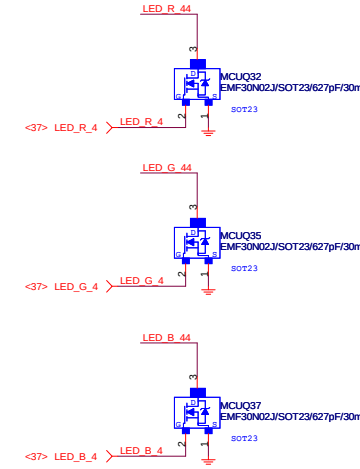
1. Debug LED (依LED依CPU/DRAM/VGA/BOOT個個位位位請)
2. 背左 RGB LED 方方方左請統統如螺 (方左正整可統統整螺保整不)
3. 正左 RGB LED 統統方方統可
4. MCU\_PW & MCU\_PW33電兩統一兩20mils
5. ECF1, ECF2, ECF3, ECF5 兩請電兩兩80mils保用或或方平加或
6. MCU LED 一pin請兩切4mils, 如: LED\_R\_1, LED\_G\_1, LED\_B\_1 .....
7. LED RGBW rule : W/S=10/5 mils 如: LED\_R\_11, LED\_G\_11, LED\_B\_11, LED\_W..... (包包請包包電包分電LED請net)
8. Digital LED NET rule W/S=4/8 mils GPD0\_SDA\_B, GPD0\_SDA\_BB, GPD0\_SDA\_C, GPD0\_SDA\_CC

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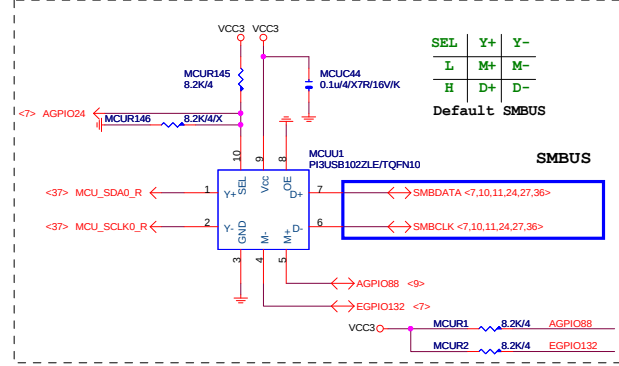
第第音 LED CONTROL



第第音 LED CONTROL



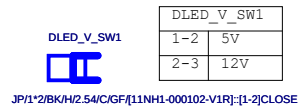
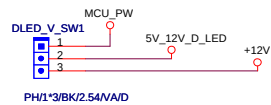
For AMD MCU update



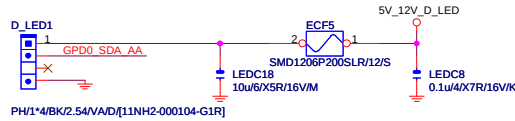
GIGABYTE™

Title			PCH/AUDIO LED
Size	Document Number	Rev	
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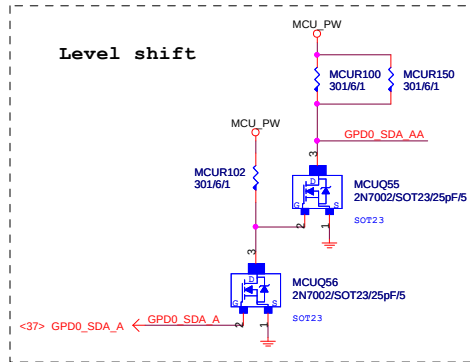
第六音 LED (請請左不左左位位)



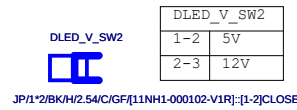
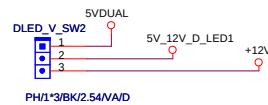
Digital LED Strip1



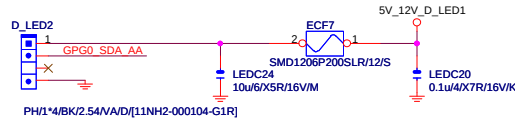
Footprint "PH1X4-CUT3-LED-L"



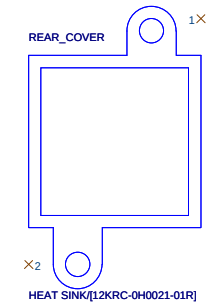
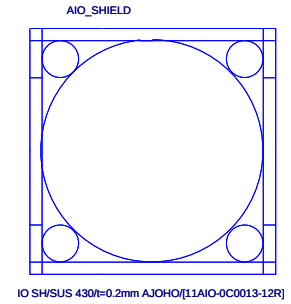
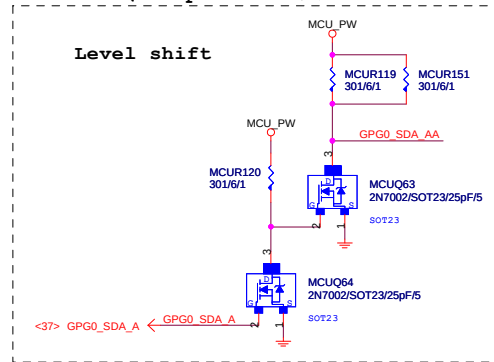
第第音 LED (請請靠螺DDR左左位位)



Digital LED Strip2



Footprint "PH1X4-CUT3-LED-I"  
(for pin-name 與 model-name 同方方)



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