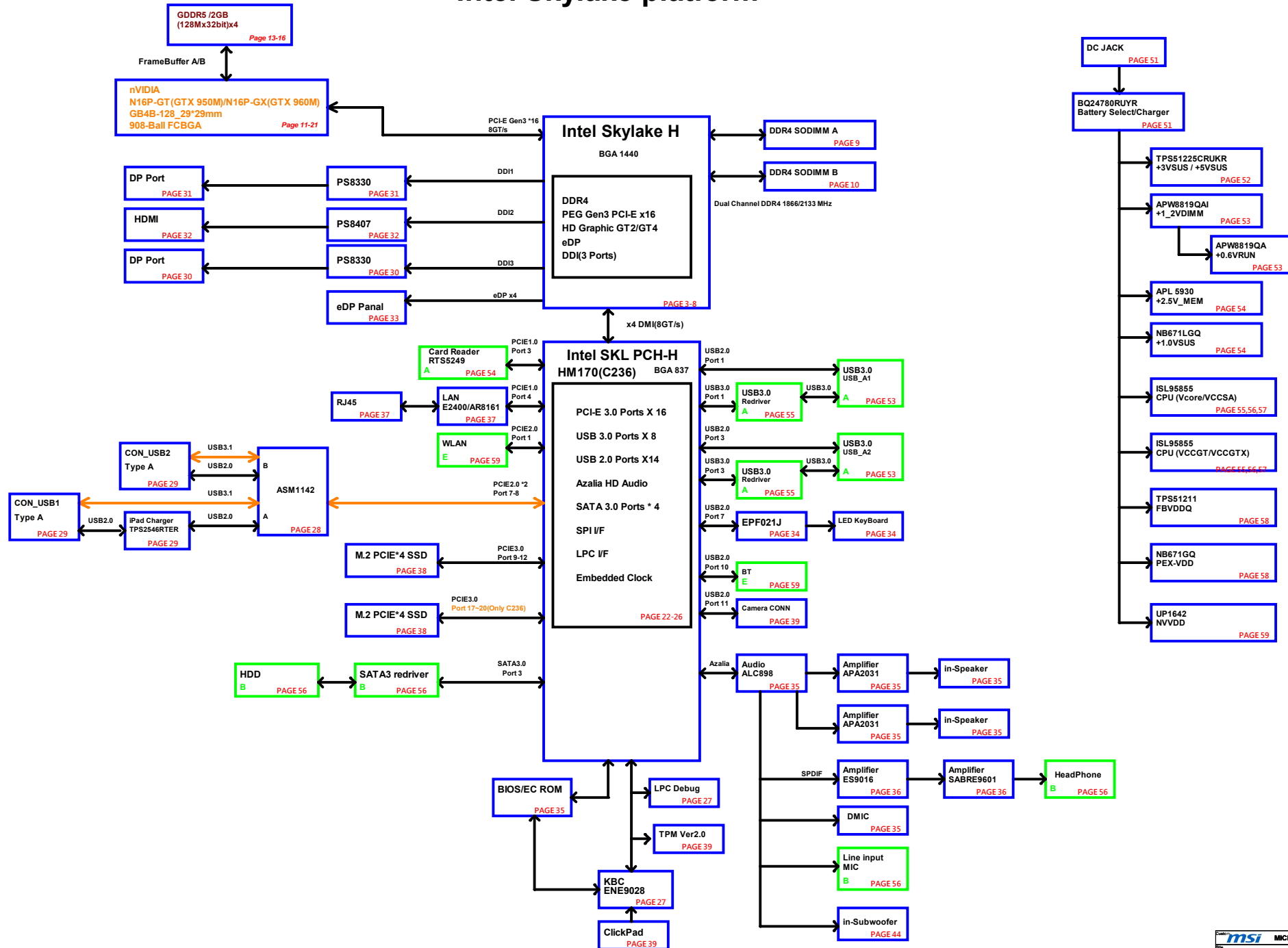


MS-1776 Ver.10

Intel Skylake platform



SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

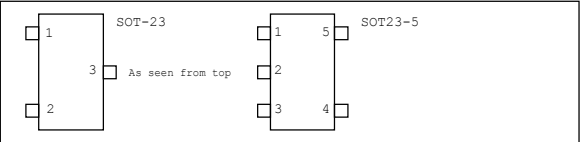
Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	PM_SLP_S4#
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	PM_SLP_S3#
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	PM_SLP_S3#
+1_5VRUN	1.5V switched power rail (off in S3-S5)	PM_SLP_S3#
+VCC_CORE	1.8V Core Voltage for Processor	VR_ON
+1_05VRUN	1.05V rail for Processor	PM_SLP_S3#
NVVD	V Core Voltage for nVIDIA N15E-GT/N15P-GX-B DGPU	VDD33_OK
+3V3_NV	3.3V PEX power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	GPU_PWRGD
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	GPU_PWRGD

Net Naming Conventions

Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints

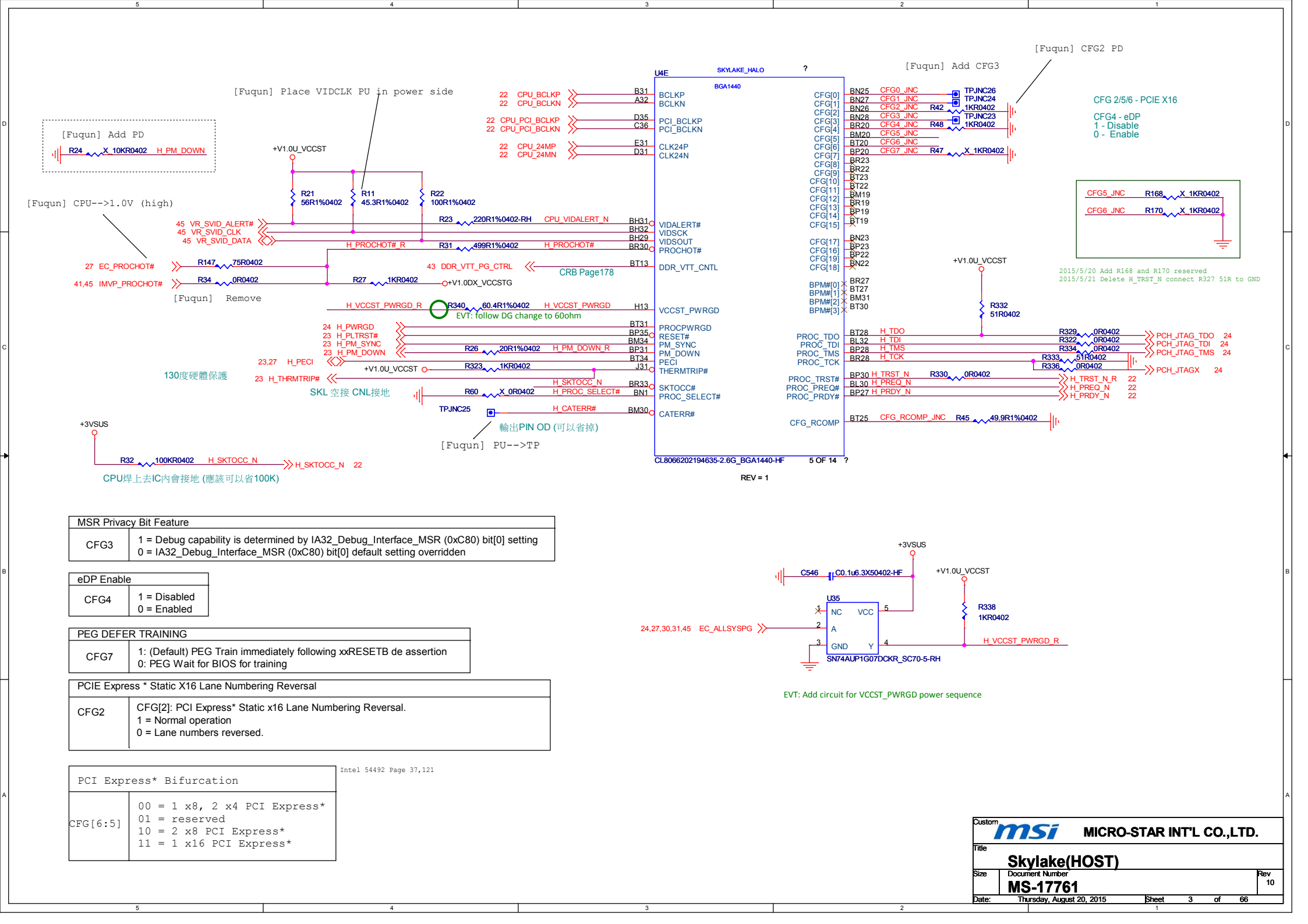


POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V*SUS will always keep high

N16E-GR	Stuff	L3006,PEC3012
	Un-Stuff	L3003
	Strap	Samsung K4G41325FC-HC03 0x2 Hynix H5GC4H24AJR-T2C 0x0
N16P-GX N16P-GT	Stuff	L3003
	Un-Stuff	L3006,PEC3012
	Strap	Samsung K4G41325FC-HC03 0x3 Hynix H5GC4H24AJR-T2C 0x6



DDR Channel A

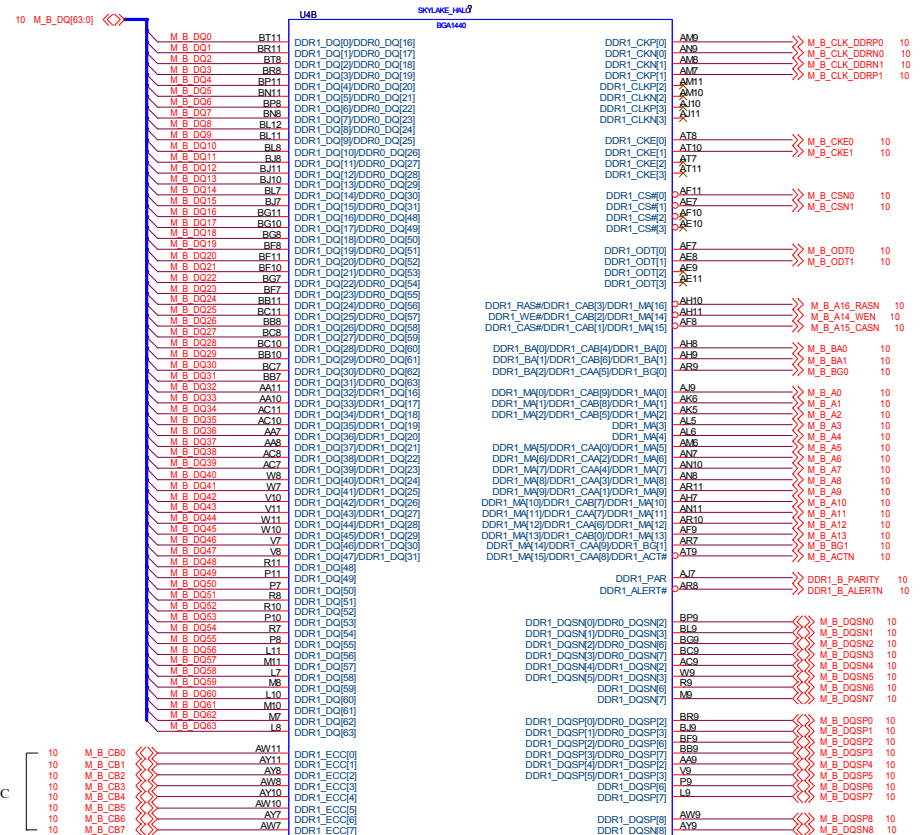


DDR CHANNEL A

CL8066202194635-2.6G_BGA1440-HF REV = 1 1 OF 14

2015/05/21 Delete R345, R339, C615

DDR Channel B

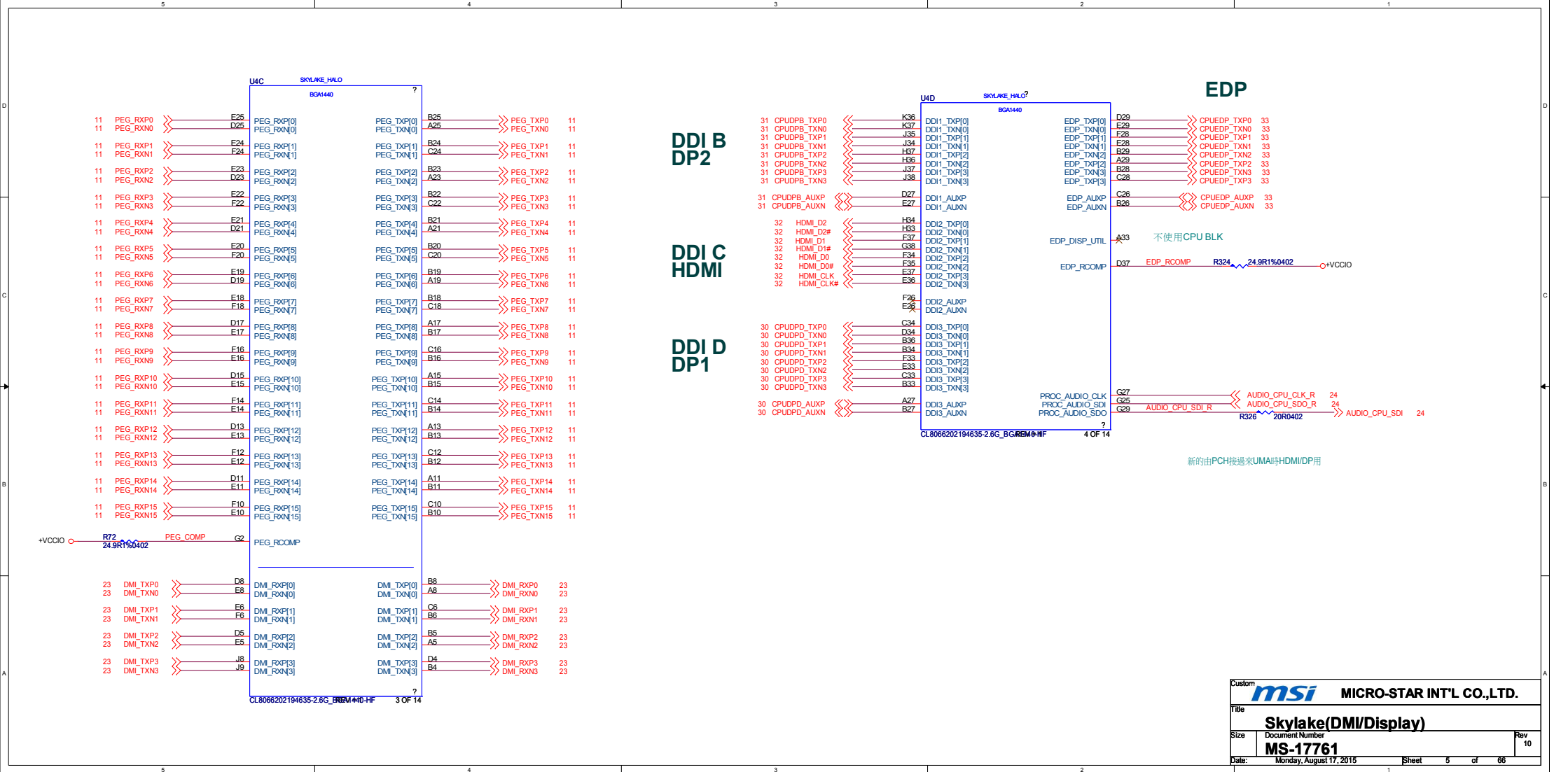


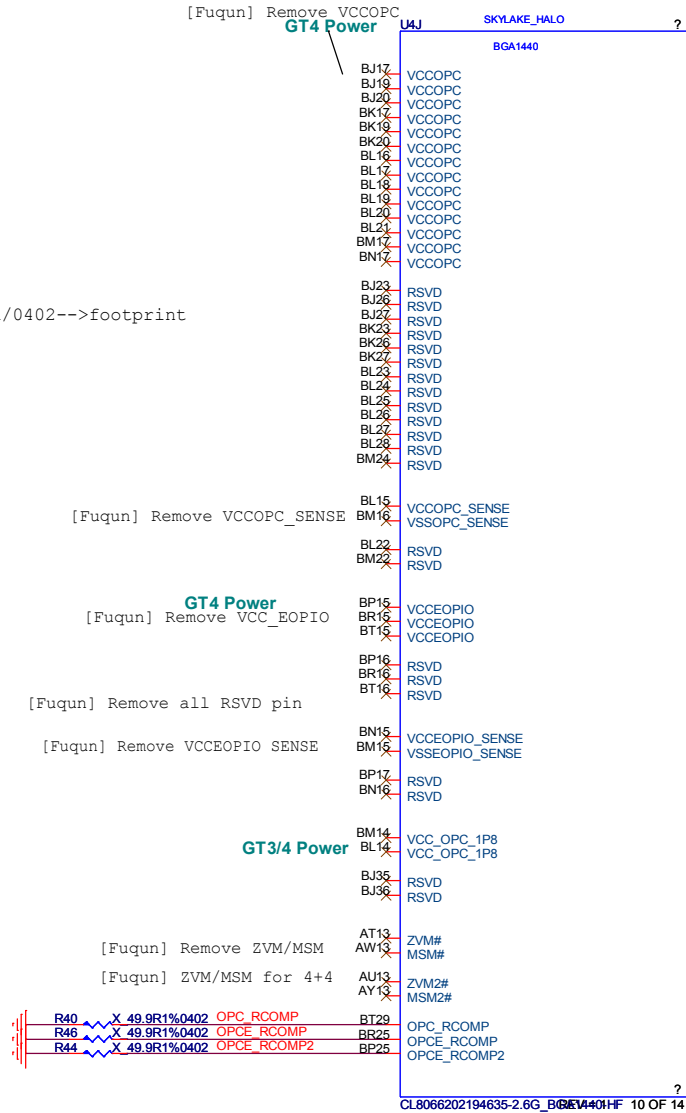
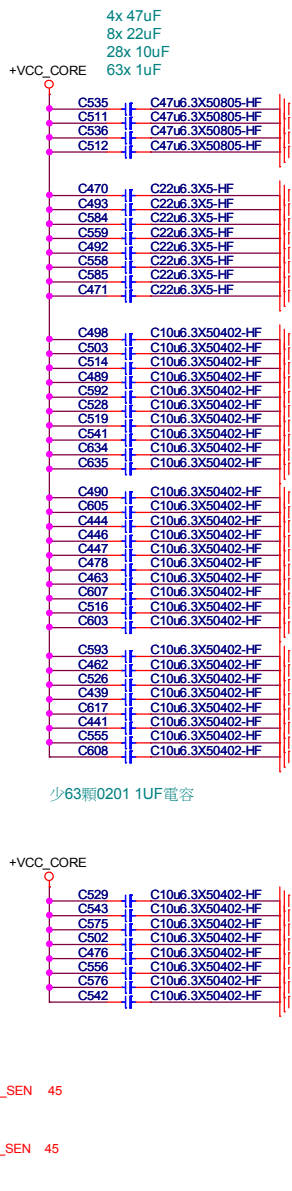
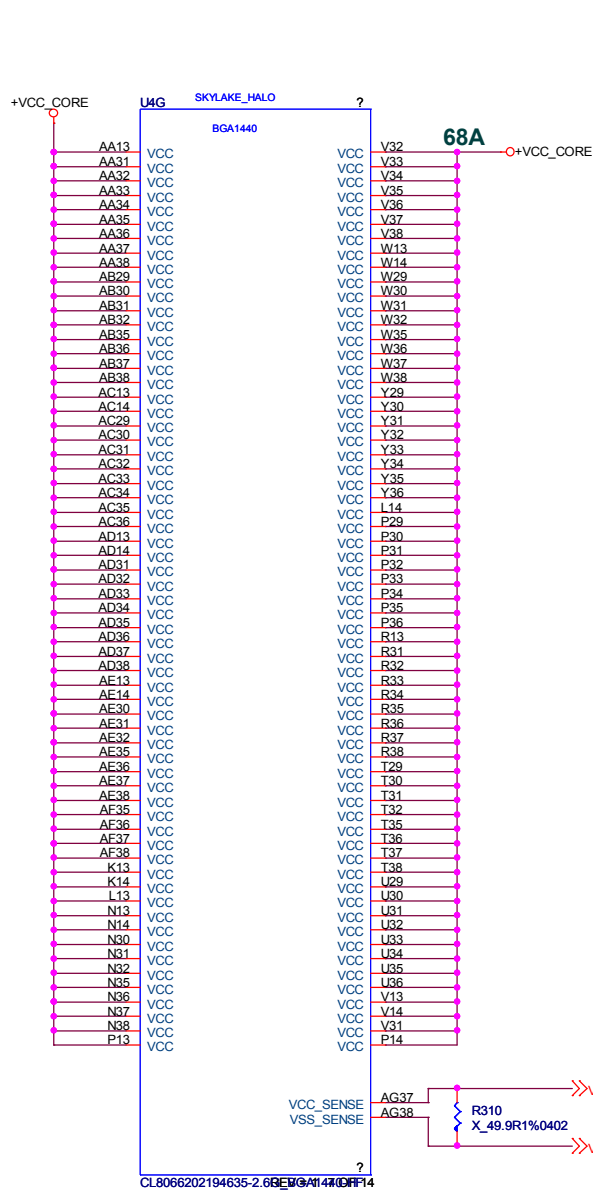
DDR CHANNEL B

CL8066202194635-2.6G_BGA1440-HF REV = 1 2 OF 14

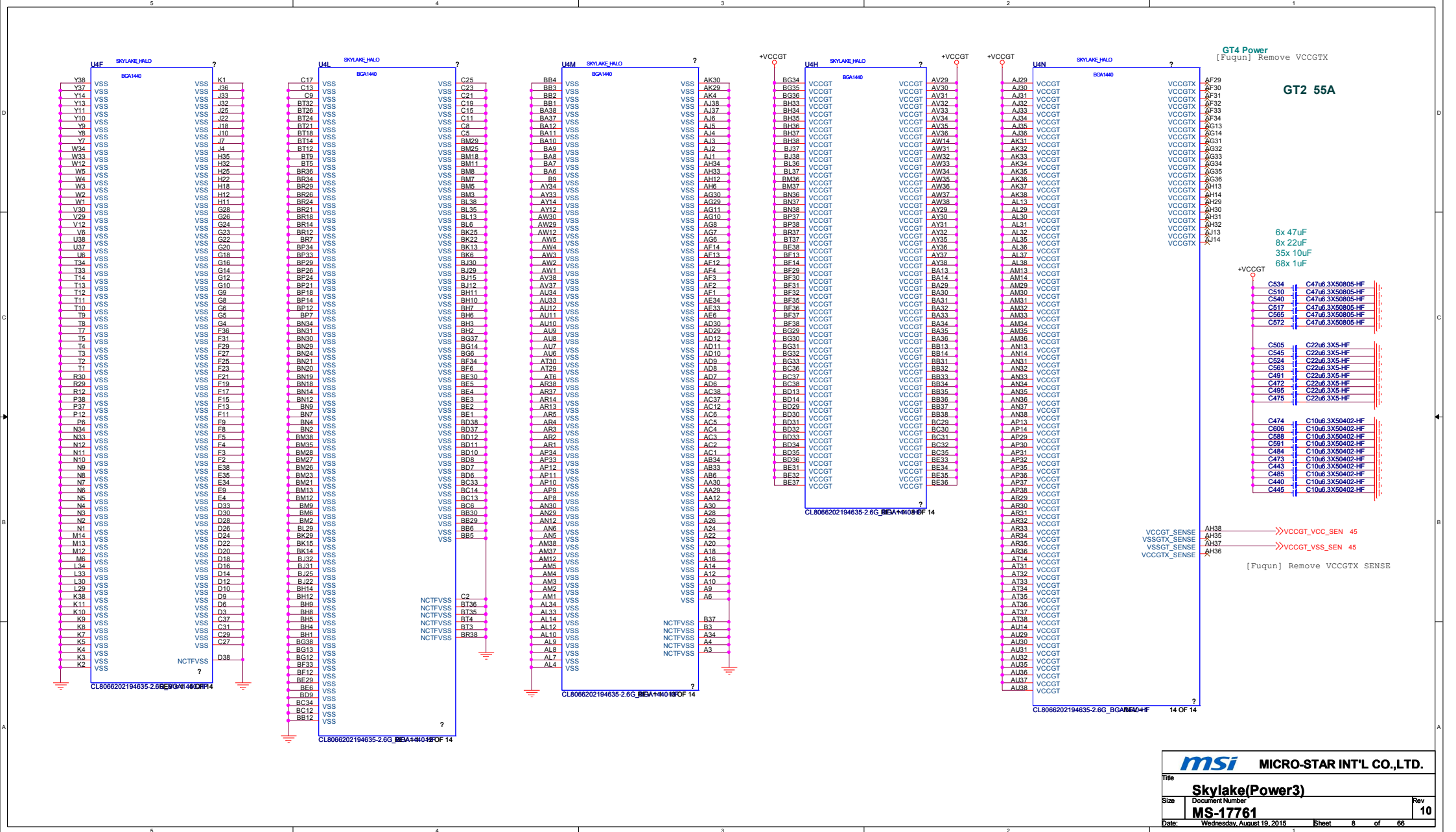
2015/05/21 M_VREF_DQ_DIMMA change to TPJNC21

Customer		msi MICRO-STAR INT'L CO.,LTD.	
File		Skylake(DDR4)	
Size	Document Number	Rev 10	
MS-17761			
Date	Monday, August 17, 2015	Sheet	4 of 66

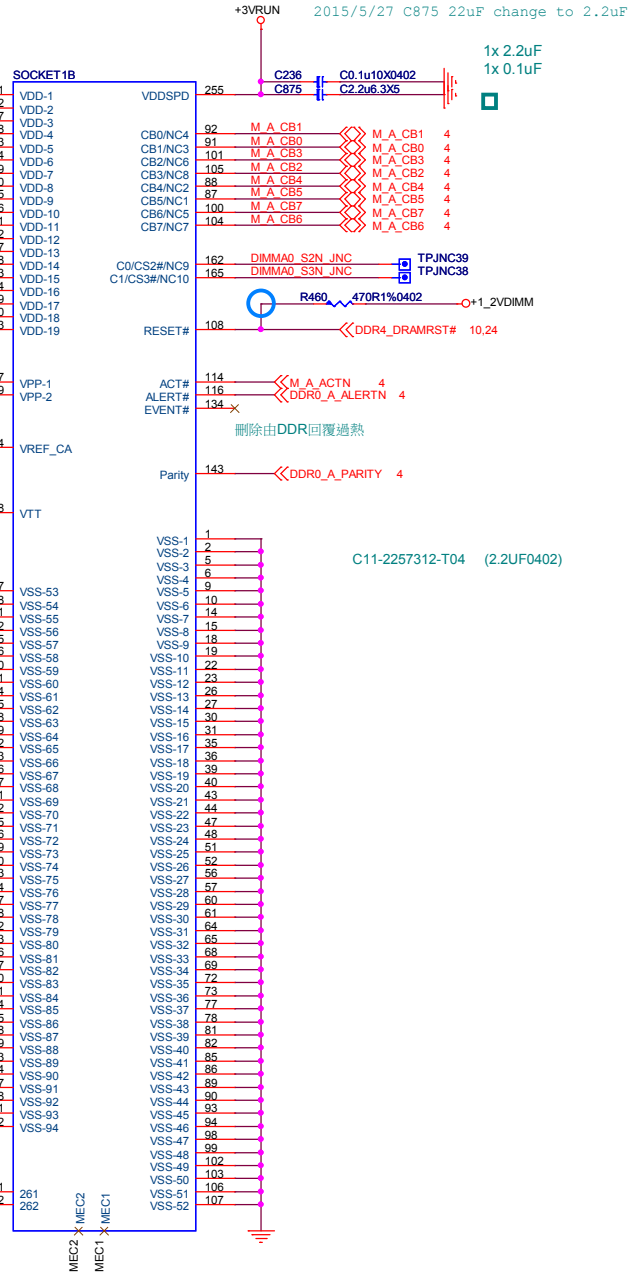
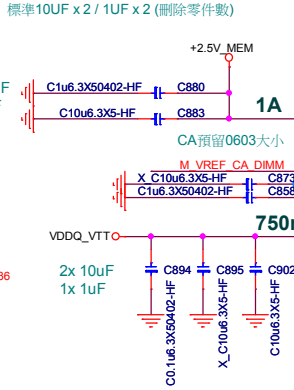
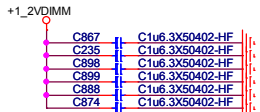
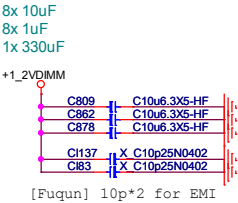
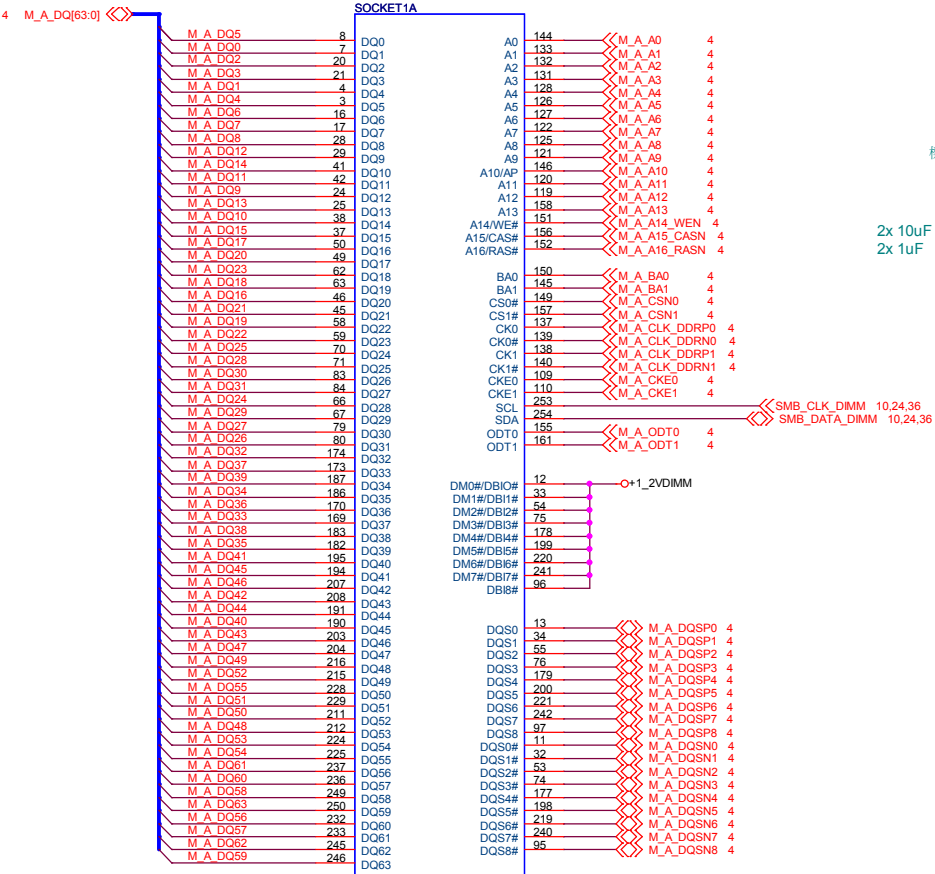




[Fuqun] +V1_8SUS_OPC move to page53



SODIMM_A0 (TOP-Reverse)

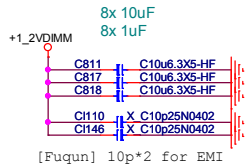



DDR4SODIMM-260PS_BLACK-HF-20

DDR4_SODIMM260P_H4_5

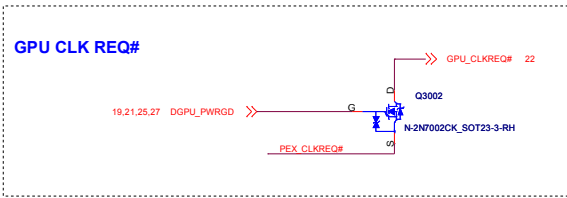
N13-2600220-L41

msi MICRO-STAR INT'L CO.,LTD.		
File		
DDR4 SODIMM A		
Size	Document Number	Rev
Custom	MS-17761	10
Date:	Wednesday, August 19, 2015	Sheet 9 of 66

[illegible]

 MICRO-STAR INT'L CO.,LTD.	
Title DDR4 SODIMM B	
Size Custom	Document Number MS-17761
Date: Tuesday, August 11, 2015	Sheet 10 of 66 Rev 10

N16P-GX(PCI-Express Gen3 x16 Interface)



GTX960

B03-0N16P25-N08
X_N16P-GX-A2-F

GTX950

B03-0N16P05-N08
X_N16P-GT-A2

缺PN

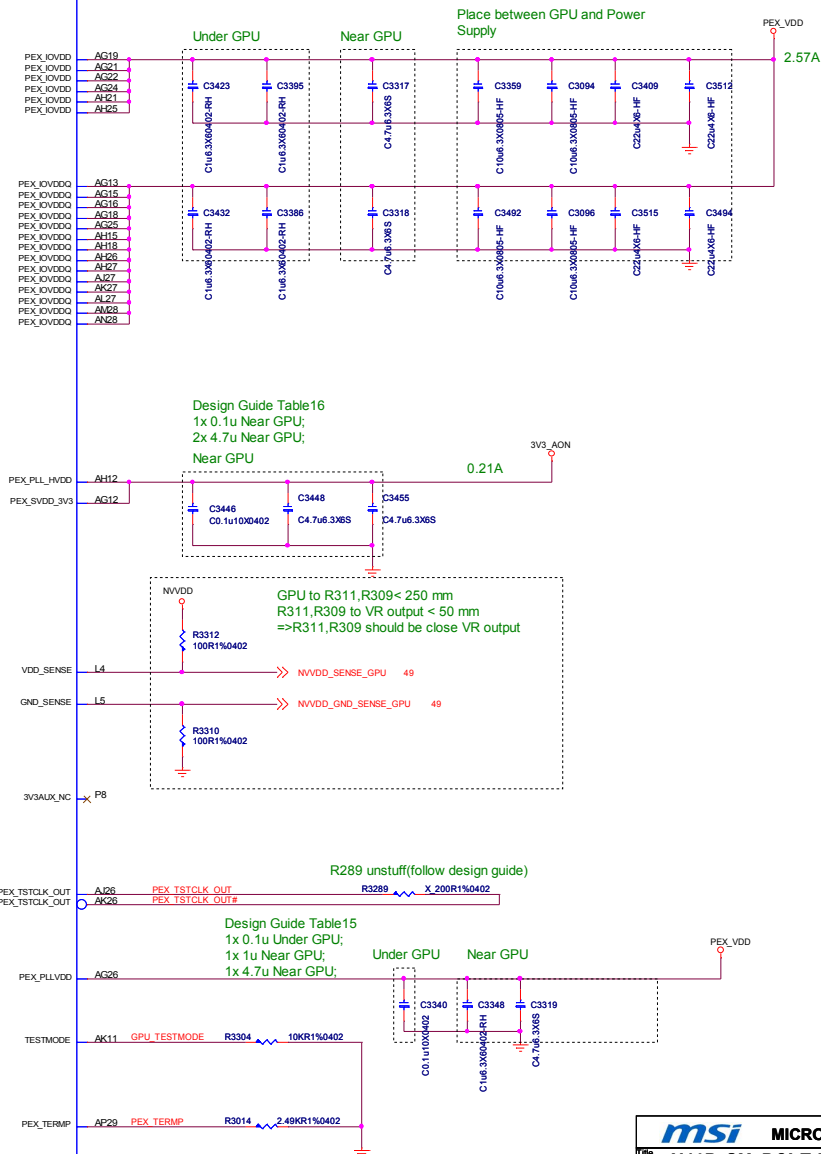
N16EGR

 **B03-0N16P05-N08**
X_N16P-GT-A2

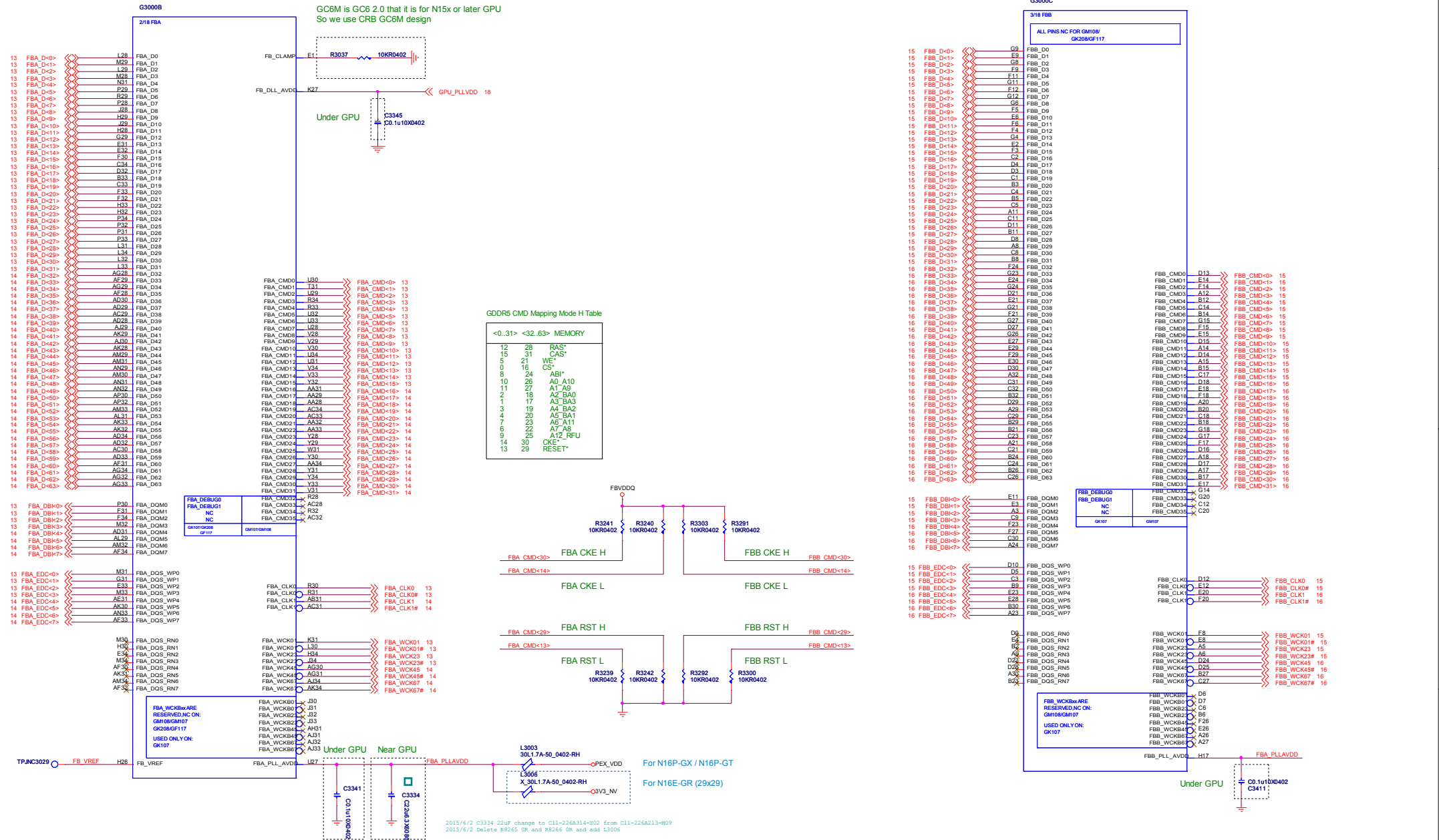
Design Guide Table 14

4x 1u under GPU;

4x 10u, 4 x 22u Place between GPU and Power Supply



N16P-GX(Frame Buffer Interface)

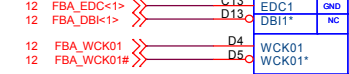
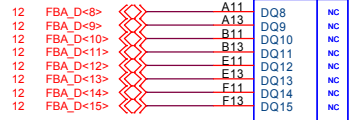
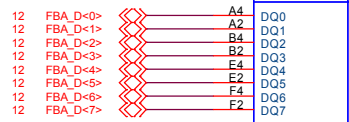


N16P_GX(GDDR5 Frame A-1)

M3000D
INS178575080
?

COMMON

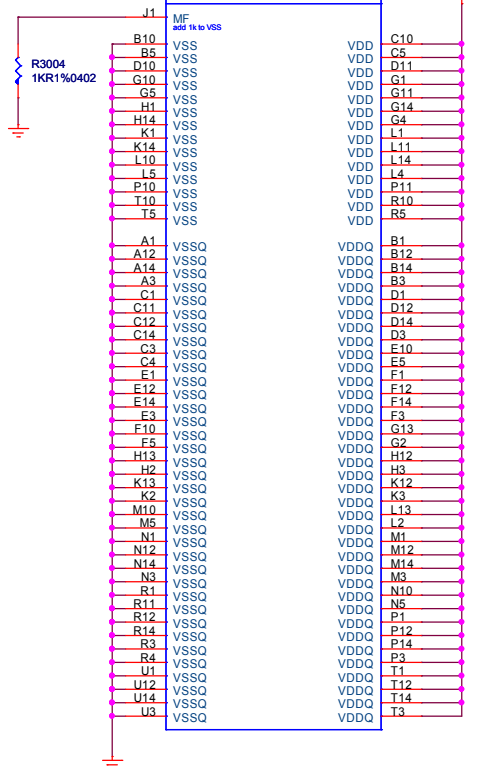
NORMAL



M3000C
INS178575145
?

COMMON

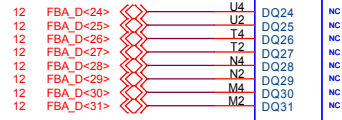
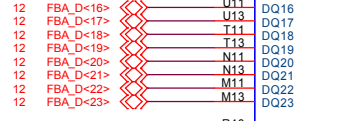
Normal



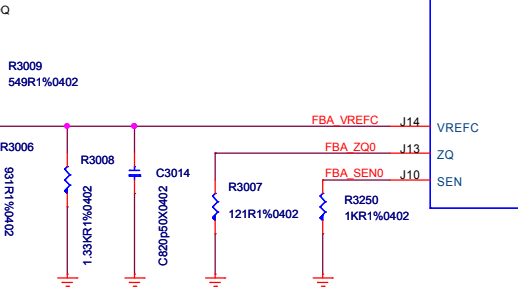
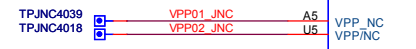
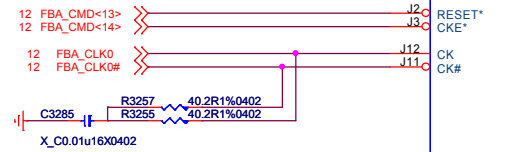
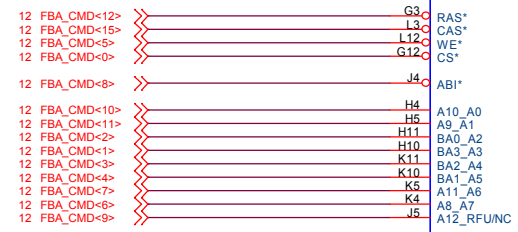
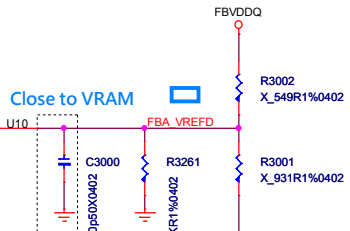
M3000A
INS178574827
?

COMMON

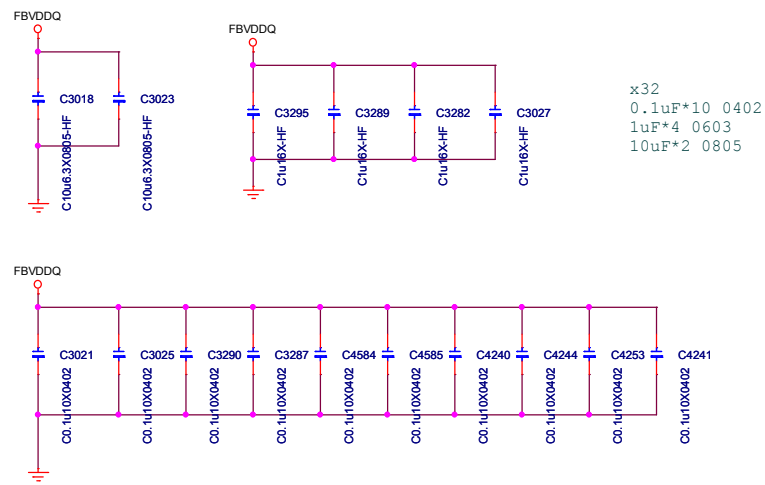
NORMAL



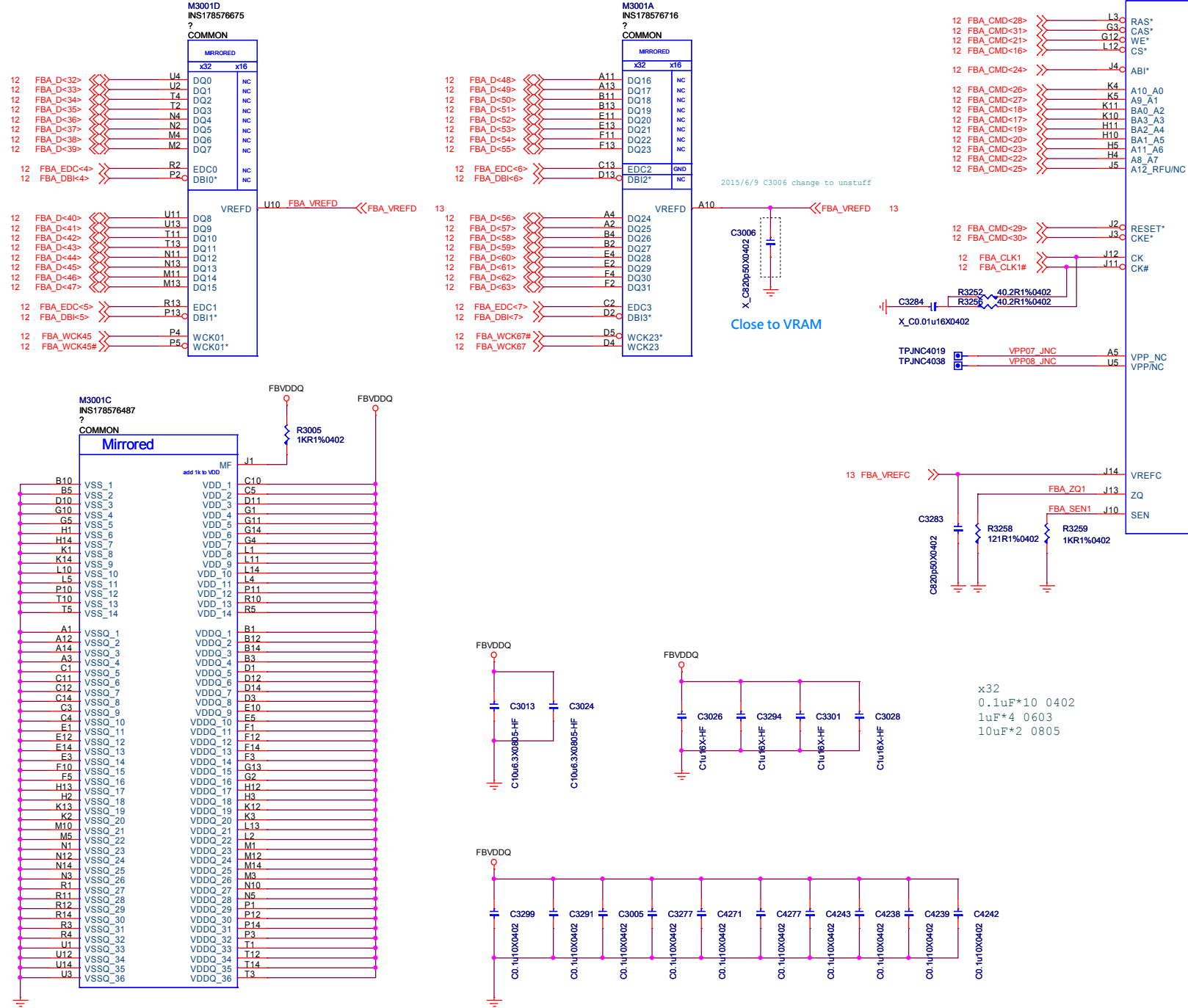
2015/6/9 C3000, R3261,R3002,R3001 change to unstuff



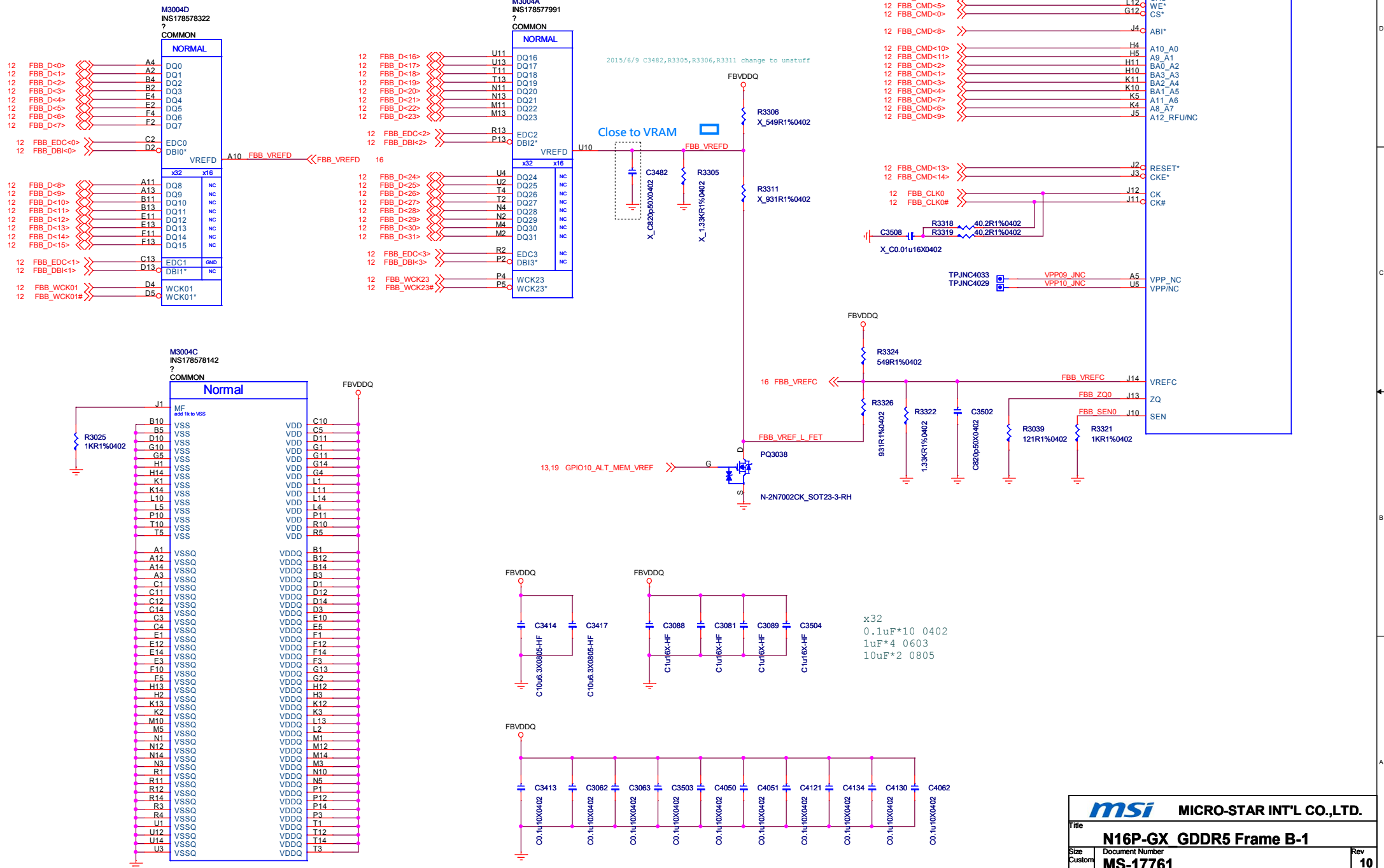
4/13 更換主料 F09-會逐漸不使用改用D03-07002F9-N47為主料



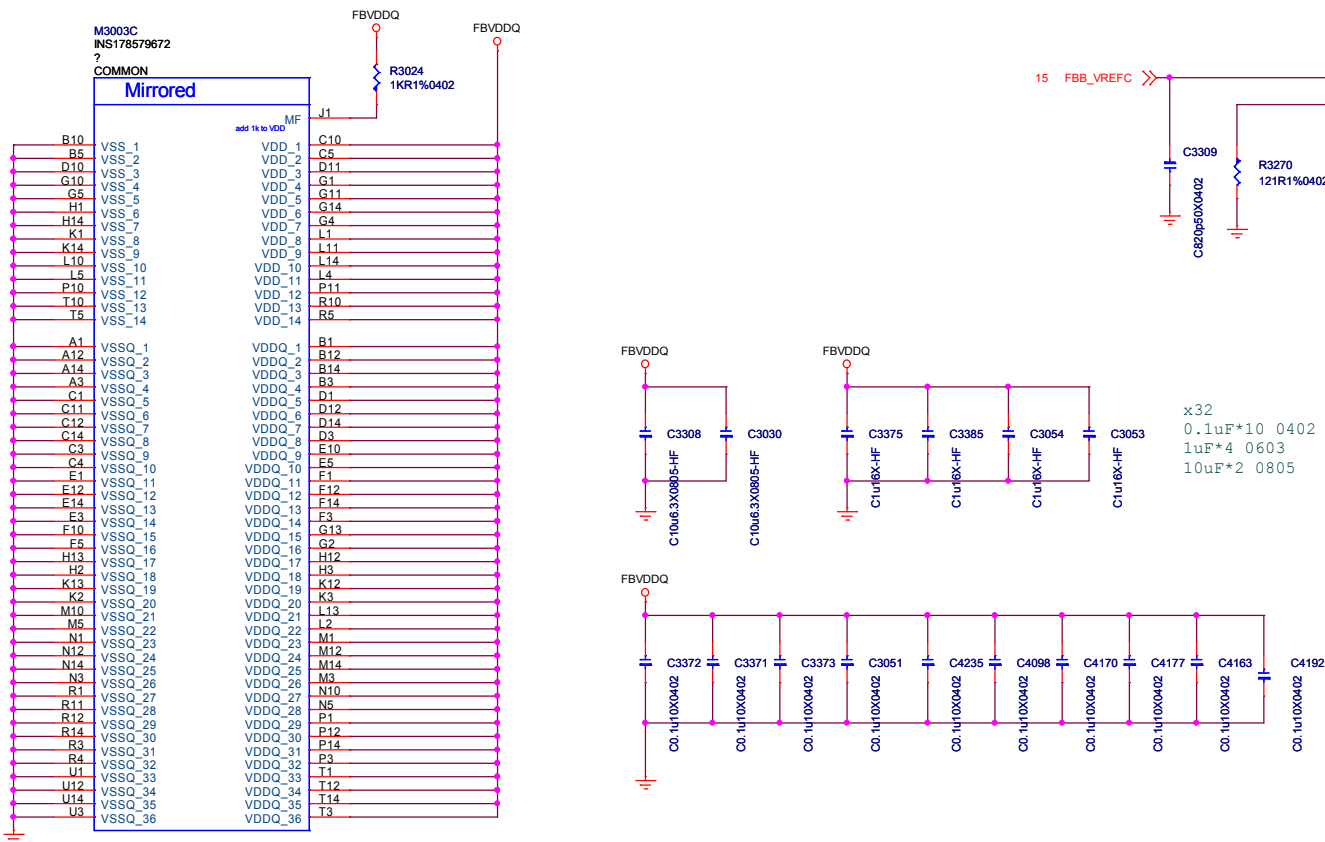
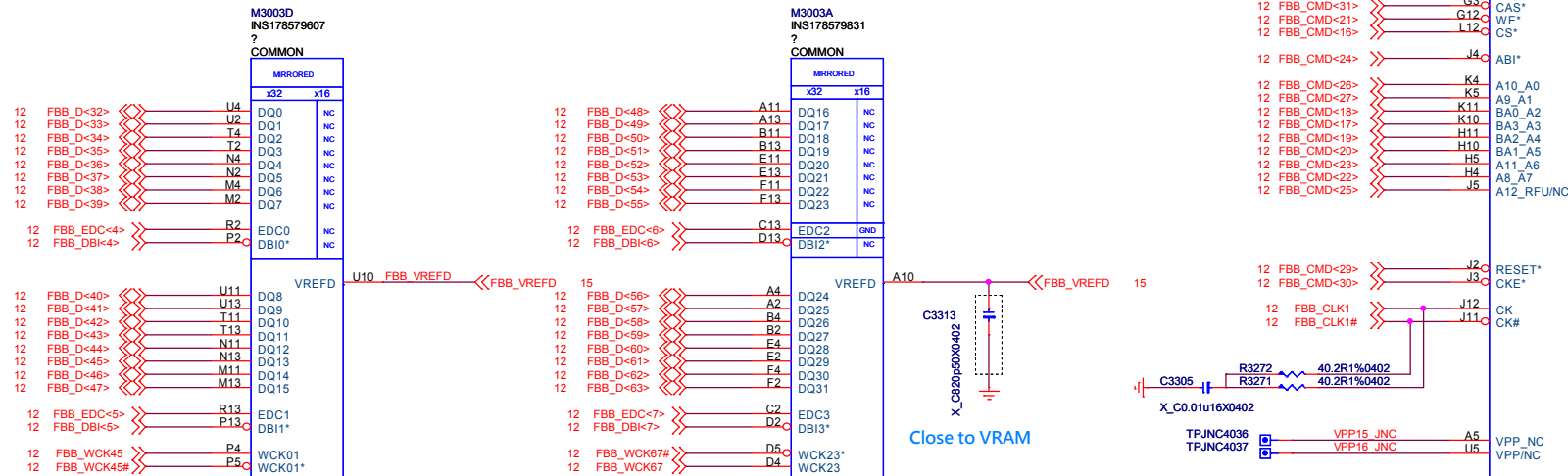
N16P_GX(GDDR5 Frame A-2)



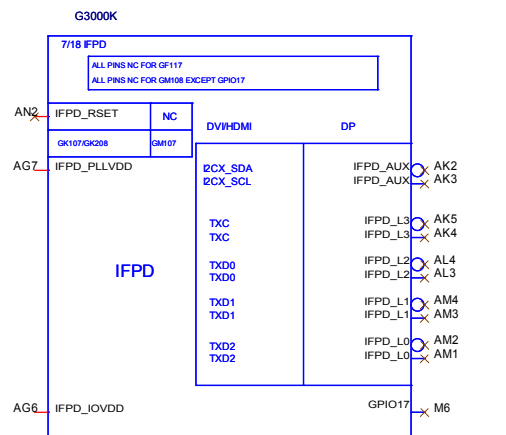
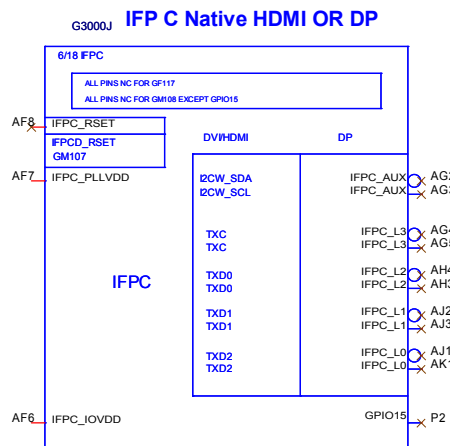
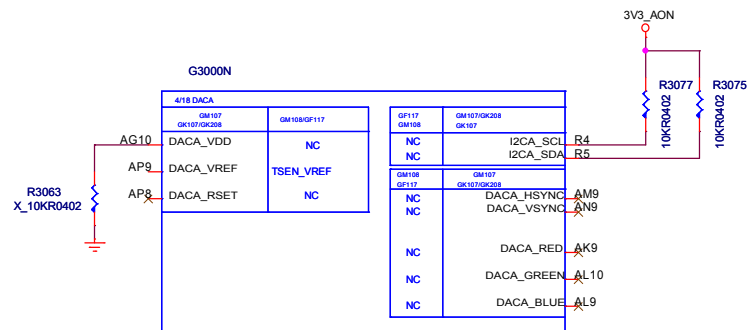
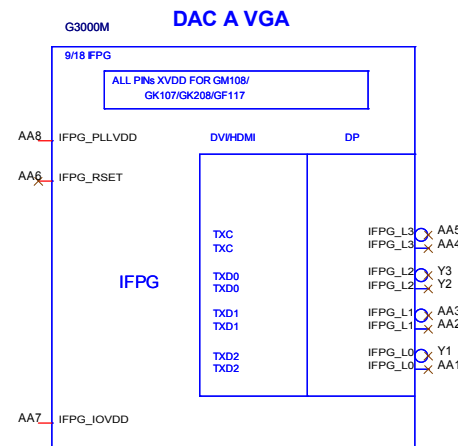
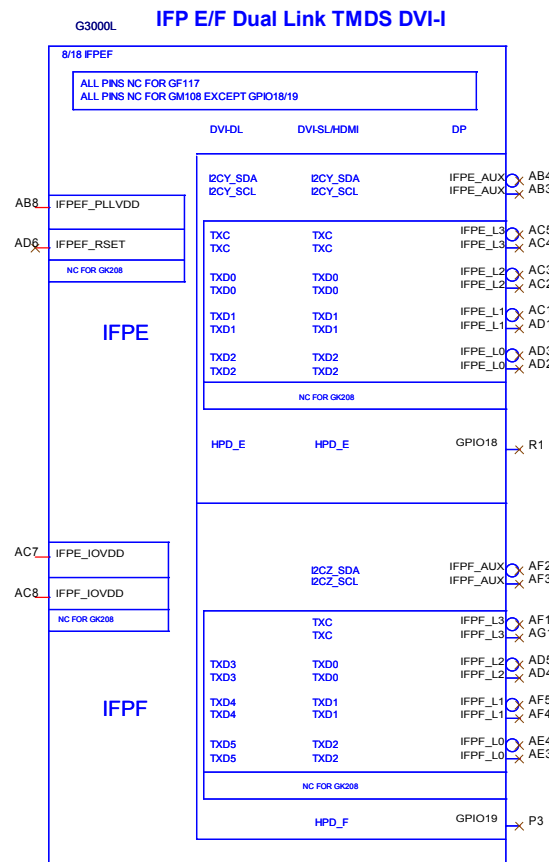
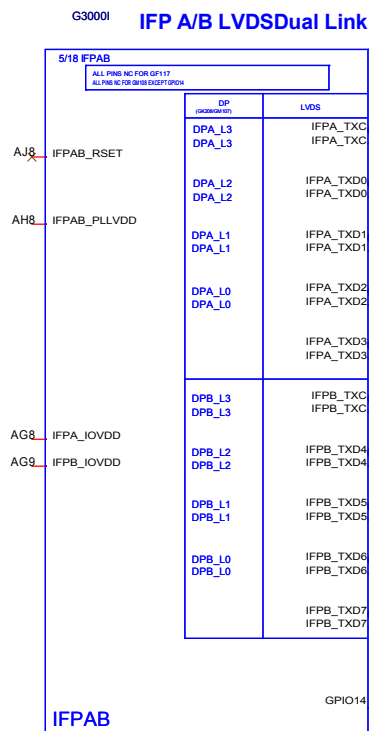
N16P_GX(GDDR5 Frame B-1)



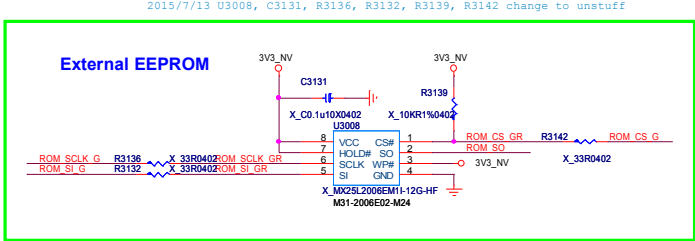
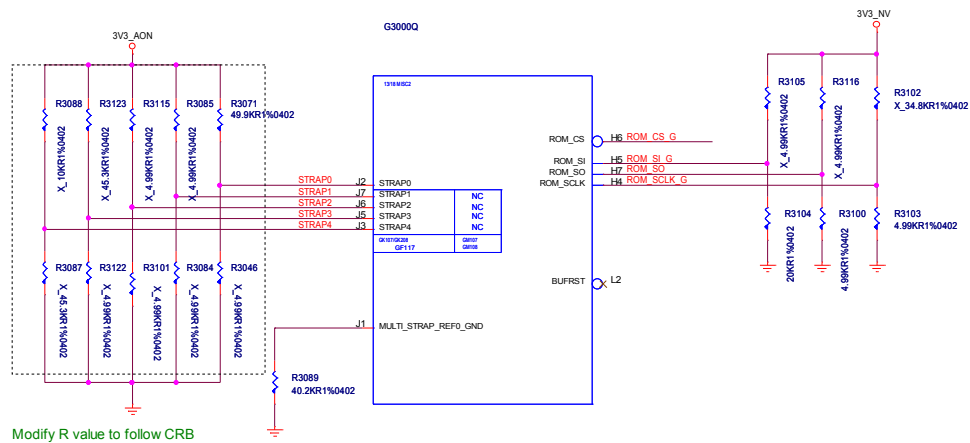
N16P_GX(GDDR5 Frame B-2)



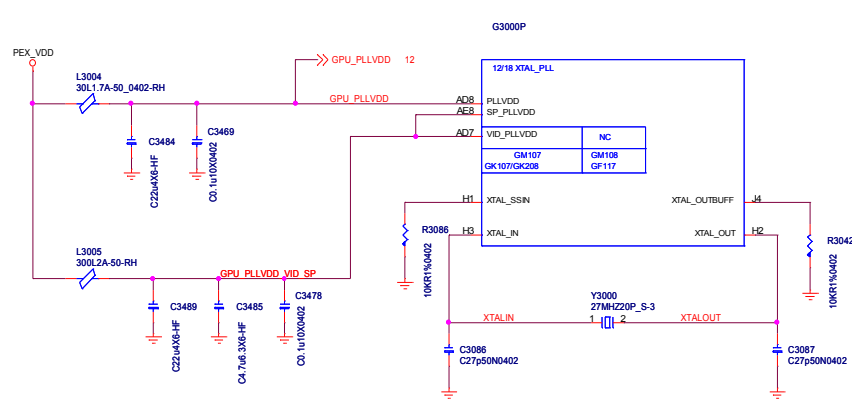
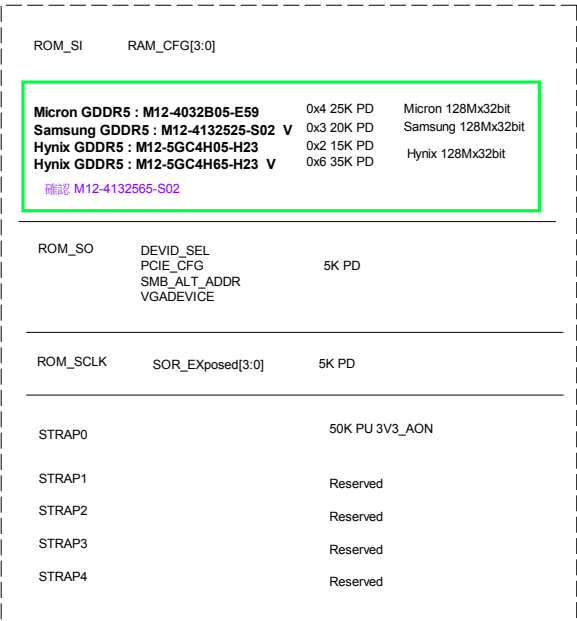
N16P-GX(Display IF)



N16P-GX_ROM & HW Straps



GND		3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
PD		PU

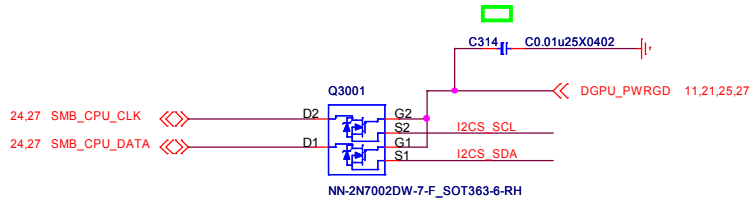


BOT 記得轉階層
DEFAULT SETTING

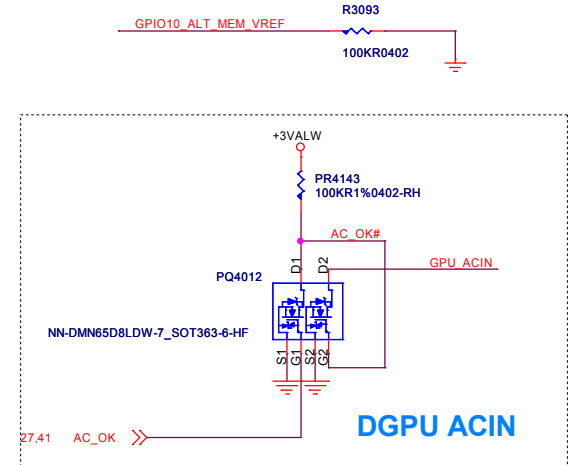
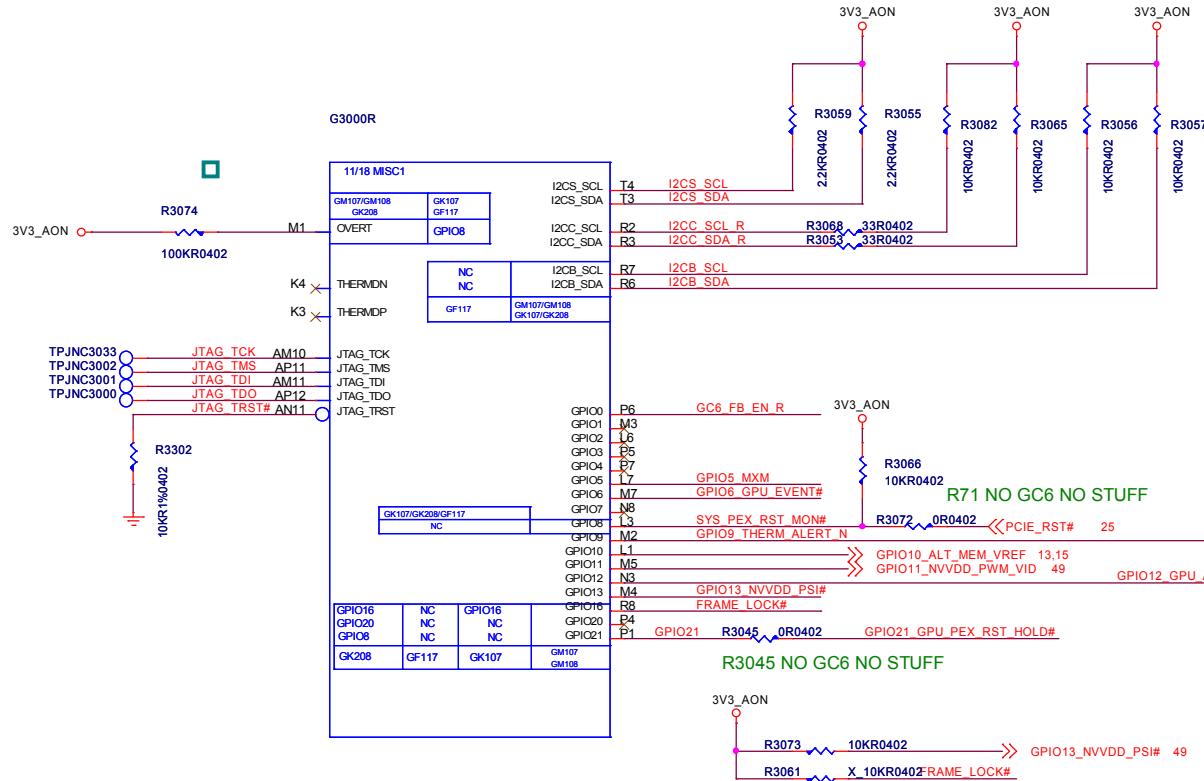
BOT 記得轉階層

ROM_S1 Samsung 128Mx32bit R11-0203T12-W08 X_20KR1%0402	5010 0X3 V	V_TOP_S1 5010 M12-413252S-S02 X_K4G41325FC-HC03
ROM_H1 Hynix 128Mx32bit R11-3482T12-W08 X_34.8KR1%0402	5010 0X6 V	V_TOP_H1 5010 M12-5GC4H65-H23 X_H5GC4H24AJR-T2C
ROM_M1 Micron 128Mx32bit R11-2492T12-W08 X_24.9KR1%0402	5010 0X4	V_TOP_M1 5010 M12-4032B05-E59 X_EDW4032BABG-60-F-HF
ROM_S2 Samsung 128Mx32bit R11-0153T12-W08 X_15KR1%0402	5010 0X2 N16-GR	V_TOP_S2 5010 M12-413252S-S02 X_K4G41325FC-HC03
ROM_H2 Hynix 128Mx32bit R11-4991T12-W08 X_4.99KR1%0402	5010 0X0 N16-GR	V_TOP_H2 5010 M12-5GC4H65-H23 X_H5GC4H24AJR-T2C

2015/8/11 Add ROM_S2,ROM_H2,V_TOP_S2,V_TOP_H2 for N16E-GR



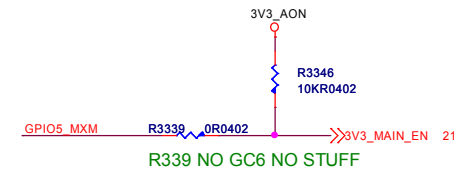
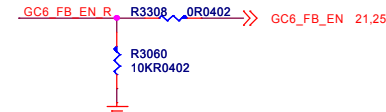
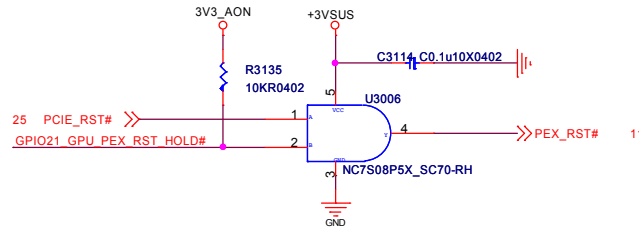
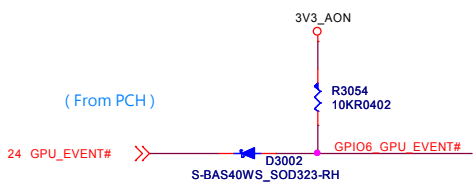
2015/6/4 Delete R3118, Q3003, R3125 on OVERT#



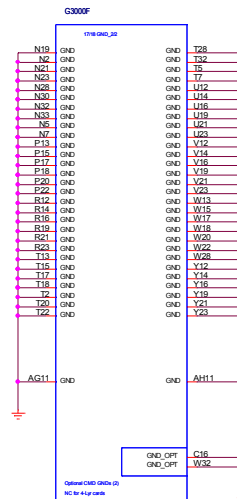
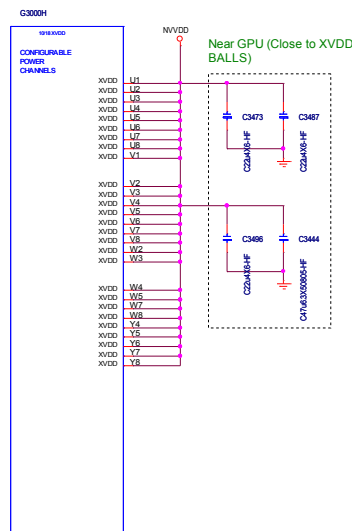
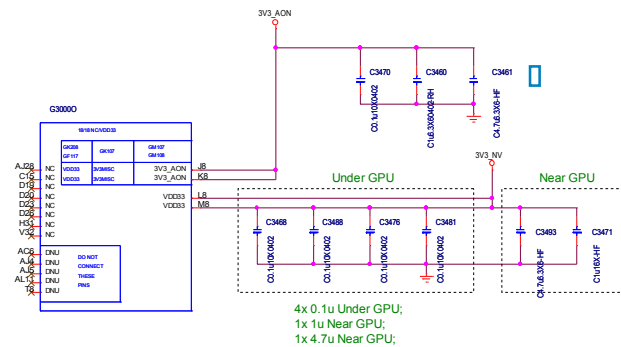
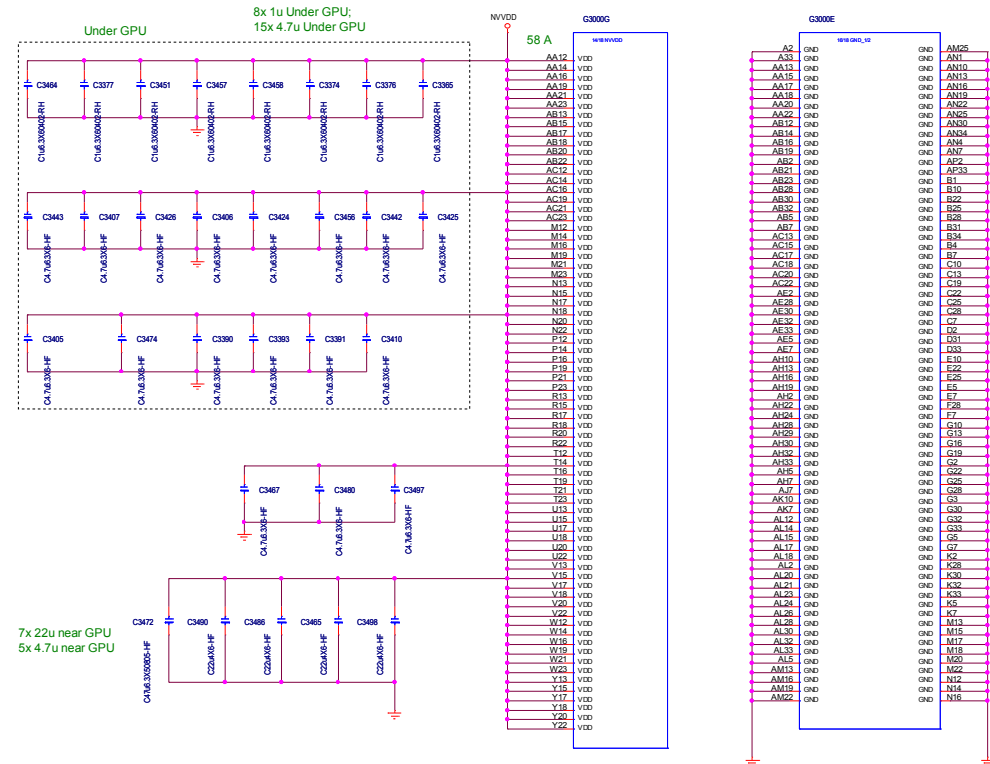
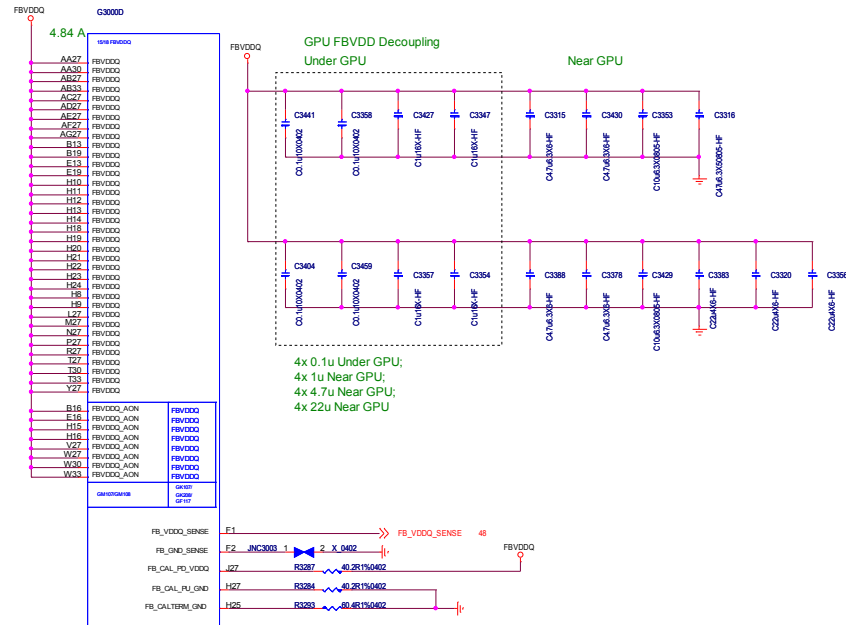
2015/6/4 Delete R3052 on EC_PROTECT_PWR

From EC
From Battery

GPIO12:
AC MODE : HIGH
DC MODE : LOW



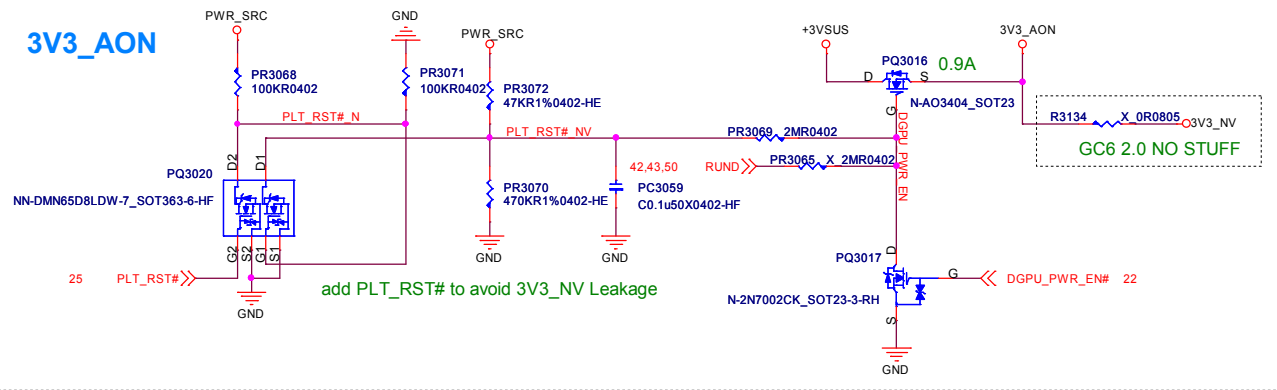
N16P-GX(Power & GND)



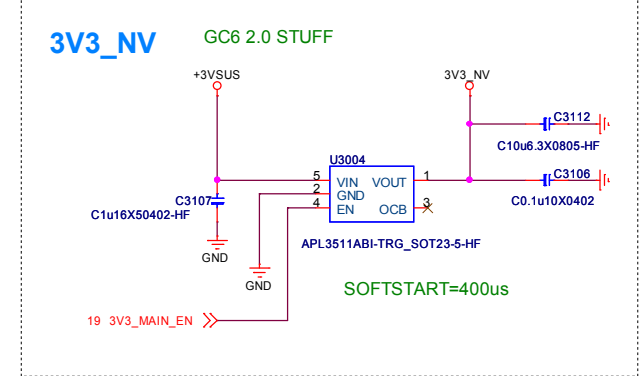
N16P-GX(Power Control)

nVIDIA Power Sequence Control
3V3_AON -> 3V3_NV -> NVVDD -> PEX_VDD -> FBVDDQ -> DGPUPWRGD

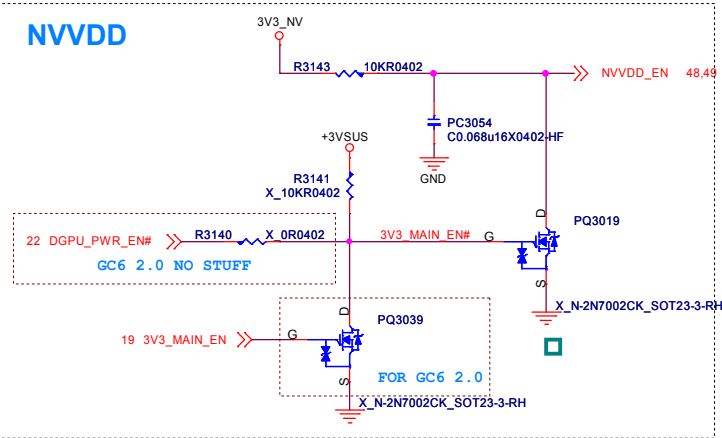
3V3_AON



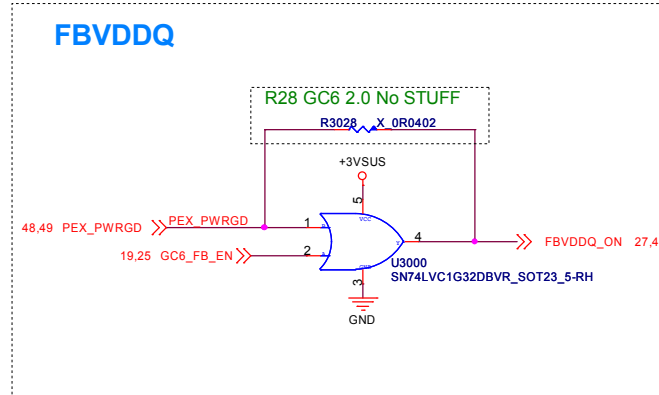
3V3_NV



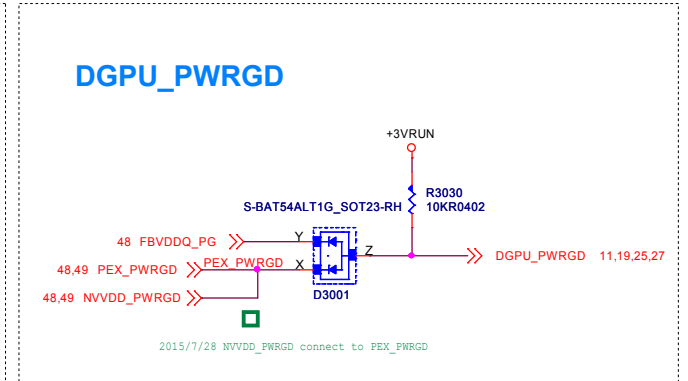
NVVDD



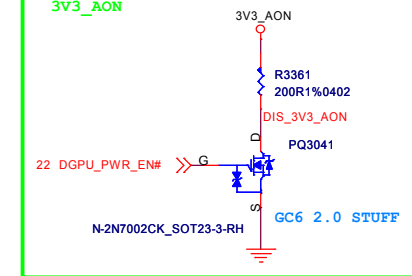
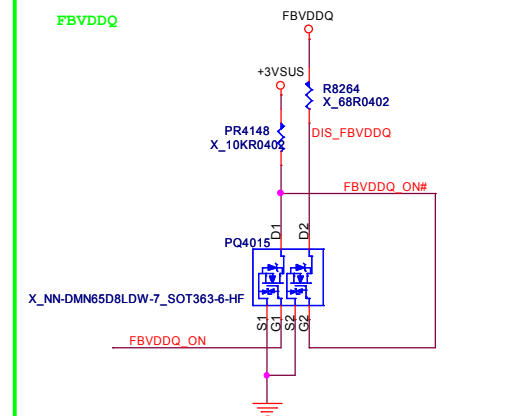
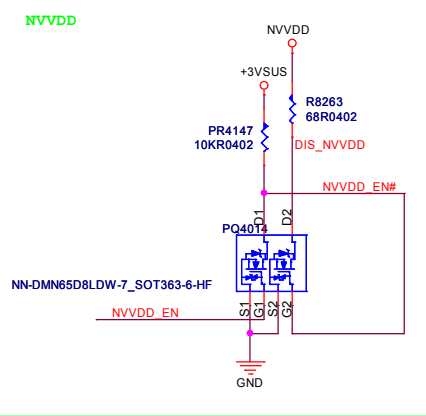
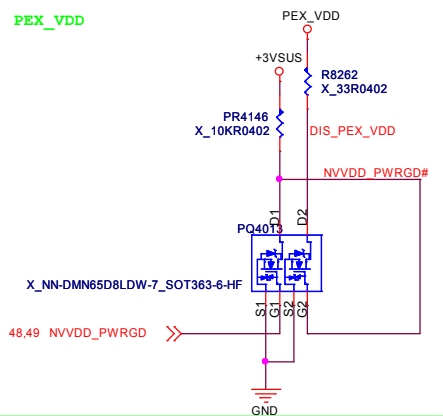
FBVDDQ

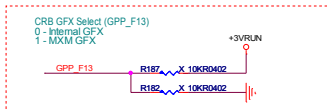
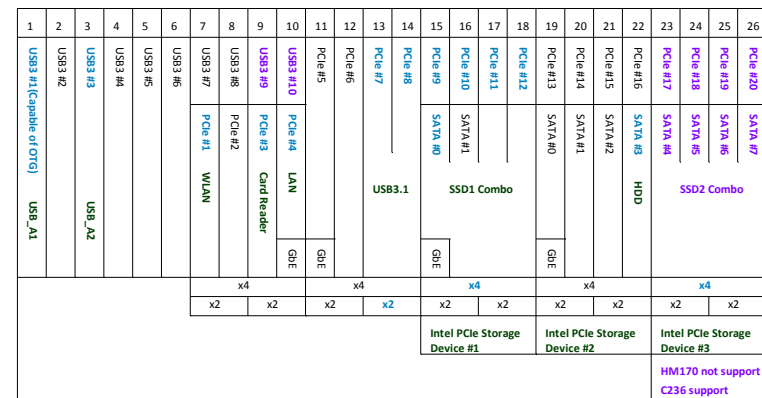
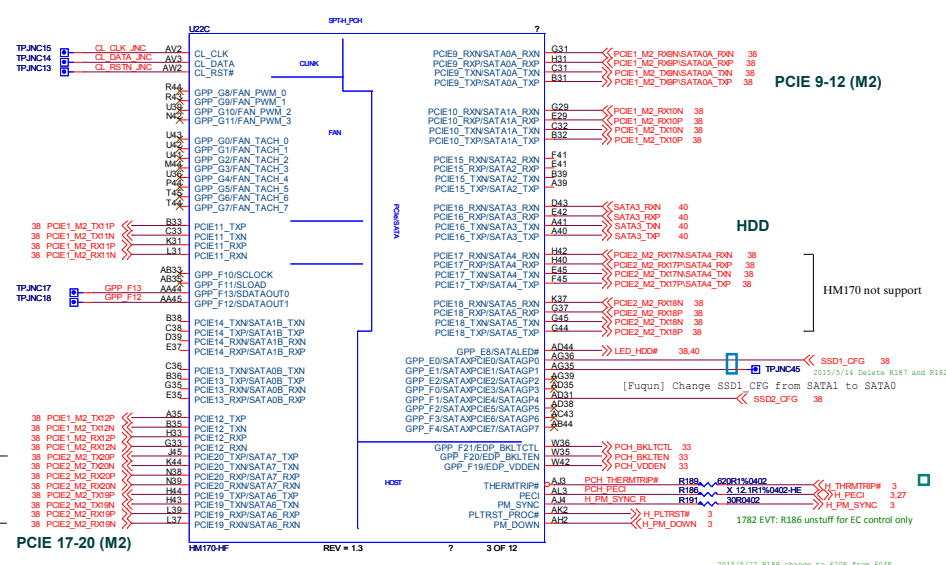
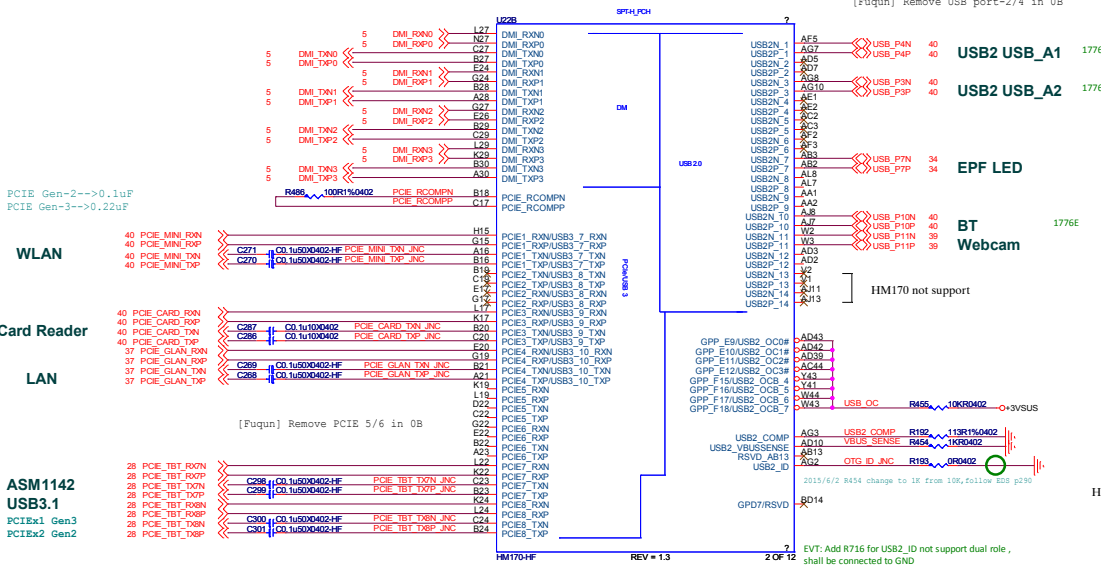


DGPU_PWRGD



Discharge Circuit

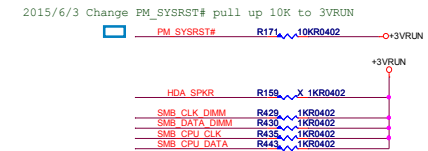
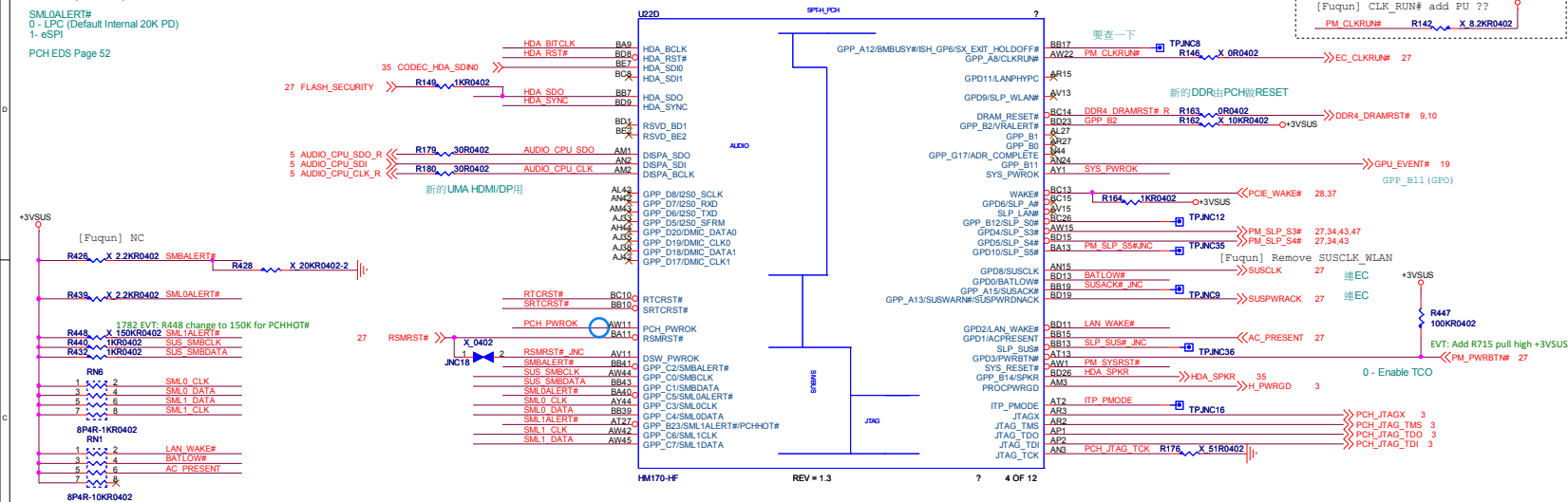




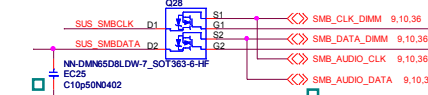
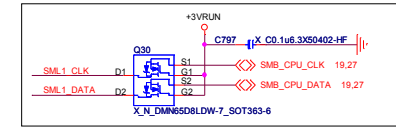
SMBALERT#
0 - Disable (Default Internal 20K PD)
1- Enable (AMT/SBA)

SML0ALERT#
0 - LPC (Default Internal 20K PD)
1- eSPI

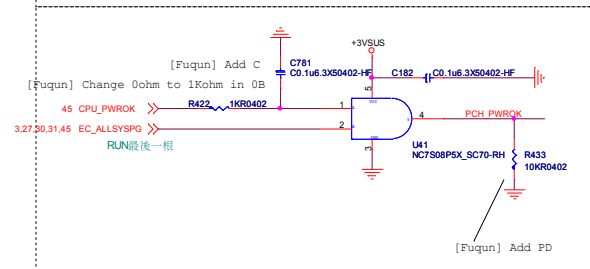
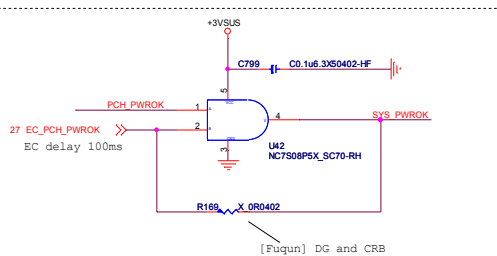
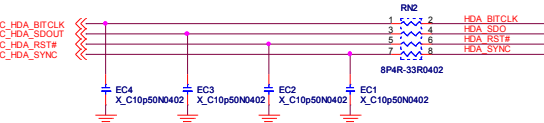
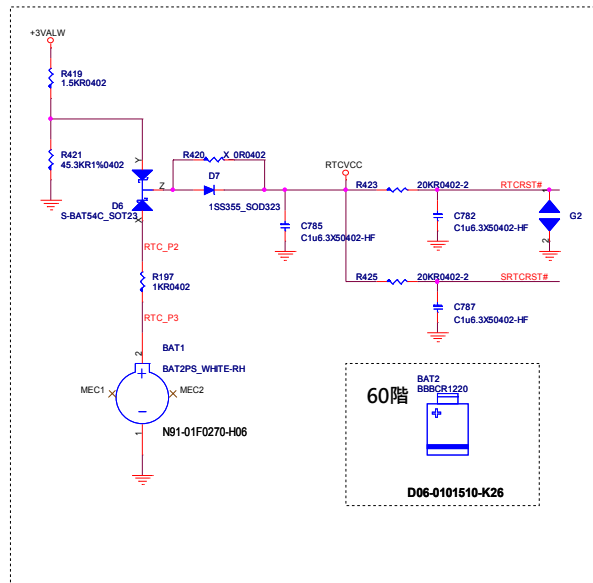
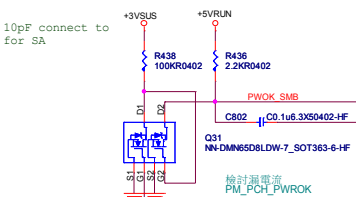
PCH EDS Page 52



2015/05/20 Q30 and C797 change to un-stuff



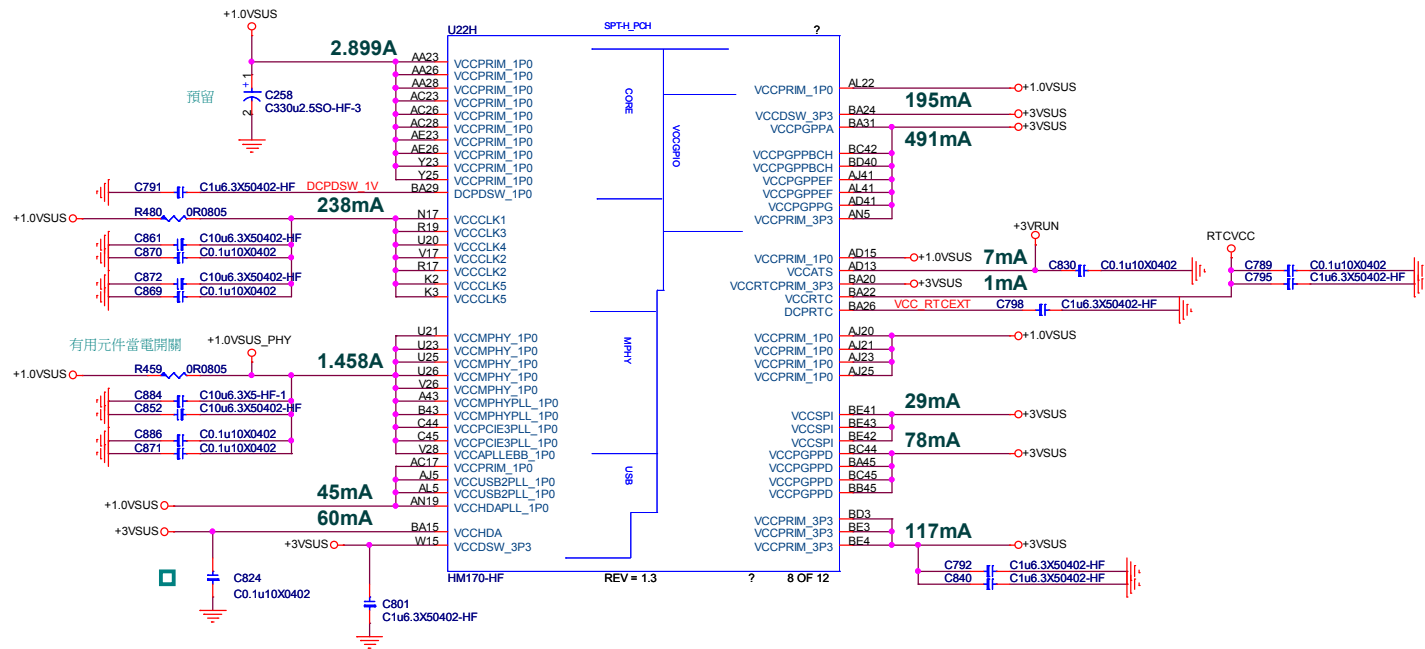
2015/7/28 Add EC25 10pF connect to
GND on SUS_SMBDATA for SA



```
2015/05/21 Add R339, R345, R427 51R pull up to +V1.0U_VCCST
2015/6/3 Delete R339, R345, R427
```

```
SML0 SMBUS to ESS
```

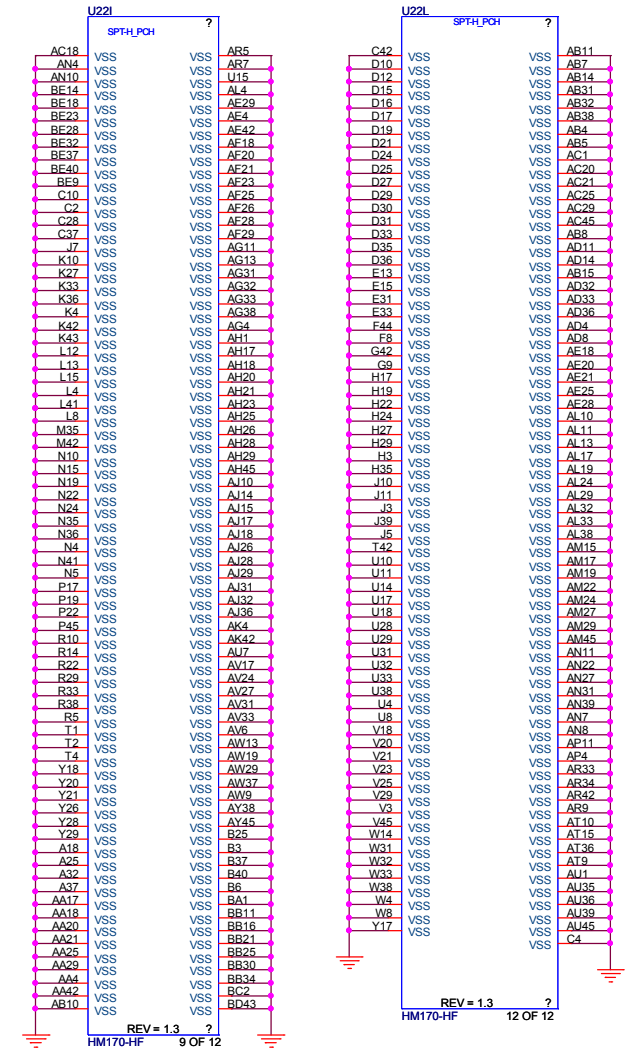
2015/7/28 Delete Q8,C206 ; SMB_AUDIO_CLK/SMB_AUDIO_DATA connect to
SMB_CLK DIMM/SMB_DATA DIMM



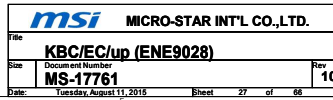
2015/05/21 C824 change to 0.1uF from 1uF

+1.0VSUS C1118 X C10p25N0402
+3VSUS C43 X C10p25N0402
[Fuqun] 10p*2 for EMI

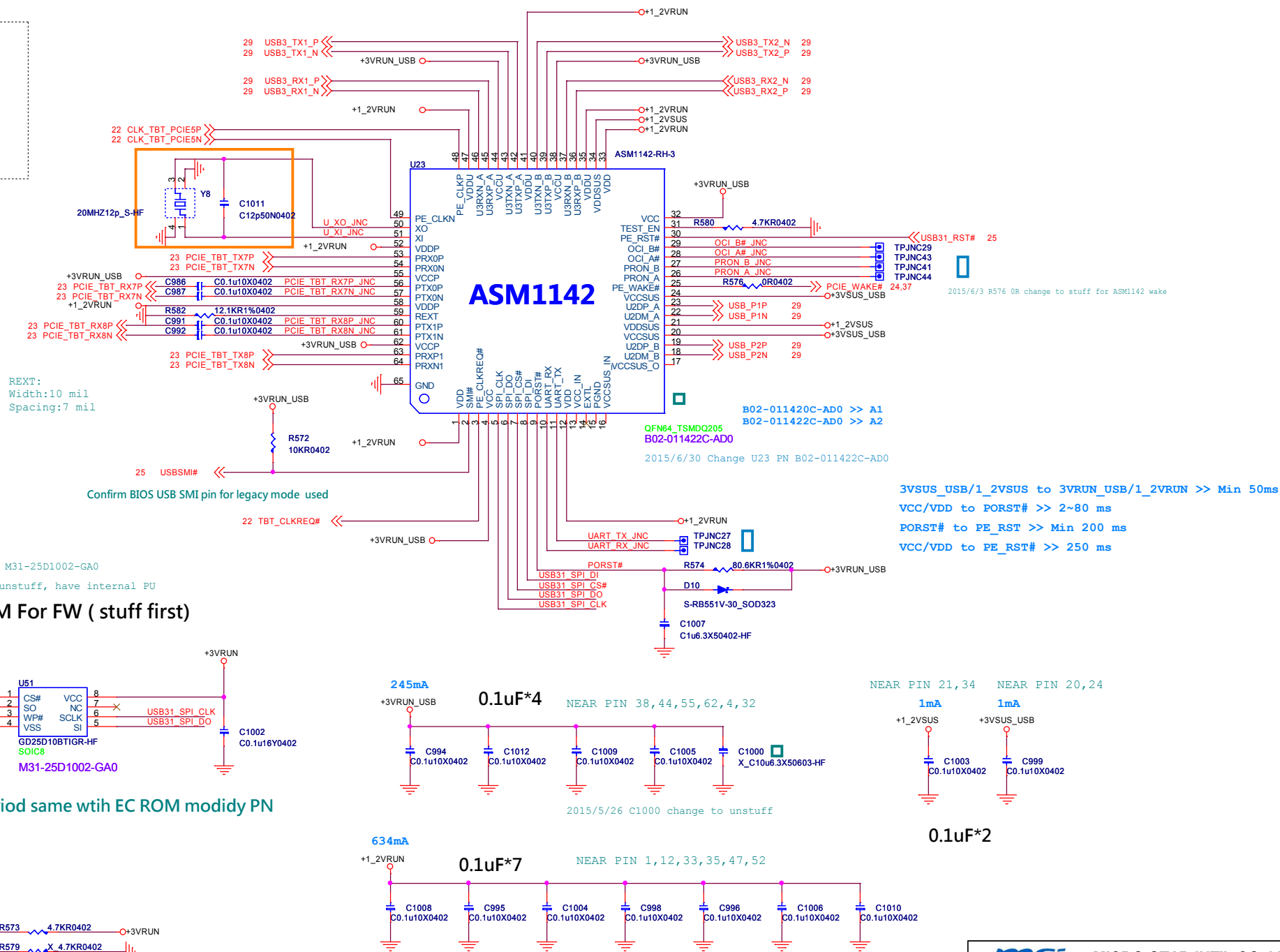
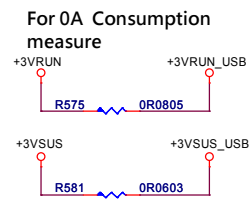
+1.0VSUS C828 C22u6 3X0603
C257 C22u6 3X0603
C803 C0.1u10X0402
C882 C0.1u10X0402
[Fuqun] Add
+3VSUS C194 C22u6 3X0603
C836 C22u6 3X0603
C183 C0.1u10X0402
C837 C0.1u10X0402
C187 C22u6 3X0603
C784 C0.1u10X0402



2015/7/28 Add C155 22pF connect to GND on LPC_FRAME# for SA



PCIE to USB 3.1

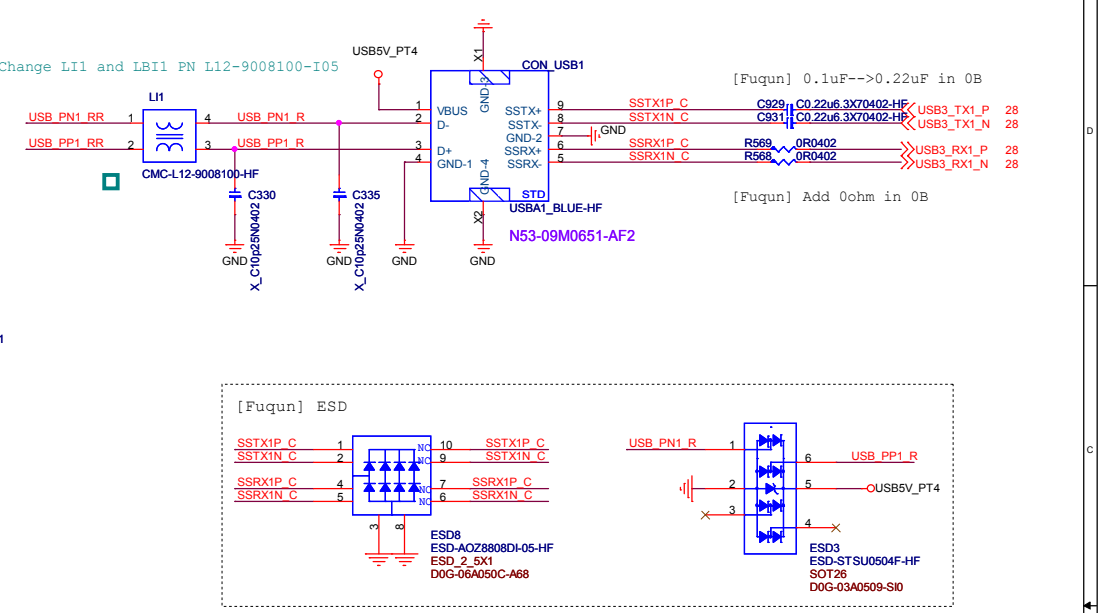
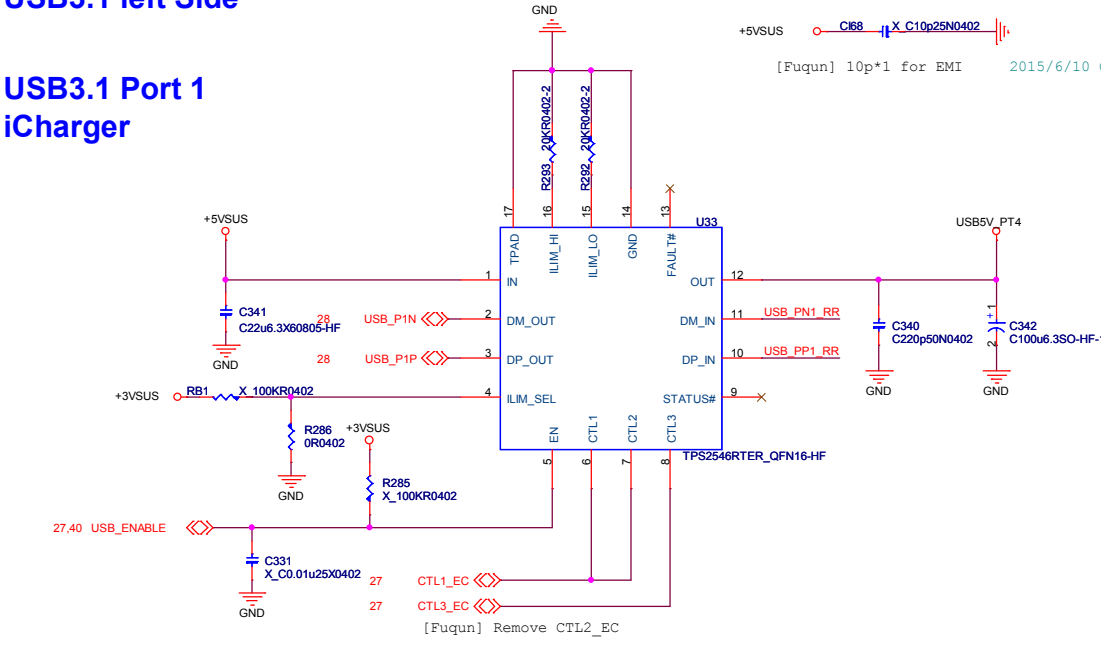


Description	
SPI_CLK	1: D3 cold (Default)
	0: D3 Hot

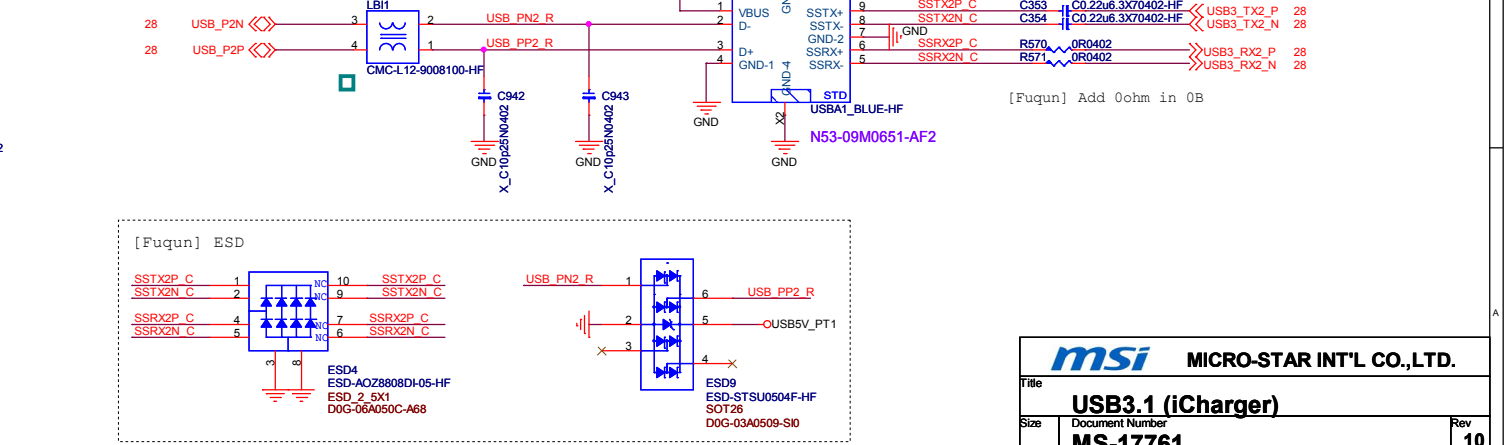
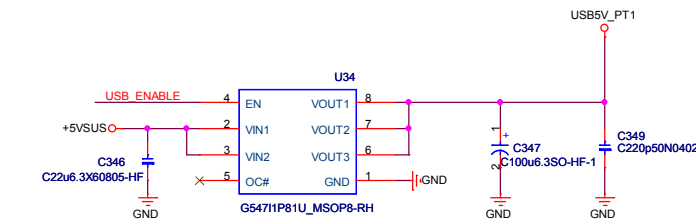
UART[RX:TX] 11: Asynchronous mode with external 20MHz crystal (Default)

USB3.1 left Side

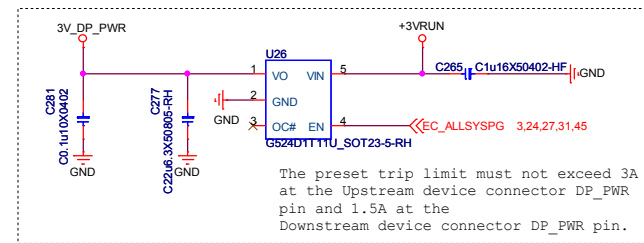
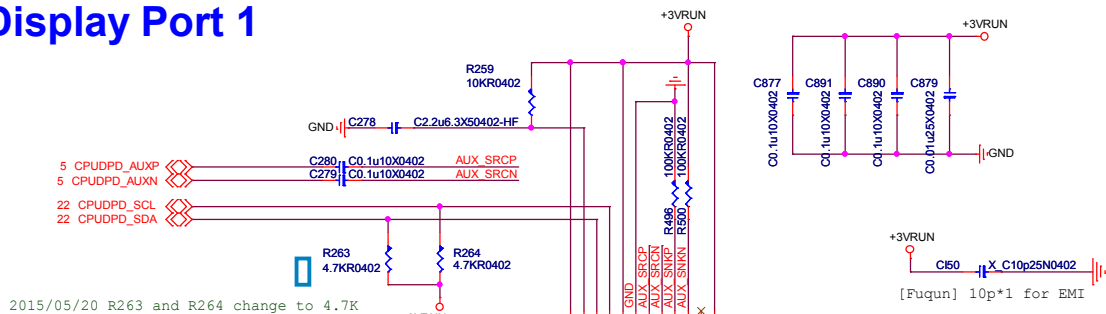
USB3.1 Port 1
iCharger



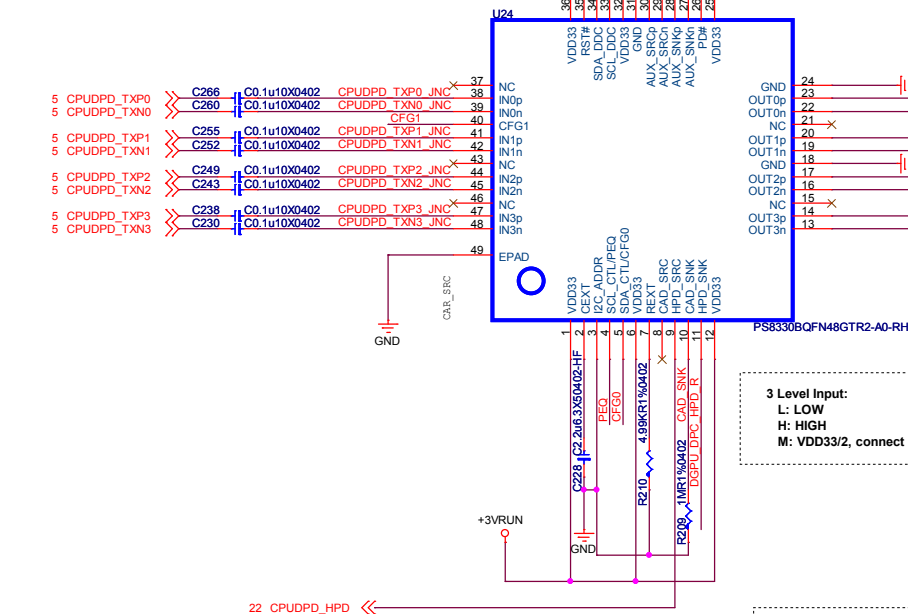
USB3.1 Port 2



Display Port 1

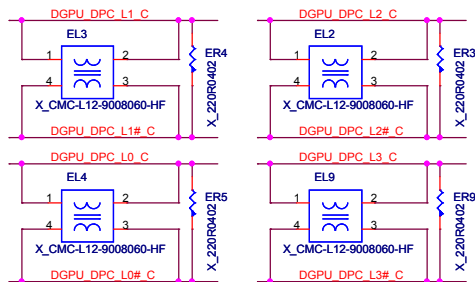


DP1&DP2 3VRUN Change to 3V_DP_PWR for V1.2

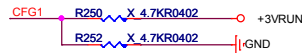
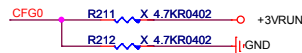


EMI

[Fuqun] EMI chnagne P/N in 0B



3 Level Input:
L: LOW
H: HIGH
M: VDD3/2, connect both pull-up and pull-down resistors

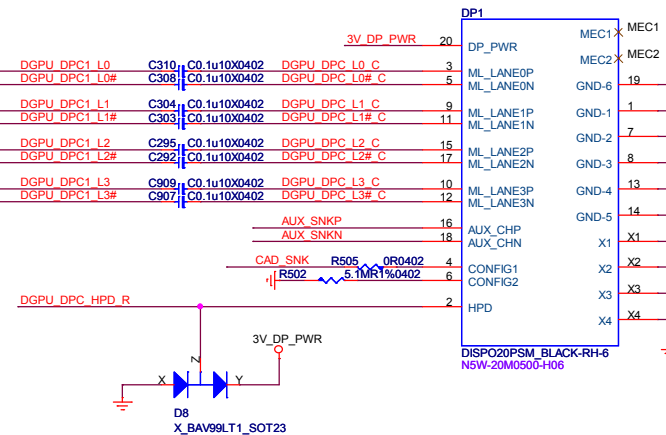


Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

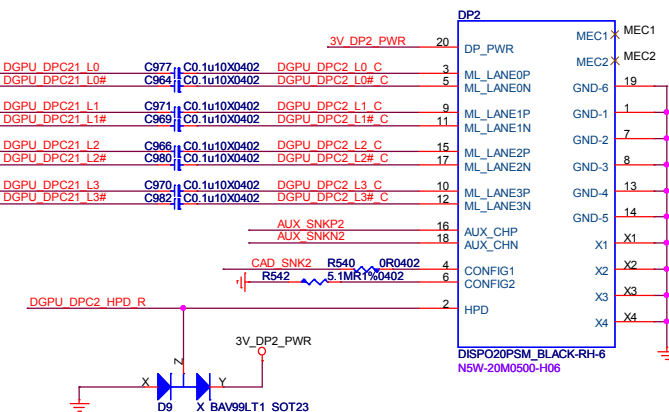
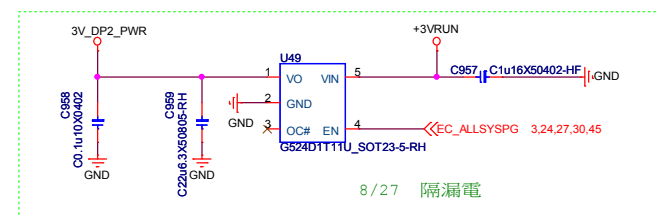
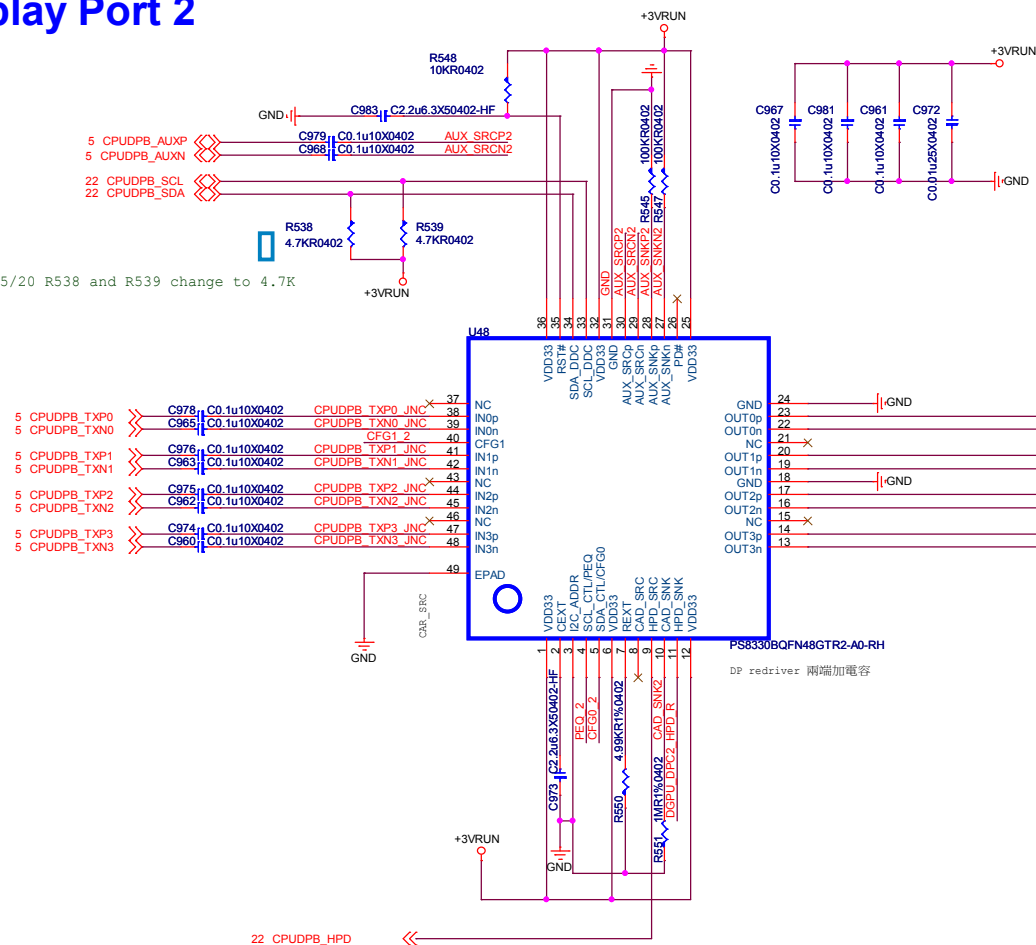
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K Ohm
H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.

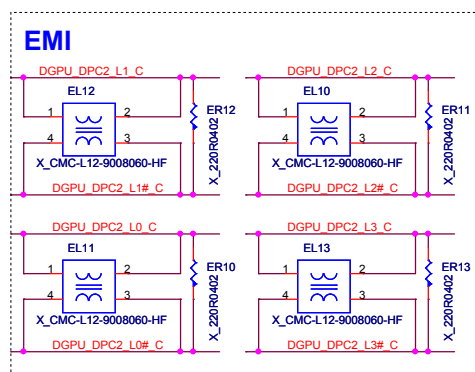
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2



Display Port 2



DP1&DP2 3VRUN Change to 3V DP PWR for 1.2



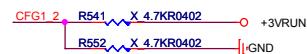
Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k Ohm, 3.3V I/O.

L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing



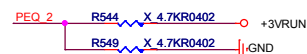
Configuration pin for auto test and input offset cancellation, 3.3V IO,
internal pull up at ~150K Ohm

H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

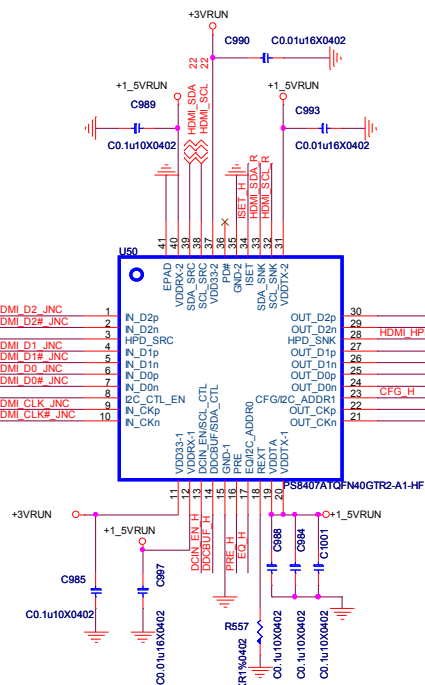


Programmable input equalization levels; Internal pull down at ~150k Ohm, 3.3V I/O.

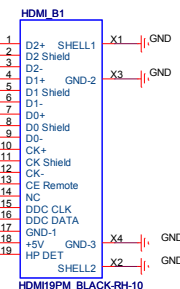
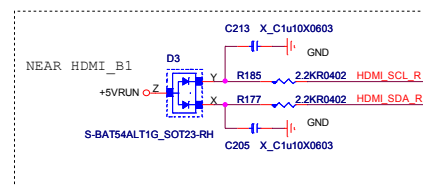
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2



2015/5/26 R566,R567 change to unstuff



[Fuqun] Add debug card function



2015/05/20 Add C804 0.1uF connect to +5VRUN_L

3 Level Input:
L: LOW, internal pull down
H: HIGH, external pull up
M: VDD3/2, both external pull-up and pull-down

Configuration pin, 3.3V IO, internal pull down at ~150k Ohm, 3.3V I/O.
L: HDMI ID disable
H: HDMI ID enable

Receiver equalization setting; Internal pull down at ~150k Ohm, 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB
H: programmable EQ for channel loss up to 4.3dB
M: programmable EQ for channel loss up to 8.6dB

TMDS output swing adjustment; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default
H: increase +13%
M: reduce -13%

DC coupling enable; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, AC coupling input
H: DC coupling input

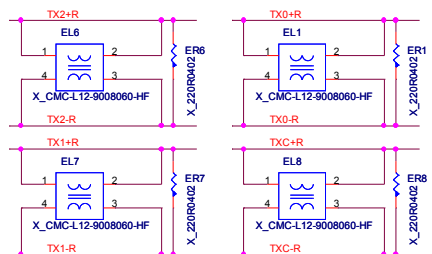
Enable active DDC buffer; Internal pull down at ~150k Ohm, 3.3V I/O.
L: default, passive DDC pass-through
H: active DDC buffer with default threshold
M: active DDC buffer without internal pull up resistor

Output pre-emphasis setting; Internal pull down at ~150k Ohm, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis

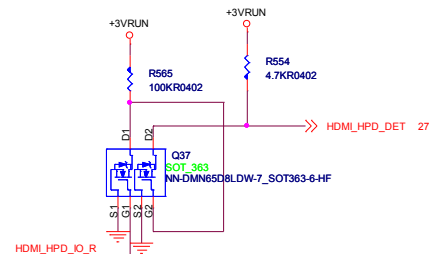
2015/05/20 R560 change to unstuff

EMI

[Fuqun] EMI chnagne P/N in 0B

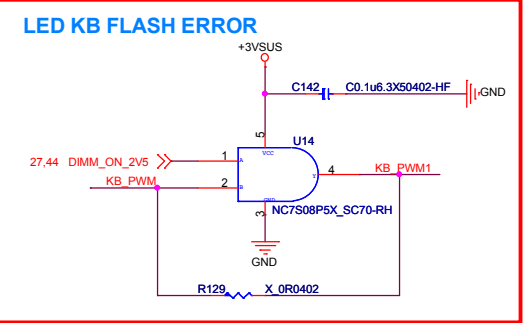
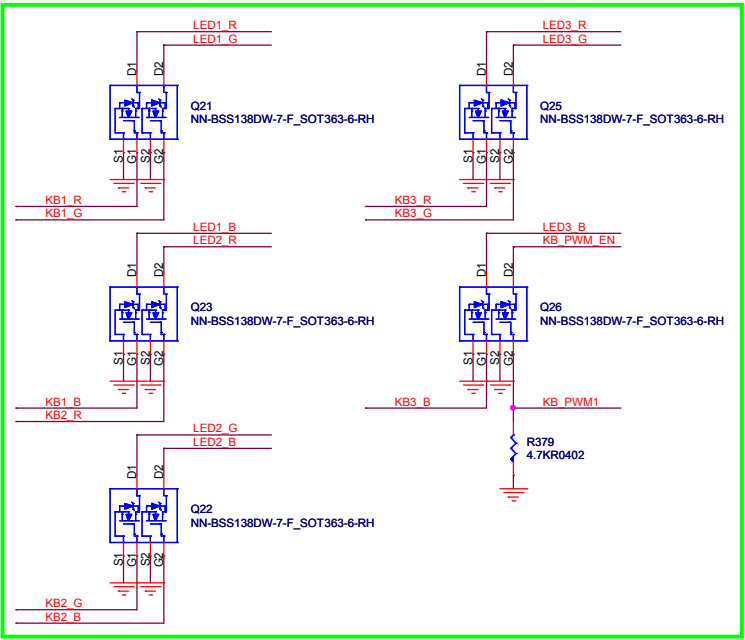
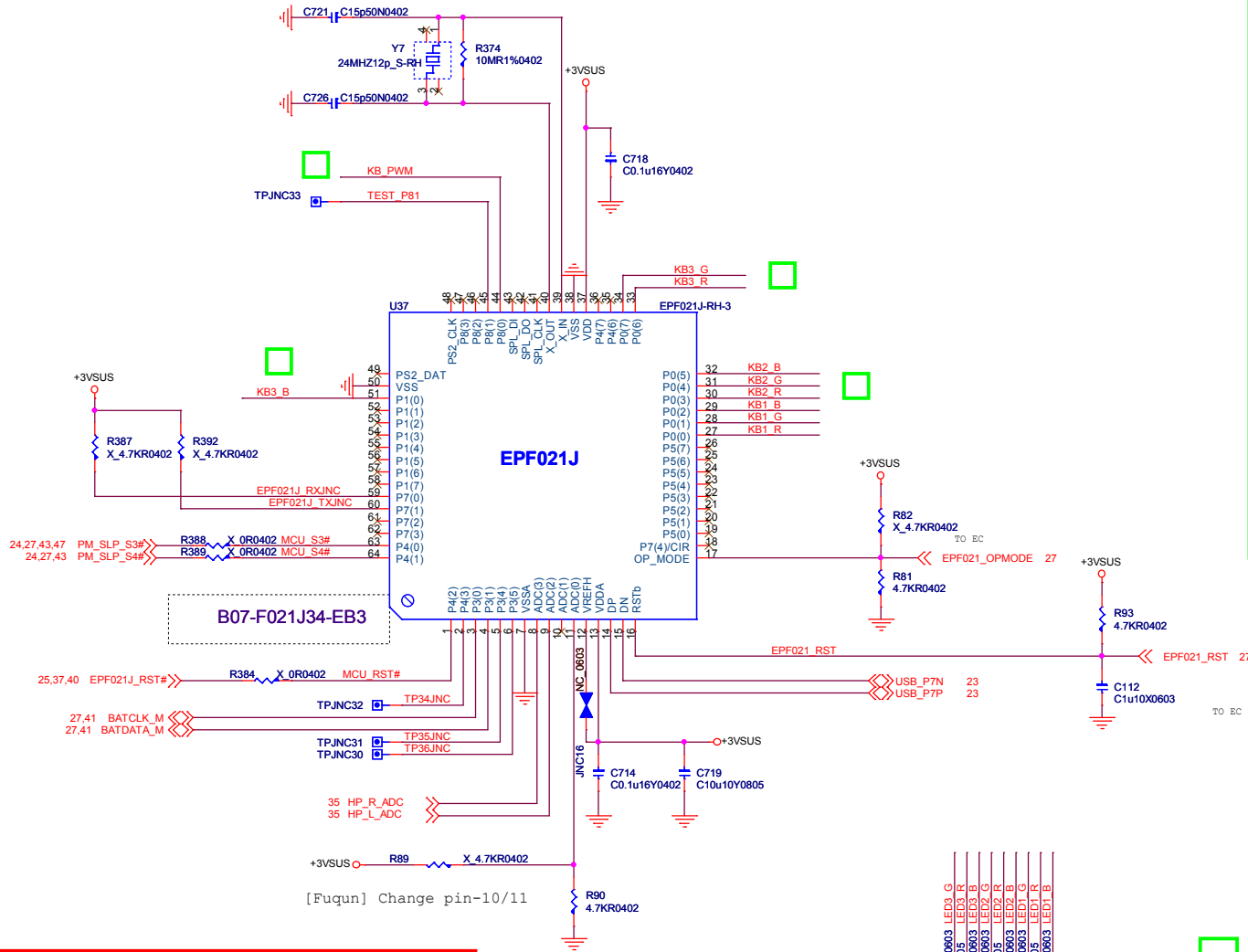


HPD Level Shift 5V to 3V

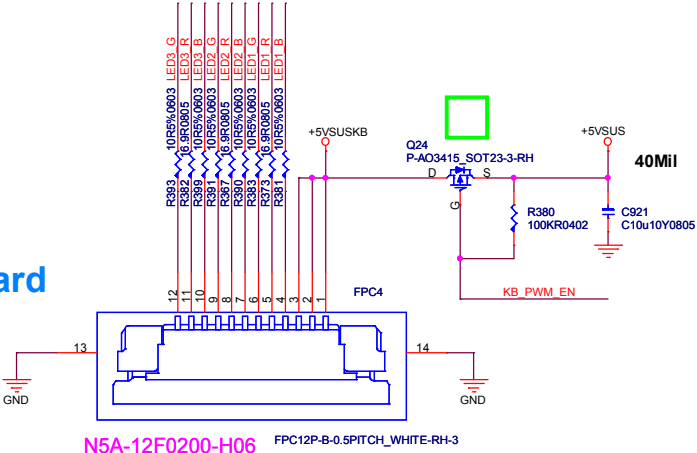


For debug card

LED 8051 Controller

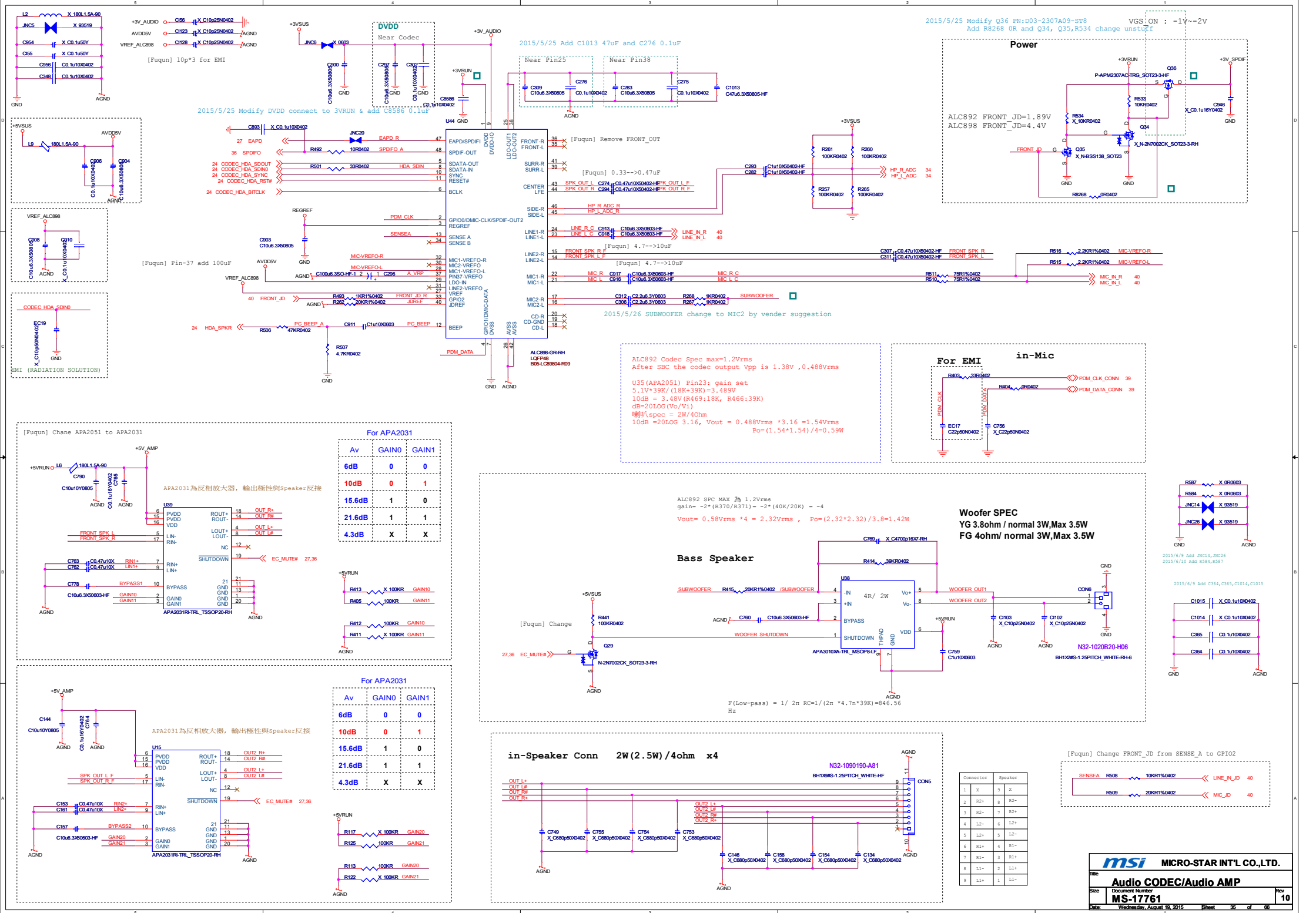


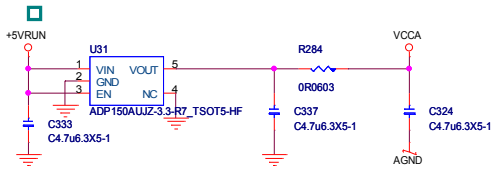
LED Keyboard



LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

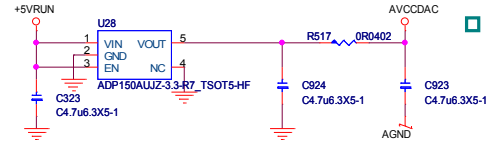
PIN1 要接 CON 的 PIN1





DIGITAL

ANALOG

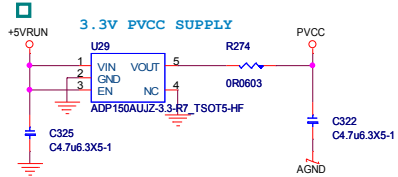
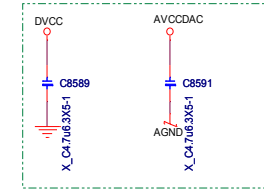


DIGITAL

ANALOG

2015/6/9 Delete C8590 and C8589, C8591 change to unstuff

Near Chip



DIGITAL

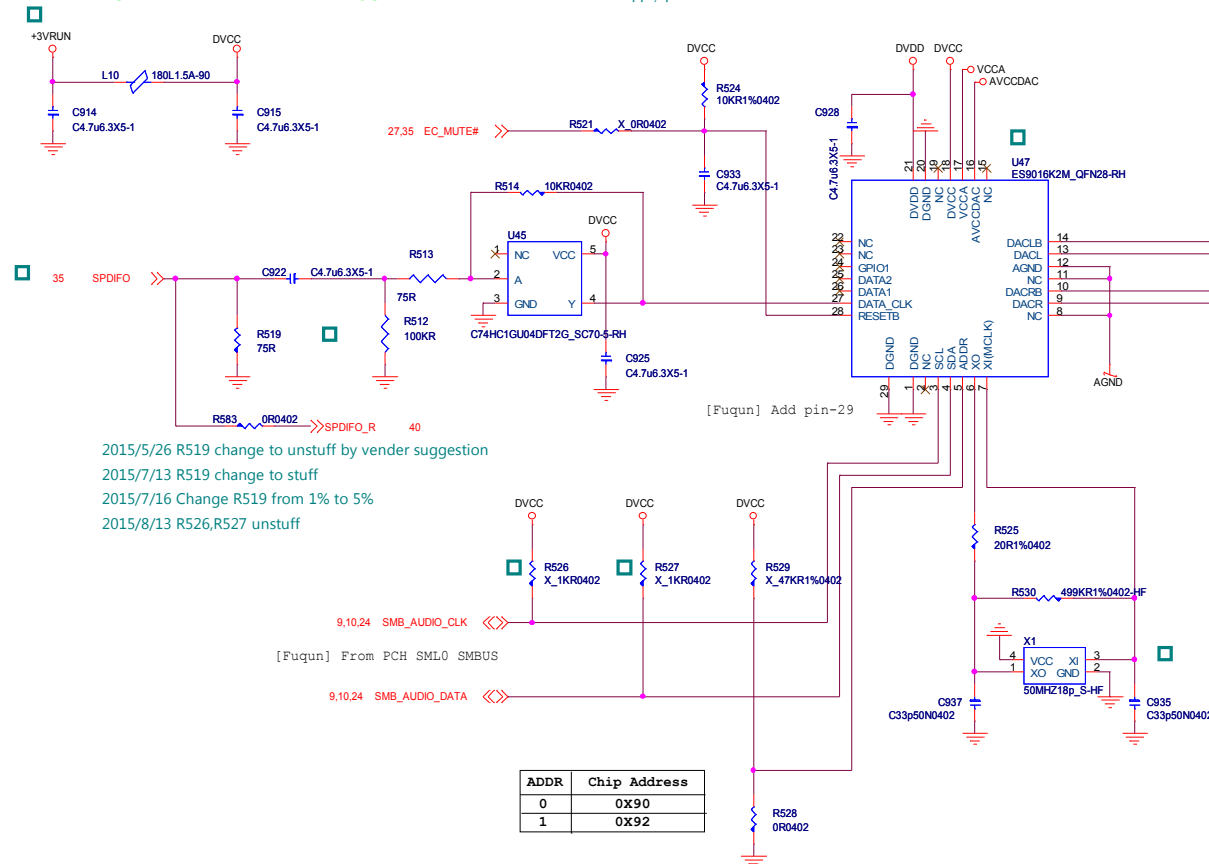
ANALOG

2015/5/26 R524,C933 change to stuff and R521 change to unstuff on EC_MUTE#
The internal DVDD supply powered from VCCA

2015/6/5 Delete U3009,R584, R488,C1014

AVCCDAC power must supply to be very low-noise

2015/6/12 Change C317 PN C11-2257523-W08



2015/5/26 R519 change to unstuff by vender suggestion

2015/7/13 R519 change to stuff

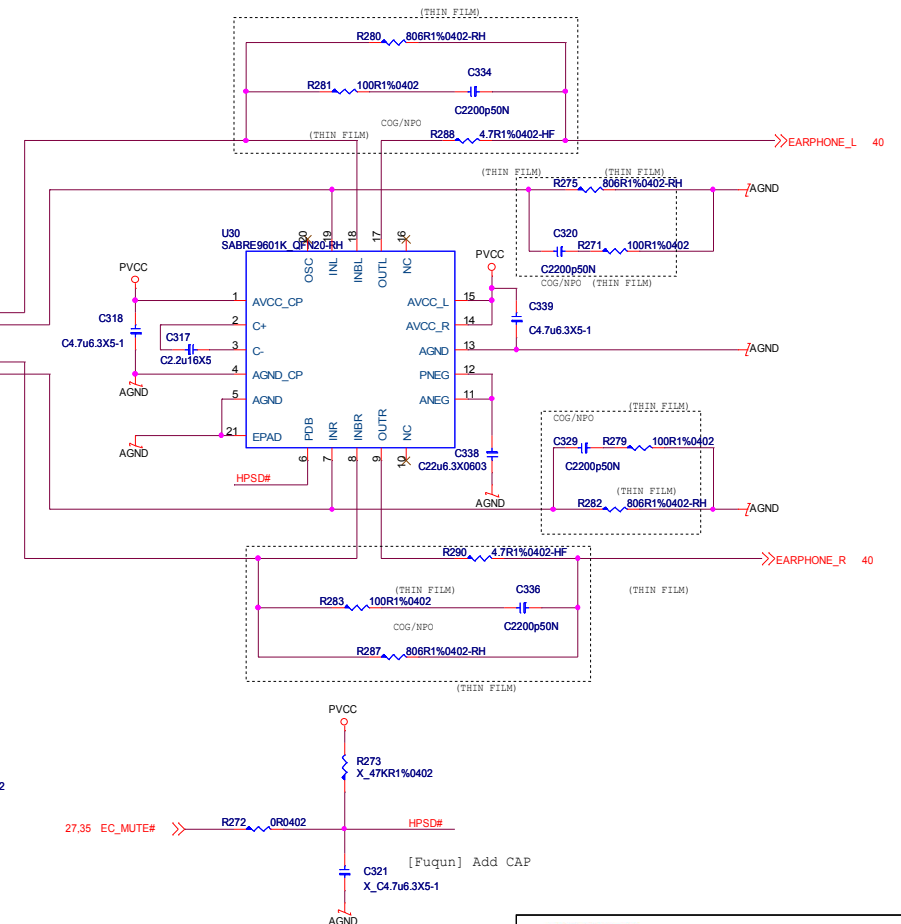
2015/7/16 Change R519 from 1% to 5%

2015/8/13 R526,R527 unstuff

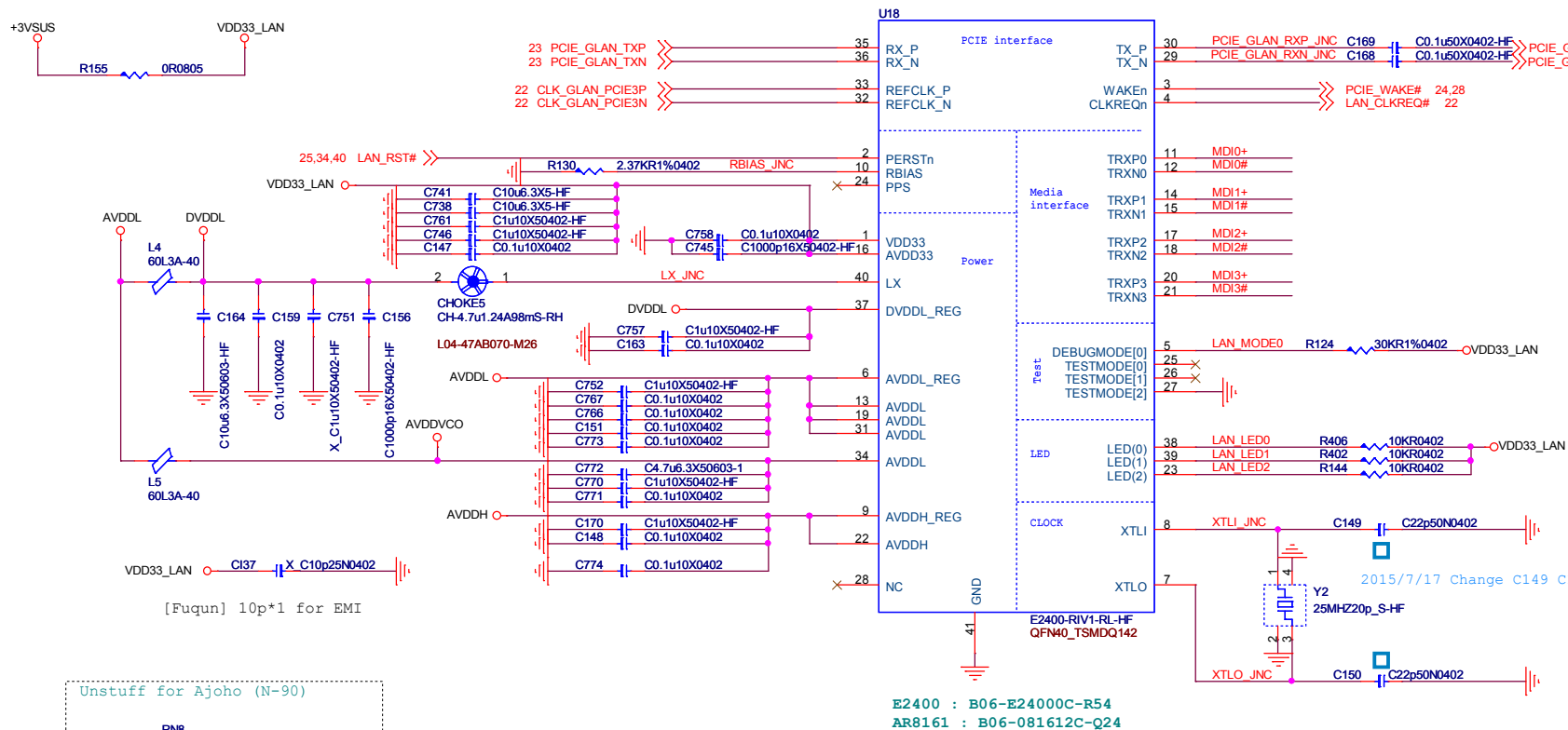
[Fuqun] From PCH SMI0 SMBUS

ADDR	Chip Address
0	0X90
1	0X92

LIN DIFF ANALOG



LAN Killer E2400/AR8161

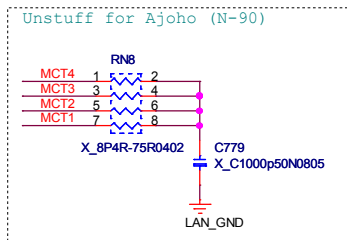


```
LED1:
SWR-----HIGH
LDO-----LOW
The chip have internal pull-up
```


```
LED2:
25MHz-----HIGH
48MHz-----LOW
The chip have internal pull-up
```

2015/7/17 Change C149 C150 from 20pF to 22pF for SA

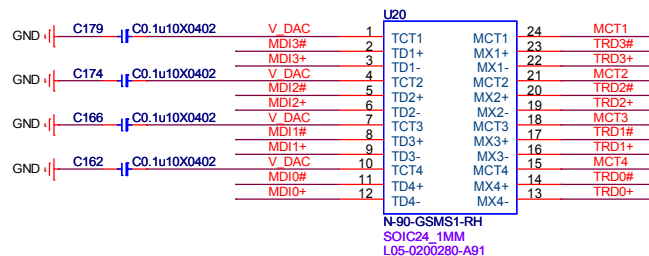
E2400 : B06-E24000C-R54
AR8161 : B06-081612C-Q24



R416 stuff for Ajoho (N-90) 

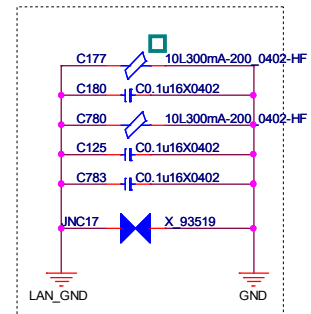
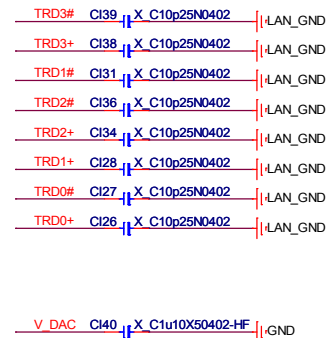
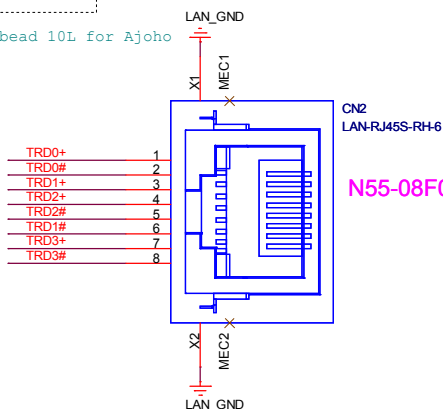


2015/6/17 Change R416 from 0R to bead 10L for Ajoho

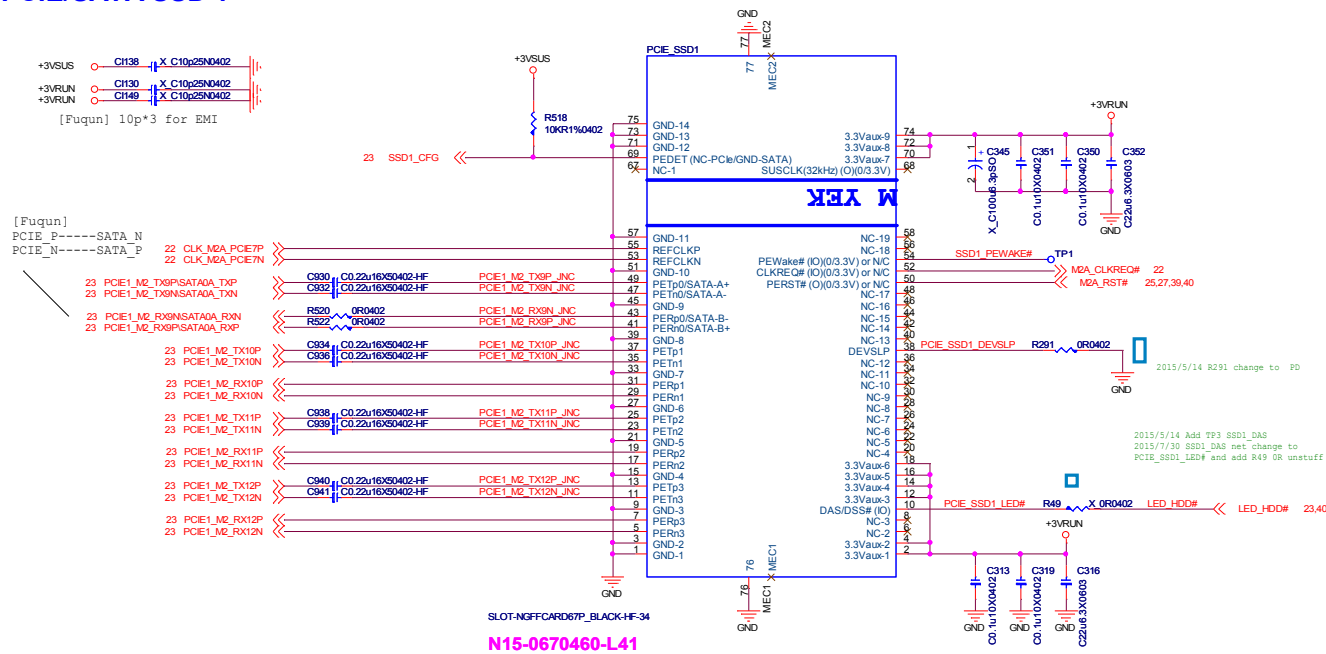


Footprint 用傳統transformer的SOIC24 1MM

BOTHHAND(GST5009-V LF) L05-0200150-B09
 AJOHO(N-90) L05-0200280-A91

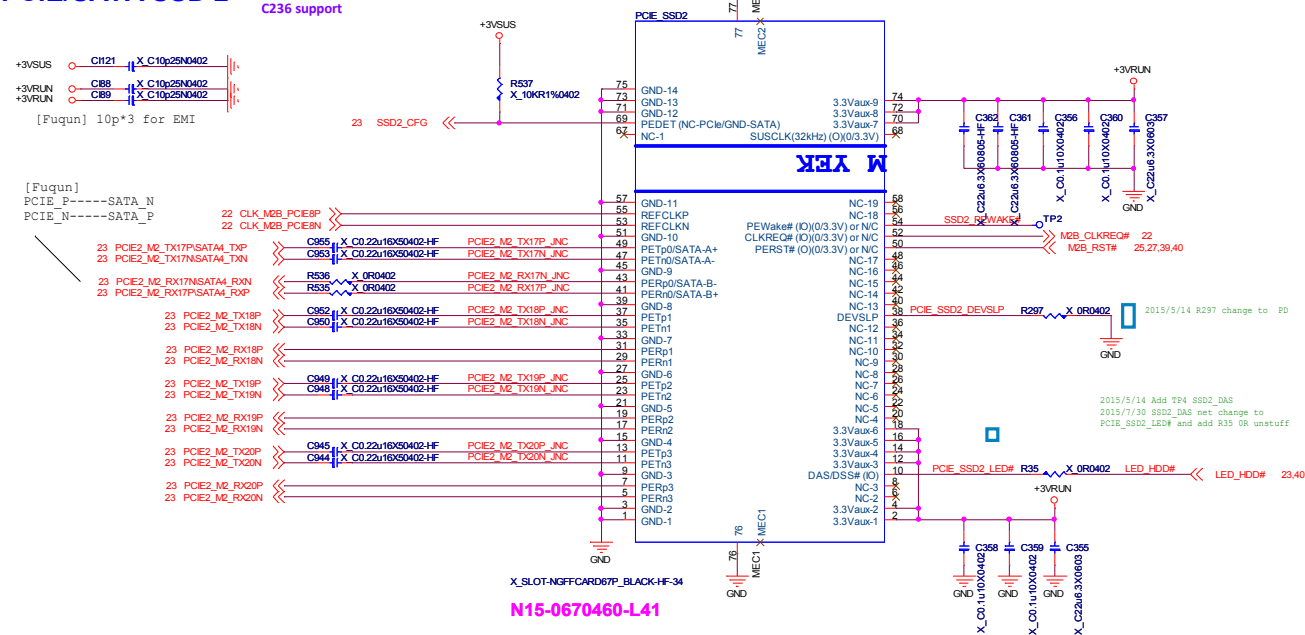


PCIe/SATA SSD 1




PCIe/SATA SSD 2

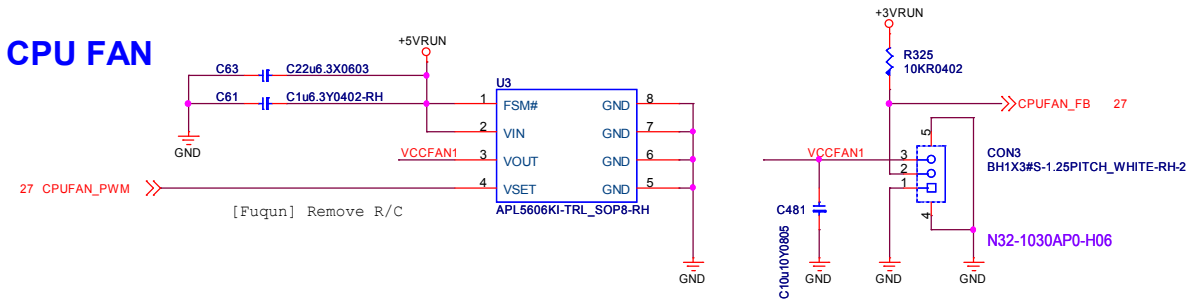
HM170 not support
C236 support



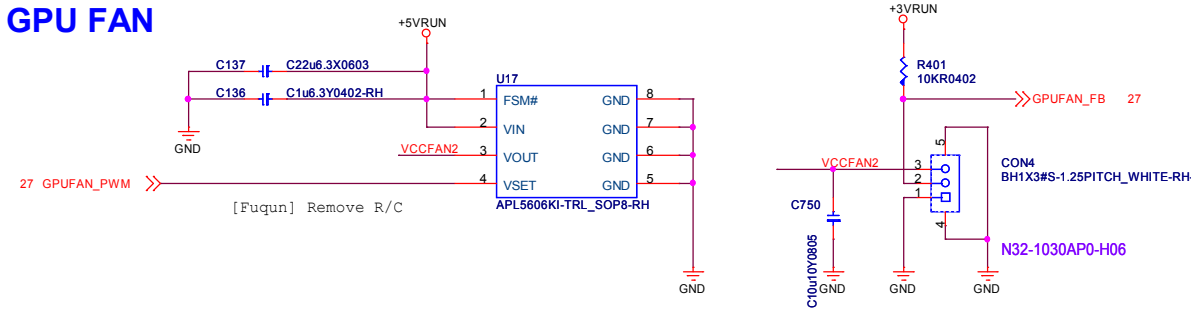
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

 MICRO-STAR INT'L CO.,LTD.	
Title	
SSD(PCIE/SATA)	
Size	Document Number MS-17761
Date	Thursday, August 20, 2015
Sheet	38 of 66
Rev	10

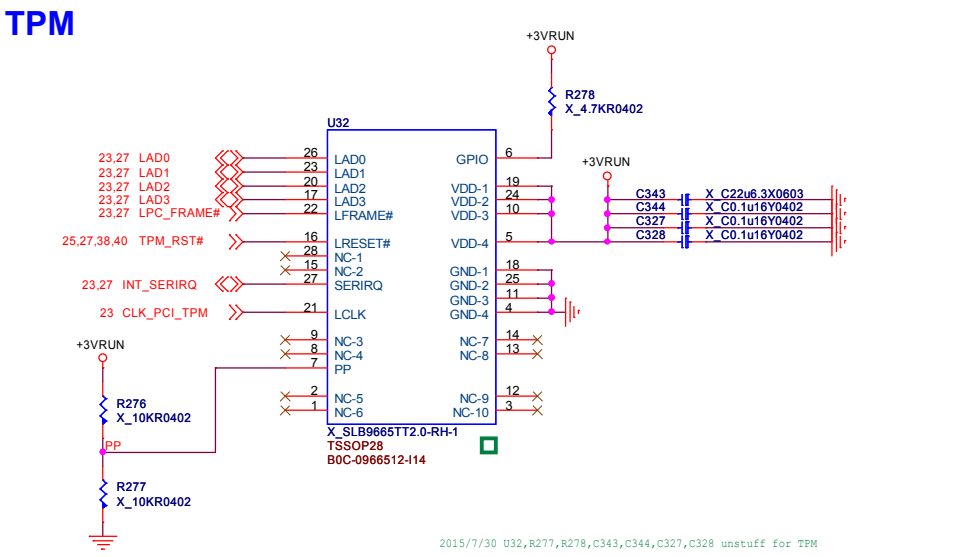
CPU FAN



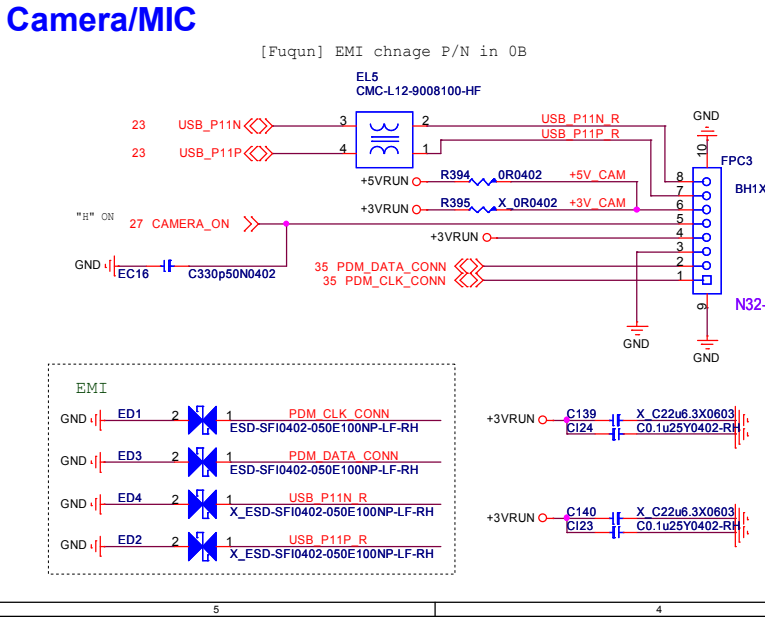
GPU FAN



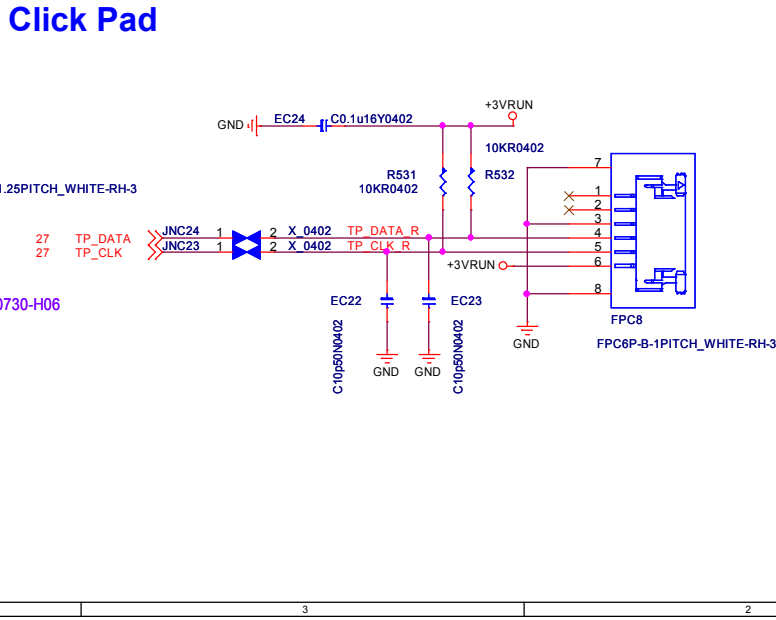
TPM



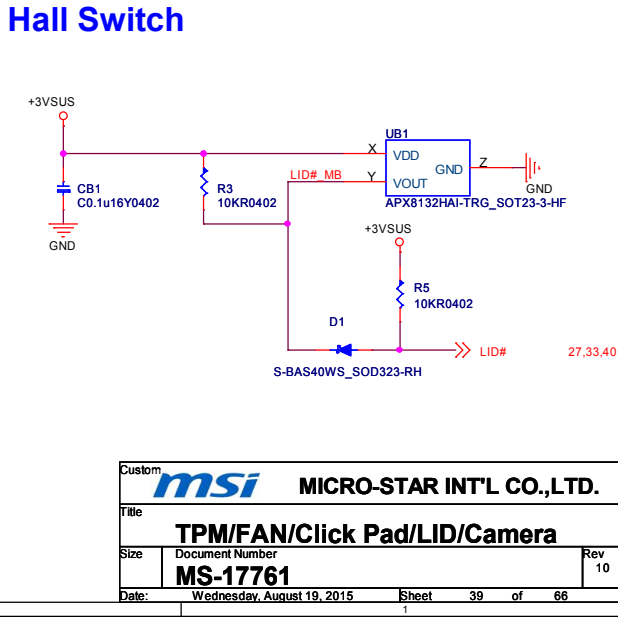
Camera/MIC



Click Pad

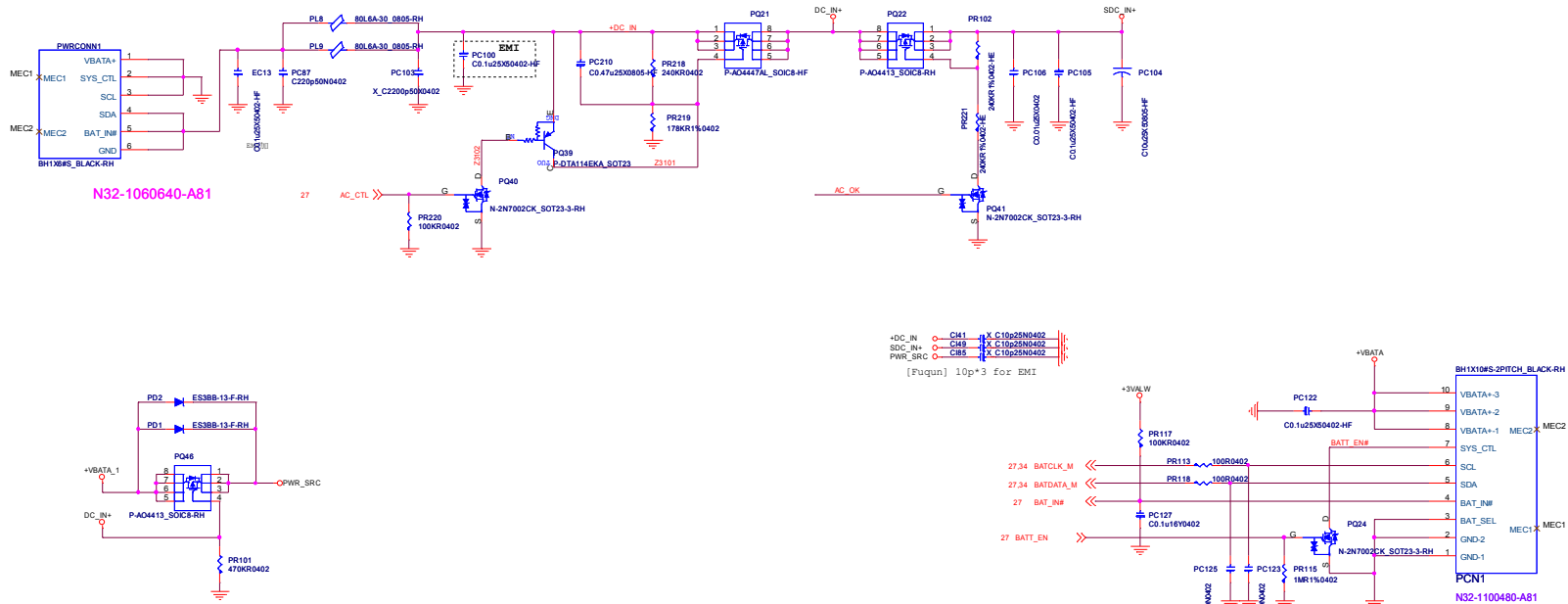


Hall Switch

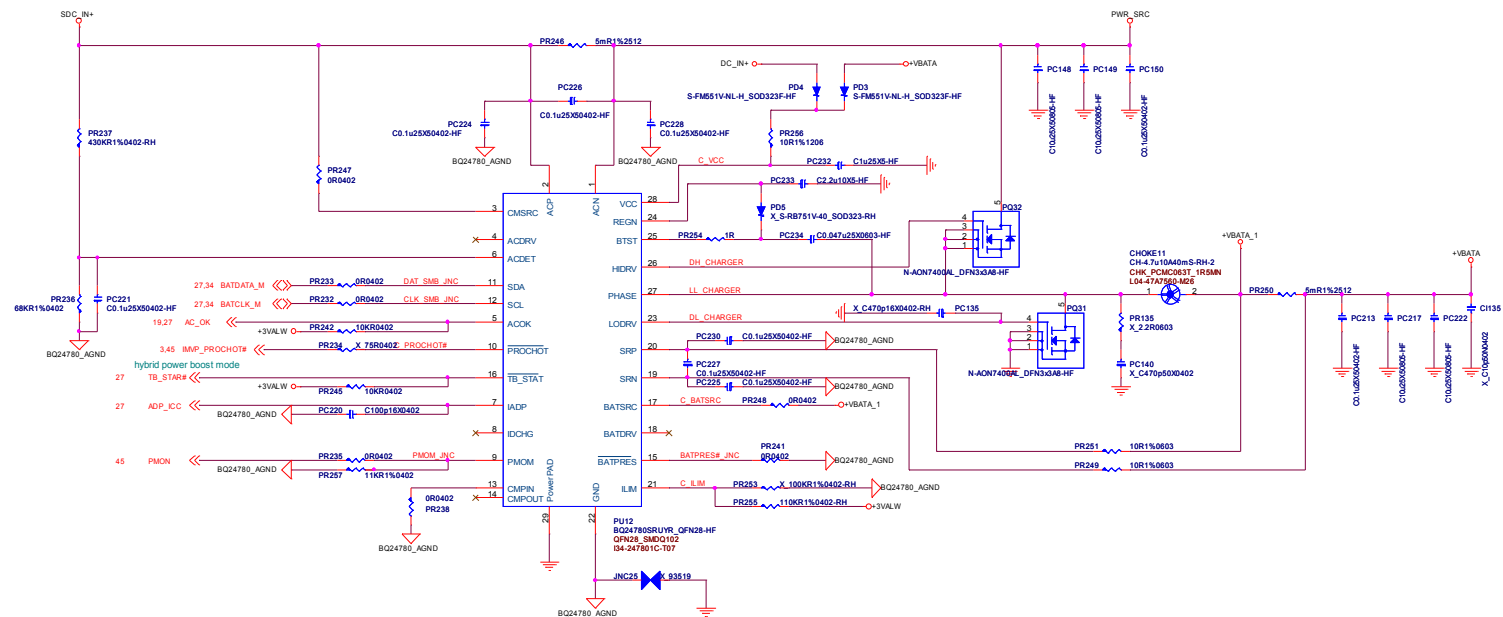


Custom		msi MICRO-STAR INT'L CO.,LTD.	
Title		TPM/FAN/Click Pad/LID/Camera	
Size		Document Number	Rev
		MS-17761	10
Date:		Wednesday, August 19, 2015	Sheet 39 of 66

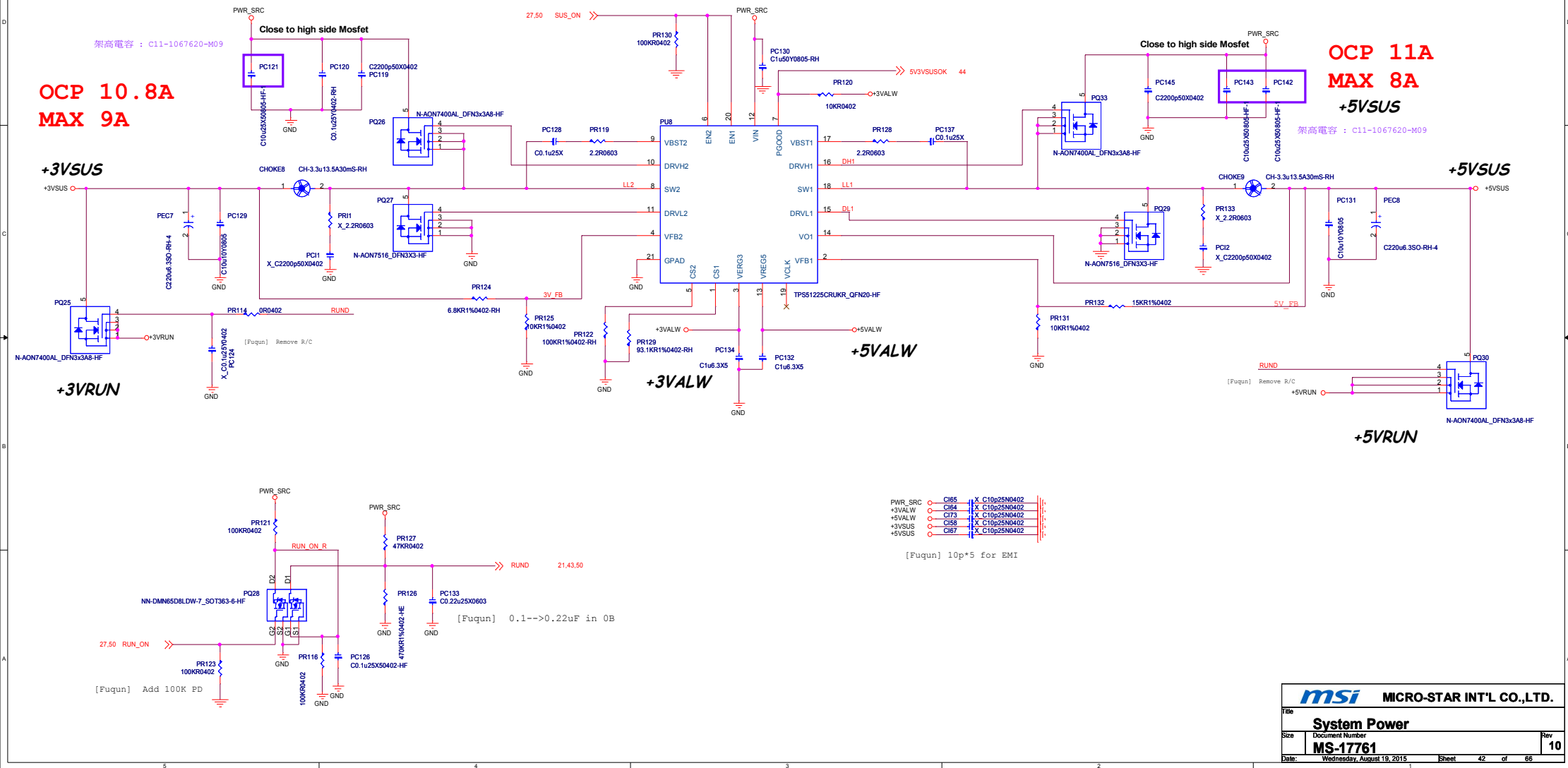
Battery Select



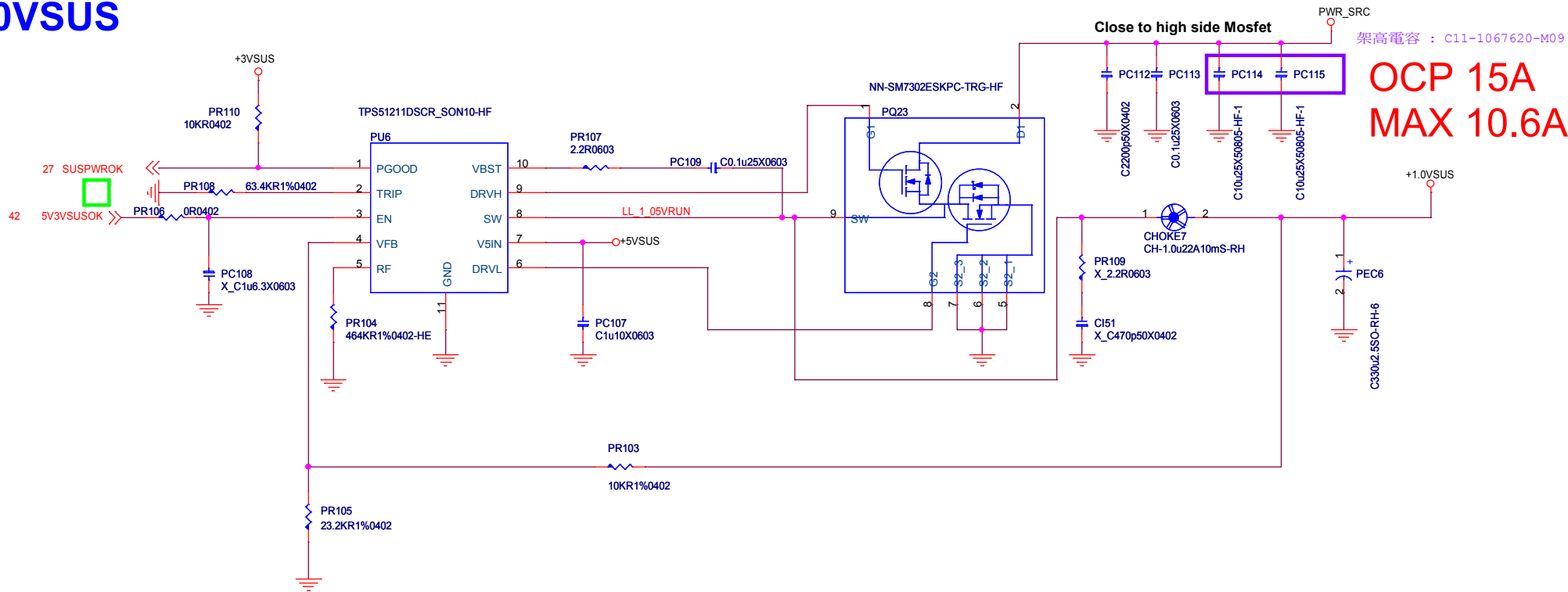
Battery Charger



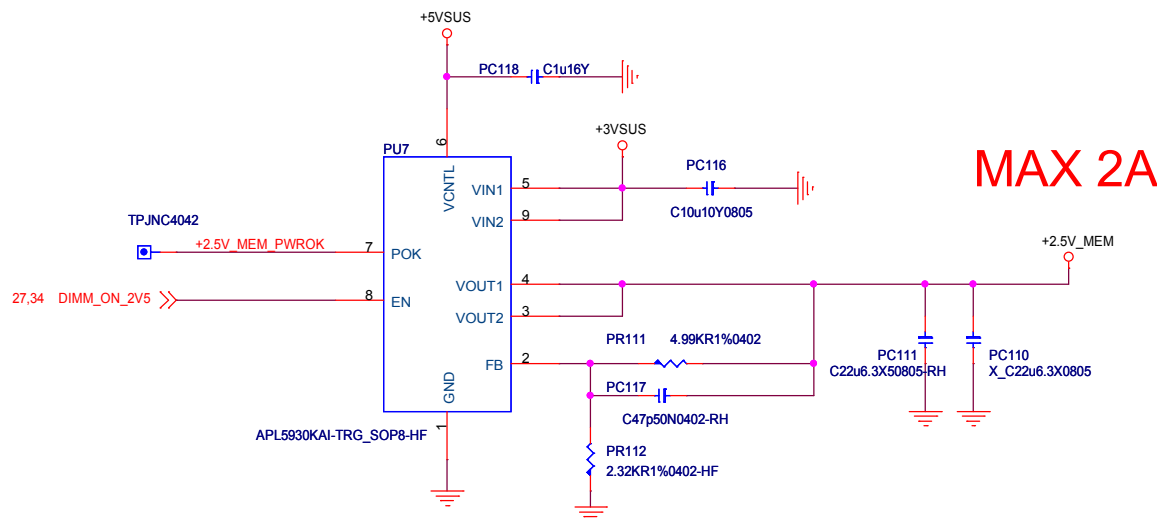
System Power



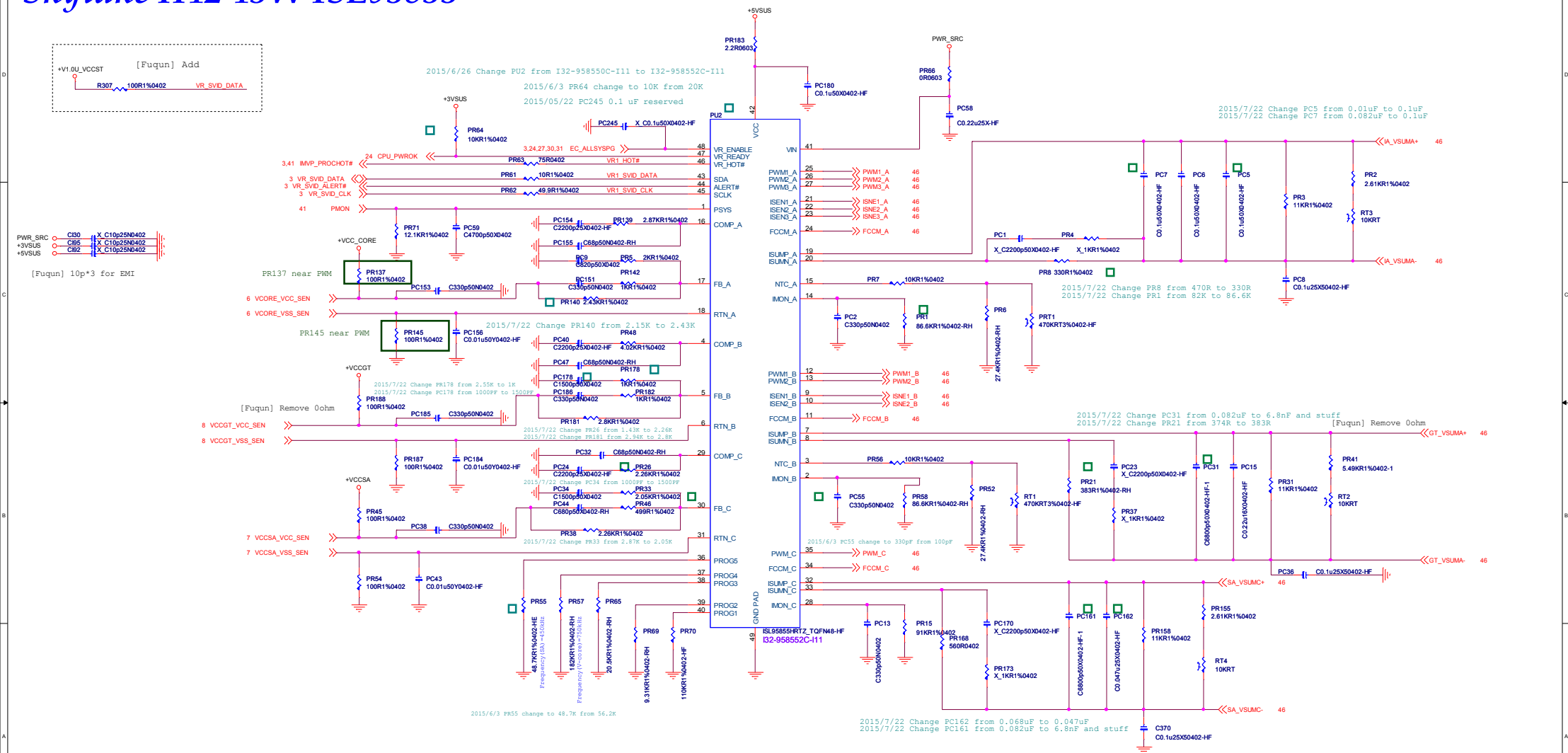
+1.0VSUS



+V2_5U_MEM



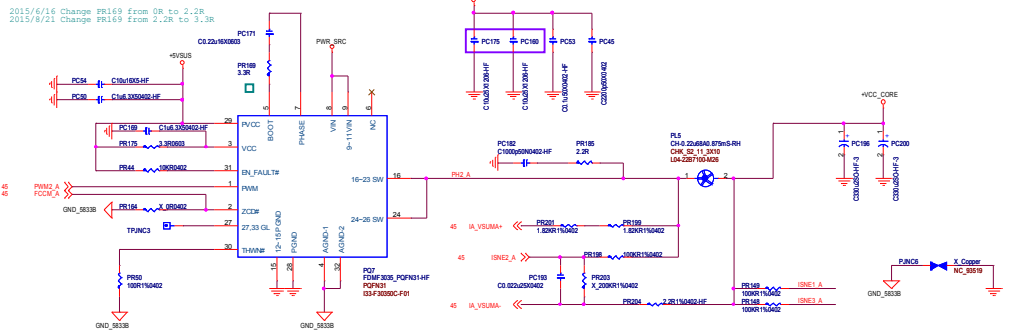
Skylake H42 45W ISL95855



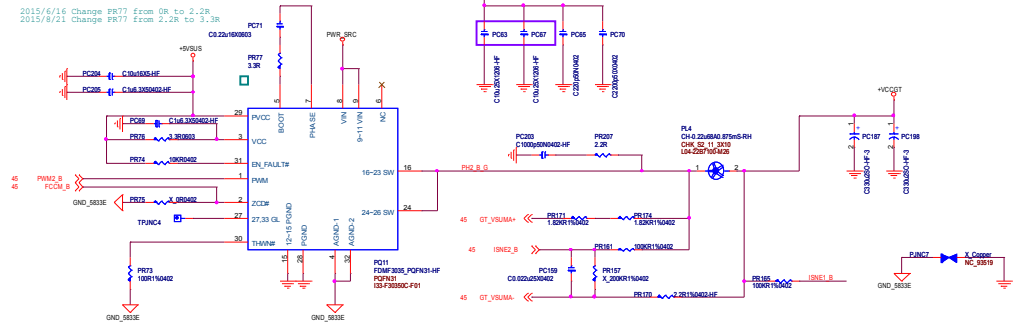
[Fuqun] 10uF:C0603-->C0402 for layout

[Fuqun] 10uF:C0603-->C0402 for layout

2015/6/16 Change PR29 from 0R to 2.2R

2015/6/16 Change PR25 from 0R to 2.2
2015/6/16 Change PR26 from 2.2R to 2.2

2015/8/21 Change PR25 from 2.2K to 3



+VCCSA

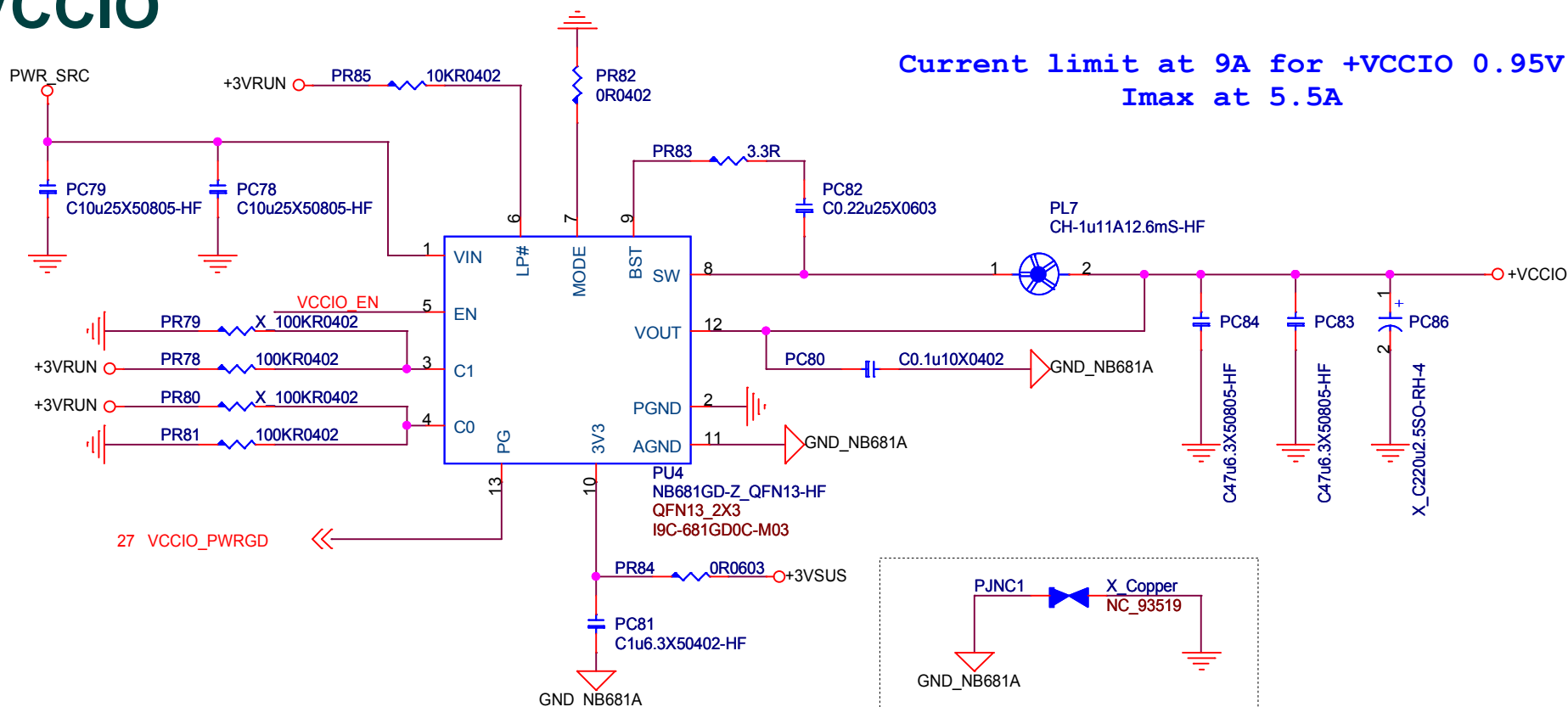
2015/6/16 Change FR10 from 0R to 2.2R

胡嘉雷容：C11-1067610-M09



+VCCIO

Current limit at 9A for +VCCIO 0.95V
I_{max} at 5.5A



2015/6/2 Delete R75, C104,C106,U11 AND gate

[Fuqun] C135 Change 0.1uF to 0.47uF in 0B

2015/5/27 Delete R121 and add U25 AND gate,C108 for tCPU28a power down sequence
2015/6/3 R86 change to 0R and C135 unstuff

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Title

+VCCIO

Size

Document Number

MS-17761

Rev

10

Date:

Wednesday, August 19, 2015

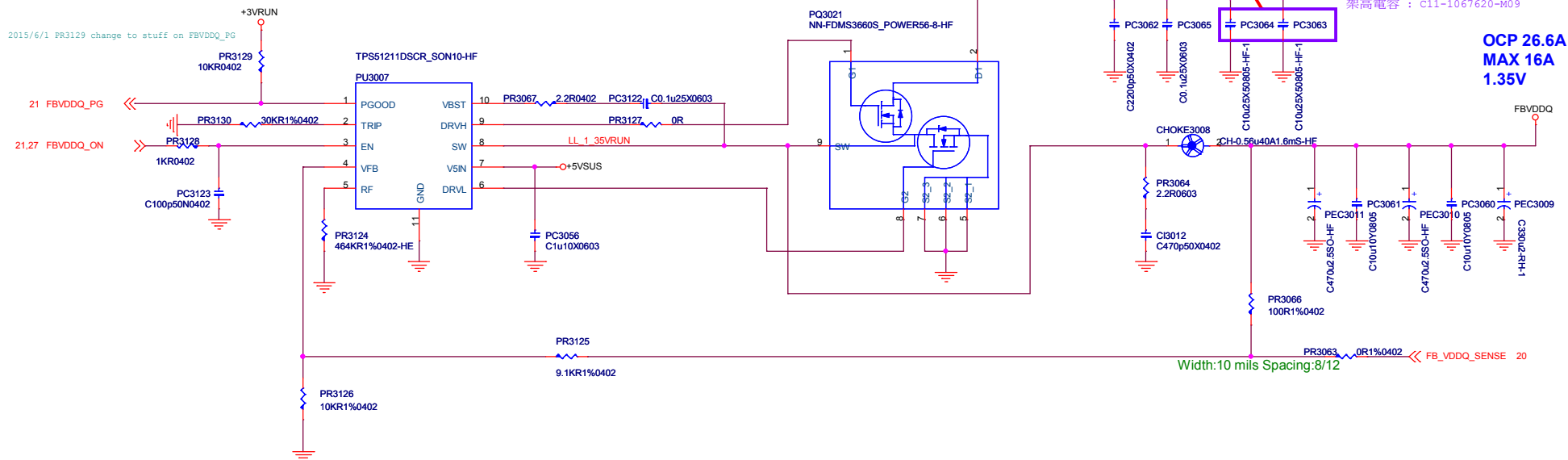
Sheet

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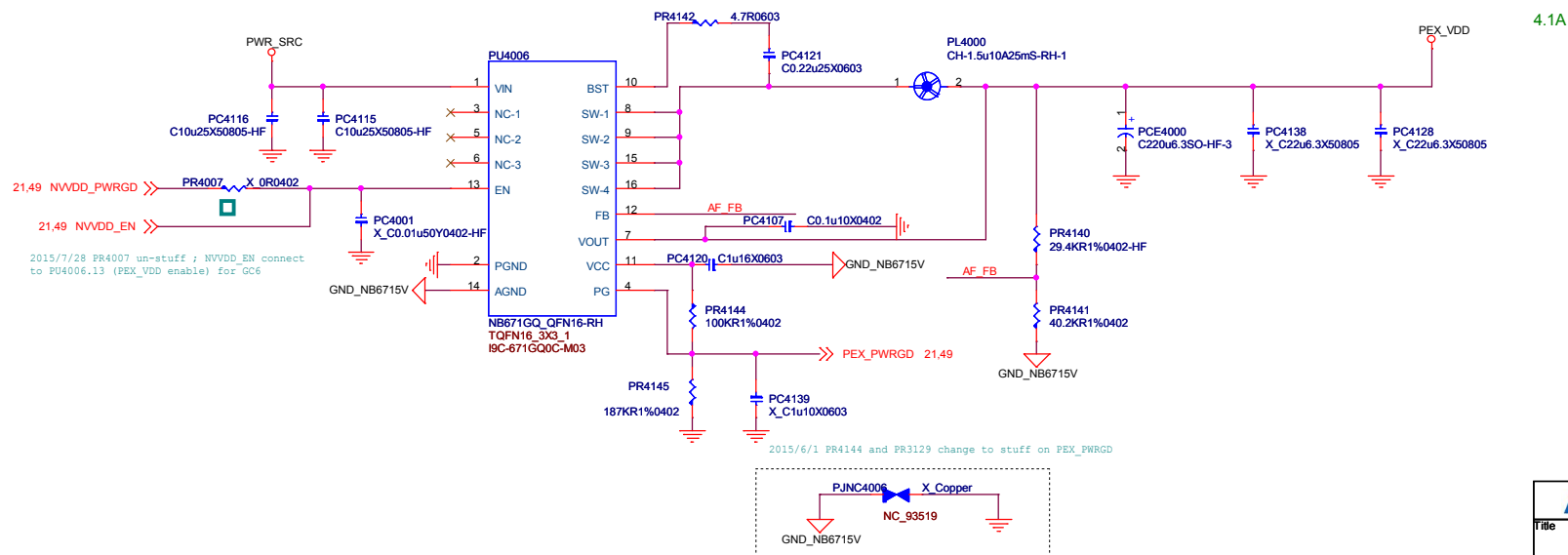
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66

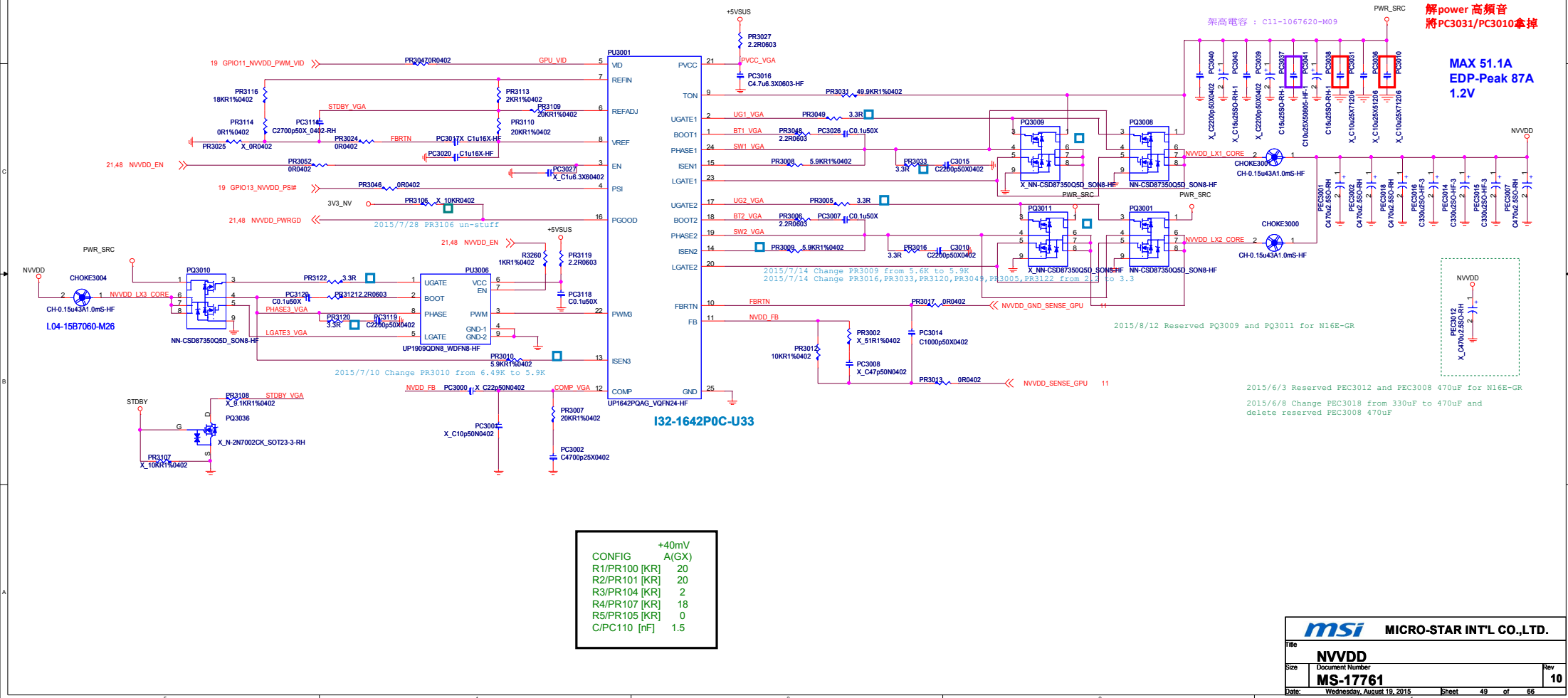
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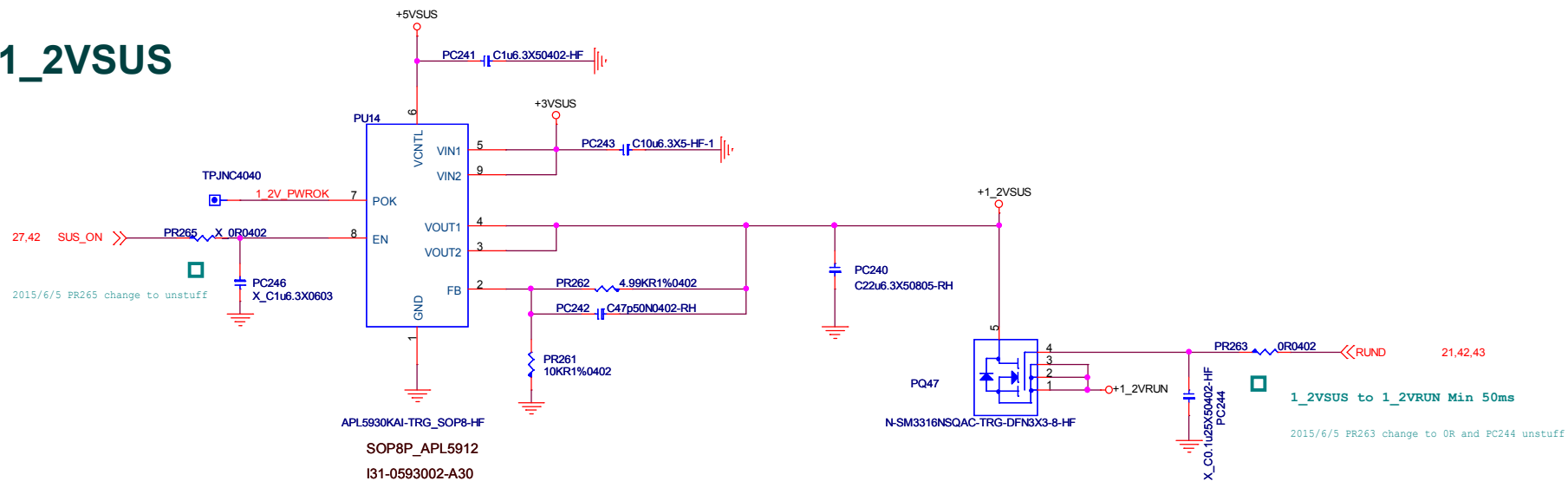
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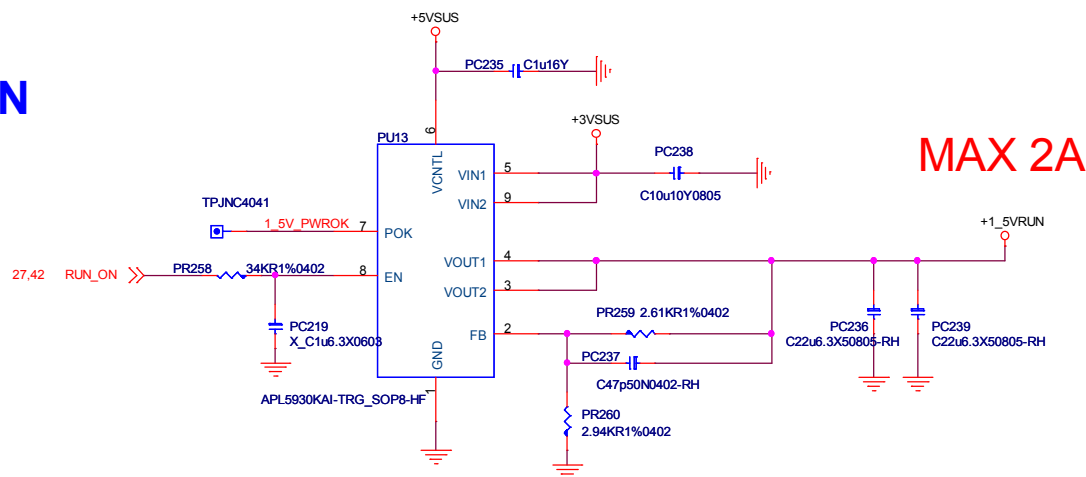
CONFIG B for N16P-GX



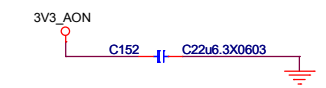
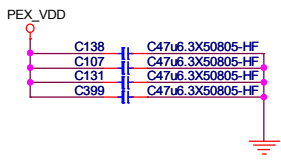
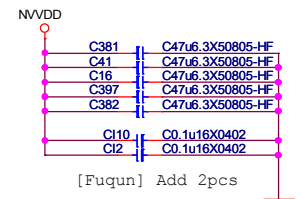
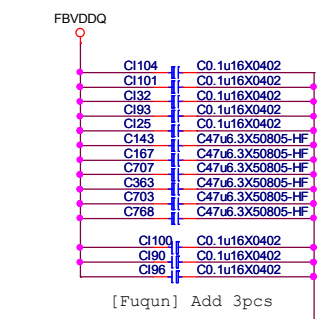
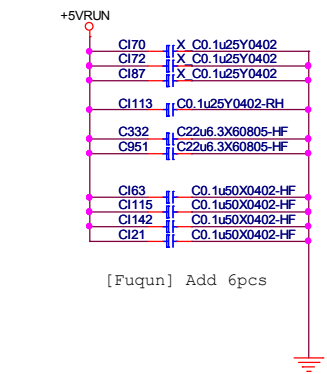
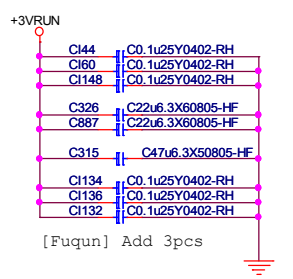
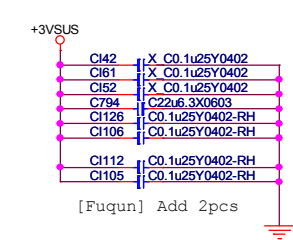
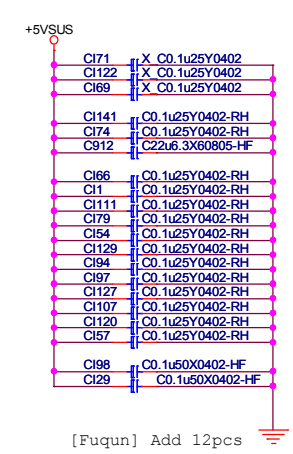
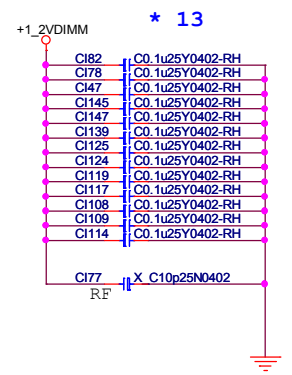
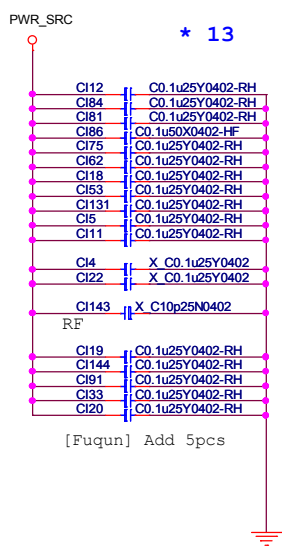
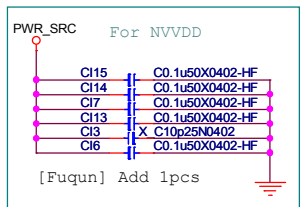
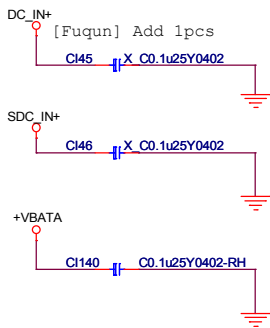
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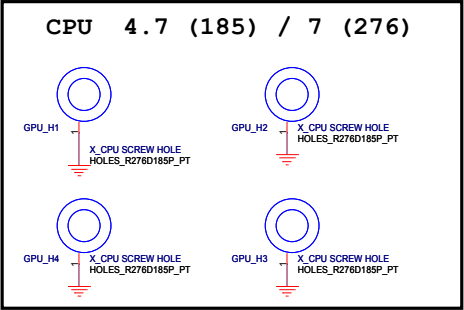
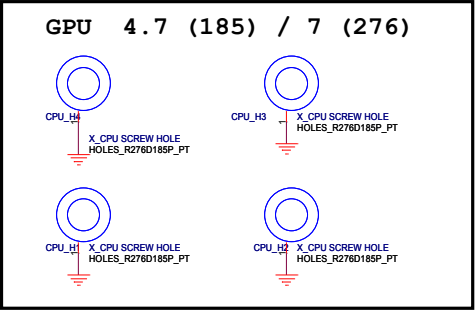
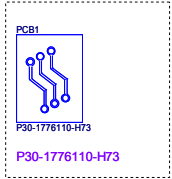
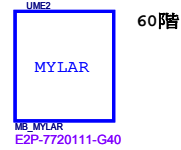
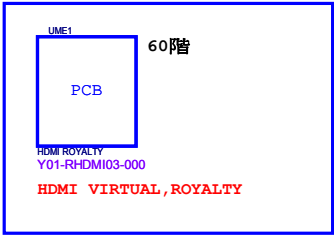
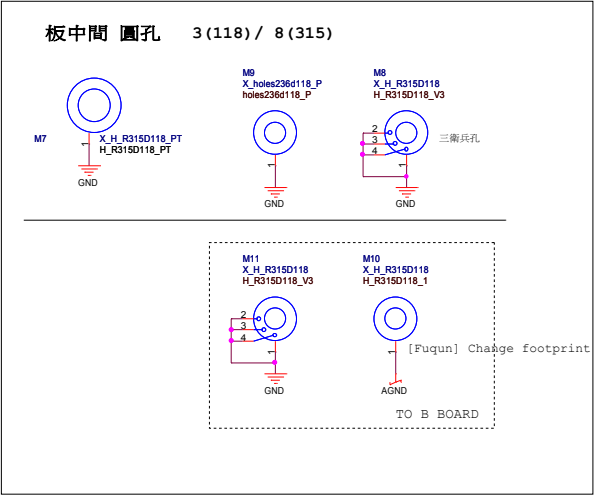
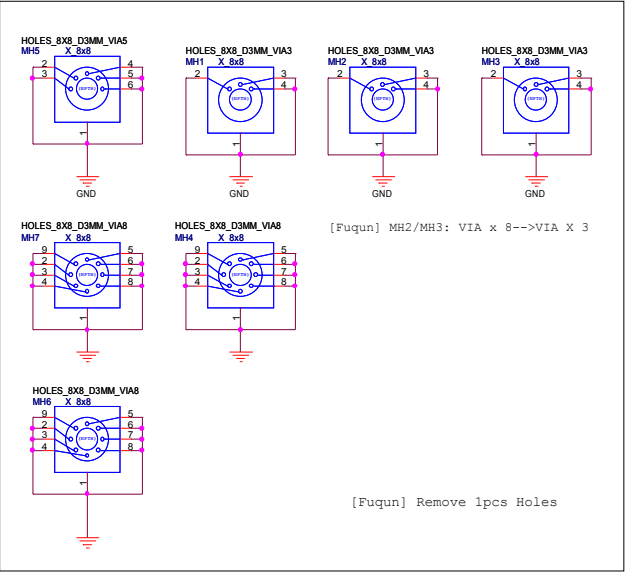
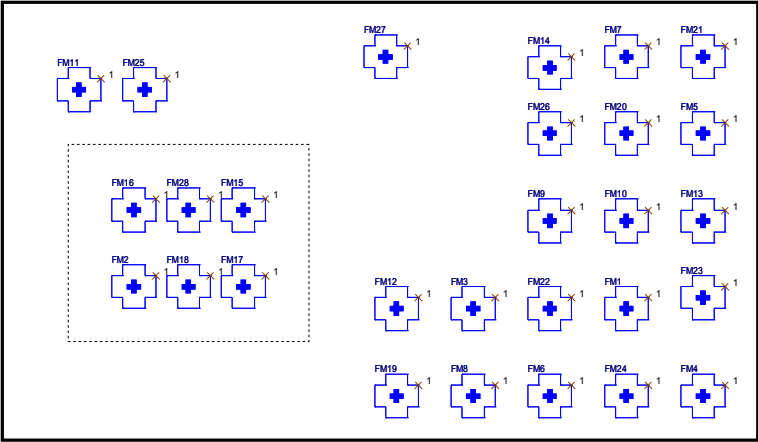
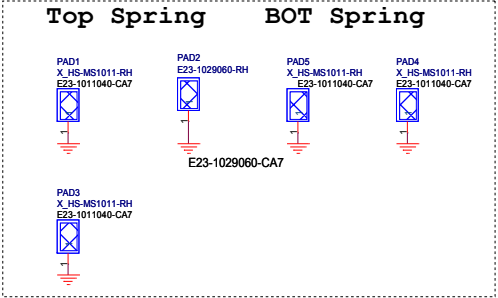
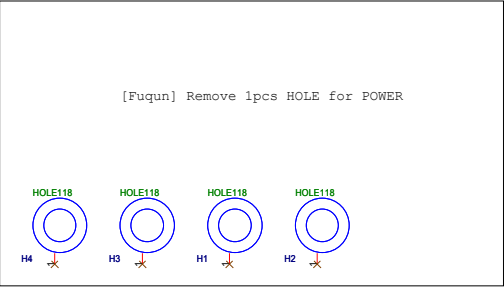


+1.5VRUN

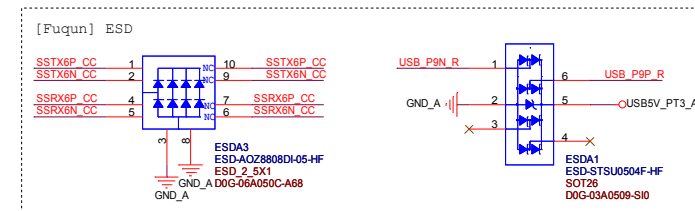
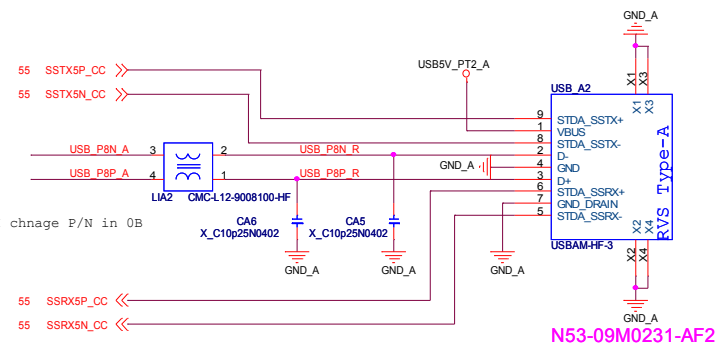
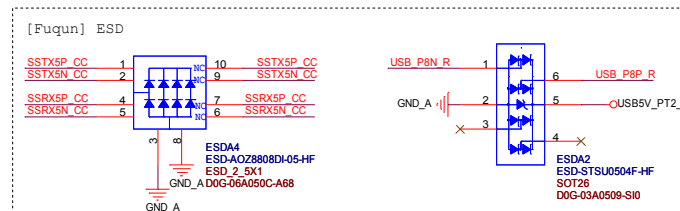
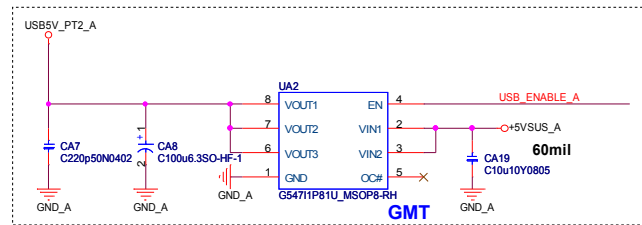


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Title	
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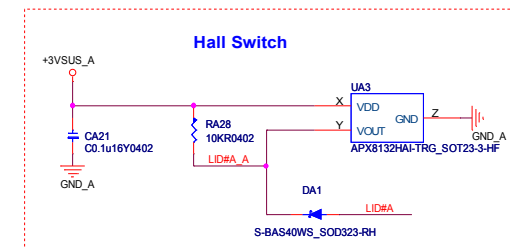
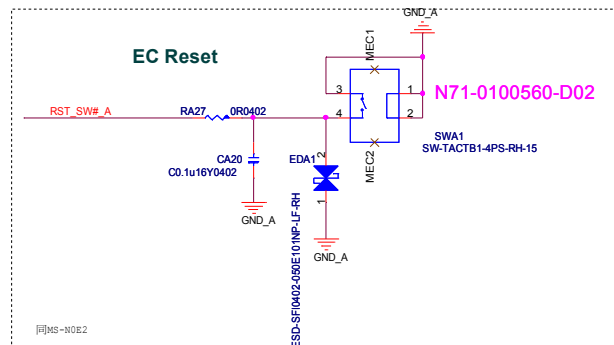
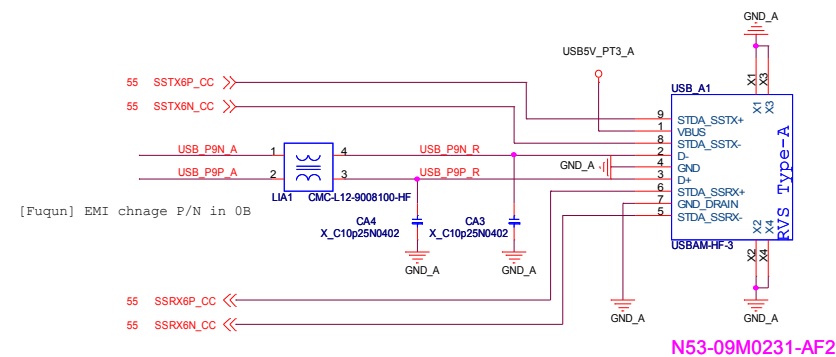
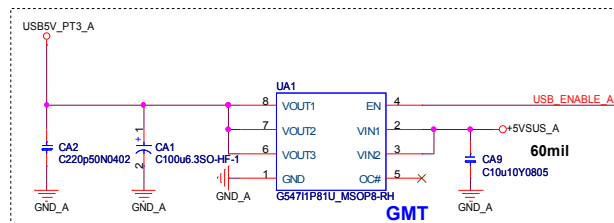




USB3.0 CNT Port 3



USB3.0 CNT Port 4



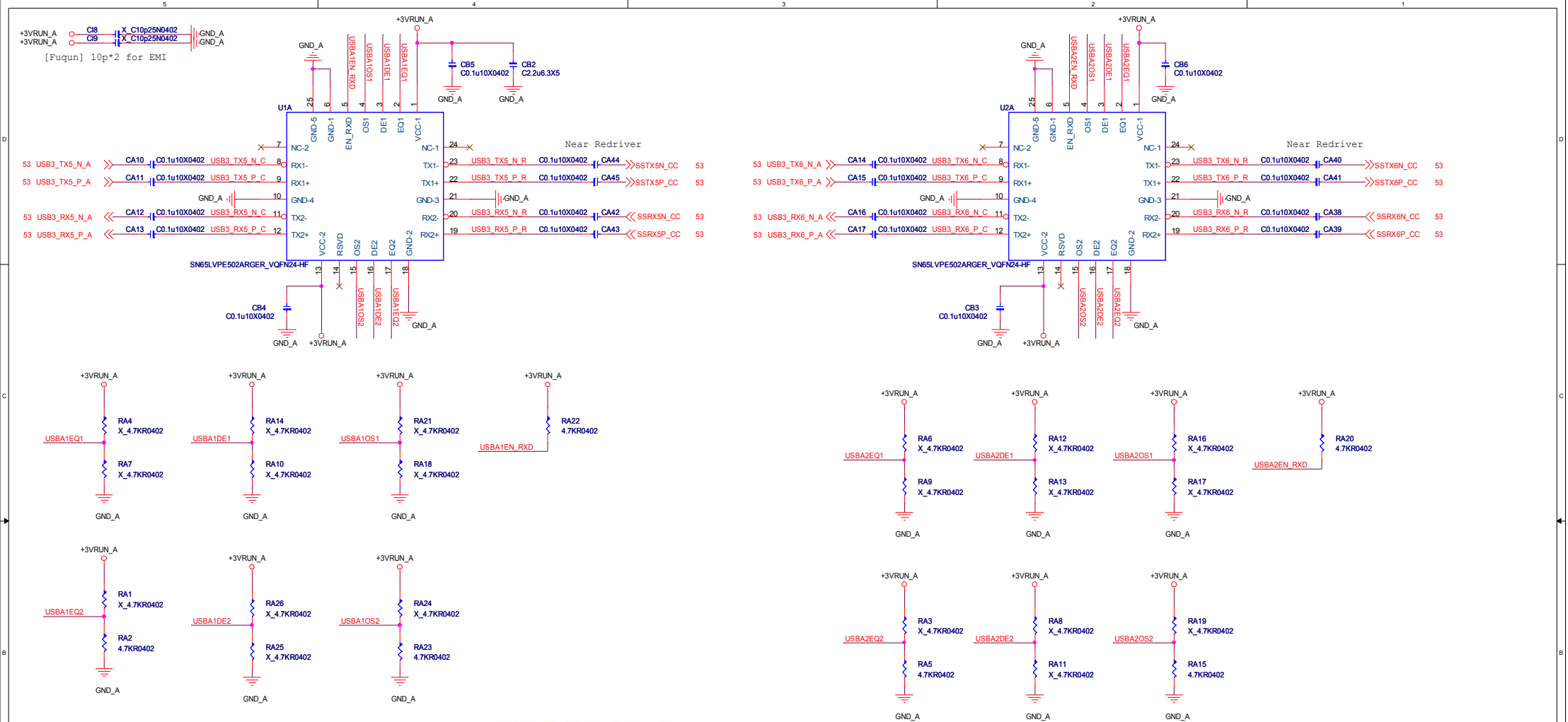


Table 2. Signal Control Pin Setting

OUTPUT SWING AND EQ CONTROL (at 2.5 GHz)			
OSx ⁽¹⁾	TRANSITION BIT AMPLITUDE (TYP mVpp)	EQx ⁽¹⁾	EQUALIZATION (dB)
NC (default)	1042	NC (default)	0
0	908	0	7
1	1127	1	15

OUTPUT DE CONTROL (at 2.5 GHz)			
DEX ⁽¹⁾	OSx ⁽¹⁾ = NC	OSx ⁽¹⁾ = 0	OSx ⁽¹⁾ = 1
NC (default)	0 dB	0 dB	0 dB
0	-3.5 dB	-2.2 dB	-4.4 dB
1	-6.0 dB	-5.2 dB	-6.0 dB

CONTROL PINS SETTINGS	
EN_RXD	DEVICE FUNCTION
1 (default)	Normal Operation
0	Sleep Mode

(1) Where x = Channel 1 or Channel 2

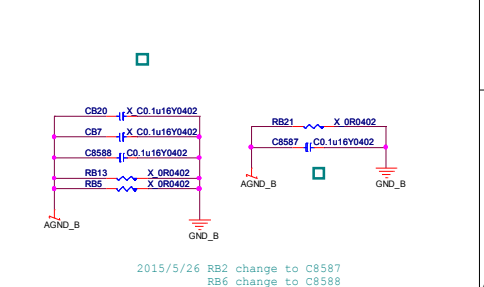
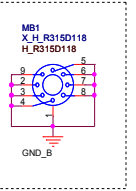
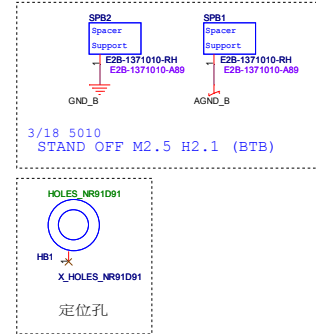
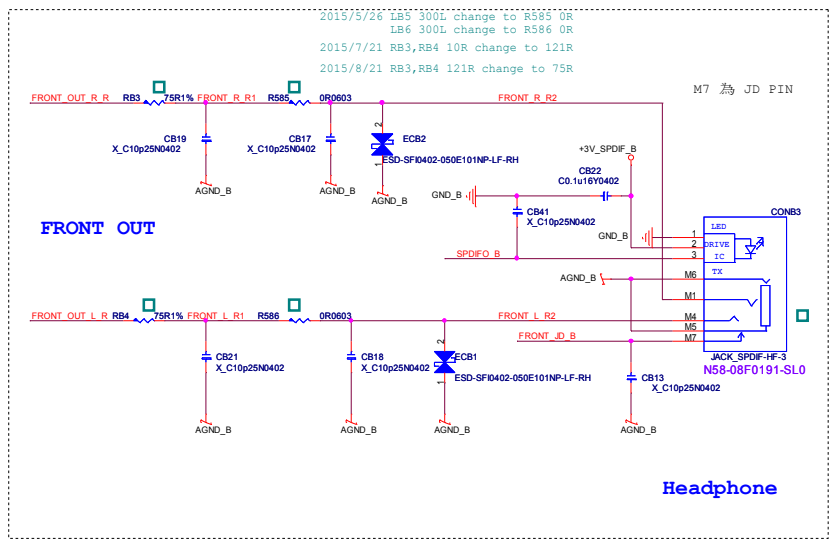
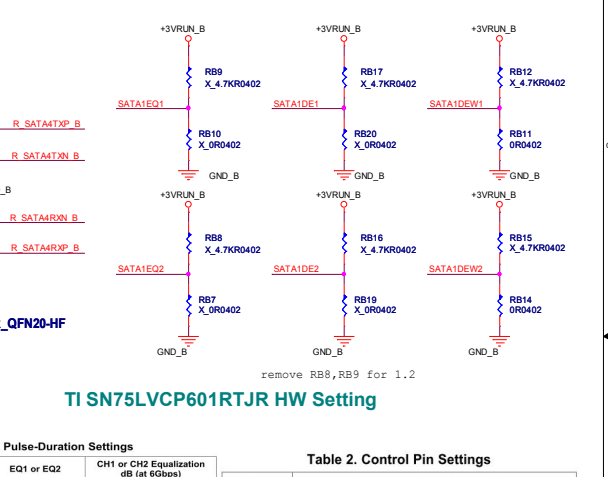
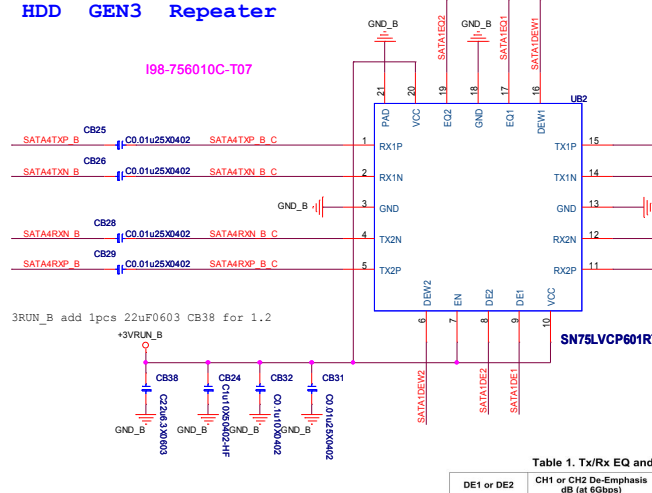
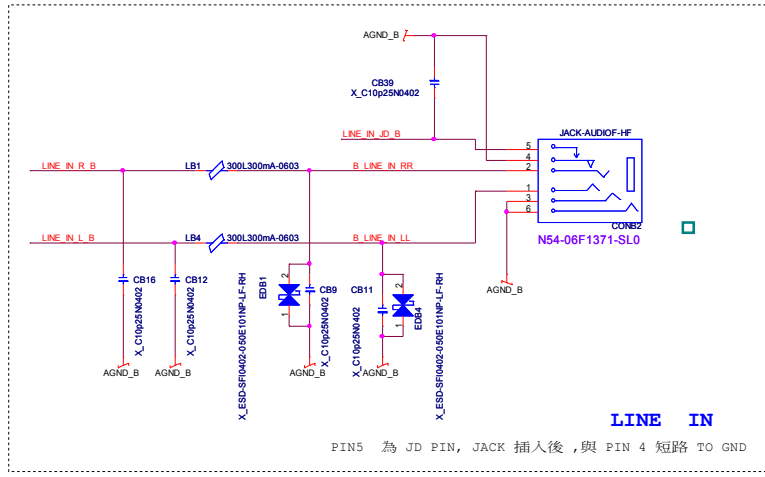
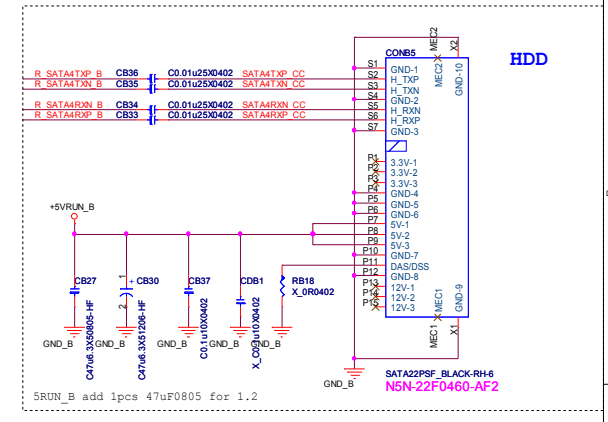
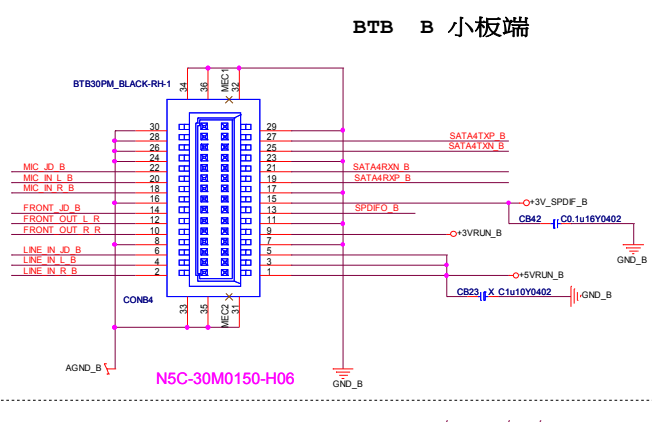
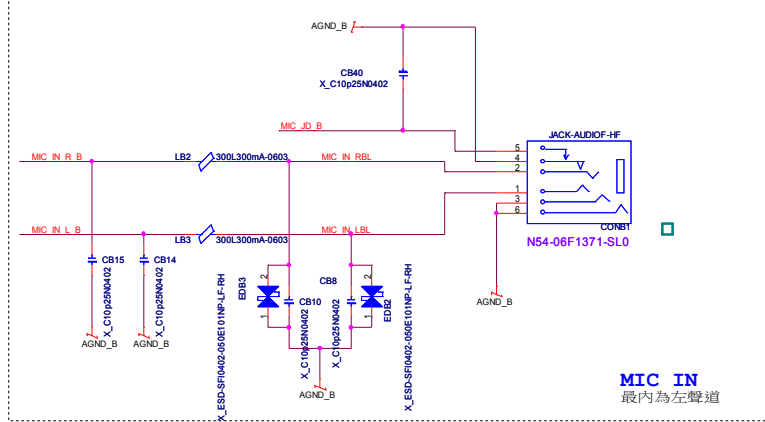


Table 1. Tx/Rx EQ and DE Pulse-Duration Settings

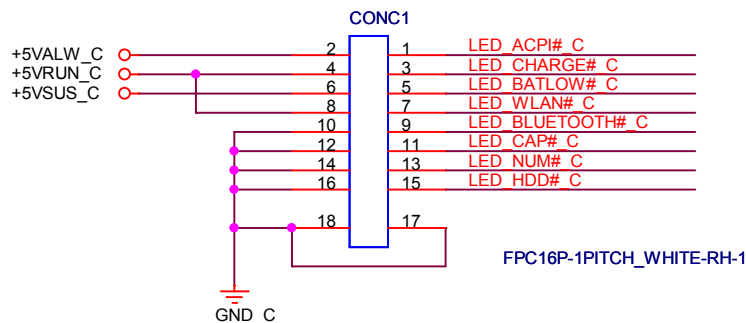
DE1 or DE2	CH1 or CH2 De-Emphasis dB (at 6Gbps)	EQ1 or EQ2	CH1 or CH2 Equalization dB (at 6Gbps)
NC (default)	-4	NC (default)	0
0	0	0	7
1	-2	1	14

DEW1 or DEW2 Device Function → DE Width for CH1/CH2

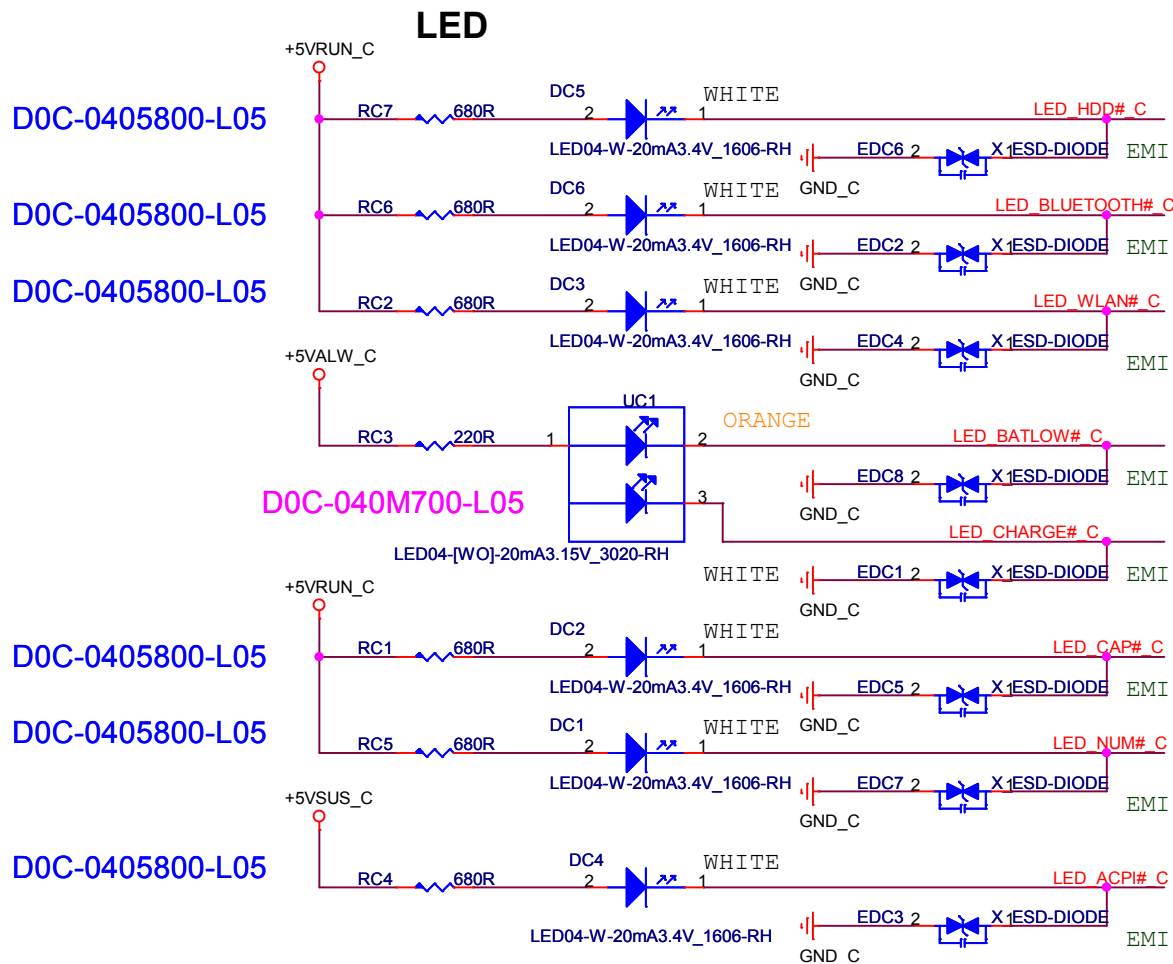
0	De-emphasis pulse duration, short
1 (default)	De-emphasis pulse duration, long

Table 2. Control Pin Settings

EN	Device Function → Standby Mode
0	Device in standby mode
1 (default)	Device enabled



N5A-16F0180-H06

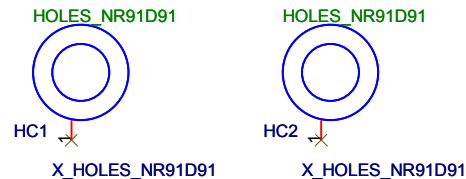


D0C-040M700-L05

D0C-0405800-L05

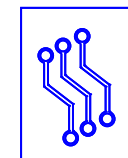
D0C-0405800-L05

D0C-0405800-L05



內徑 2.3mm, 破孔非鎖螺絲

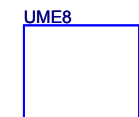
PCBC1



P30-1776C10-H73

P30-1776C10-H73

瀚宇博德 P30-1776C10-H73
健鼎無錫 P30-1776C10-T53

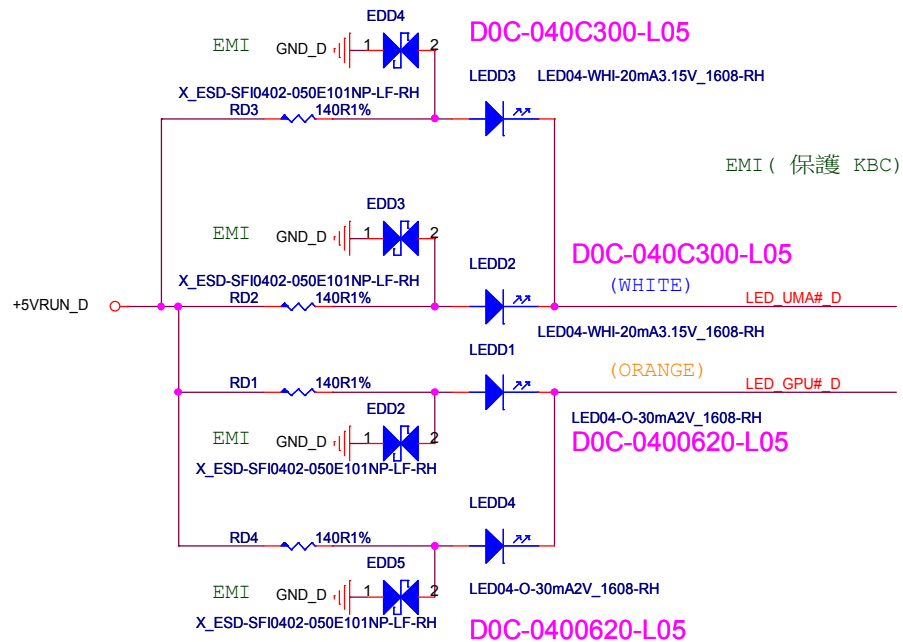


60階

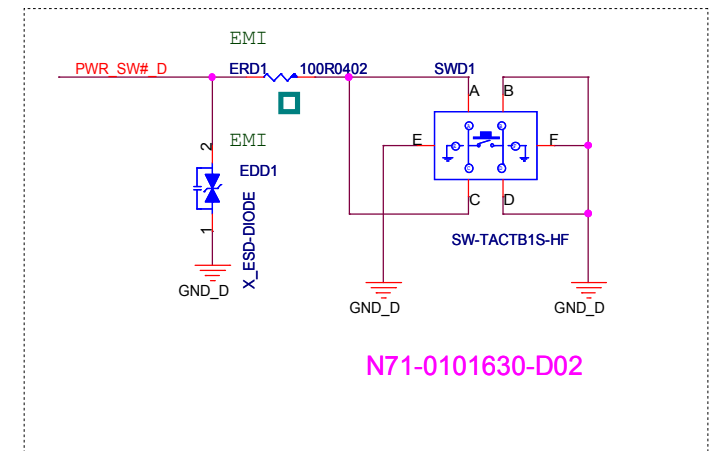
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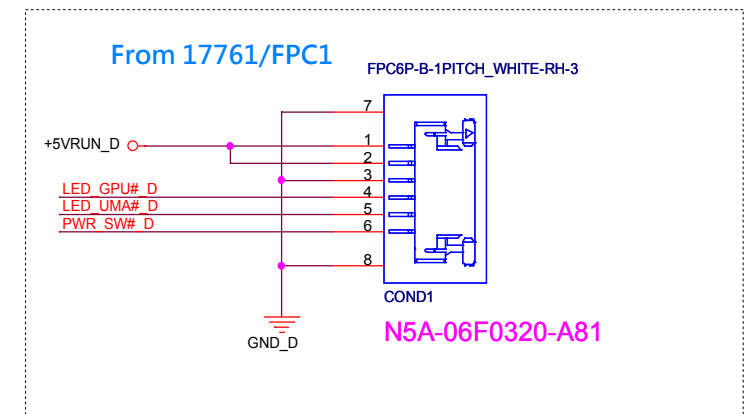
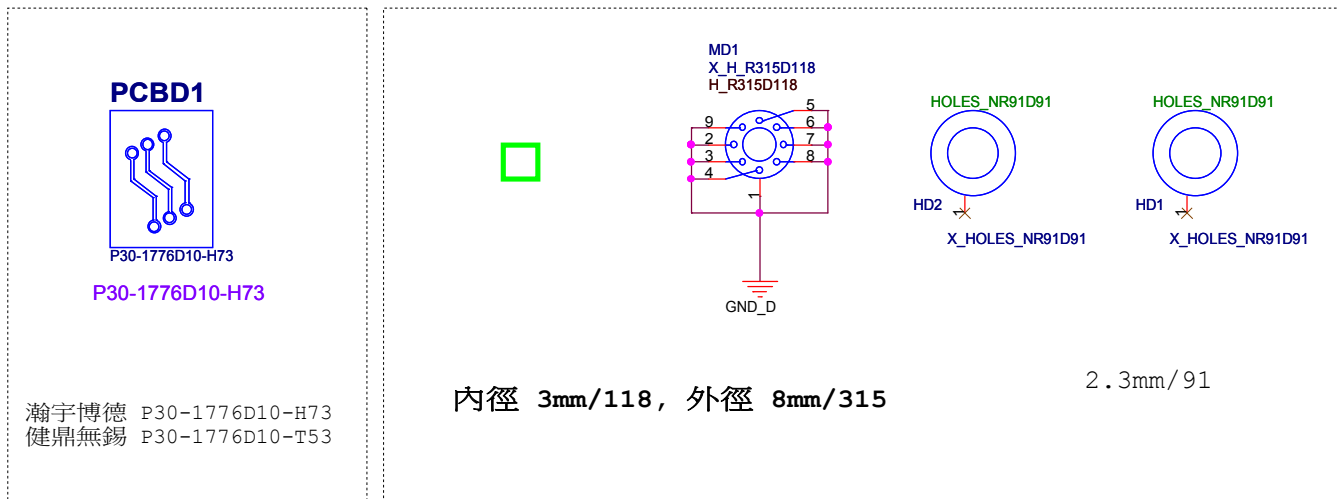
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LED Board		
Size	Document Number	Rev
	MS-1776C	10
Date:	Thursday, August 20, 2015	Sheet 57 of 66



2015/7/9 Change ERD1 from 0R to 100R



N71-0101630-D02

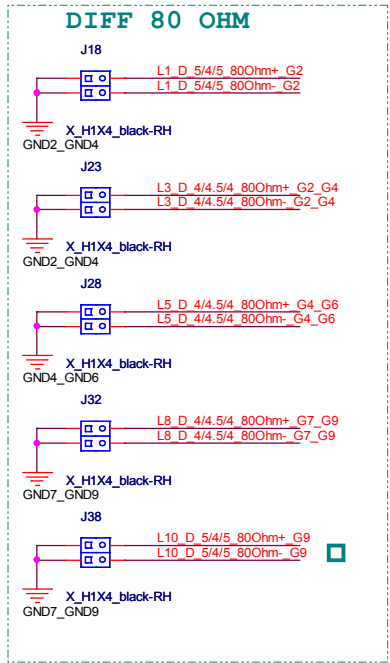
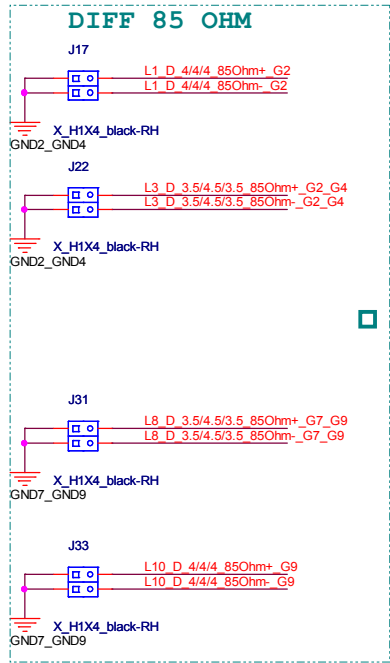
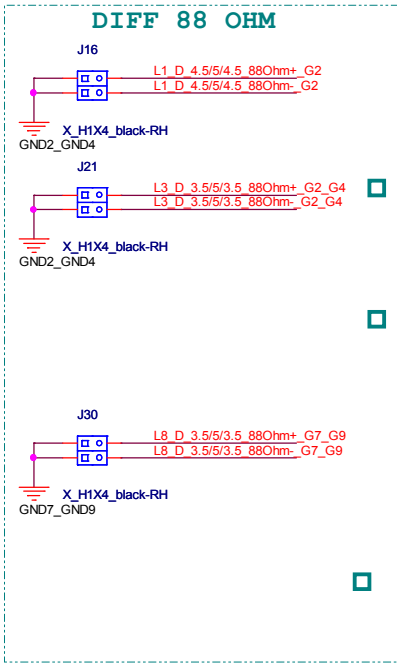
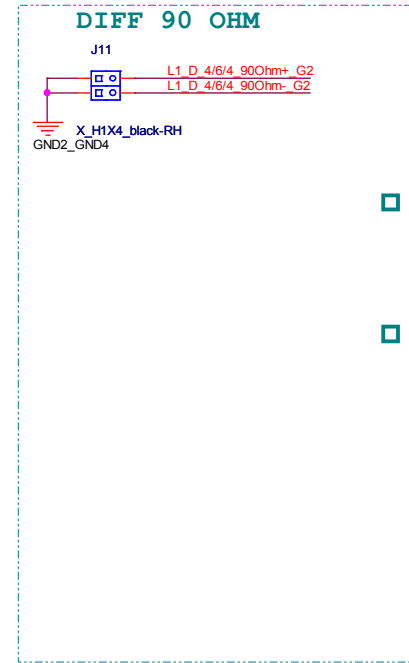
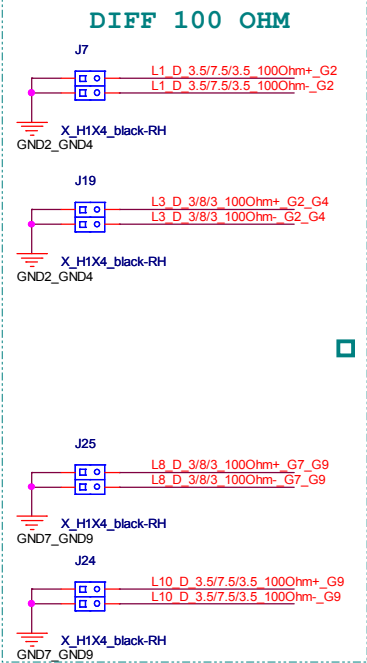
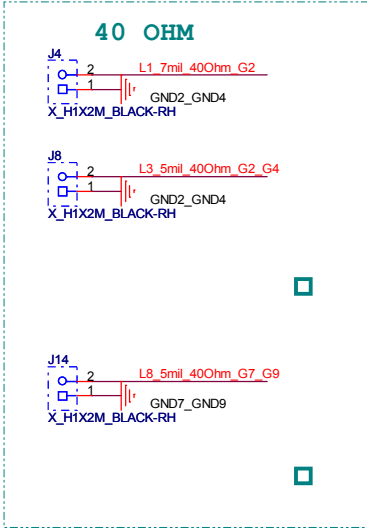
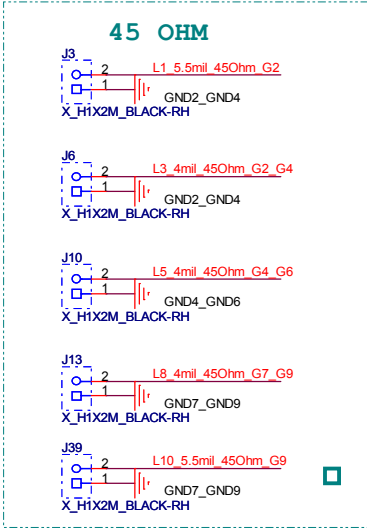
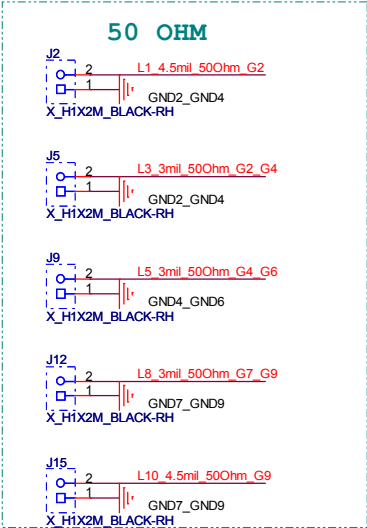


N5A-06F0320-A81

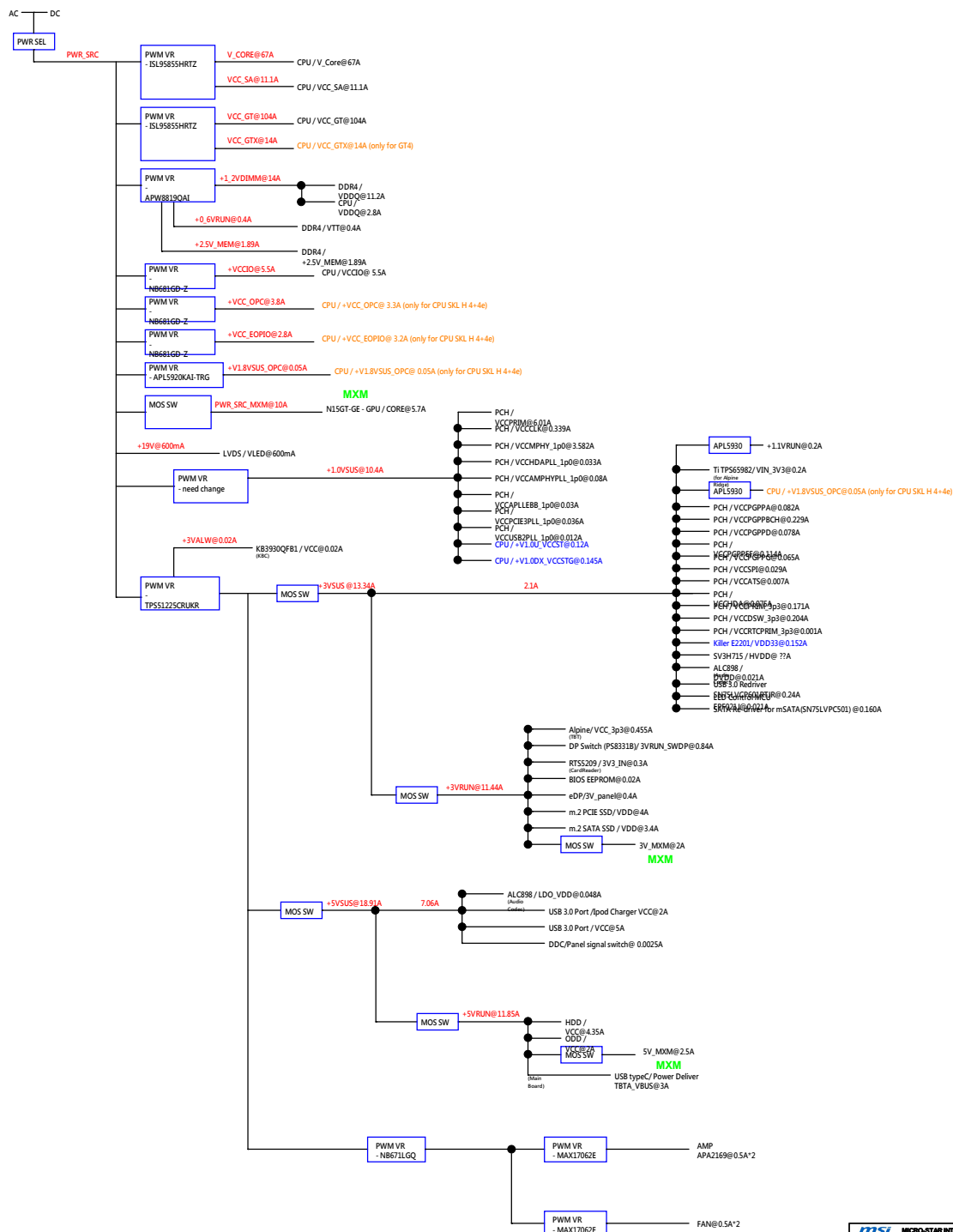
瀚宇博德 P30-1776D10-H73
健鼎無錫 P30-1776D10-T53

內徑 3mm/118, 外徑 8mm/315

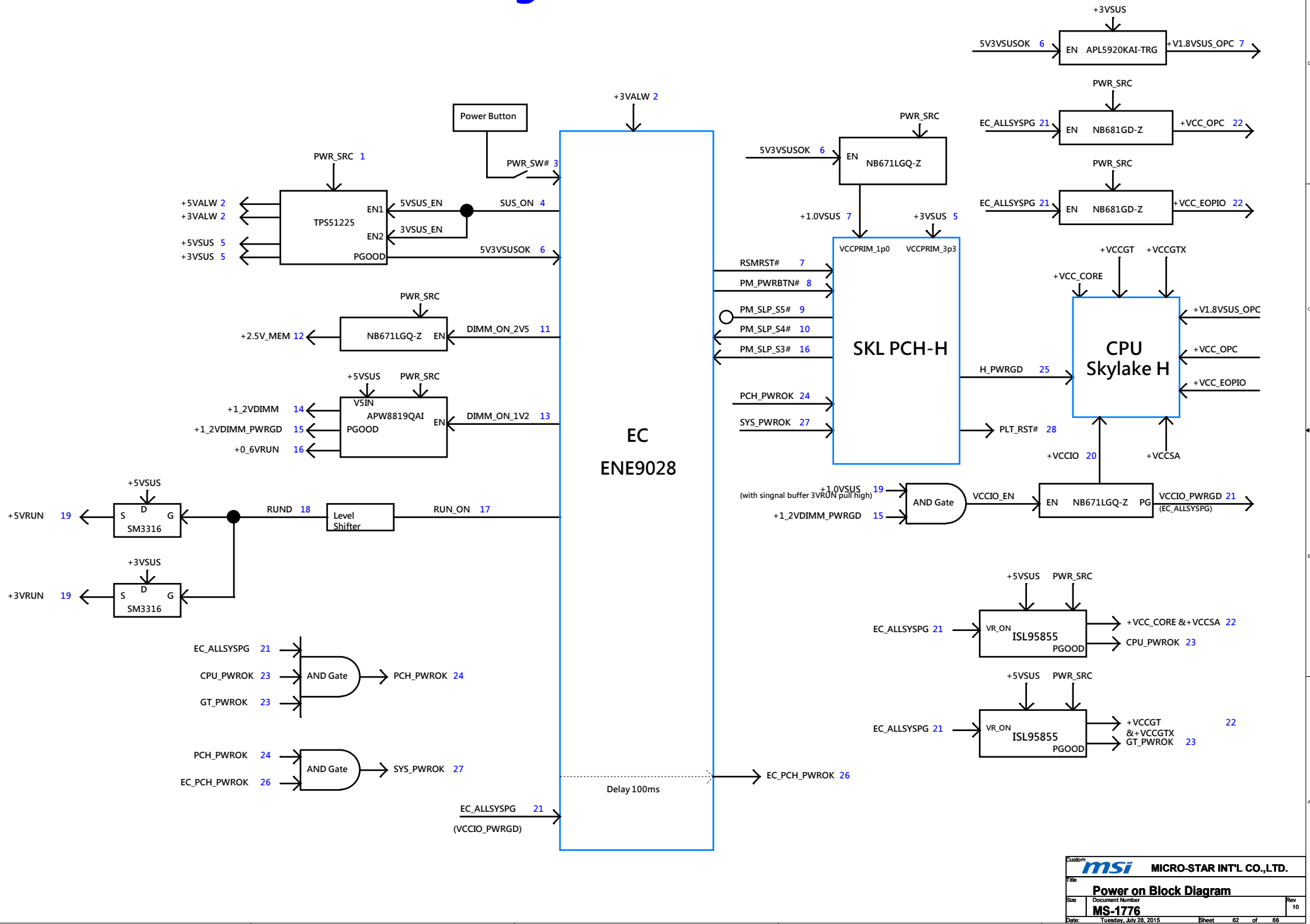
2.3mm/91



1776 Power Delivery Chart

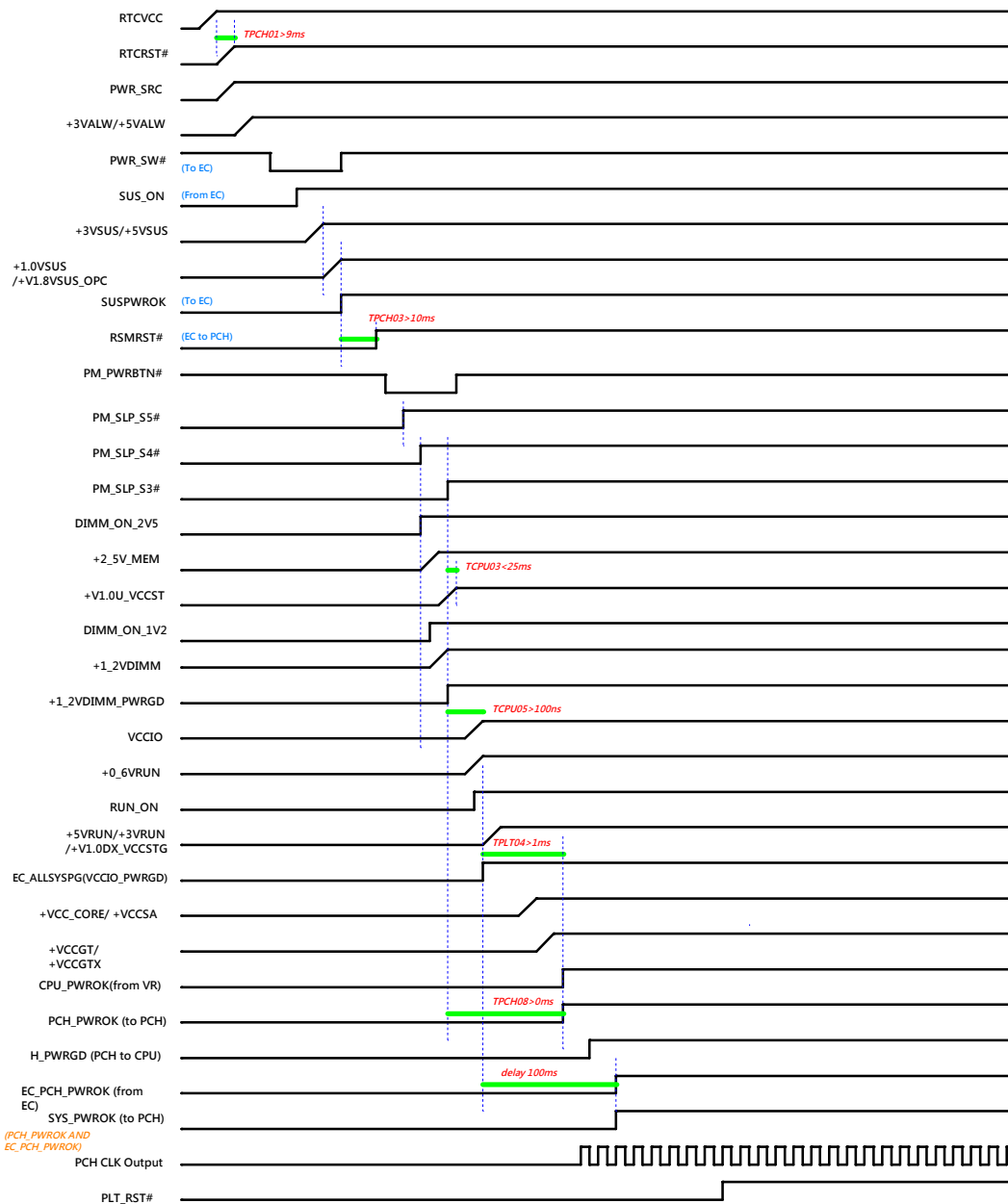


1776 Power on Block Diagram



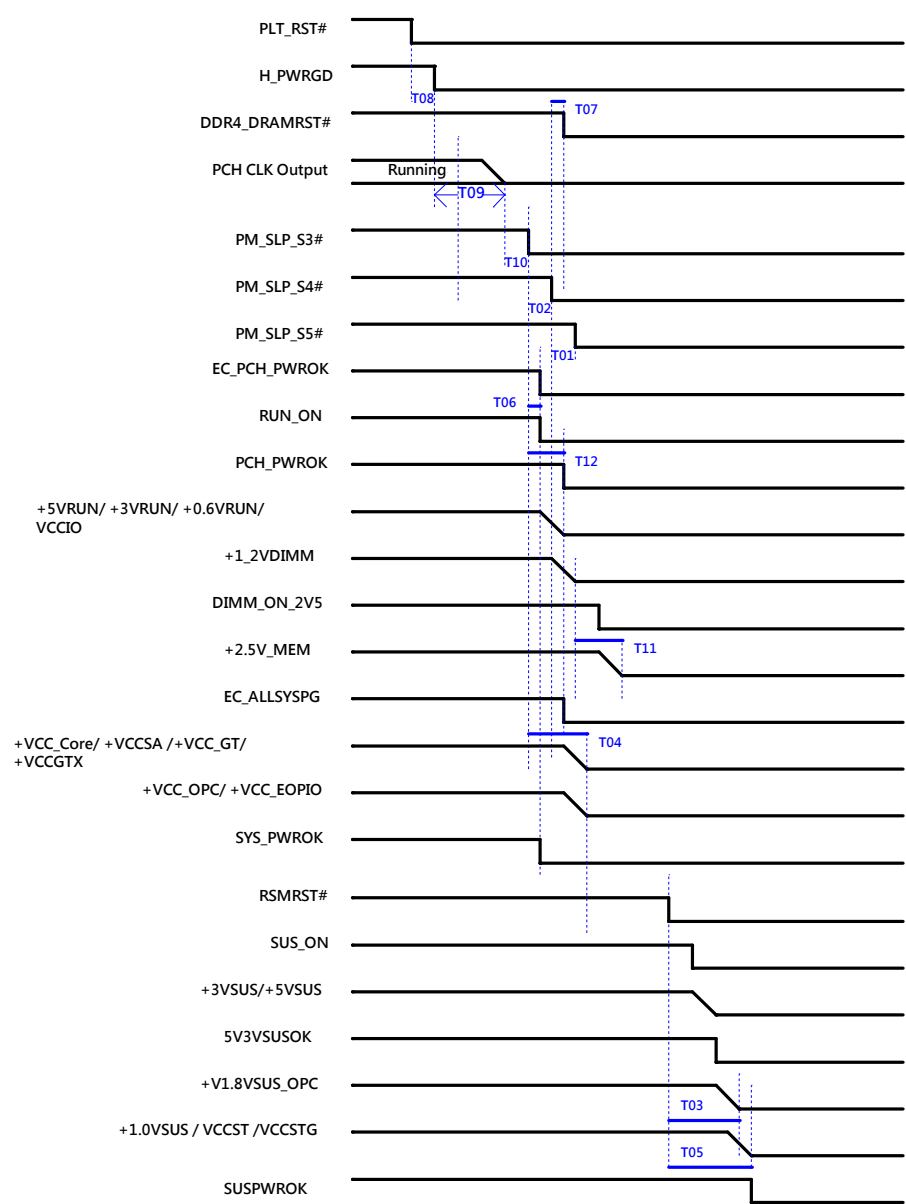
Power on Sequence

G3 -> S0



Power down Sequence

S0 -> G3




	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

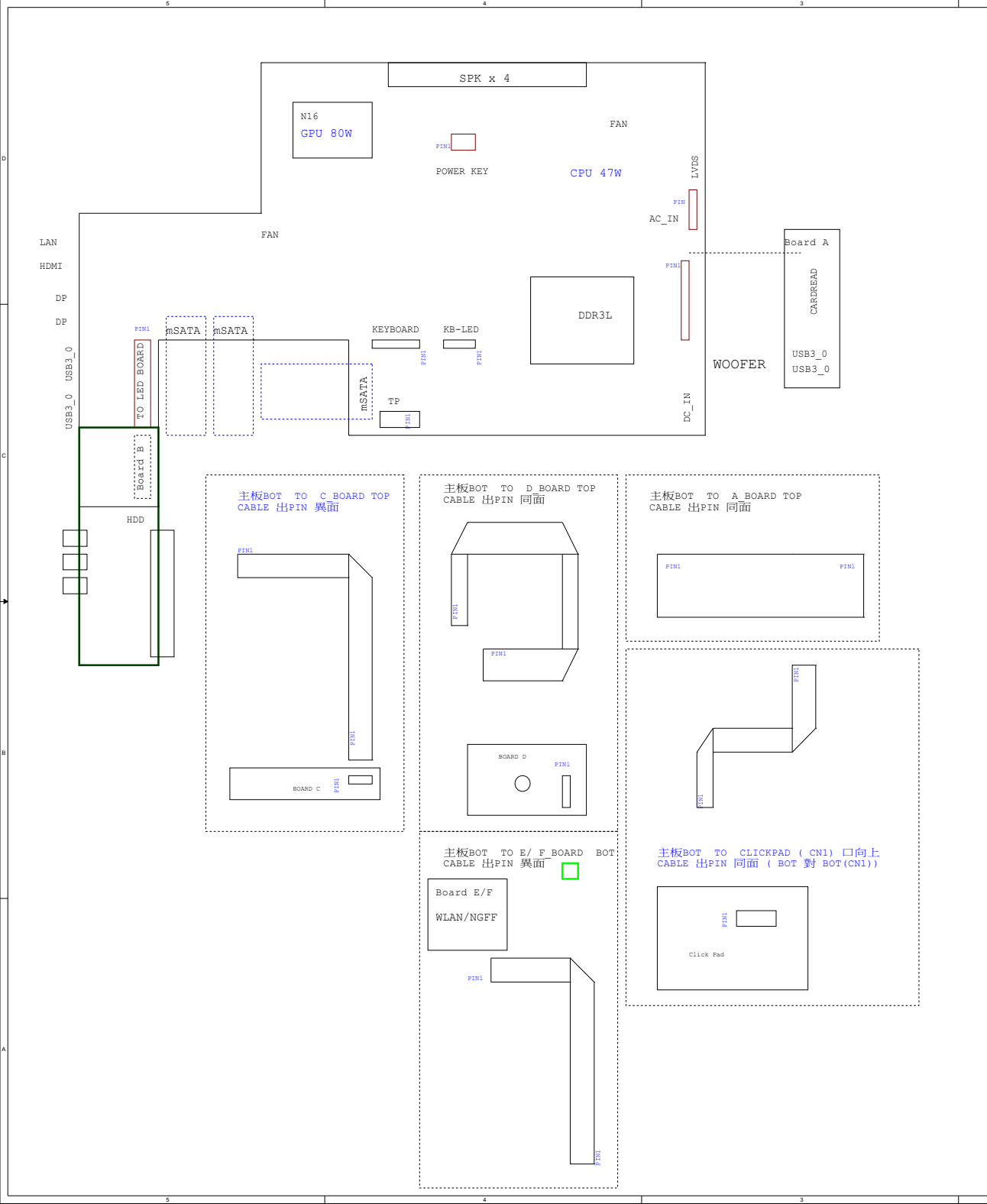
MS-1776 0A Change List

Date	Page	Description	Date	Page	Description
2015/5/14	38	R291 and R297 change to PD	2015/6/16	46	Change PR29, PR169, PR19, PR25, PR77, PR10 from 0R to 2.2R
2015/5/14	38	Add TP3 SSD1_DAS and TP4 SSD2_DAS	2015/6/17	37	Change C177 and C780 from 0.1u to bead 10L
2015/5/20	03	Add R168 and R170 reserved	2015/6/17	37	Change R416 from 0R to bead 10L
2015/5/20	24	Q30 and C797 change to un-stuff	2015/6/25	45	Change PU2 PN from I32-958550C-II1 to I32-958552C-II1
2015/5/20	23	Delete R187 and R182	2015/6/30	28	Change U23 PN B02-011422C-AD0
2015/5/20	30-31	R263, R264, R538 and R539 change to 4.7K	2015/7/9	58	Change ERD1 from 0R to 100R
2015/5/20	32	R560 change to unstuff	2015/7/13	18	U3008, C3131, R3136, R3132, R3139, R3142 change to unstuff
2015/5/20	32	Add C804 0.1uF connect to +5VRUN_L	2015/7/13	36	R519 75R change to stuff
2015/5/20	22	R477 change to 20K PD and R474, R477, R485 change to unstuff	2015/7/14	49	Change PR3009 from 5.6K to 5.9K
2015/5/20	04	Delete R345, R339, C615, M_VREF_DQ_DIMMA change to TPJNC21	2015/7/14	49	Change PR3010 from 6.49K to 5.9K
2015/5/21	03	Delete H_TRST_N connect R327 51R to GND	2015/7/14	49	Change PR3016, PR3033, PR3120, PR3049, PR3005, PR3122 from 2.2 to 3.3
2015/5/21	24	Add PCH_JTAG_TMS, PCH_JTAG_TDO, PCH_JTAG_TDI pull up 51R to +V1.0U_VCCST	2015/7/14	25	Change U52, C8577 unstuff; R8251 0R stuff
2015/5/21	24	Change PM_SYSRST# pull up 10K to 3VSUS from 3VRUN	2015/7/15	25	Change R143/R137 stuff
2015/5/21	22	Delete M2B_CLKREQ# connect R418 10K to GND	2015/7/16	36	Change R519 from 1% to 5%
2015/5/21	23	Add R327 0R and R294 change to unstuff	2015/7/17	37	Change C149 C150 from 20pF to 22pF for SA
2015/5/21	26	C824 change to 0.1uF from 1uF	2015/7/17	22	Change C175 C176 from 16pF to 12pF for SA
2015/5/22	23	R189 change to 620R from 604R	2015/7/21	56	RB3,RB4 10R change to 121R
2015/5/22	45	Reserve PC245 0.1 uF to GND on EC_ALLSYSPG	2015/7/22	45	Change PR8 from 470R to 330R
2015/5/25	35	Modify Q36 PN:D03-2307A09-ST8 ; Add R8268 0R and Q34, Q35,R534 change unstuff	2015/7/22	45	Change PR140 from 2.15K to 2.43K
2015/5/25	35	Add C1013 47uF and C276 0.1uF ; Modify ALC898 DVDD connect to 3VRUN & add C8586 0.1uF	2015/7/22	45	Change PC5 from 0.01uF to 0.1uF
2015/5/25	36	Add OP AMP for ES9016 AVCCDAC pin	2015/7/22	45	Change PC7 from 0.082uF to 0.1uF
2015/5/26	28	R577 change to unstuff, have internal PU	2015/7/22	45	Change PR1 from 82K to 86.6K
2015/5/26	36	U31 and U29 Vin change to 5VSUS from 5VRUN	2015/7/22	45	Change PR21 from 374R to 383R
2015/5/26	36	R524,C933 change to stuff and R521 change to unstuff on EC_MUTE#	2015/7/22	45	Change PR181 from 2.94K to 2.8K
2015/5/26	36	X1 PN change to D04-5100200-T16	2015/7/22	45	Change PC178 from 1000PF to 1500PF
2015/5/26	56	LB5 300L change to R585 0R ; LB6 300L change to R586 0R	2015/7/22	45	Change PR178 from 2.55K to 1K
2015/5/26	56	RB2 change to C8587 ; RB6 change to C8588	2015/7/22	45	Change PC31 from 0.082uF to 6.8nF and stuff
2015/5/26	36	R519 change to unstuff by vender suggestion	2015/7/22	45	Change PC162 from 0.068uF to 0.047uF
2015/5/26	35	SUBWOOFER change to MIC2 port by vender suggestion	2015/7/22	45	Change PC161 from 0.082uF to 6.8nF and stuff
2015/5/26	32	R566,R567 change to unstuff on HDMI_SDC/SDA	2015/7/22	45	Change PR26 from 1.43K to 2.26K
2015/5/27	47	Delete R121 and add U25 AND gate,C108 for rCPU28a power down sequence	2015/7/22	45	Change PC34 from 1000PF to 1500PF
2015/5/27	43	Add U27 AND gate,C181 for tPLT15 power down sequence	2015/7/22	45	Change PR33 from 2.87K to 2.05K
2015/5/27	43	Delete PQ42,R503,R504,PC211,PR222,Q33,PR229,PC212,U46A on +0_675VRUN_EN control circuit			
2015/5/27	43	Add C547,R76,U36 SN74AUP1G07 circuit by DDR_VTT_PG_CTRL control to enable VDDQ_VTT			
2015/5/27	9-10	C808,C875 22uF change to 2.2uF			
2015/5/28	27	R296 change to unstuff on L_LDRQ0#			
2015/5/29		C0402_EXTRA_T footprint change to C0402_EXTRA			
2015/5/29	56	CONB1,CONB2 change to N54-06F1371-SL0 ; CONB3 change to N58-08F0191-SL0			
2015/6/1	48	PR4144 and PR3129 change to stuff on PEX_PWRGD			
2015/6/1	48	PR3129 change to stuff on FBVDDQ_PG			
2015/6/1	23	Delete TPJNC17 on GPP_F13			
2015/6/2	59	Delete RE1 100K PU and key E pin1 connect to GND			
2015/6/2	28	U51 PN change to M31-25D1002-GA0			
2015/6/2	12	C3334 22uF change to C11-226A314-S02 from C11-226A213-M09			
2015/6/2	12	Delete R8265 0R and R8266 0R and add L3006			
2015/6/2	47	Delete R75, C104,C106,U11 AND gate			
2015/6/2	23	R454 change to 1 K from 10K, follow EDS p290			
2015/6/2	21	R3141, PQ3039,PQ3019 change to unstuff on 3V3_MAIN_EN			
2015/6/3	49	Reserved PEC3012 and PEC3008 470uF on NVVDD for N16E-GR			
2015/6/3	45	PR64 change to 10K from 20K			
2015/6/3	45	PR55 change to 48.7K from 56.2K			
2015/6/3	45	PC55 change to 330pF from 100pF			
2015/6/3	47	R86 change to 0R and C135 unstuff on VCCIO_EN			
2015/6/3	24	Change PM_SYSRST# pull up 10K to 3VRUN			
2015/6/3	24	Delete R339, R345, R427			
2015/6/3	28	R576 0R change to stuff for ASM1142 wake			
2015/6/4	19,27	Delete R3118, Q3003, R3125 on OVERT#			
2015/6/4	19,27	Delete R3052 on EC_PROTECT_PWR			
2015/6/5	50	PR263 change to 0R and PC244 unstuff			
2015/6/5	50	PR265 change to unstuff			
2015/6/5	36	Delete U3009,R584, R488			
2015/6/8	49	Change PEC3018 from 330uF to 470uF and delete reserved PEC3008 470uF			
2015/6/8	21	PQ4013,PR4146,R8262 change to unstuff (PEX_VDD discharge)			
2015/6/9	13-14	C3000,C3006, R3261,R3002,R3001 change to unstuff on FBA_VREFD			
2015/6/9	15-16	C3313,C3482,R3305,R3306,R3311 change to unstuff on FBB_VREFD			
2015/6/9	35	Add C364,C365,C1014,C1015			
2015/6/9	36	Delete C8590 and C8589, C8591 change to unstuff			
2015/6/10	35	Add JNC14,JNC26			
2015/6/10	29	Change LI1 and LB1 PN L12-9008100-I05			
2015/6/10	35	Add R584,R587			
2015/6/12	36	Change C317 PN C11-2257523-W08			

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Date	Page	Description
2015/7/28	33	Add C207,R434,R437; Change R37 from 20KR to 68KR; Change PQ12 from 2N7002CK to DMN65D8LDW-7 for panel sequence
2015/7/28	24	Delete Q8,C206 ; SMB_AUDIO_CLK/SMB_AUDIO_DATA connect to SMB_CLK_DIMM/SMB_DATA_DIMM
2015/7/28	48	PR4007 un-stuff ; NVVDD_EN connect to PU4006.13 (PEX_VDD enable) for GC6
2015/7/28	21,49	PR3106 un-stuff ; NVVDD_PWRGD connect to PEX_PWRGD
2015/7/28	27	Add C155 22pF connect to GND on LPC_FRAME# for SA
2015/7/28	25	EC6 10pF stuff for SA
2015/7/28	24	Add EC25 10pF connect to GND on SUS_SMBDATA for SA
2015/7/30	46	Add PC85,PC88 47uF connect to GND on +VCCSA
2015/7/30	38	SSD2_DAS net change to PCIE_SSD2_LED# and add R35 0R unstuff
2015/7/30	38	SSD2_DAS net change to PCIE_SSD1_LED# and add R49 0R unstuff
2015/7/30	39	U32,R277,R278,C343,C344,C327,C328 unstuff for TPM unstuff
2015/7/30	23	R327 change to unstuff on CLK_PCI_TPM
2015/8/6	3-10	Change CPU PN : A0D-6700H15-I06
2015/8/6	22-26	Change PCH PN : B01-HM17005-I06
2015/8/11	18	Add ROM_S2,ROM_H2,V_TOP_S2,V_TOP_H2 for N16E-GR
2015/8/12	49	Reserved PQ3009 and PQ3011 for N16E-GR
2015/8/13	36	R526,R527 unstuff
2015/8/13	60	Modify impedance
2015/8/14	60	Modify impedance
2015/8/20		Modify PCB PN
2015/8/21	56	RB3,RB4 121R change to 75R
2015/8/21A	46	Change PR29,PR169,PR19,PR77,PR25 from 2.2R to 3.3R for VCC_CORE & VCCGT

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" GT " 改 "GX-B

GX-B

G3=OB3-16H2001
R323=15K
PR67=X
R180=10K

不上件

R155
R55
R57
R153
page20 ,21, 22

GT

G3=B03-0N15E05-N08
R323=10K
PR67=100K
R180=X

上件

R155
R55
R57
R153
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" GC6 1.0 " 改 " GC6 2.0
"

GC6 2.0

上件 不上件
R152 R151
PQ15 R148
PQ37 R137
R368 R266
C128 R355
C144 R198
U9 R192
C126
C127
R63
R105
R92
R146
R147
U10
C135
R120
R315
R316
R93
R110
R354

GC6 1.0

不上件 上件
R152 R151
PQ15 R148
PQ37 R137
R368 R266
C128 R355
C144 R198
U9 R192
C126
C127
R63
R105
R92
R146
R147
U10
C135
R120
R315
R316
R93
R110
R354