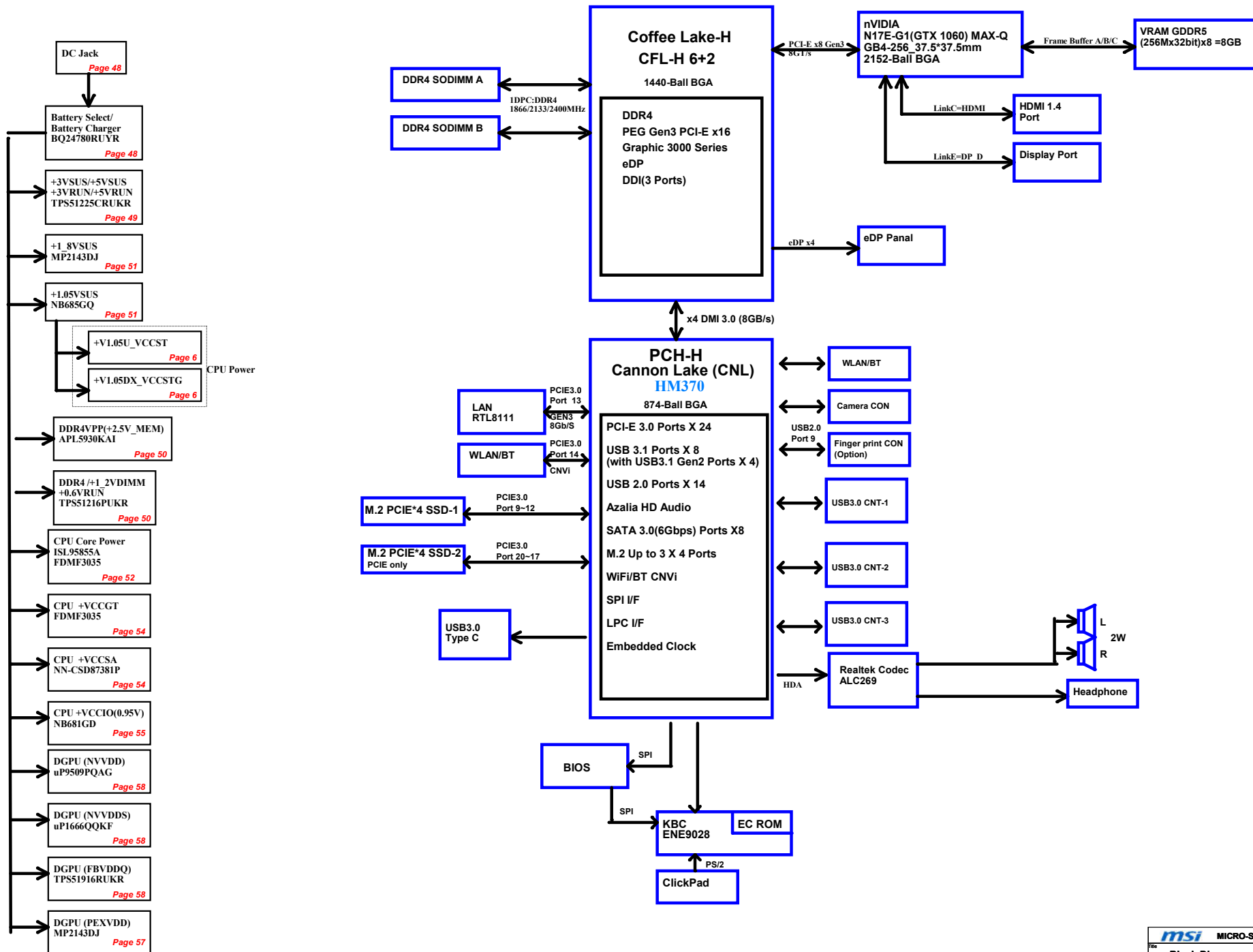
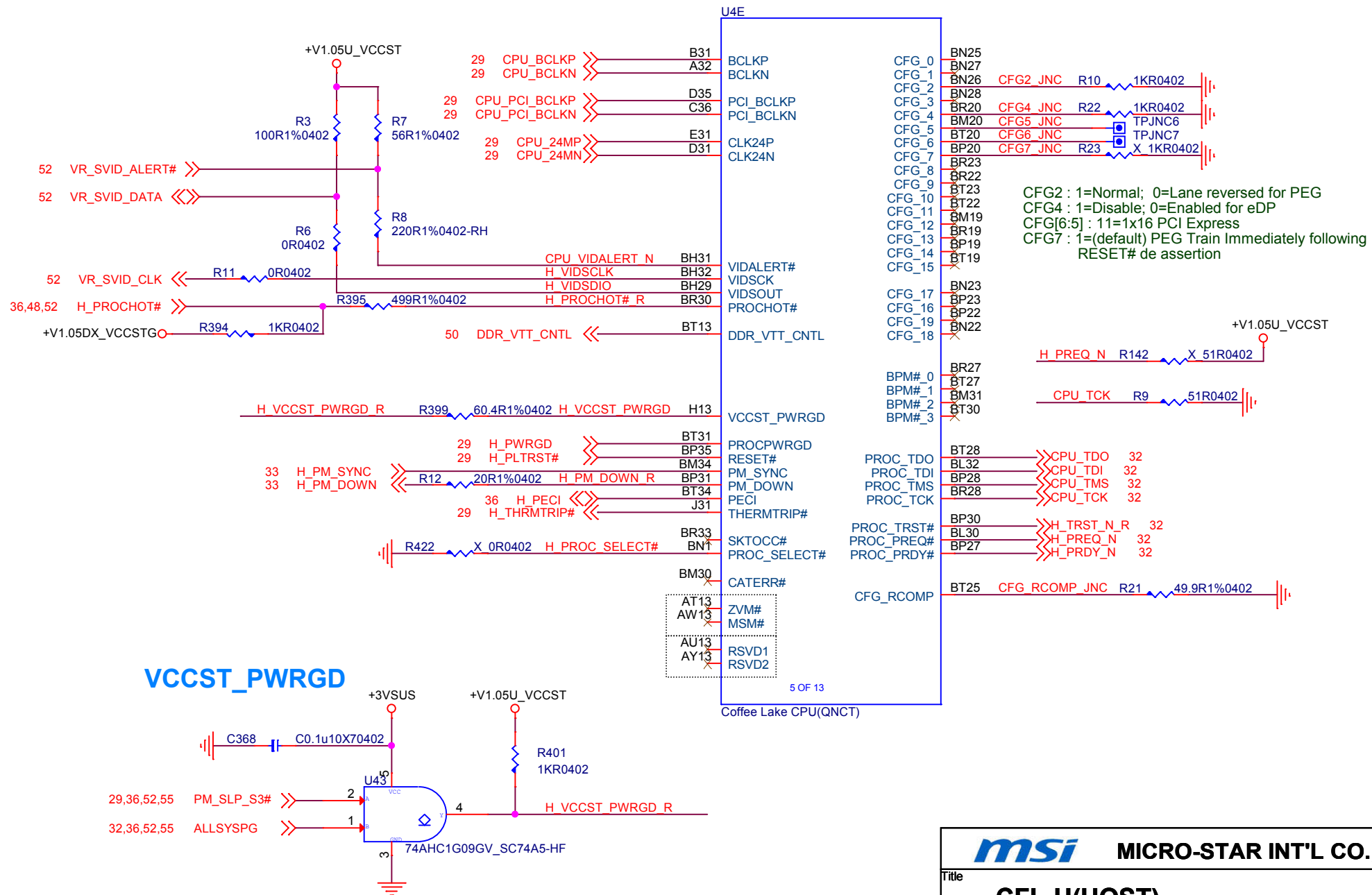


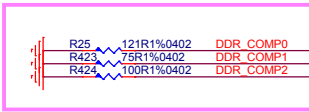
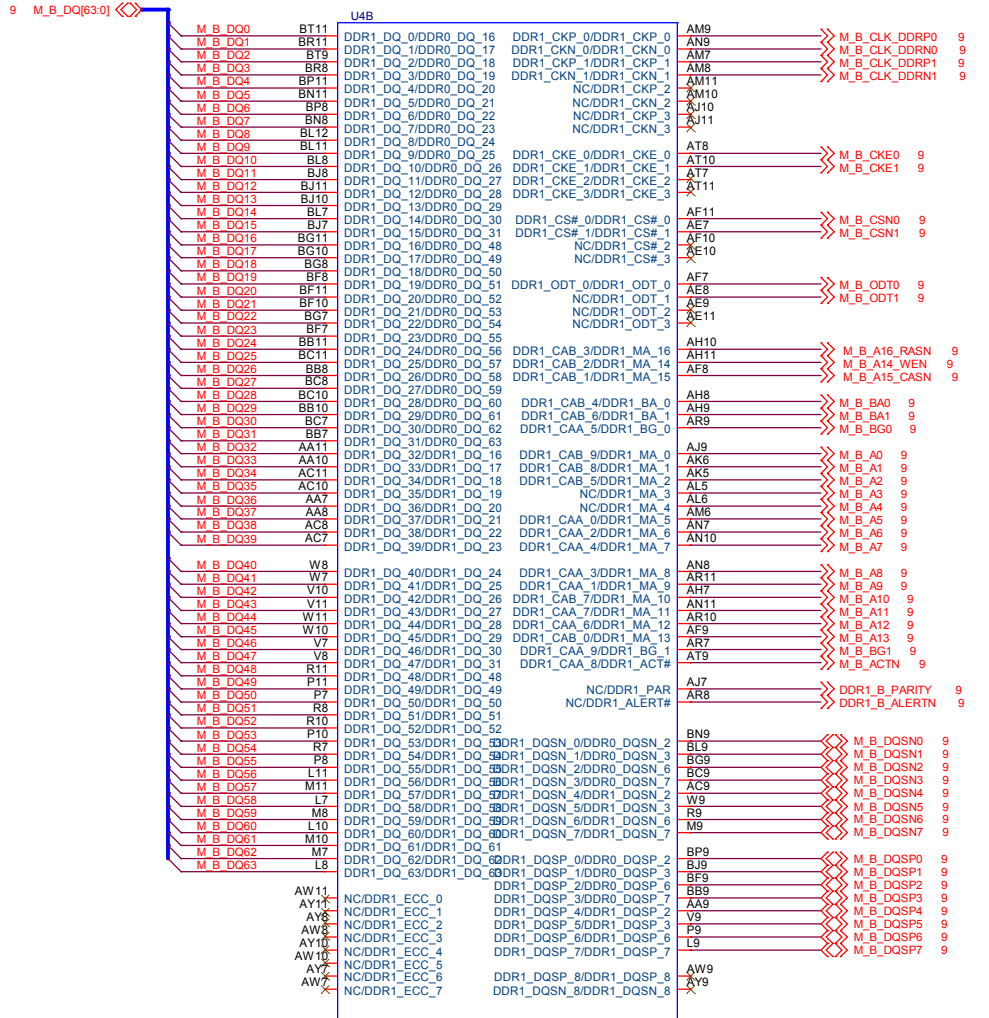
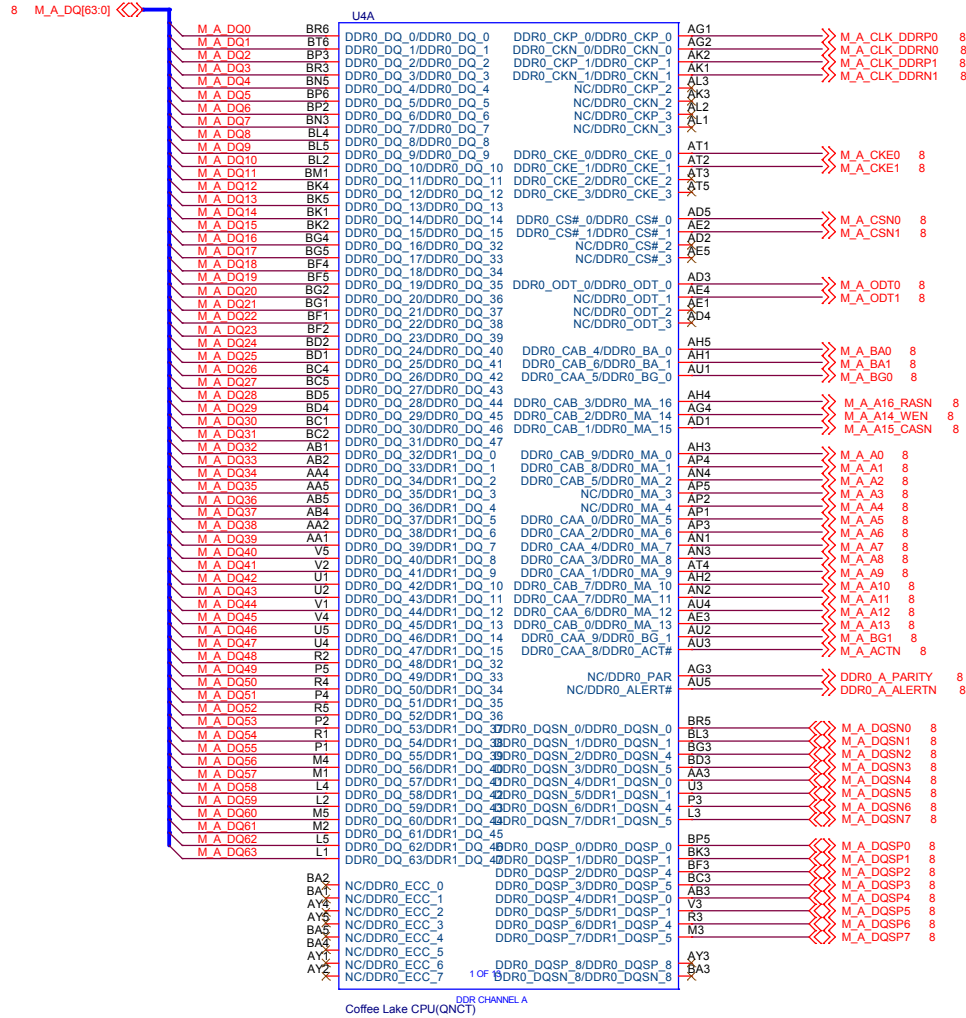
Intel Coffee Lake-H

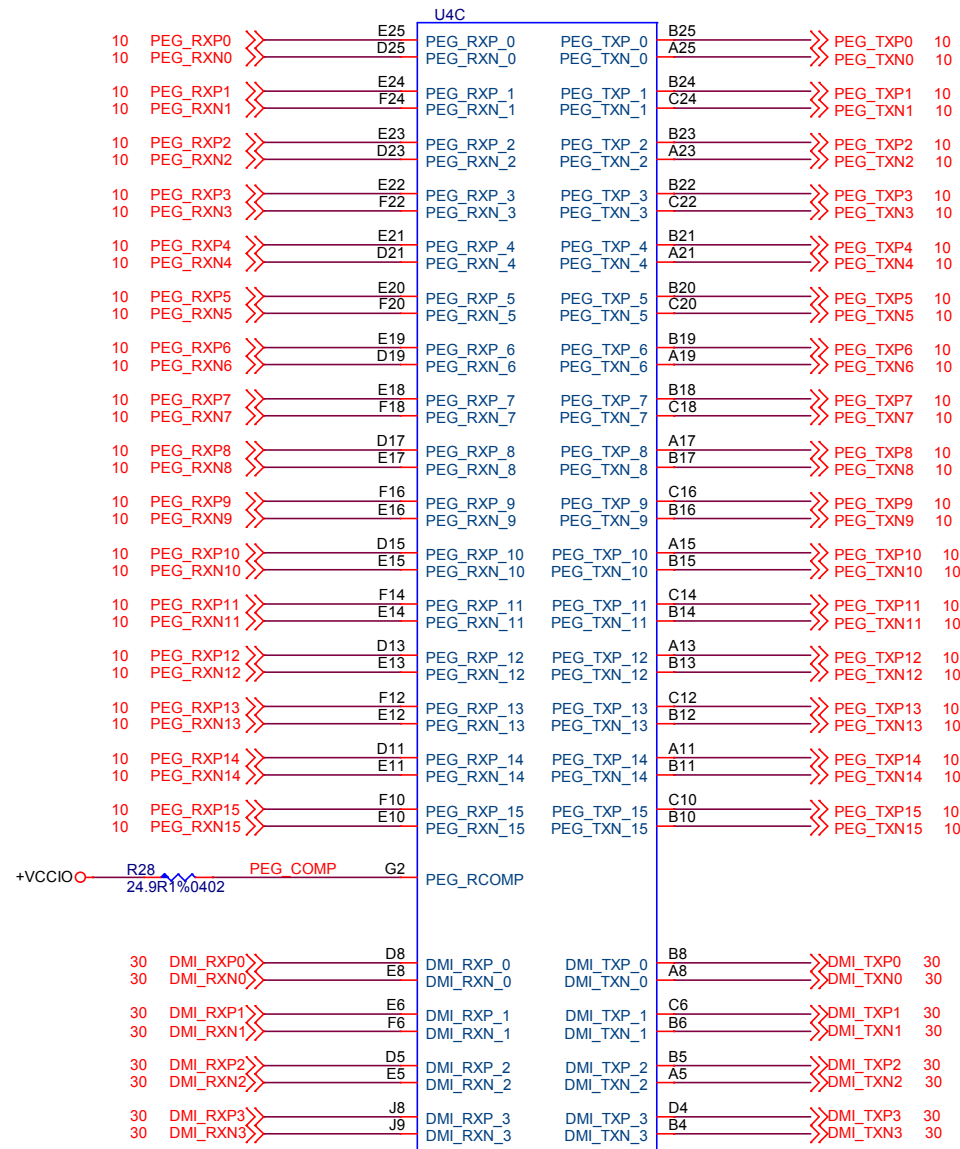


CFL-H (HOST)

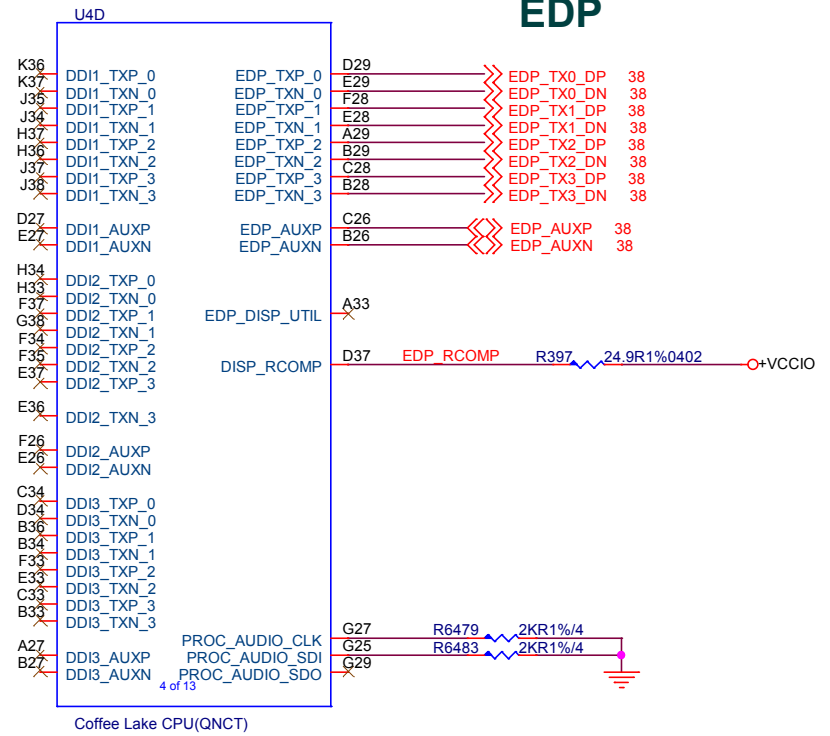


DDR Channel A



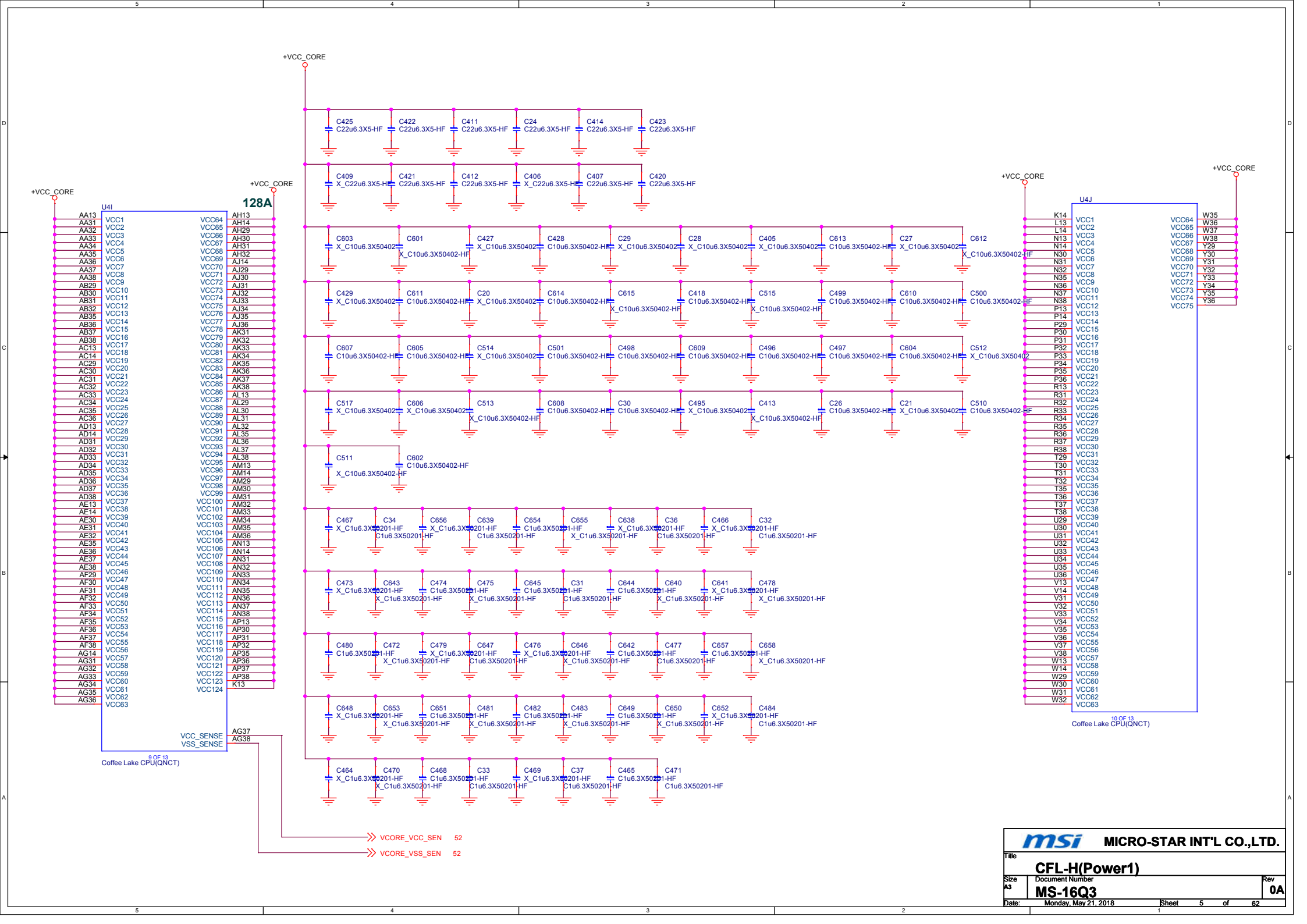


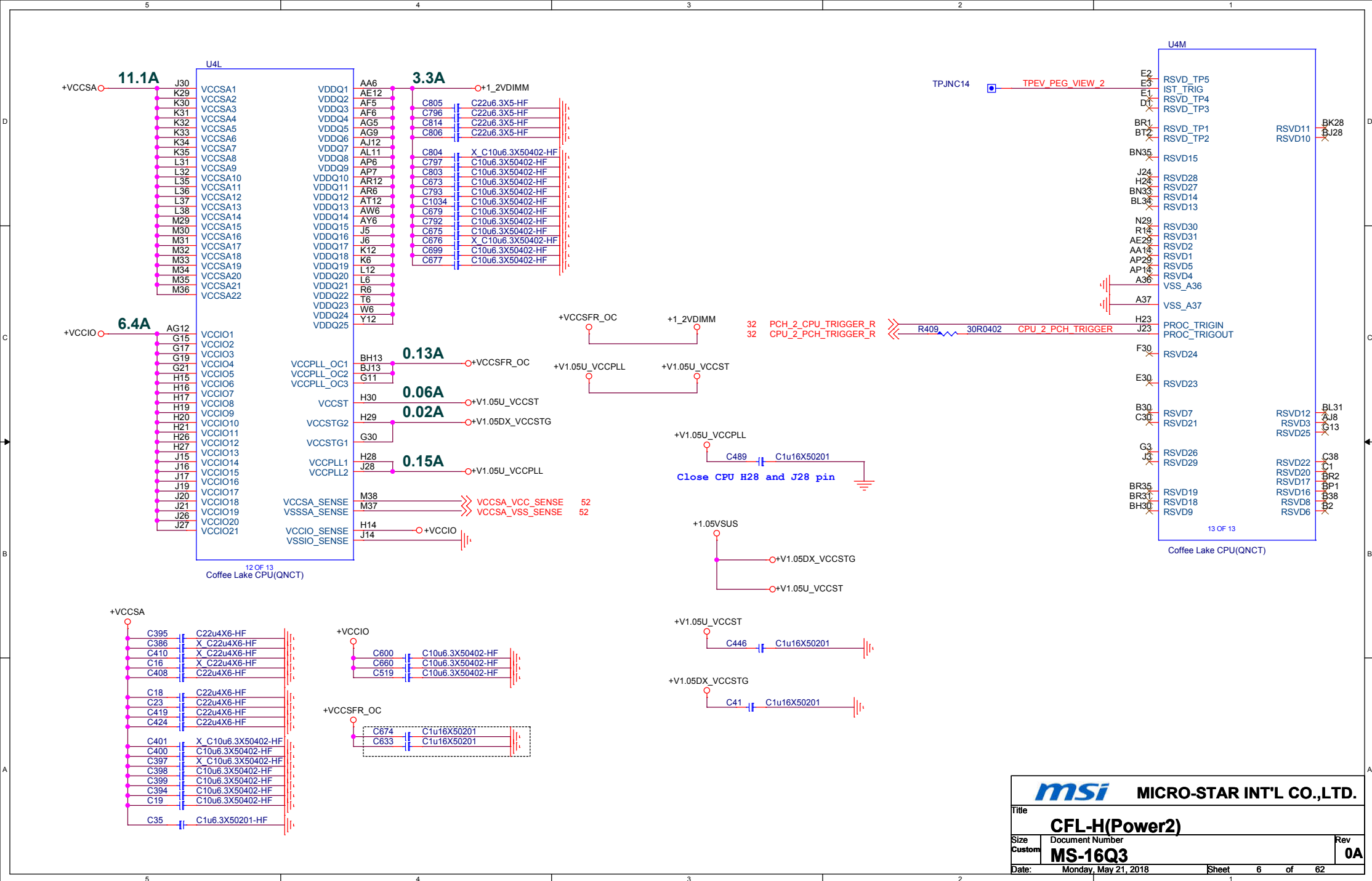
3 OF 13
Coffee Lake CPU(QNCT)

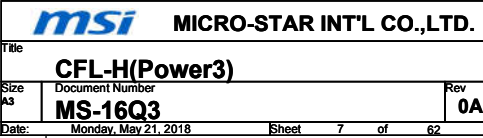


EDP

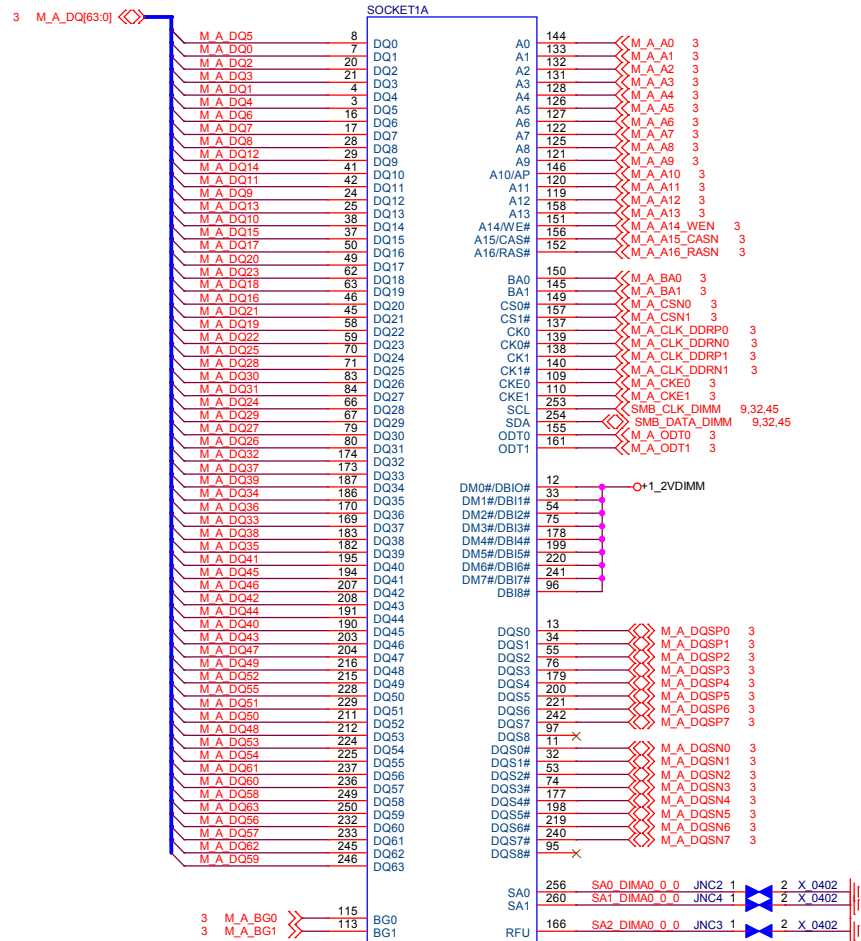
msi		MICRO-STAR INT'L CO.,LTD.	
Title			
CFL-H(DMI/Display)			
Size	Document Number	Rev	
Custom	MS-16Q3	0A	
Date:	Monday, May 21, 2018	Sheet	4 of 62



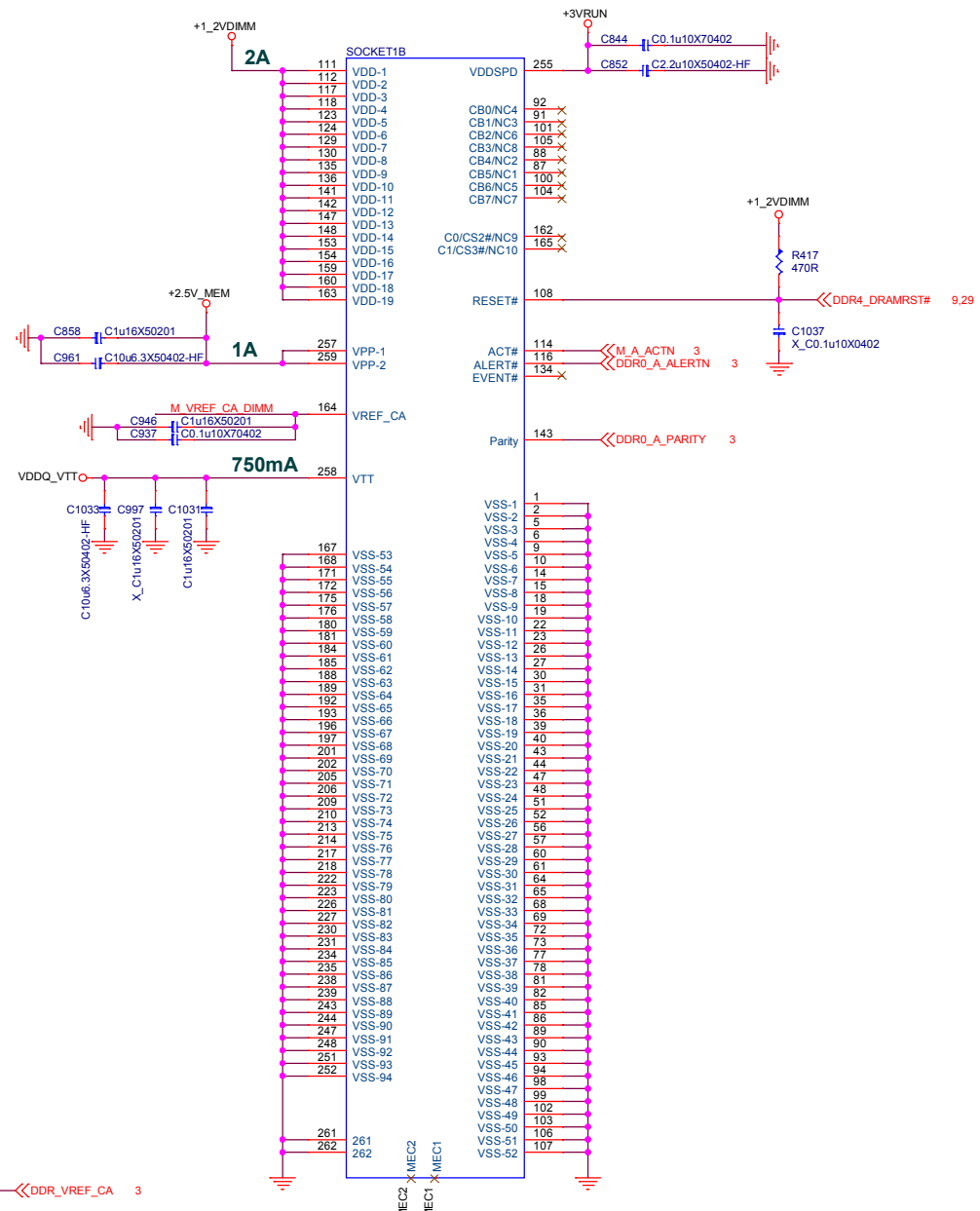
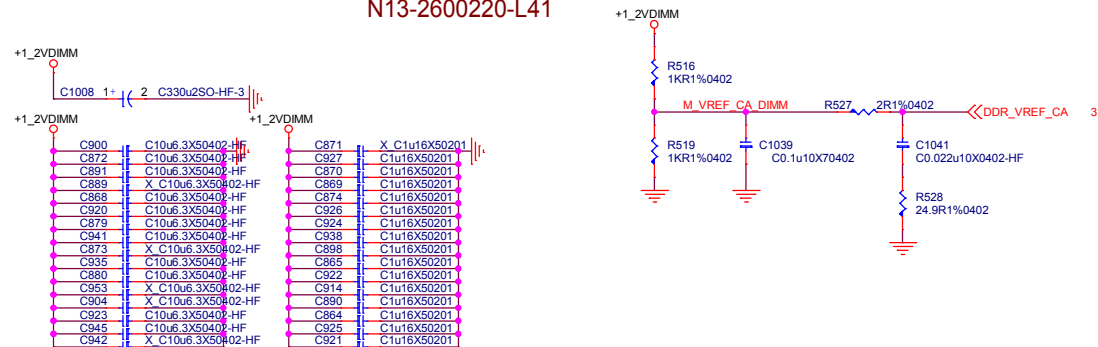




SODIMM_A0 (TOP-Reverse)

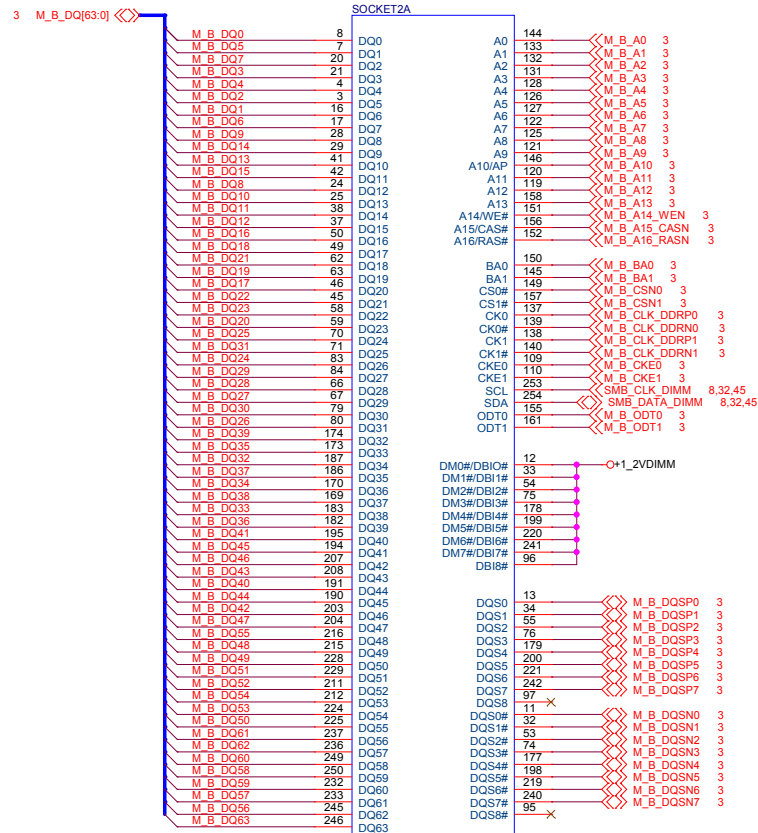


DDR4SODIMM-260PS_BLACK-HF-20
DDR4_SODIMM260P_H4_5
N13-2600220-L41

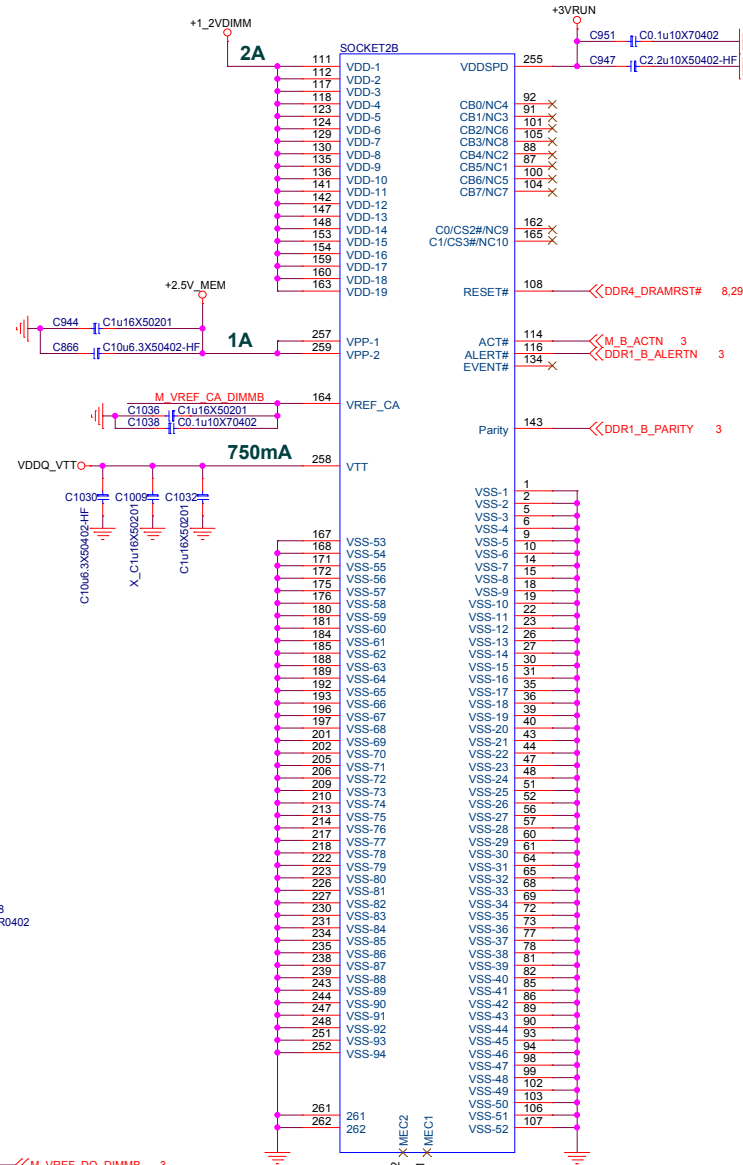


msi MICRO-STAR INT'L CO.,LTD.		
Title		
DDR4 SODIMM A0		
Size	Document Number	Rev
Custom	MS-16Q3	0A
Date:	Monday, May 21, 2018	Sheet 8 of 62

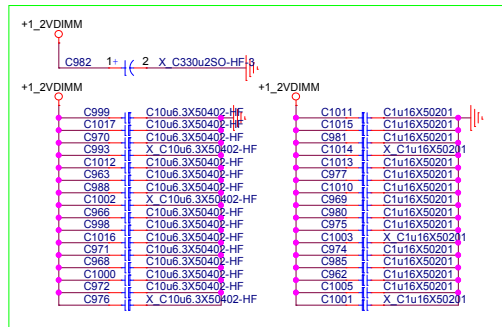
SODIMM_B0 (TOP-Standard)

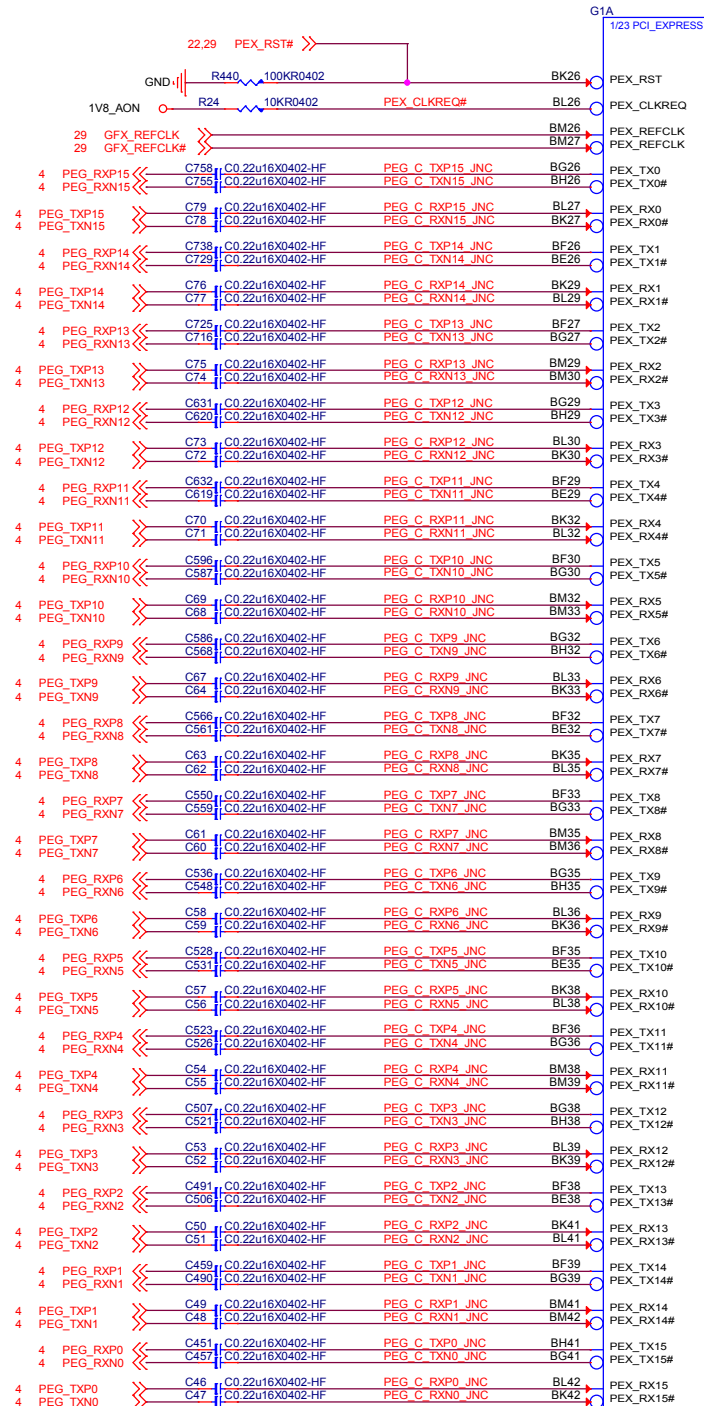


DDR4SODIMM-260PS_BLACK-HF-1
DDR4_SODIMM260P_H4_3
N13-2600230-L41

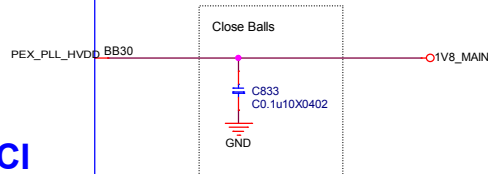
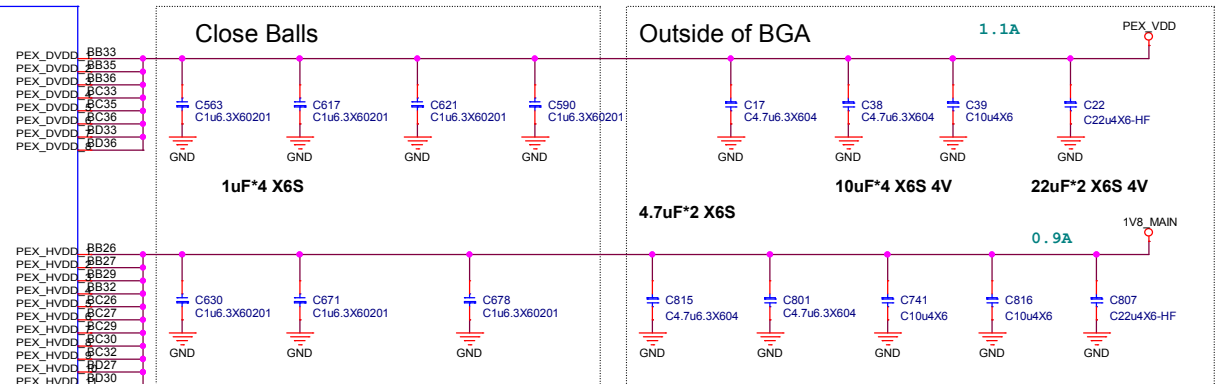


DDR4SODIMM-260PS_BLACK-HF-19
DDR4_SODIMM260P_H4_3
N13-2600230-L41

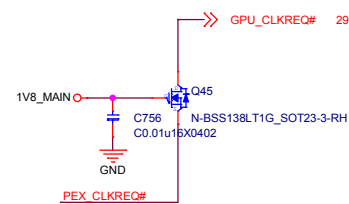




GPU PCI EXPRESS

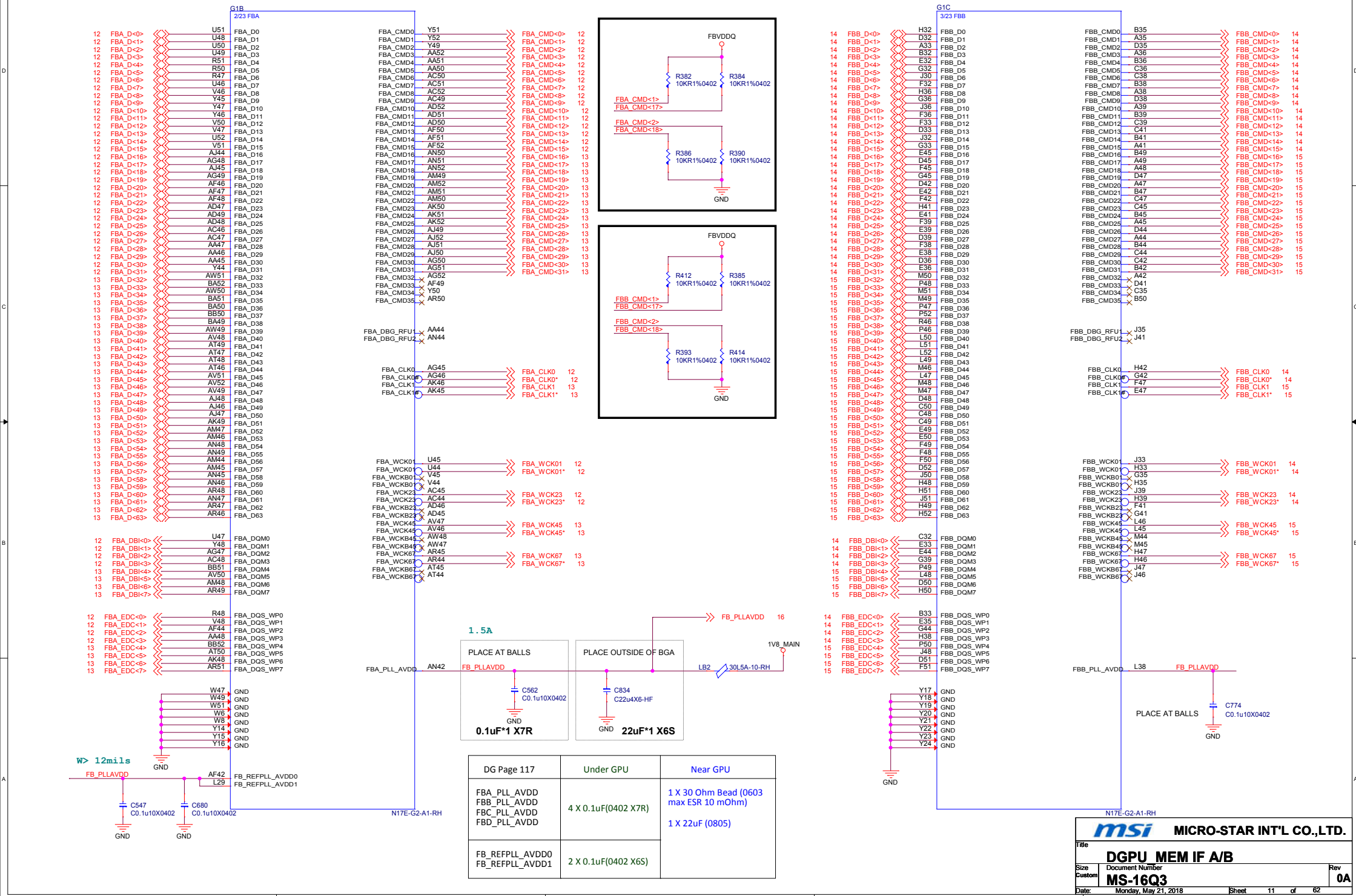


GPU CLK REQ#



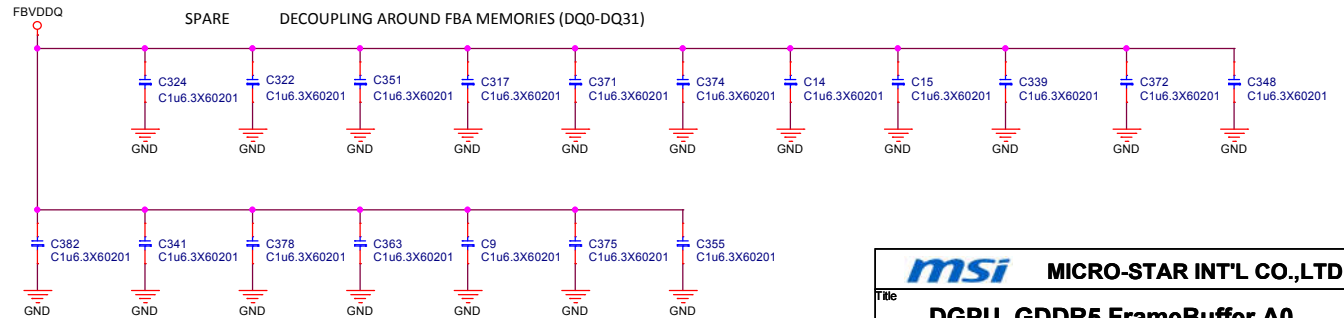
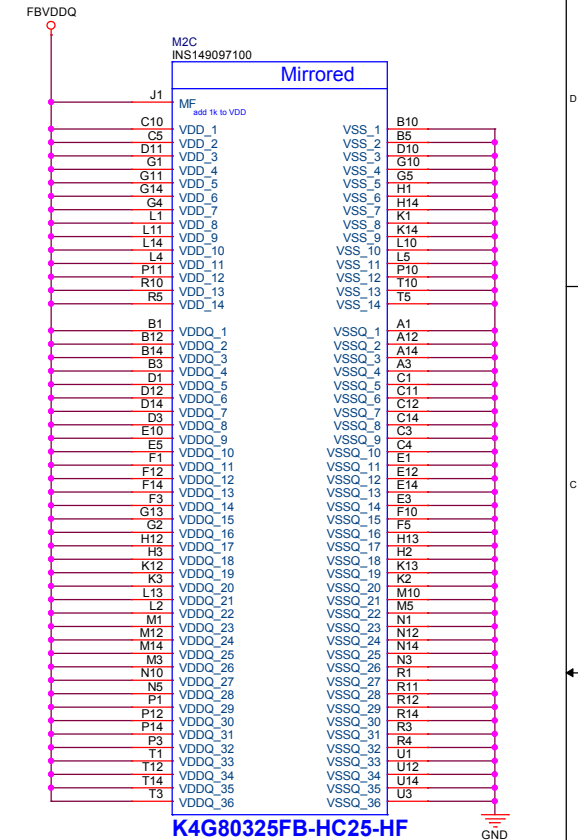
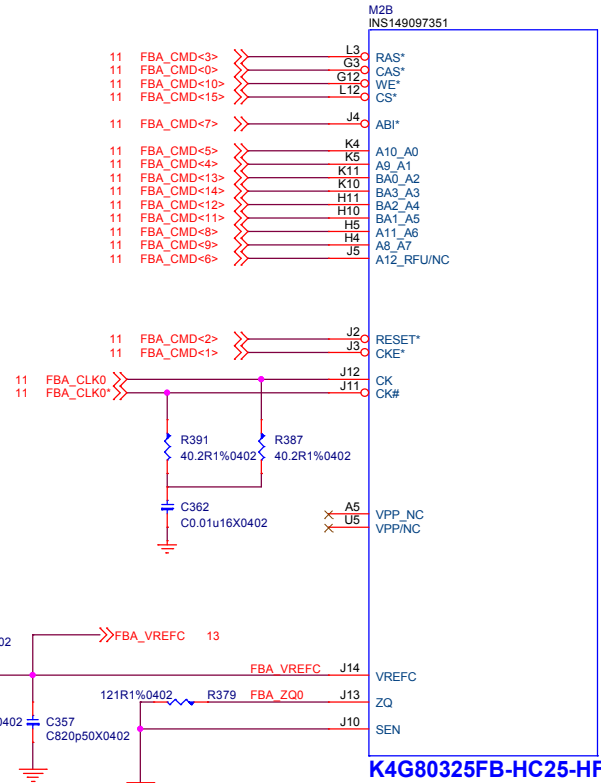
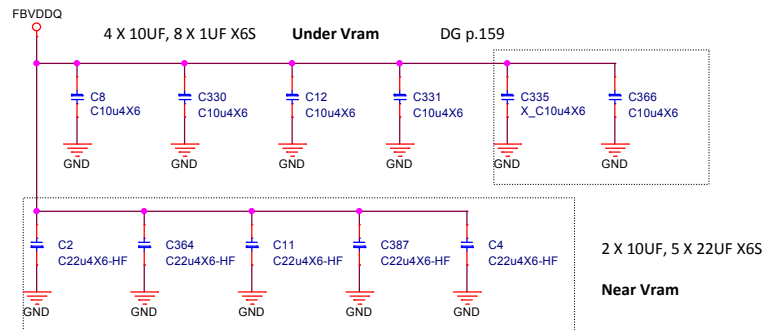
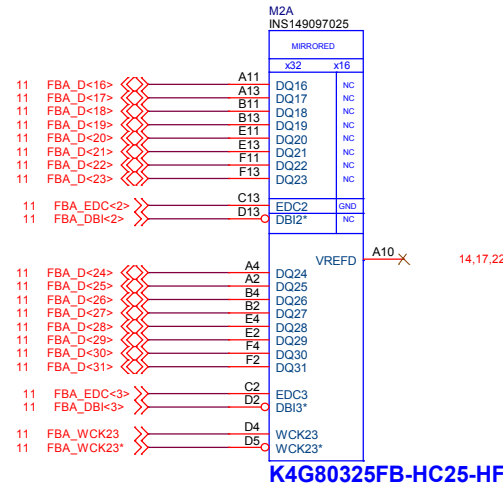
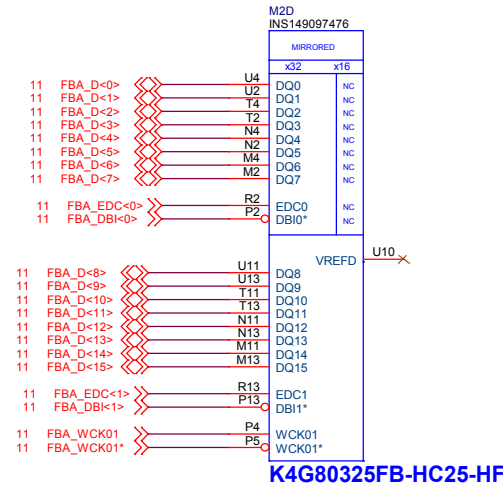
DG Page 117	Under GPU	Near GPU
PEX_HVDD	4 X 1uF(0402 X6S)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_DVDD	4 X 1uF(0402 X6S)	Near GPU: 2 X 4.7uF (0603) Midway btw GPU & VR: 1 X 10uF (0805) 1 X 22uF (0805)
PEX_PLL_HVDD	1 X 0.1uF(0402)	

GPU Frame Buffer Partition A/B

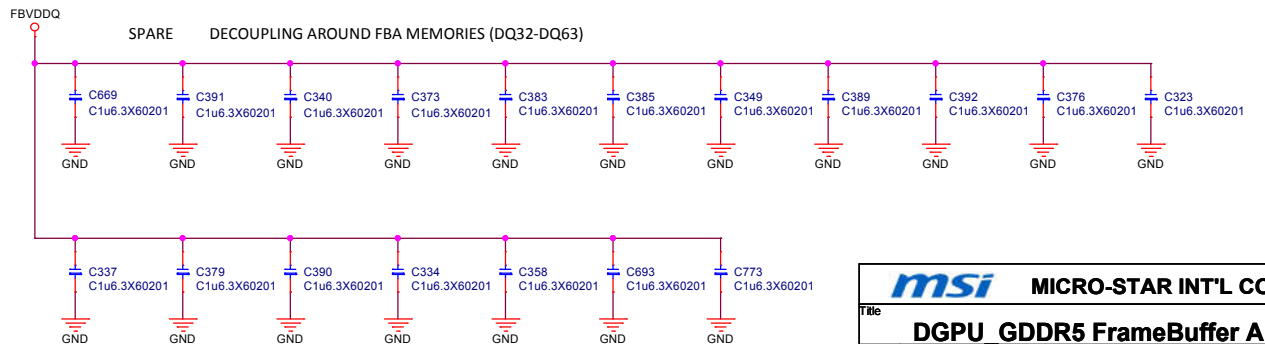
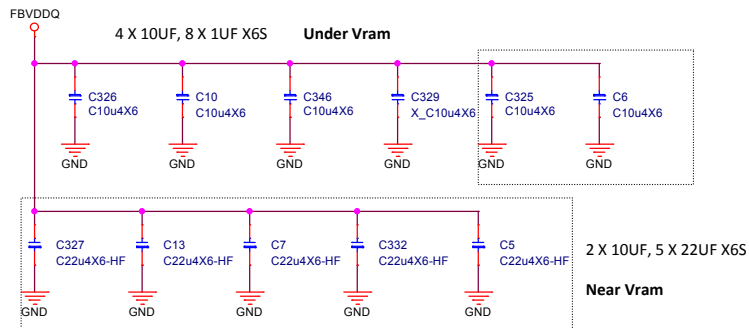
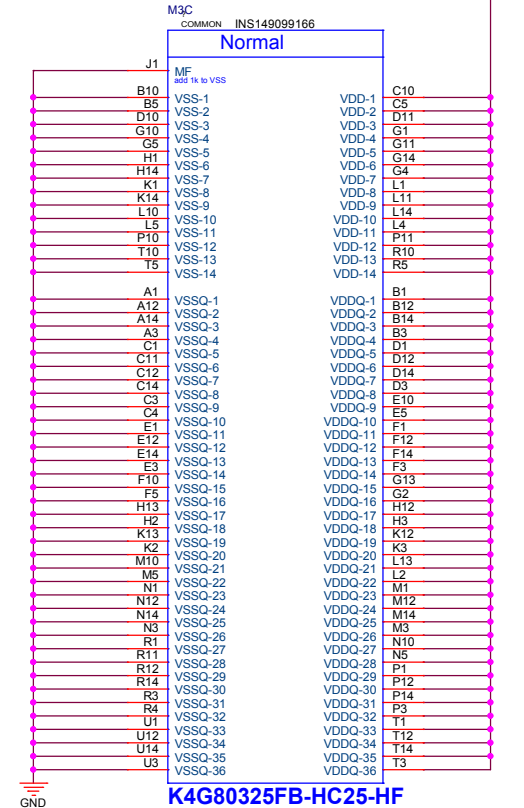
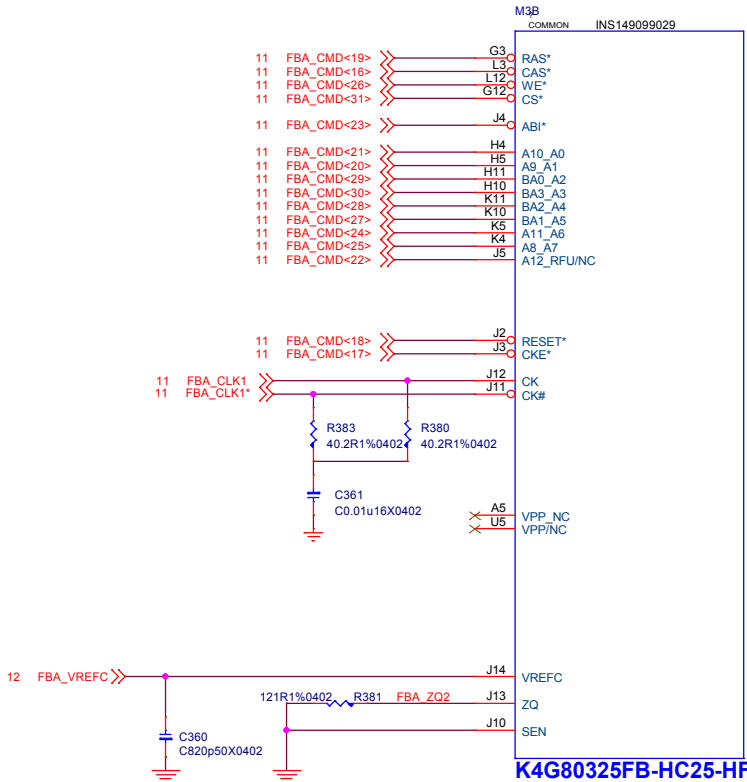
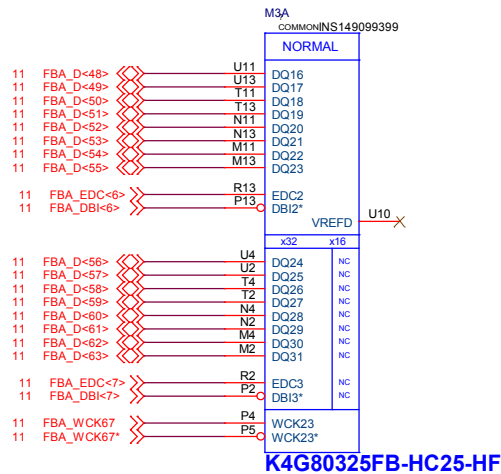
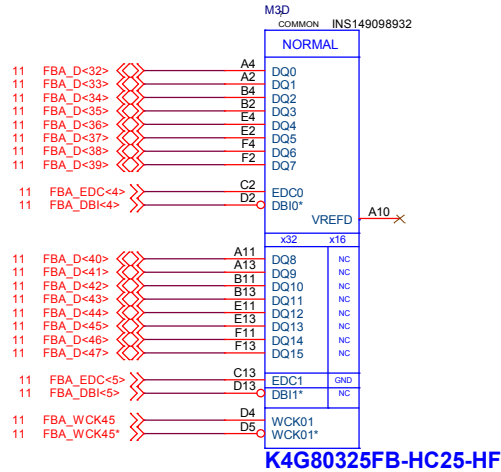


Hynix PN : M12-5GC2H05-H23 2G(64Mx32bit)
Samsung PN : M12-2032585-S02 2G(64Mx32bit)

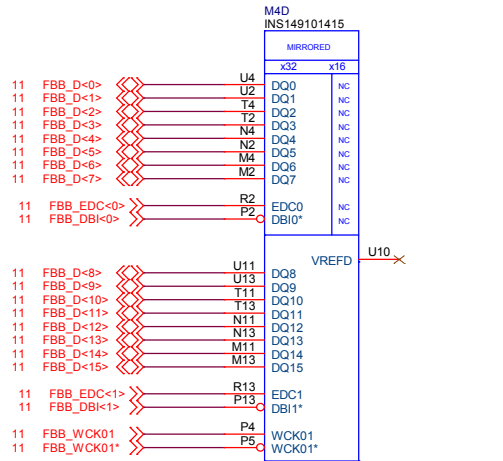
DGPU_GDDR5 FrameBuffer A0



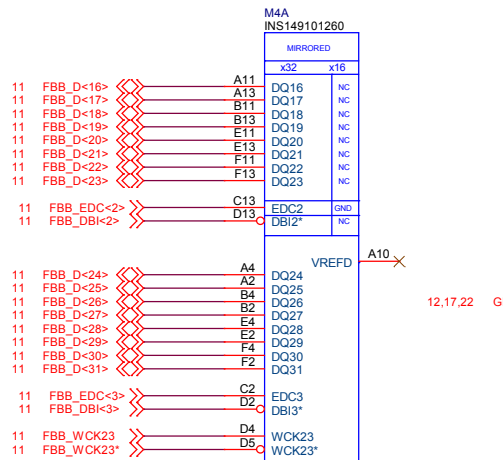
DGPU_GDDR5 FrameBuffer A1



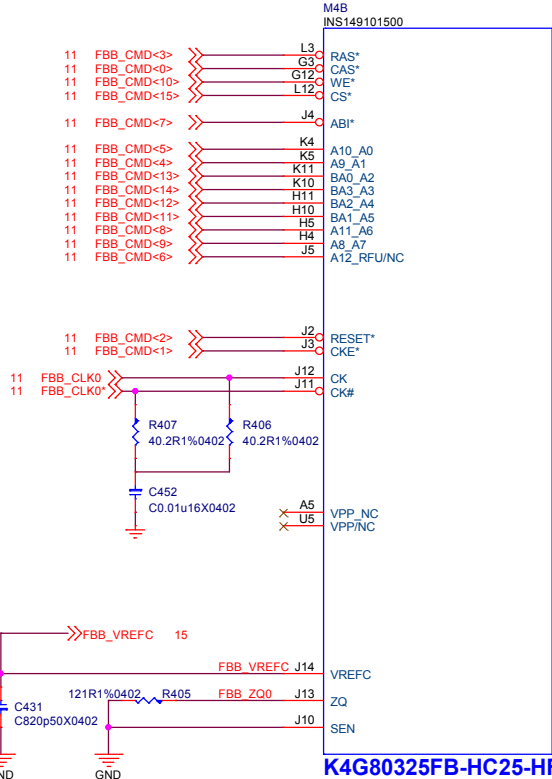
DGPU_GDDR5 FrameBuffer B0



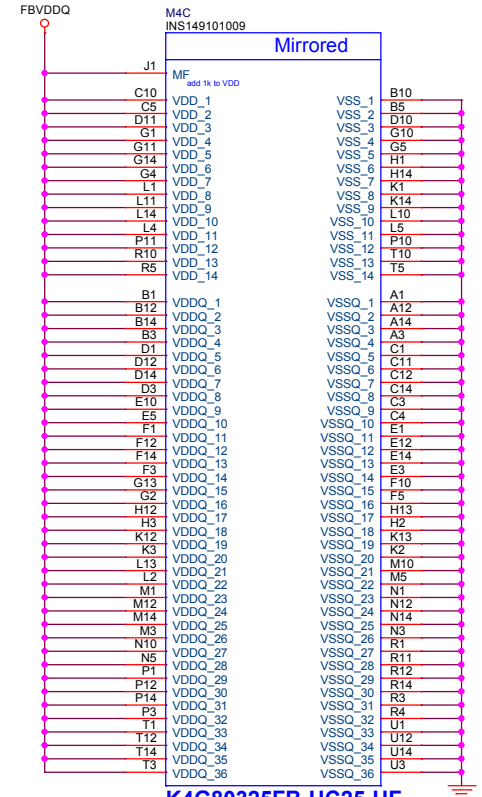
K4G80325FB-HC25-HF



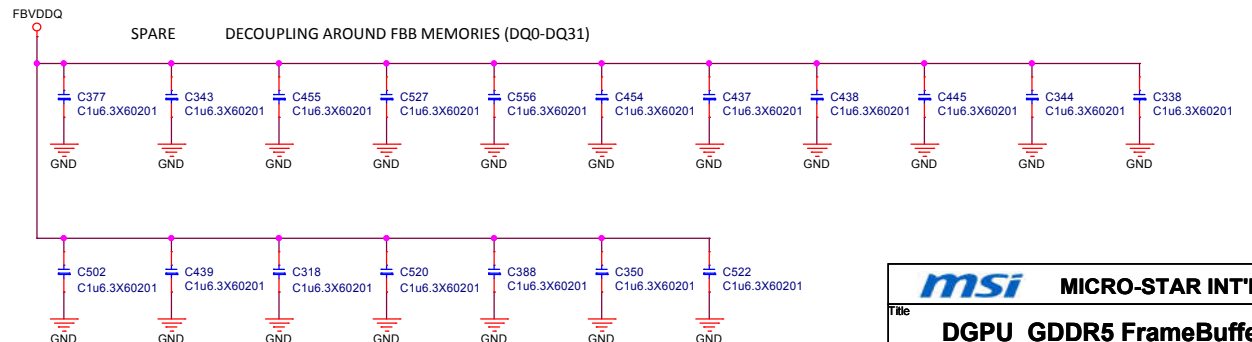
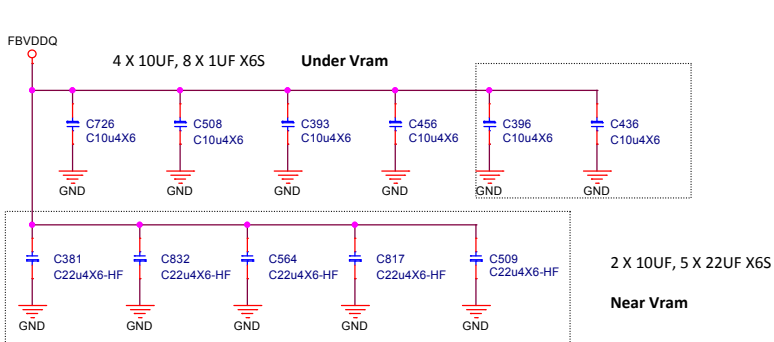
K4G80325FB-HC25-HF



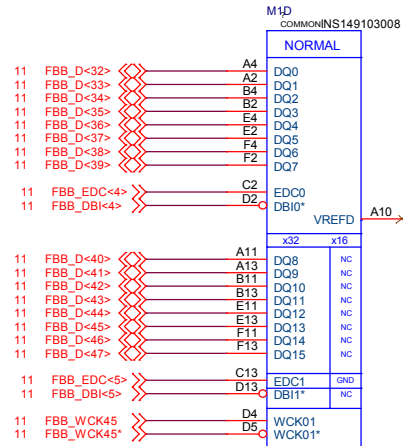
K4G80325FB-HC25-H



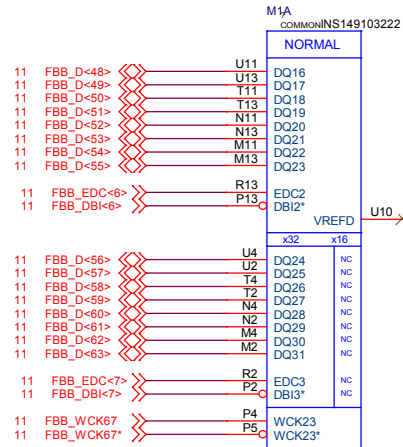
K4G80325FB-HC25-HF



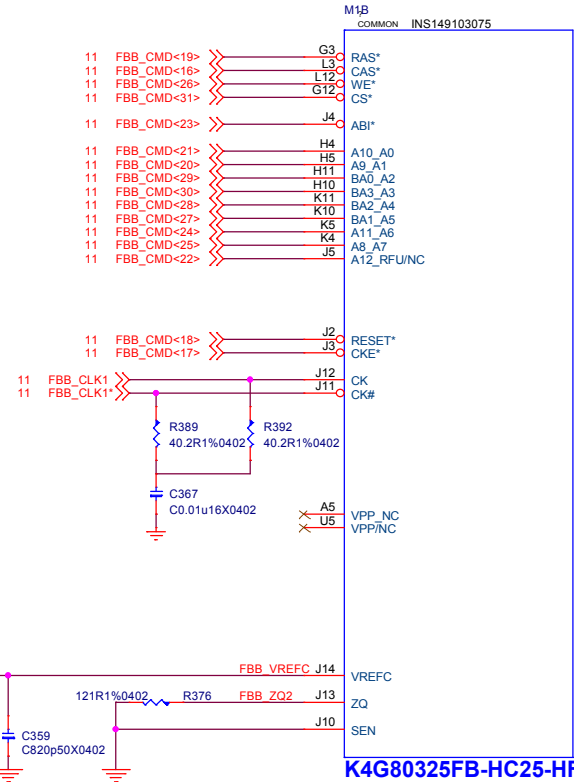
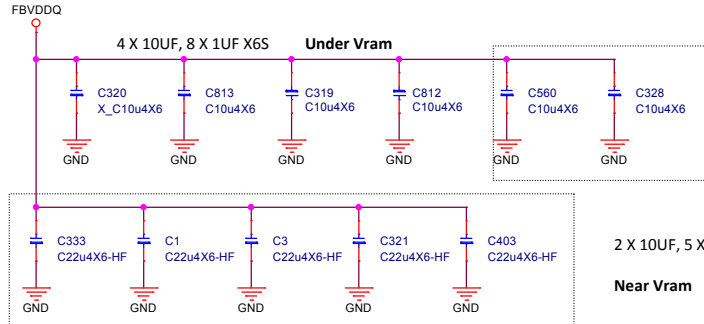
DGPU_GDDR5 FrameBuffer B1



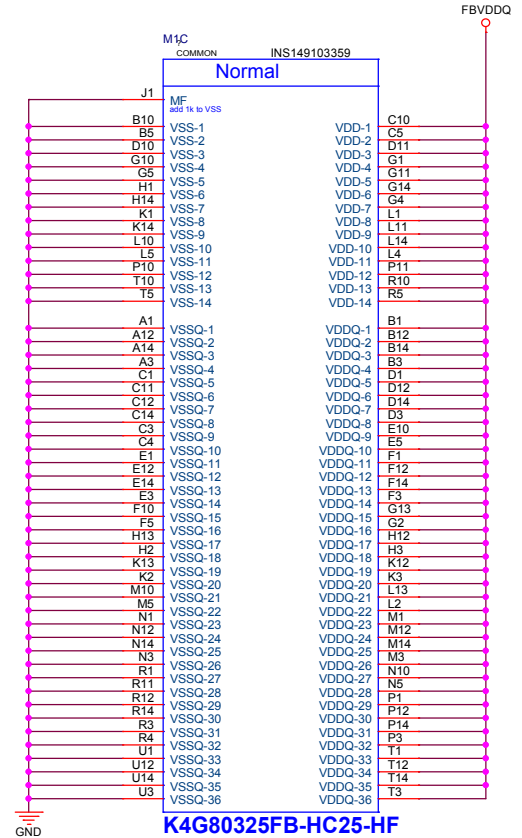
K4G80325FB-HC25-HF



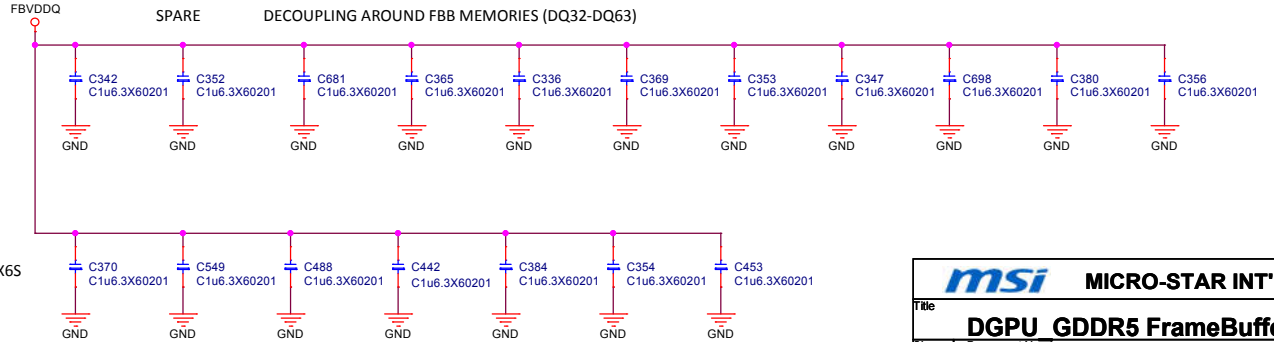
K4G80325FB-HC25-HF



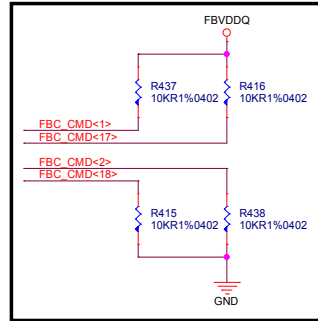
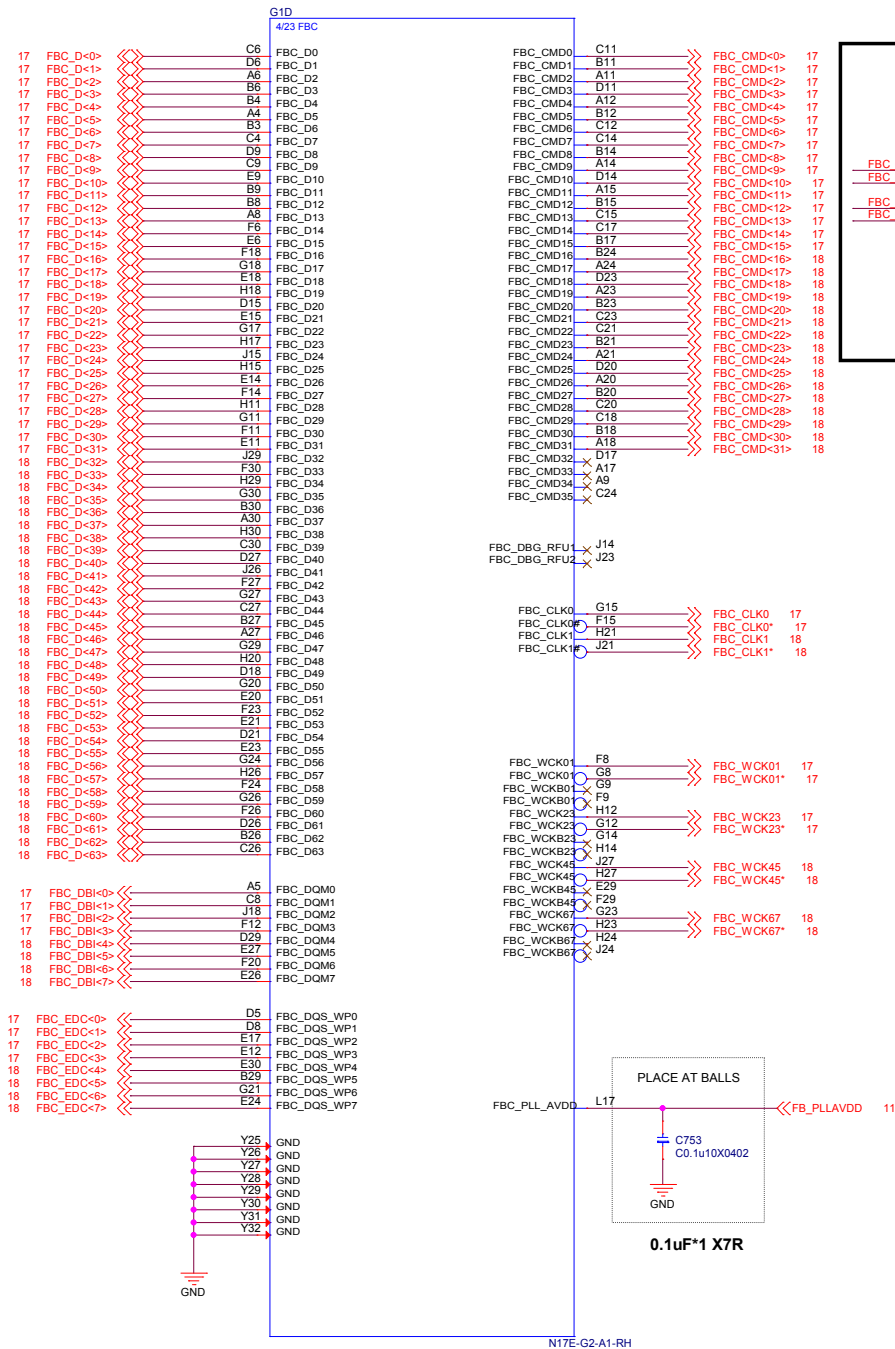
K4G80325FB-HC25-HF



K4G80325FB-HC25-HF

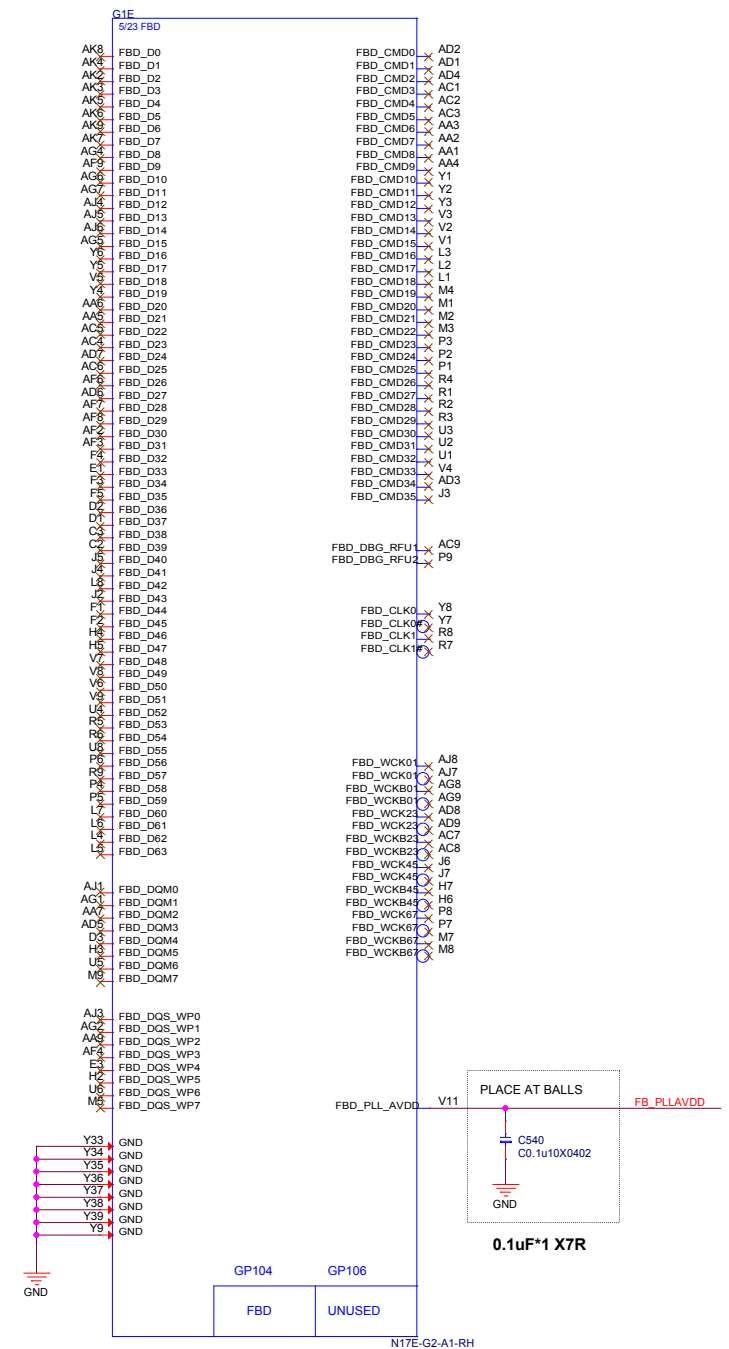


GPU Frame Buffer Partition C/D

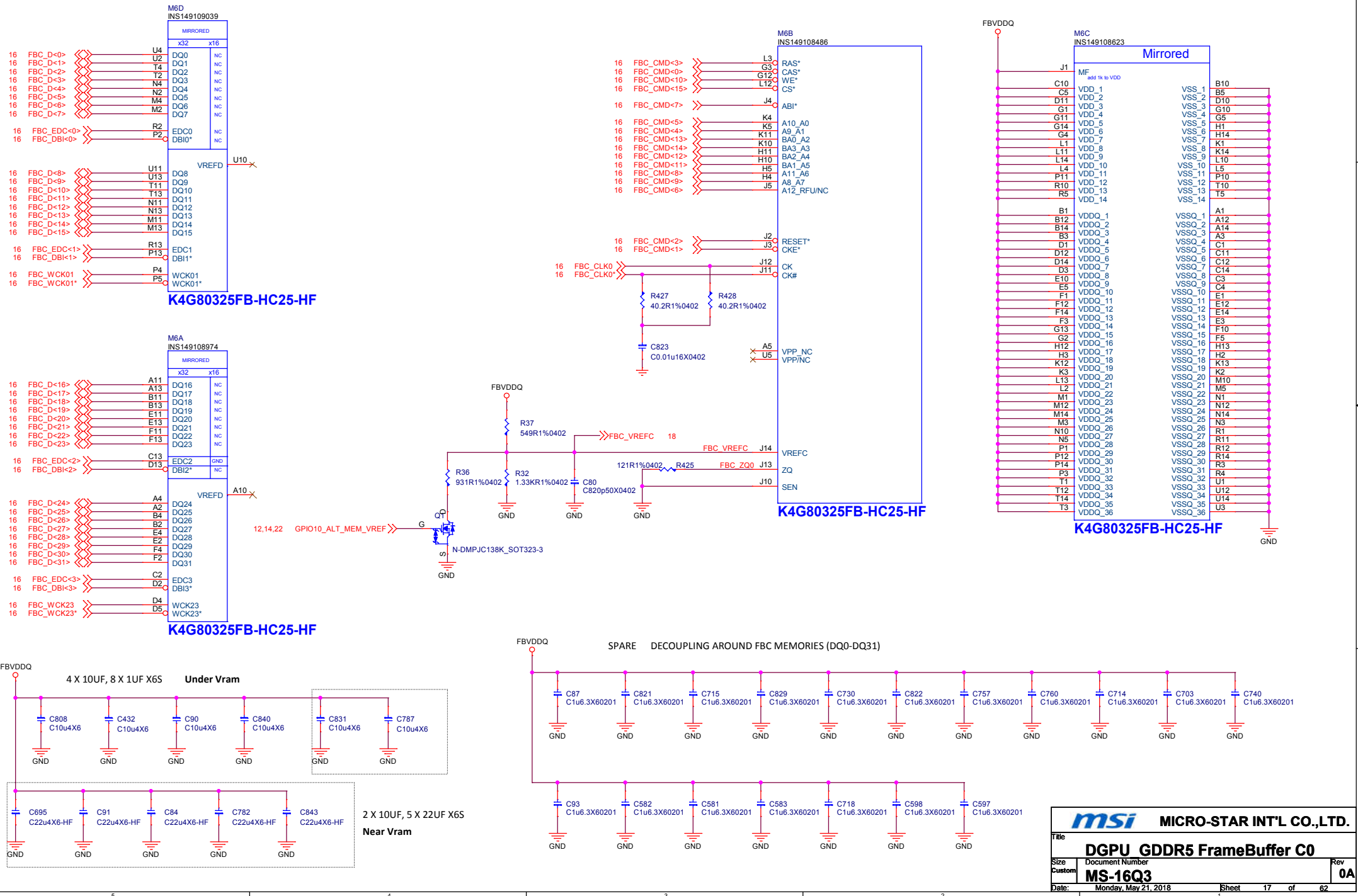


GDDR5 Mapping By GB4-256

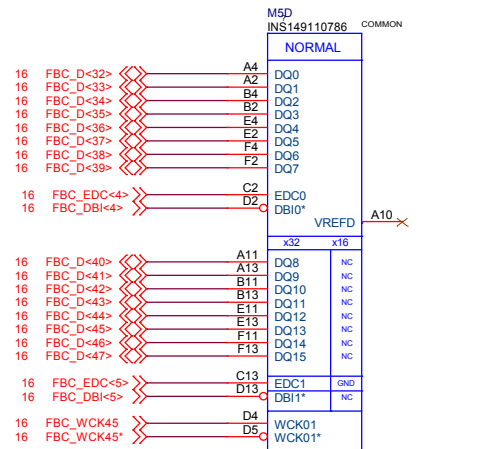
	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1 A9	
CMD5	A0 A10	
CMD6	A17 REFU	
CMD7	AB1*	
CMD8	A6 A11	
CMD9	A7 A8	
CMD10	WE*	
CMD11	A5 BA1	
CMD12	A4 BA2	
CMD13	A2 BA0	
CMD14	A3 BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1 A9
CMD21		A0 A10
CMD22		A17 REFU
CMD23		AB1*
CMD24		A6 A11
CMD25		A7 A8
CMD26		WE*
CMD27		A5 BA1
CMD28		A4 BA2
CMD29		A2 BA0
CMD30		A3 BA3
CMD31		CS*



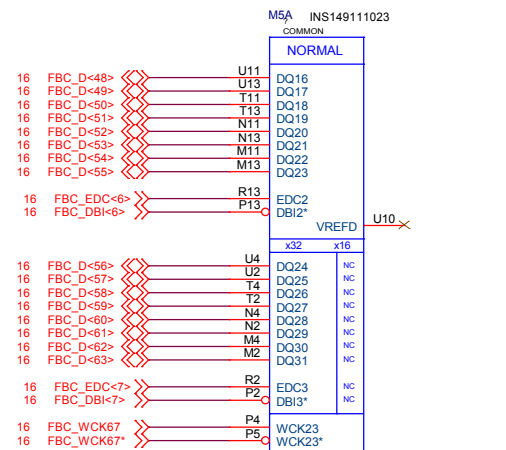
DGPU_GDDR5 FrameBuffer C0



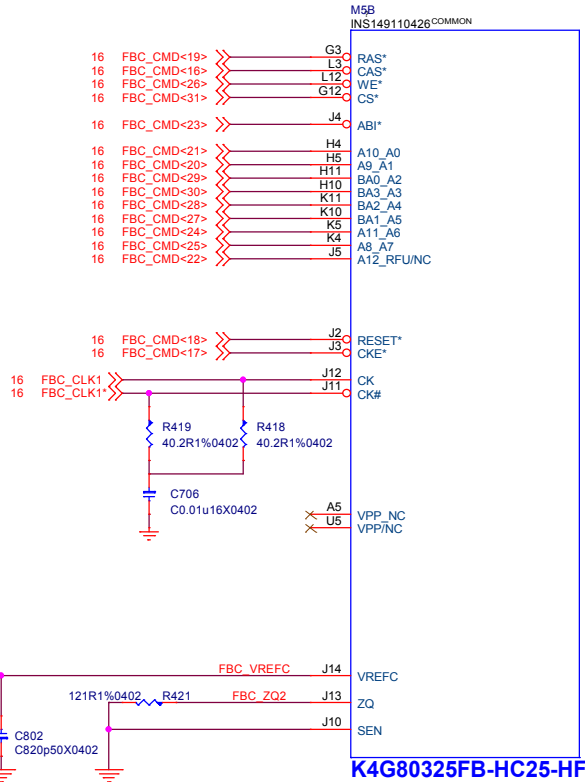
DGPU_GDDR5 FrameBuffer C1



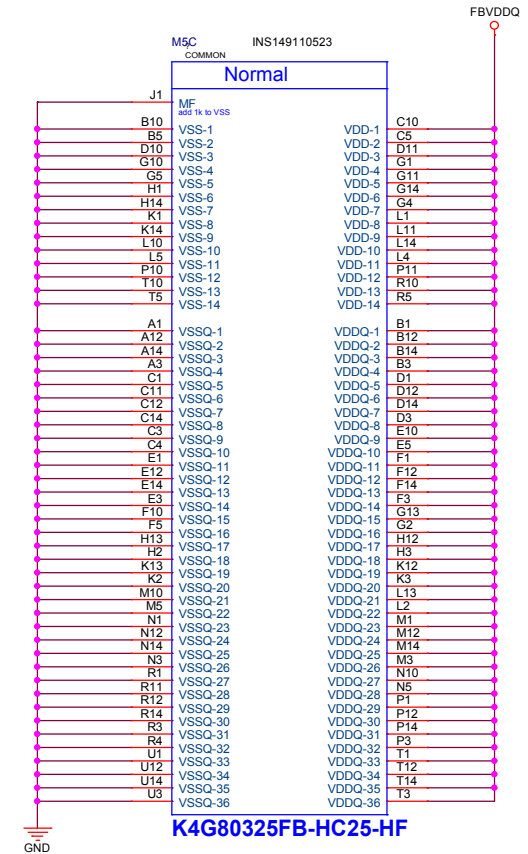
K4G80325FB-HC25-HF



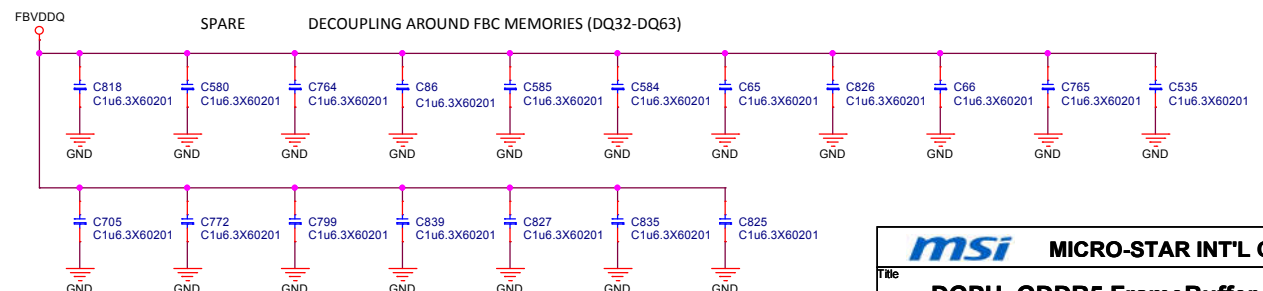
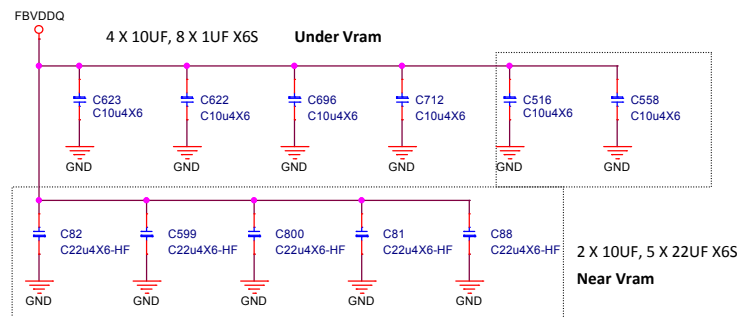
K4G80325FB-HC25-HF



K4G80325FB-HC25-HF

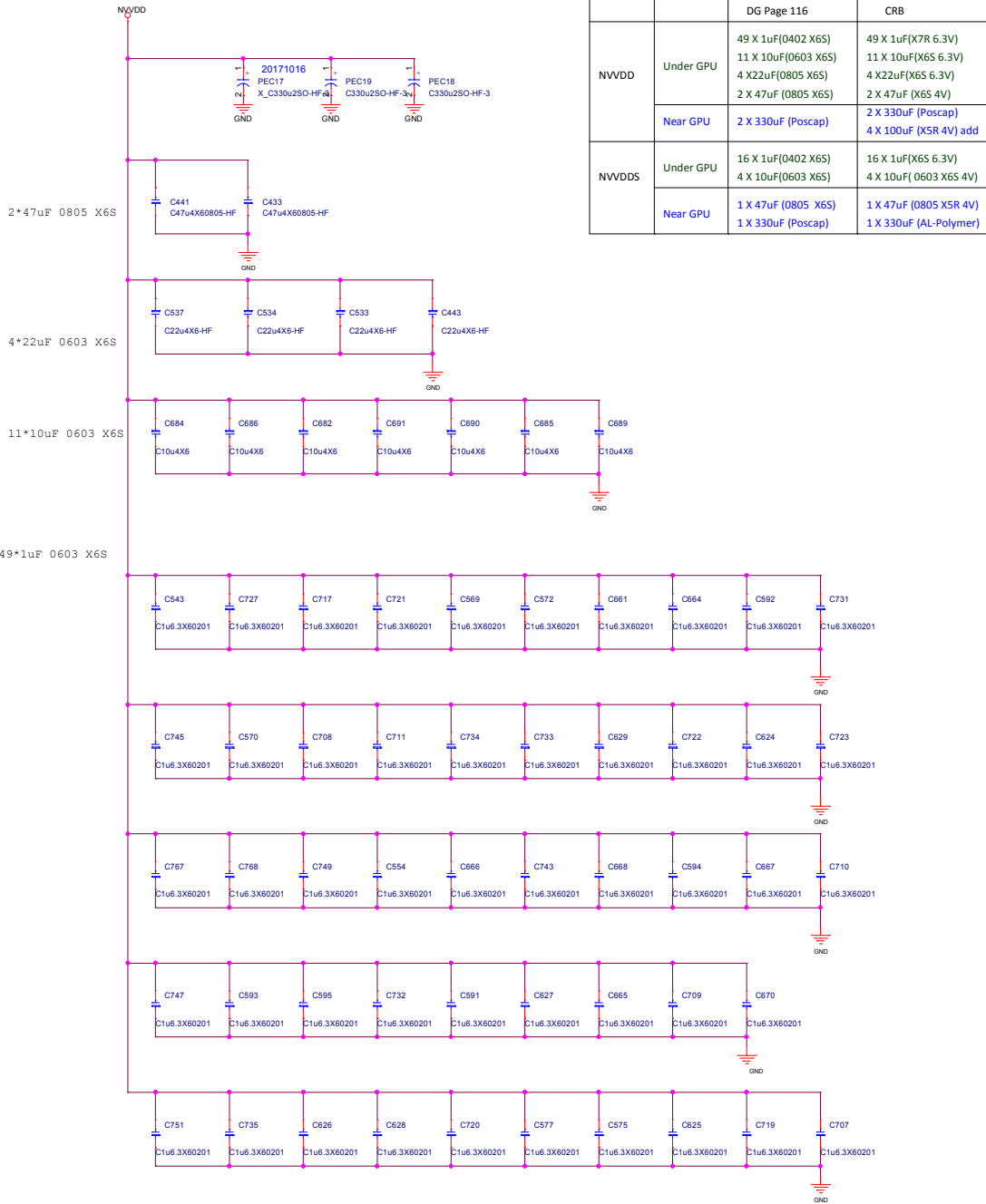


K4G80325FB-HC25-HF



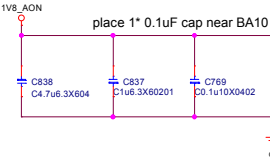
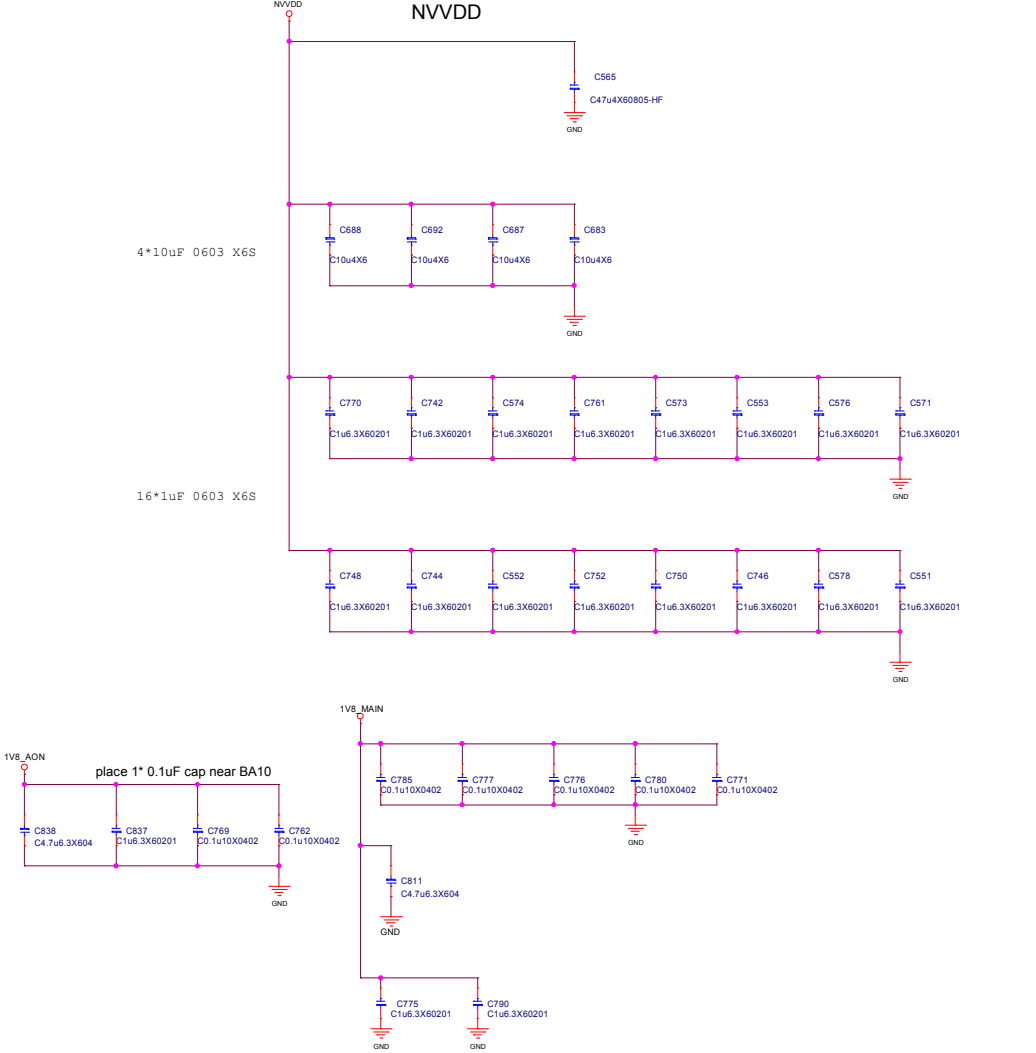
GPU DECOUPLING A

NVDD



		DG Page 116	CRB
NVDD	Under GPU	49 X 1uF(0402 X6S) 11 X 10uF(0603 X6S) 4 X22uF(0805 X6S) 2 X 47uF (0805 X6S)	49 X 1uF(X7R 6.3V) 11 X 10uF(X6S 6.3V) 4 X22uF(X6S 6.3V) 2 X 47uF (X6S 4V)
	Near GPU	2 X 330uF (Poscap)	2 X 330uF (Poscap) 4 X 100uF (X5R 4V) add
NVDDS	Under GPU	16 X 1uF(0402 X6S) 4 X 10uF(0603 X6S)	16 X 1uF(X6S 6.3V) 4 X 10uF (0603 X6S 4V)
	Near GPU	1 X 47uF (0805 X6S) 1 X 330uF (Poscap)	1 X 47uF (0805 X5R 4V) 1 X 330uF (AL-Polymer)

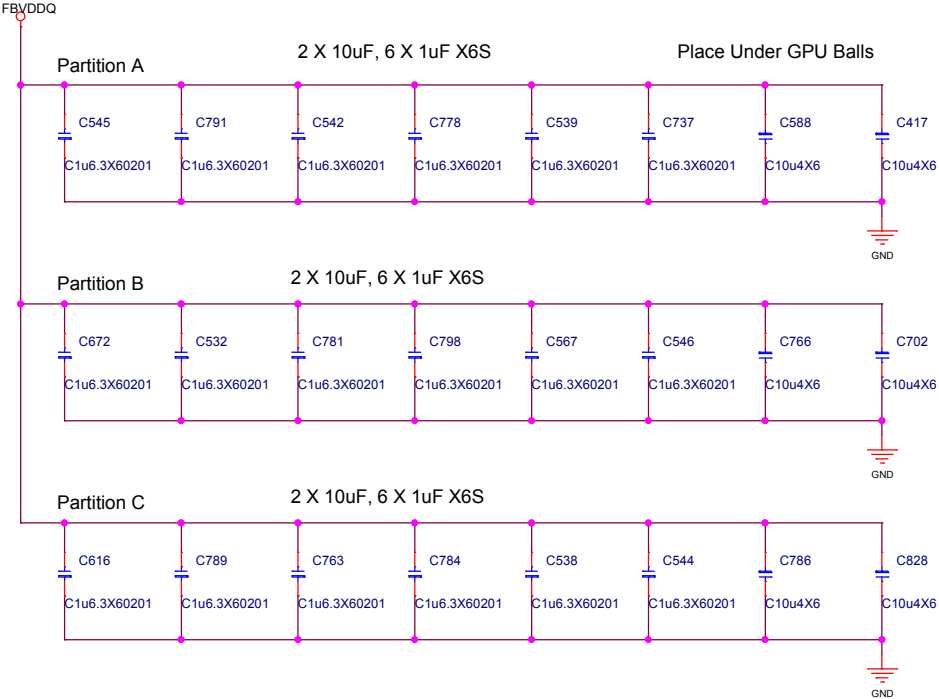
NVDD



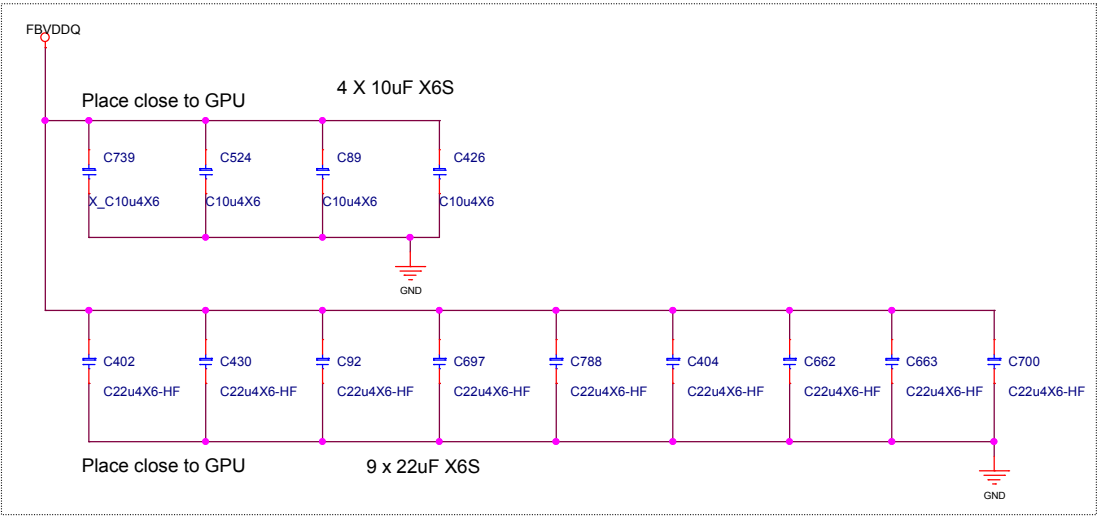
		DG Page 117	CRB
1V8_MAIN	Under GPU	7 X 0.1uF(0402)	7 X 0.1uF(0402 X7R)
	Near GPU	3 X 1uF (0402) 3 X 4.7uF (0603)	3 X 1uF (0603 X7R) 3 X 4.7uF (0603 X6S)
1V8_AON	Under GPU	2 X 0.1uF(0402)	2 X 0.1uF(0402 X7R)
	Near GPU	1 X 1uF (0402) 1 X 4.7uF (0603)	1 X 1uF (0603 X7R) 1 X 4.7uF (0603 X6S)

GPU DECOUPLING B

FBVDDQ

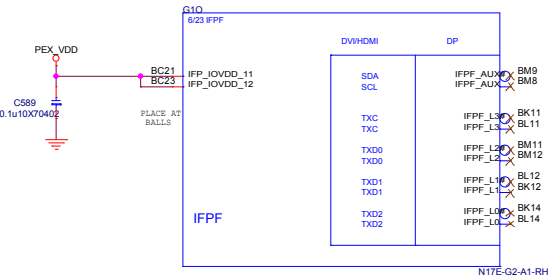
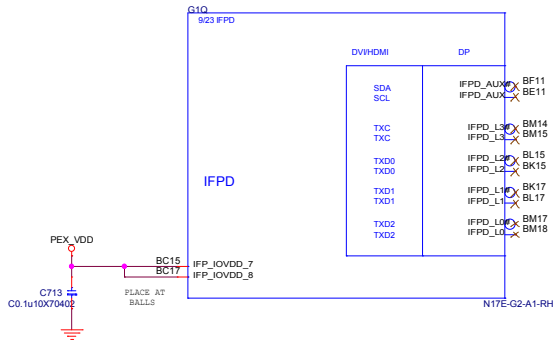
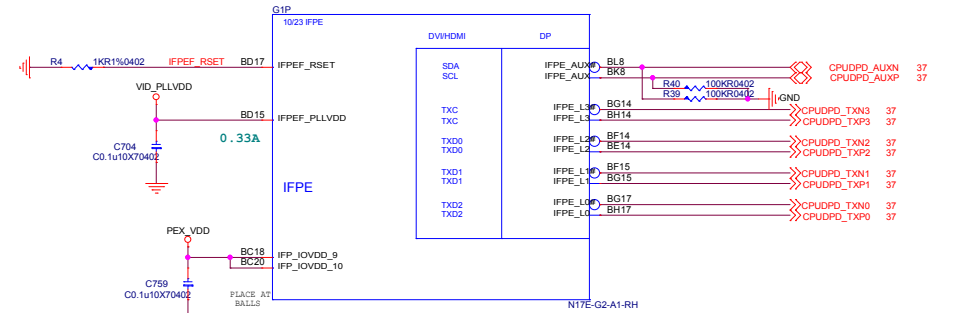
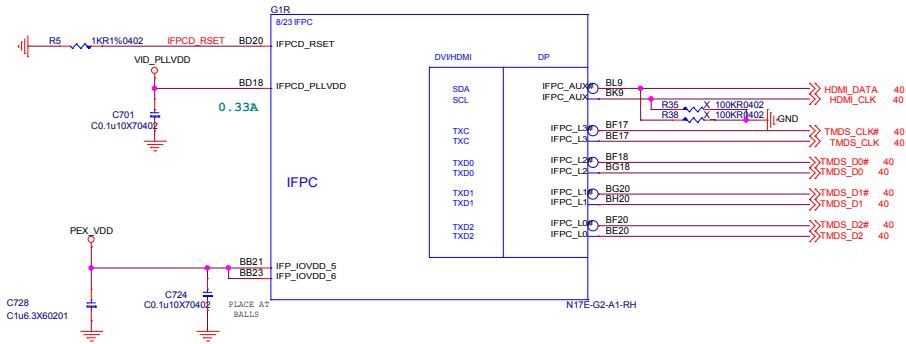
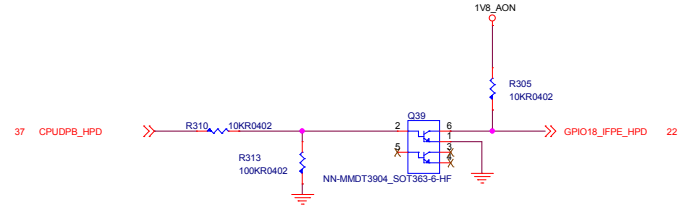
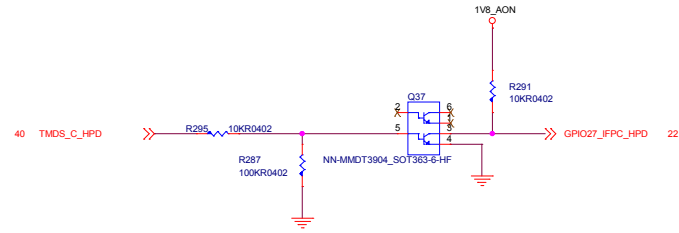
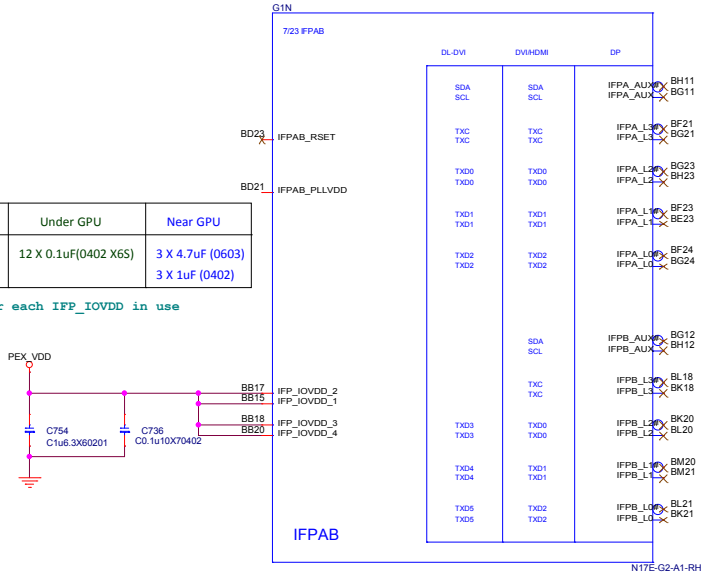


		DG Page 116	CRB
FBVDDQ (GPU side)	Under	24 X 1uF(0402 X6S) 5 X 10uF(0603 X6S)	24 X 1UF(0402 X6S 6.3V) 5 X 10uF(X6S 4V)
	Near	7 X 10uF(0603 X6S) 9 X 22uF(0603 X6S)	7 X 10uF(0603 X6S 4V) 9 X 22UF(0603 X6S 4V)

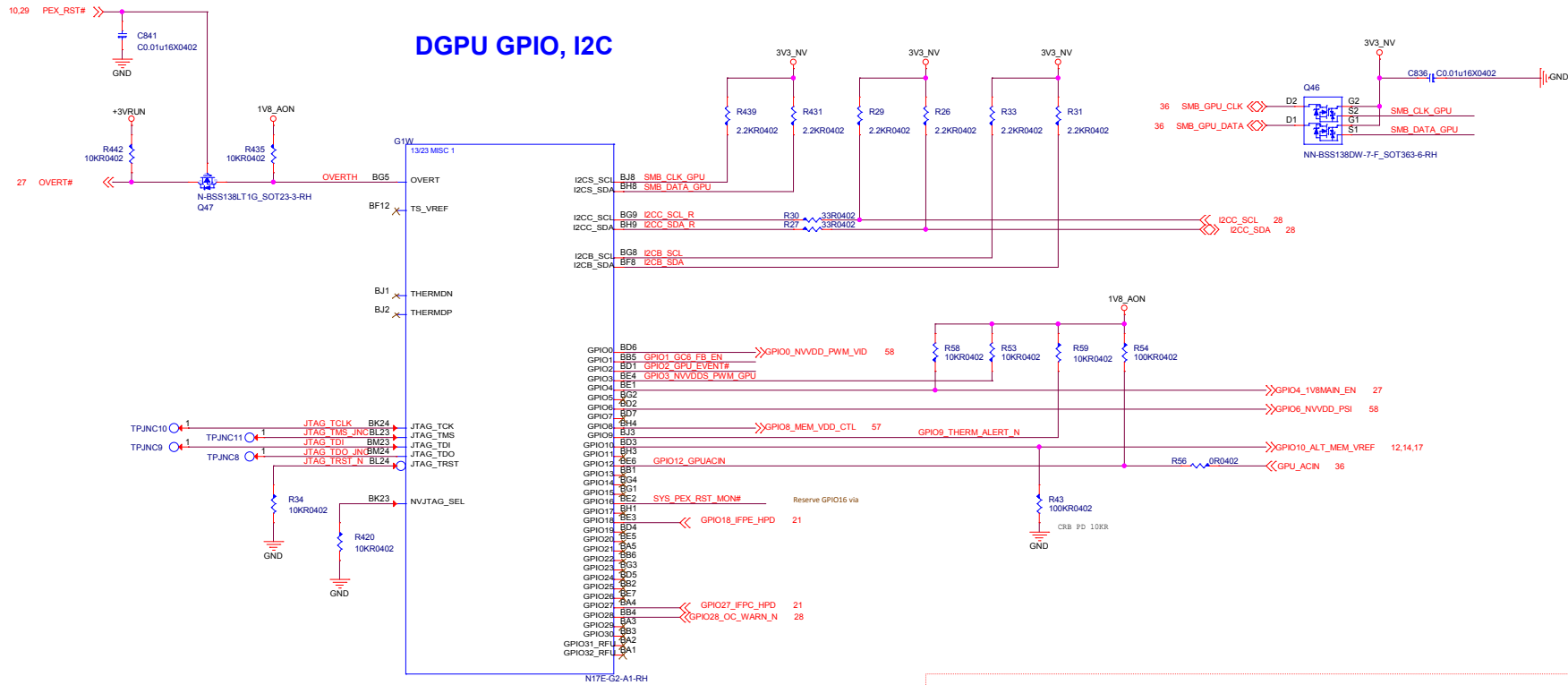


DG Page 117	Under GPU	Near GPU
IFP_IOVDD	12 X 0.1uF(0402 X6S)	3 X 4.7uF (0603) 3 X 1uF (0402)

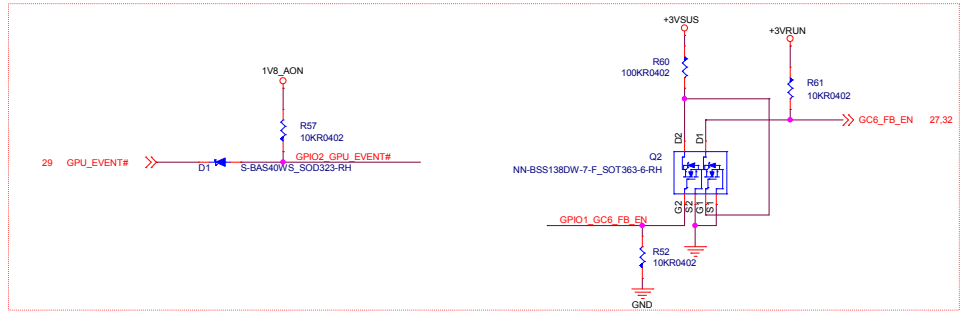
0.305A for each IFP_IOVDD in use



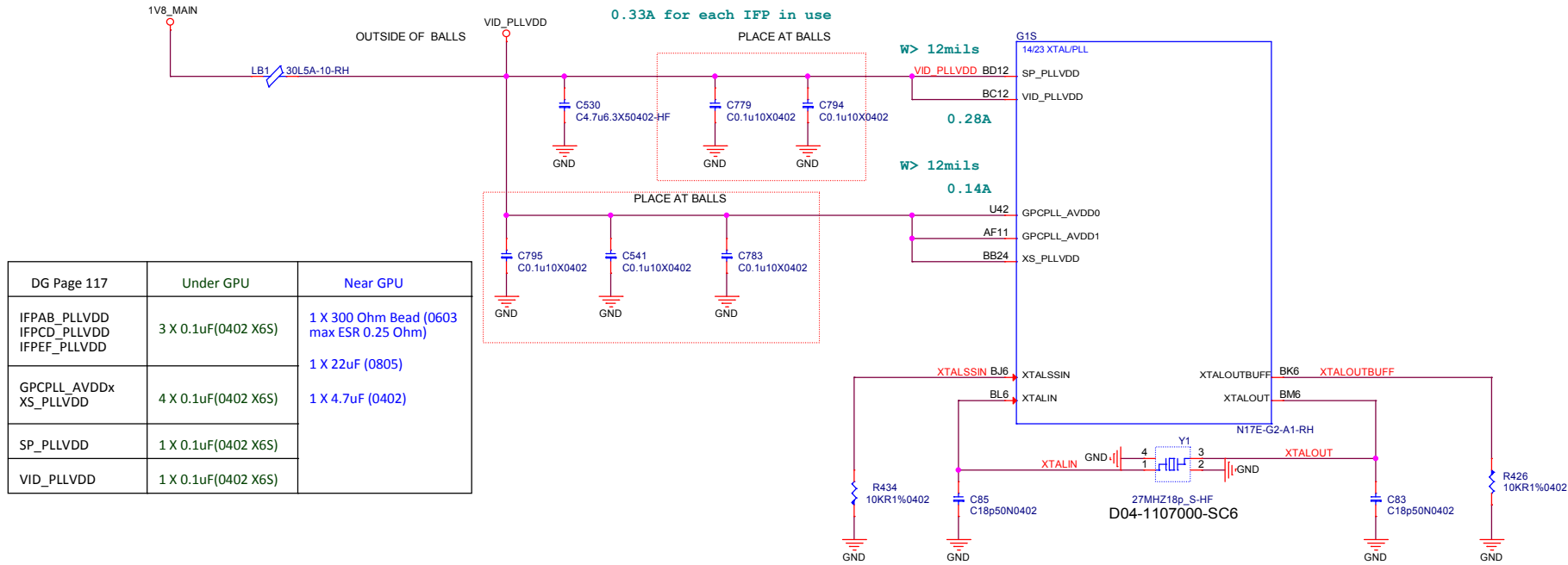
DGPU GPIO, I2C



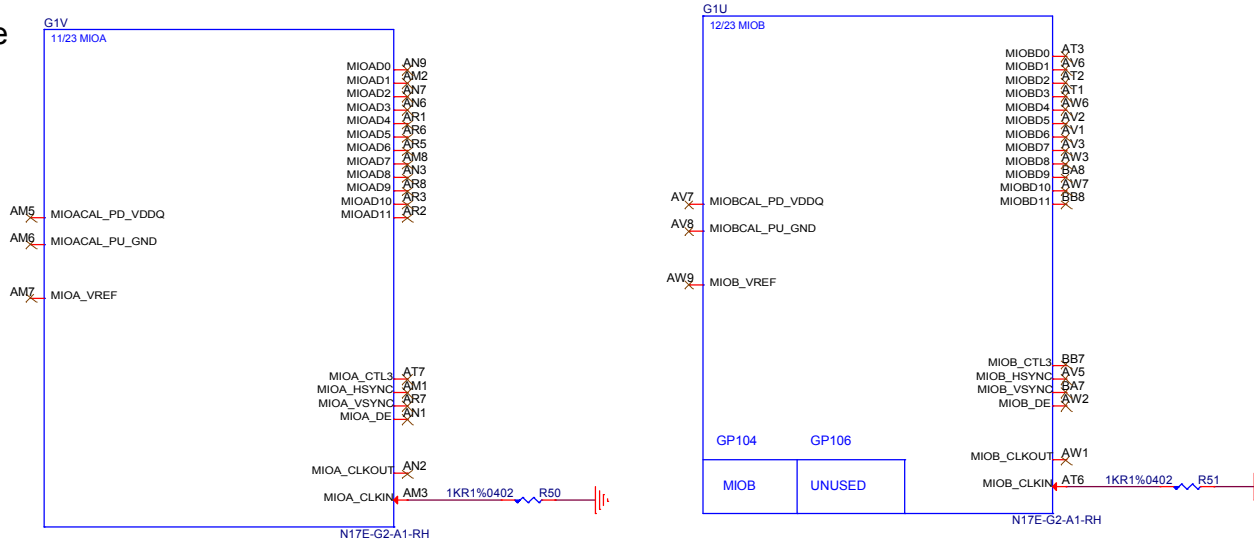
Pin Number	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to 1V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source, 10K pull-down
GPIO2	GC6M: GPU_EVENT#/WAKE#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8_AON
GPIO3	NVVDDS_PWM	O	PWM output to control the NVVDDS power supply	0 to 1V8 output
GPIO4	GC6M:1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8_AON
GPIO5	FRM_LCK#	I	Active low Fram Lock	OD, 10K pull-up to 1V8_AON
GPIO6	NVVDD_PSI#/NVVDDS_PSI#	O	Phase shedding	10K pull-up to 1V8_AON
GPIO7	LCD_BL_PWM	O	Panel Backlight enable control signal to turn on a logo LED	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT#	I/O	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VDD; Quadro: Power_Brake#	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	
GPIO14	HPD_IFPA#	I	Hot Plug Detect for IFPA	Inverted input
GPIO15	HPD_IFPB#	I	Hot Plug Detect for IFPB	Inverted input
GPIO16	GC6M: SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 1V8_AON
GPIO17	HPD_IFPD#	I	Hot Plug Detect for IFPD	Inverted input
GPIO18	HPD_IFPE#	I	Hot Plug Detect for IFPE	Inverted input
GPIO19	3DVision/STEREO	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE	I/O		
GPIO21	RASTER_SYNC0	I/O	Input when master GPU or Output when Slave GPU	100K pull-down
GPIO22	SWAP_RDY0 or SWAPRDY_IN	I/O	SLI Swap Ready Out	
GPIO23	GC6M: GPU_PEX_RST_HOLD#	I/O	GPU PCIe self-reset control	OD, 10K pull-up to gated 3V3
GPIO24	HPD_IFPF#	I	Hot Plug Detect for IFPF	Inverted input
GPIO25	Unused	I/O		
GPIO26	Unused	I/O		
GPIO27	HPD_IFPC#	I	Hot Plug Detect for IFPC	Inverted input
GPIO28	OC_WARN/HT	I	Over current throttling trigger	10K pull-up to 1V8_AON
GPIO29	EDPC_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	Unused	I/O		

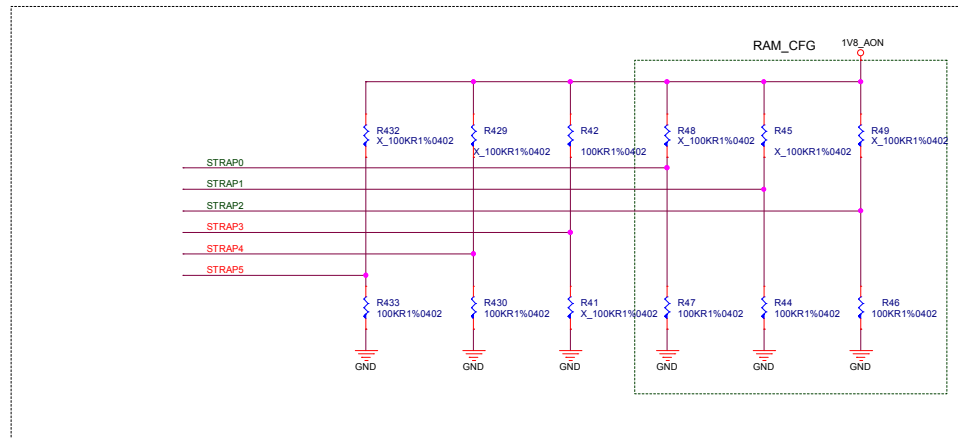
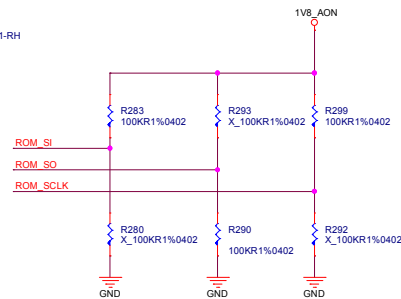
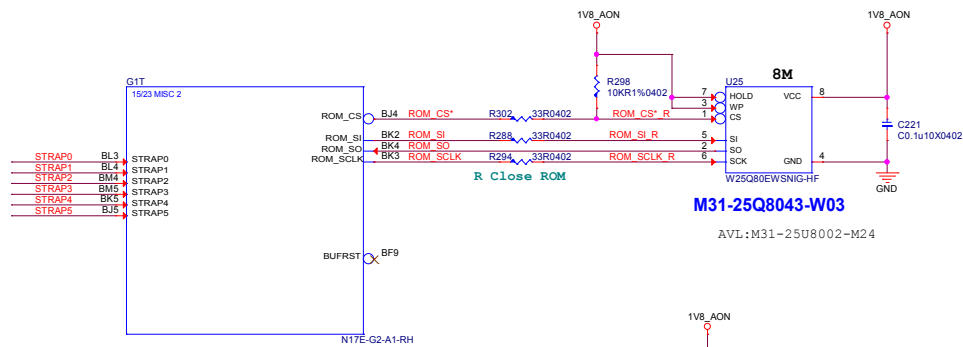


DGPU MIO & XTAL



Multi-use IO(MIO) Interface





V_TOP1		5010	256M*32
DEFAULT SETTING	<input checked="" type="checkbox"/>	M12-8032535-S02	
SAMSUNG	<input type="checkbox"/>	X_K4G80325FB-HC25-HF	
V_TOP2		5010	256M*32
MICRON	<input checked="" type="checkbox"/>	M12-2563215-M30	
	<input type="checkbox"/>	X_MT51J256M32HF-80-A-HF	

GPU1		B03-0N17E25-N08	X_GTX1060_N17E-G1-A1
GPU2		B03-0N17P95-N08	X_GTX1050_TI_N17P-G1-B-KC-A1
GPU3		B03-0N17P85-N08	X_GTX1050_TI_N17P-G1-B-KB-A1

STRAP2	STRAP1	STRAP0	RAMCFG[2:0]	
L	L	L	00000	V
L	L	H	00001	V
L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

256M*32
SAMSUNG 0X0
MICRON 0X1
HYNIX 0X2

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	V
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

SOR_EXPOSED :GPU AUDIO SETTING

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

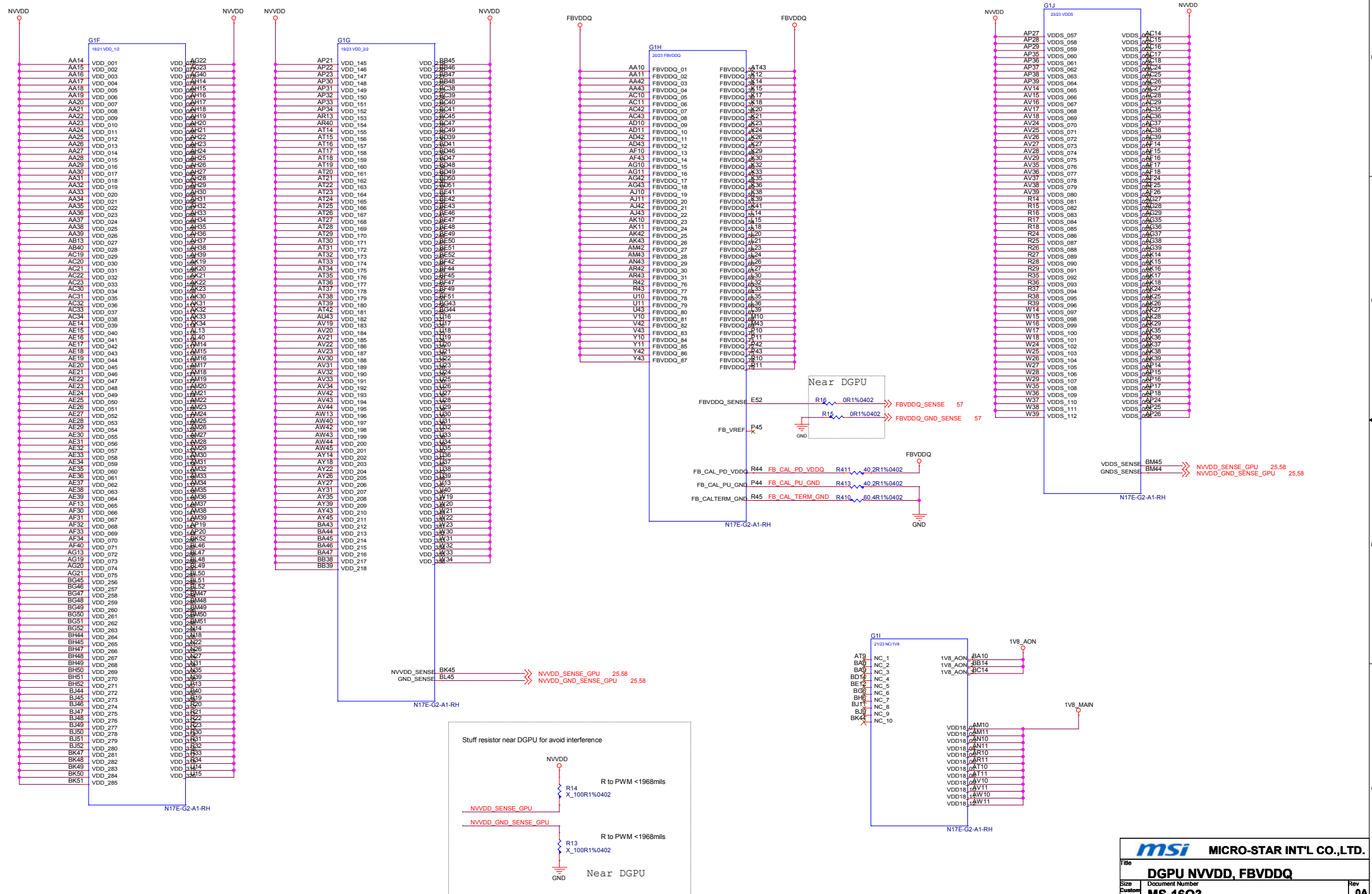
1:SMB_ALT_ADDR ENABLE (DUAL GPU)
0:SMB_ALT_ADDR DISABLE (SINGLE GPU)

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

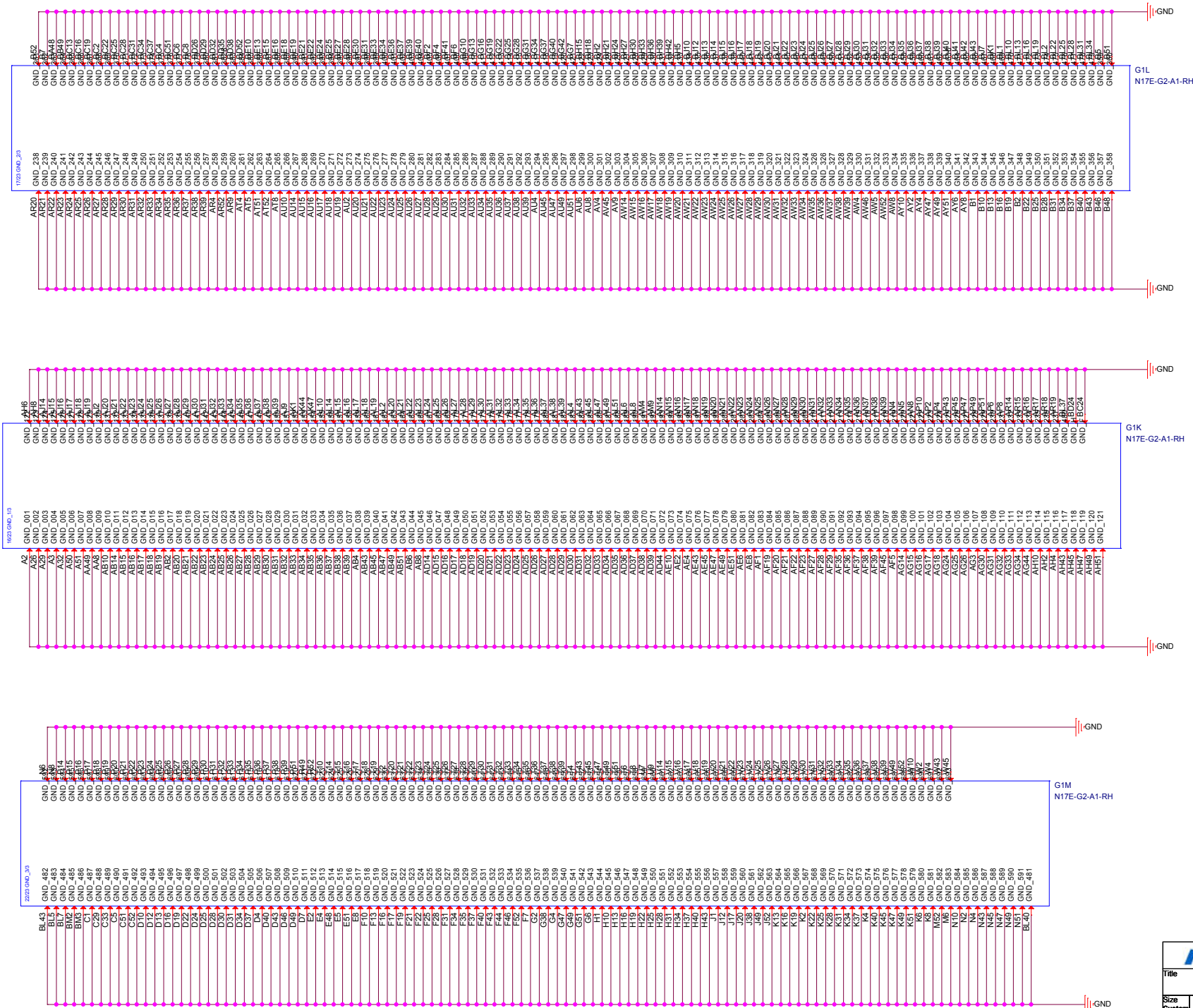
1:PCIE_CFG LOW SWING POWER
0:PCIE_CFG HIGH SWING POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

GPU NVVDD, FBVDDQ



DGPU GND

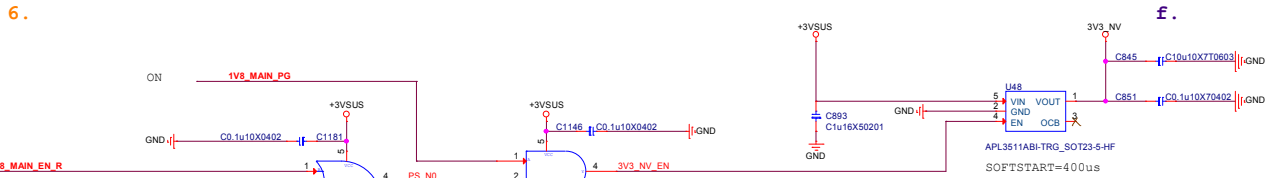
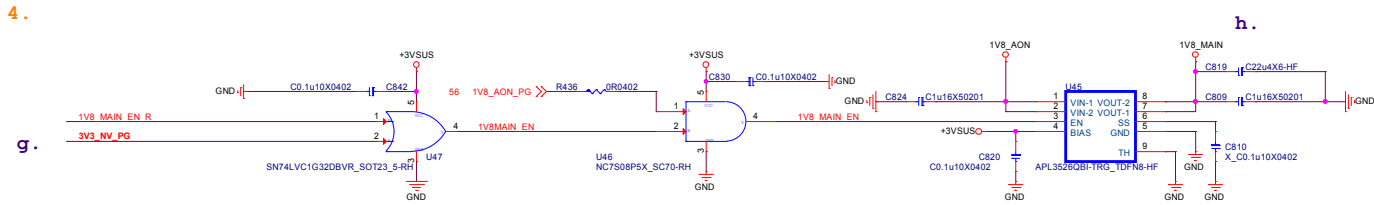
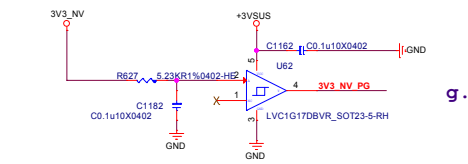
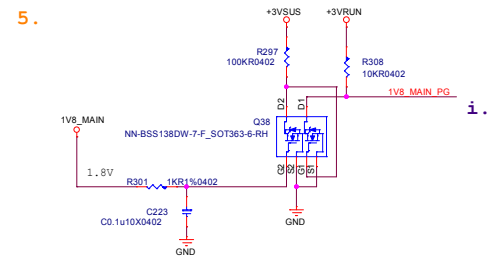
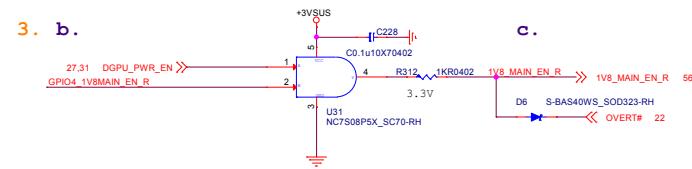
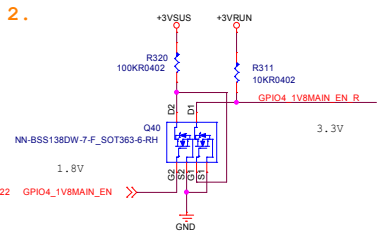
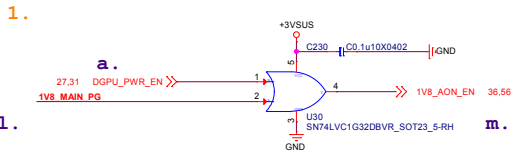


Power on = 1V8_AON -> 1V8_MAIN -> 3V3_NV -> NVVDD -> PEX_VDD -> FBVDDQ -> DGPUPWRGD

Power off = DGPUPWREN -> (PEX_VDD -> NVVDDQ -> 3V3_NV) -> FBVDDQ -> 1V8_MAIN -> 1V8_AON

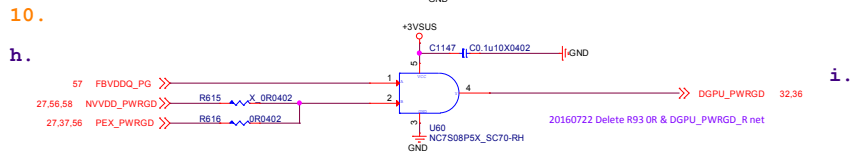
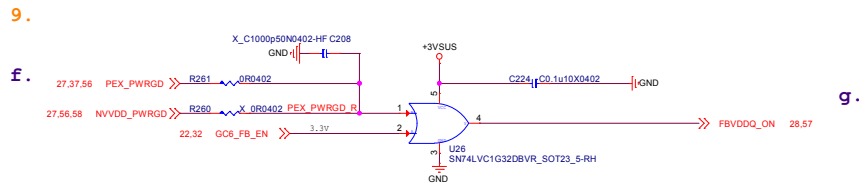
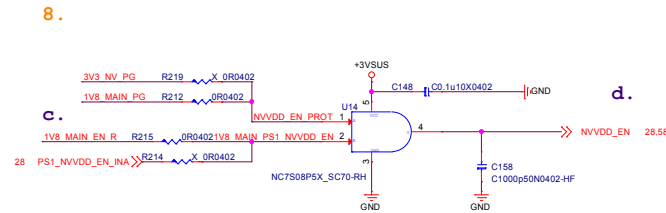
The ramp time for any rail must be more than 40us and is recommended to be less than 2ms
From 1V8_MAIN_EN to PEX_VDD must NOT exceed 4ms

nVIDIA Power Sequence Control

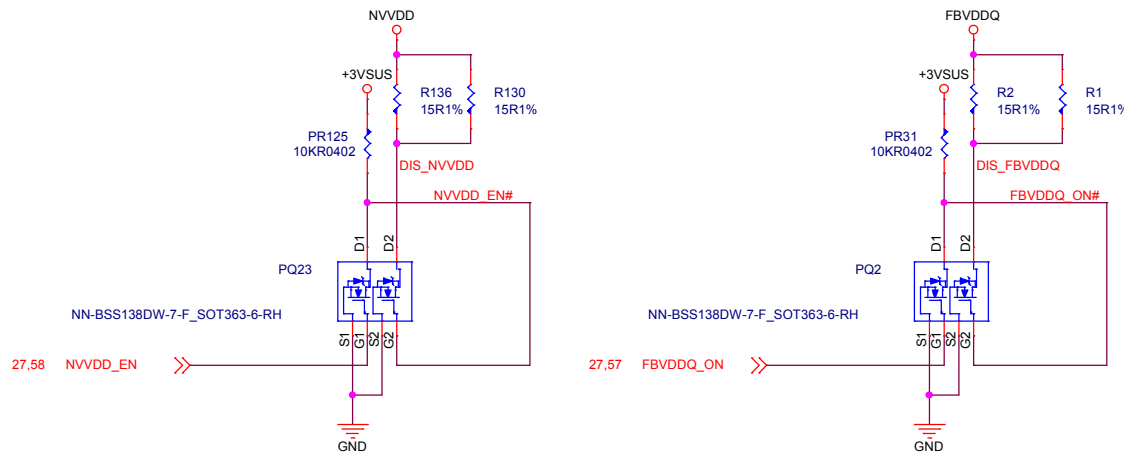
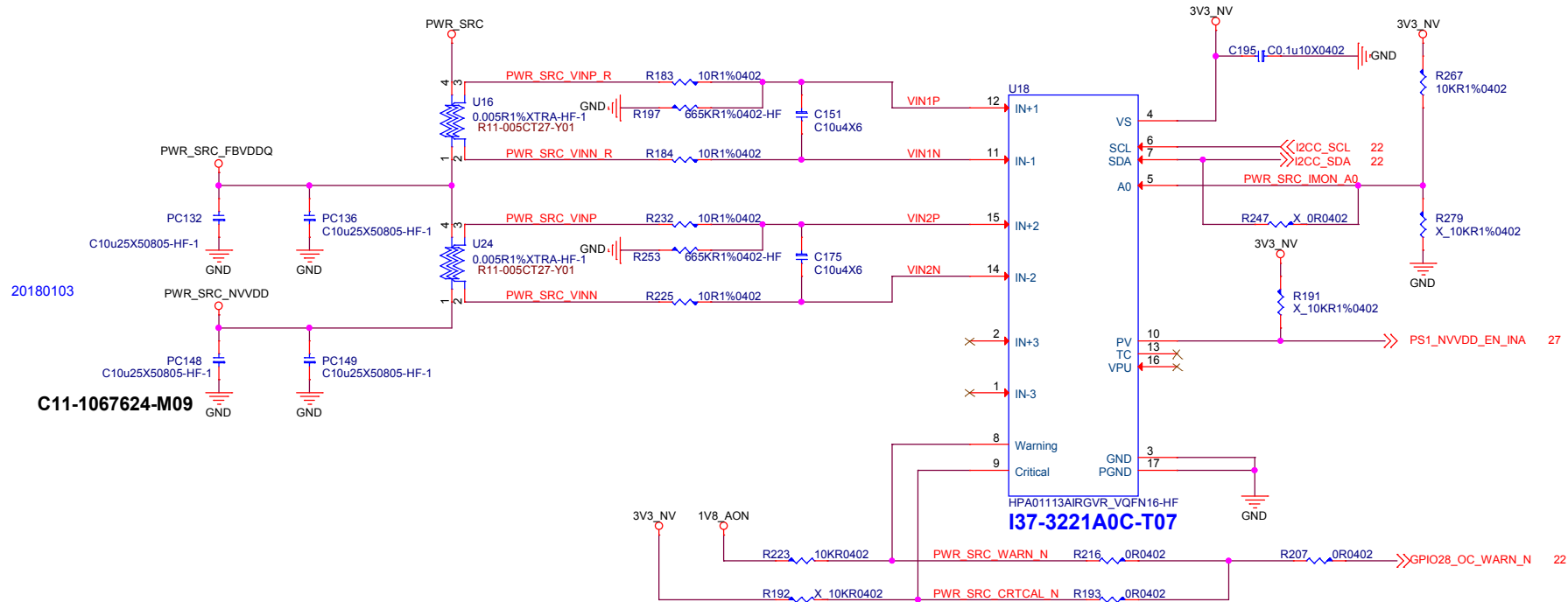


NVVDD Power Enable

The propagation delay between 1V8_MAIN_EN and the NVVDD_EN needs to be less than 300us during both power up and power down

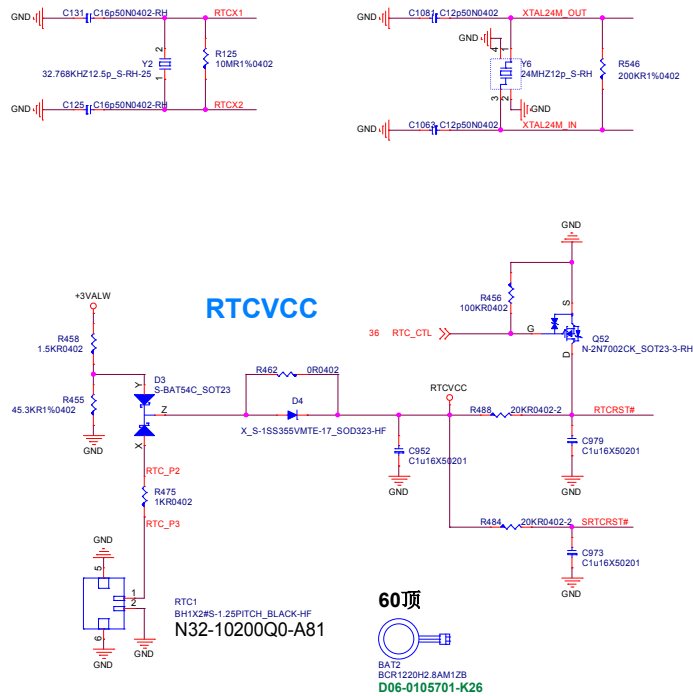
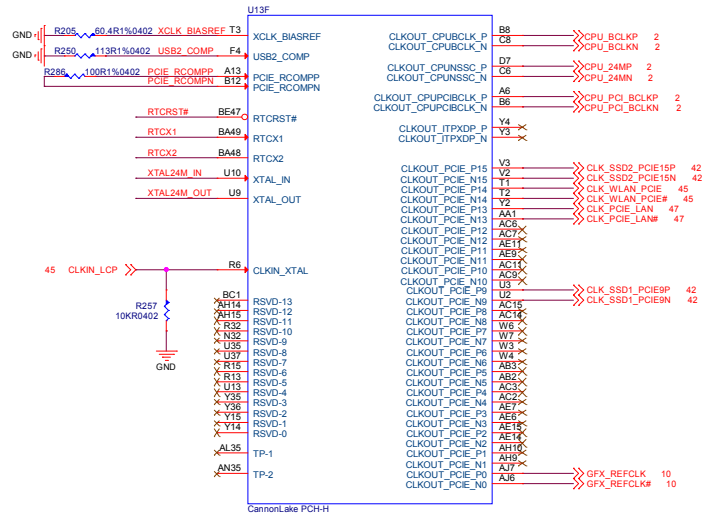


DGPU_Power Control

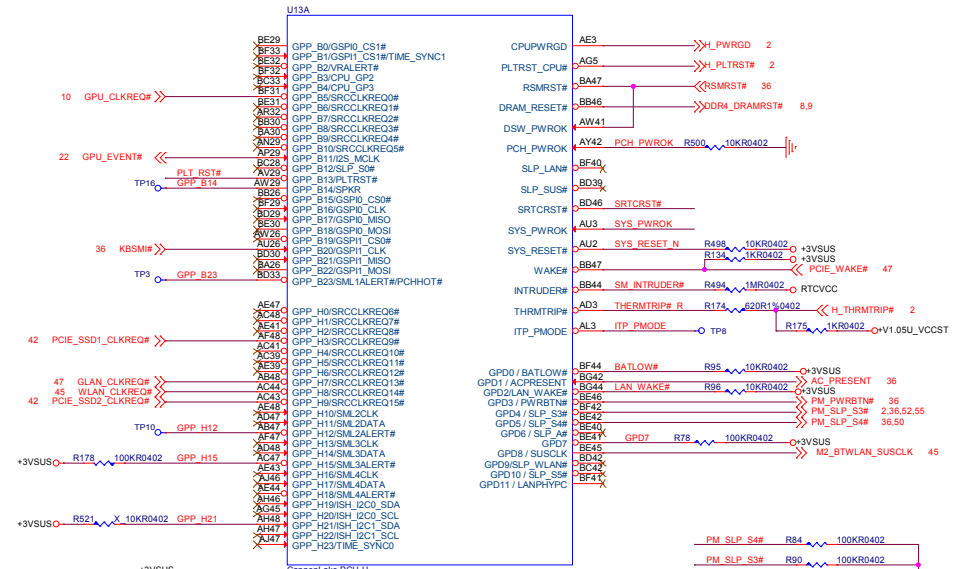


msi MICRO-STAR INT'L CO.,LTD.	
Title DGPU Discharge	
Size Custom	Document Number MS-16Q3
Date: Monday, May 21, 2018	Rev 0A
Sheet 28 of 62	

HM370 (RTC/PCIE_Clock/Clock/RSVD)



HM370 (CLKREQ/ACPI)



Functional Strap Definitions

SPKR / GPP_B14

The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)

GSPI0_MOSI / GPP_B18

The signal has a weak internal pull-down.
0 = Disable No Reboot mode. (Default)
1 = Enable No Reboot mode

GSPH1_MOSI / GPP_B22

This Signal has a weak internal pull-down	
Bit 6 Boot BIOS	Destination
0	SPI (Default)
1	LPC

CM14ALERT#/DCUHQOT#/CDB_P02

This signal has an internal pull-down.

GPP_H12

This signal has a weak internal pull-down

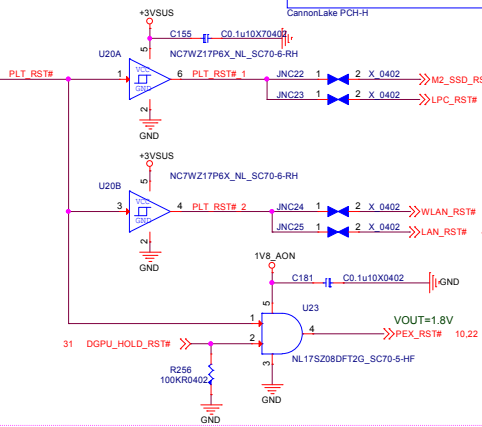
GPP_H15

External pull-up is required. Recommend up to 3.3V or 75K if pulled up to 1.8V.

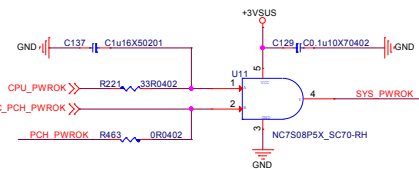
GPPD7

External pull-up is required. Recommend 100K.
This strap should sample HIGH. There should NOT be
any on-board device driving it to opposite direction
during strap sampling

DG/ RTC Well Input Strap

RSMRST# & DSW_PWROK, PCH_PWROK : PD
RTCRST#, SRTCRST#, INTRUDER# : PU

SYS_PWROK



HM370 (DMI/PCIE/USB3.1/USB2.0/CNVi)

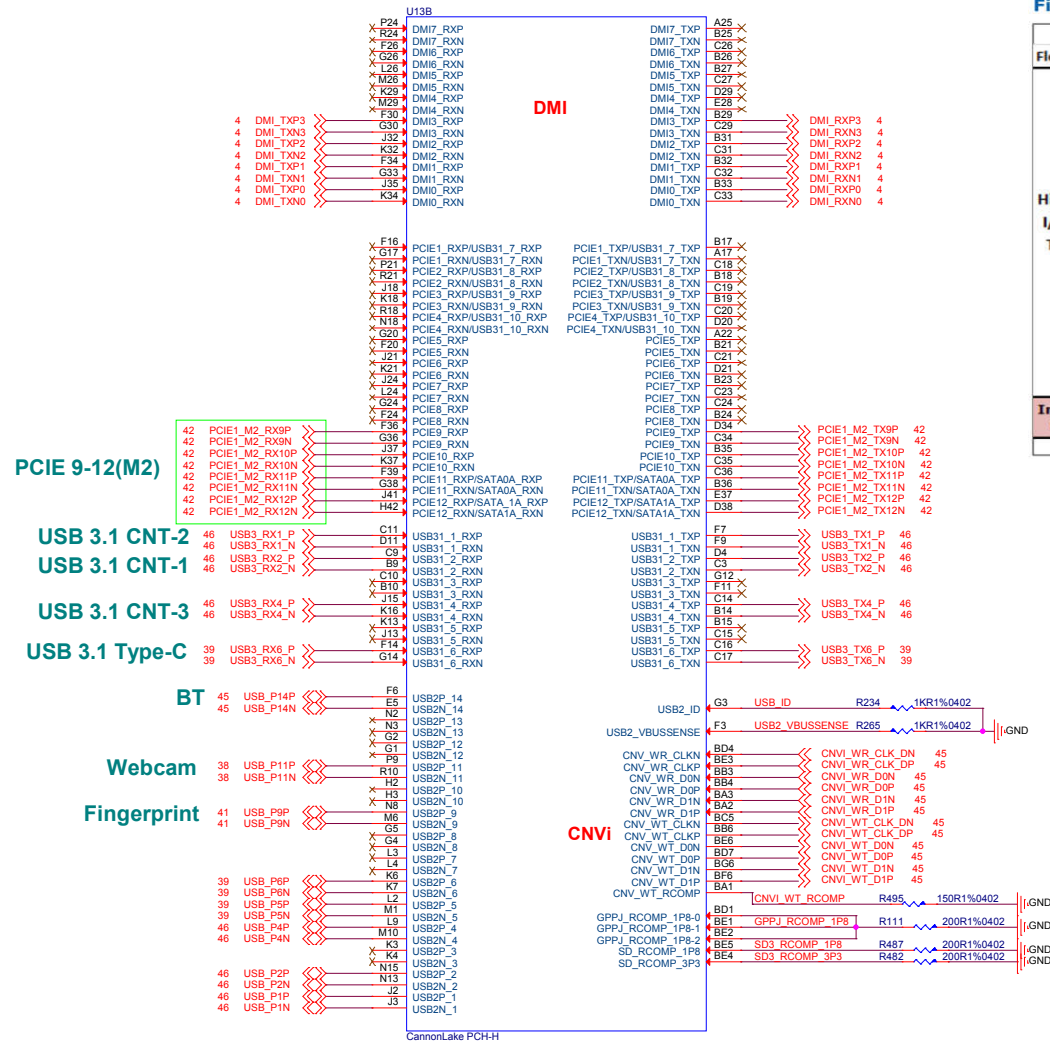


Figure 14-1. High Speed I/O (HSIO) Lane Multiplexing in PCH

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1 #7 PCIe* #1	USB3.1 Gen1 #8 PCIe* #2	USB3.1 Gen1 #9 PCIe* #3	USB3.1 Gen1 #10 PCIe* #4	PCIe* #5 GBE	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9 GBE	PCIe* #10	PCIe* #11 SATA 0a	PCIe* #12 SATA 1a GBE	PCIe* #13 SATA 0b GBE	PCIe* #14 SATA 1b	PCIe* #15 SATA 2	PCIe* #16 SATA 3	PCIe* #17 SATA 4	PCIe* #18 SATA 5	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							No Support				No Support		Yes				No Support		Yes		Yes									
Intel® RST Support							No Support				No Support		Yes				No Support		Yes		Yes									

[illegible]

- Added 4 new PCIe 3.0 lanes versus KBL-H platform.
- GbE LAN removed from lane 10 and SATA #0/#1 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

HM370(SATA/PCIE/USB_OC/DDI)

U13C

GLAN

WLAN

PCIE 17-20(SSD2)

47 PCIE_GLAN_RXP
47 PCIE_GLAN_RXN
45 PCIE_RXP1_SLOT
45 PCIE_RXN1_SLOT

42 PCIE2_M2_RX17P
42 PCIE2_M2_RX17N
42 PCIE2_M2_RX18P
42 PCIE2_M2_RX18N
42 PCIE2_M2_RX19P
42 PCIE2_M2_RX19N
42 PCIE2_M2_RX20P
42 PCIE2_M2_RX20N

42 M2_SSD1_PEDET
36 SCI_WAKE_UP#

+3VRUN
+3VSUS

38 EDP_HPD

38 EDP_VDDEN
38 EDP_BKLTEN
38 EDP_BKLTCTL

C46
C45
C47
D46
E45
F44
M40
L41
K44
K43
R40
P41
N42
M44
R37
R35
R44
T43
U41
U40
W44
W43
Y41
Y40

AH41
AJ43
AK47
AL47
AL48
AH35
AH40
AM45
AK48
AH36
AL40
AJ44
AL41

AT6
AN10
AP9
AL15
AN6
AL13
AR8
AN13
AL10
AL9
AR3
AP3
AP2
AN4
AM7
AV44
AV46
AU48

CannonLake PCH-H

PCIE13_RXP/SATA0B_RXP
PCIE13_RXN/SATA0B_RXN
PCIE14_RXP/SATA1B_RXP
PCIE14_RXN/SATA1B_RXN
PCIE15_RXP/SATA2_RXP
PCIE15_RXN/SATA2_RXN
PCIE16_RXP/SATA3_RXP
PCIE16_RXN/SATA3_RXN
PCIE17_RXP/SATA4_RXP
PCIE17_RXN/SATA4_RXN
PCIE18_RXP/SATA5_RXP
PCIE18_RXN/SATA5_RXN
PCIE19_RXP/SATA6_RXP
PCIE19_RXN/SATA6_RXN
PCIE20_RXP/SATA7_RXP
PCIE20_RXN/SATA7_RXN
PCIE21_RXP
PCIE21_RXN
PCIE22_RXP
PCIE22_RXN
PCIE23_RXP
PCIE23_RXN
PCIE24_RXP
PCIE24_RXN

GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2
GPP_E3/CPU_GP0
GPP_E4/SATA_DEVSLP0
GPP_E5/SATA_DEVSLP1
GPP_E6/SATA_DEVSLP2
GPP_E7/CPU_GP1
GPP_E8/SATALED#
GPP_E9/USB2_OC0#
GPP_E10/USB2_OC1#
GPP_E11/USB2_OC2#
GPP_E12/USB2_OC3#
GPP_I0/DDPB_HPD0/DISP_MISC0
GPP_I1/DDPC_HPD1/DISP_MISC1
GPP_I2/DPPD_HPD2/DISP_MISC2
GPP_I3/DPPE_HPD3/DISP_MISC3
GPP_I4/EDP_HPD/DISP_MISC4
GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA
GPP_I11/M2_SKT2_CFG0
GPP_I12/M2_SKT2_CFG1
GPP_I13/M2_SKT2_CFG2
GPP_I14/M2_SKT2_CFG3
GPP_F19/eDP_VDDEN
GPP_F20/eDP_BKLTEN
GPP_F21/eDP_BKLTCTL

GPP_F22/DDPF_CTRLCLK
GPP_F23/DDPF_CTRLDATA

C38
B38
D39
C39
C40
B40
C41
B41
B42
A42
D42
C42
D43
C44
B44
A44
F46
G47
H48
H47
G48
G49
G45
G46

PCIE_GLAN_TXP
PCIE_GLAN_TXN
PCIE_TXP1_SLOT
PCIE_TXN1_SLOT
PCIE2_M2_TX17P
PCIE2_M2_TX17N
PCIE2_M2_TX18P
PCIE2_M2_TX18N
PCIE2_M2_TX19P
PCIE2_M2_TX19N
PCIE2_M2_TX20P
PCIE2_M2_TX20N

AN47
AM46
AM43
AM47
AM48
AP48
AR47
AN46
AN37
AP47
AR42
AR48
AU46
AU47
AP41
AV47
AR35
AR37
AV43

DGPU_PWR_EN
R153
100KR0402

USB_OC#

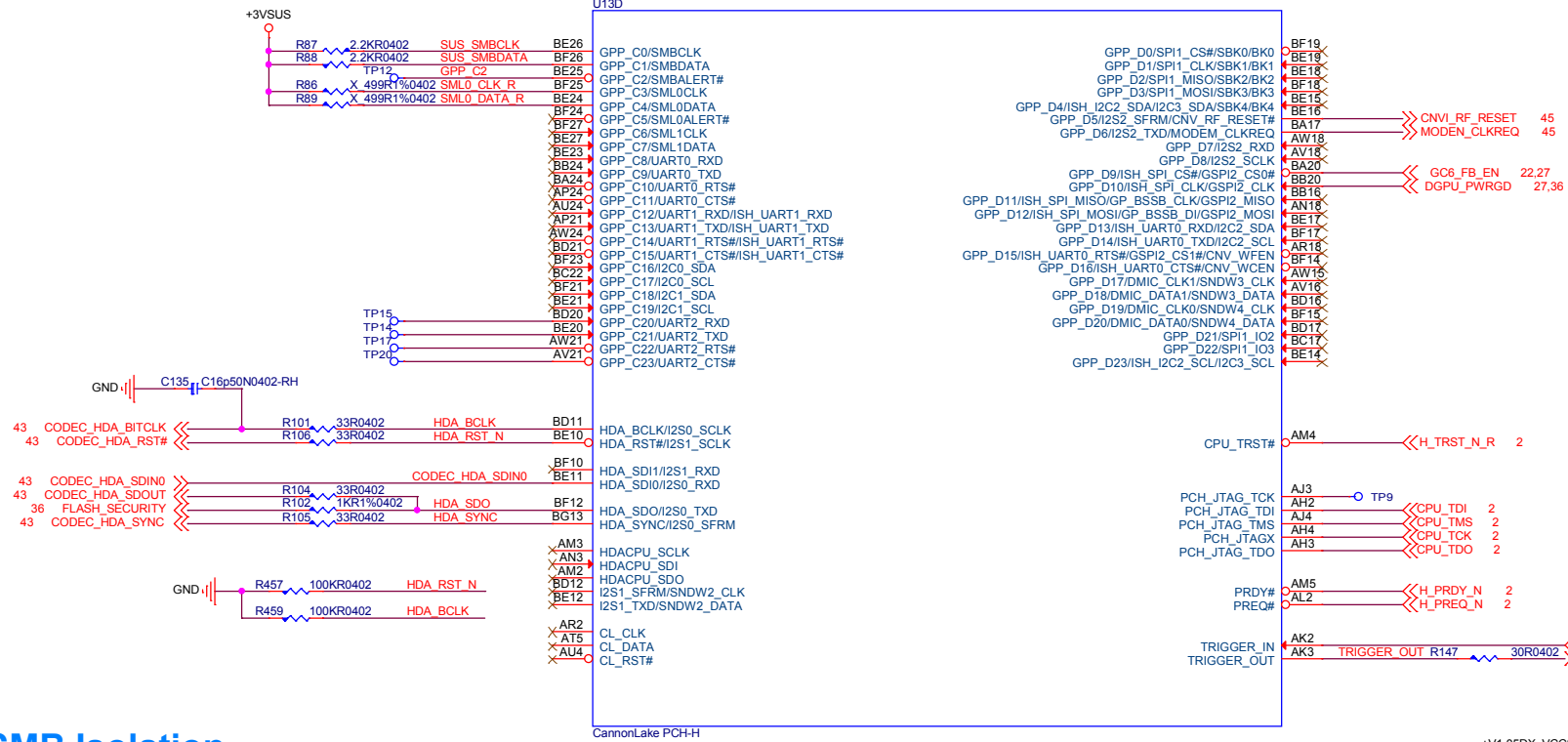
DGPU_HOLD_RST#

msi

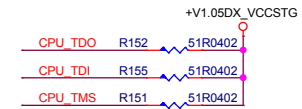
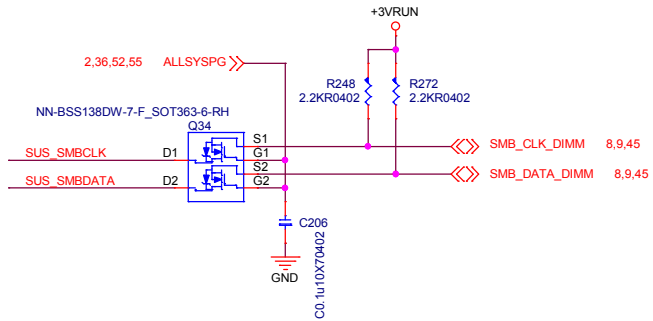
MICRO-STAR INT'L CO.,LTD.

Title		PCH-3(SATA/PCIE/USB_OC/DDI)	
Size	Document Number	Rev	0A
Custom	MS-16Q3		
Date:	Monday, May 21, 2018	Sheet	31 of 62

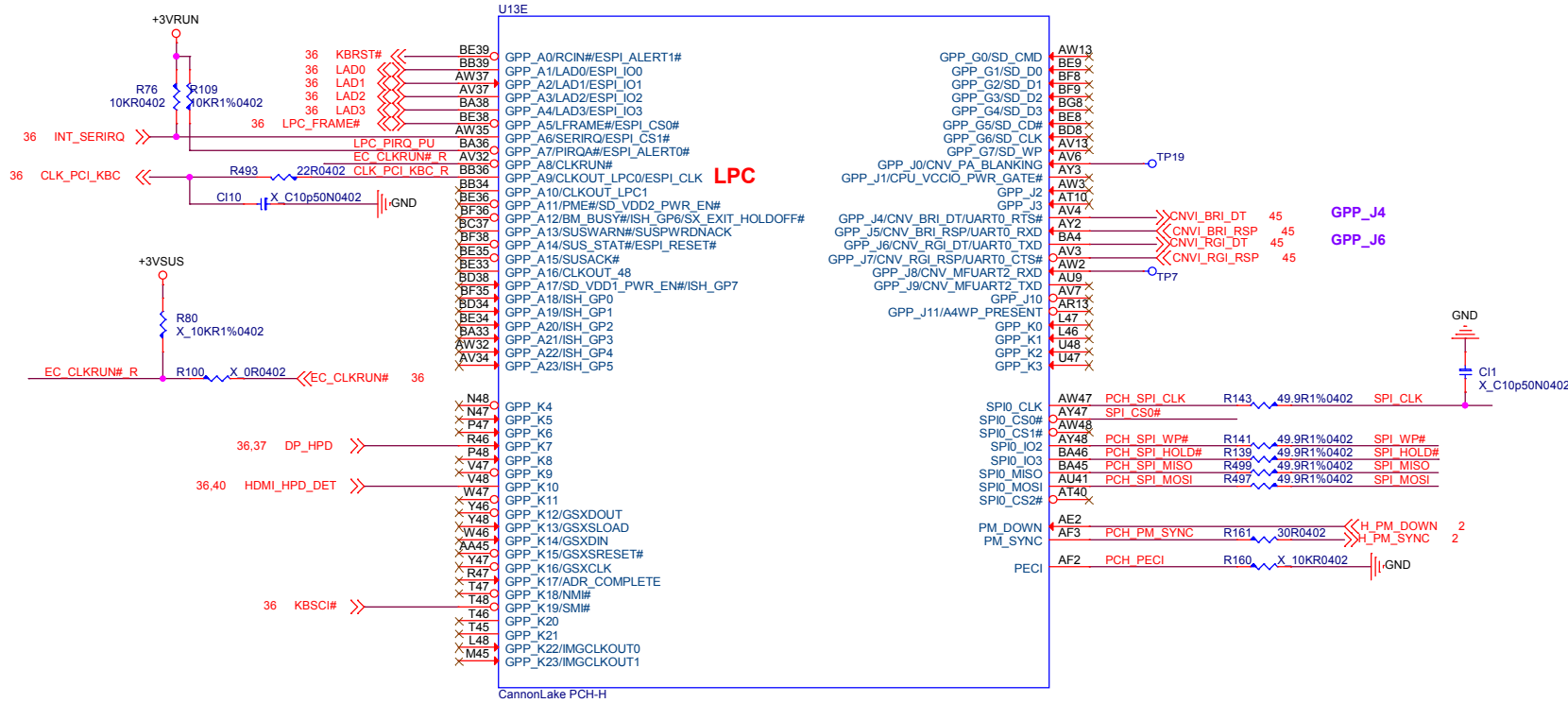
HM370 (HDA/GPIO/TJAG)



SMB Isolation



HM370 (UART/I2C/SPI)



Functional Strap Definitions

GPP_J4

This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected.

GPP_J6

An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.

GPP_J9

The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail

SPI0_IO2

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPI0_IO3

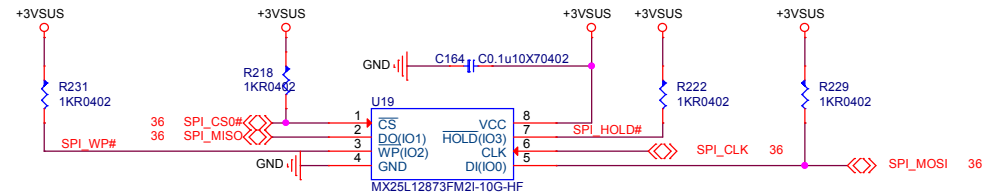
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

SPI0_MOSI

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

MISO isn't Strap

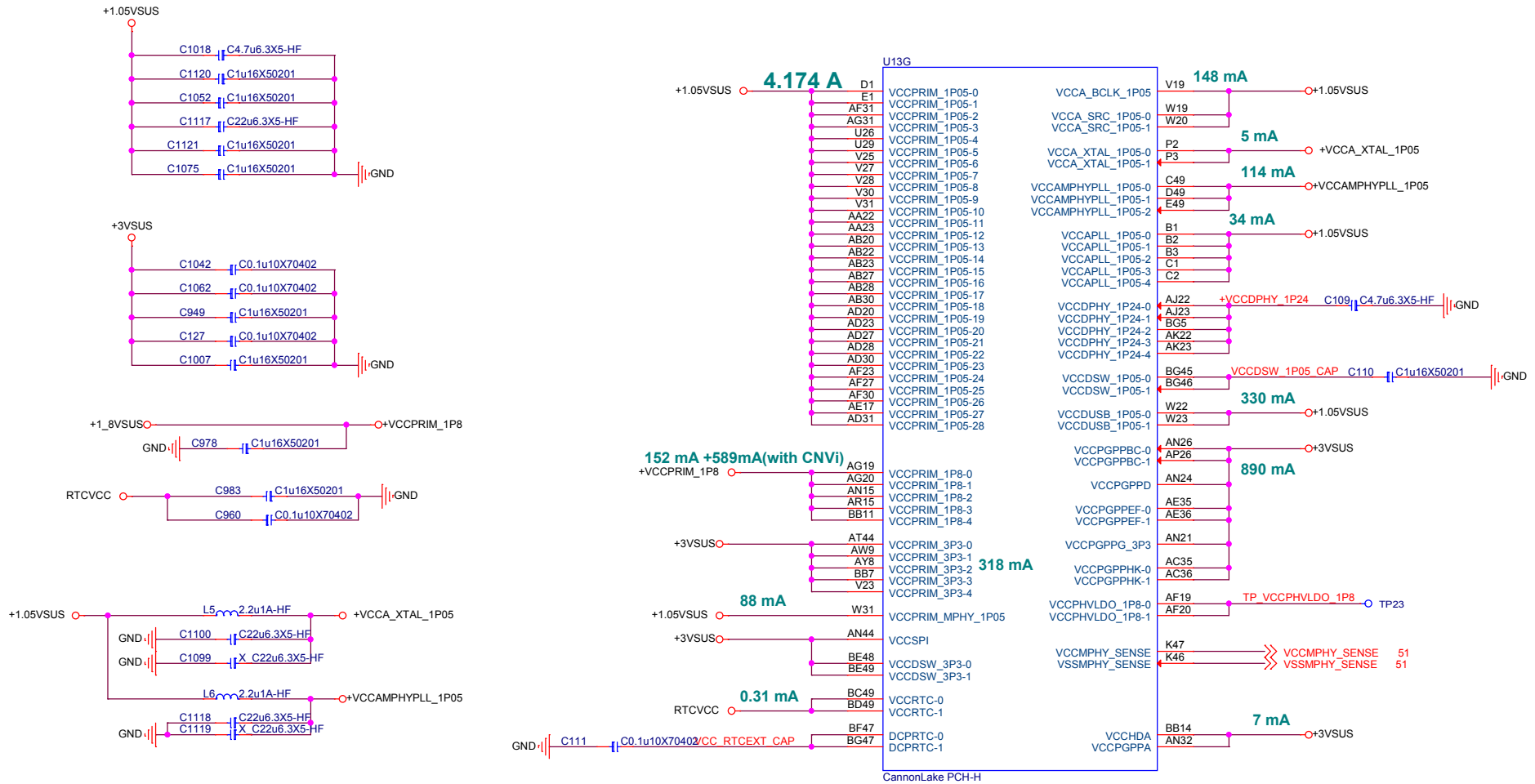
SPI FLASH ROM



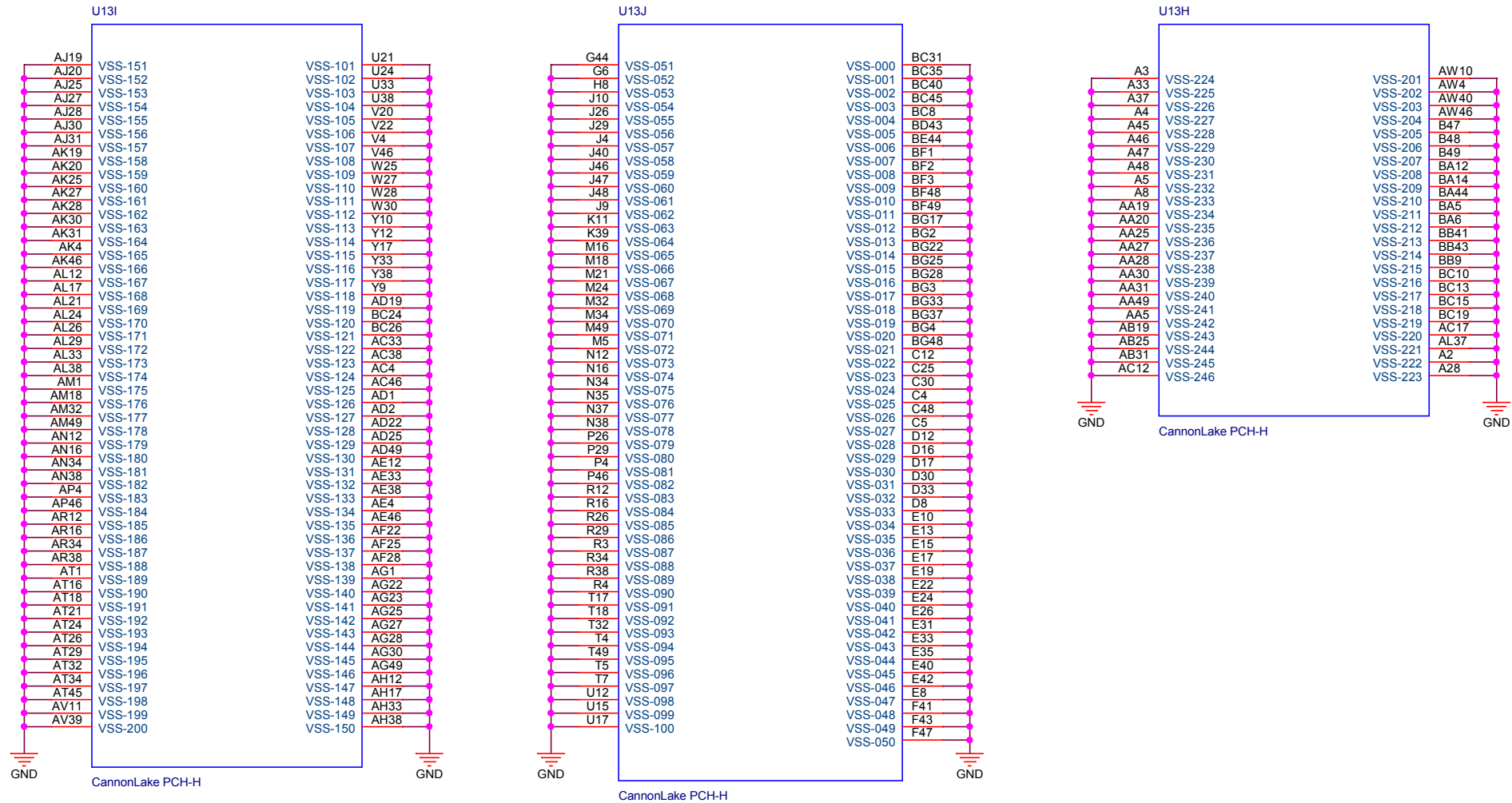
MICRO-STAR INT'L CO.,LTD.

Title		PCH-5(UART/I2C/SPI)	
Size	Document Number	MS-16Q3	Rev 0A
Date:	Monday, May 21, 2018	Sheet 33	of 62

HM370 (Power)



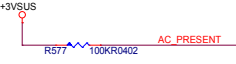
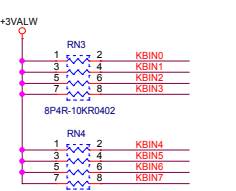
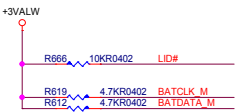
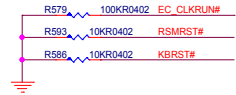
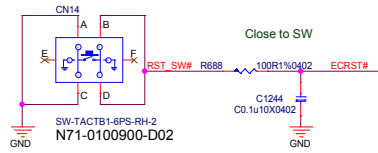
PCH-H(GND)



msi		MICRO-STAR INT'L CO.,LTD.	
Title			
PCH-7(GND)			
Size	Document Number		Rev
Custom	MS-16Q3		0A
Date:	Monday, May 21, 2018		Sheet 35 of 62

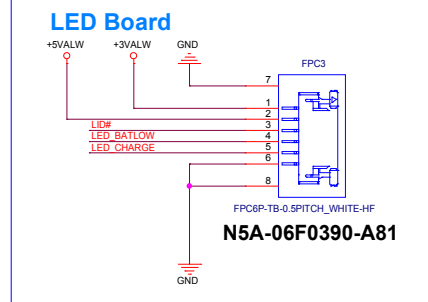
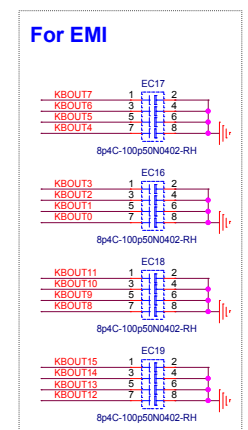
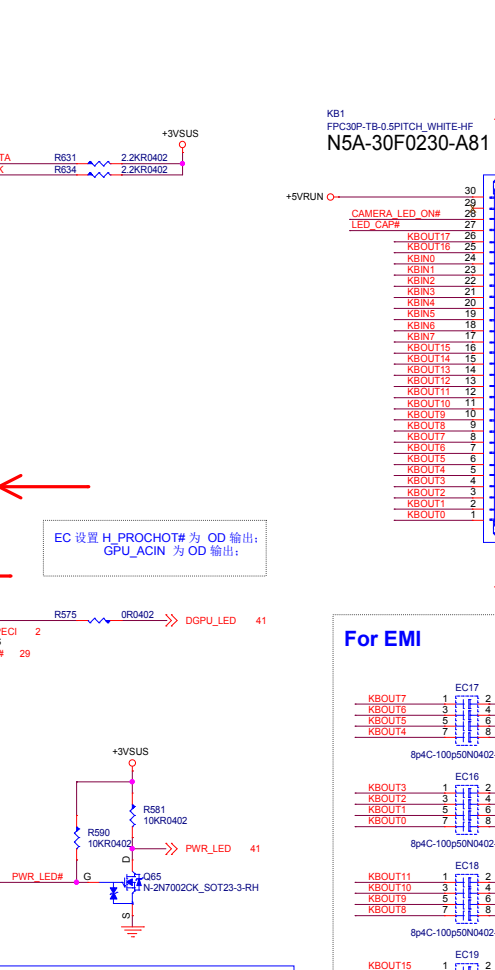
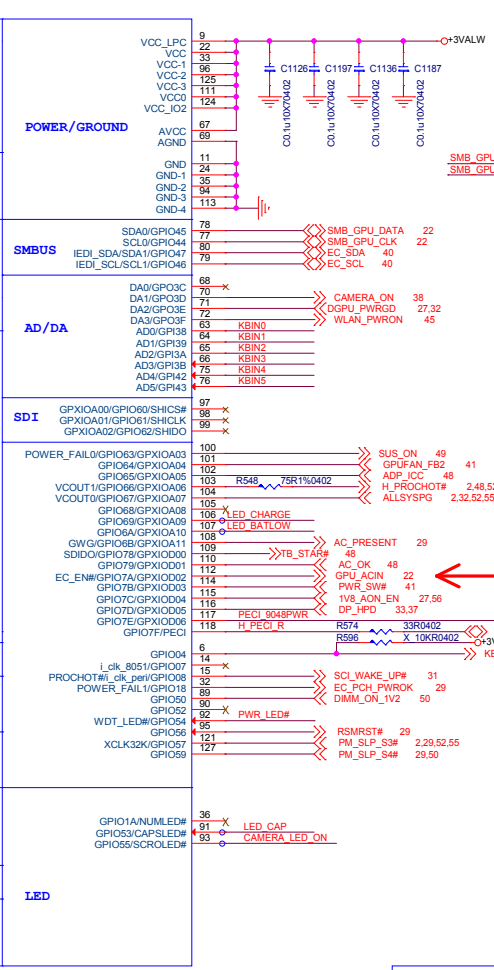
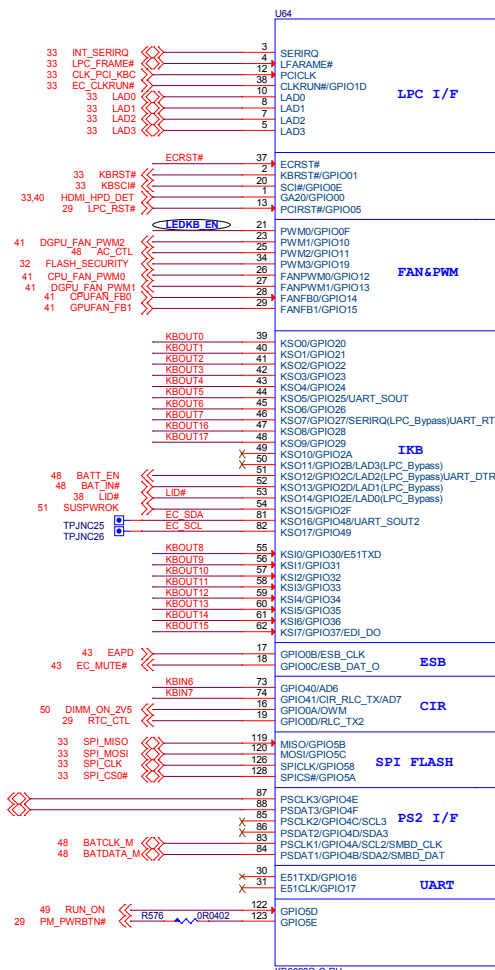
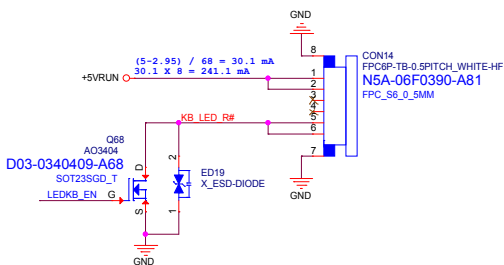
KBC/EC/uP (ENE9028)

Hardware Reset

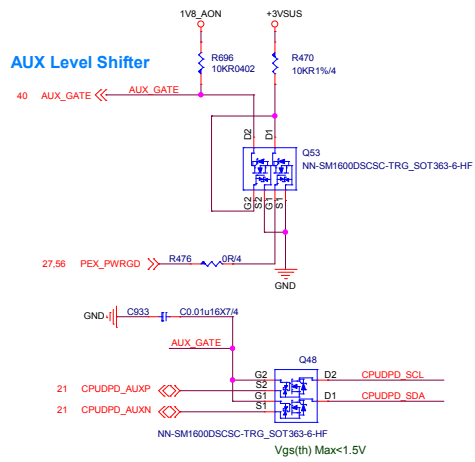


Pin1 to Pin1

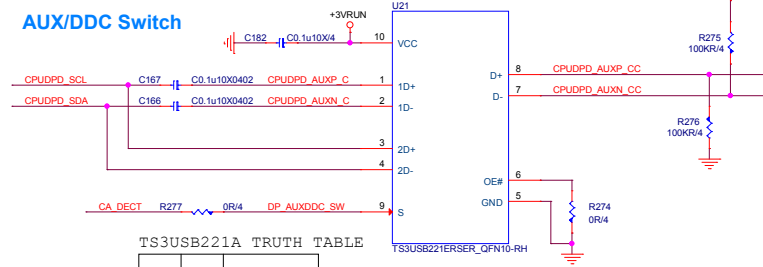
Change CON14 P/N from N5A-06F0420-A81 to N5A-06F0390-A81 for ME. 20180115



DP 1.2



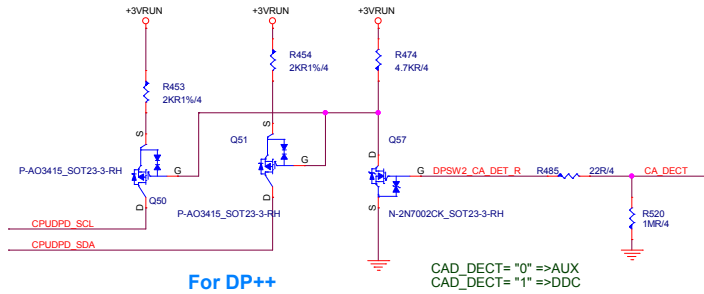
AUX/DDC Switch



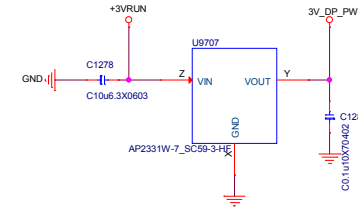
TS3USB221A TRUTH TABLE

S	OE#	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

CAD_DECT= "0" ==>AUX
CAD_DECT= "1" ==>DDC

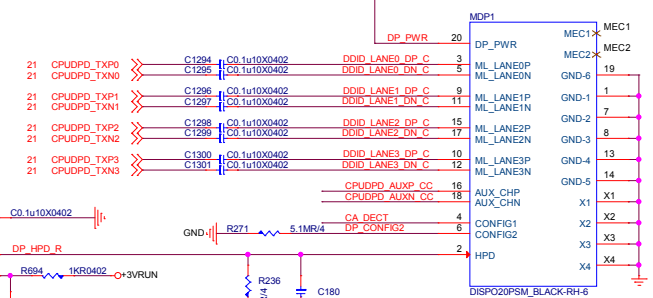


Avoid DP Leakage



W>20mils

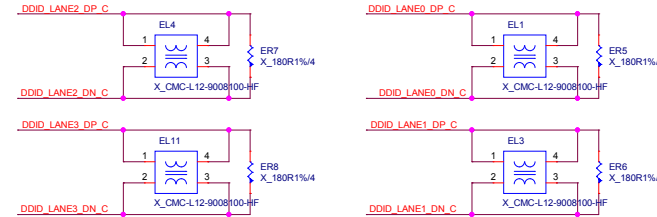
Display Port



CAD_SNK Have Internal Pull down 1Mohm.
HPD_SNK Have Internal Pull down 150kohm.
No problem with Leakage from DP device
The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

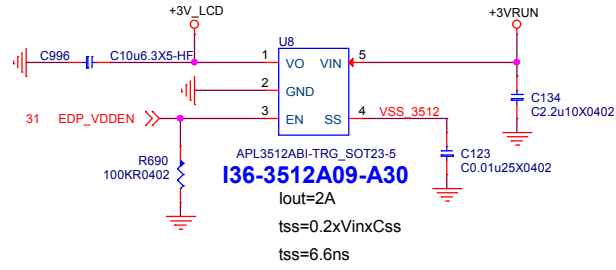
TO DGPU
TO EC/PCH

EMI Close CONN

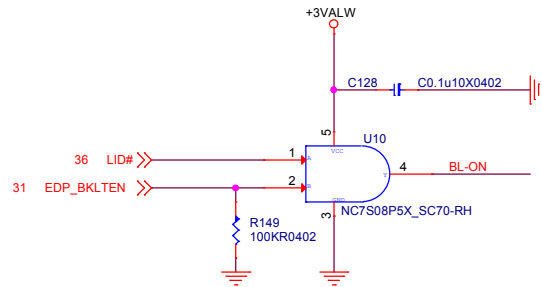


msi MICRO-STAR INT'L CO.,LTD.	
Title	
DP 1.2	
Size	Document Number
Custom	MS-16Q3
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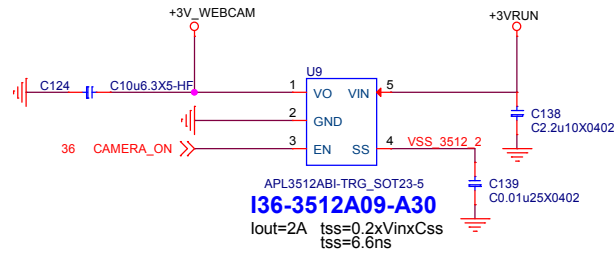
Panel Device Logic Power



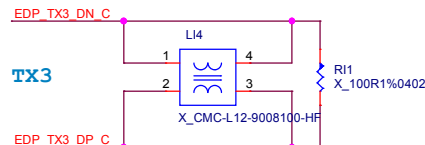
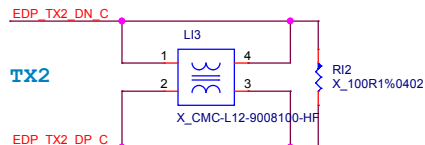
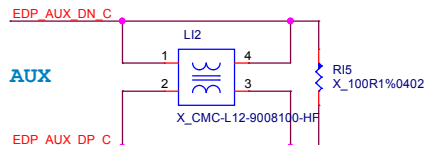
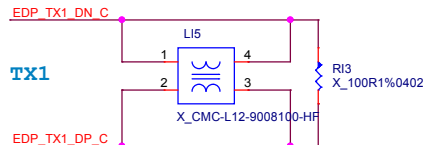
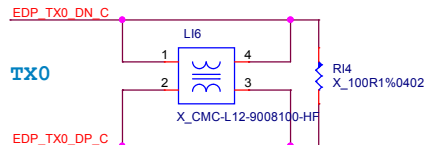
Backlight



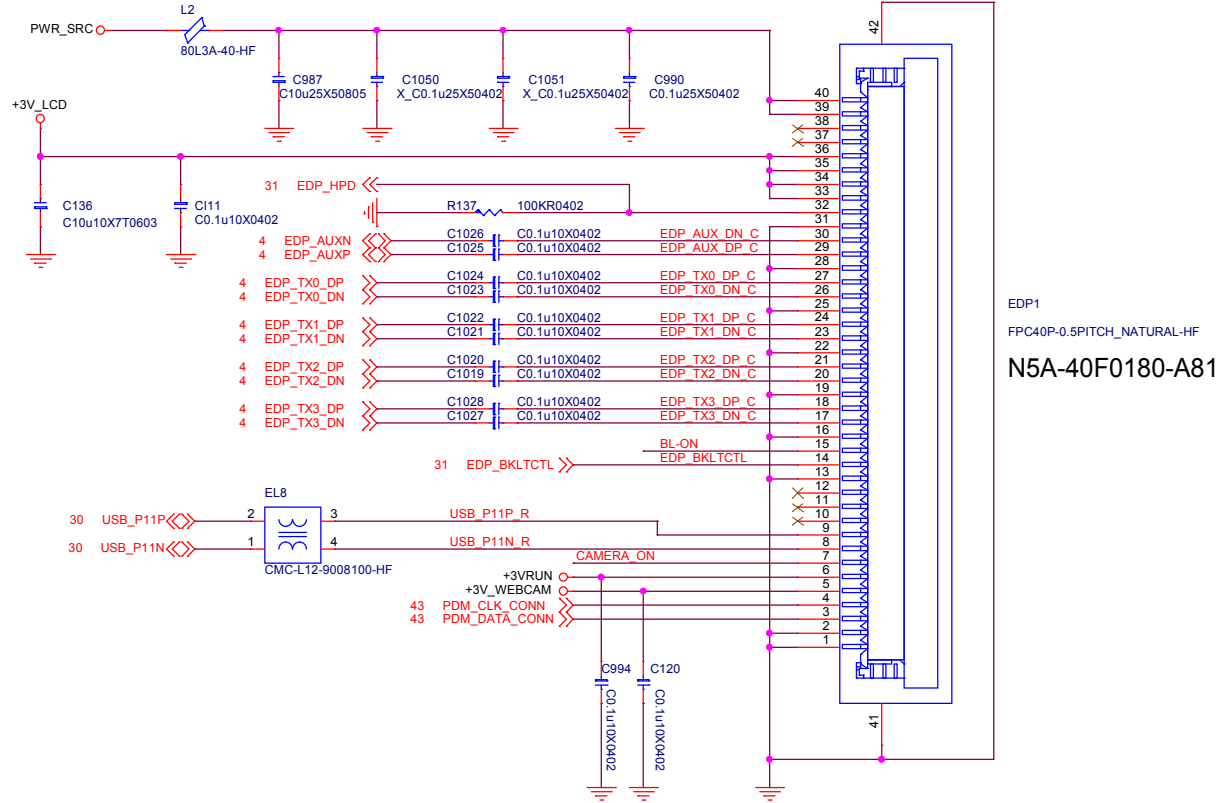
CAMERA Power



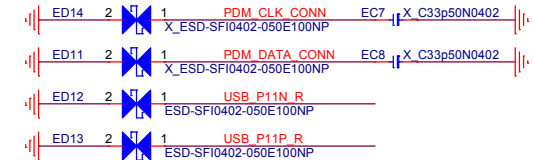
EMI Close Connector

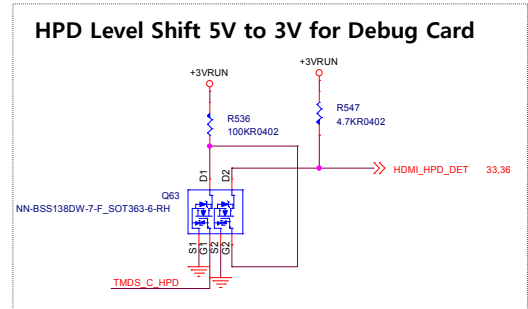
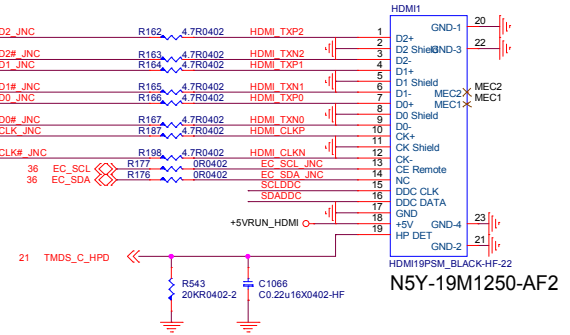
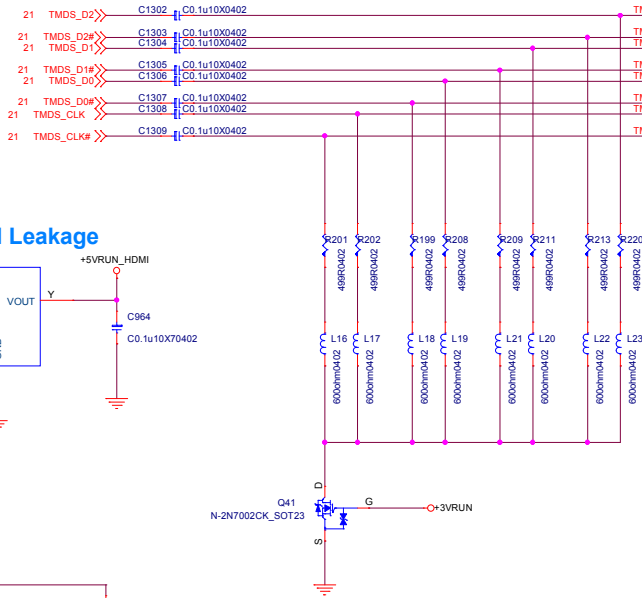
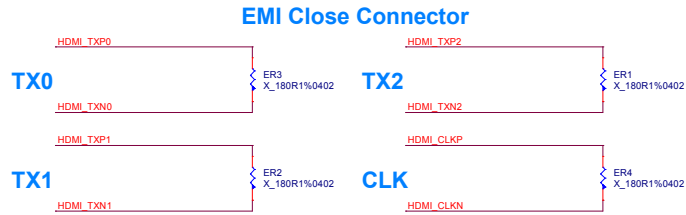
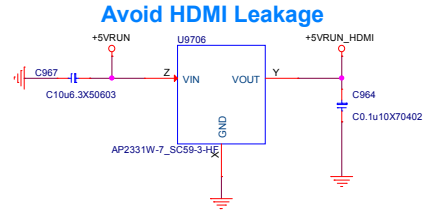
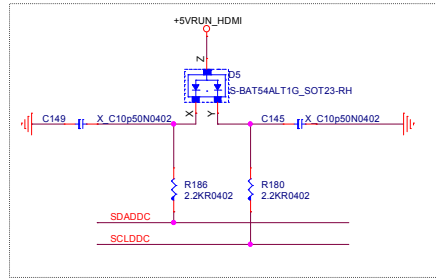
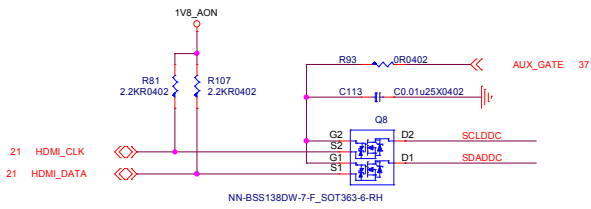


eDP Connector



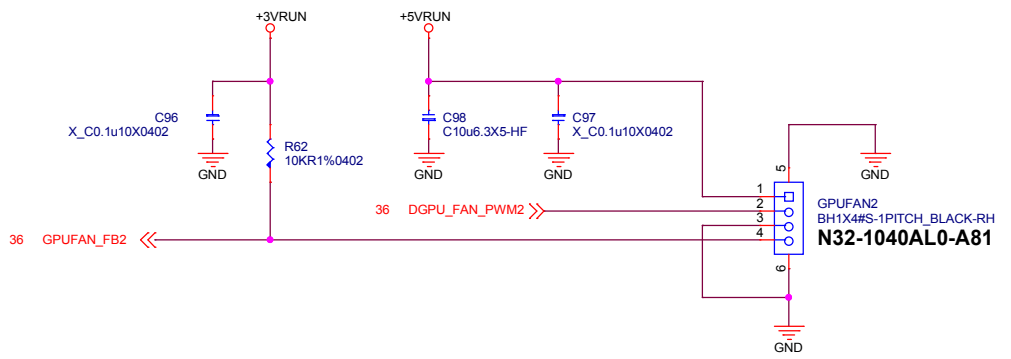
ESD



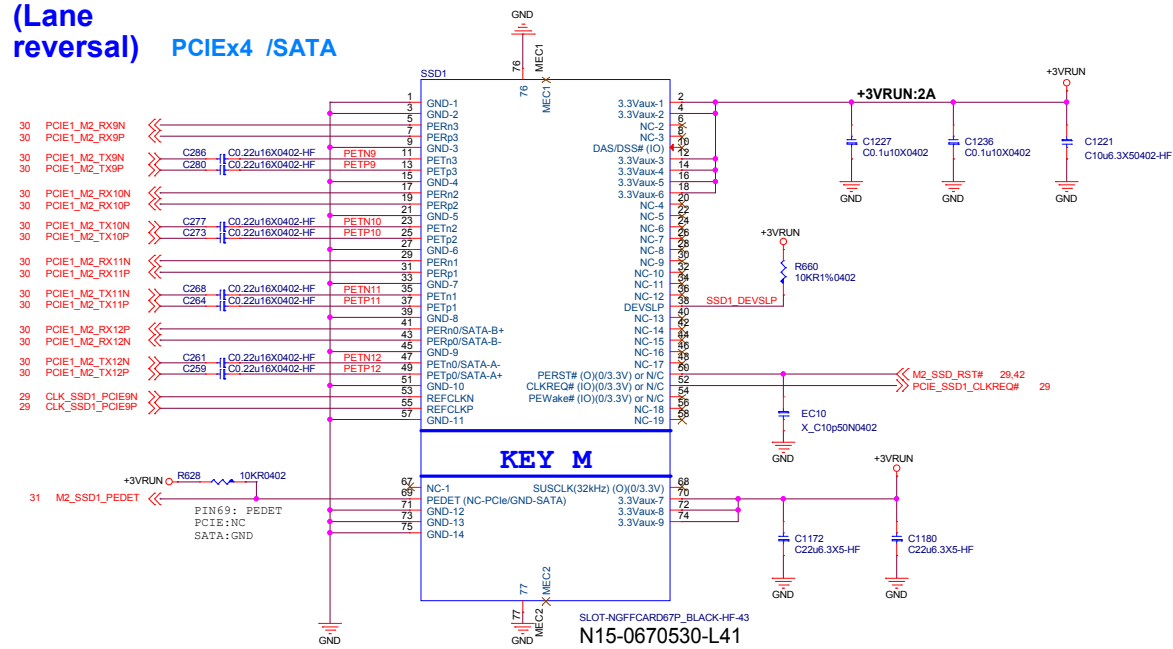


msi MICRO-STAR INT'L CO.,LTD.			
Title	HDMI		
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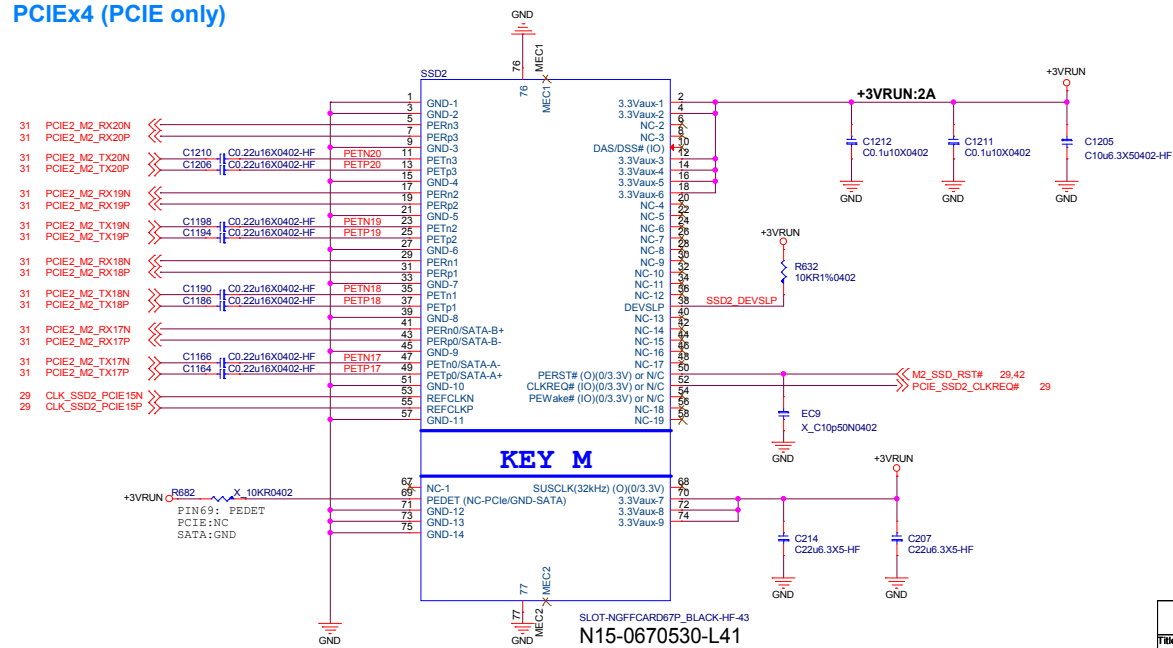
The schematic diagram shows a cross connection between three signals: +3VALW, PWR_SW#, and PWR_SW# R. A vertical line connects +3VALW to a central node. A horizontal line connects PWR_SW# to the same central node. A diagonal line connects PWR_SW# R to the central node. A 10K resistor (R635) is connected between +3VALW and the central node. A 100R resistor (R624) is connected between PWR_SW# R and the central node. A 0.1uF capacitor (C1193) is connected between the central node and GND.



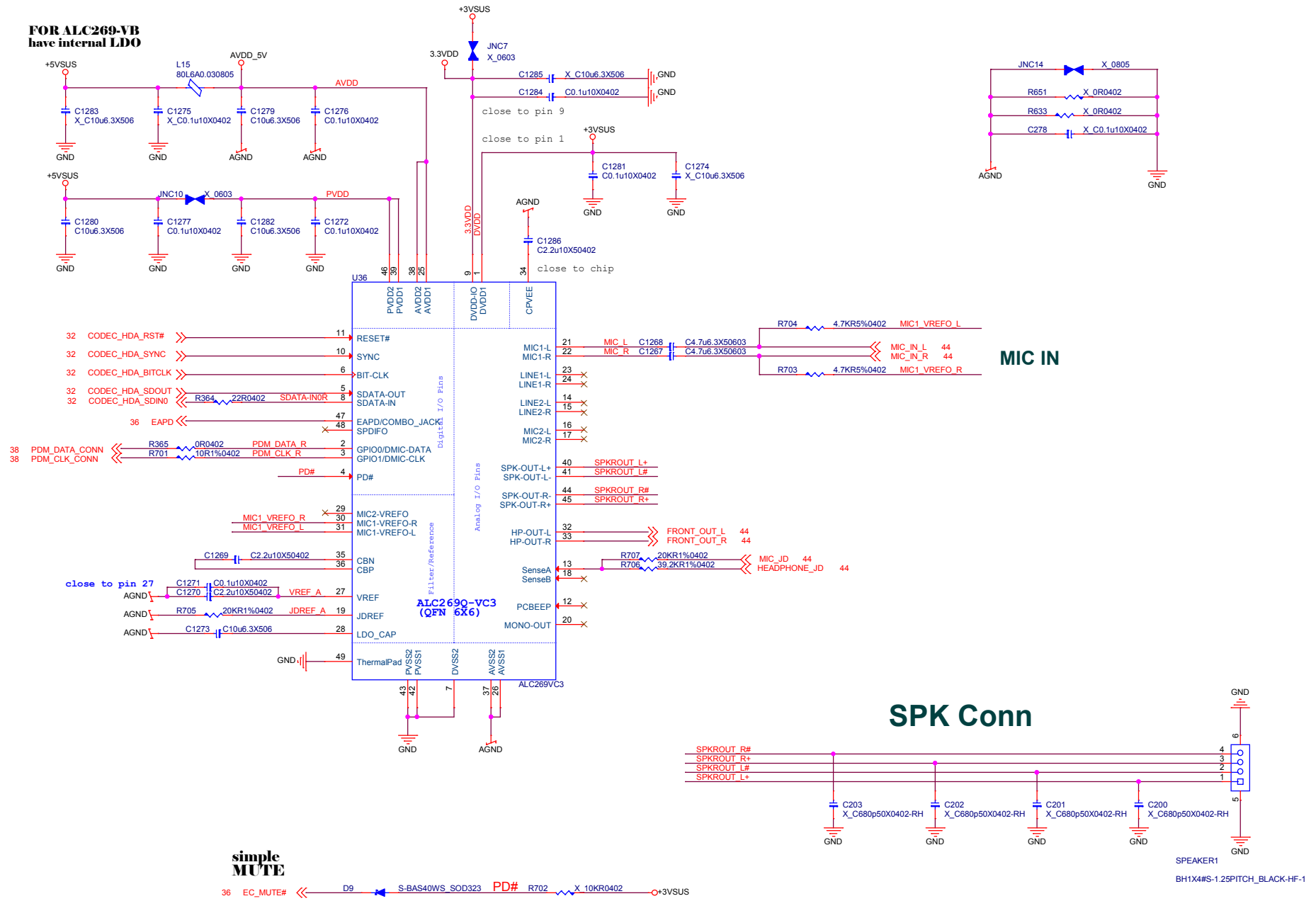
M2 SSD -1 (Lane reversal) PCIEx4 /SATA



M2 SSD -2 PCIEx4 (PCIe only)

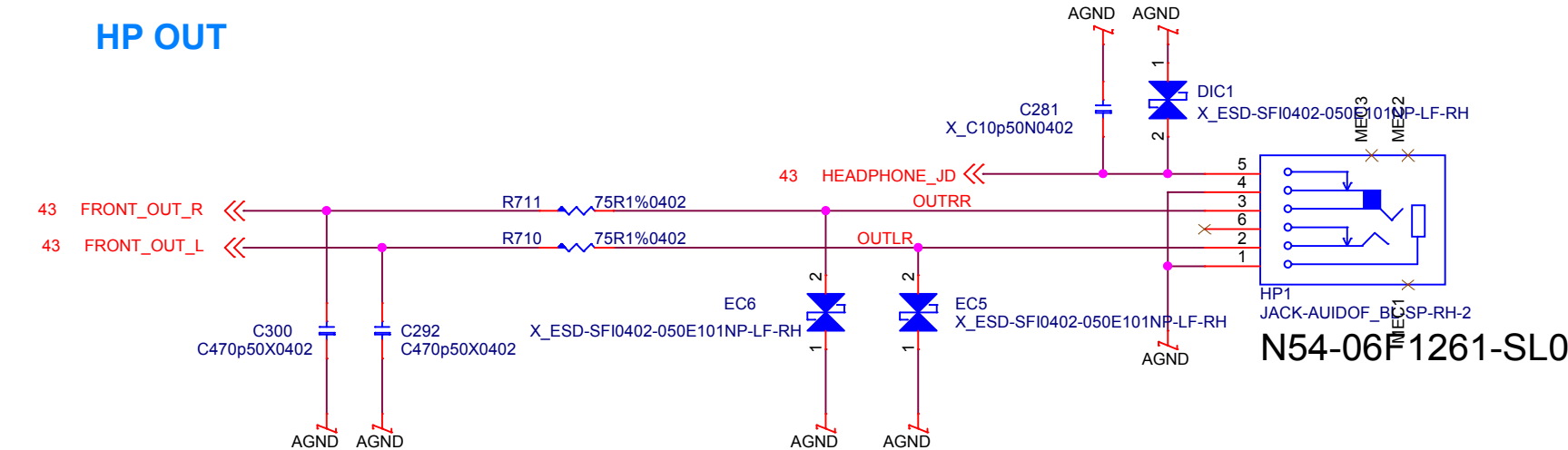


**FOR ALC269-VB
have internal LDO**

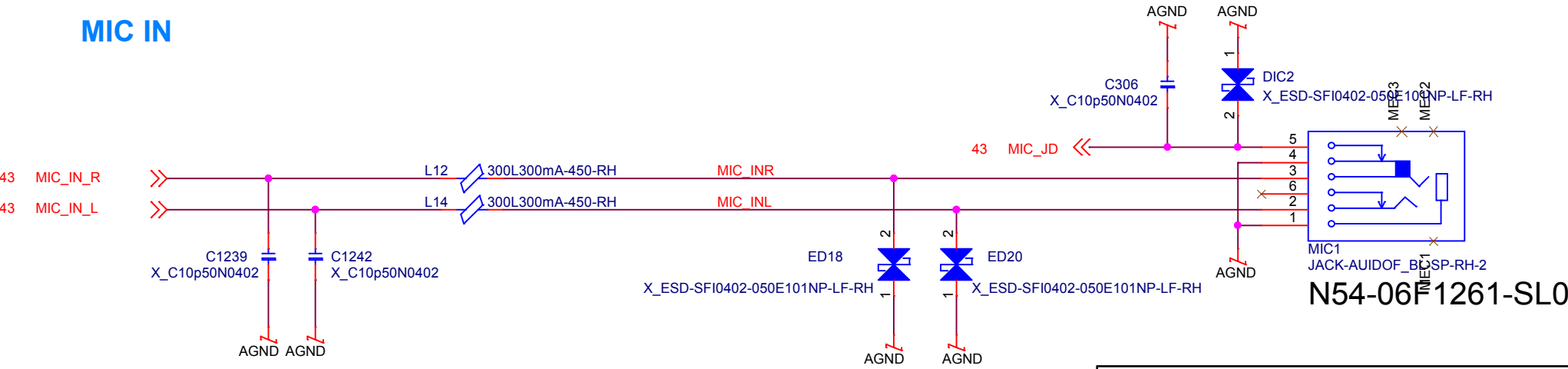


Audio CONN

HP OUT



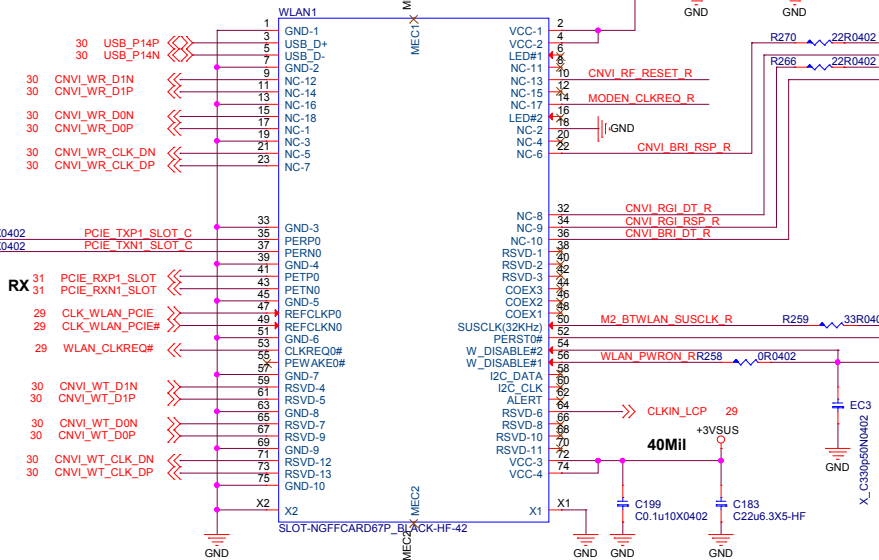
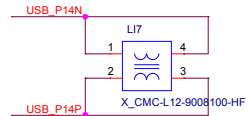
MIC IN



msi MICRO-STAR INT'L CO.,LTD.	
Title	
Audio Jack	
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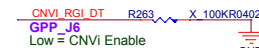
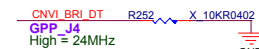
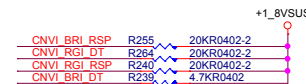
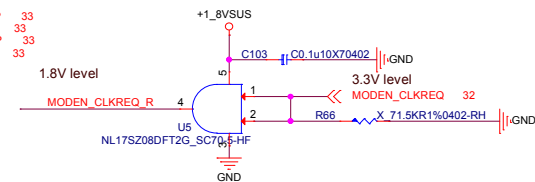
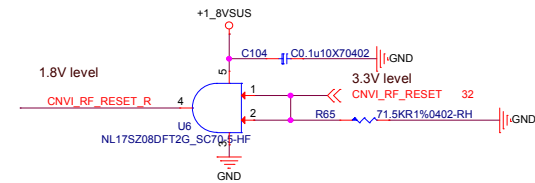
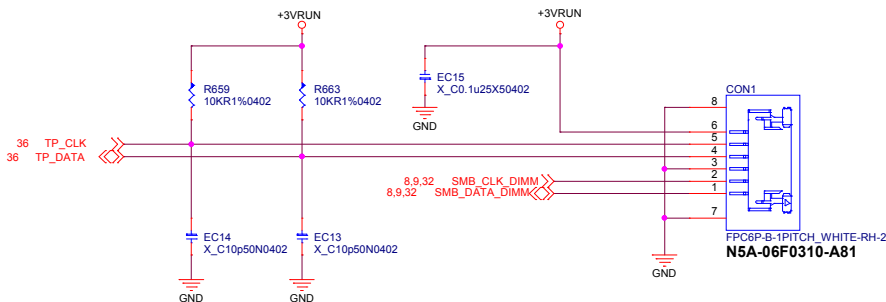
WLAN /ClickPad/FP

EMI



N15-0670520-L41
SLOT_NGFFCARD67_H2_15

Click Pad



Functional Strap Definitions

GPP_J4

This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 MHz XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.

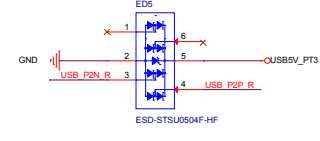
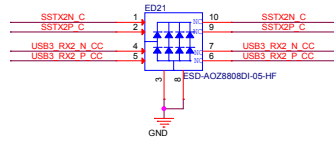
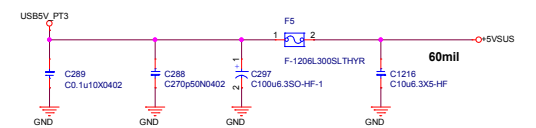
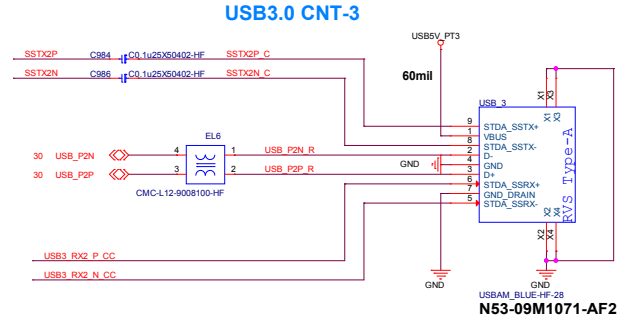
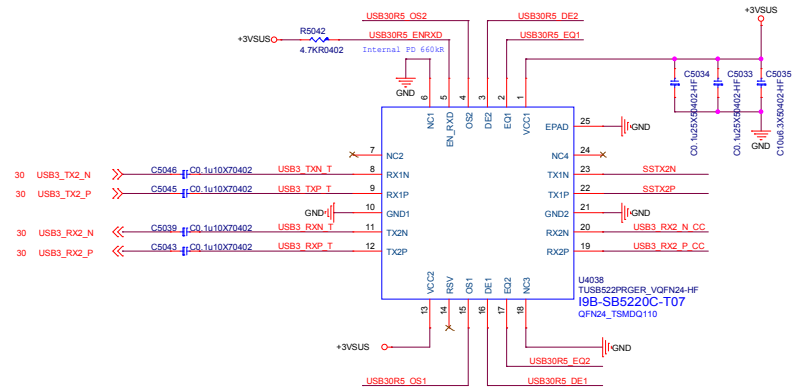
GPP_J6

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.



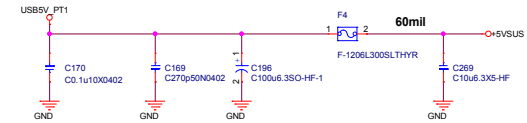
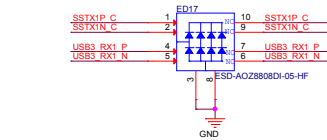
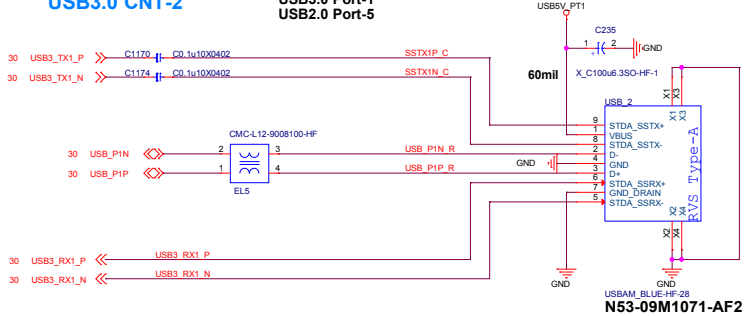
MICRO-STAR INT'L CO.,LTD.

Title			
WLAN /ClickPad/FP			
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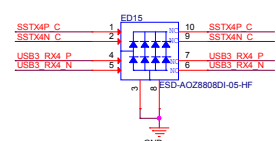
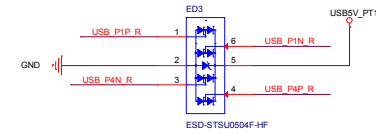
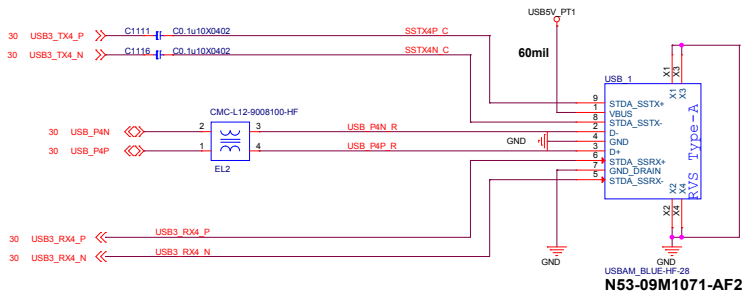
USB3.0 CNT-2

USB3.0 Port-1 USB2.0 Port-5

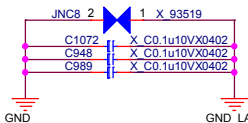
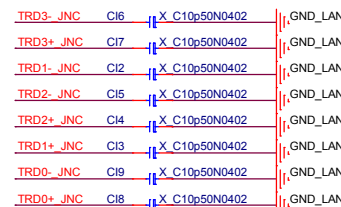


USB3.0 CNT-1

USB3.0 Port-4 USB2.0 Port-2



8111H:TYP: 202mA



LAN1
LAN-RJ45-HF-4
N55-08F0691-AF2

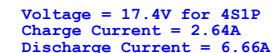
Change CN6 PN. 7/13.

180W,19.5V/9.23A
N54-03F0751-S56
9.5A/20V



N32-1100480-A81

Reverse PIN define for 16Q1 layout



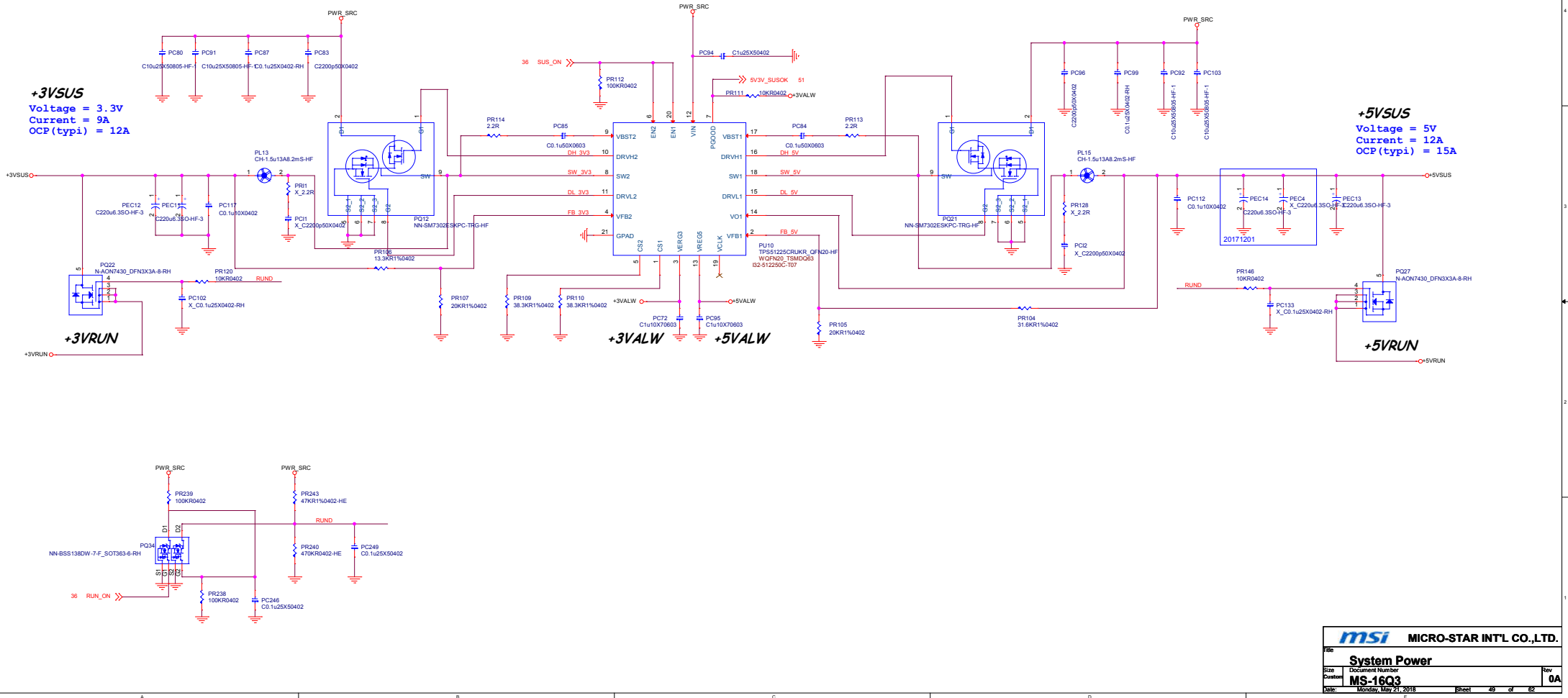
Register name	Register address	FOR state	Description	Note
Charge current(5mR)	0x14H	050x	2.56A	S0
		050x	2.56A	S3/S4/S5
Prepare charge(5mR)	0x14H	008x	0.256A	
Input current(5mR)	0x3FH	19.5V 110x	8.704A	180W
Charge voltage	0x15H	43Fx	17.392V	4S1P
Discharge current(5mR)	0x39H	800x	4.096A	BOOST current

```

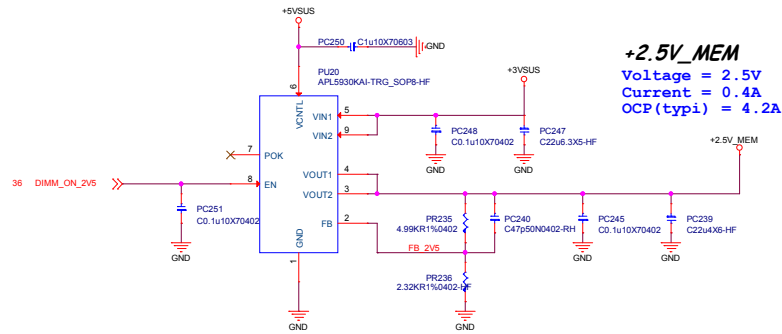
ICHG limi = VILIM/(20*Rsr)=3A
IDISCH limit = VILIM/(5*Rsr)=12A
PR278 1M Adjust battery charging current limit.

```

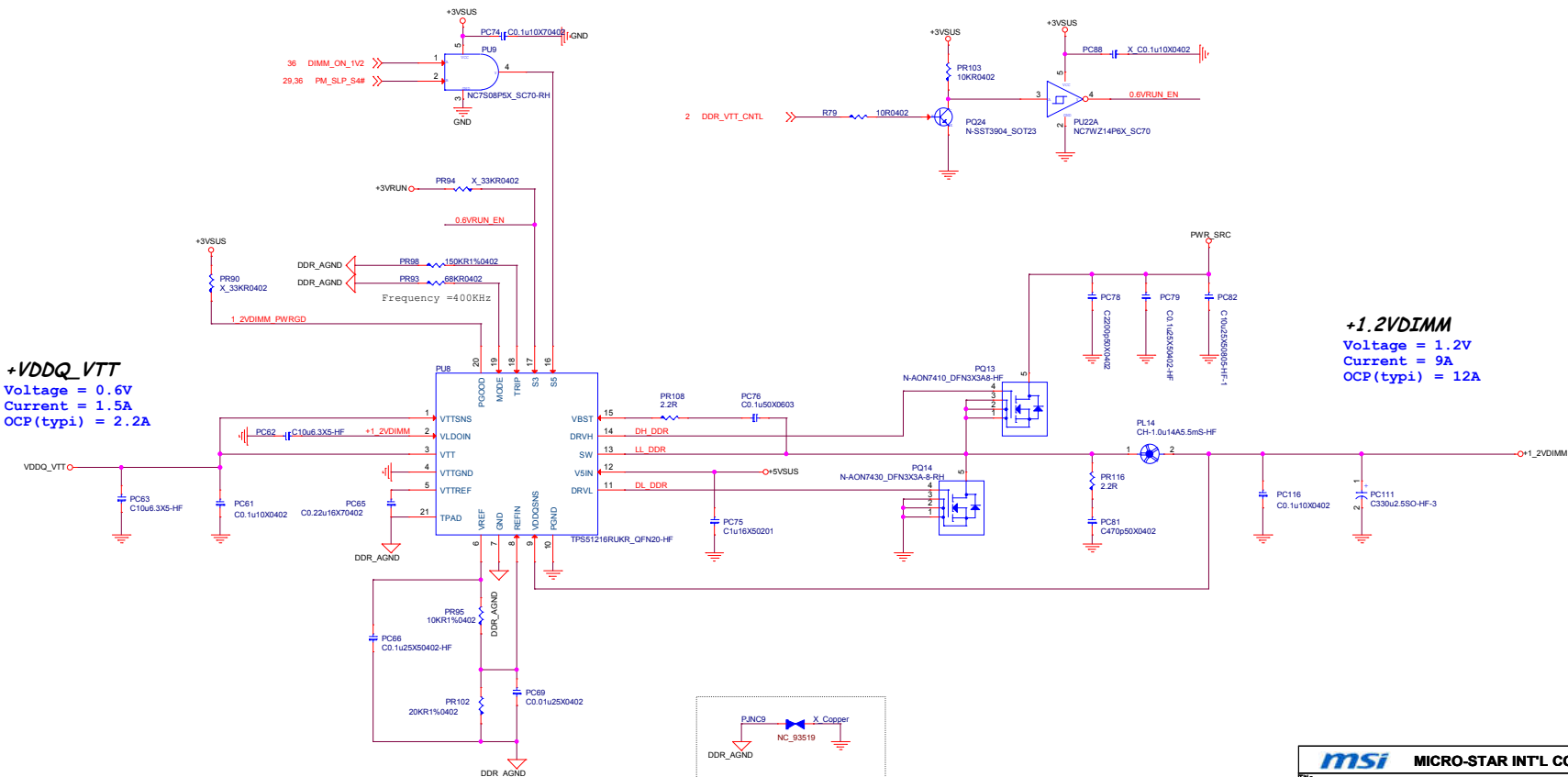
System Power



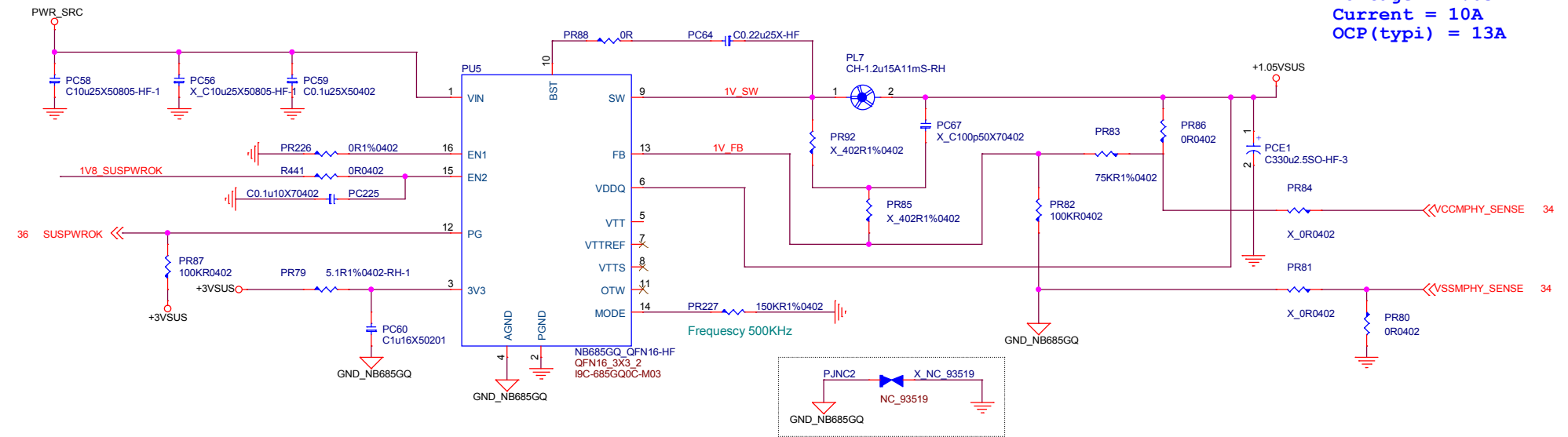
+2.5V_MEM (DDR4/Vpp)



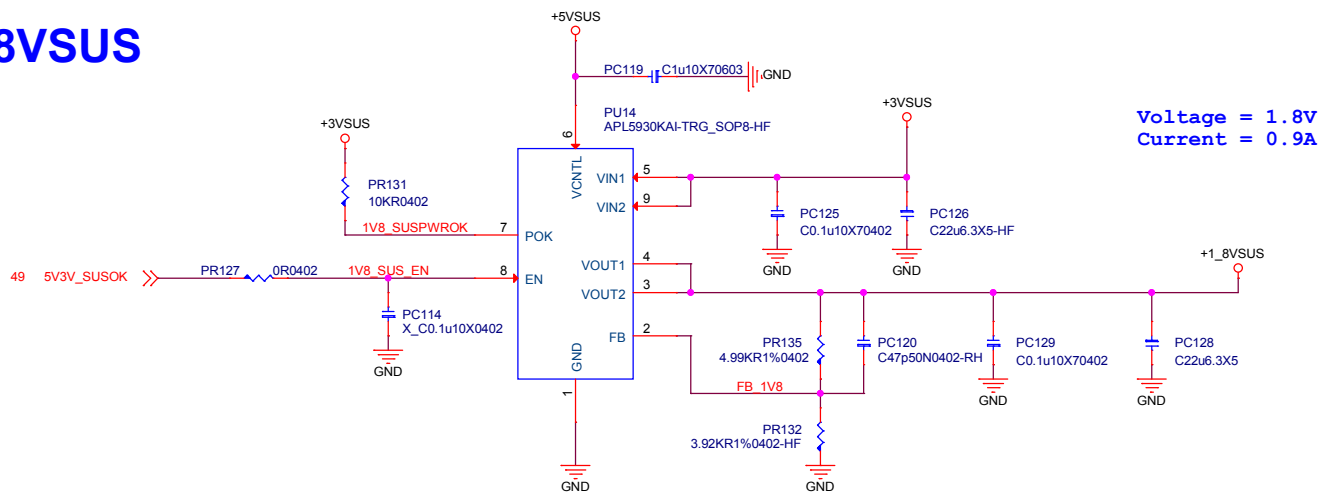
+1.2VDIMM / VDDQ_VTT(0.6V)



+1.05VSUS



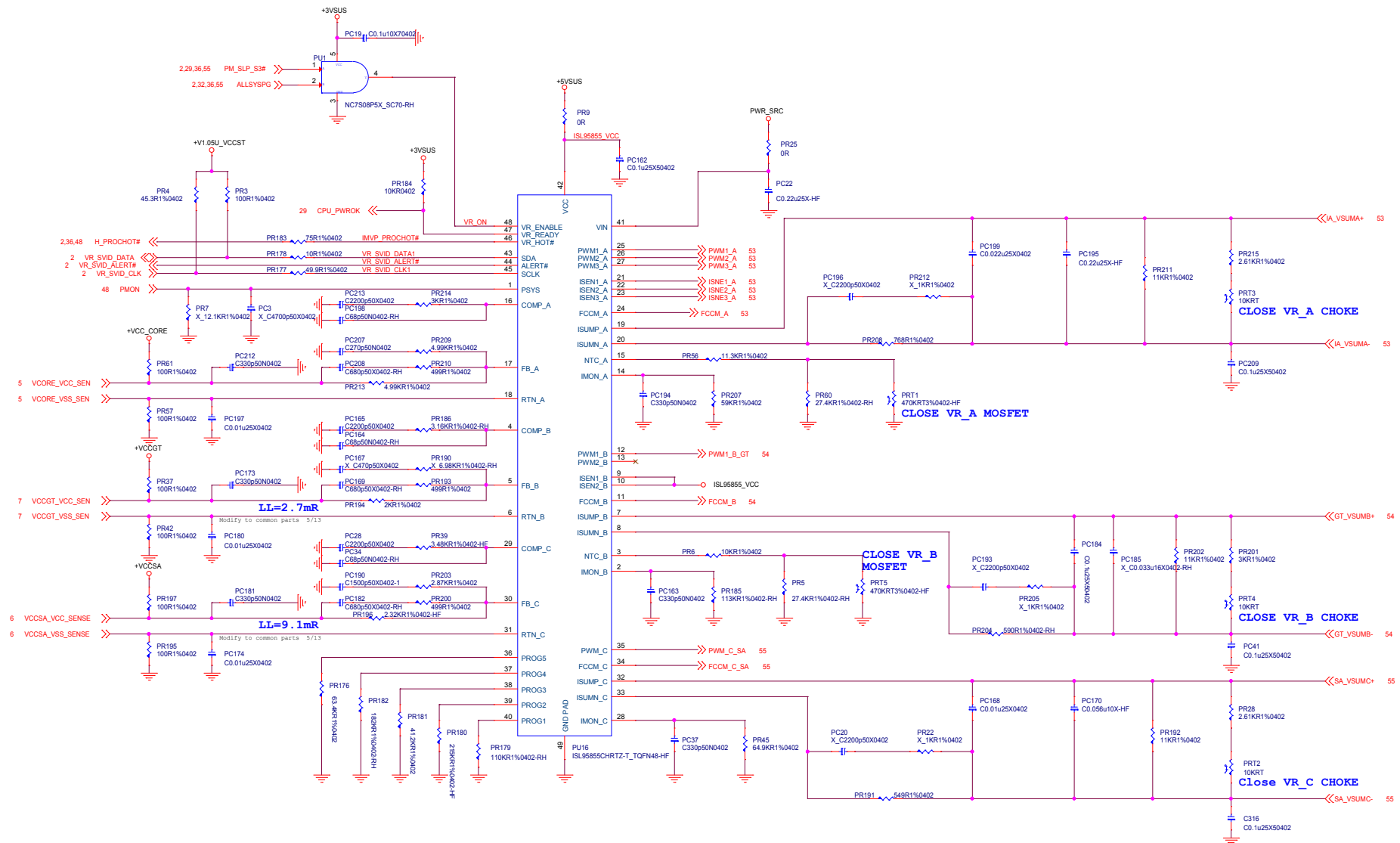
+1_8VSUS



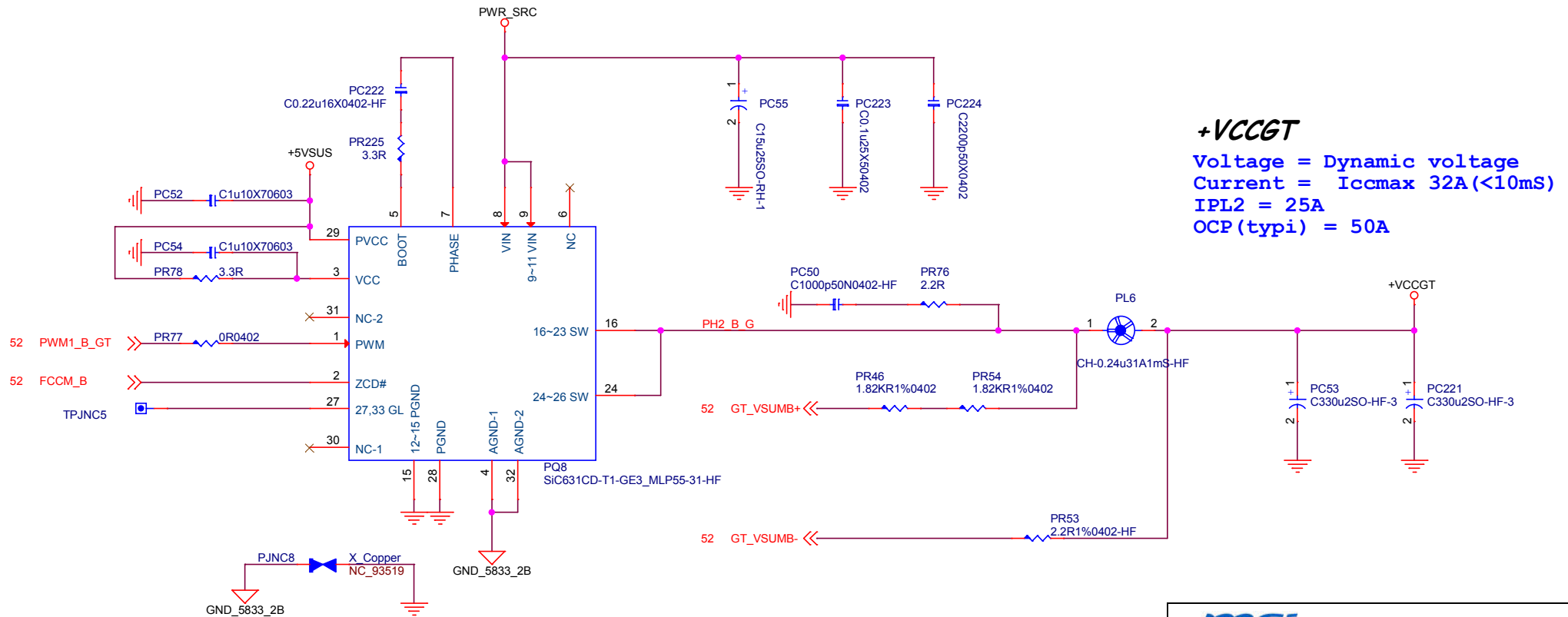
msi MICRO-STAR INT'L CO.,LTD.	
Title +1.05VSUS/+1_8VSUS	
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Coffee Lake H-line

6+2 45W ISL95855C




+VCCGT

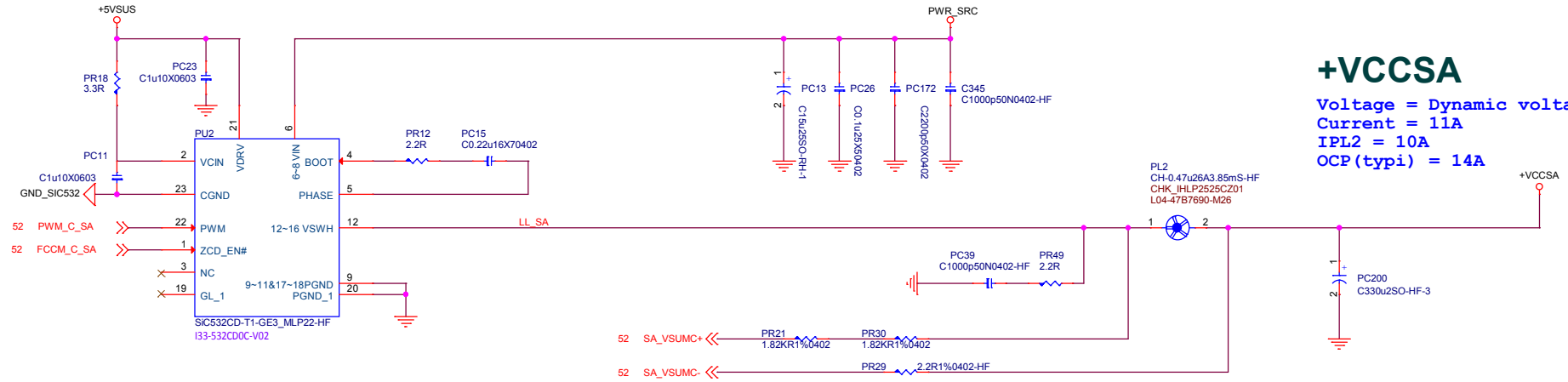


+VCCGT

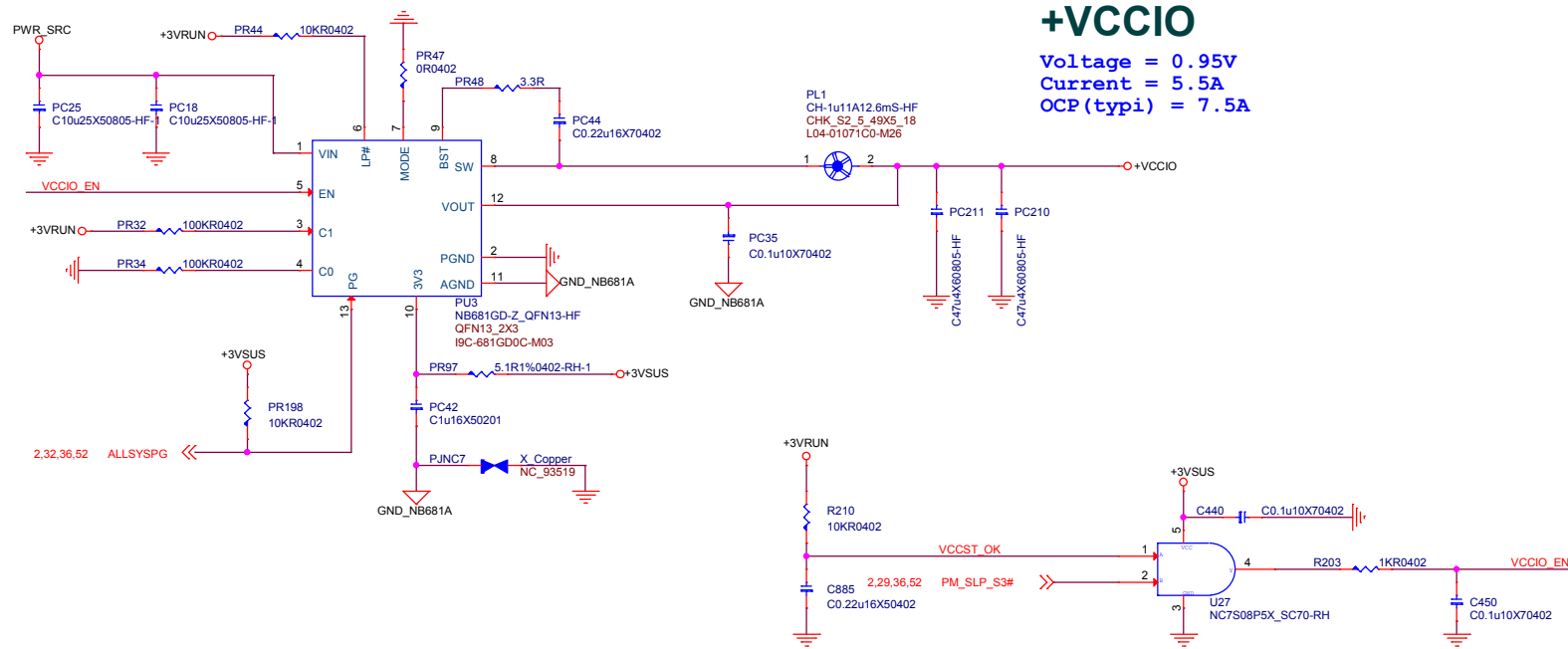
Voltage = Dynamic voltage
 Current = Iccmax 32A (<10ms)
 IPL2 = 25A
 OCP(typi) = 50A

		MICRO-STAR INT'L CO.,LTD.	
Title			
VCCGT			
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+VCCSA

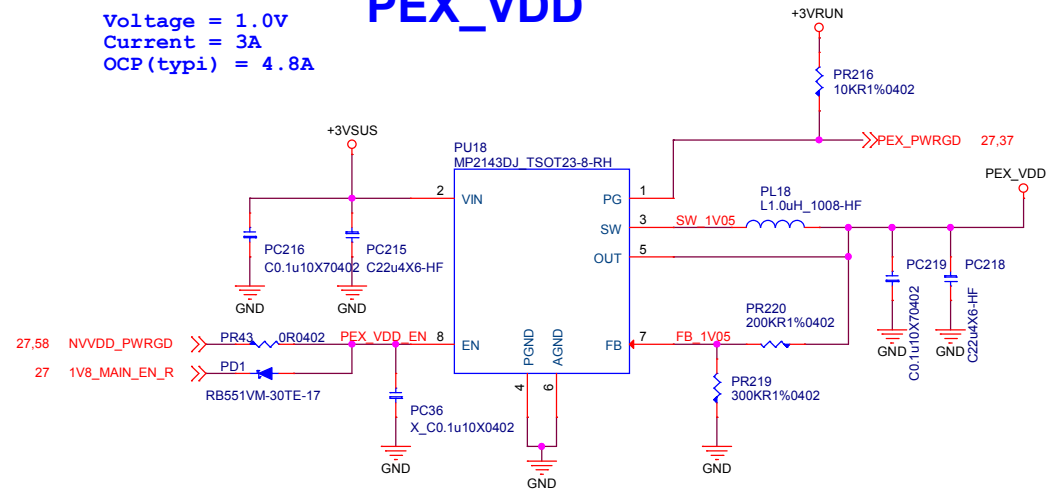


+VCCIO



Voltage = 1.0V
Current = 3A
OCP (typi) = 4.8A

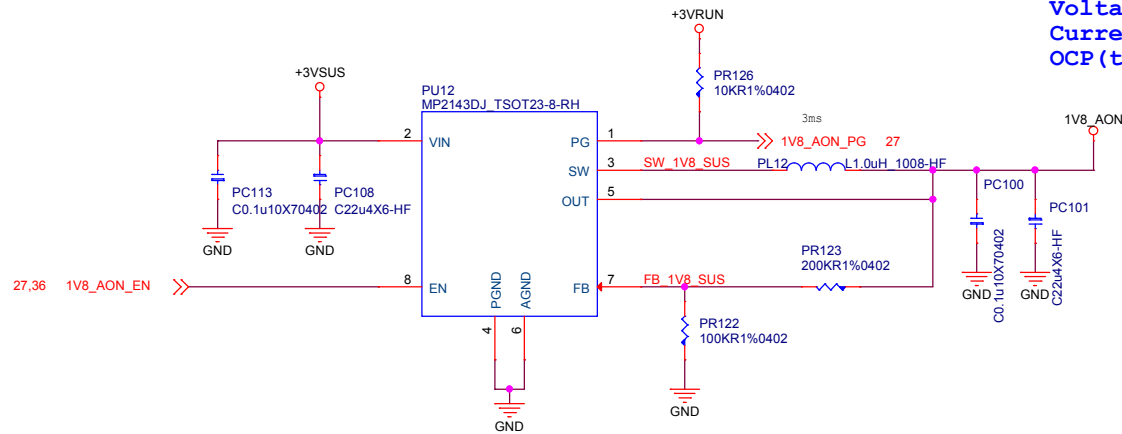
PEX_VDD



1V8_AON

1V8_AON

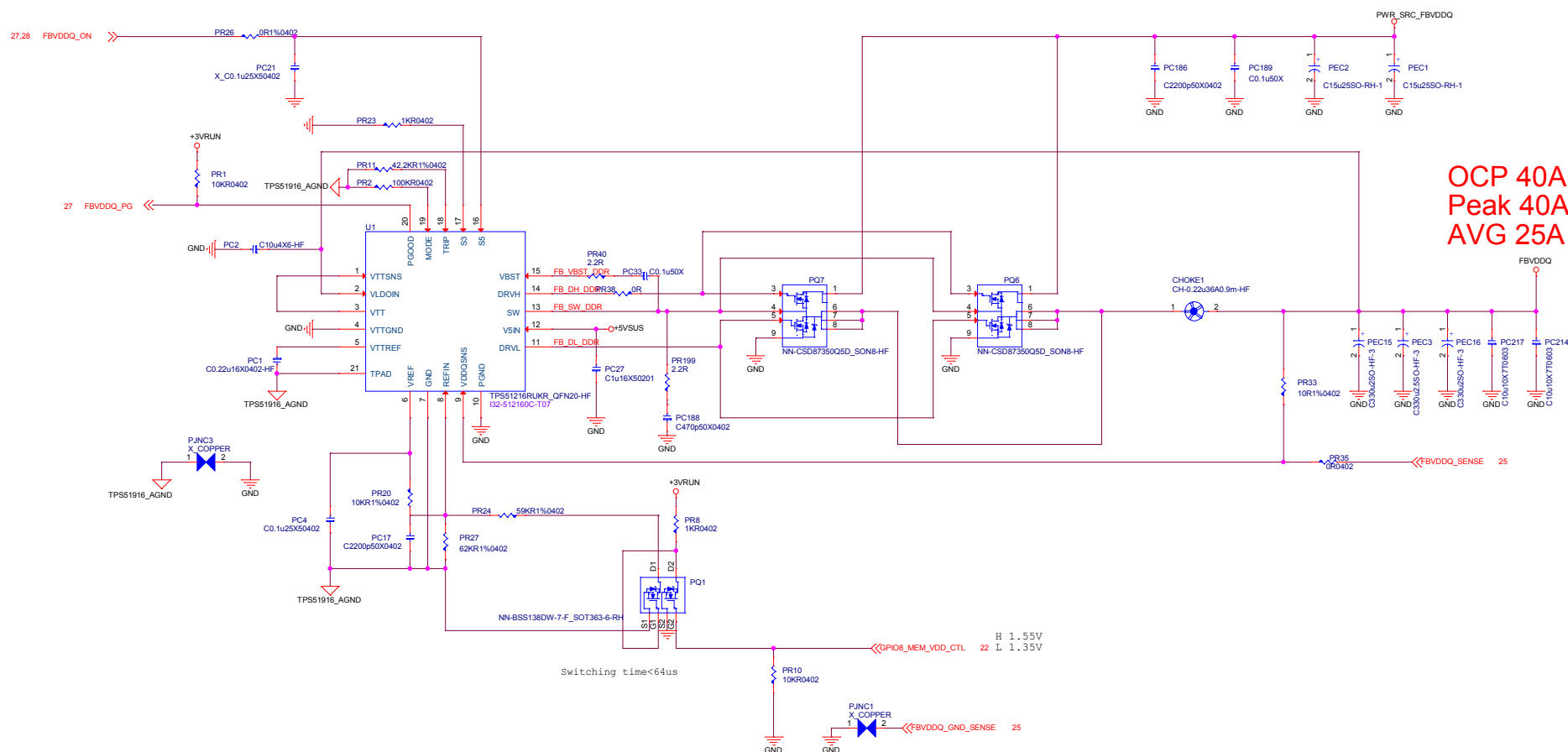
Voltage = 1.8V
Current = 2.26A
OCP (typi) = 4.8A




msi

MICRO-STAR INT'L CO.,LTD.

Title			1V8_AON/PEX_VDD
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OCP 40A
Peak 40A
AVG 25A

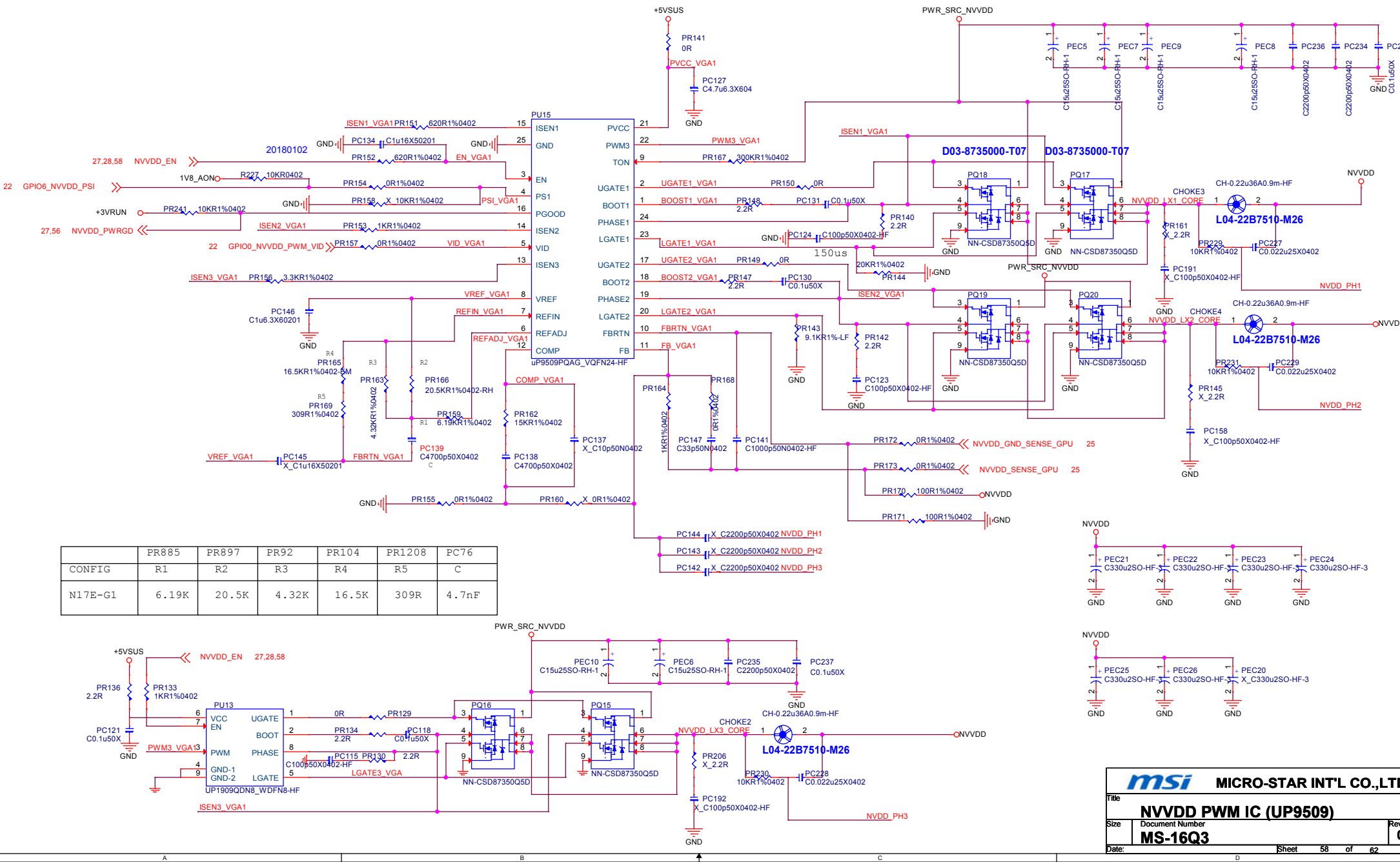
 MICRO-STAR INT'L CO.,LTD.	
Title DGPU POWER FBVDDQ	
Size Document Number MS-16Q3	Rev 0A
Date	Sheet 57 of 62

DGPU POWER / UP9509P

EDP-Peak 180A
EDP-Con 80A

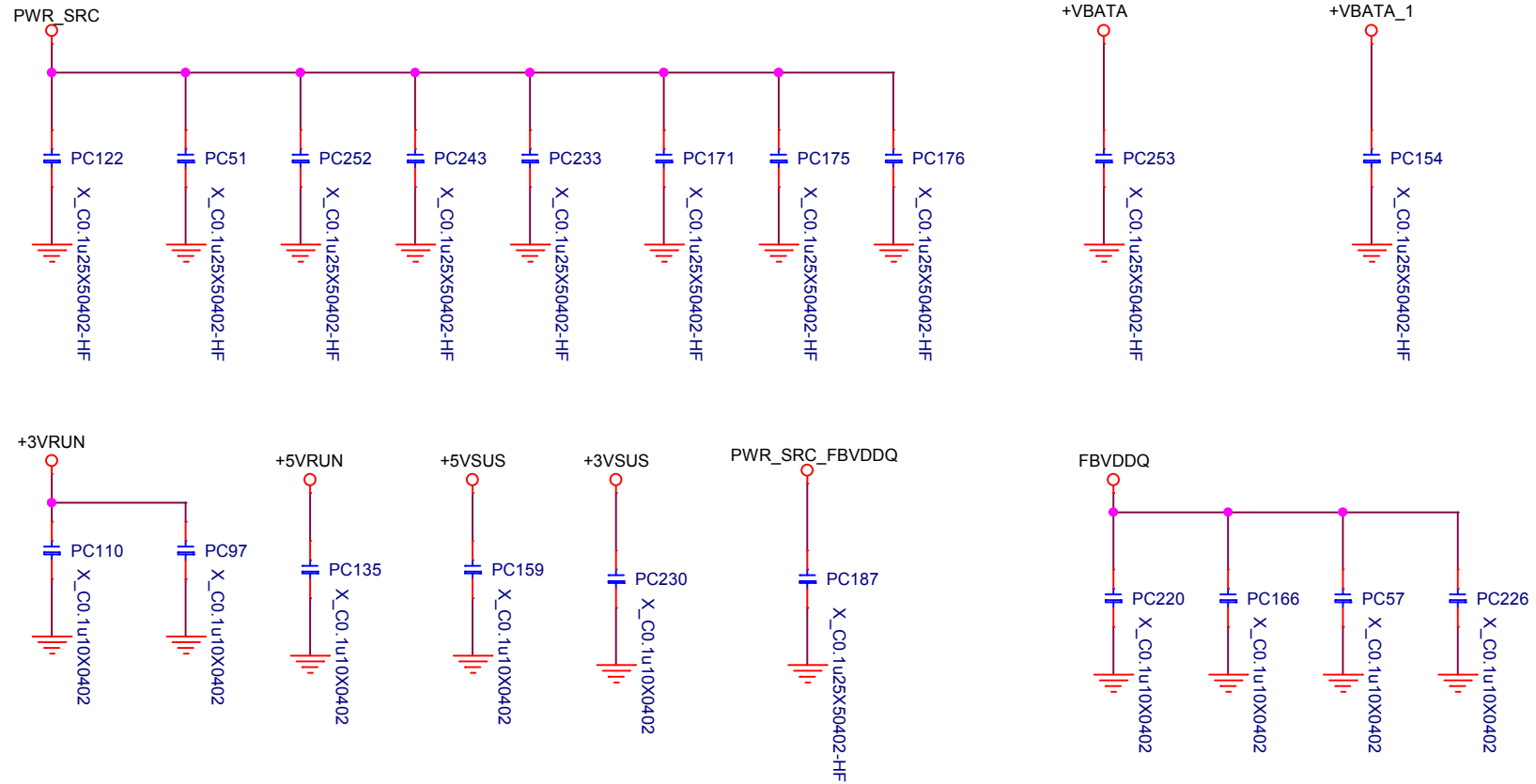
DGPU POWER NVVDD

VBoot:0.8V
Vmin:0.3V / Vmax:1.3V



	PR885	PR897	PR92	PR104	PR1208	PC76
CONFIG	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	4.7nF

EMI



MICRO-STAR INT'L CO.,LTD.

Title

EMI

Size
Custom

Document Number

MS-16Q3

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0A

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Monday, May 21, 2018

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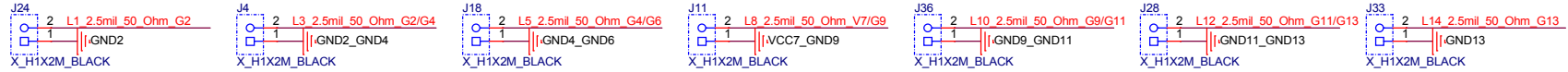
of

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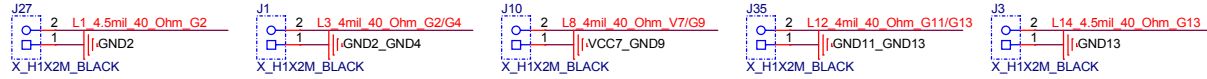
Impedance

Single End

50 ohm

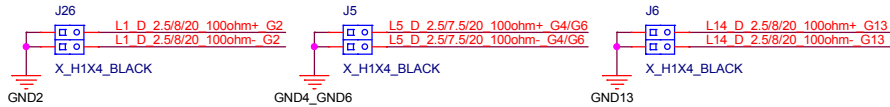


40 ohm

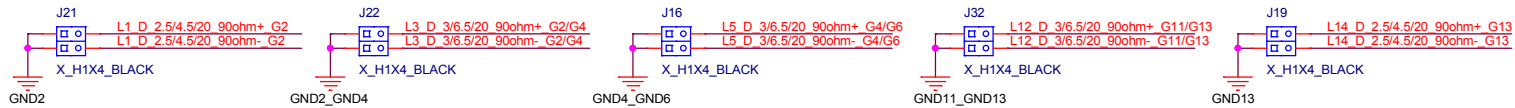


Differential

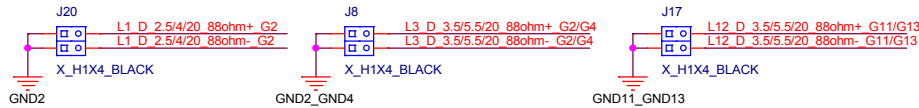
100 ohm



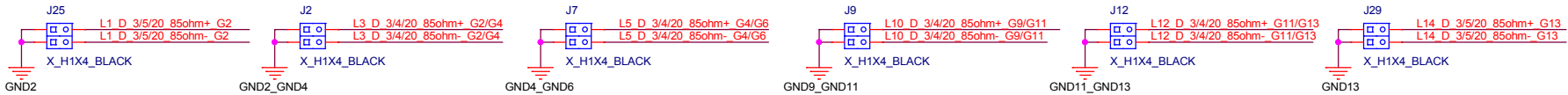
90 ohm



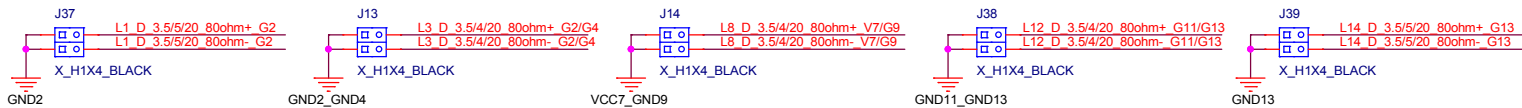
88 ohm



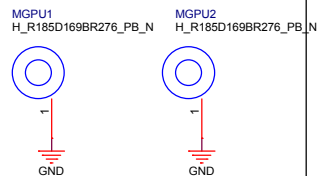
85 ohm



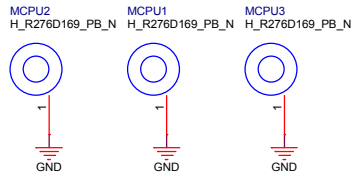
80 ohm



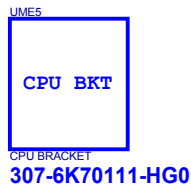
dGPU Holes



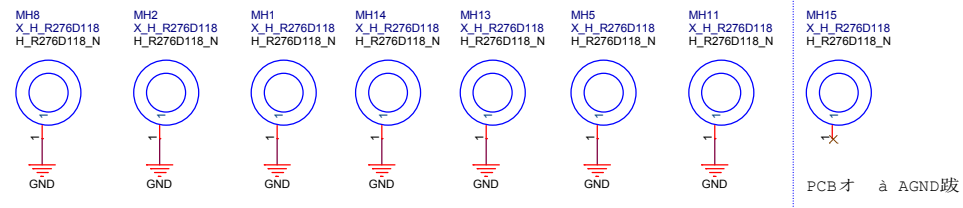
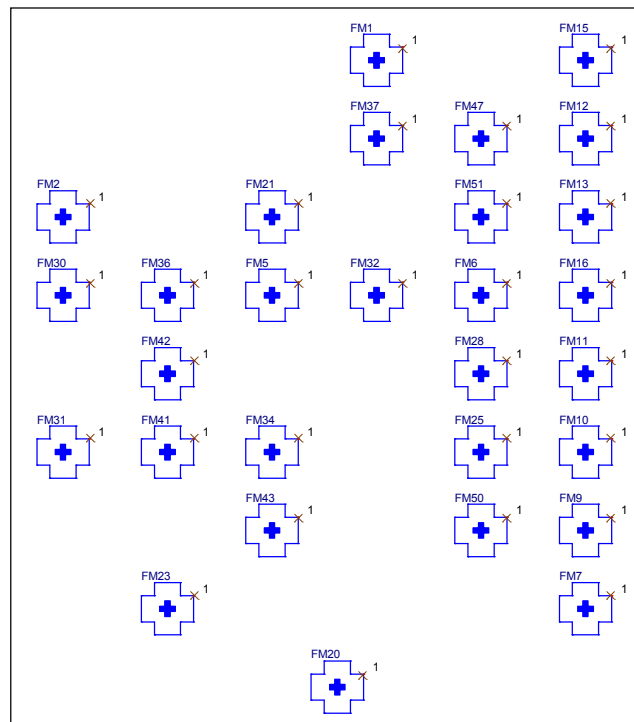
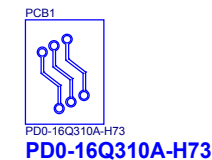
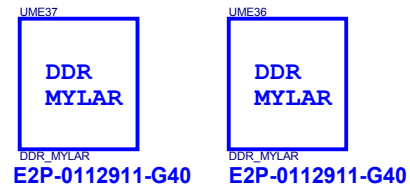
CPU Holes



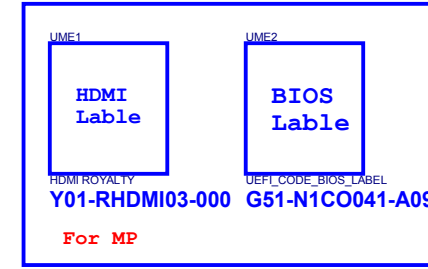
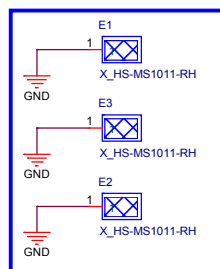
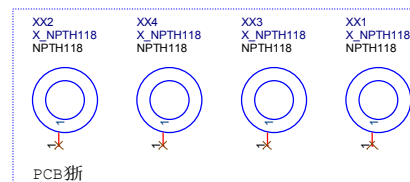
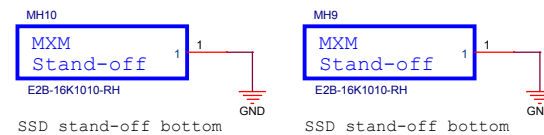
BKT



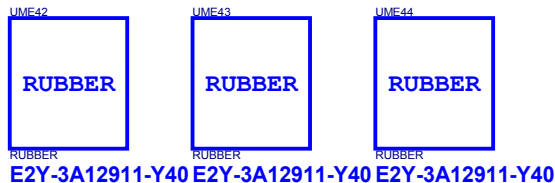
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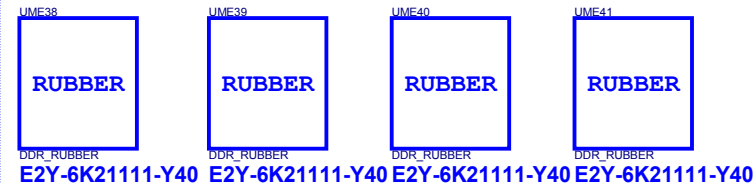
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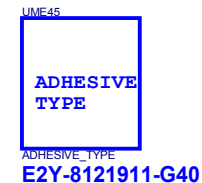
RUBBER

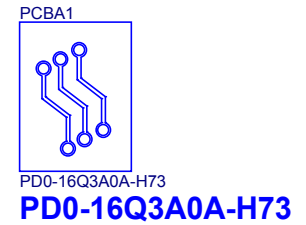
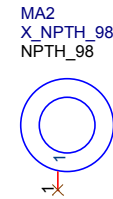
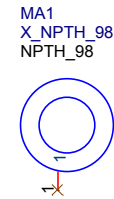
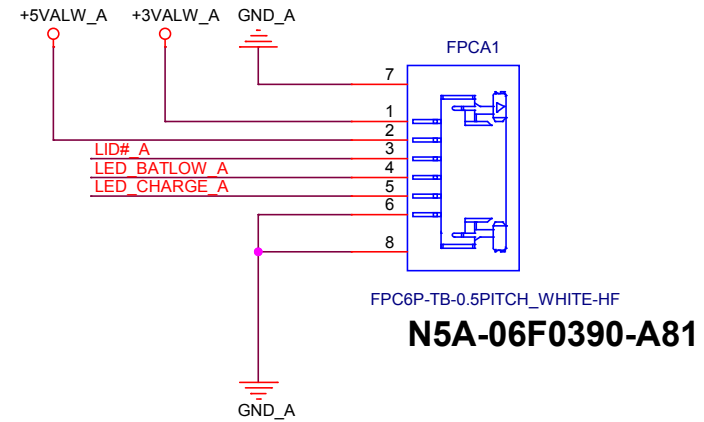
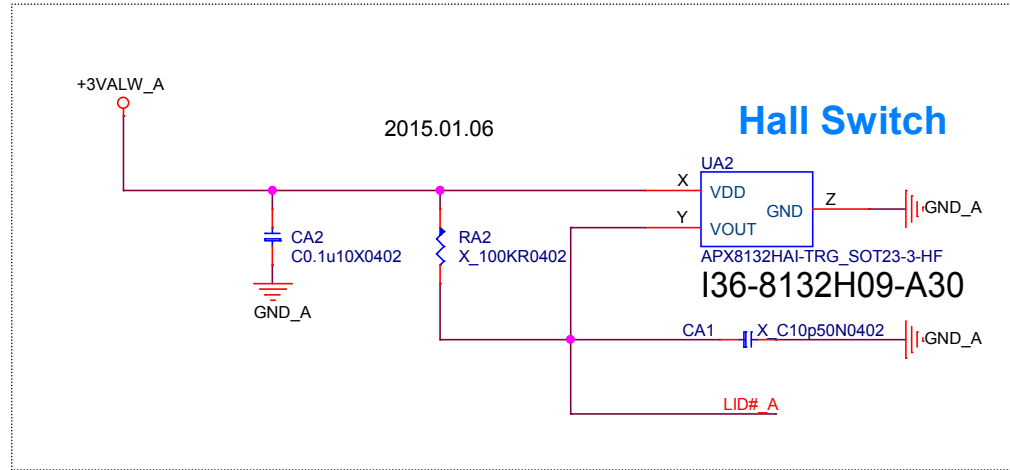
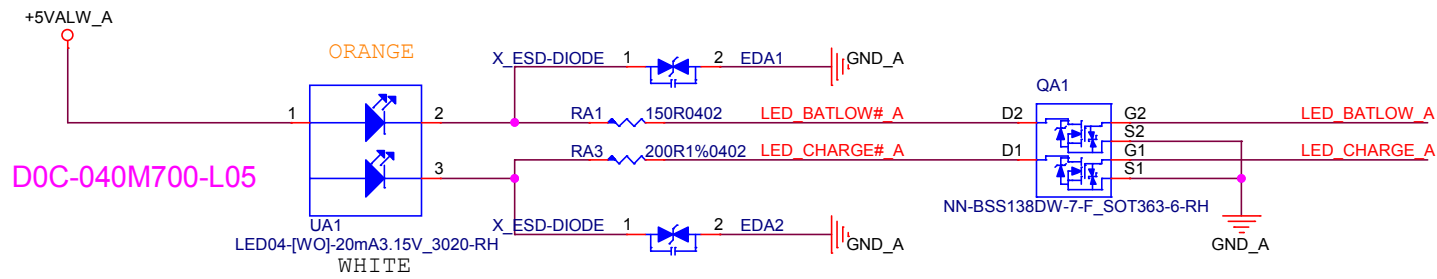



DDR_RUBBER



ADHESIVE_TYPE





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