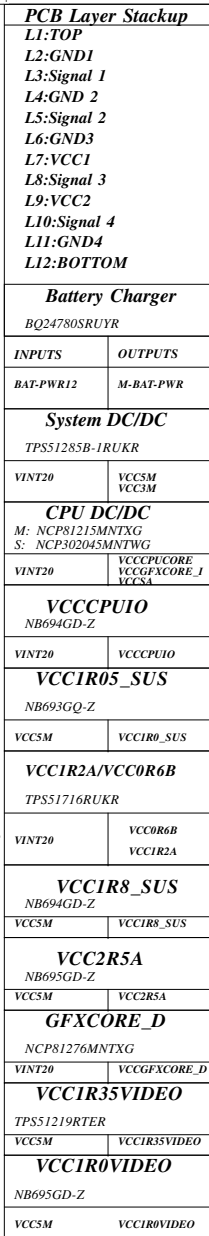



P15/P17 Schematic Page Number

001_ TITLE PAGE	047_Titan Ridge (1/3)	093_Power tree
002_BLOCK DIAGRAM	048_Titan Ridge (2/3)	094_BLANK
003_SYSTEM DEFINED	049_Titan Ridge (3/3)	095_BLANK
004_CPU CML-H : DDR4 CH-A	050_POWER DELIVERY (TPS65988)	096_BLANK
005_CPU CML-H : DDR4 CH-B	051_USB TYPE-C CONNECTOR(1/2)	097_BLANK
006_CPU CML-H : PEG/DMI	052_BLANK	098_BLANK
007_CPU CML-H : DDI/EDP	053_USB TYPE-C CONNECTOR(2/2)	099_BLANK
008_CPU CML-H : MISC/CLK/JTAG	054_eDP DEMUX	100_BLANK
009_CPU CML-H : GND	055_LCD CONNECTOR	101_DC-IN
010_CPU CML-H : VCC	056_BLANK	102_BATTERY INPUT
011_CPU CML-H : VCCGT	057_HDMI RETIMER	103_BATTERY CHARGER
012_CPU CML-H : VCCSA/VCCIO/VDD	058_HDMI CONNECTOR	104_BLANK
013_CPU CML-H : RSVD	059_dGPU board CONNECTOR	105_DC/DC VCC5M/VCC3M
014_PCH CML-H : CNV	060_BLANK	106_DC/DC VCC1R2A/VCC0R6B
015_PCH CML-H : SPI	061_M.2 SATA/PCIE SSD SLOT_1	107_DC/DC VCC2R5A
016_PCH CML-H : DMI/PCIE/USB	062_M.2 SATA/PCIE SSD SLOT_2	108_BLANK
017_PCH CML-H : SATA/PCIE	063_M.2 WLAN_2230	109_DC/DC IMVP8
018_PCH CML-H : AUDIO/SMBUS/JTAG	064_M.2 WWAN CARD SLOT	110_DC/DC VCCPUCORE 1
019_PCH CML-H : DDI CONTROL	065_GBE 1G LAN	111_DC/DC VCCPUCORE 2
020_PCH CML-H : USB3/LPC	066_GBE MAGNETICS	112_DC/DC VCCGFXCORE_I
021_PCH CML-H : CLK	067_GBE RJ45 CONNECTOR	113_DC/DC VCCSA
022_PCH CML-H : POWER	068_AUDIO CODEC	114_VCCPUCORE DECOUPLING1
023_PCH CML-H : GND/RSVD	069_HP/MIC/SPEAKER/DEBUG PORT	115_VCCPUCORE DECOUPLING2
024_PCH CML-H : UART/I2C	070_BLANK	116_DC/DC VCCCPUIO
025_RTC BATTERY	071_NPCX897KA0BX(1/3)	117_DC/DC VCC1R05_SUS
026_SPI FLASH	072_NPCX897KA0BX(2/3)	118_BLANK
027_DDR4 CH-A PRIMARY	073_NPCX897KA0BX(3/3)	119_DC/DC VCC1R8_SUS
028_DDR4 CH-A SECONDARY	074_THINK ENGINE 2(1/2)	120_BLANK
029_DDR4 CH-B PRIMARY	075_THINK ENGINE 2(2/2)	121_BLANK
030_DDR4 CH-B SECONDARY	076_FAN CONNECTOR	122_BLANK
031_BLANK	077_APS CONN.	123_BLANK
032_BLANK	078_USB Re-driver	124_BLANK
033_BLANK	079_BLANK	125_BLANK
034_BLANK	080_AOU USB POWER/CONN	126_BLANK
035_BLANK	081_APS G-SENSOR	127_BLANK
036_BLANK	082_DISCRETE TPM 2.0	128_LOAD SW VCCST/VCCSTG
037_BLANK	083_SMBUS SWITCH/eSPI DEBUG	129_LOAD SW PCH SUS/TP
038_BLANK	084_SMART CARD	130_LOAD SW LAN
039_BLANK	085_CAMERA/TOUCH	131_LOAD SW B
040_BLANK	086_KEYBOARD/TRACK POINT	132_LOAD SW WWAN&WLAN
041_BLANK	087_CLICK PAD	133_LOAD BOM
042_BLANK	088_Finger Print	
043_BLANK	089_Card Reader	
044_BLANK	090_IO/B CONN./POWER SWITCH	
045_TBT1 repeater	091_SCREW HOLE	
046_TBT2 repeater	092_Platform mPower Sequence	

NV N19P-O1/O3,N19E-O1/O3/O5,N18E-G2/G3

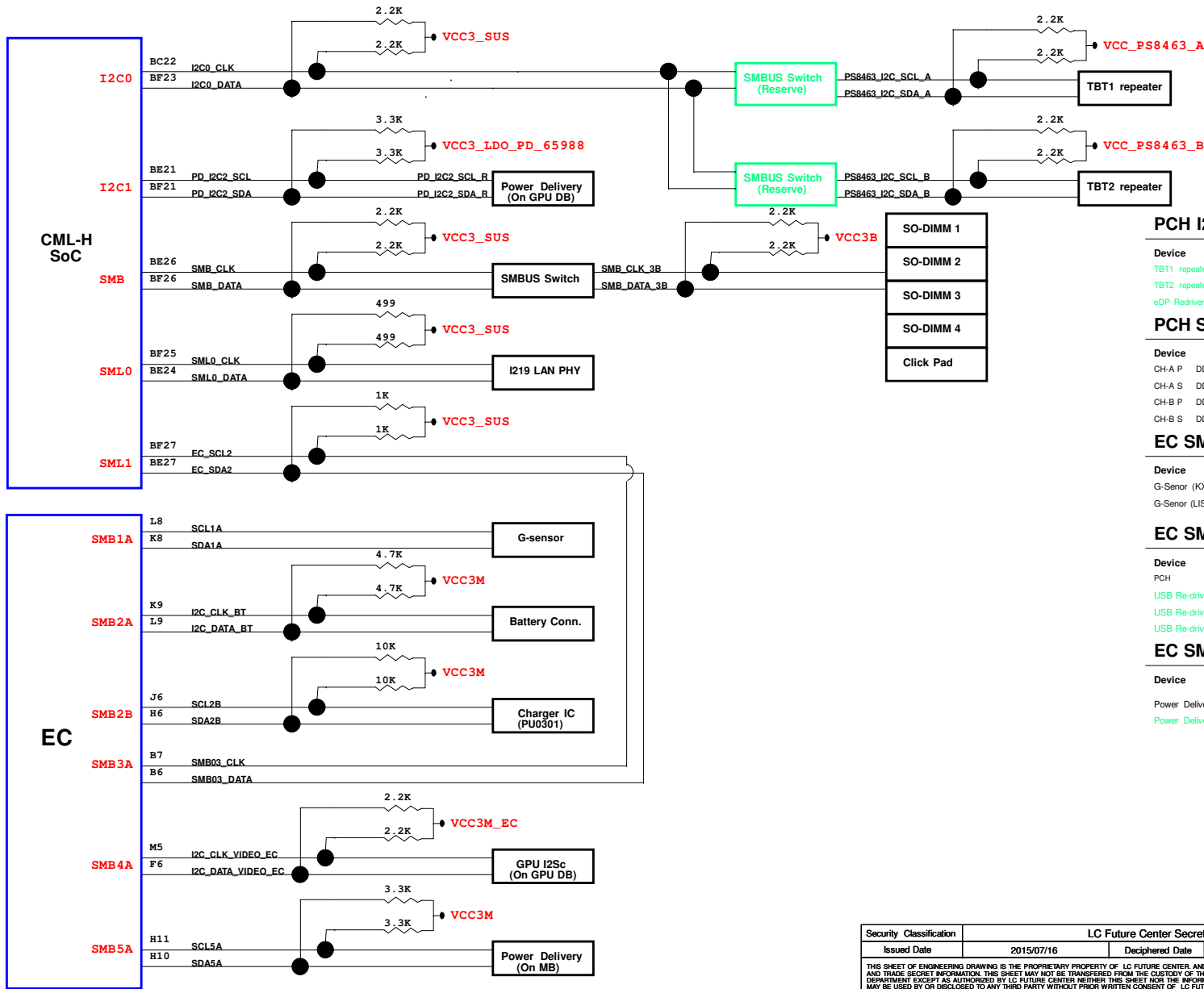
 **Internal Switch**

Title BLOCK DIAGRAM			
Size C	Document Number <div style="text-align: center; font-size: 1.5em; font-weight: bold;">Raptor</div>	Rev 0.1	
Date: Thursday, May 14, 2020		Sheet 2 of 133	

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TABLE: SYSTEM POWER STATE

Gx State (System State)	Sx State (System State)	Mx State (System State)	SW Power	M Power	SUS Power	AMT Power	A Power	B Power	User Observation	Chipset
G0	S0	M0	ON	ON	ON	ON	ON	ON	System Operating	Full On
G1	S3	M3	ON	ON	ON	ON	ON	OFF	Standby	Suspend-to-RAM (STR)
		M-OFF	ON	ON	ON	OFF	ON	OFF	Standby with USB wake enabled	
	Deep S3	M-OFF	ON	ON	OFF	OFF	ON	OFF	Standby	Suspend-to-Disk (STD)
	S4	M3	ON	ON	ON	ON	OFF	OFF	Hibernation with RTC wakeup	
G2	Deep S4	M-OFF	ON	ON	OFF	OFF	OFF	OFF	Hibernation or Shutdown	Soft Off
	S5	M3	ON	ON	ON	ON	OFF	OFF		
	Deep S5	M-OFF	ON	ON	OFF	OFF	OFF	OFF		
G3	S5 EC OFF	M-OFF	OFF	OFF	OFF	OFF	OFF	OFF	No Power	Mechanical Off
	---	---	OFF	OFF	OFF	OFF	OFF	OFF		



PCH I2C0 address

Device	Address
TBT1 repeater (8463)	0x10h-0x2Fh (Reserve)
TBT2 repeater (8463)	0x90h-0x9Fh ; 0xD0h-0xDFh (Reserve)
eDP Redriver (8461)	0x90h-0x9Fh ; 0xD0h-0xDFh (Reserve)

PCH I2C1 address

Device	Address
Power Delivery (65988)	0x70h / 0x71h

PCH SM Bus address

Device	Address
CH-A P DDR DIMM0	0xA0h
CH-A S DDR DIMM1	0xA2h
CH-B P DDR DIMM2	0xA4h
CH-B S DDR DIMM3	0xA6h

PCH SM L0 address

Device	Address
Intel Lan_I219	0XC8h

EC SMBus1 address

Device	Address
G-Senor (KX022-1020)	0x3Ch (W) / 0x3Dh (R)
G-Senor (LIS2DWLTR)	0x30h (W) / 0x31h (R)

EC SMBus2 address

Device	Address
Smart Battery note:P15P17 Battery P/N is not already yet	0x16h
Charge Controller	0x12h

EC SMBus3 address

Device	Address
PCH	0x4Ch (W) / 0x4Bh (R)
USB Re-driver (8735)	0x20h / 0x21h (Reserve)
USB Re-driver (8713)	0x52h / 0x53h (Reserve)
USB Re-driver (8713)	0x52h / 0x53h (Reserve)

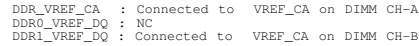
EC SMBus4 address


Device	Address
DGPU	0x9Eh
HDMI Re-timer (8409A)	0x10h-0x2Fh (Reserve)

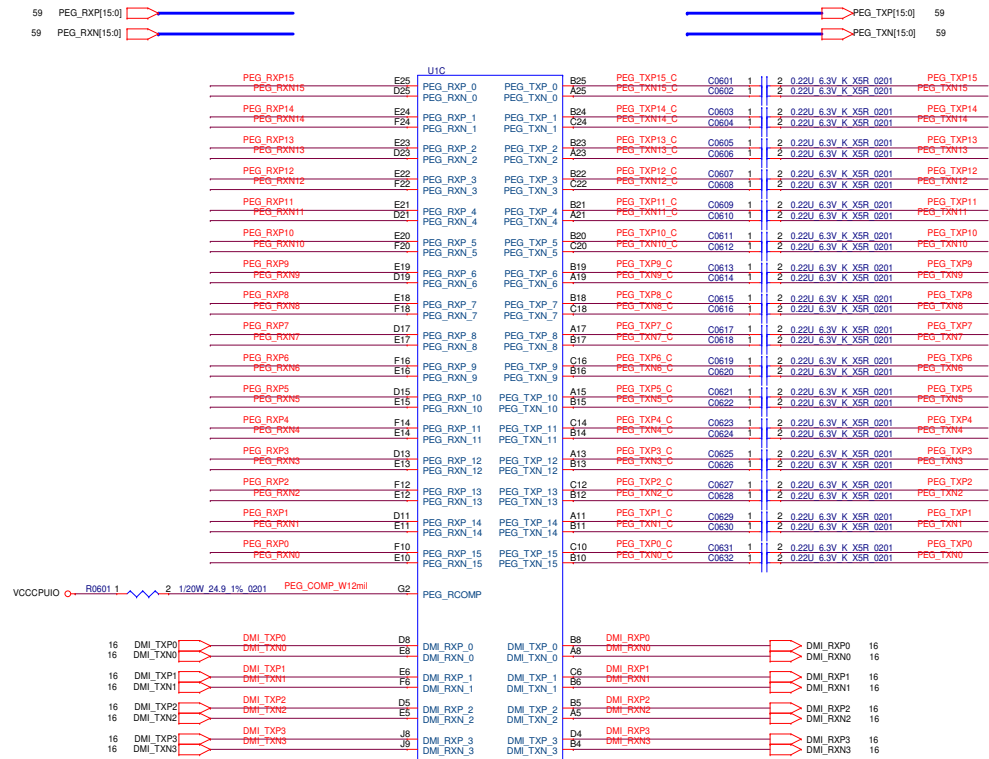
EC SMBus5 address

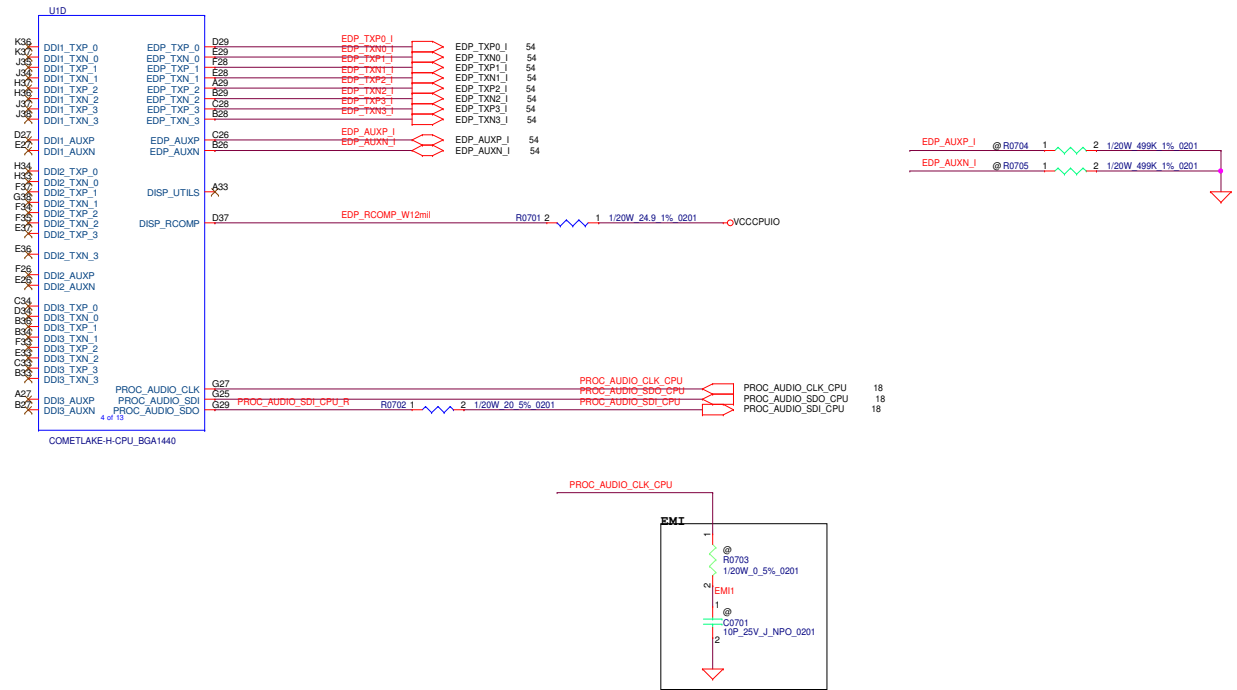
Device	Address
Power Delivery (65988)	Port1 : 0x46h / 0x47h Port2 : 0x4Fh / 0x4Eh
Power Delivery (65988)	0x46h / 0x47h (Reserve)

UJA					
BR6	DDRR_DQ_0,DDR0_DQ_0	DDRR_CK1_0,DDR0_CK1_0	AG1	M_A_DORCLK0_2400M	M_A_DORCLK0_2400M
BR7	DDRR_DQ_1,DDR0_DQ_1	DDRR_CK1_1,DDR0_CK1_1	AG2	M_A_DORCLK1_2400M	M_A_DORCLK1_2400M
BR8	DDRR_DQ_2,DDR0_DQ_2	DDRR_CK1_2,DDR0_CK1_2	AG3	M_A_DORCLK2_2400M	M_A_DORCLK2_2400M
BR9	DDRR_DQ_3,DDR0_DQ_3	DDRR_CK1_3,DDR0_CK1_3	AL1	M_A_DORCLK3_2400M	M_A_DORCLK3_2400M
BR10	DDRR_DQ_4,DDR0_DQ_4	NC,DDR0_CK1_4	AK3	M_A_DORCLK2_2400M	M_A_DORCLK2_2400M
BR11	DDRR_DQ_5,DDR0_DQ_5	NC,DDR0_CK1_5	AK4	M_A_DORCLK3_2400M	M_A_DORCLK3_2400M
BR12	DDRR_DQ_6,DDR0_DQ_6	NC,DDR0_CK1_6	AL1	M_A_DORCLK3_2400M	M_A_DORCLK3_2400M
BR13	DDRR_DQ_7,DDR0_DQ_7	NC,DDR0_CK1_7			
BR14	DDRR_DQ_8,DDR0_DQ_8		AT1	M_A_CKE0	M_A_CKE0 27
BR15	DDRR_DQ_9,DDR0_DQ_9	DDRR_CKE_0,DDR0_CKE_0	AT2	M_A_CKE1	M_A_CKE1 27
BR16	DDRR_DQ_10,DDR0_DQ_10	DDRR_CKE_1,DDR0_CKE_1	AT3	M_A_CKE2	M_A_CKE2 27
BR17	DDRR_DQ_11,DDR0_DQ_11	DDRR_CKE_2,DDR0_CKE_2	AT4	M_A_CKE3	M_A_CKE3 28
BR18	DDRR_DQ_12,DDR0_DQ_12	DDRR_CKE_3,DDR0_CKE_3			
BR19	DDRR_DQ_13,DDR0_DQ_13		AD5	M_A_CS0	M_A_CS0 27
BR20	DDRR_DQ_14,DDR0_DQ_14	DDRR_CSM_0,DDR0_CSM_0	AE2	M_A_CS1	M_A_CS1 27
BR21	DDRR_DQ_15,DDR0_DQ_15	DDRR_CSM_1,DDR0_CSM_1	AE3	M_A_CS2	M_A_CS2 28
BR22	DDRR_DQ_16,DDR0_DQ_16	NC,DDR0_CSM_2	AE4	M_A_CS3	M_A_CS3 28
BR23	DDRR_DQ_17,DDR0_DQ_17	NC,DDR0_CSM_3			
BR24	DDRR_DQ_18,DDR0_DQ_18		AD3	M_A_ODT0	M_A_ODT0 27
BR25	DDRR_DQ_19,DDR0_DQ_19	DDRR_ODT_0,DDR0_ODT_0	AE4	M_A_ODT1	M_A_ODT1 27
BR26	DDRR_DQ_20,DDR0_DQ_20	NC,DDR0_ODT_1	AE1	M_A_ODT2	M_A_ODT2 28
BR27	DDRR_DQ_21,DDR0_DQ_21	NC,DDR0_ODT_2	AD4		M_A_ODT3 28
BR28	DDRR_DQ_22,DDR0_DQ_22	NC,DDR0_ODT_3			
BR29	DDRR_DQ_23,DDR0_DQ_23		AH5	M_A_BA0	M_A_BA0 27,28
BR30	DDRR_DQ_24,DDR0_DQ_24	DDRR_CAB_4,DDR0_CAB_4	AH1	M_A_BA1	M_A_BA1 27,28
BR31	DDRR_DQ_25,DDR0_DQ_25	DDRR_CAB_5,DDR0_CAB_5	AH1	M_A_B0A	M_A_B0A 27,28
BR32	DDRR_DQ_26,DDR0_DQ_26	DDRR_CAB_6,DDR0_CAB_6			
BR33	DDRR_DQ_27,DDR0_DQ_27	DDRR_CAB_7,DDR0_CAB_7	AH4	M_A_A16_RAS_N	M_A_A16_RAS_N 27,28
BR34	DDRR_DQ_28,DDR0_DQ_28	DDRR_CAB_8,DDR0_CAB_8	AG4	M_A_A16_WE_N	M_A_A16_WE_N 27,28
BR35	DDRR_DQ_29,DDR0_DQ_29	DDRR_CAB_9,DDR0_CAB_9	AD1	M_A_A16_CAS_N	M_A_A16_CAS_N 27,28
BR36	DDRR_DQ_30,DDR0_DQ_30	DDRR_CAB_1,DDR0_CAB_1	AH5		
BR37	DDRR_DQ_31,DDR0_DQ_31		AD1	M_A_A0	M_A_A0_9.1 27,28
BR38	DDRR_DQ_32,DDR0_DQ_32	DDRR_CAB_8,DDR0_CAB_8	AH1	M_A_A1	
BR39	DDRR_DQ_33,DDR0_DQ_33	DDRR_CAB_8,DDR0_CAB_8	AN1	M_A_A2	
BR40	DDRR_DQ_34,DDR0_DQ_34	DDRR_CAB_5,DDR0_CAB_5	AP5	M_A_A3	
BR41	DDRR_DQ_35,DDR0_DQ_35	NC,DDR0_CAB_4	AP2	M_A_A4	
BR42	DDRR_DQ_36,DDR0_DQ_36	NC,DDR0_CAB_4	AP1	M_A_A5	
BR43	DDRR_DQ_37,DDR0_DQ_37	DDRR_CAA_2,DDR0_CAA_2	AP3	M_A_A6	
BR44	DDRR_DQ_38,DDR0_DQ_38	DDRR_CAA_2,DDR0_CAA_2	AN1	M_A_A7	
BR45	DDRR_DQ_39,DDR0_DQ_39	DDRR_CAA_4,DDR0_CAA_4	AP3	M_A_A8	
BR46	DDRR_DQ_40,DDR0_DQ_40	DDRR_CAA_3,DDR0_CAA_3	AT4	M_A_A9	
BR47	DDRR_DQ_41,DDR0_DQ_41	DDRR_CAA_1,DDR0_CAB_1	AH2	M_A_A10_AP	M_A_A10 AP 27,28
BR48	DDRR_DQ_42,DDR0_DQ_42	DDRR_CAB_7,DDR0_CAB_7	AN2	M_A_A11	M_A_A11 27,28
BR49	DDRR_DQ_43,DDR0_DQ_43	DDRR_CAA_7,DDR0_CAB_11	AL4	M_A_A12	M_A_A12 27,28
BR50	DDRR_DQ_44,DDR0_DQ_44	DDRR_CAA_7,DDR0_CAB_12	AL2	M_A_A13	M_A_A13 27,28
BR51	DDRR_DQ_45,DDR0_DQ_45	DDRR_CAB_8,DDR0_CAB_13	AL3	M_A_A14	M_A_A14 27,28
BR52	DDRR_DQ_46,DDR0_DQ_46	DDRR_CAA_8,DDR0_CAB_15	UA	M_A_ACT	M_A_ACT 27,28
BR53	DDRR_DQ_47,DDR0_DQ_47	DDRR_CAA_8,DDR0_CAB_16			
BR54	DDRR_DQ_48,DDR0_DQ_48		AG3	M_A_PARITY	M_A_PARITY 27,28
BR55	DDRR_DQ_49,DDR0_DQ_49	NC,DDR0_PAR	AU5	M_A_ALERT	M_A_ALERT 27,28
BR56	DDRR_DQ_50,DDR0_DQ_50	NC,DDR0_ALERT1			
BR57	DDRR_DQ_51,DDR0_DQ_51				
BR58	DDRR_DQ_52,DDR0_DQ_52		BR5	M_A_DQSG	M_A_DQSG[0..7] 27,28
BR59	DDRR_DQ_53,DDR0_DQ_53	DD			

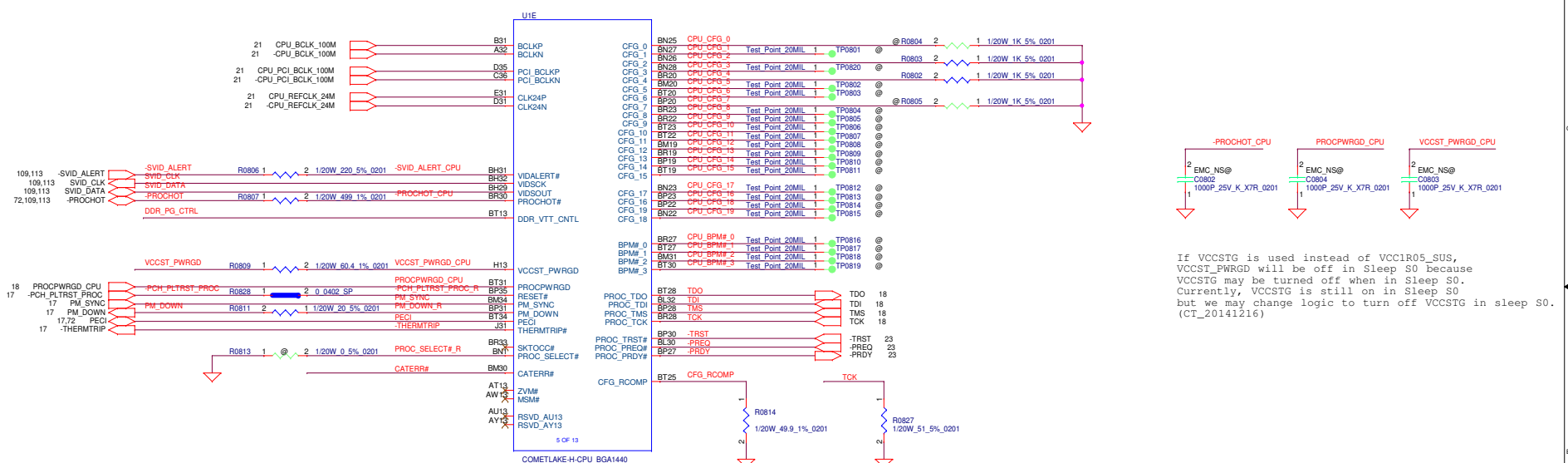
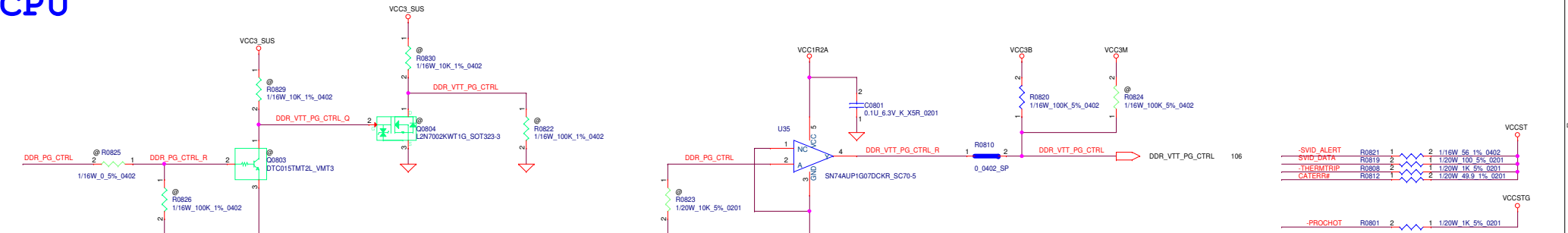


Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/07/16	Deciphered Date	2016/01/16	CPU CML-H : DDR4 CH-B	
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				Date: Thursday, May 14, 2020	Sheet 5 of 133

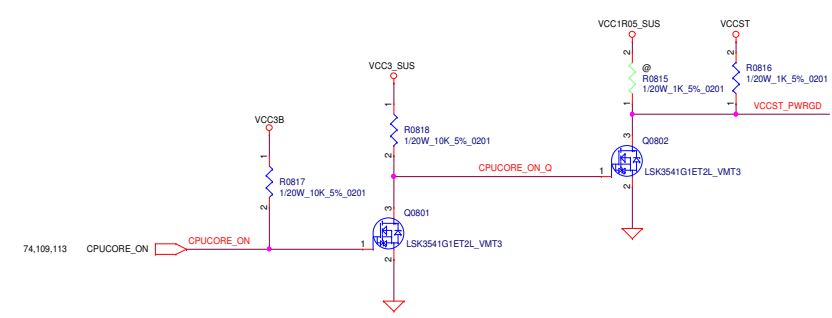




CPU




If VCCSTG is used instead of VCC1R05_SUS, VCCSTG_PWRGD will be off in Sleep S0 because VCCSTG may be turned off when in Sleep S0. Currently, VCCSTG is still on in Sleep S0 but we may change logic to turn off VCCSTG in sleep S0. (CT_20141216)



VCCST_PWRGD requirements

- 1) Indication that the VCCST/VDDQ power supplies are stable and within specification
- 2) VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
- 3) VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.

TABLE	CFG[19:0] pin has internal Pull up to VCCCPUPIO with 5-8 k ohm.
CFG[0] : Stall reset sequence after CPU PLL lock until de-asserted:	
1 : No Stall	<----- LOGIC
0 : Stall	
CFG[2] : PEG Static Lane Reversal	
1 : Normal Operation	
0 : Lane Reversal	<----- LOGIC
CFG[4] : eDP enable	
1 : Disabled	
0 : Enabled	<----- LOGIC
CFG[6:5] : PEG Bifurcation, bus#:dev#:func#=0:1:0	
11 : 1x16	<----- LOGIC
CFG[7] : PEG Training	
1 : PEG Train immediately following RESET# deassertion	<----- LOGIC
0 : PEG Wait for BIOS for training	
CFG[19:8] : Reserved	
For x16 Reversal Lanes - CFG[6/5/2]	setting is 110
For x4 Reversal Lanes - CFG[6/5/2]	setting is 000

Security Classification	LC Future Center Secret Data			Title	
Issued Date	2015/07/16	Deciphered Date	2016/01/16	CPU CML-H : MISC/CLK/JTAG	
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Date: Thursday, May 14, 2020				Sheet 8 of 133	

UIF		AK4	
A10	VSS 1VSS 82	AK4	AK4
A12	VSS 2VSS 83	AK10	AK10
A16	VSS 2VSS 84	AK14	AK14
A18	VSS 2VSS 85	AK18	AK18
A20	VSS 2VSS 86	AK22	AK22
A22	VSS 2VSS 87	AK26	AK26
A24	VSS 2VSS 88	AK30	AK30
A26	VSS 2VSS 89	AK34	AK34
A28	VSS 2VSS 90	AK38	AK38
A30	VSS 2VSS 91	AK42	AK42
A32	VSS 2VSS 92	AK46	AK46
A34	VSS 2VSS 93	AK50	AK50
A36	VSS 2VSS 94	AK54	AK54
A38	VSS 2VSS 95	AK58	AK58
A40	VSS 2VSS 96	AK62	AK62
A42	VSS 2VSS 97	AK66	AK66
A44	VSS 2VSS 98	AK70	AK70
A46	VSS 2VSS 99	AK74	AK74
A48	VSS 2VSS 100	AK78	AK78
A50	VSS 2VSS 101	AK82	AK82
A52	VSS 2VSS 102	AK86	AK86
A54	VSS 2VSS 103	AK90	AK90
A56	VSS 2VSS 104	AK94	AK94
A58	VSS 2VSS 105	AK98	AK98
A60	VSS 2VSS 106	AK102	AK102
A62	VSS 2VSS 107	AK106	AK106
A64	VSS 2VSS 108	AK110	AK110
A66	VSS 2VSS 109	AK114	AK114
A68	VSS 2VSS 110	AK118	AK118
A70	VSS 2VSS 111	AK122	AK122
A72	VSS 2VSS 112	AK126	AK126
A74	VSS 2VSS 113	AK130	AK130
A76	VSS 2VSS 114	AK134	AK134
A78	VSS 2VSS 115	AK138	AK138
A80	VSS 2VSS 116	AK142	AK142
A82	VSS 2VSS 117	AK146	AK146
A84	VSS 2VSS 118	AK150	AK150
A86	VSS 2VSS 119	AK154	AK154
A88	VSS 2VSS 120	AK158	AK158
A90	VSS 2VSS 121	AK162	AK162
A92	VSS 2VSS 122	AK166	AK166
A94	VSS 2VSS 123	AK170	AK170
A96	VSS 2VSS 124	AK174	AK174
A98	VSS 2VSS 125	AK178	AK178
A100	VSS 2VSS 126	AK182	AK182
A102	VSS 2VSS 127	AK186	AK186
A104	VSS 2VSS 128	AK190	AK190
A106	VSS 2VSS 129	AK194	AK194
A108	VSS 2VSS 130	AK198	AK198
A110	VSS 2VSS 131	AK202	AK202
A112	VSS 2VSS 132	AK206	AK206
A114	VSS 2VSS 133	AK210	AK210
A116	VSS 2VSS 134	AK214	AK214
A118	VSS 2VSS 135	AK218	AK218
A120	VSS 2VSS 136	AK222	AK222
A122	VSS 2VSS 137	AK226	AK226
A124	VSS 2VSS 138	AK230	AK230
A126	VSS 2VSS 139	AK234	AK234
A128	VSS 2VSS 140	AK238	AK238
A130	VSS 2VSS 141	AK242	AK242
A132	VSS 2VSS 142	AK246	AK246
A134	VSS 2VSS 143	AK250	AK250
A136	VSS 2VSS 144	AK254	AK254
A138	VSS 2VSS 145	AK258	AK258
A140	VSS 2VSS 146	AK262	AK262
A142	VSS 2VSS 147	AK266	AK266
A144	VSS 2VSS 148	AK270	AK270
A146	VSS 2VSS 149	AK274	AK274
A148	VSS 2VSS 150	AK278	AK278
A150	VSS 2VSS 151	AK282	AK282
A152	VSS 2VSS 152	AK286	AK286
A154	VSS 2VSS 153	AK290	AK290
A156	VSS 2VSS 154	AK294	AK294
A158	VSS 2VSS 155	AK298	AK298
A160	VSS 2VSS 156	AK302	AK302
A162	VSS 2VSS 157	AK306	AK306
A164	VSS 2VSS 158	AK310	AK310
A166	VSS 2VSS 159	AK314	AK314
A168	VSS 2VSS 160	AK318	AK318
A170	VSS 2VSS 161	AK322	AK322
A172	VSS 2VSS 162	AK326	AK326

COMETLAKE-H-CPU_BGA1440

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UIG		BJ15	
AW5	VSS 16VSS 244	BJ15	BJ15
AW6	VSS 16VSS 245	BJ16	BJ16
AW7	VSS 16VSS 246	BJ17	BJ17
AW8	VSS 16VSS 247	BJ18	BJ18
AW9	VSS 16VSS 248	BJ19	BJ19
AW10	VSS 16VSS 249	BJ20	BJ20
AW11	VSS 16VSS 250	BJ21	BJ21
AW12	VSS 17VSS 251	BJ22	BJ22
AW13	VSS 17VSS 252	BJ23	BJ23
AW14	VSS 17VSS 253	BJ24	BJ24
AW15	VSS 17VSS 254	BJ25	BJ25
AW16	VSS 17VSS 255	BJ26	BJ26
AW17	VSS 17VSS 256	BJ27	BJ27
AW18	VSS 17VSS 257	BJ28	BJ28
AW19	VSS 17VSS 258	BJ29	BJ29
AW20	VSS 17VSS 259	BJ30	BJ30
AW21	VSS 17VSS 260	BJ31	BJ31
AW22	VSS 18VSS 261	BJ32	BJ32
AW23	VSS 18VSS 262	BJ33	BJ33
AW24	VSS 18VSS 263	BJ34	BJ34
AW25	VSS 18VSS 264	BJ35	BJ35
AW26	VSS 18VSS 265	BJ36	BJ36
AW27	VSS 18VSS 266	BJ37	BJ37
AW28	VSS 18VSS 267	BJ38	BJ38
AW29	VSS 18VSS 268	BJ39	BJ39
AW30	VSS 18VSS 269	BJ40	BJ40
AW31	VSS 18VSS 270	BJ41	BJ41
AW32	VSS 19VSS 271	BJ42	BJ42
AW33	VSS 19VSS 272	BJ43	BJ43
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AW35	VSS 19VSS 274	BJ45	BJ45
AW36	VSS 19VSS 275	BJ46	BJ46
AW37	VSS 19VSS 276	BJ47	BJ47
AW38	VSS 19VSS 277	BJ48	BJ48
AW39	VSS 19VSS 278	BJ49	BJ49
AW40	VSS 19VSS 279	BJ50	BJ50
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AW46	VSS 20VSS 285	BJ56	BJ56
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AW48	VSS 20VSS 287	BJ58	BJ58
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AW57	VSS 21VSS 296	BJ67	BJ67
AW58	VSS 21VSS 297	BJ68	BJ68
AW59	VSS 21VSS 298	BJ69	BJ69
AW60	VSS 21VSS 299	BJ70	BJ70
AW61	VSS 21VSS 300	BJ71	BJ71
AW62	VSS 22VSS 301	BJ72	BJ72
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AW68	VSS 22VSS 307	BJ78	BJ78
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AW72	VSS 23VSS 311	BJ82	BJ82
AW73	VSS 23VSS 312	BJ83	BJ83
AW74	VSS 23VSS 313	BJ84	BJ84
AW75	VSS 23VSS 314	BJ85	BJ85
AW76	VSS 23VSS 315	BJ86	BJ86
AW77	VSS 23VSS 316	BJ87	BJ87
AW78	VSS 23VSS 317	BJ88	BJ88
AW79	VSS 23VSS 318	BJ89	BJ89
AW80	VSS 23VSS 319	BJ90	BJ90
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AW82	VSS 24VSS 321	BJ92	BJ92
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AW85	VSS 24VSS 324	BJ95	BJ95

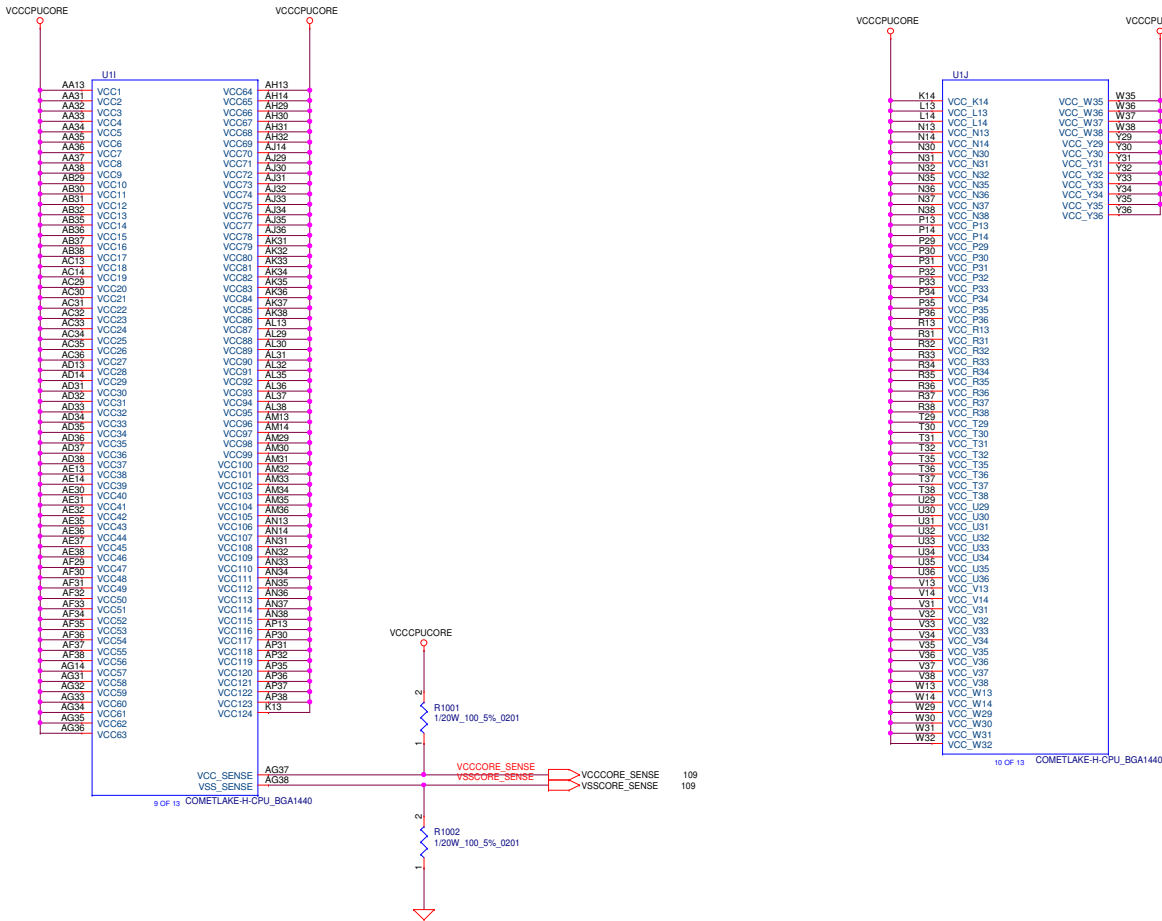
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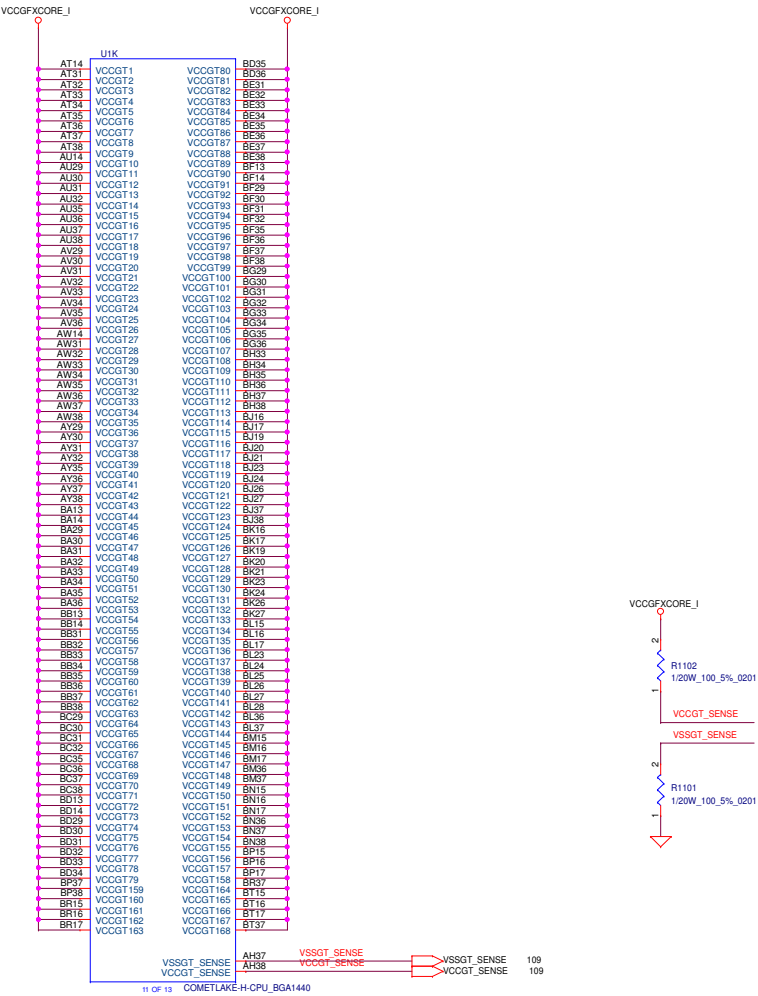
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UIH		F15	
BN4	VSS 325	VSS 409	F15
BN5	VSS 326	VSS 410	F16
BN6	VSS 327	VSS 411	F17
BN7	VSS 328	VSS 412	F18
BN8	VSS 329	VSS 413	F19
BN9	VSS 330	VSS 414	F20
BN10	VSS 331	VSS 415	F21
BN11	VSS 332	VSS 416	F22
BN12	VSS 333	VSS 417	F23
BN13	VSS 334	VSS 418	F24
BN14	VSS 335	VSS 419	F25
BN15	VSS 336	VSS 420	F26
BN16	VSS 337	VSS 421	F27
BN17	VSS 338	VSS 422	F28
BN18	VSS 339	VSS 423	F29
BN19	VSS 340	VSS 424	F30
BN20	VSS 341	VSS 425	F31
BN21	VSS 342	VSS 426	F32
BN22	VSS 343	VSS 427	F33
BN23	VSS 344	VSS 428	F34
BN24	VSS 345	VSS 429	F35
BN25	VSS 346	VSS 430	F36
BN26	VSS 347	VSS 431	F37
BN27	VSS 348	VSS 432	F38
BN28	VSS 349	VSS 433	F39
BN29	VSS 350	VSS 434	F40
BN30	VSS 351	VSS 435	F41
BN31	VSS 352	VSS 436	F42
BN32	VSS 353	VSS 437	F43
BN33	VSS 354	VSS 438	F44
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BN77	VSS 398	VSS 482	F88
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BN81	VSS 402	VSS 486	F92
BN82	VSS 403	VSS 487	F93
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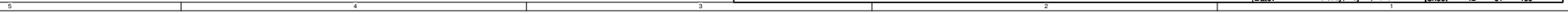
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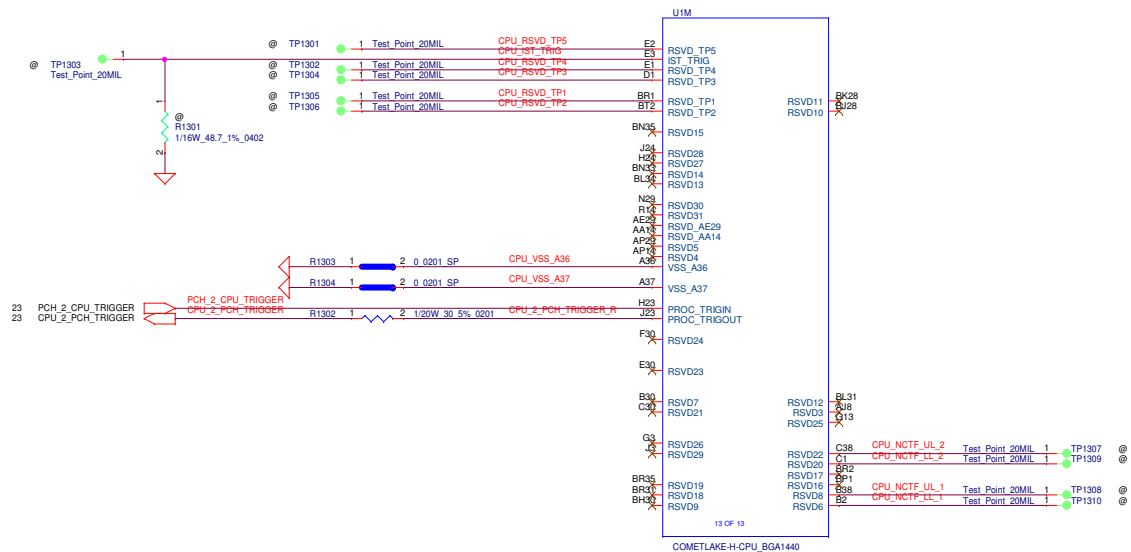




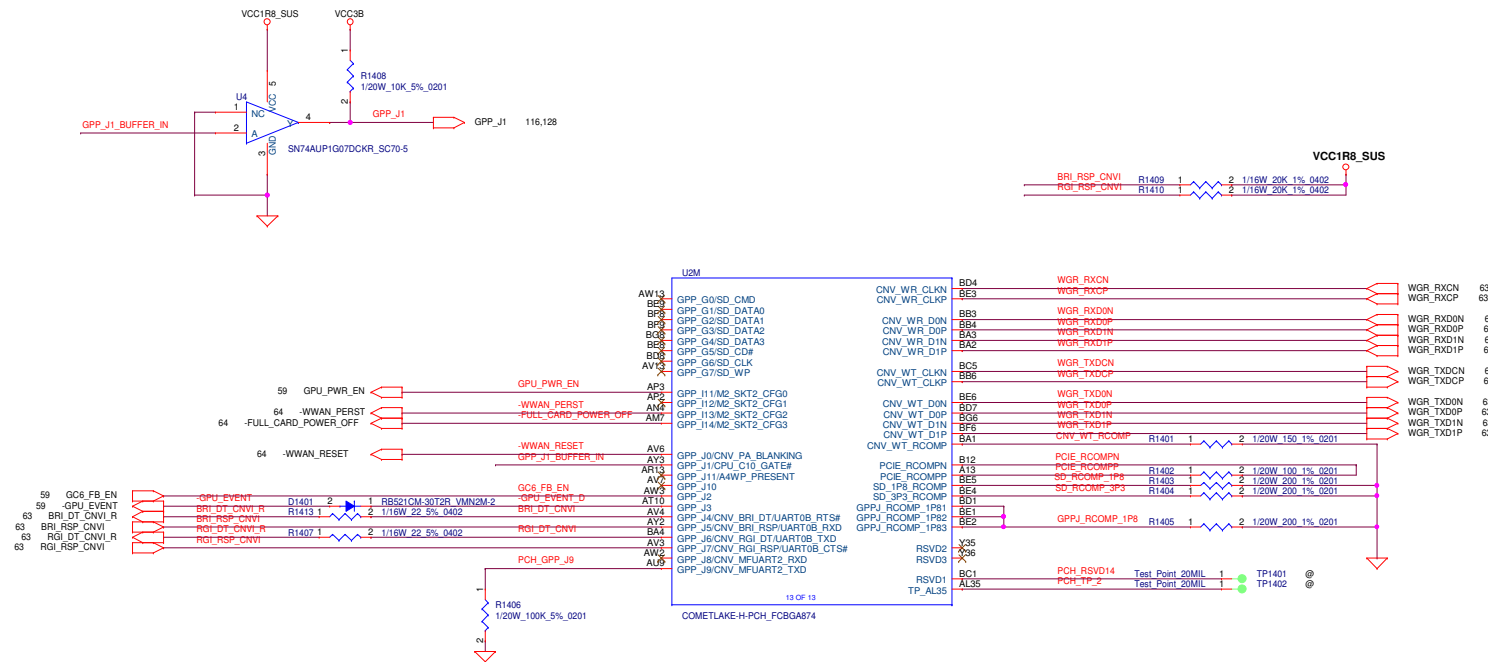
11 OF 13 COMETLAKE-H-CPU_BGA1440





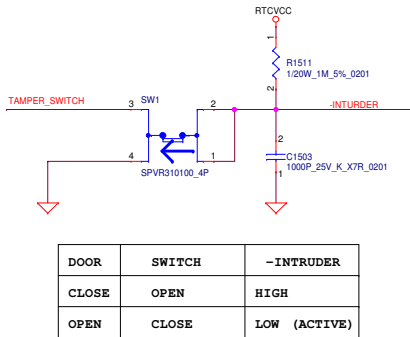
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PCH



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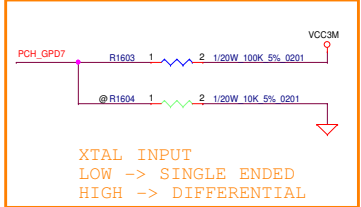
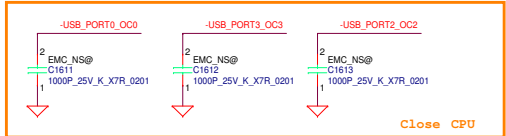
DOOR	SWITCH	-INTRUDER
CLOSE	OPEN	HIGH
OPEN	CLOSE	LOW (ACTIVE)

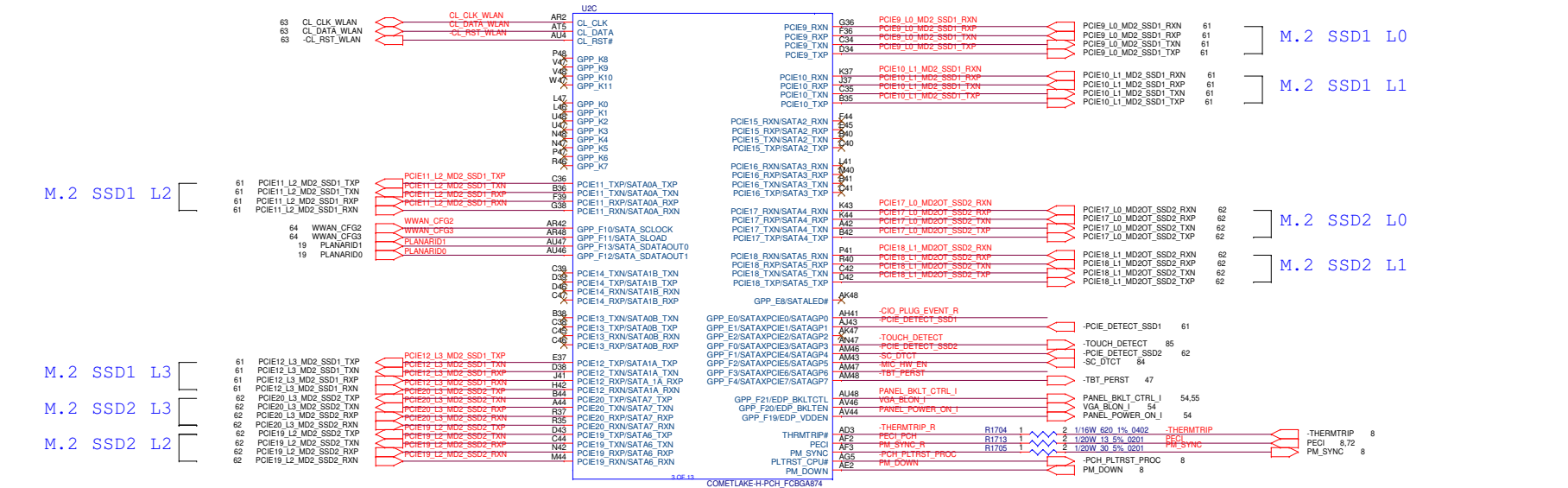
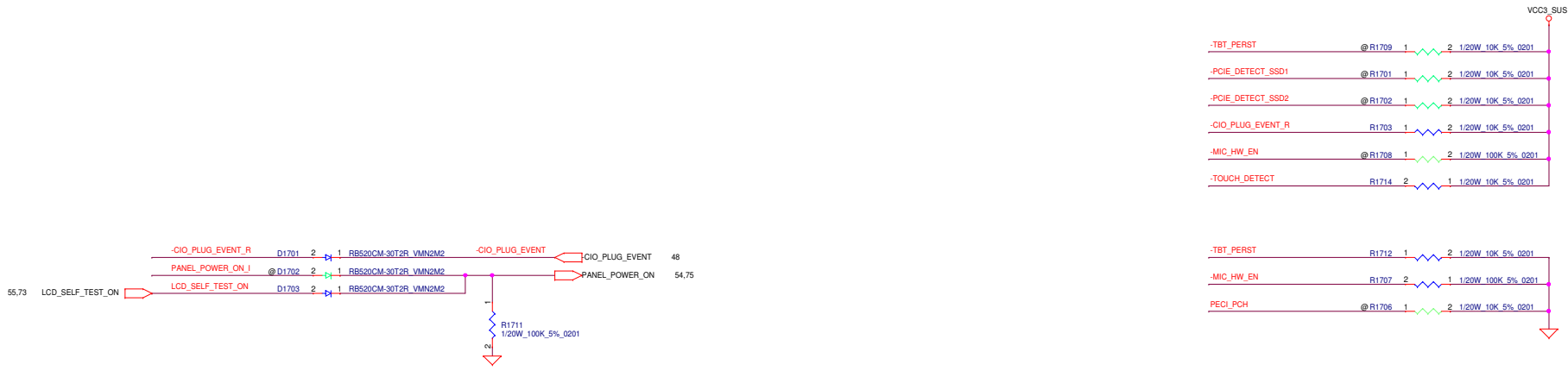
PROJECT_DET	
Pull-Up	P15
Pull-Down	P17

GPP_H12/SML2ALERT# eSPI Flash Sharing Mode	
HIGH	Slave Attached Flash Sharing (SAFS) enabled
LOW	Master Attached Flash Sharing (MAFS) enabled (Default)

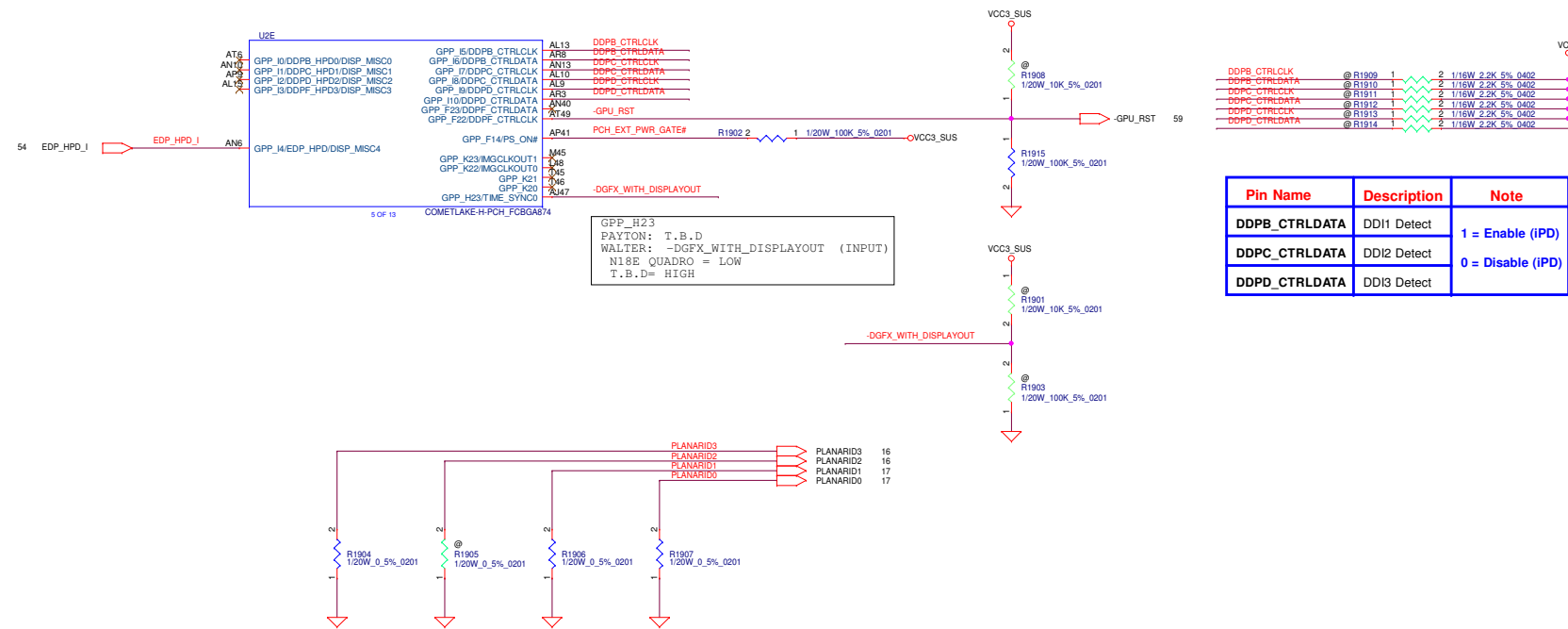
Thunderbolt x 4

GbE
WLAN Card
WWAN Card
Media Card





HDA_SDO is used to update the Descriptor and/or the ME regions of the SPI after MFG Done bit is set.



Pin Name	Description	Note
DDPB_CTRLDATA	DDI1 Detect	1 = Enable (iPD)
DDPC_CTRLDATA	DDI2 Detect	0 = Disable (iPD)
DDPD_CTRLDATA	DDI3 Detect	

TABLE

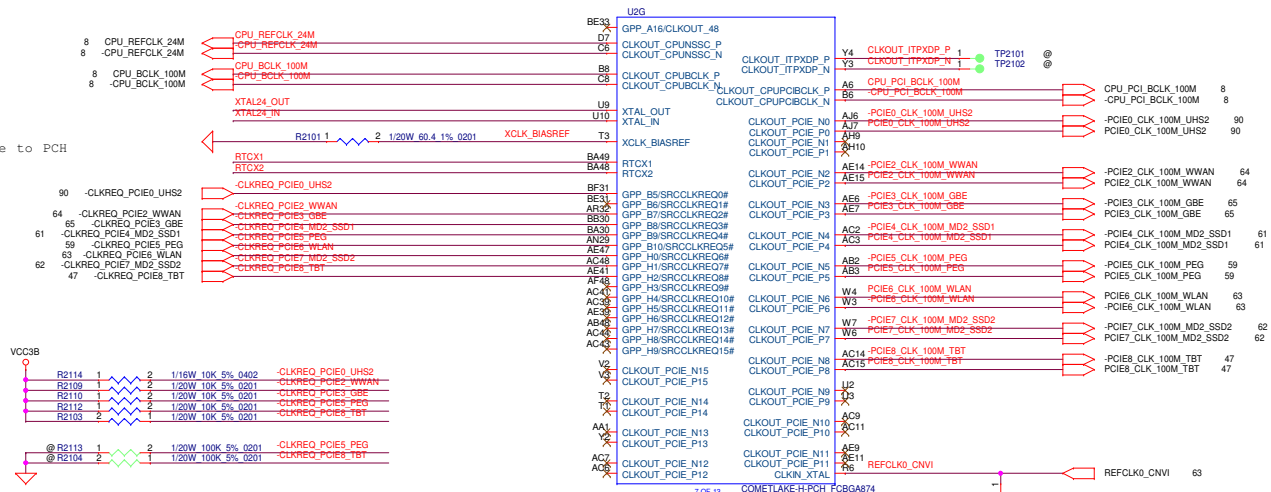
	PLANAR ID			
	3	2	1	0
	R1904	R1905	R1906	R1907
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

TABLE

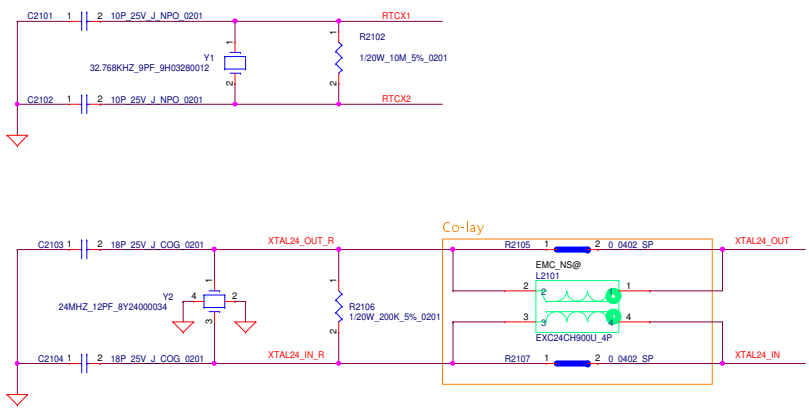
LEVEL	PLANARID[3..0]	CPU	PCH
PDV	-----	-----	-----
EVT	0001b	ES	ES
FVT	0010b	ES	ES
SIT	0011b	QS	QS
SVT	0100b	MP	MP

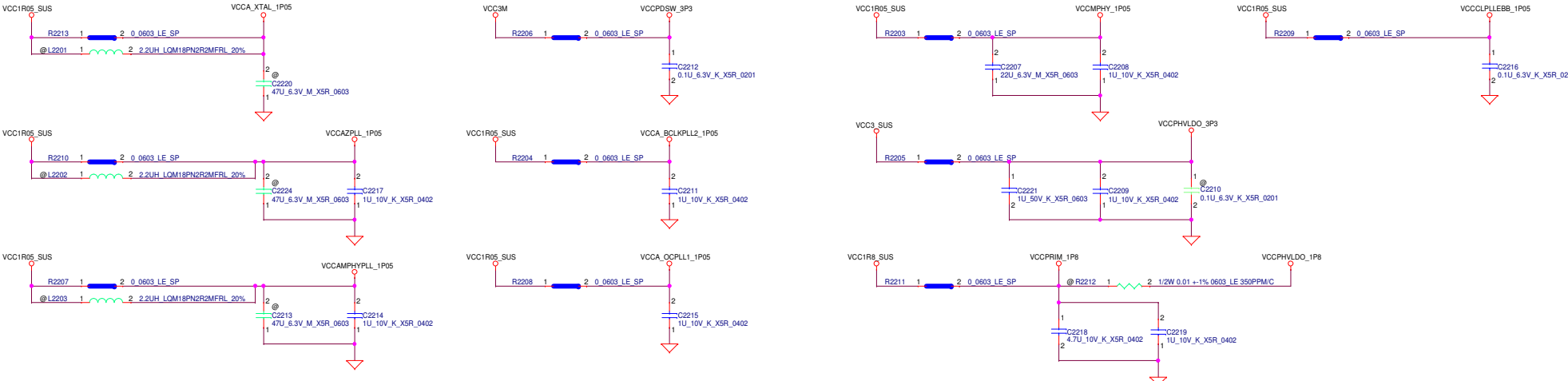
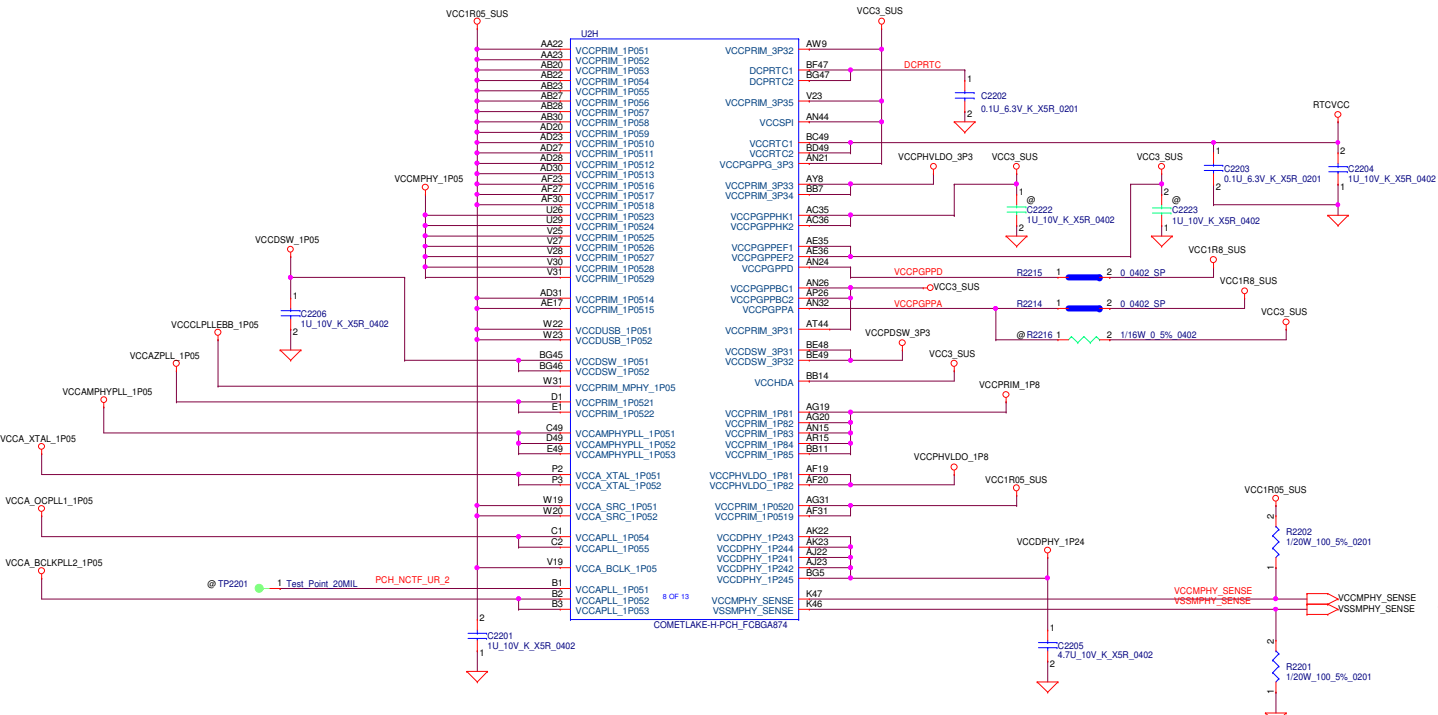




XCLK_BIASREF RES: Close to PCH
Refer GUIDELINE

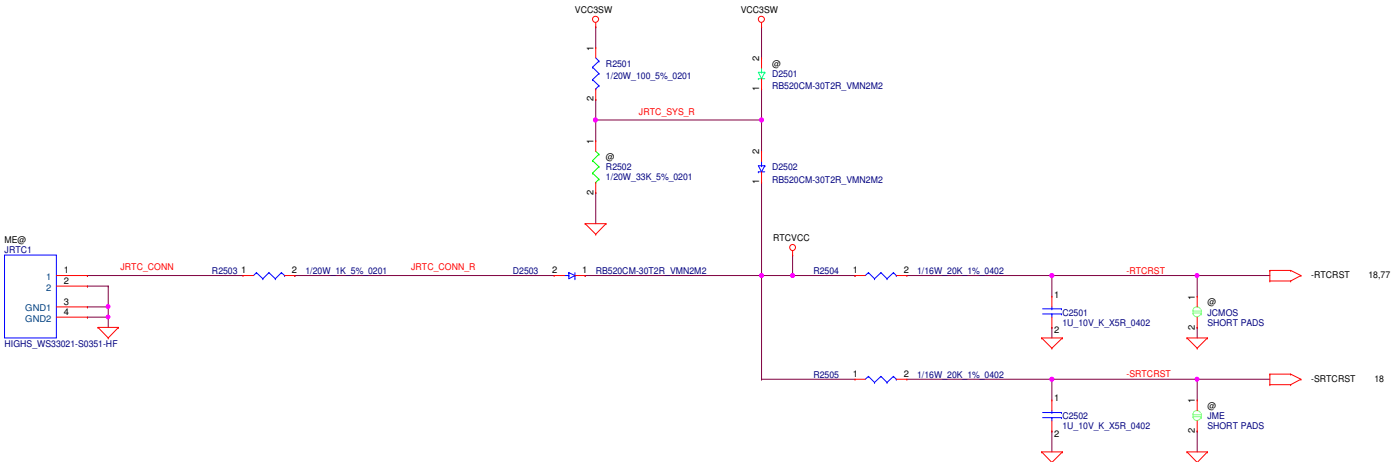


External Pull on CLKREQ# should be placed in device page,
as power rails may be different from PCH-H..



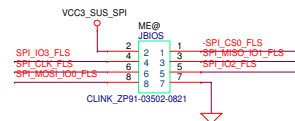


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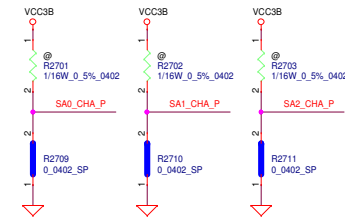
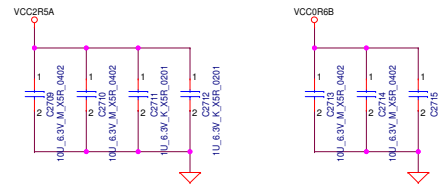
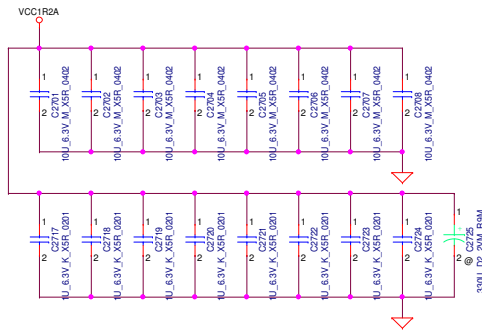
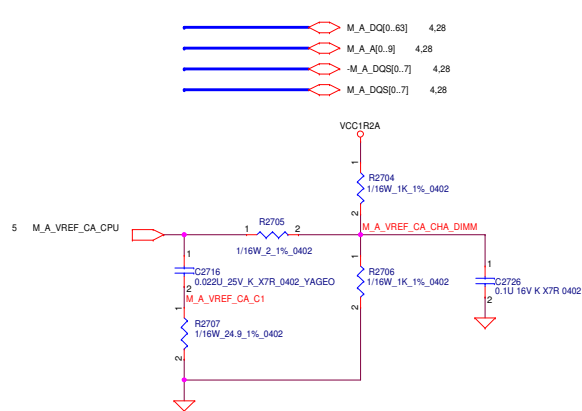




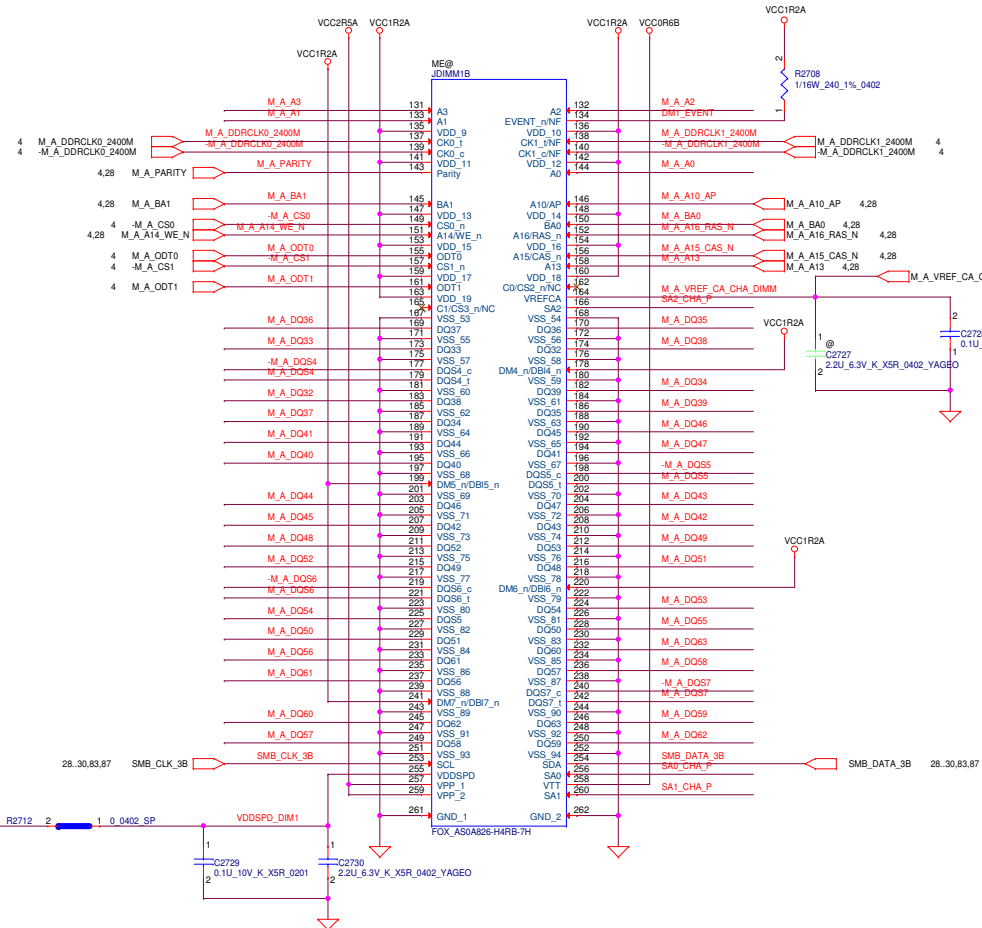
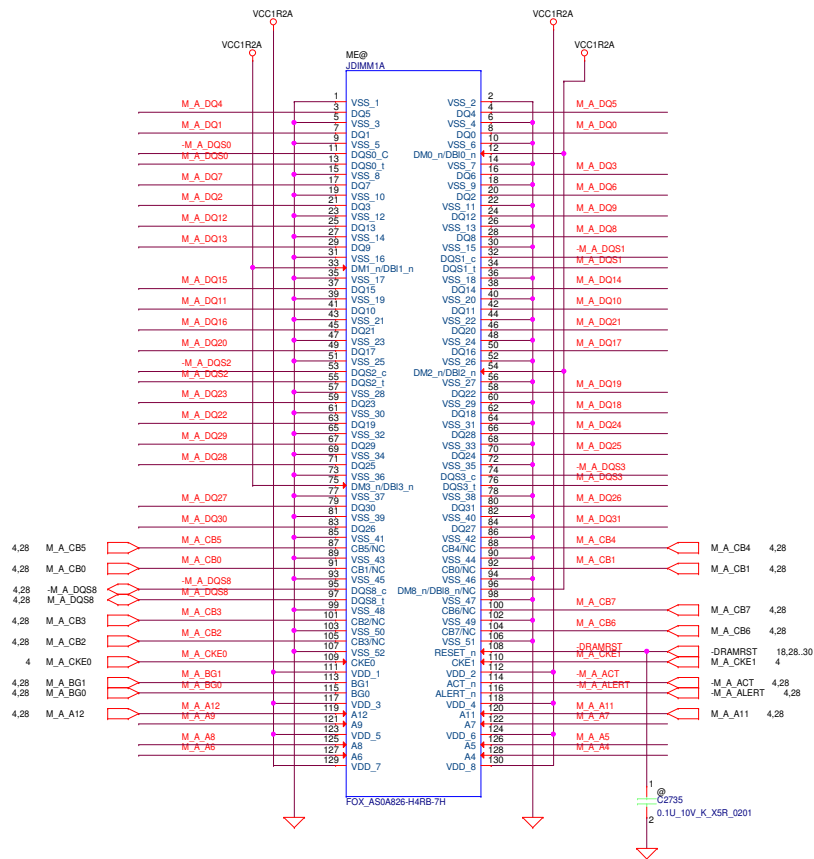
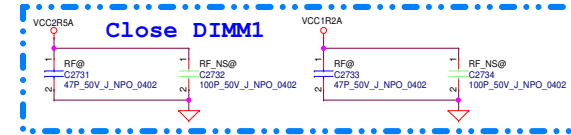
2017/10/27



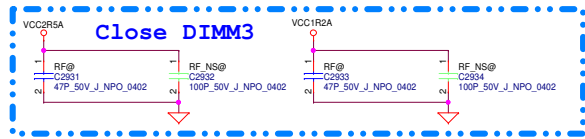
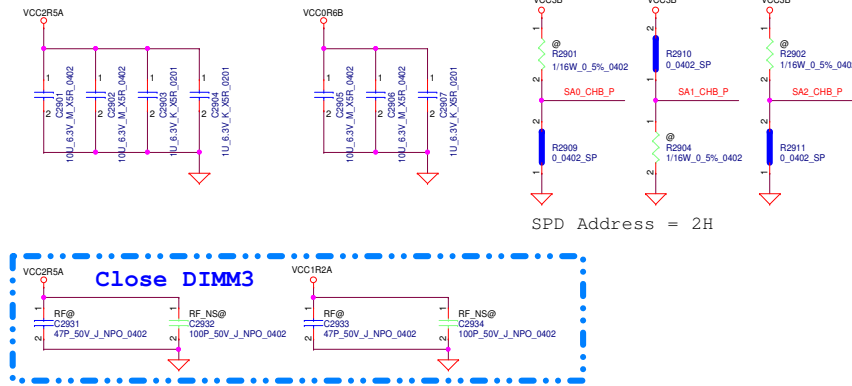
5	4	3	2	1
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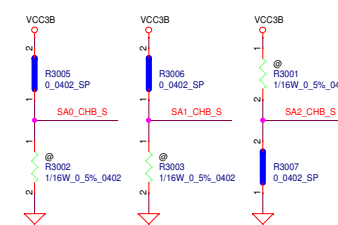
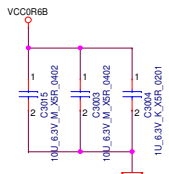
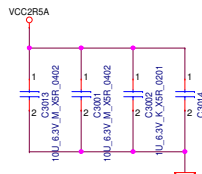
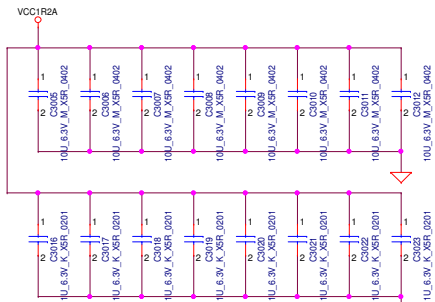
SPD Address = 0H



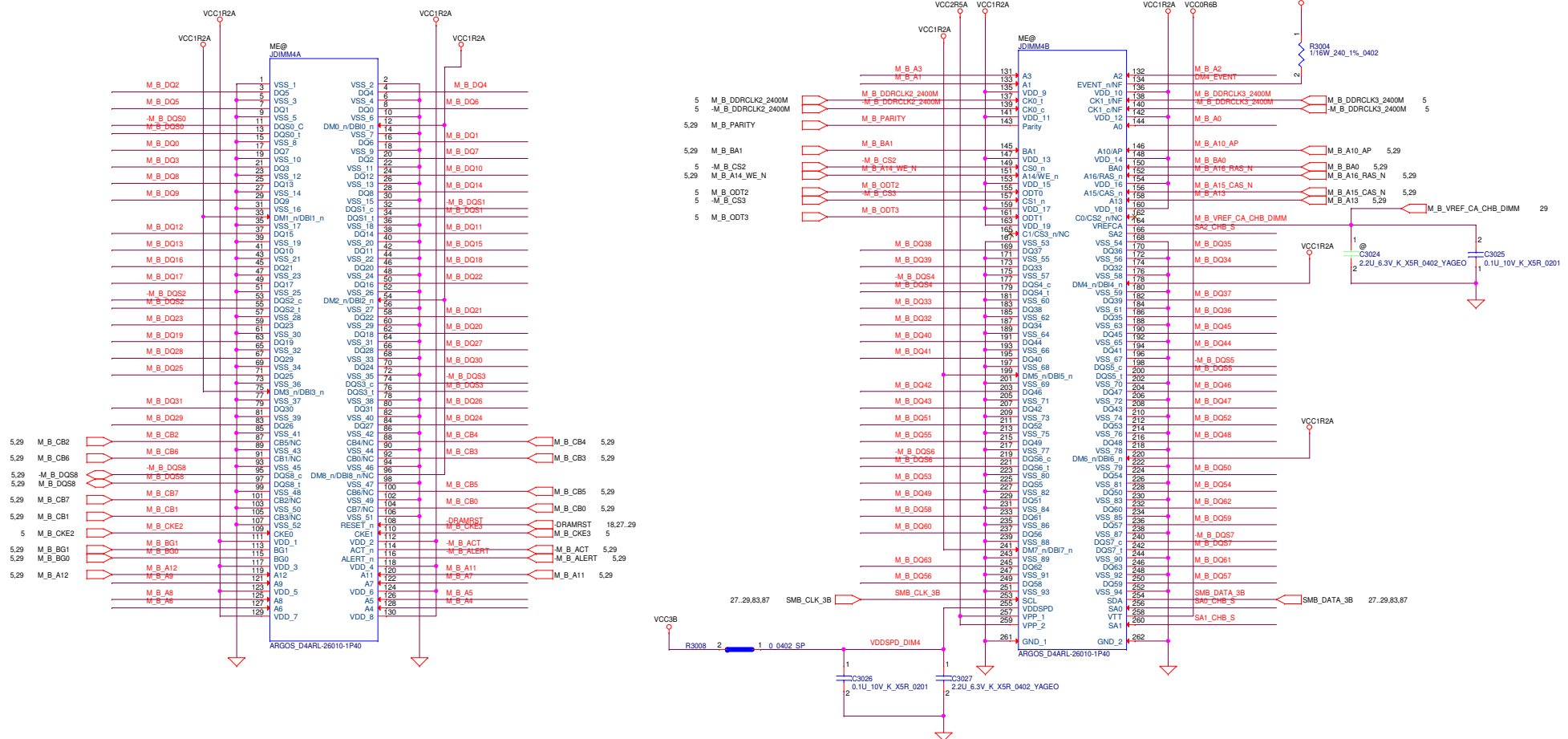






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The image shows two identical schematic diagrams side-by-side. The left diagram is labeled 'Close DIMM4' and the right is labeled 'VCC1R2A'. Both diagrams show a differential signal path. On the left, there is a VCC2R5A supply. On the right, there is a VCC1R2A supply. The signal path consists of two parallel lines. The top line has an RF component (C3028 for DIMM4, C3030 for VCC1R2A) connected to the supply. The bottom line has an RF component (C3029 for DIMM4, C3031 for VCC1R2A) connected to the supply. Both lines then connect to NPO_0402 capacitors. The signal is then connected to NS components (C3029 for DIMM4, C3031 for VCC1R2A) which are connected to 100P_50V_J_NPO_0402 capacitors. The signal is then connected to NS components (C3030 for DIMM4, C3031 for VCC1R2A) which are connected to 100P_50V_J_NPO_0402 capacitors. The signal is then connected to NS components (C3031 for DIMM4, C3031 for VCC1R2A) which are connected to 100P_50V_J_NPO_0402 capacitors.




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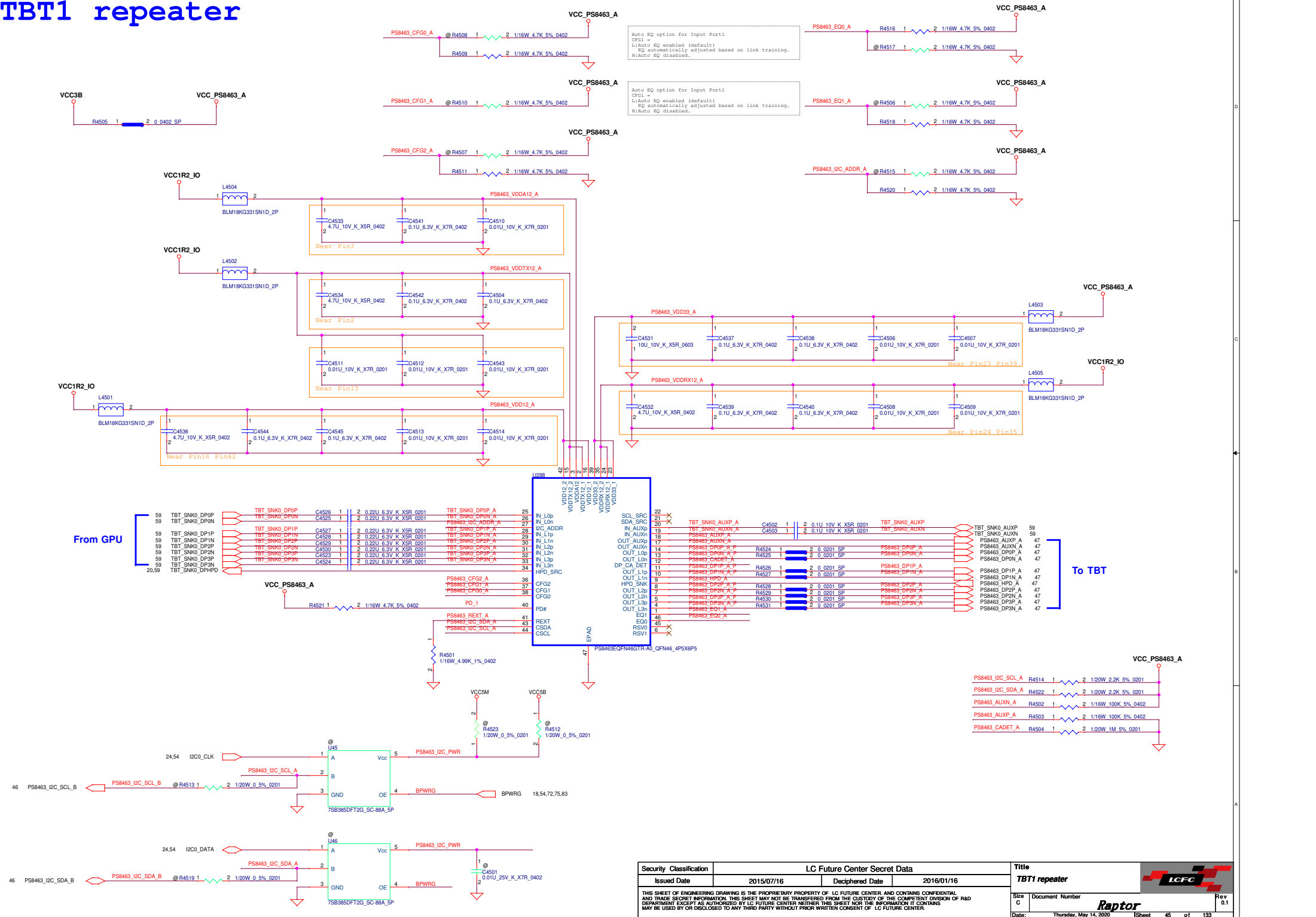
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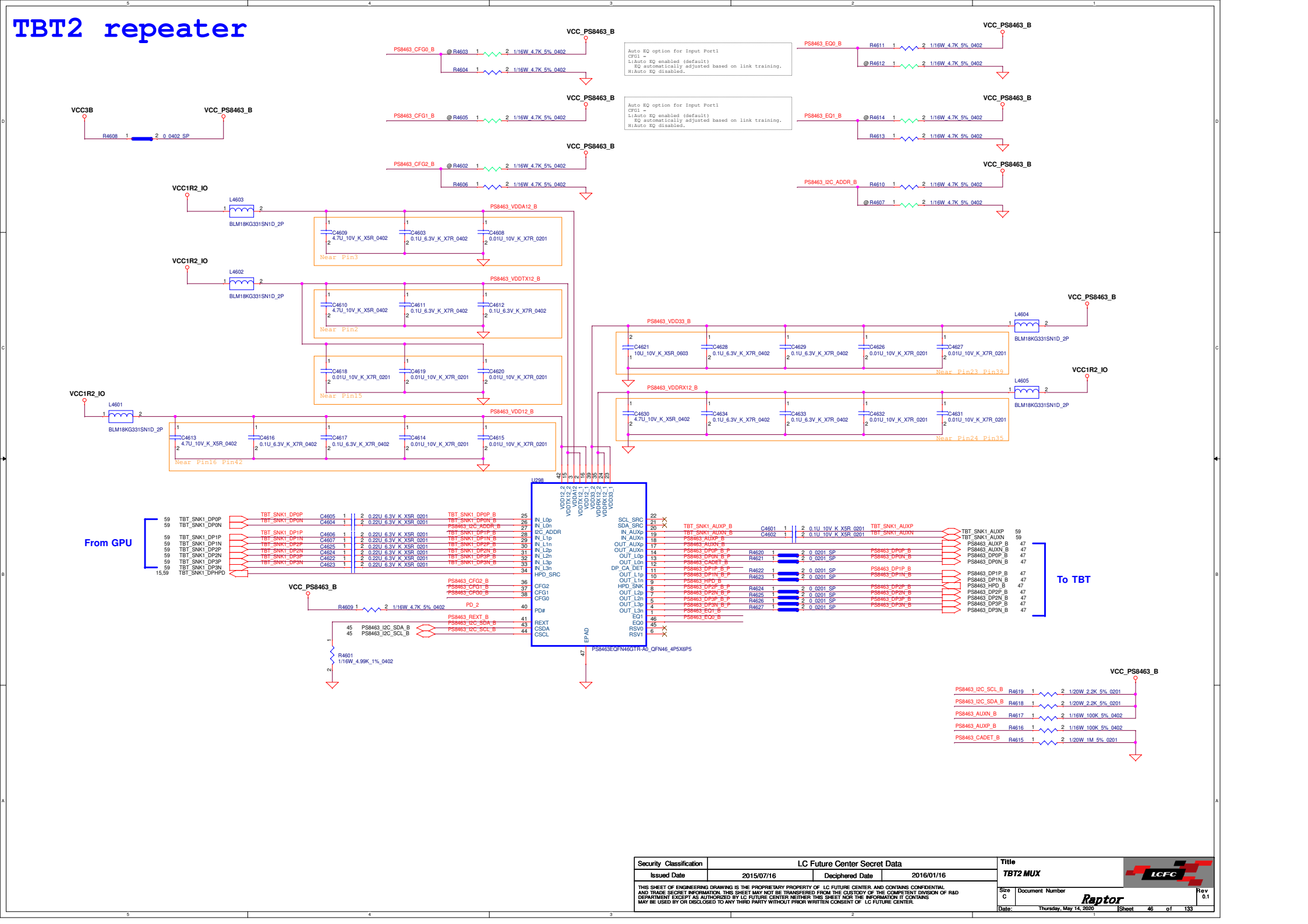
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TBT1 repeater



[illegible]

TBT2 repeater

Legend:

- Auto EQ option for Input Port1
- CP01 =
- Auto EQ enabled (default)
- EQ automatically adjusted based on link training.
- Auto EQ disabled.

From GPU

To TBT

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Title: TBT2 MUX

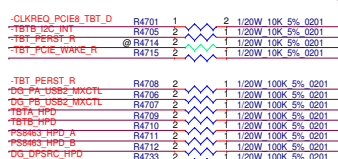
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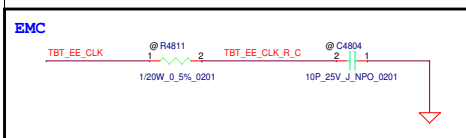
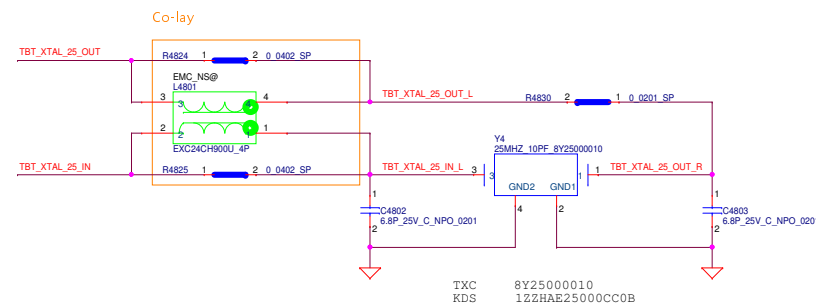
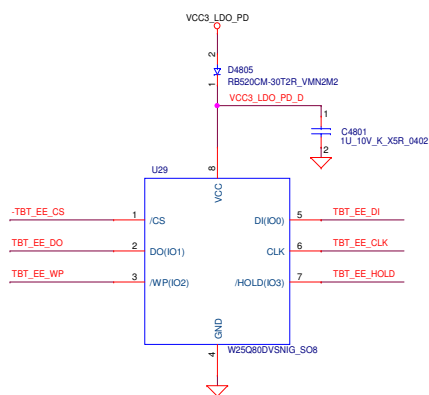
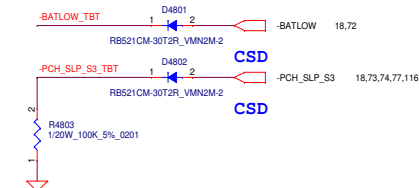
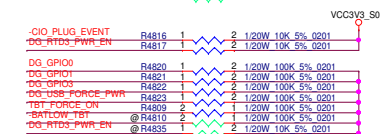
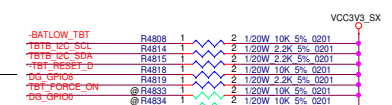
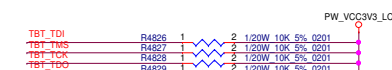
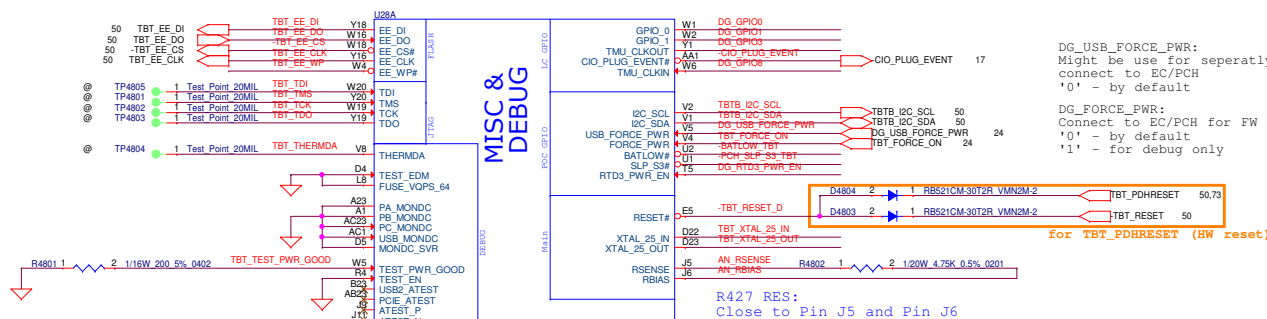
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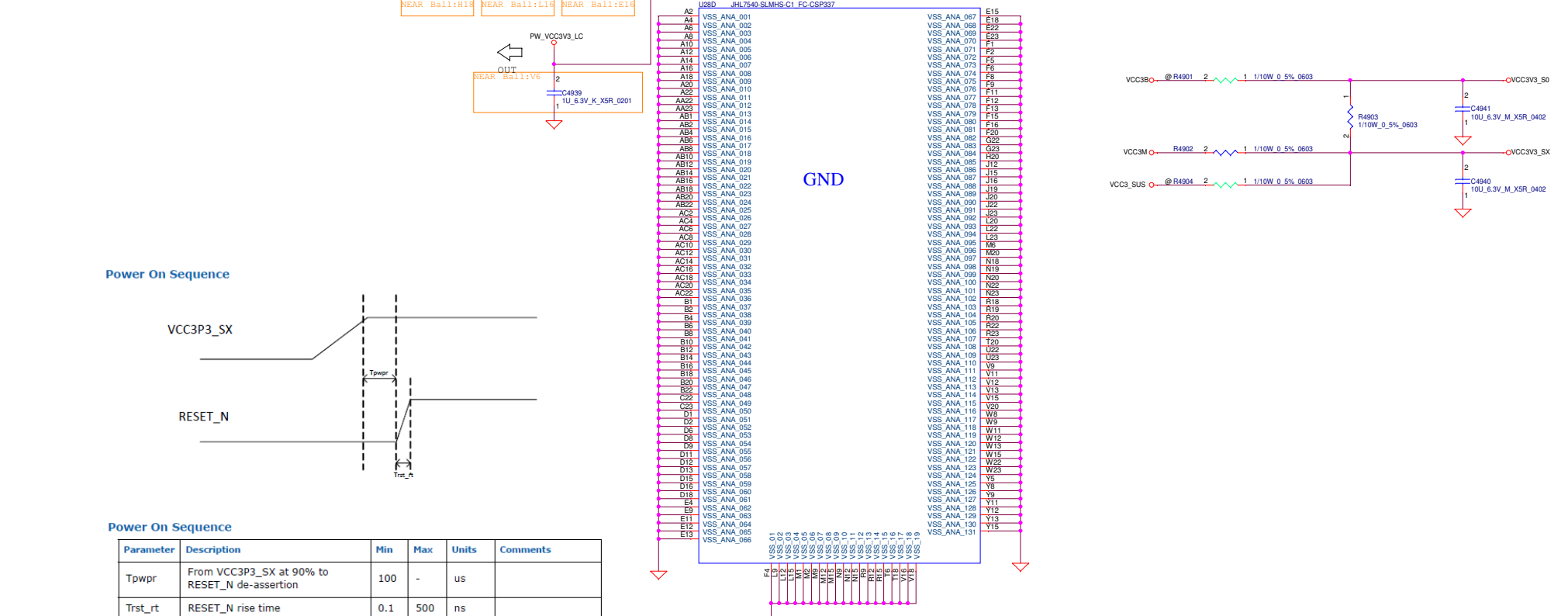
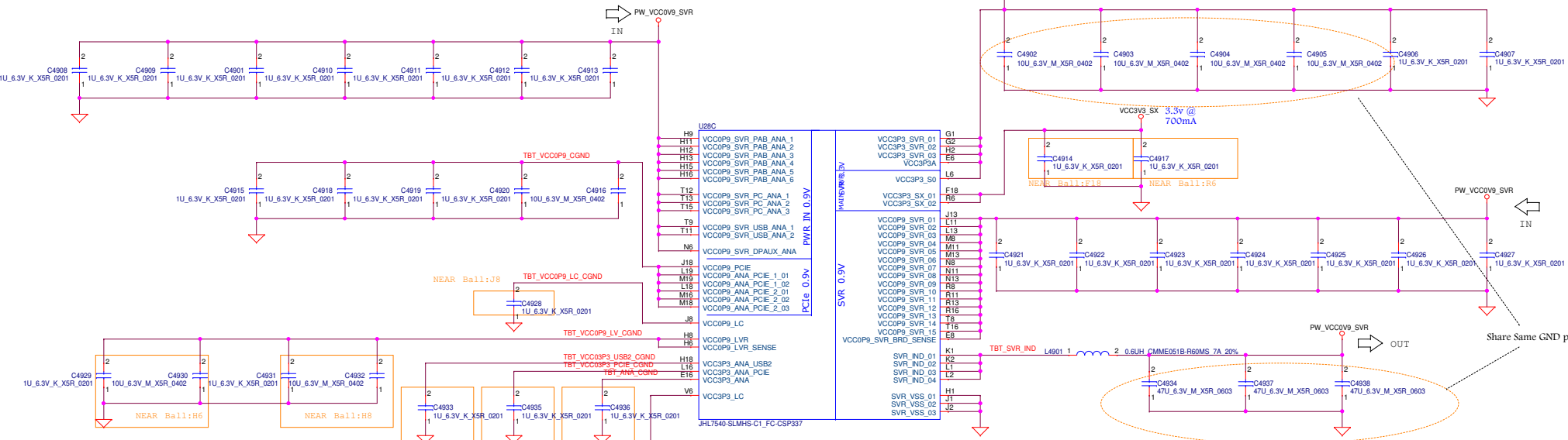
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TUNDEBOLT

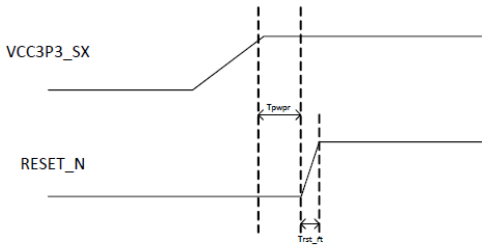


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TUNDEBOLT



Power On Sequence



Power On Sequence

Parameter	Description	Min	Max	Units	Comments
Tpwr	From VCC3P3_SX at 90% to RESET_N de-assertion	100	-	us	
Trst_rt	RESET_N rise time	0.1	500	ns	

POWER DELIVERY

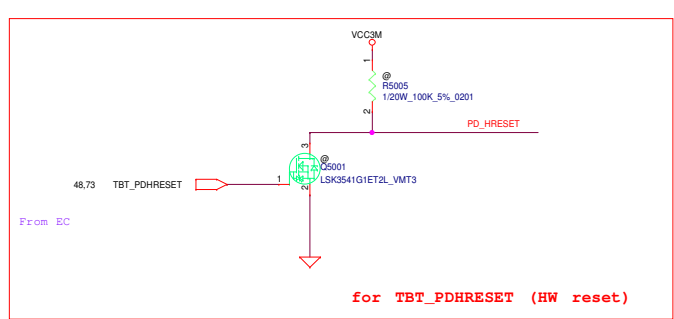
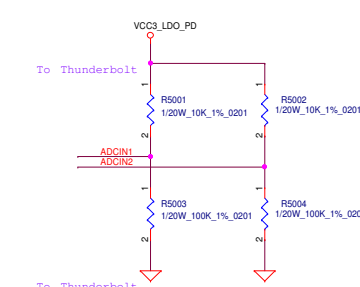
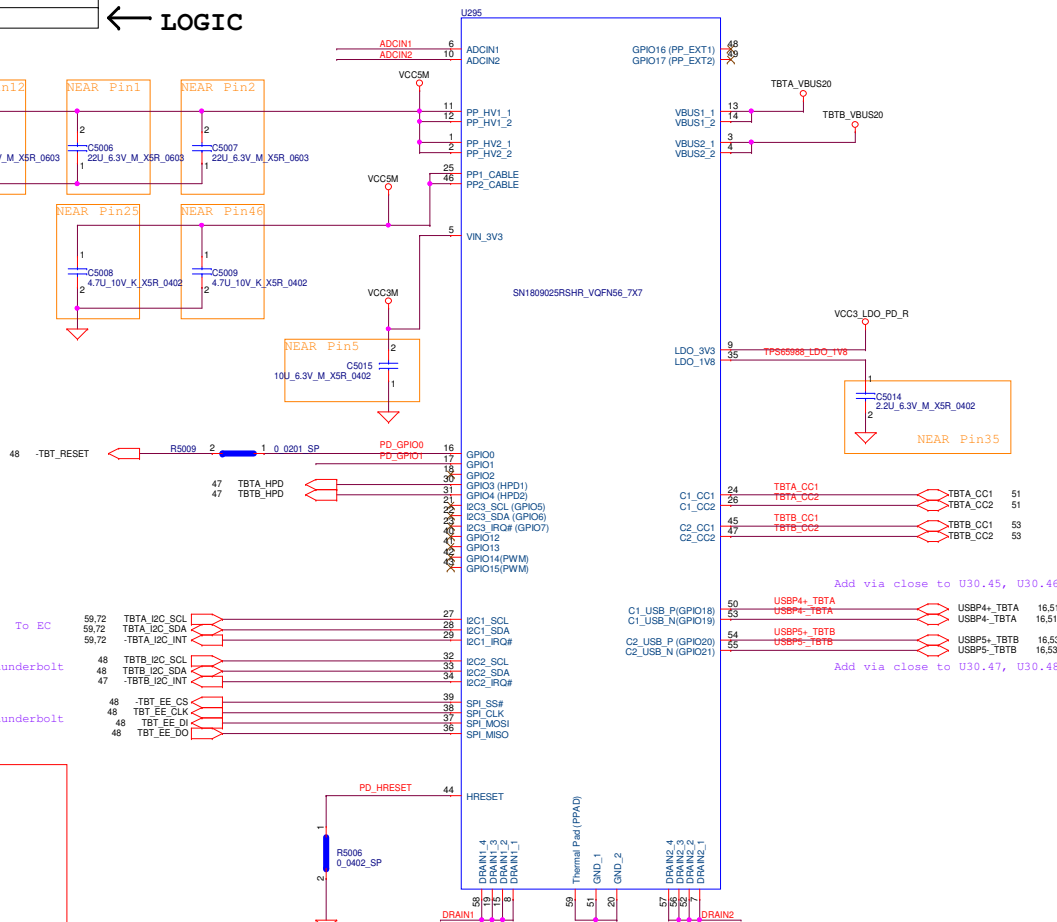
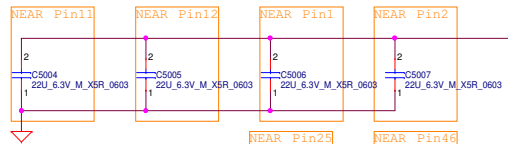
ADCIN1 BUSPOWER CONFIGURATION		
DIV = R5003/(R5001+R5003)		CONFIGURATION
DIV MIN	DIV MAX	
0.00	0.18	BP_NoResponse
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

← LOGIC


ADCIN2 I2C Address Setting			
DIV = R5004/(R5002+R5004)		I2C Unique Address [3:1]	
DIV MIN	DIV MAX	ADC_ADDR_DECODE_C1	ADC_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

← LOGIC

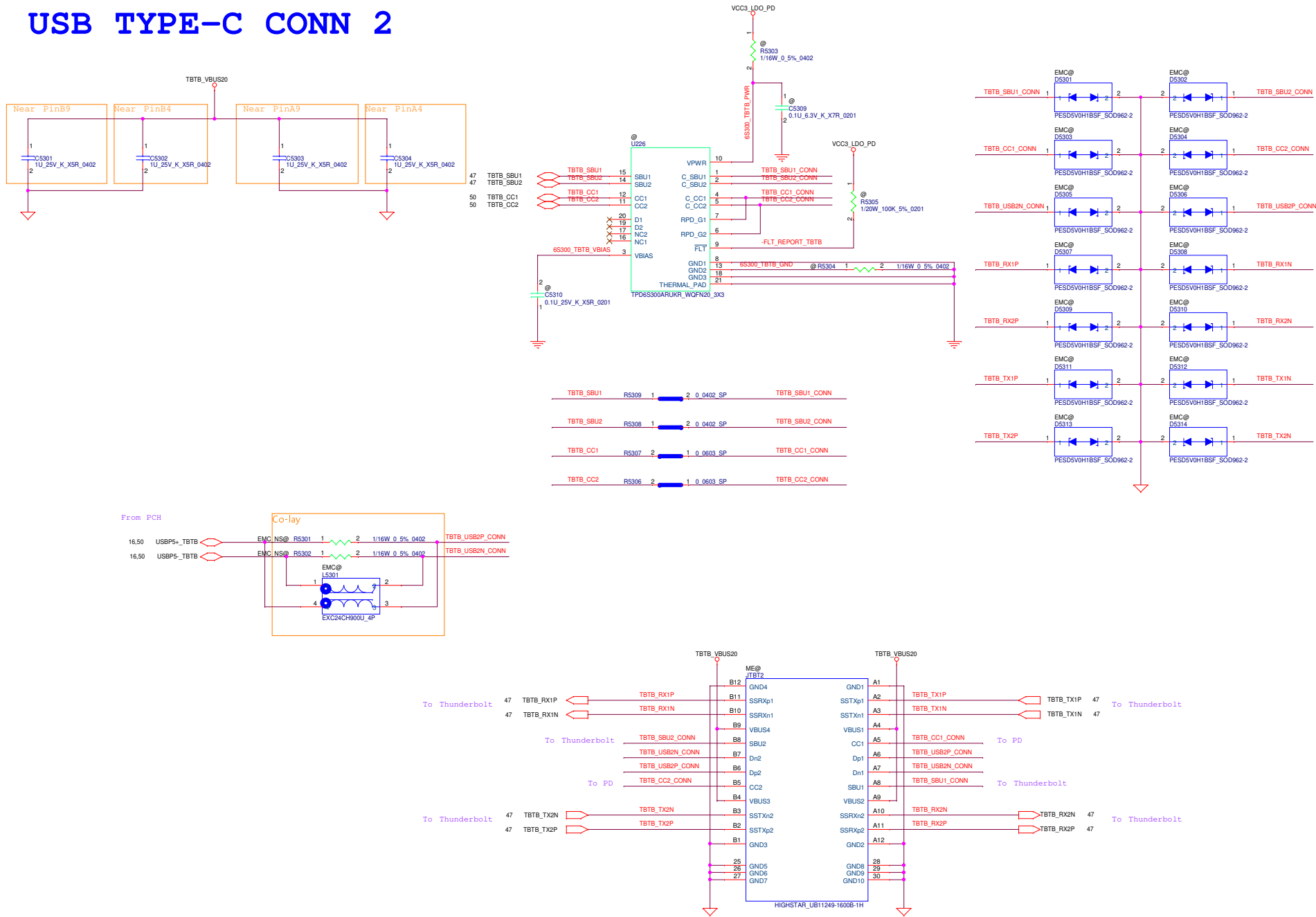
I2C Address		
I2C1 (to EC)	TBT PORT	0X23
	USBC PORT	0X27
I2C2 (to TR)	TBT PORT	0X38
	USBC PORT	0X3F



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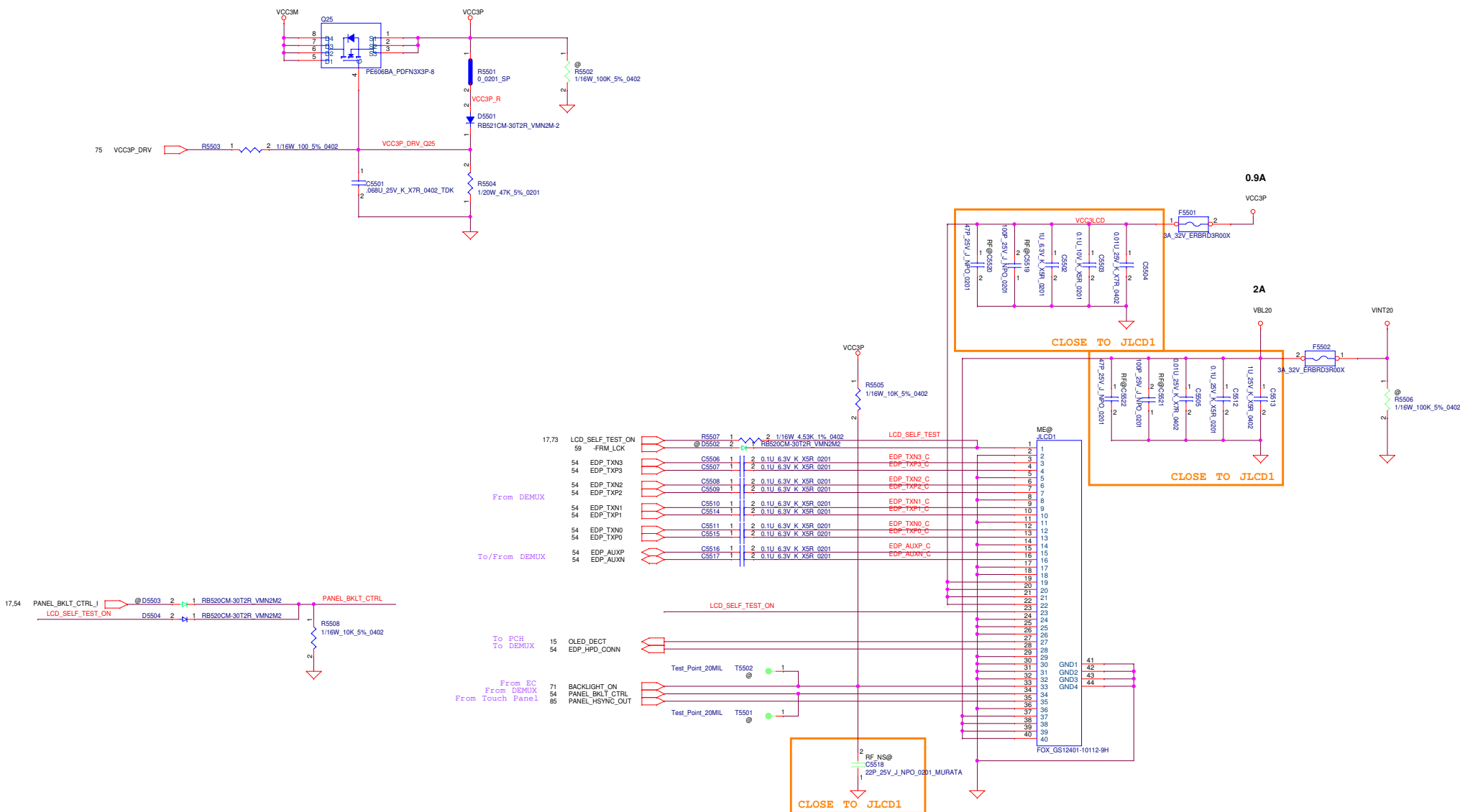
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USB TYPE-C CONN 2





[illegible][illegible]

LCD CONN



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HDMI Re-Timer

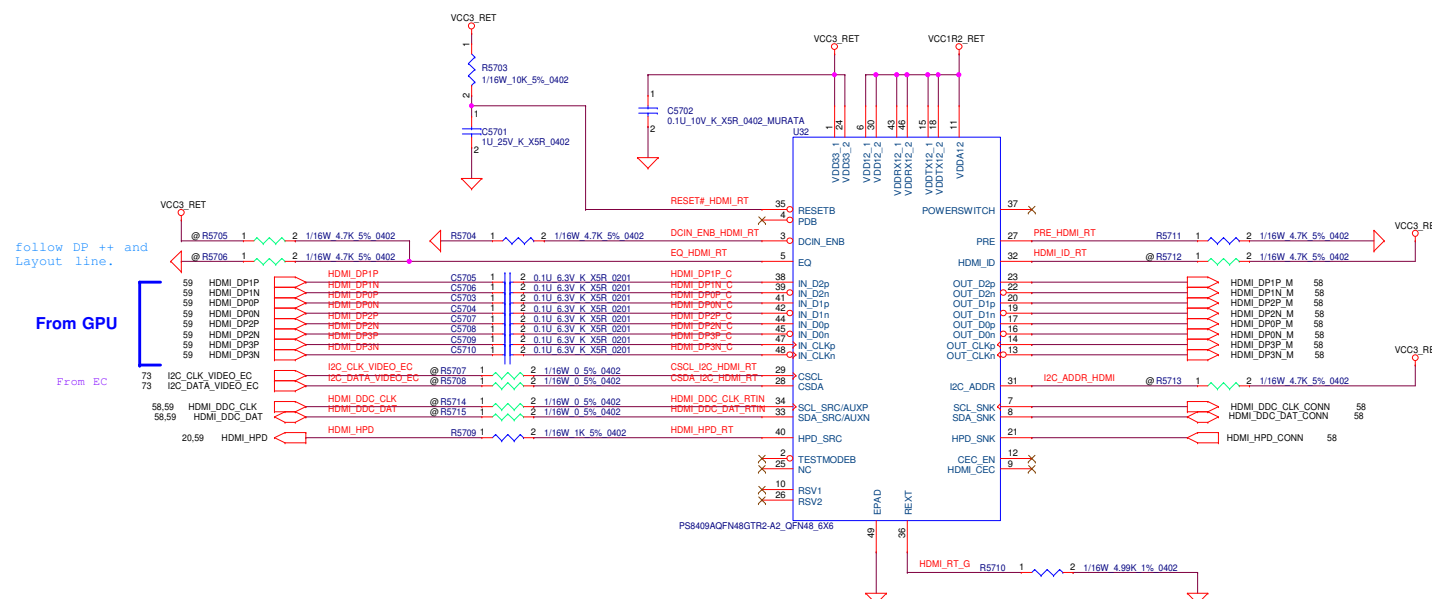
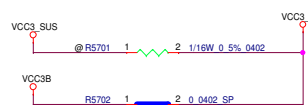
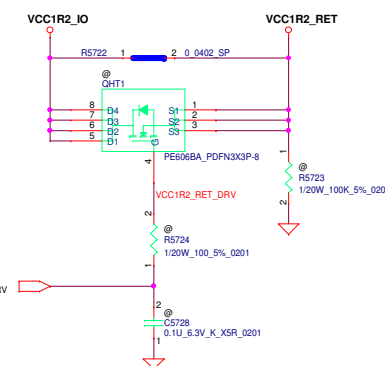
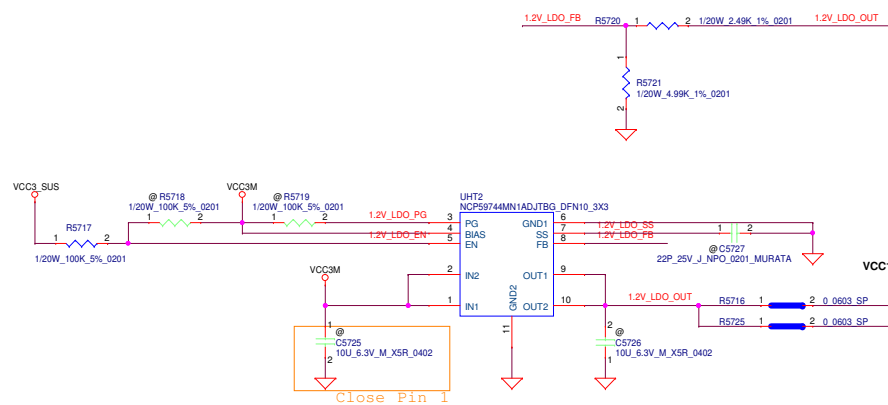
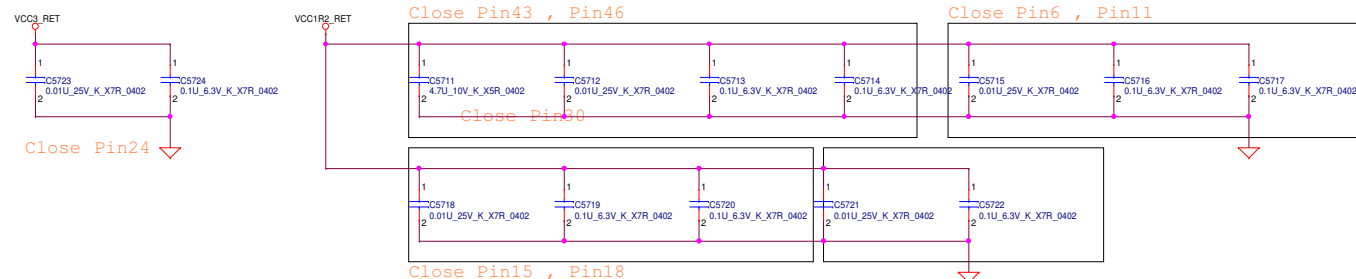


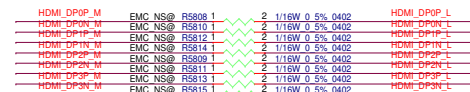
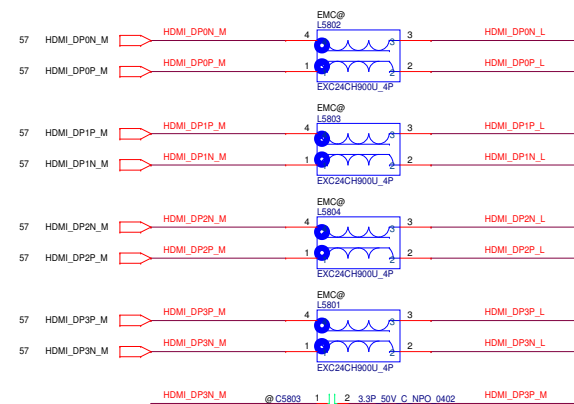
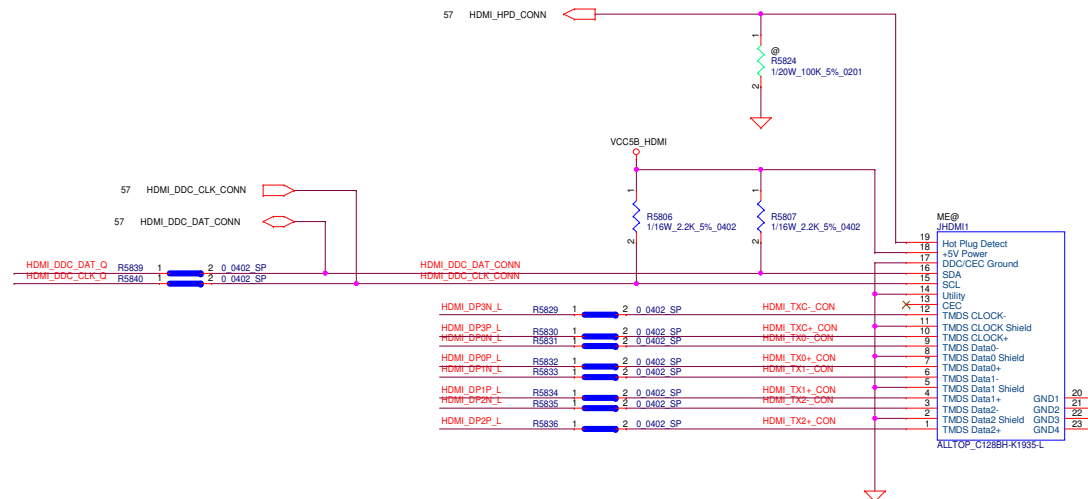
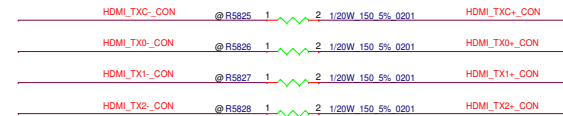


Table 9.12 Display Connector with DVI/HDMI Dongle Support

DP Connector Pin	DisplayPort Signal	DVI/HDMI Signal
1	Main Link Lane 0 +	TX Data 2 +
2	GND	GND
3	Main Link Lane 0 -	TX Data 2 -
4	Main Link Lane 1 +	TX Data 1 +
5	GND	GND
6	Main Link Lane 1 -	TX Data 1 -
7	Main Link Lane 2 +	TX Data 0 +
8	GND	GND
9	Main Link Lane 2 -	TX Data 0 -
10	Main Link Lane 3 +	Clock +
11	GND	GND
12	Main Link Lane 3 -	Clock -
13	CONFIG1 (Connected to GND)	DP MODE
14	CONFIG1 (Connected to GND)	CEC
15	AUX CH +	SCL (DDC Clock)
16	GND	GND
17	AUX CH -	SDA (DDC Data)
18	Hot Plug Detect	Hot Plug Detect
19	GND Return	GND Return
20	PWR (3.3V)	PWR (3.3V)

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[illegible][illegible]

dGPU board CONNECTOR

ME@ J081A

ME@ J081B

FOXCONN_AS38826-S55B1-7H

AGND_EC

VCC3M

VCC3M

VCC1R8_SUS

VCC1R8_SUS

VCC1R8_MAIN

VCC1R8_MAIN

PROJECT_ID2

PROJECT_ID0

PROJECT_ID1

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LCFC

Raptor

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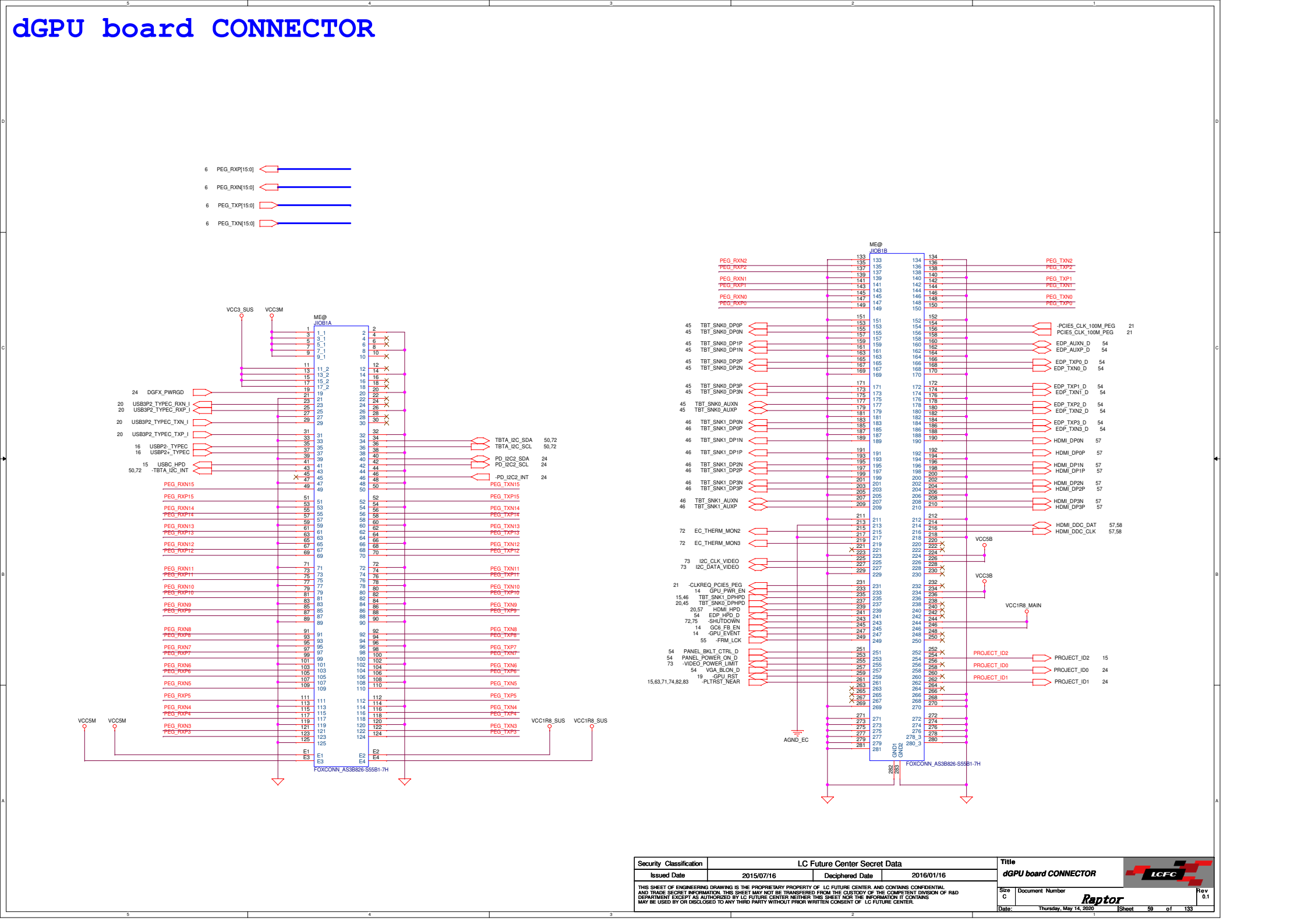
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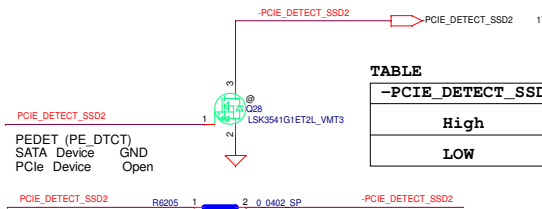
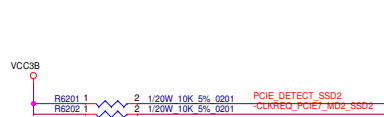
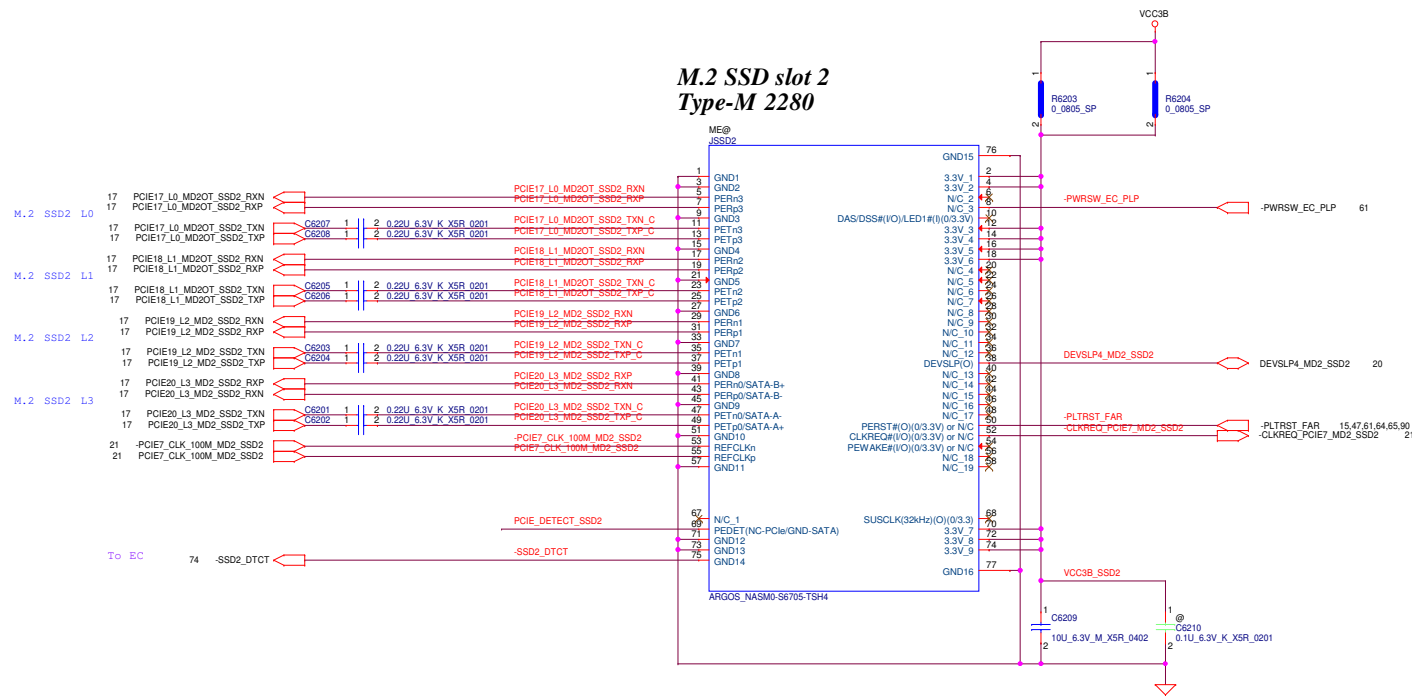
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M.2 SSD

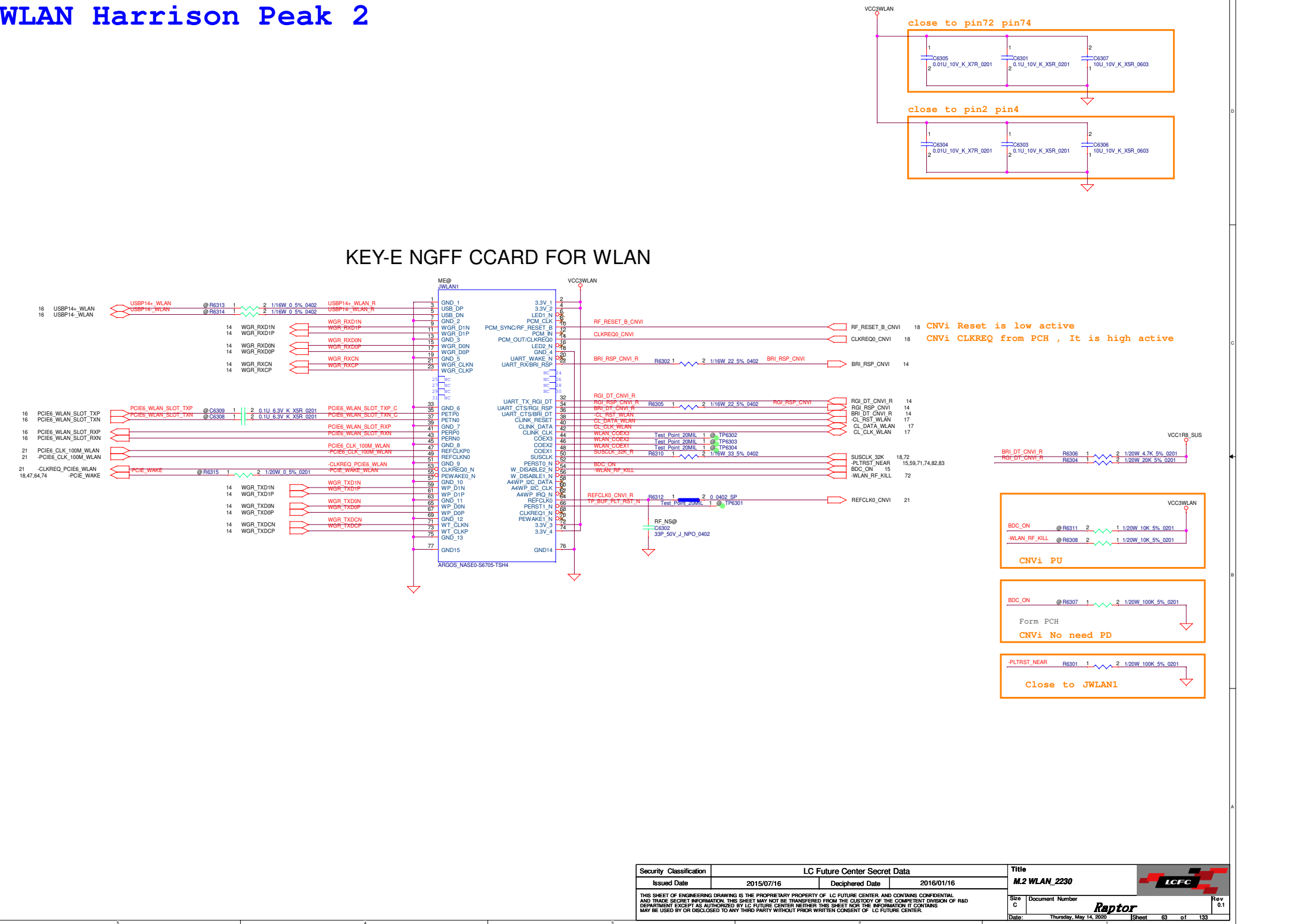


TABLE

-PCIE_DETECT_SS2	Device
High	PCIe SSD
LOW	SATA SSD

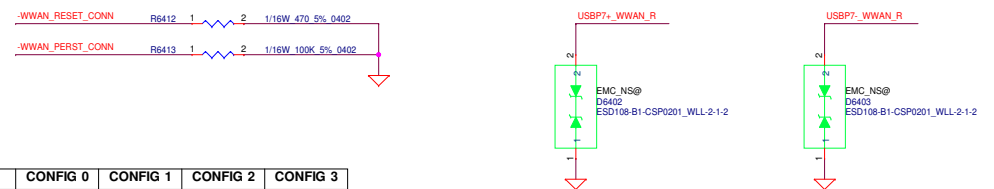
WLAN Harrison Peak 2

KEY-E NGFF CCARD FOR WLAN





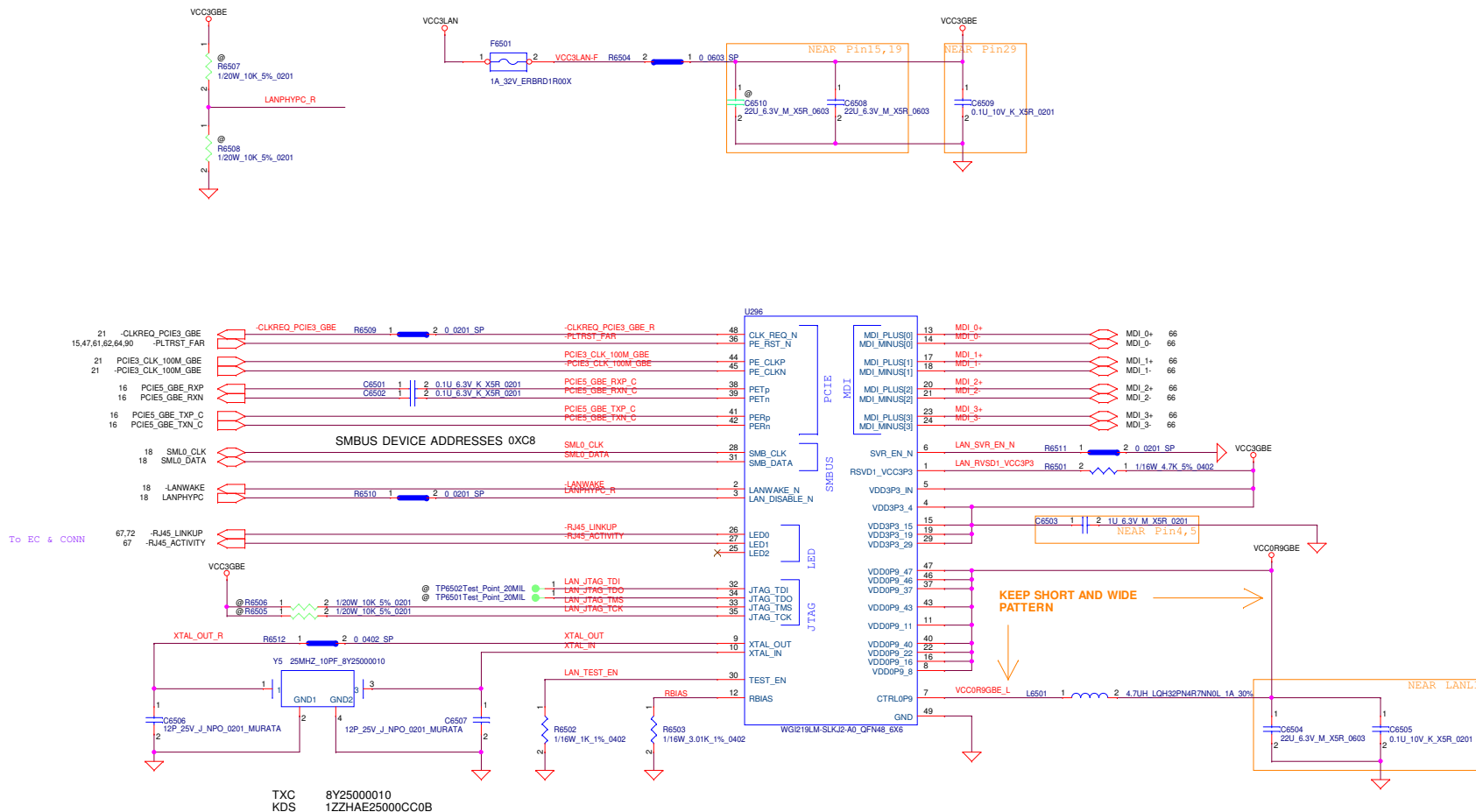
[illegible]

Pin	Pin Name	I/O	Reset Value	Description	Type
36	UIM_PWR	PO	-	USIM power supply	1.8V/3V
30	UIM_RESET	O	L	USIM reset	1.8V/3V
32	UIM_CLK	O	L	USIM clock	1.8V/3V
34	UIM_DATA	I/O	L	USIM data, internal pull up(4.7KΩ)	1.8V/3V
66	SIM_DETECT	I	PD	USIM card detect, internal 390K pull-up. Active high, and high level indicates SIM card is inserted; and low level indicates SIM card is detached.	1.8V

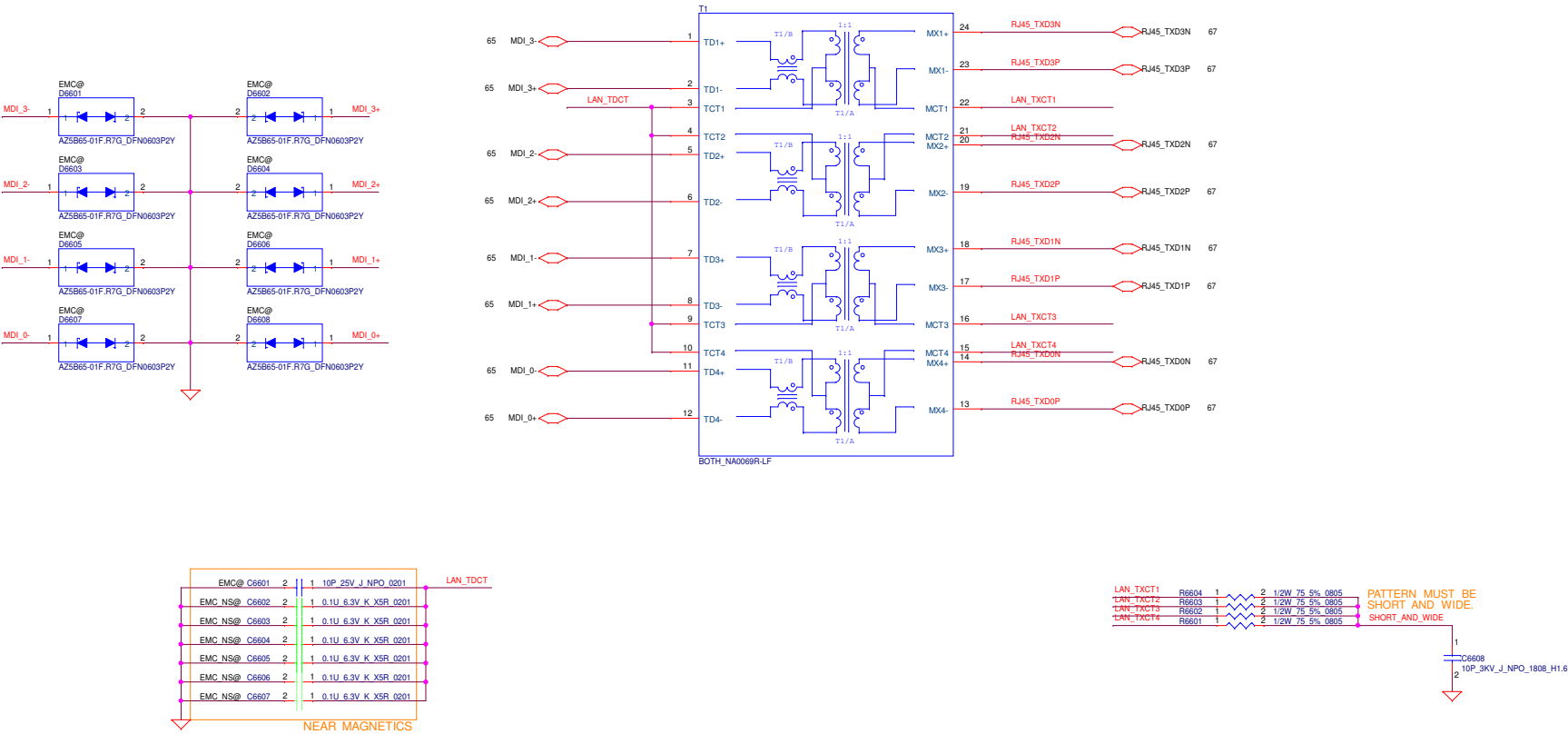


	CONFIG 0	CONFIG 1	CONFIG 2	CONFIG 3
Fibocom L860-GL	NC	GND	NC	NC

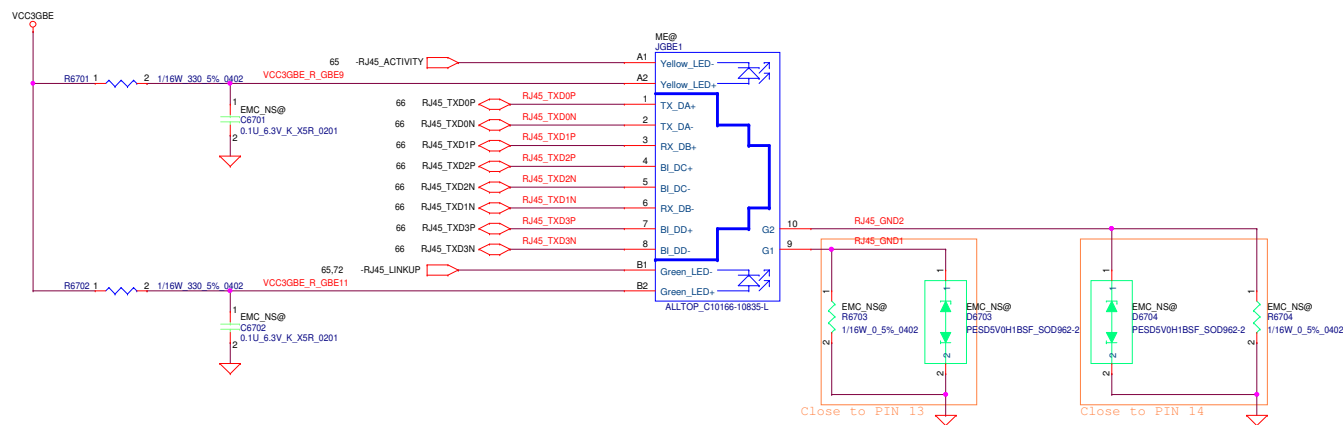
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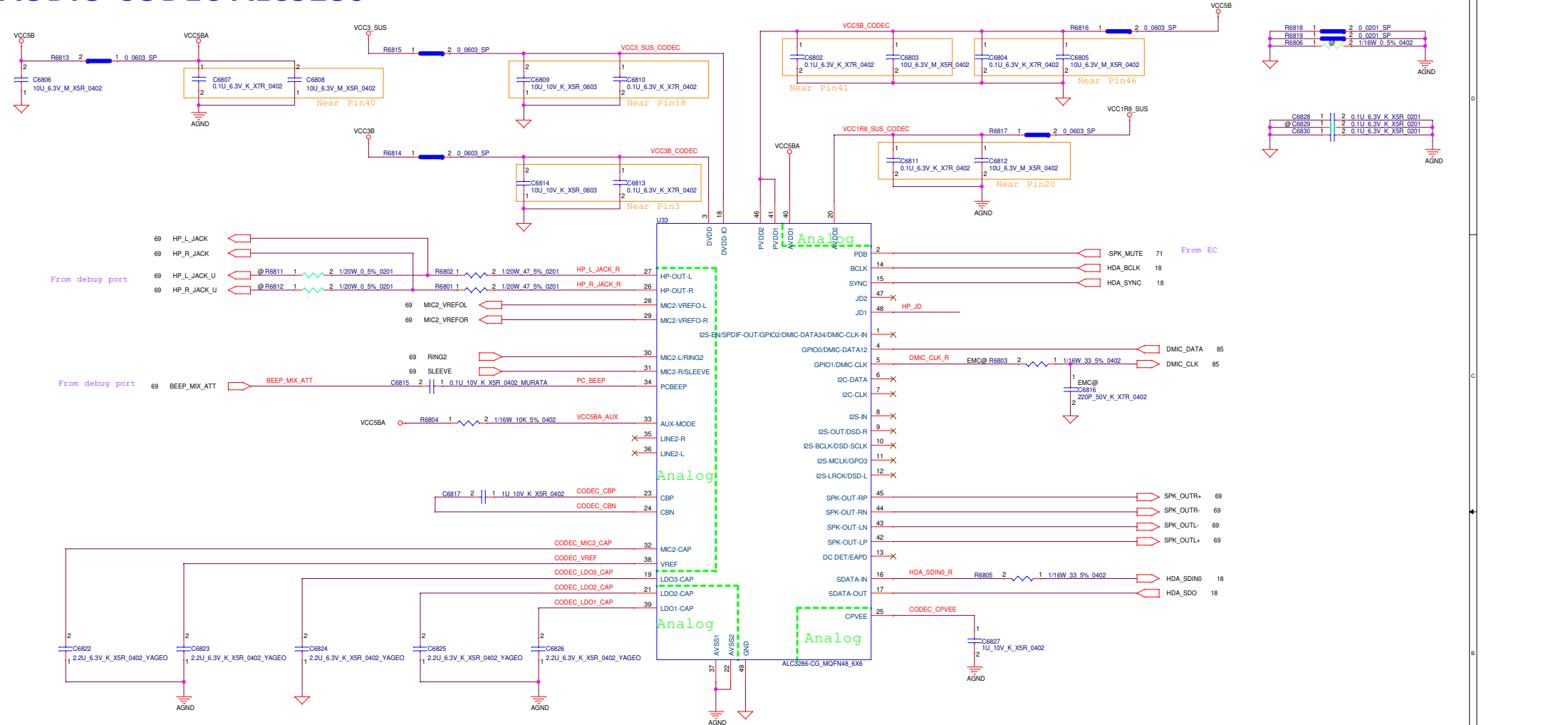
vPRO Model	Non-vPRO Model
I219LM	I219V



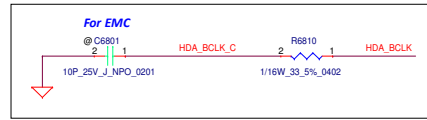
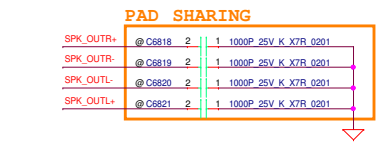
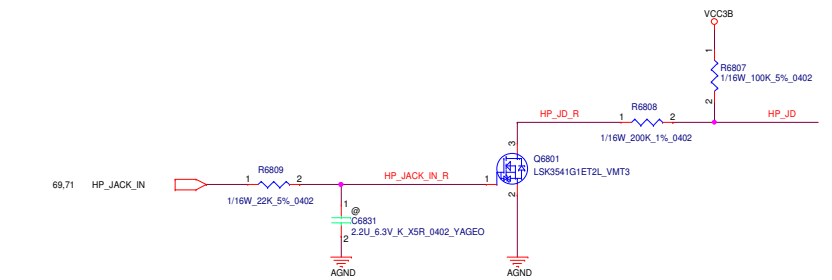
LAN



AUDIO CODEC ALC3286

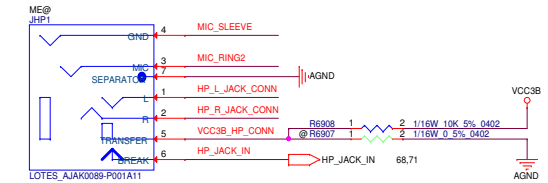
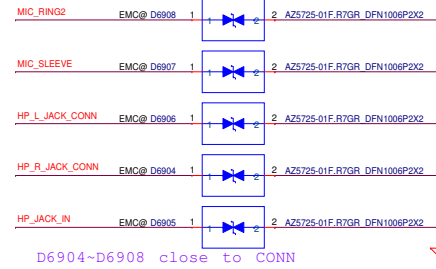
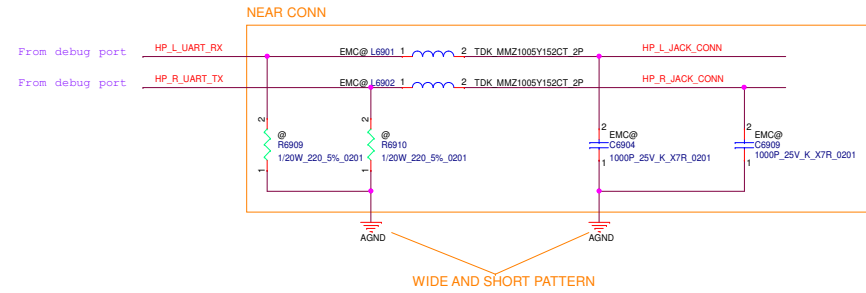
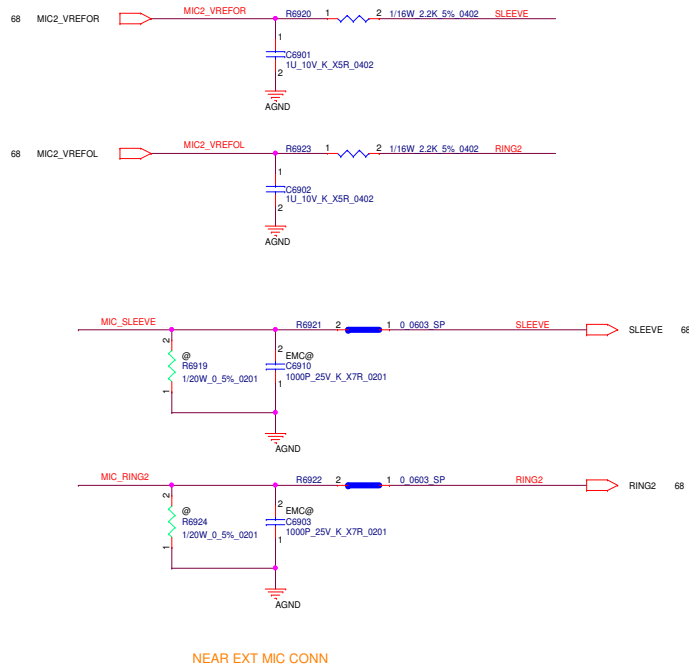


AUDIO JACK SENSE



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HEAD PHONE/AUDIO JACK



AUDIO DEBUG PORT

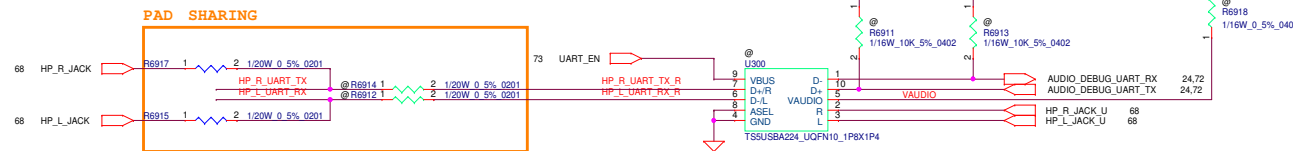


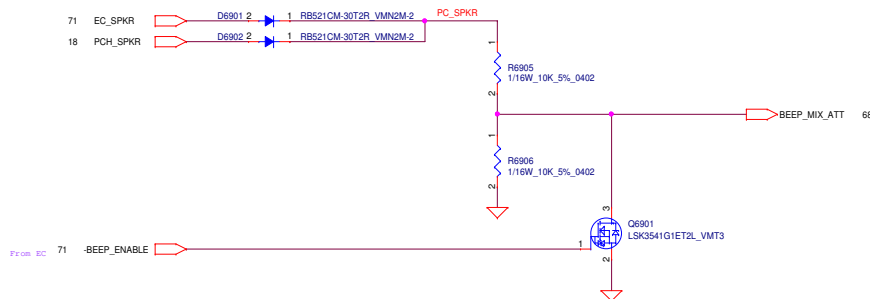
TABLE:

Mode	Audio	UART
UART_EN	L	H

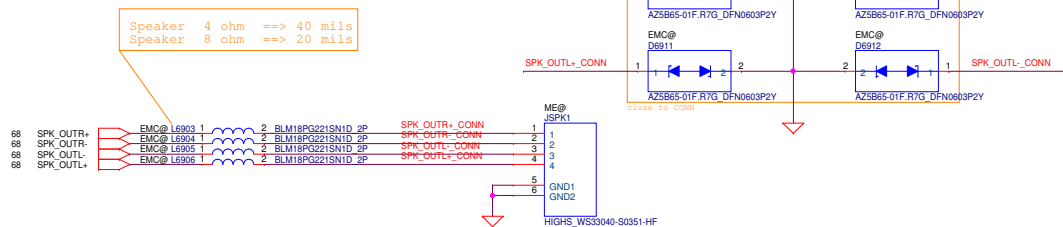
TABLE:

Debug feature	Enable	Disable
U300	ASM	NA
R6912	ASM	NA
R6914	ASM	NA
R6913	ASM	NA
R6918	ASM	NA
R6915	NA	ASM
R6917	NA	ASM



PC BEEP



SPEAKER



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Place near DC-IN CONNECTOR (MB EDGE)

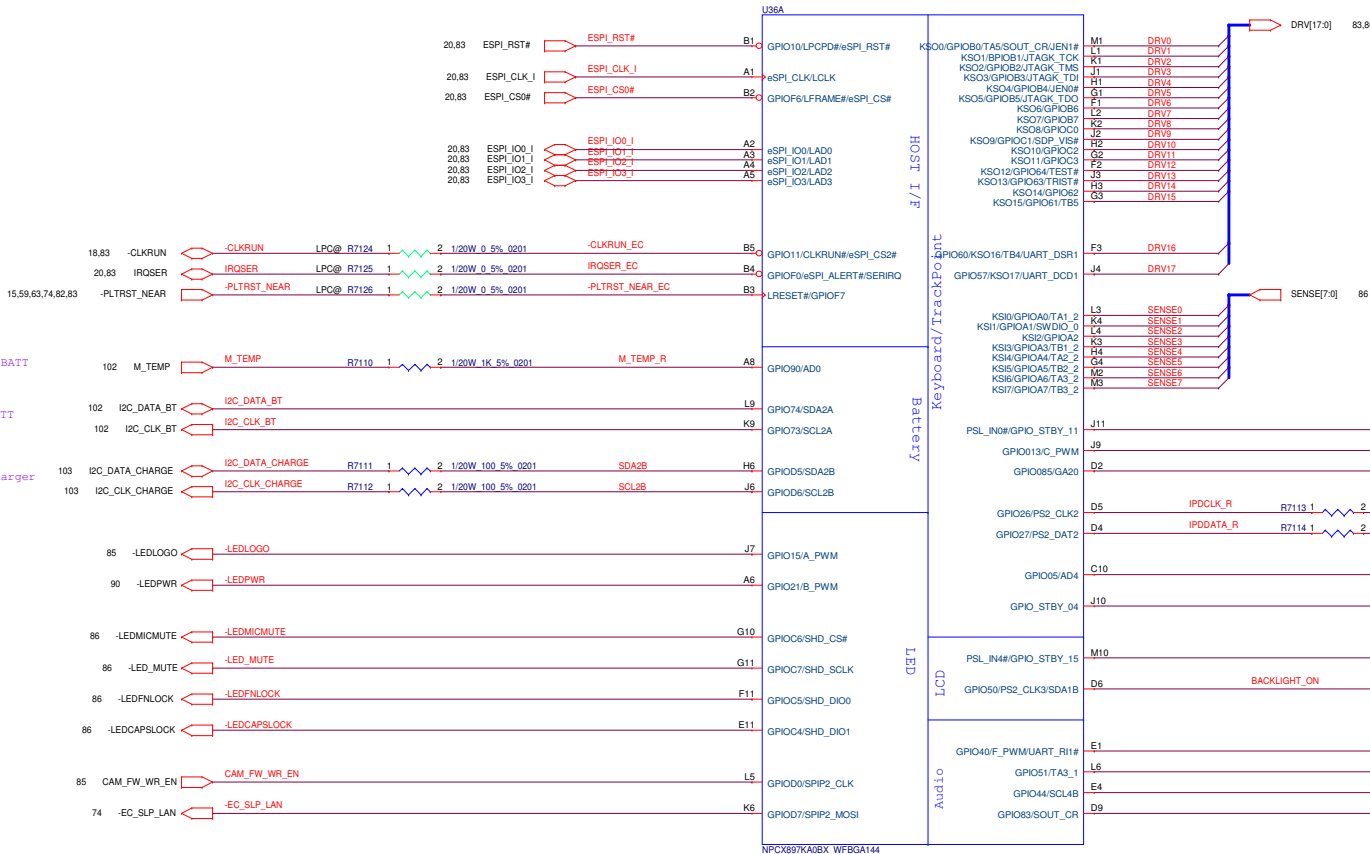
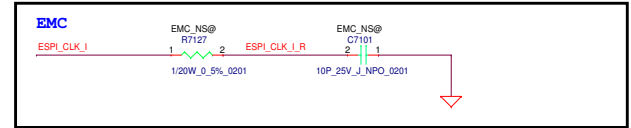
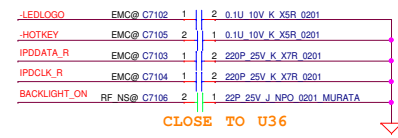
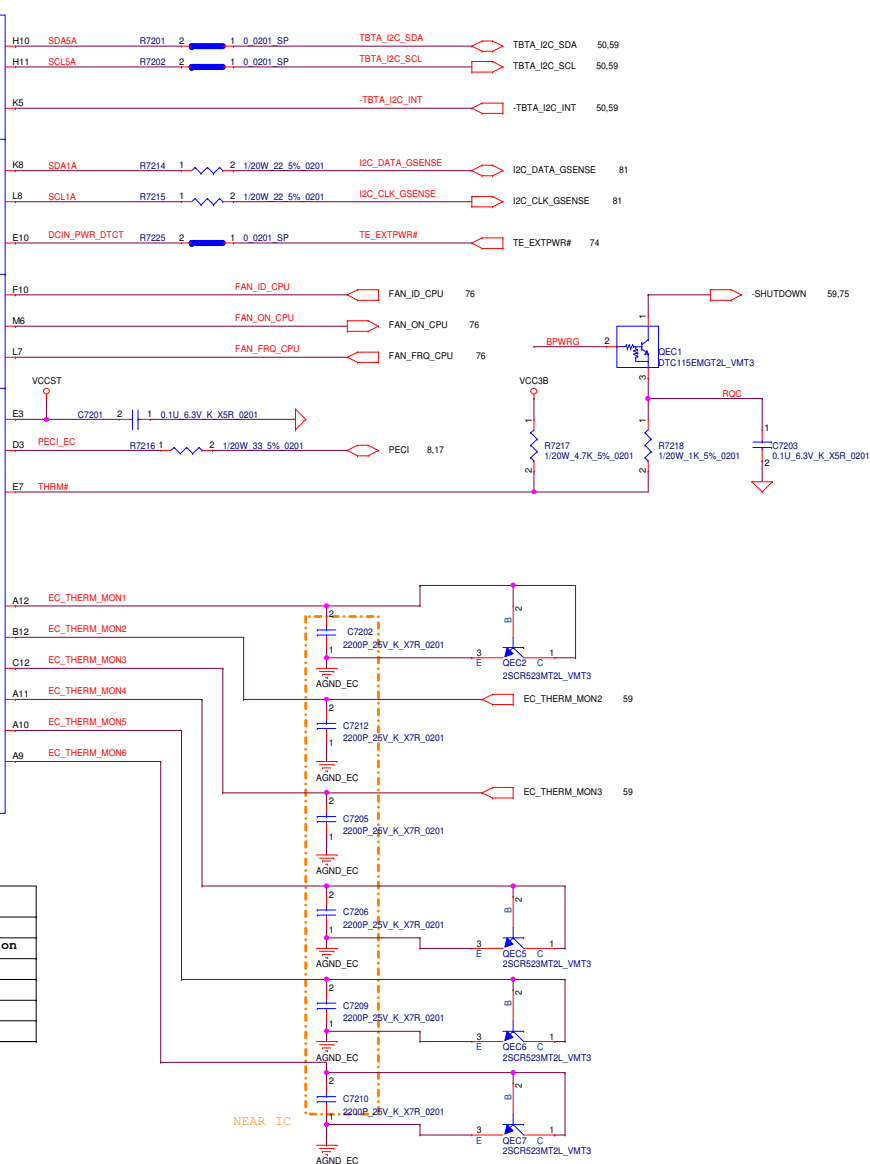
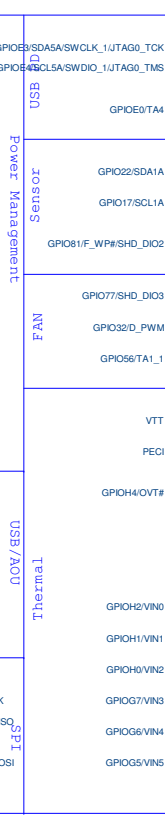
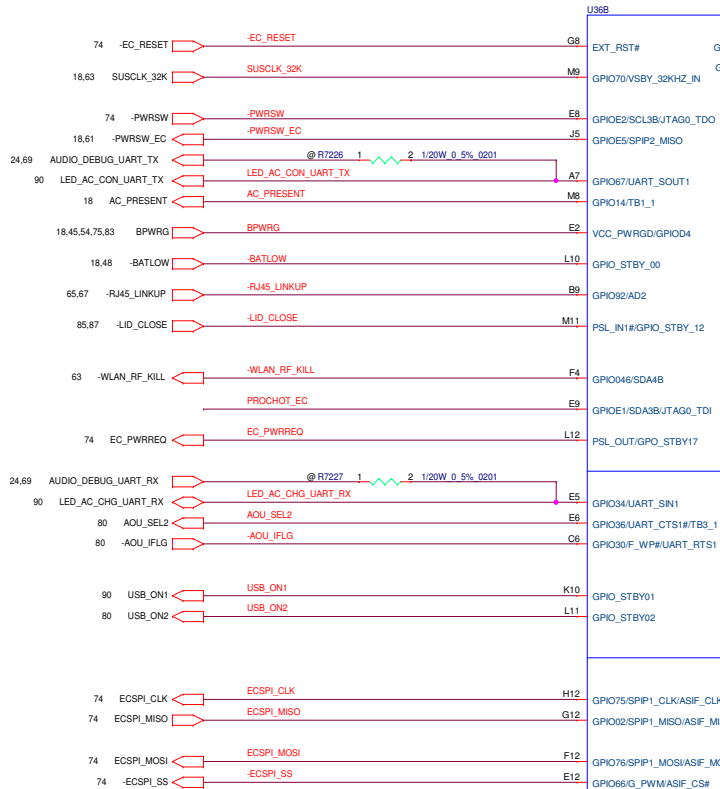
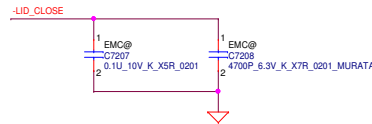
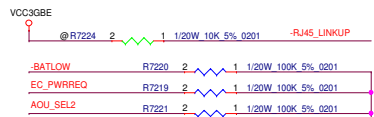
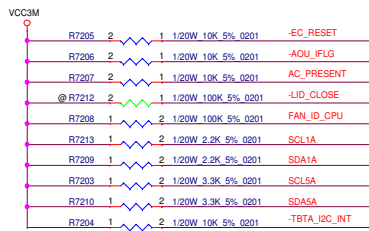


TABLE : Functional Strap

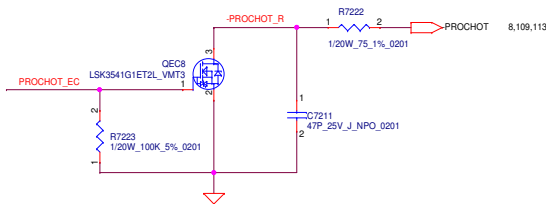
JEN1#/KSO0 (JTAG 1 Select)	
OPEN	JTAG K is disabled
LOW	JTAG K is selected

LOGIC

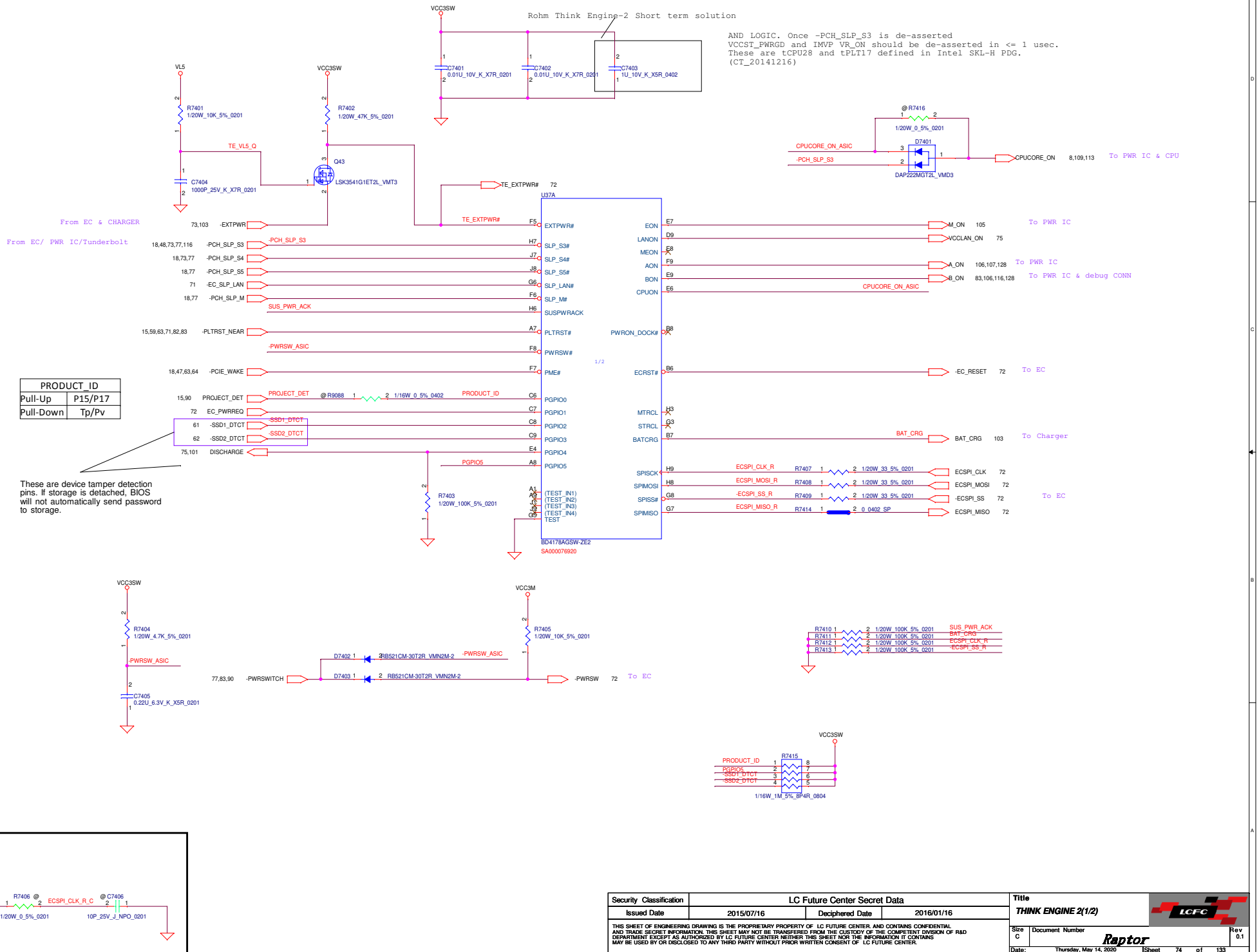




Thermal Diode Table		
ID (Location)	Raptor	
	Device	Placed on
DIODE 1 (QEC2)	CPU DCDC	BOT
DIODE 4 (QEC5)	CPU FAN	TOP
DIODE 5 (QEC6)	DDR DCDC	TOP
DIODE 6 (QEC7)	SSD	BOT

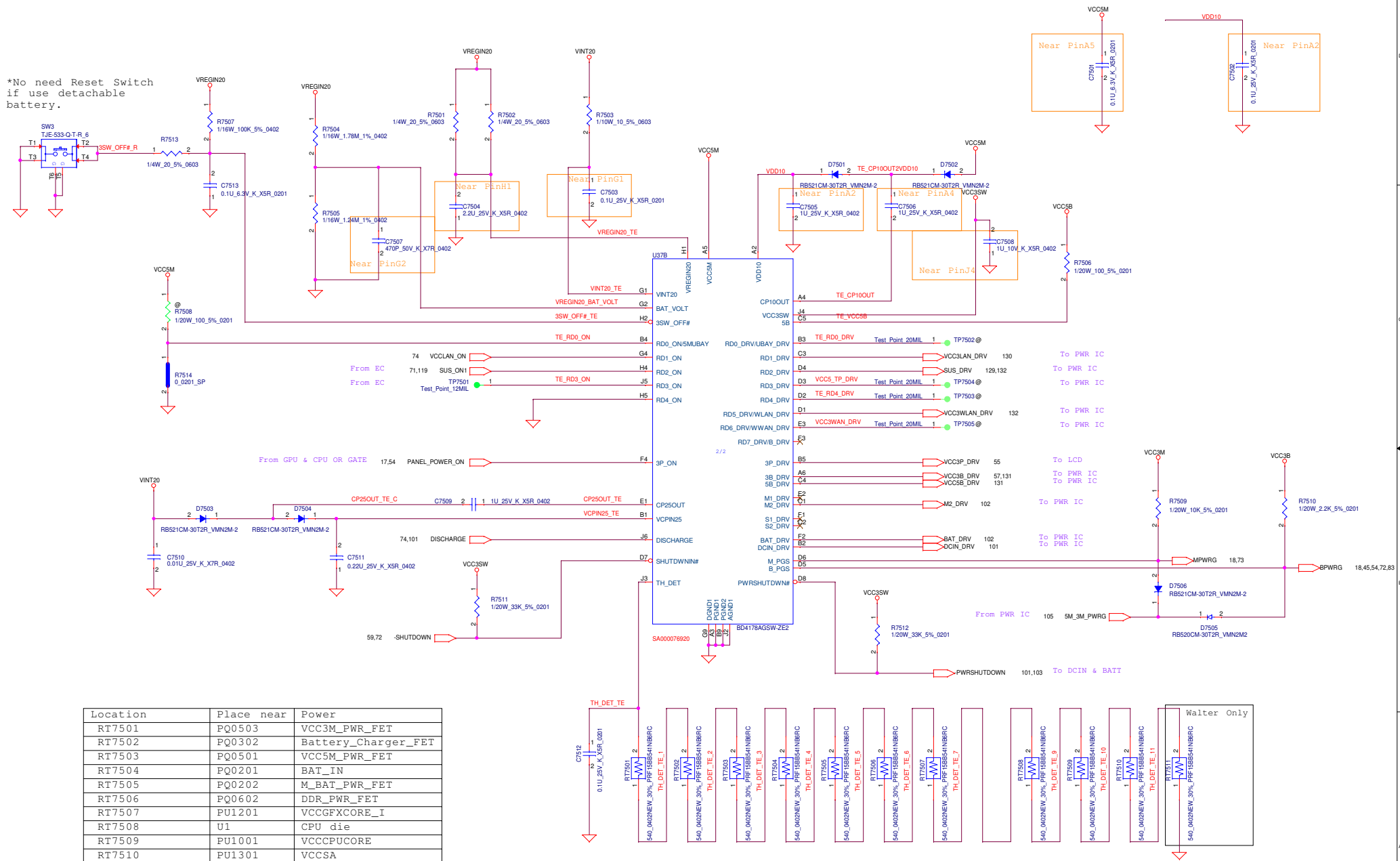


THINK ENGINE



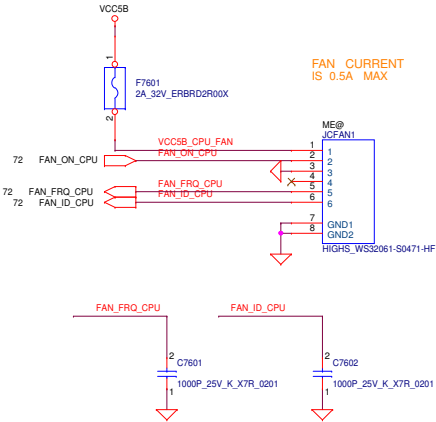
THINK ENGINE

*No need Reset Switch
if use detachable
battery.

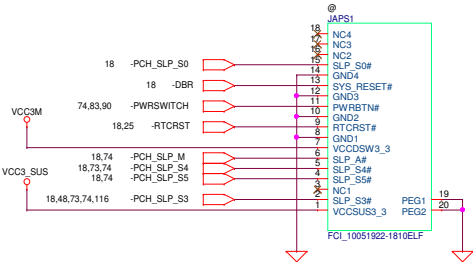


Location	Place near	Power
RT7501	PQ0503	VCC3M_PWR_FET
RT7502	PQ0302	Battery_Charger_FET
RT7503	PQ0501	VCC5M_PWR_FET
RT7504	PQ0201	BAT_IN
RT7505	PQ0202	M_BAT_PWR_FET
RT7506	PQ0602	DDR_PWR_FET
RT7507	PUI201	VCCGFXCORE_I
RT7508	U1	CPU die
RT7509	PUI001	VCCCPUCORE
RT7510	PUI301	VCCSA
RT7511	PQ0101	DCIN_PWR_FET

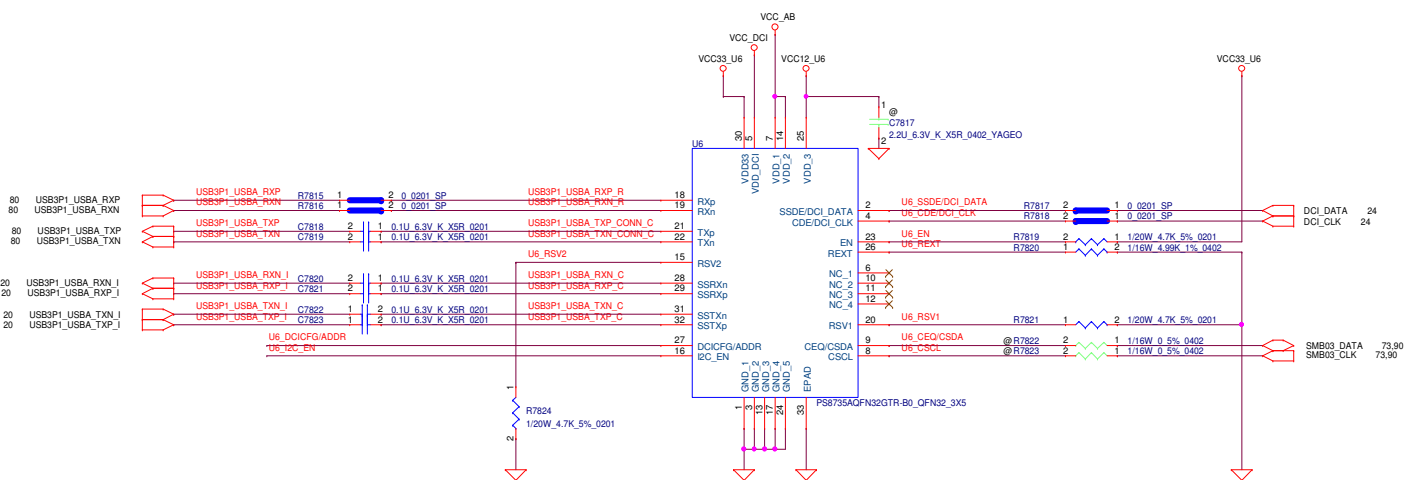
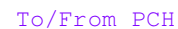
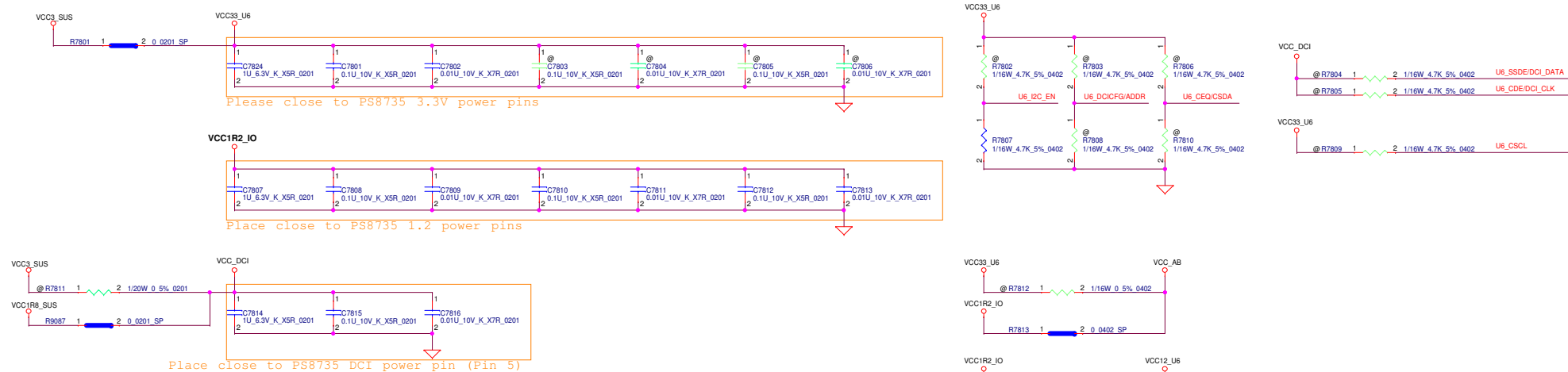
CPU FAN





APS CONN.




USB3.1 Redriver

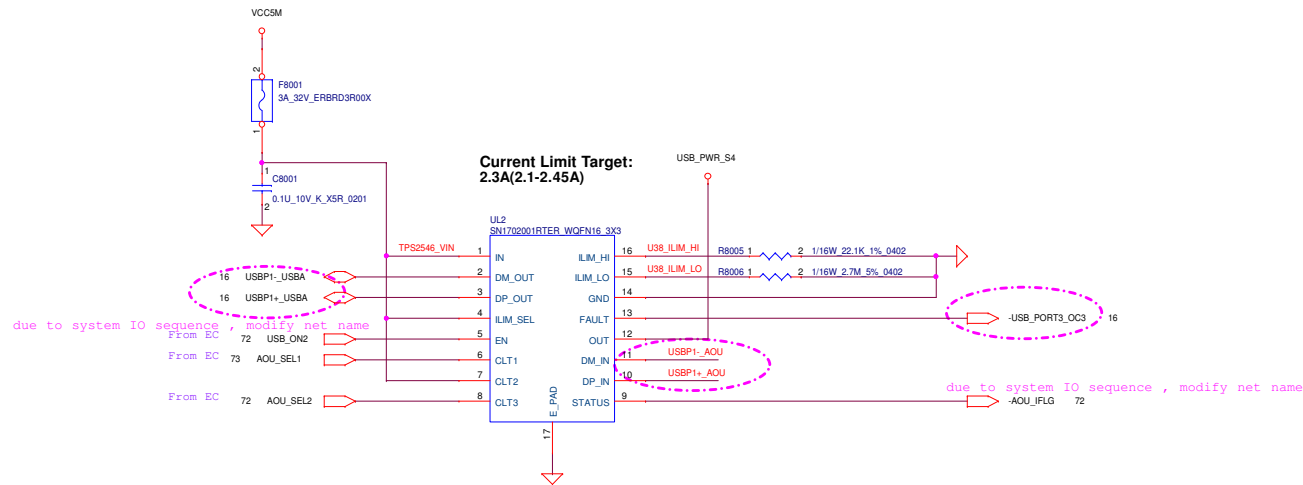


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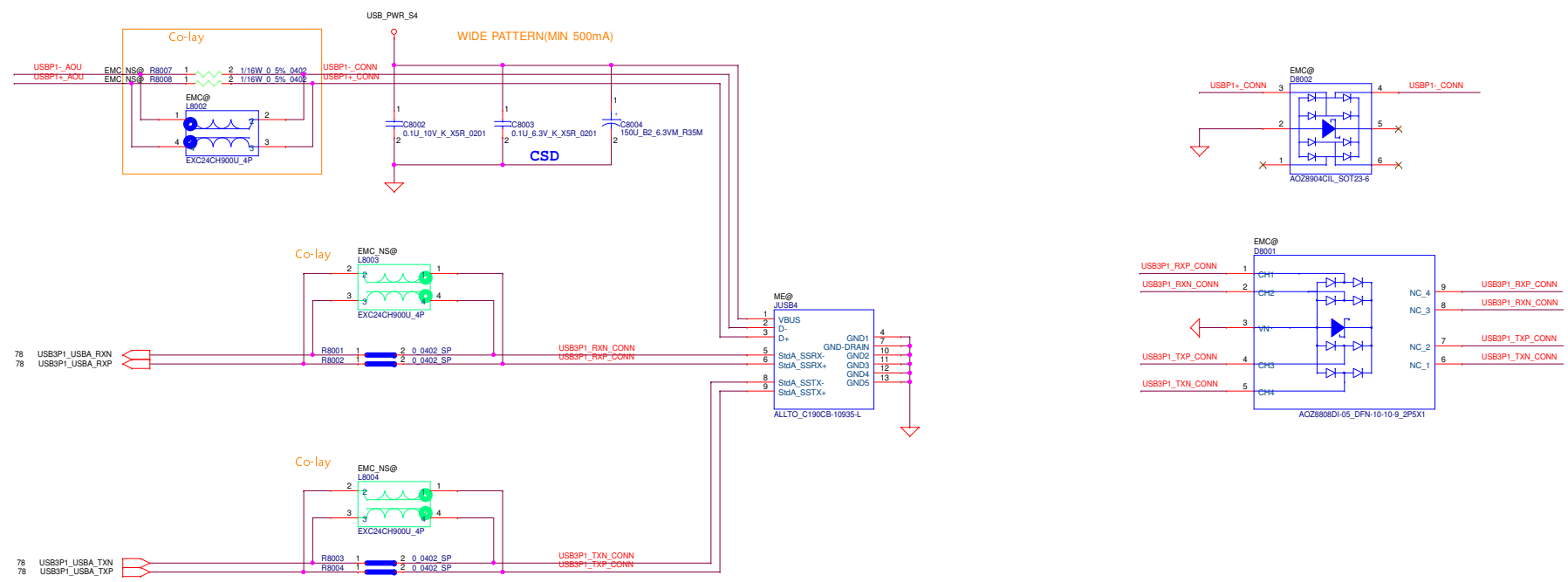
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USB Charger IC



USB3.0 CONN



Vendor	ADDR_SEL	Address
Kionix	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)
ST	H L	32h (W) & 33h (R) 30h (W) & 31h (R)

DISCRETE TPM 2.0

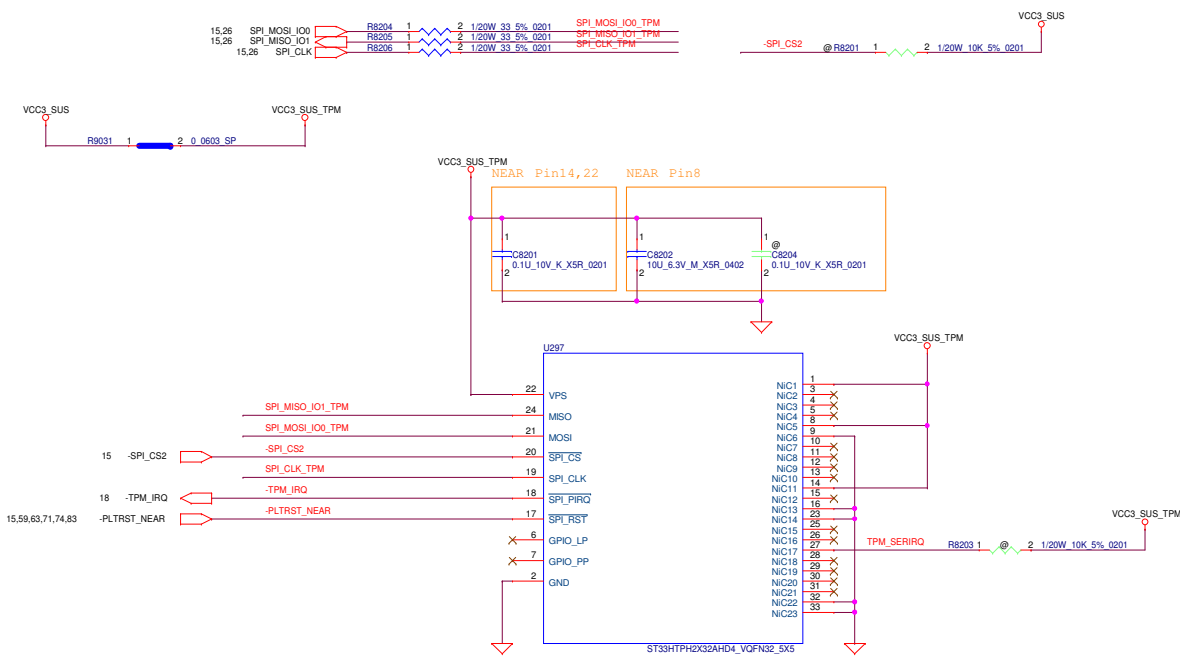
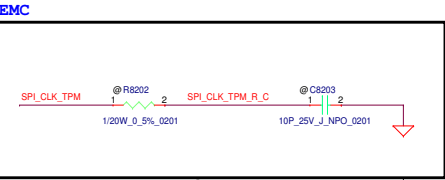
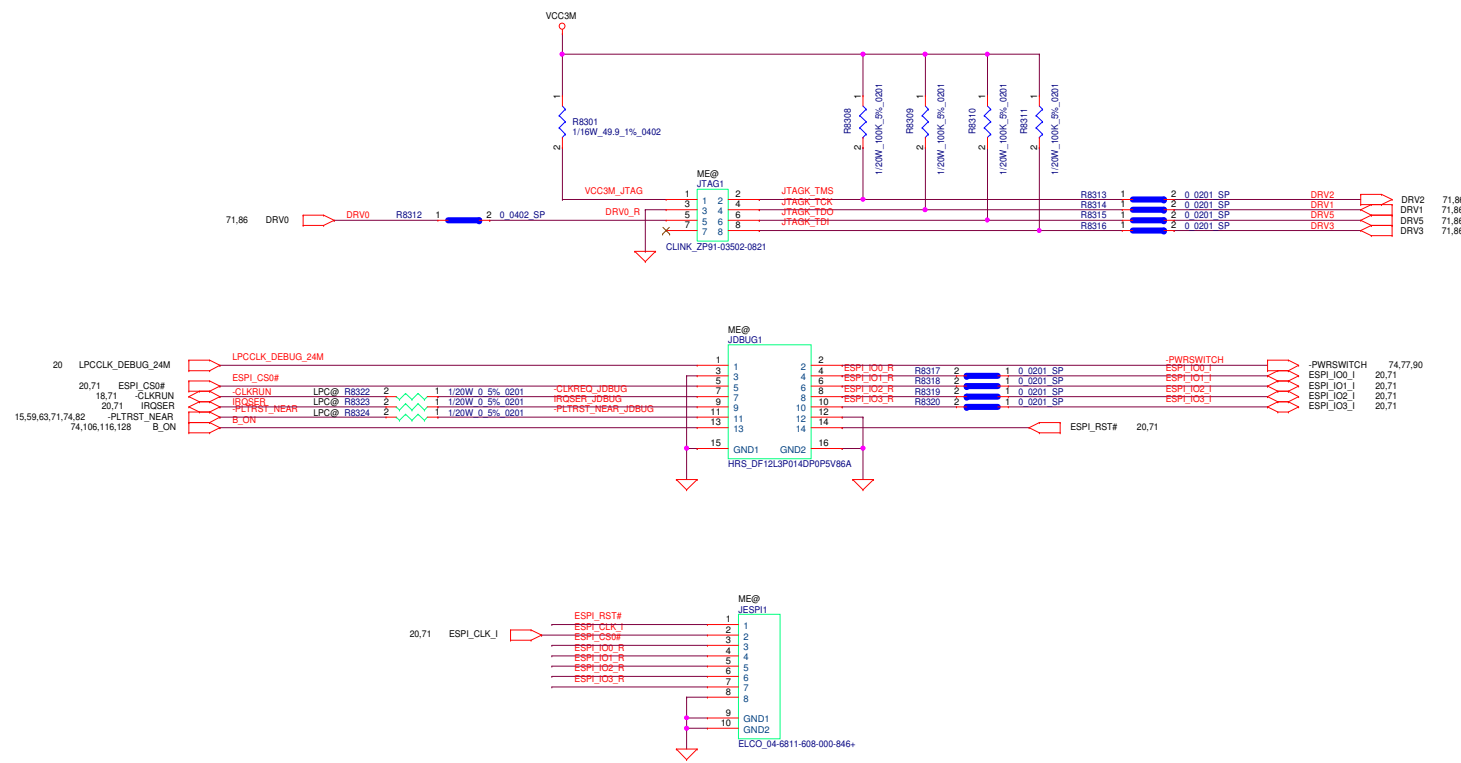


TABLE	Main Source		2nd Source	
	Pin No	ST Micro ST33HTPH2X32AHD4 SA0000AB710	NUVOTON NPCT750LABYX SA00006KS20	
	1	NIC	VSB	
	2	GND	NC	
	3	NIC	NC	
	4	NIC	PP/GPIO6	
	5	NIC	NC	
	6	GPIO_LP	GPIO3	
	7	GPIO_PP	NC	
	8	NIC	VHIO	
	9	NIC	NC	
	10	NIC	NC	
	11	NIC	NC	
	12	NIC	NC	
	13	NIC	GPIO4	
	14	NIC	NC	
	15	NIC	NC	
	16	NIC	GND	
	17	SPI_RST#	PLTRST#	
	18	SPI_PIRQ#	PIRQ#/GPIO2	
	19	SPI_CLK	SCLK	
	20	SPI_CS#	SCS#/GPIO5	
	21	MOSI	MOSI/GPIO7	
	22	VPS	VHIO	
	23	NIC	GND	
	24	MISO	MISO	
	25	NIC	NC	
	26	NIC	NC	
	27	NIC	NC	
	28	NIC	NC	
	29	NIC	SDA/GPIO0	
	30	NIC	SCL/GPIO1	
	31	NIC	NC	
	32	NIC	NC	



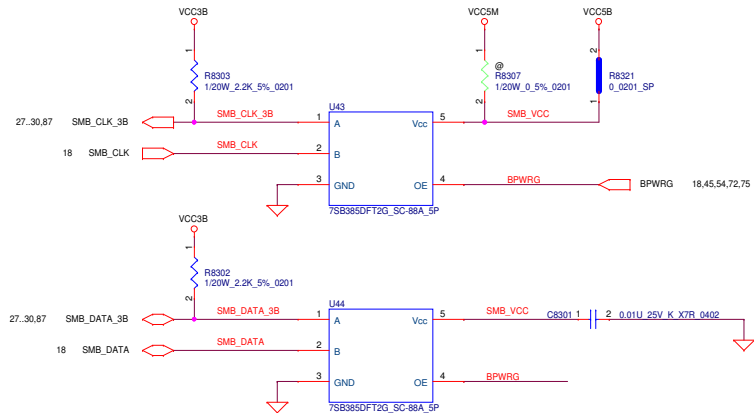
LPC/eSPI DEBUG PORT



LPC Debug Port

	ENABLE	DISABLE
JTAG1	ASM	NO ASM
JTAG2	ASM	NO ASM
JTAG3	ASM	NO ASM
JTAG4	ASM	NO ASM
JTAG5	ASM	NO ASM

SMBUS SWITCH



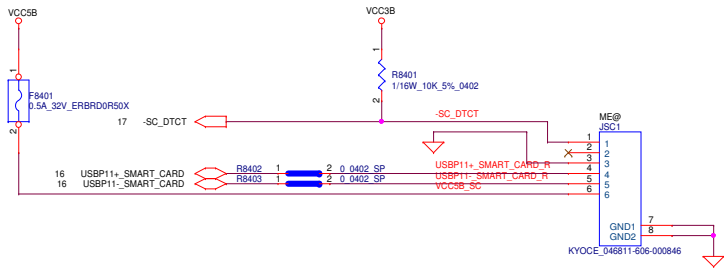
Close to U43.1 and U43.2

SMB_CLK_3B @R8305 2 1/20W 0.5% 0201 SMB_CLK

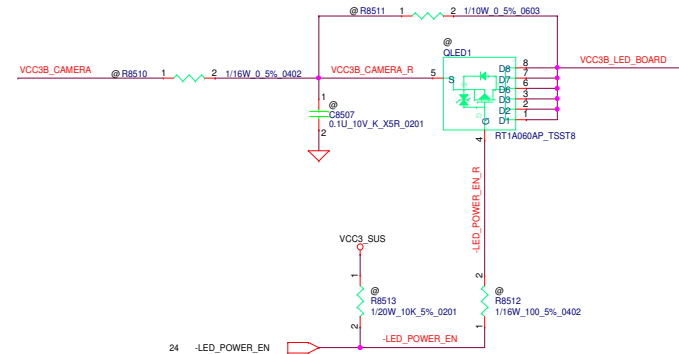
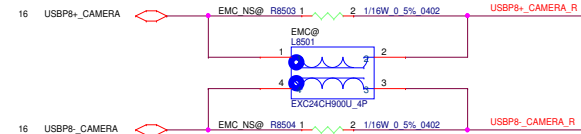
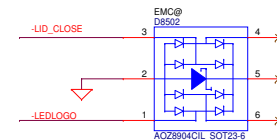
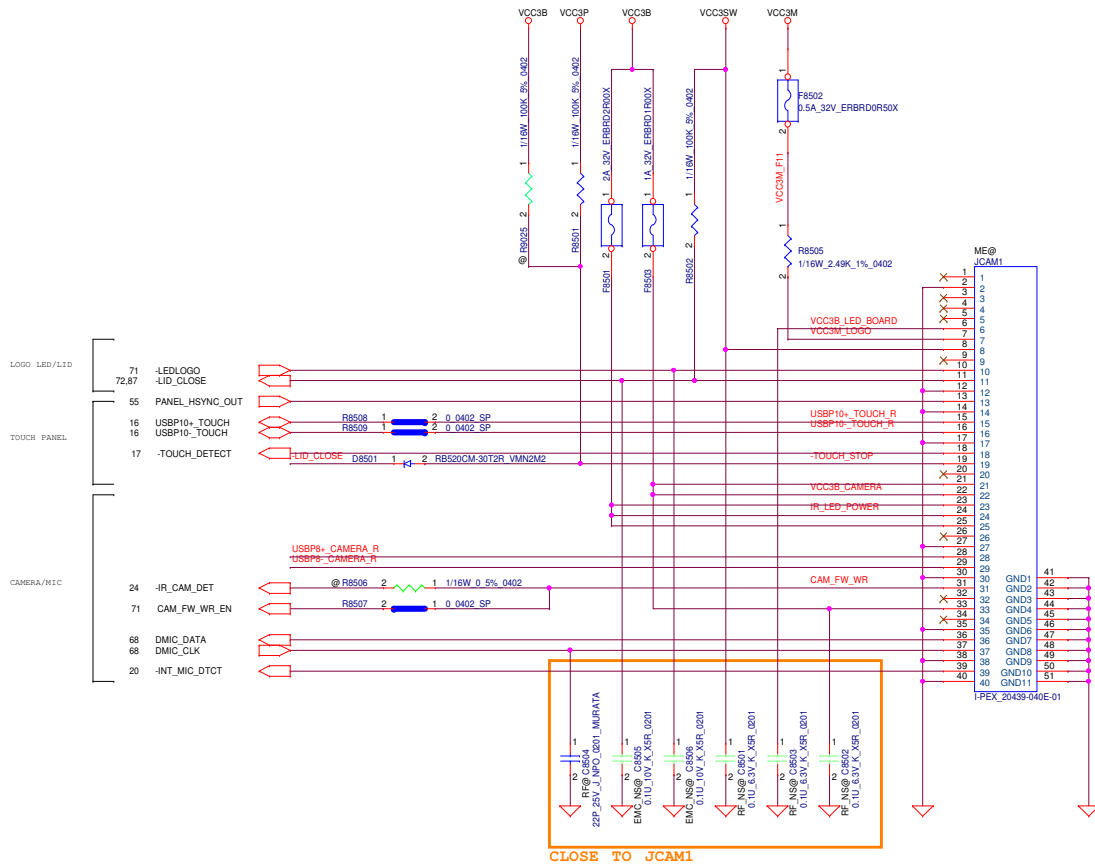
Close to U44.1 and U44.2

SMB_DATA_3B @R8306 2 1/20W 0.5% 0201 SMB_DATA

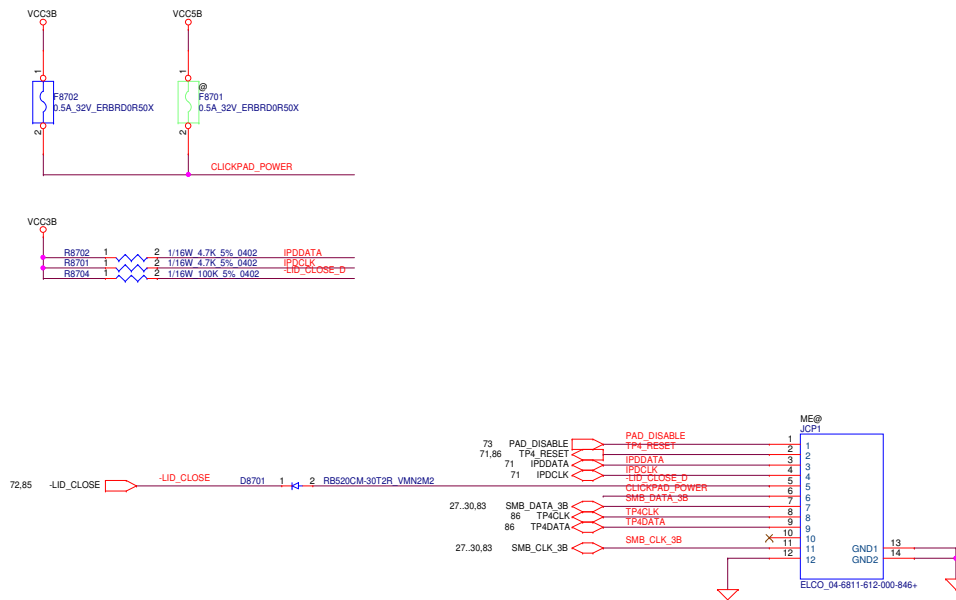
SMART CARD



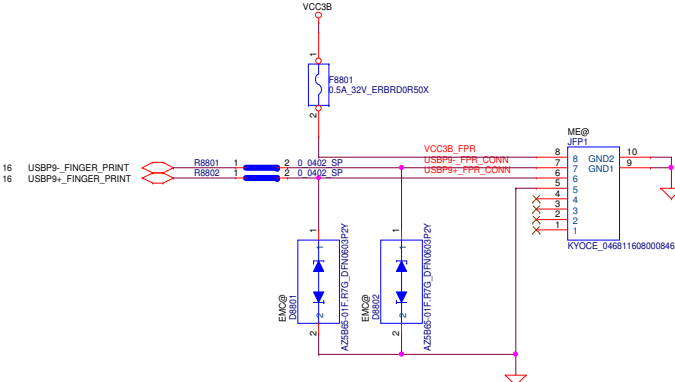
CAMERA/TOUCH




CLICK PAD



Finger Print

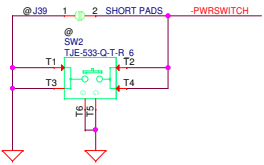


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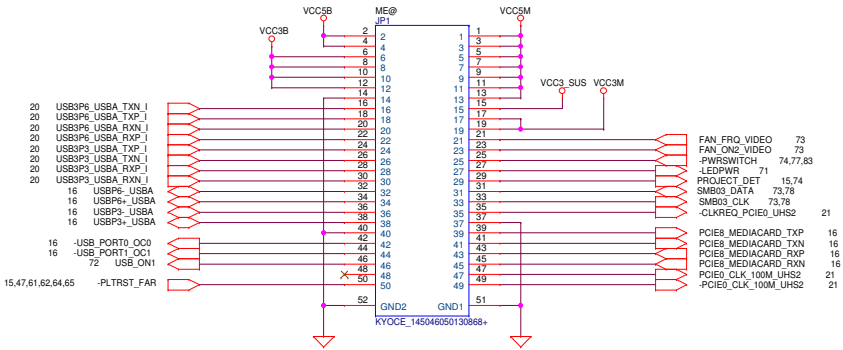
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Power Switch

ON/OFF switch



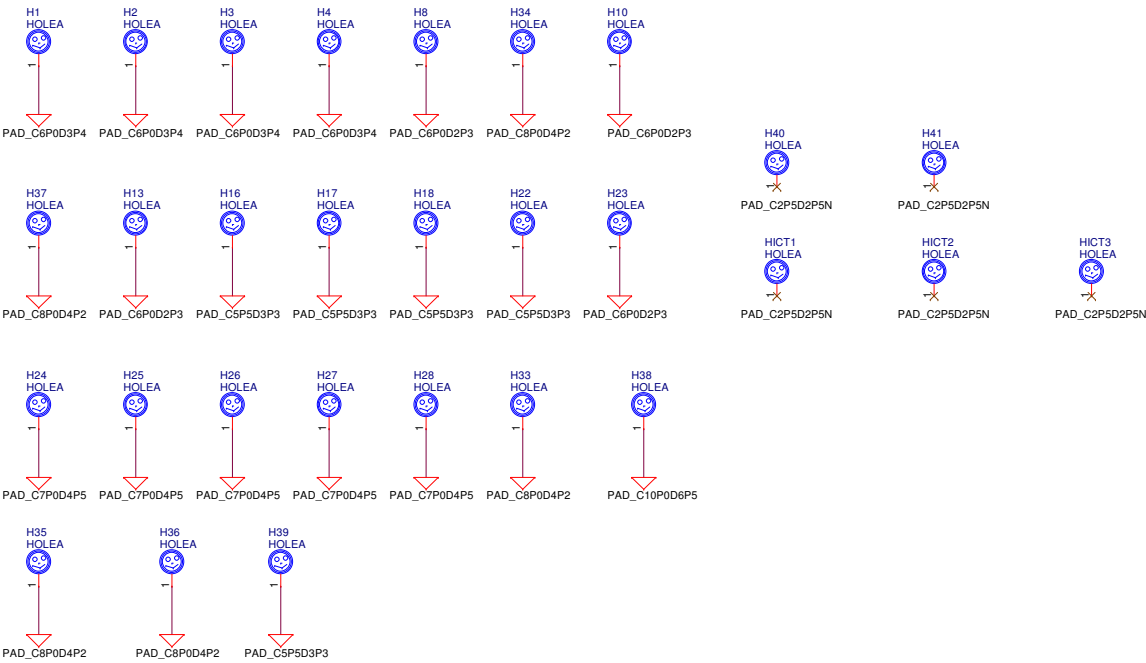
IO/B CONN.



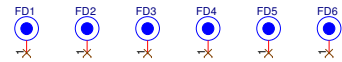
AC-IN LED



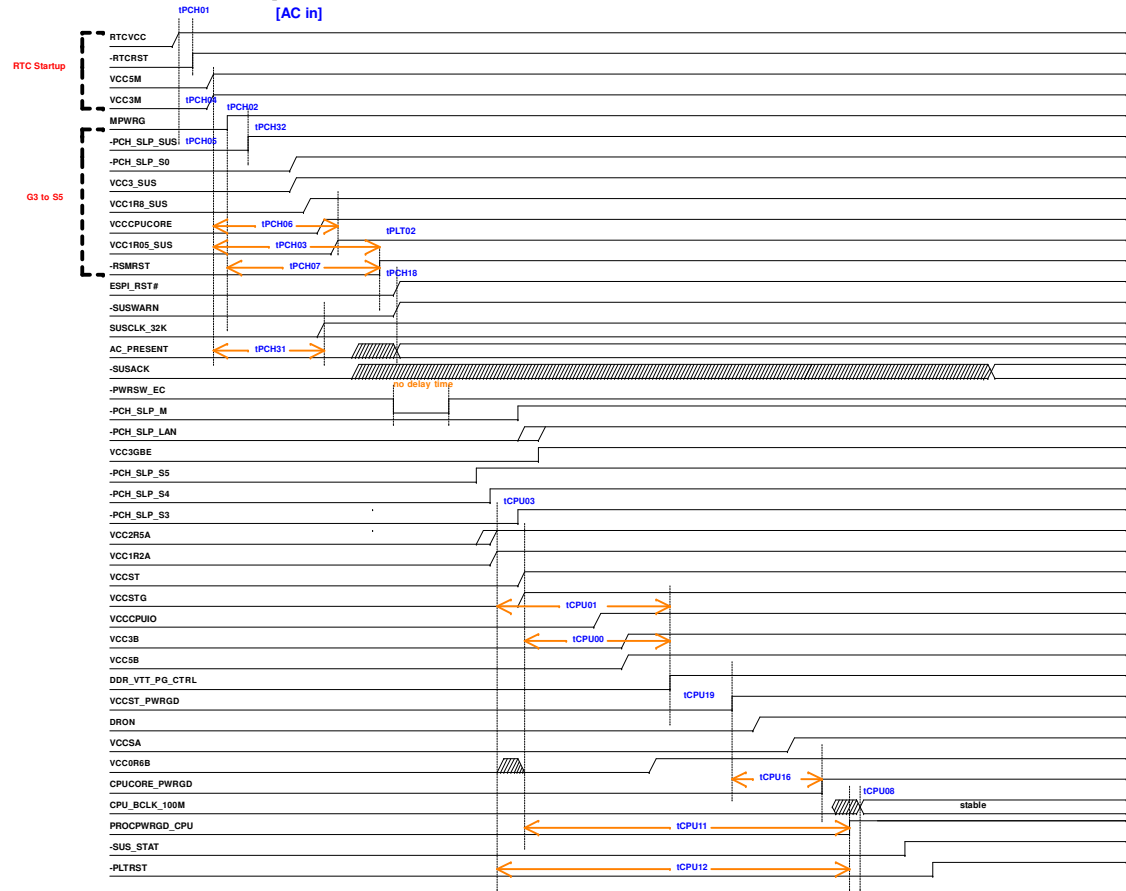
Raptor Unique



PCB Fedical Mark PAD



CML-H Power On Sequence
G3 to S0/M0 [Deep Sx Platform]



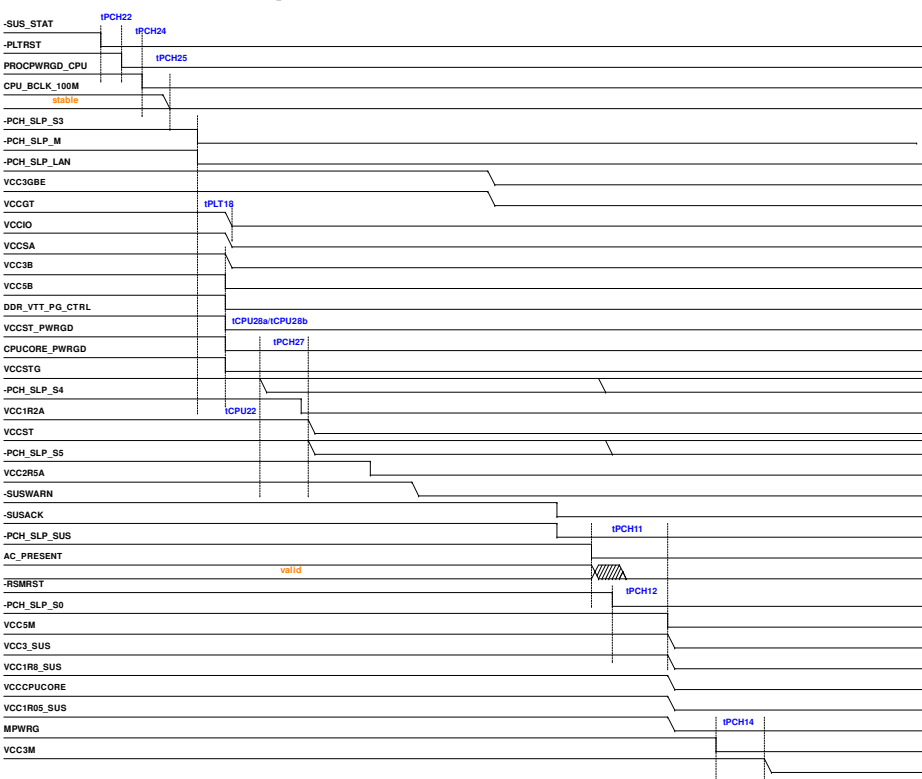
Item	Measure Point	Spec. time	P15/P17 time	Result
IPCH01	RTCVCC To -RTCRST	>9ms	128.5ms	PASS
IPCH04	RTCVCC To VCC3M	>9ms		
IPCH05	-RTCRST To MPWRG	>1us		
IPCH02	VCC3M To -PCH_SLP_SUS	>10ms		
IPCH32	MPWRG To VCC1R05_SUS	>95ms		
IPCH06	VCC3M To VCC1R8_SUS	>200us		
	VCC3_SUS To VCCCPUCORE			
	VCC1R8_SUS To VCCCPUCORE			
	VCCCPUCORE To VCC1R05_SUS			
	VCC1R05_SUS To -RSMRST		18ms	
IPCH18	-RSMRST To ESPL_RST#	>90us		
IPCH107	MPWRG To -RSMRST	>0ms		
IPCH31	VCC3M To SUSCLK_32K	<105ms		
IPCH03	VCC1R05_SUS To -RSMRST	>10ms		
IPLT02	-RSMRST To ACPRESENT	<0ms		
IPCH15	-PCH_SLP_LAN To VCC3GBE	<20ms		
	-PCH_SLP_S5 To -PCH_SLP_S4			
	-PCH_SLP_S4 To -PCH_SLP_S3			
ICPU03	VCC1R2A To VCCST	<25ms		

Item	Measure Point	Spec. time	P15/P17 time	Result
	VCCST To VCCCPUIO		5.73ms	
	VCCCPUIO To VCC3B		2.43ms	
	VCC3B To VCC5B		2.435ms	
tCPU01	VCC1R2A To VCCST_PWRGD	>1ms	8.66ms	
ICPU00	VCCSTG To VCCST_PWRGD	>1ms	4.89ms	
ICPU11	VCCST To PROC_PWRGD_CPU	>1ms	93.6ms	
ICPU19	VCCST_PWRGD To DDR_VTT_CTRL	0~100ms	0s	
ICPU12	VCC1R2A To PROC_PWRGD_CPU	<1ms	93ms	
ICPU16	VCCST_PWRGD To CPUCORE_PWRGD	>0ms	21.2ms	
ICPU08	CPU_BCLK_100M To PROC_PWRGD_CPU	>1ms	1.015ms	

CPU_C10_GATE# sequence (reserved)

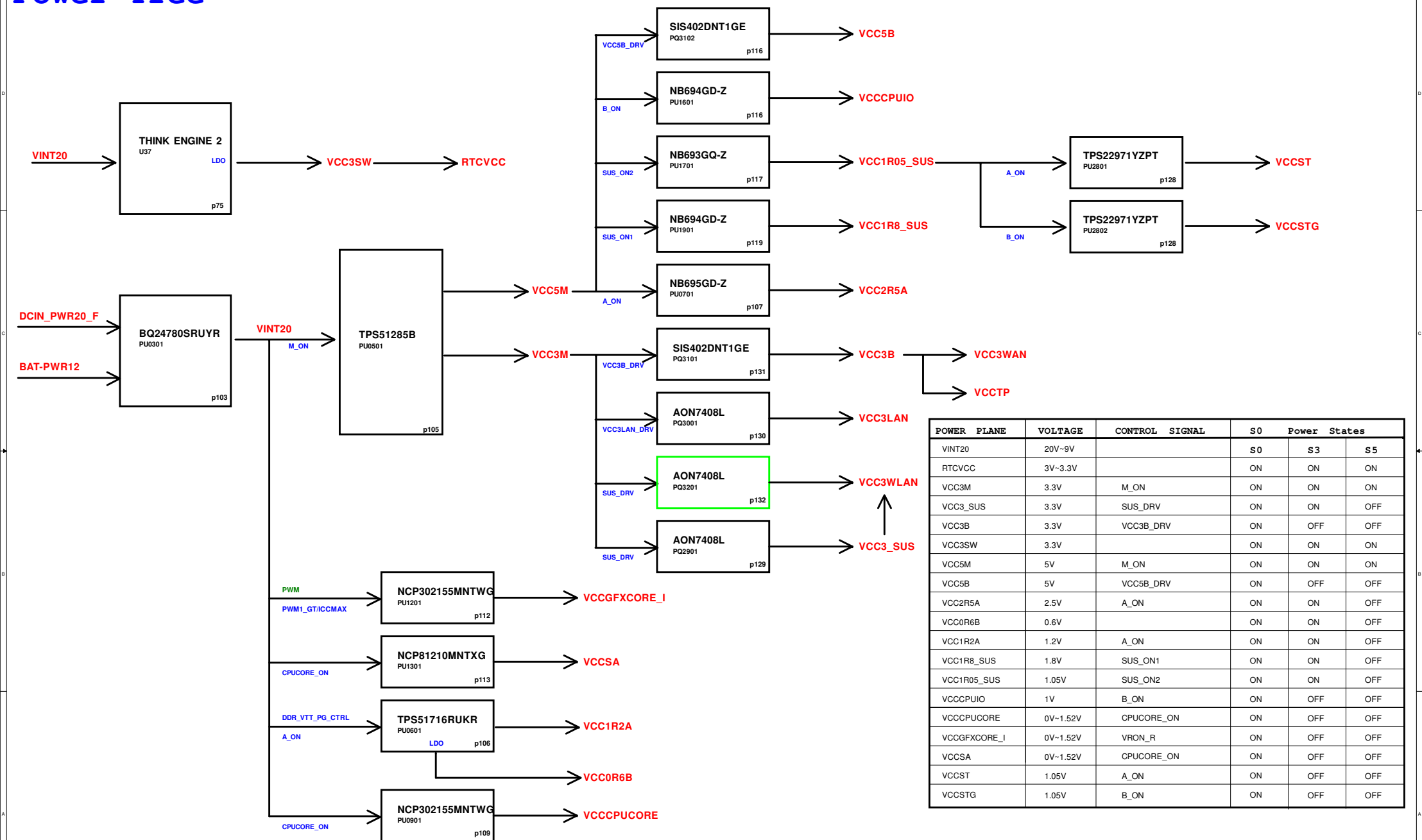
tCPU26	All	CPU	PLT	10	65	us	11	CPU_C10_GATE# de-assertion to VCCSTG stable Note: CPU_C10_GATE# de-assertion to VCCST also needs to meet max 65us on cold boot
tCPU27	All	CPU	PLT	10	240	us	11	CPU_C10_GATE# de-assertion to VCCIO stable
tCPU33	All	CPU	PLT		240	us	11	CPU_C10_GATE# de-assertion to VCCPLL_OC stable

CML-H Power Off Sequence
S0/M0 to G3 [Deep Sx Platform]




Item	Measure Point	Spec. time	P15/P17 time	Result
IPCH22	ESPL_RST# To -PLTRST	>210us		PASS
IPCH24	-PLTRST To PROC_PWRGD_CPU	>30us		
IPCH25	PROC_PWRGD_CPU To CPU_BCLK_100M	>10us		
IPLT18	-PCH_SLP_S3 To VCCCPUIO	<200us		
ICPU28a	-PCH_SLP_S3 To VCCST_PWRGD	<200us		
ICPU28b	VCCST_PWRGD To VCCST	>0us		
IPCH27	-PCH_SLP_S4 To -PCH_SLP_S5	>30us		
ICPU22	VCCST_PWRGD To VCCSTG	>1us		
IPCH11	-PCH_SLP_SUS To VCC1R05_SUS	>100ns		
IPCH12	-RSMRST To VCC5M	>400ns		
IPCH14	MPWRG To VCC3M	>400ns		

Power Tree




POWER PLANE	VOLTAGE	CONTROL SIGNAL	S0	Power States	
VINT20	20V~9V		S0	S3	S5
RTCVCC	3V~3.3V		ON	ON	ON
VCC3M	3.3V	M_ON	ON	ON	ON
VCC3_SUS	3.3V	SUS_DRV	ON	ON	OFF
VCC3B	3.3V	VCC3B_DRV	ON	OFF	OFF
VCC3SW	3.3V		ON	ON	ON
VCC5M	5V	M_ON	ON	ON	ON
VCC5B	5V	VCC5B_DRV	ON	OFF	OFF
VCC2R5A	2.5V	A_ON	ON	ON	OFF
VCC0R6B	0.6V		ON	ON	OFF
VCC1R2A	1.2V	A_ON	ON	ON	OFF
VCC1R8_SUS	1.8V	SUS_ON1	ON	ON	OFF
VCC1R05_SUS	1.05V	SUS_ON2	ON	ON	OFF
VCCCPUIO	1V	B_ON	ON	OFF	OFF
VCCCPUCORE	0V~1.52V	CPUCORE_ON	ON	OFF	OFF
VCCGFXCORE_I	0V~1.52V	VRON_R	ON	OFF	OFF
VCCSA	0V~1.52V	CPUCORE_ON	ON	OFF	OFF
VCCST	1.05V	A_ON	ON	OFF	OFF
VCCSTG	1.05V	B_ON	ON	OFF	OFF



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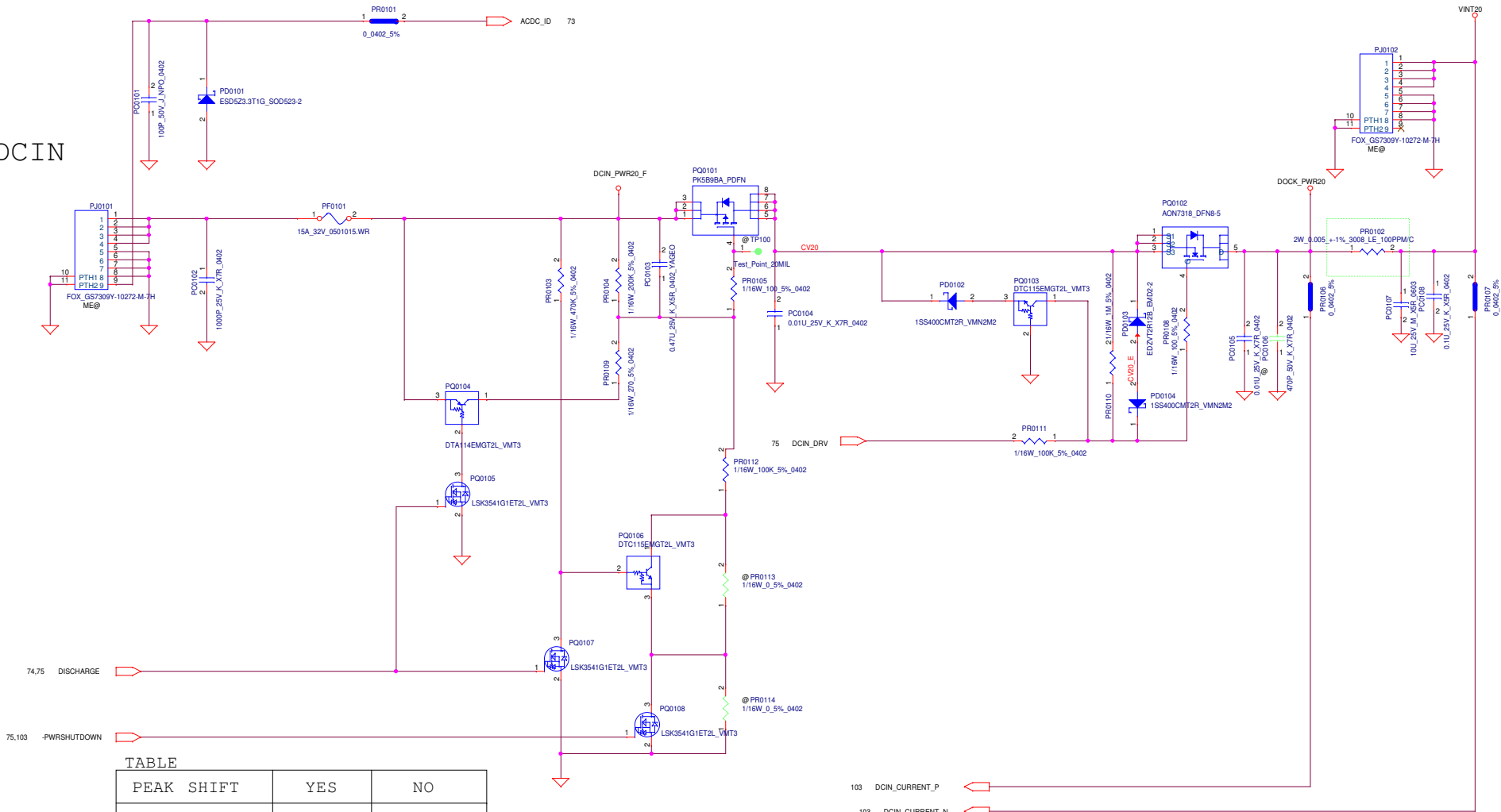
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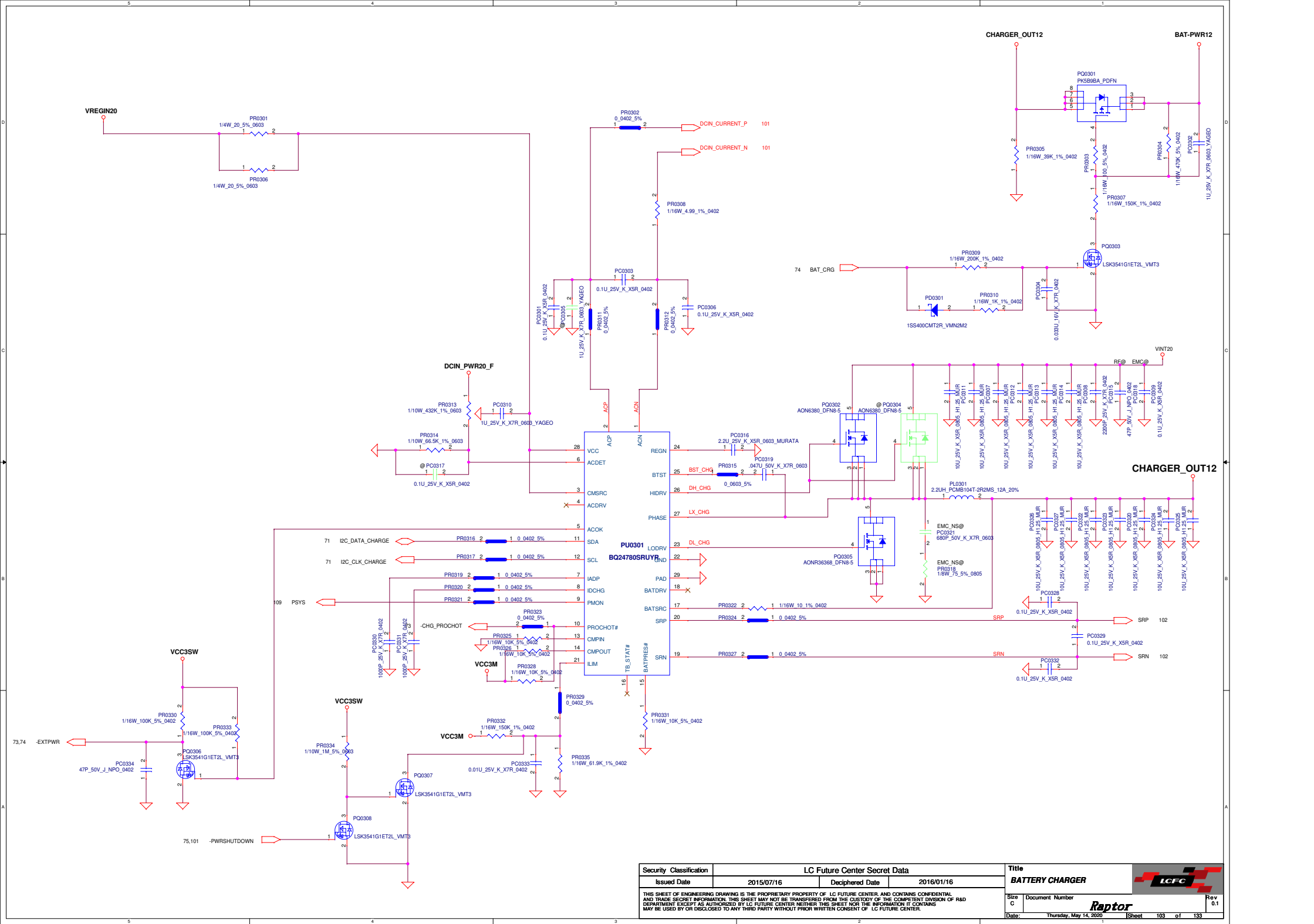
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TABLE


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PR1	ASM	NO-ASM
PQ6	ASM	NO-ASM
PQ7	ASM	NO-ASM

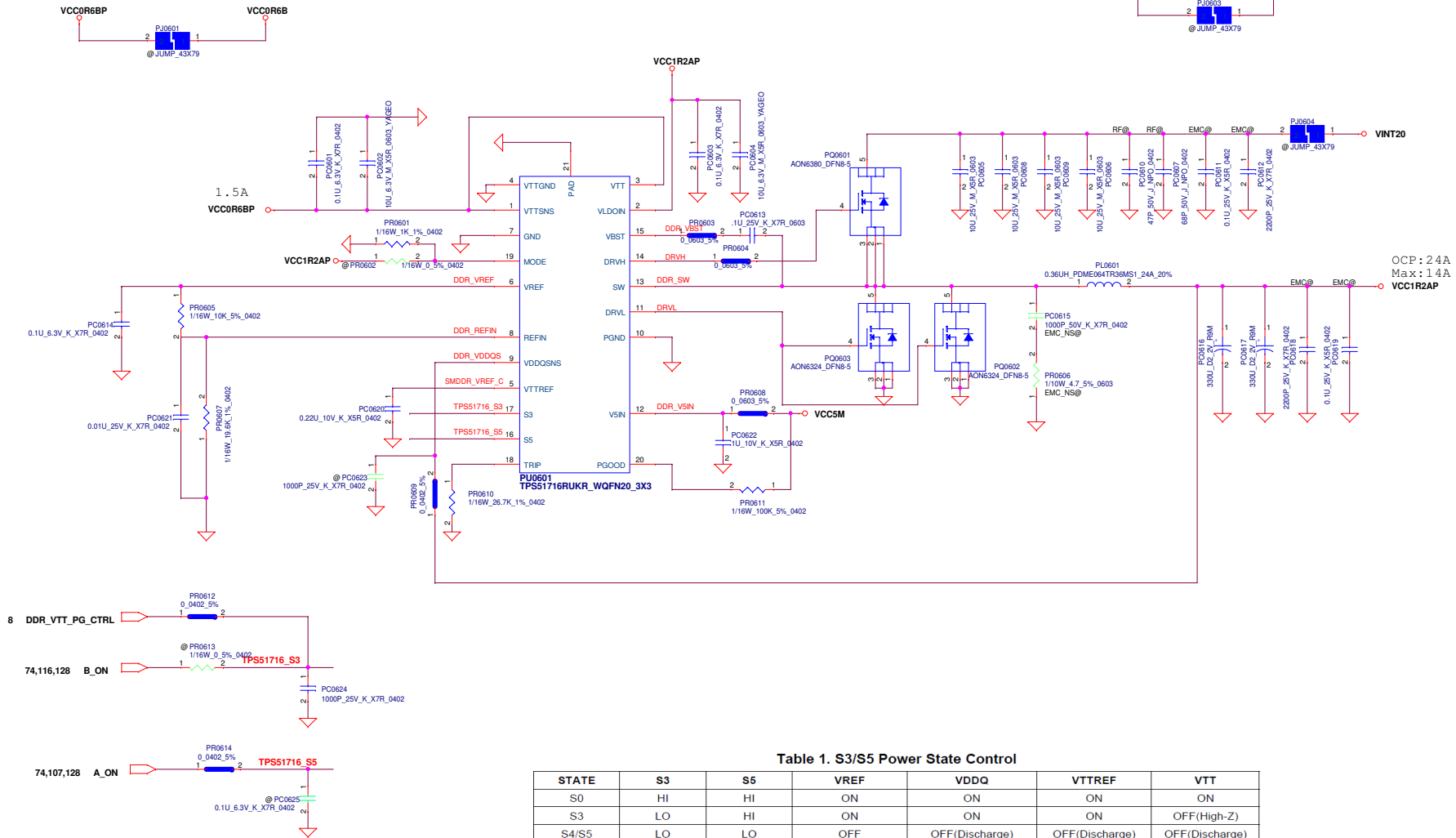
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LOGIC

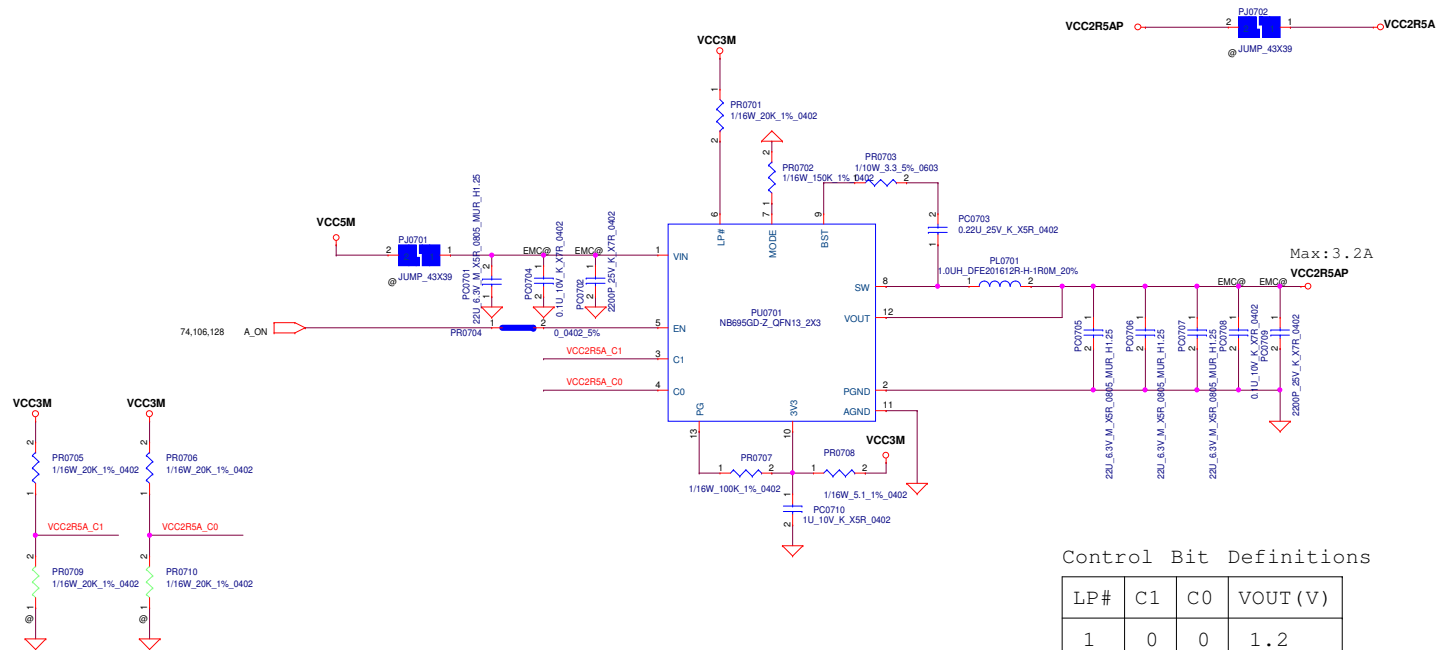


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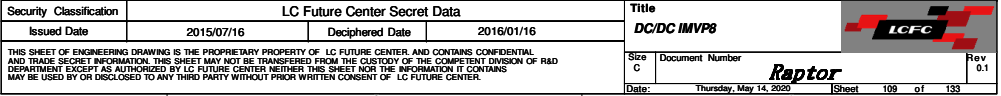
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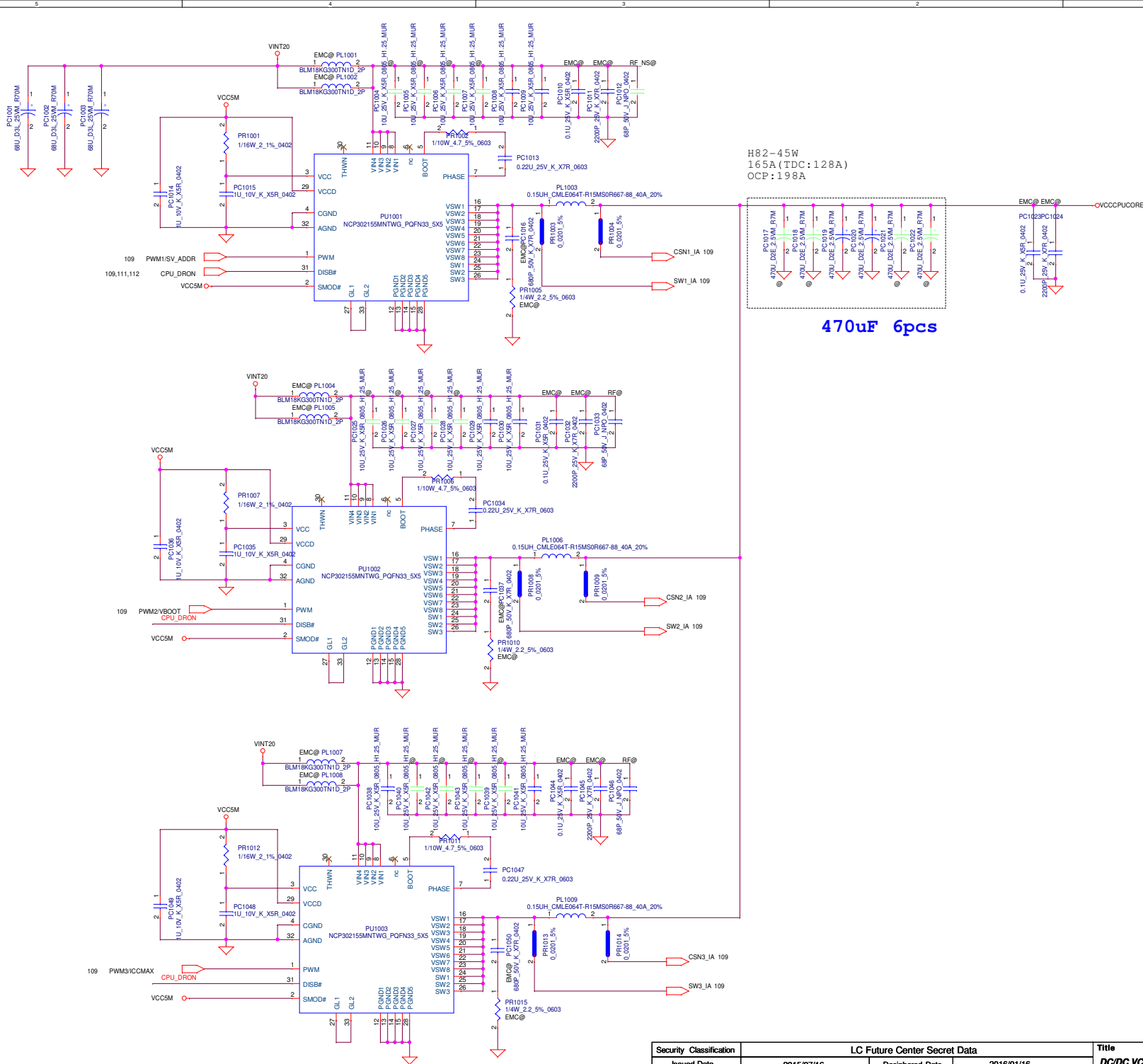
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1	1	0	1.8
1	1	1	2.5



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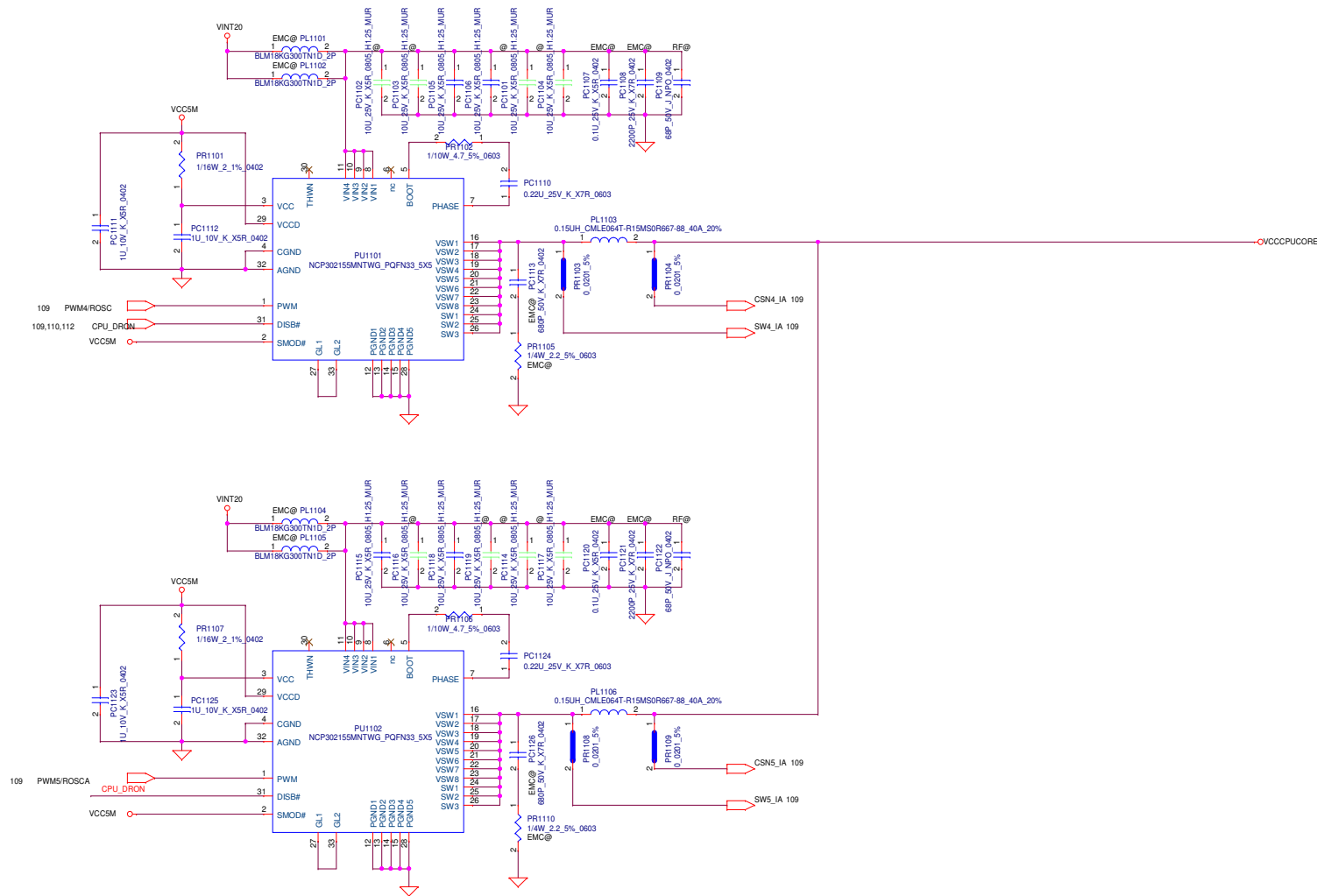
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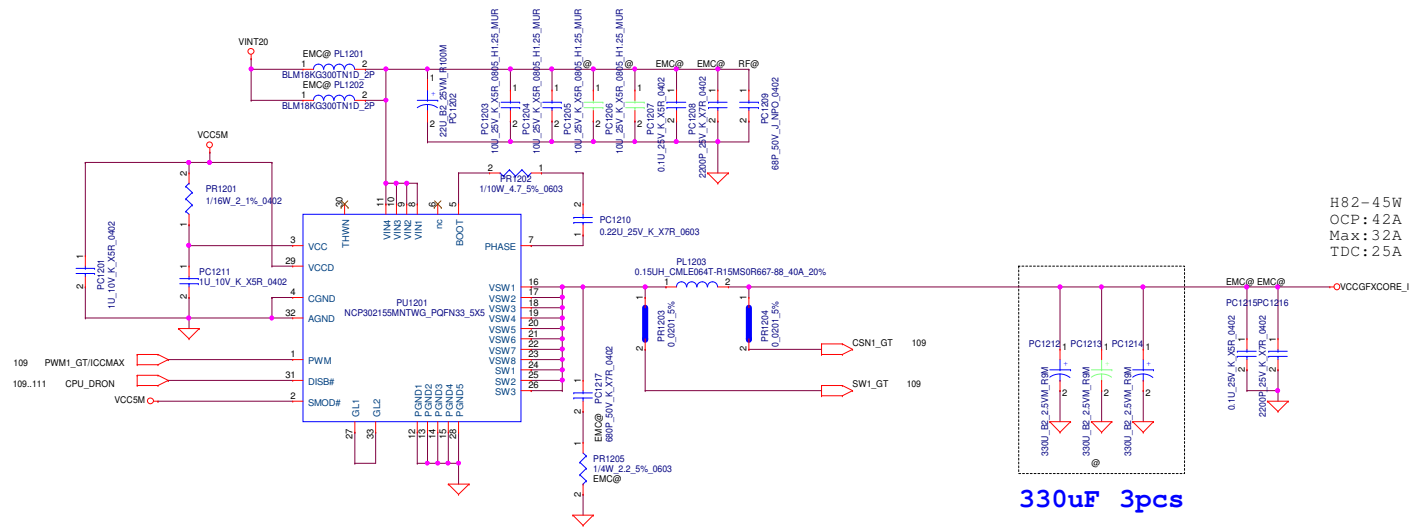


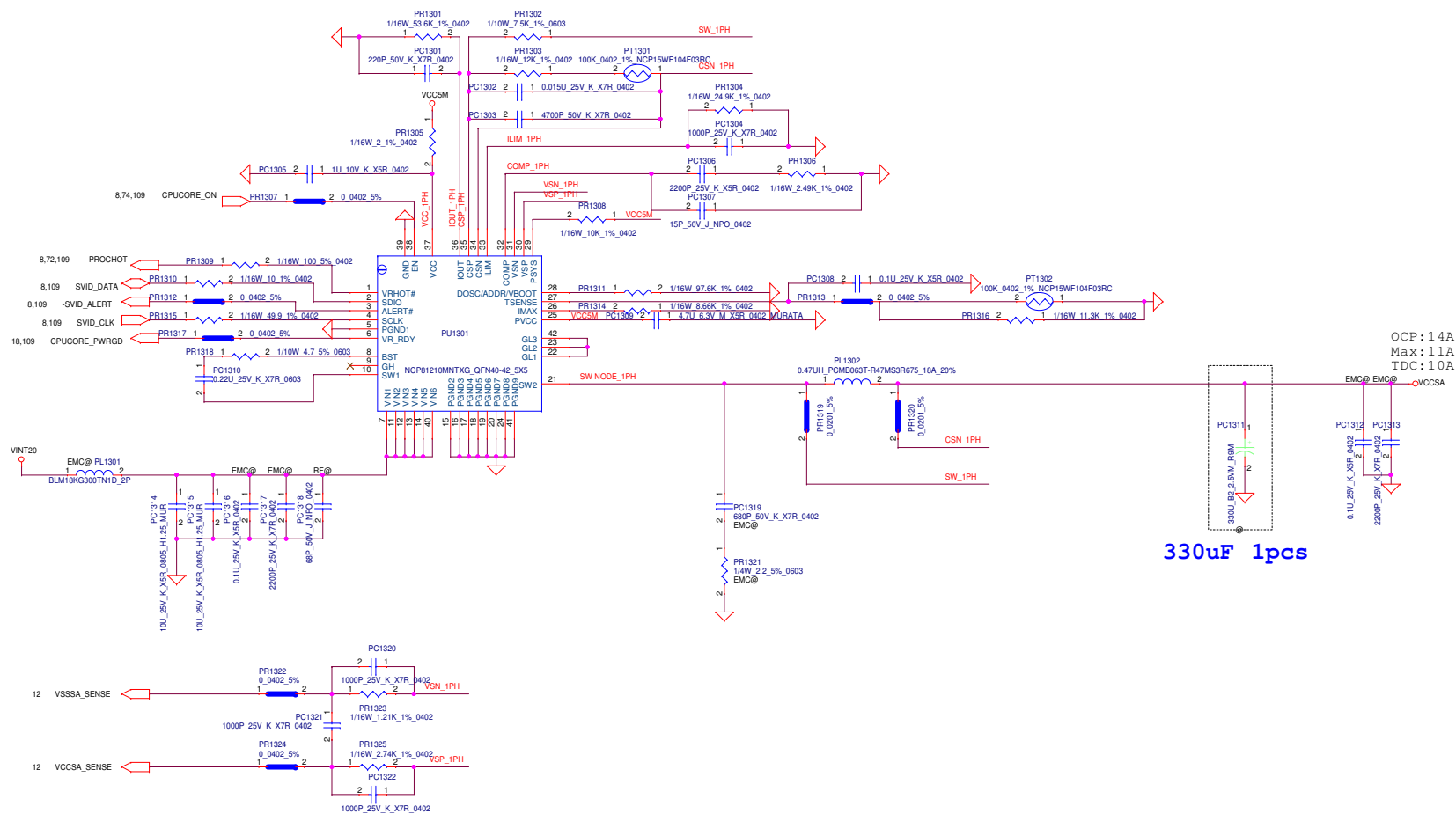


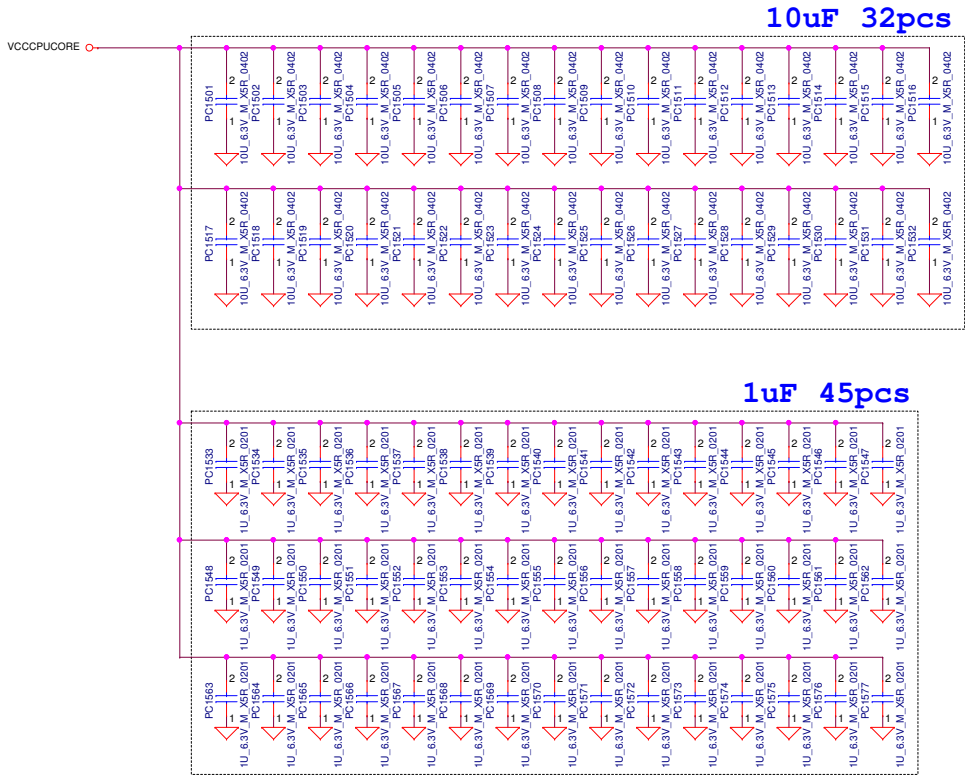
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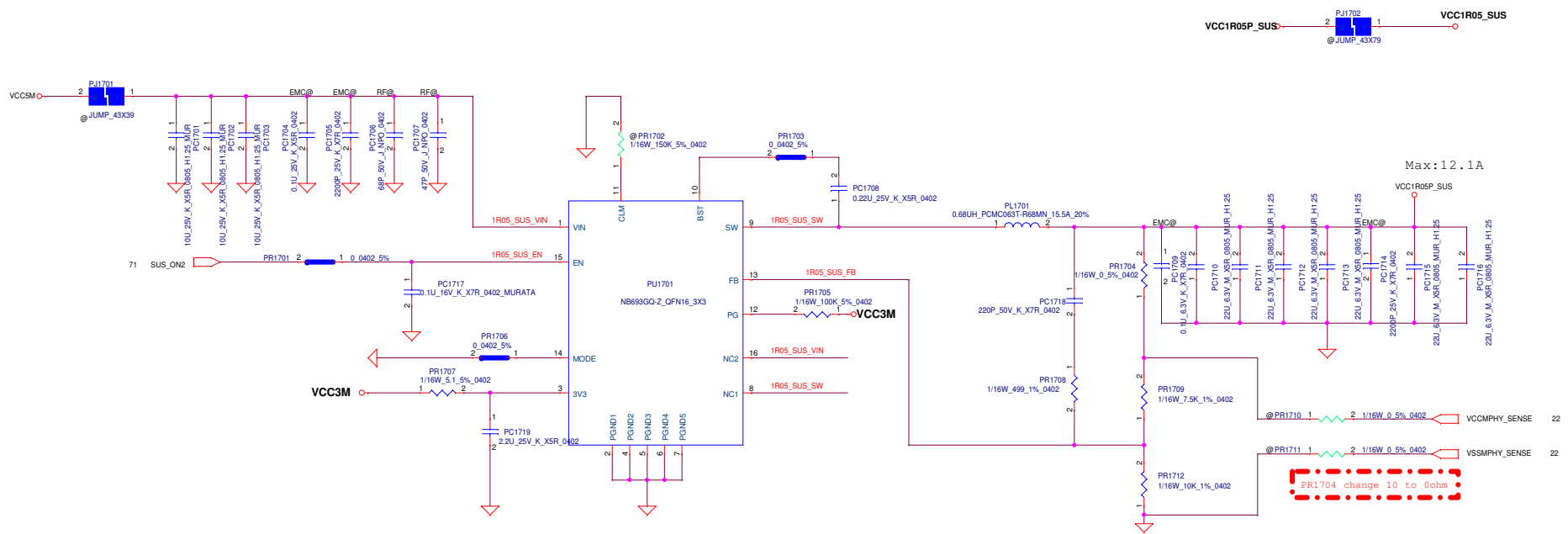








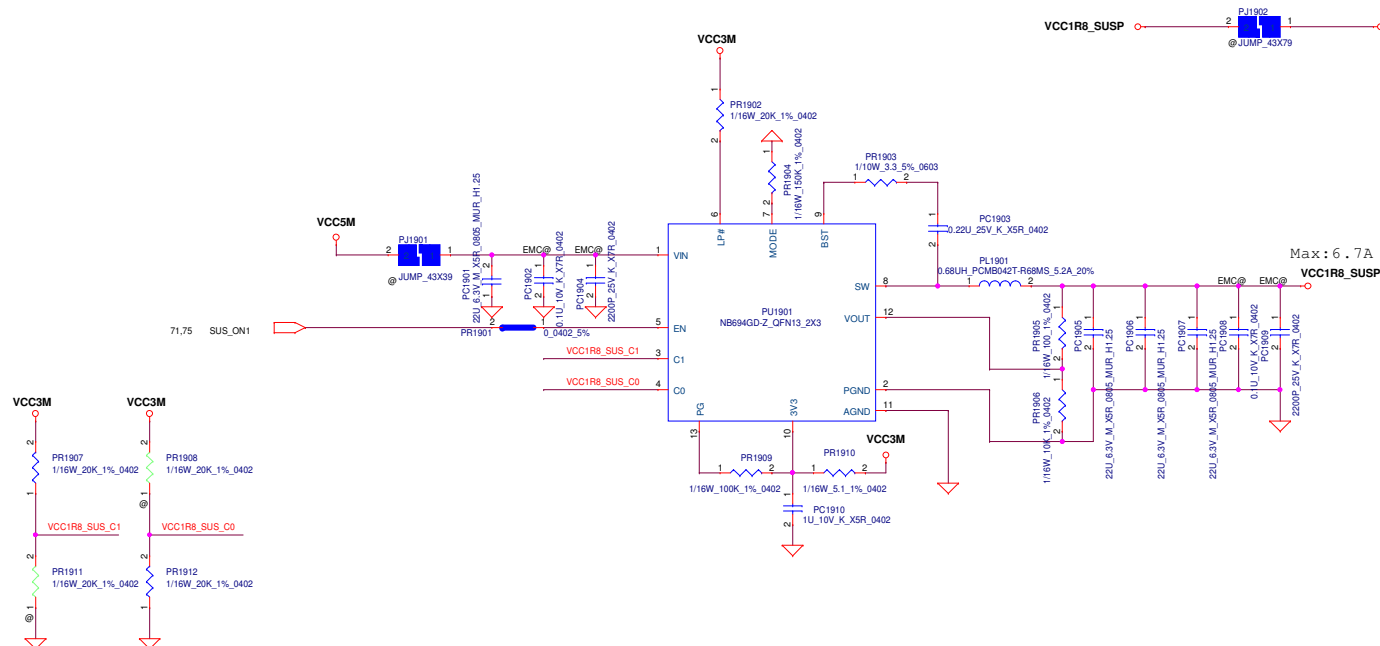
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Control Bit Definitions

LP#	C1	C0	VOUT(V)
1	0	0	1.2
1	0	1	1.5
1	1	0	1.8
1	1	1	2.5


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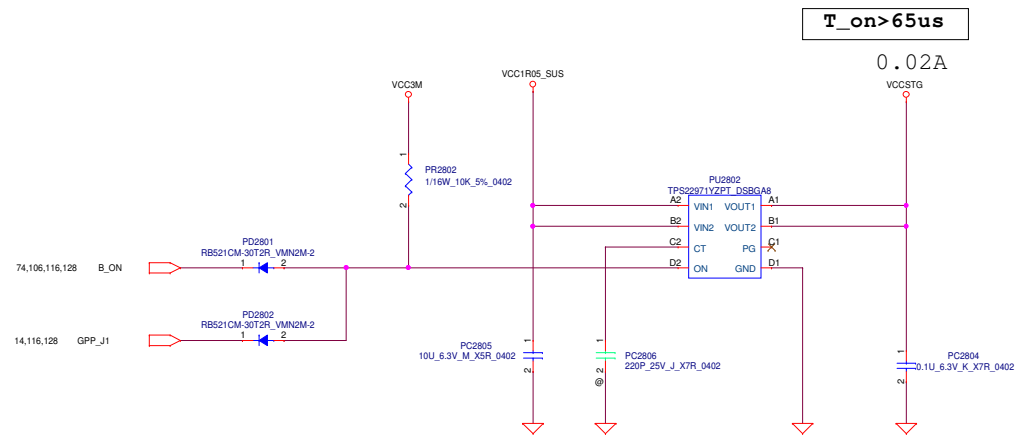
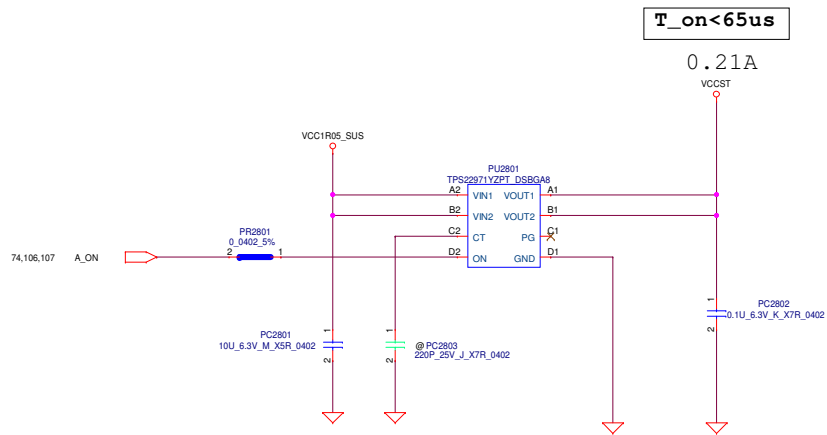
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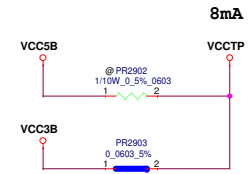
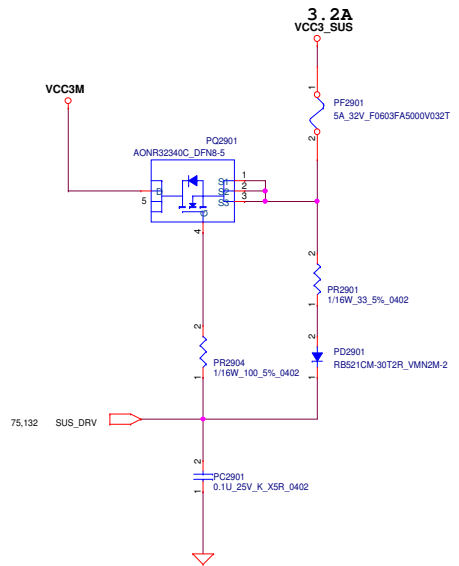


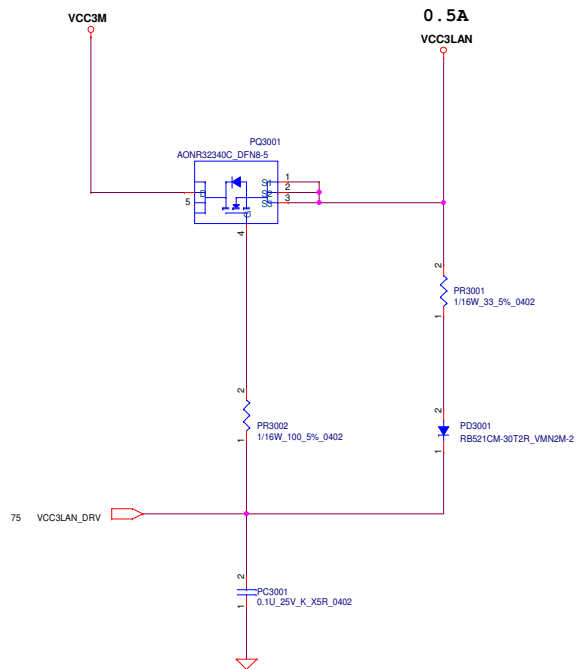
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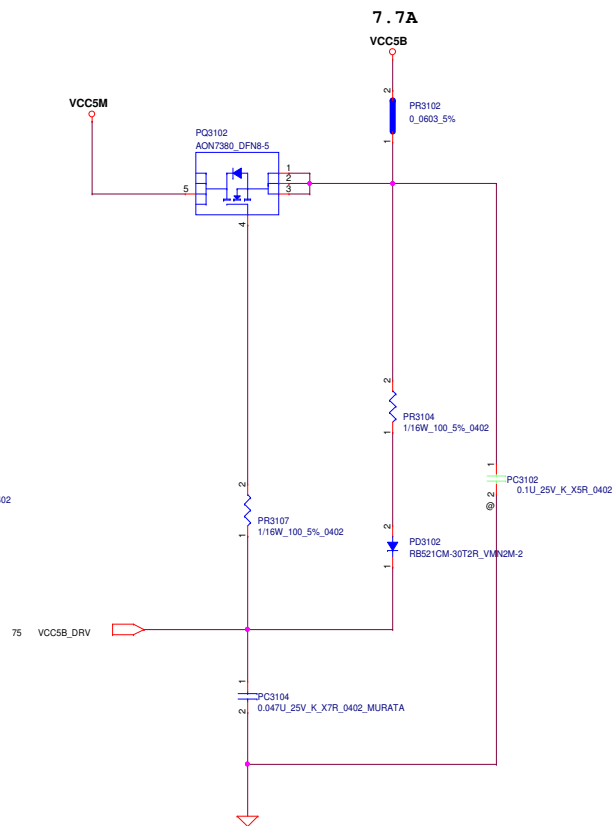
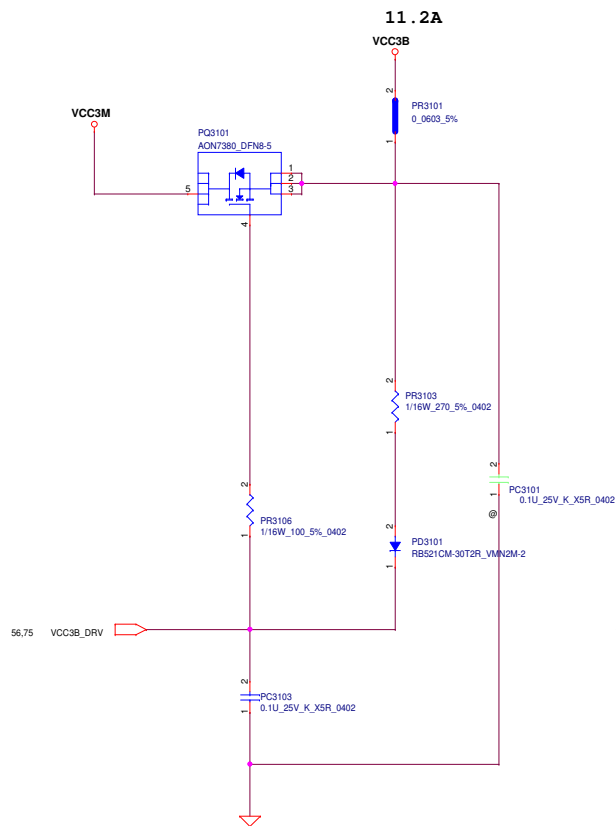


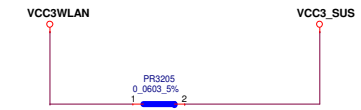
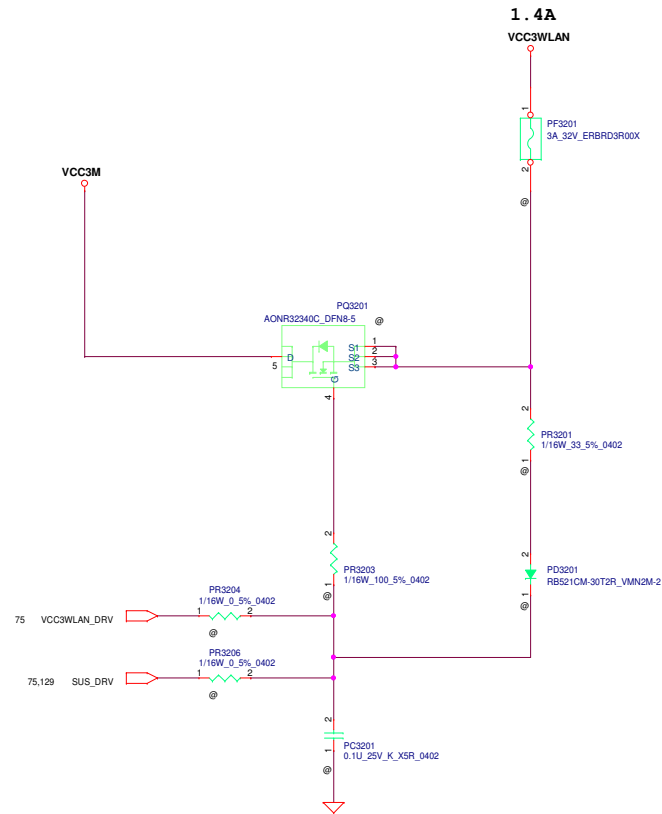


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