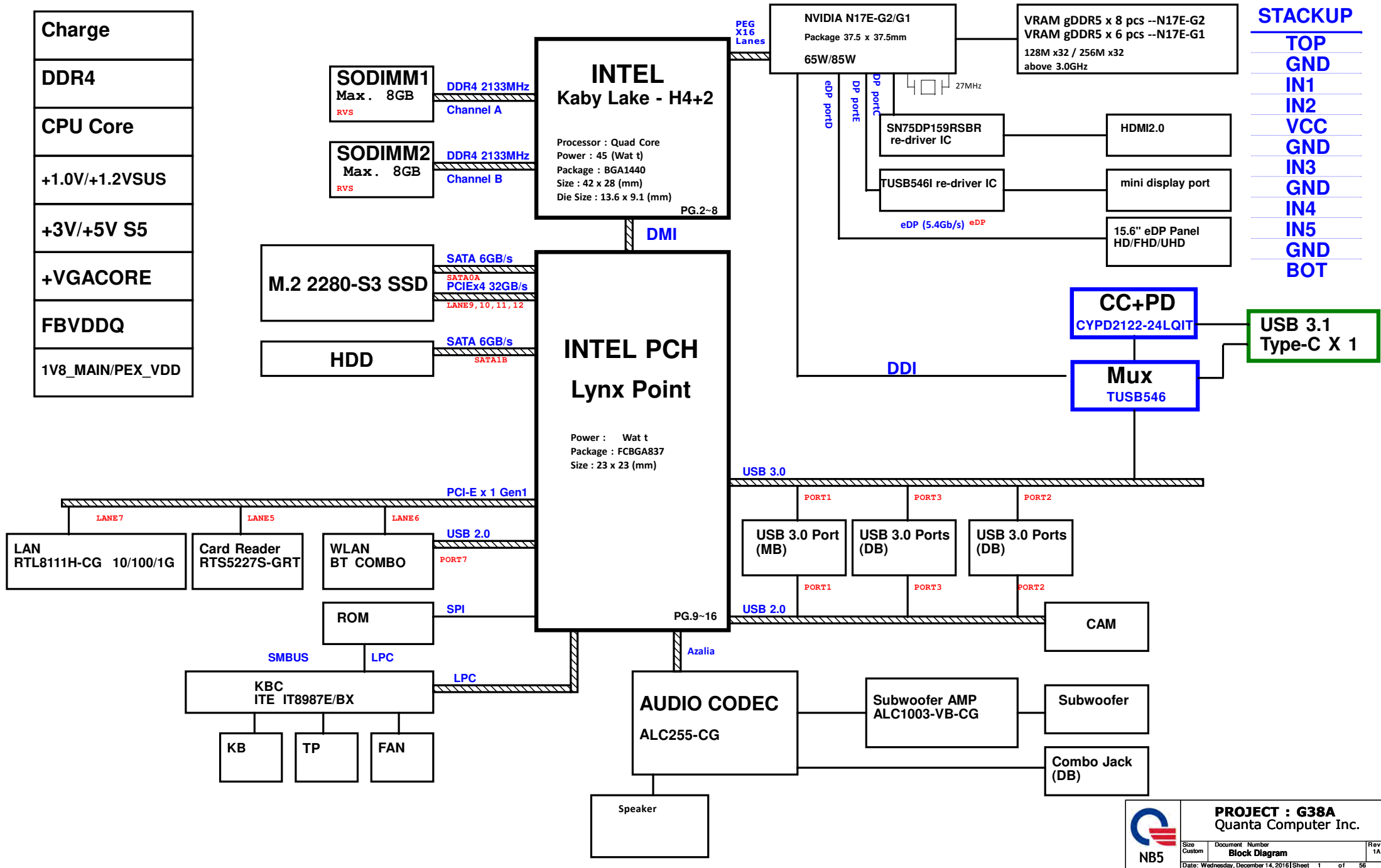


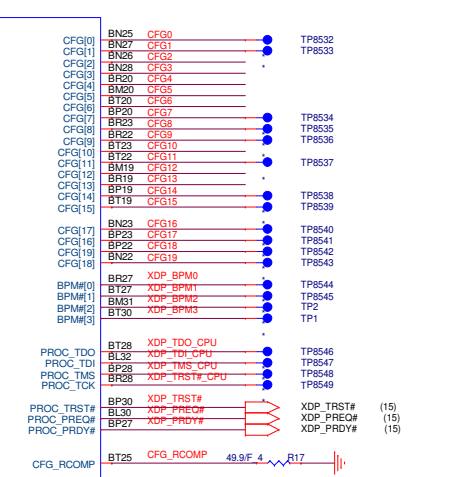
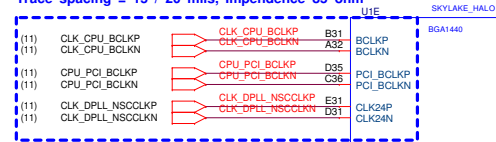
# NL5/NL5A N17E-G1/G2 INTEL KABY -H SYSTEM DIAGRAM

01

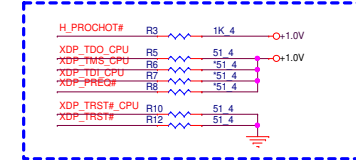


## SKYLAKE Processor (CLK, MISC, JTAG)

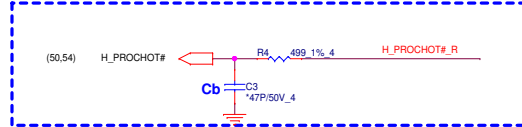
Host CLK:  
Trace length < 11000 mils  
Trace spacing = 15 / 20 mils, Impedance 85 ohm



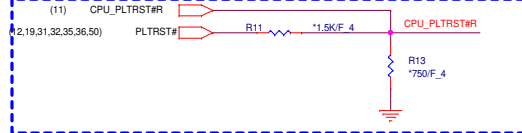
## Processor pull-up (CPU)



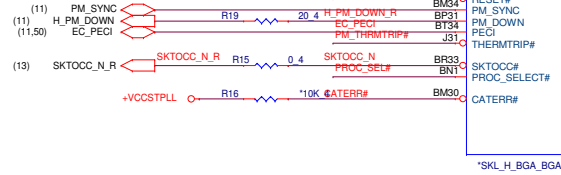
PROCHOT# (50ohm)  
Trace Length <11 inches  
Cb need placement near VR



CPU\_PLTRST# (50ohm)  
Trace Length: 10~17 inches



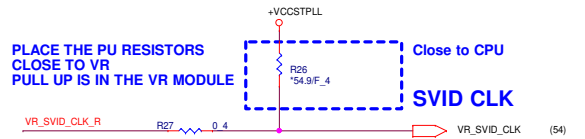
PM\_SYNC (50ohm)  
Trace Length: 1~11.25 inches



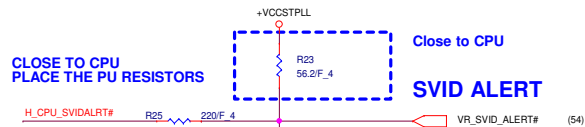
## CPU CORE SVID

Layout note:  
1. Need routing together  
2. ALERT need between CLK and DATA.

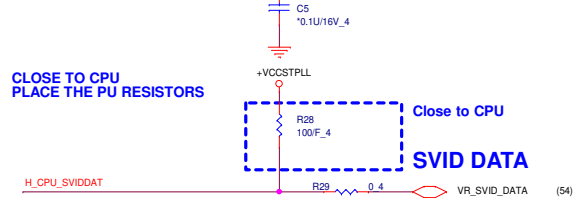
PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE



CLOSE TO CPU  
PLACE THE PU RESISTORS



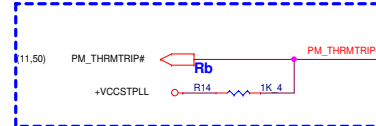
CLOSE TO CPU  
PLACE THE PU RESISTORS



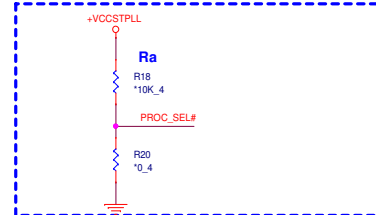
PROCPWRGD (50ohm)  
Trace Length: 1~11.25 inches



THERMTRIP# (50ohm)  
Trace Length: 1.1~12 inches  
Rb need placement near PCH

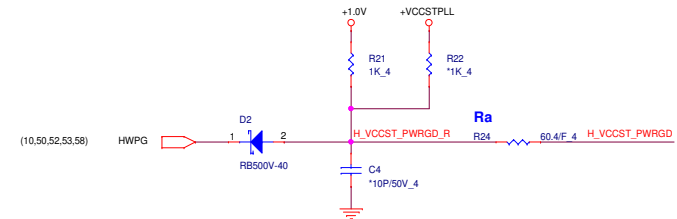


Ra(R18) Not install in SKL-H



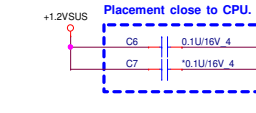
## HWPD

Ra close to CPU side  
H\_VCCST\_PWRGD trace 0.3" - 1.5"



## CPU VDDQ

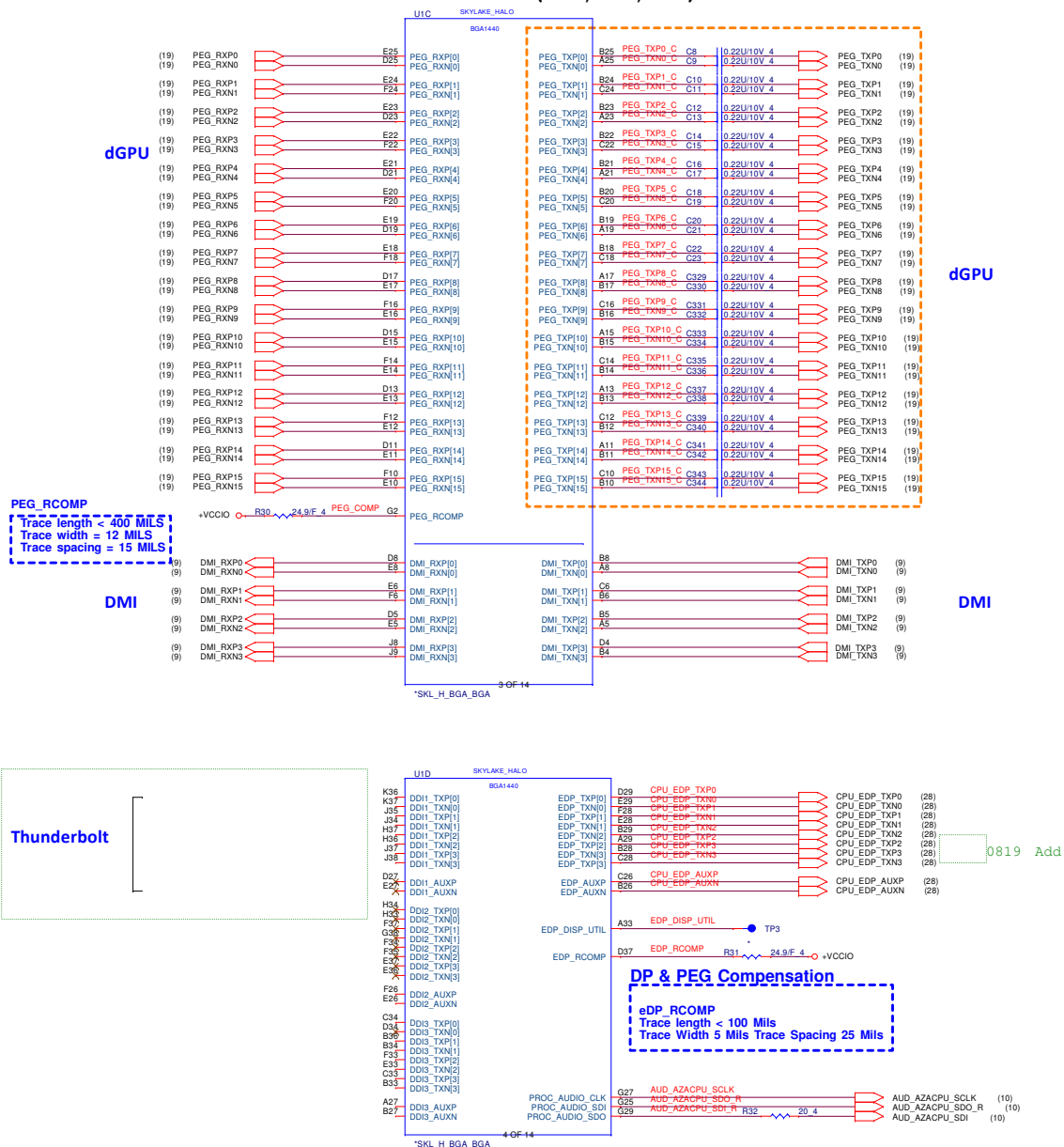
Note: please keep plane is enough for VDDQ 2.8A



**PROJECT : G38A**  
Quanta Computer Inc.

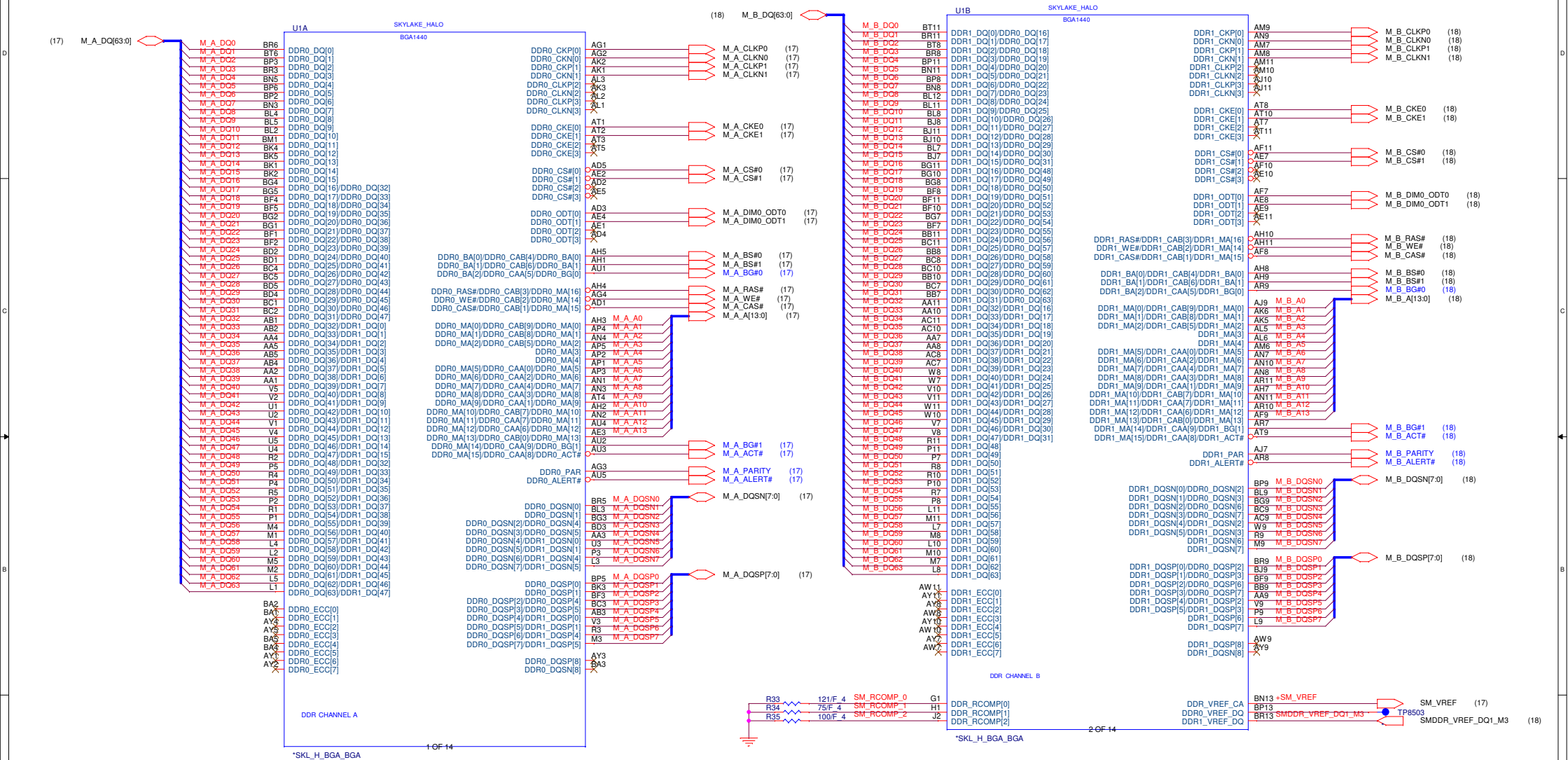
Size Custom Document Number SKL 1/7 (JTAG/MISC) Rev 1A  
Date: Wednesday, December 14, 2016 Sheet 2 of 56

## SKYLAKE Processor (DMI, PEG, FDI)




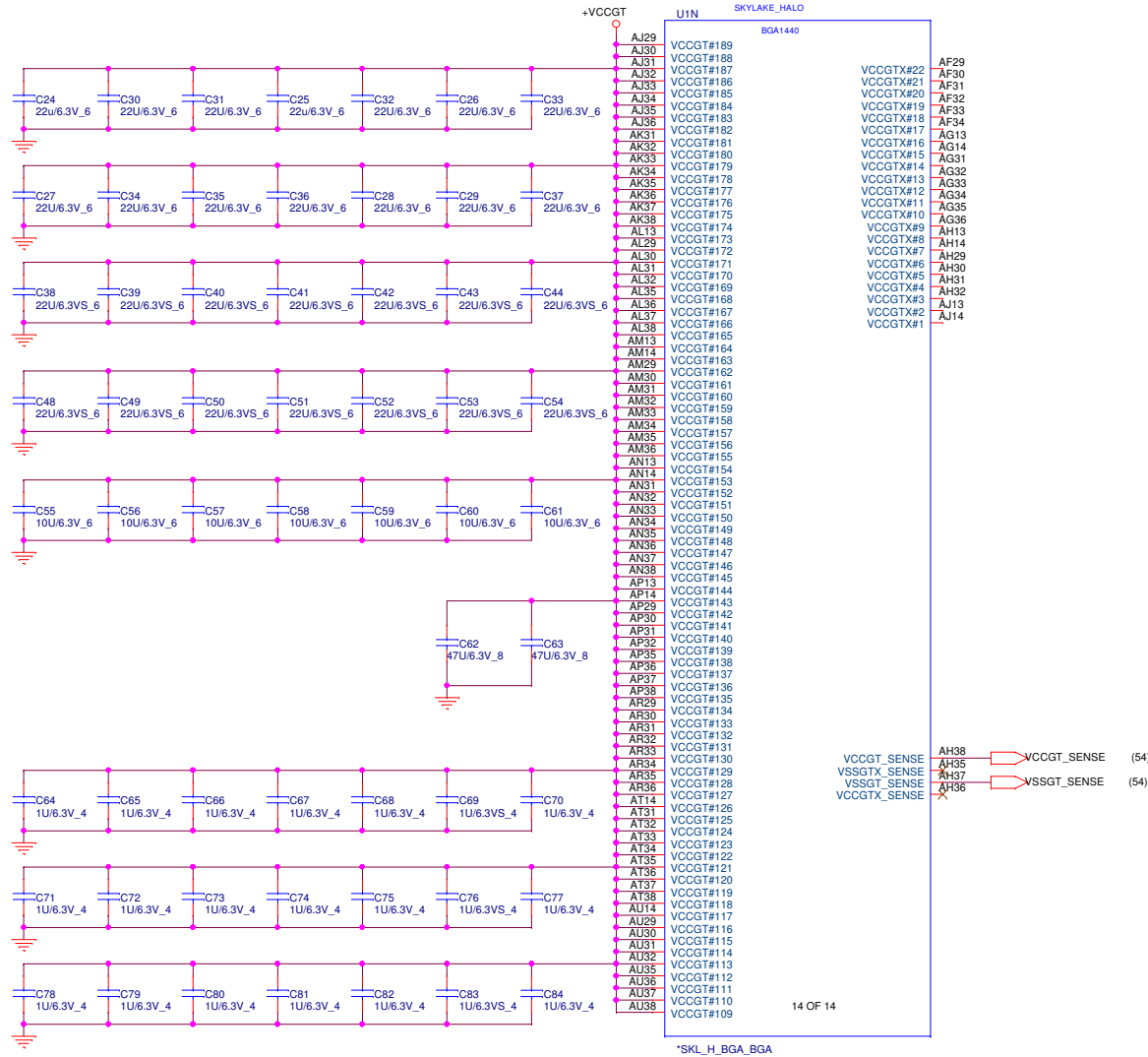
+1.2VSUS (2,6,10,17,18,53,59,64)  
+3VSS (10,12,14,16,29,30,33,35,36,37)  
+3V (9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,35)

## SKYLAKE Processor (DDR4)



## SKYLAKE Processor (POWER)

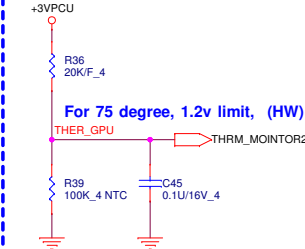
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

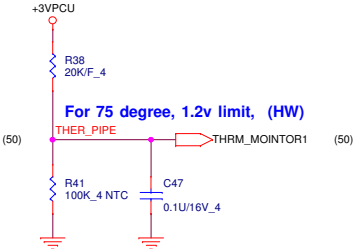
## IO Thrm Protect

Location need thermal confirm

## For GPU USE



## For CPU USE




0801 Del CPU thermal IC

## CPU Thermal Sensor

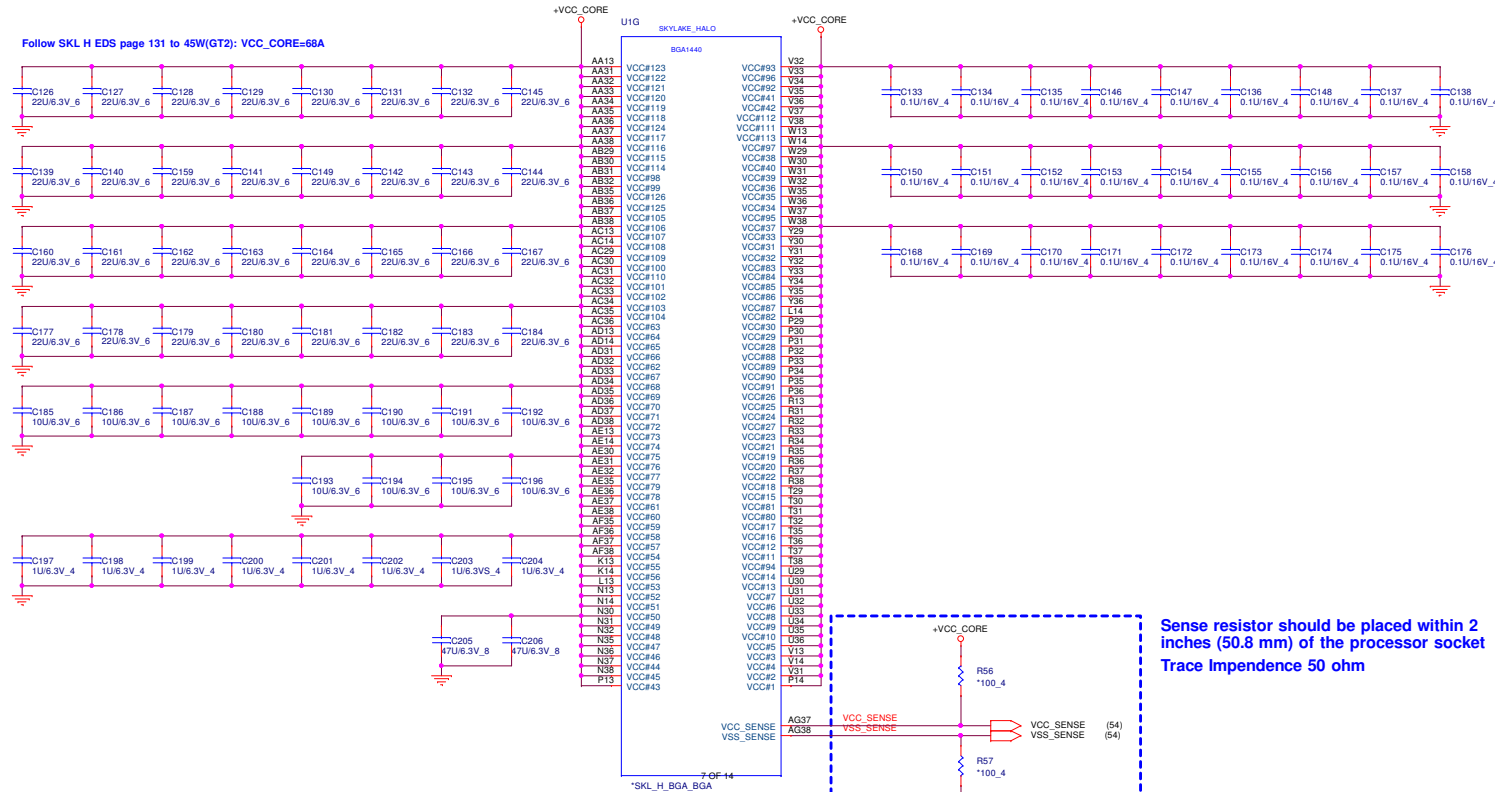
Location need thermal confirm

0801 Del GPU thermal IC

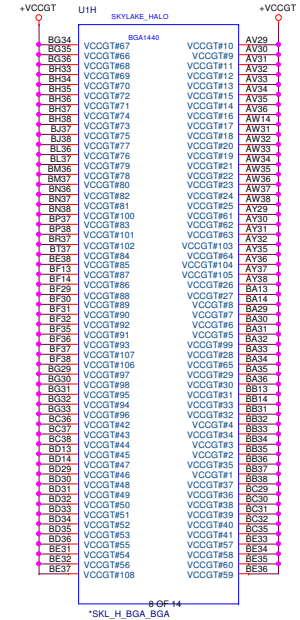
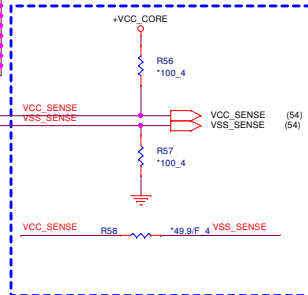
## GPU Thermal Sensor

	<b>PROJECT : G38A</b> Quanta Computer Inc.		
	Size Custom	Document Number SKL 5/7 (POWER&GND)	Rev 1A
Date: Wednesday, December 14, 2016 Sheet 6 of 56			

Follow SKL H EDS page 131 to 45W(GT2): VCC\_CORE=68A



Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket  
Trace Impedance 50 ohm



+VCC\_CORE (54,55)

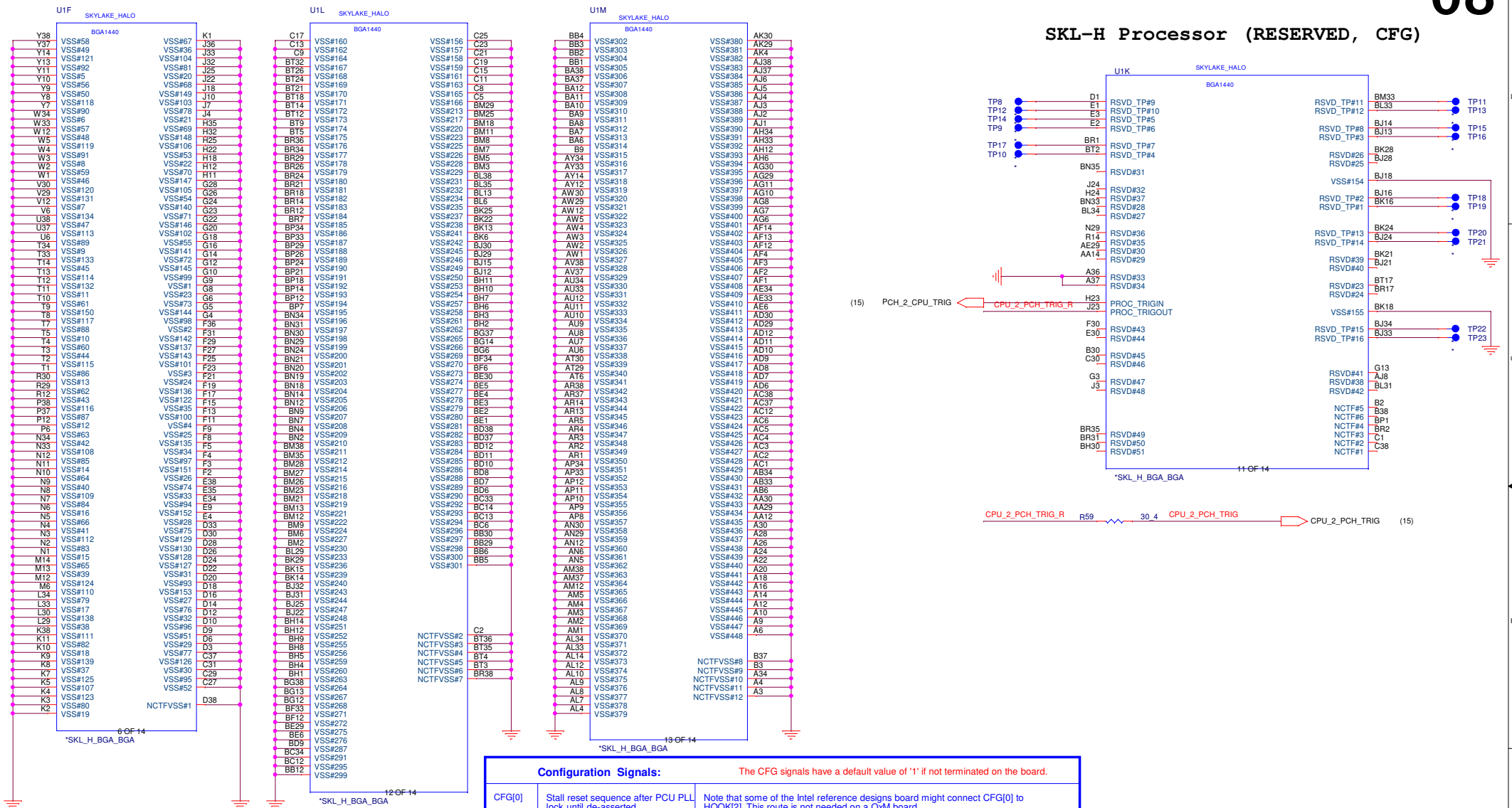


**PROJECT : G38A**  
**Quanta Computer Inc.**

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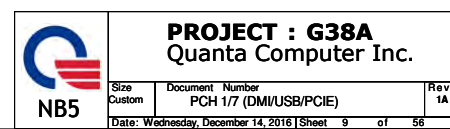


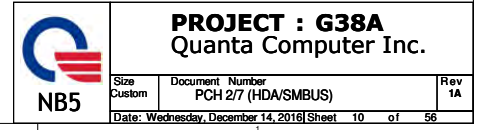
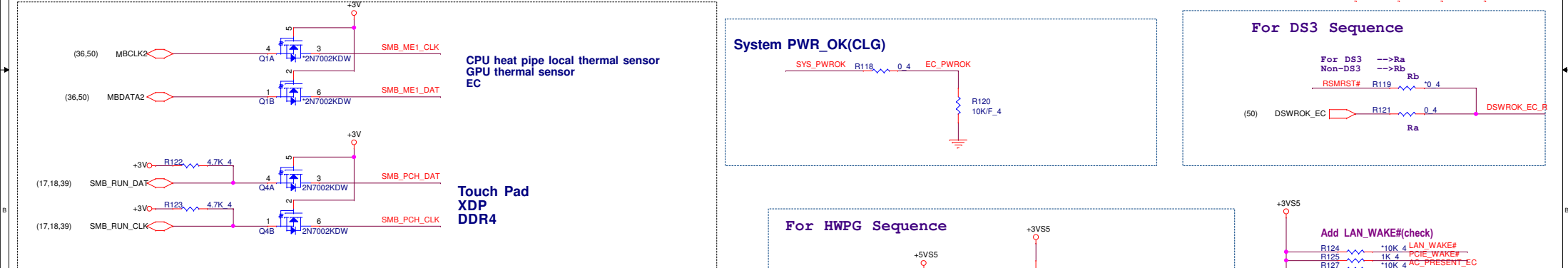
## SKL-HPprocessor (GND)



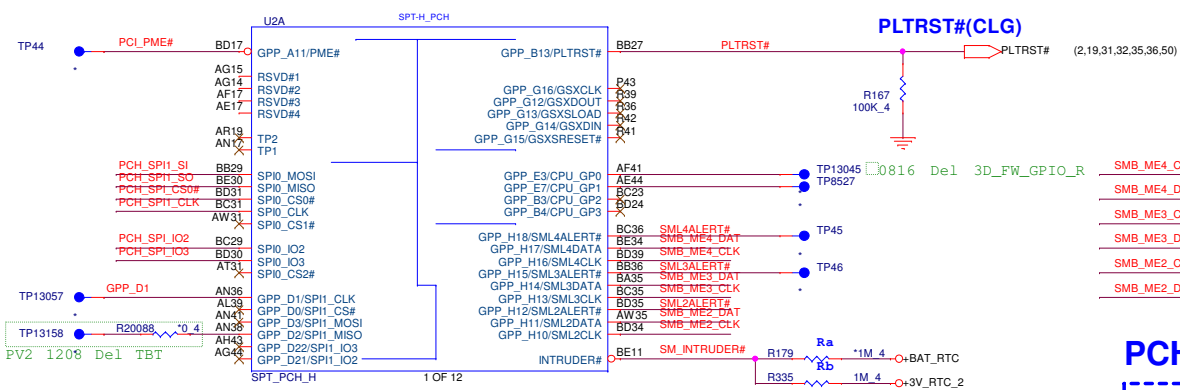
Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a OSM board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS fro training	



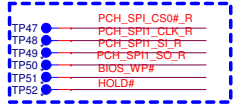




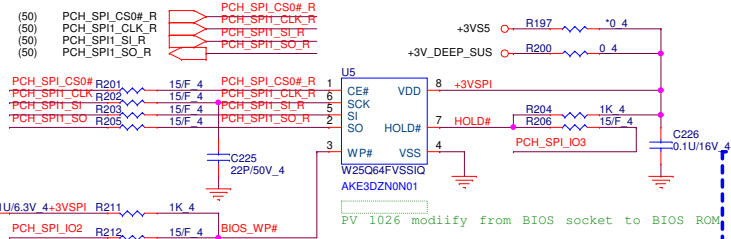




### PCH SPI ROM(CLG)



### Place to TOP



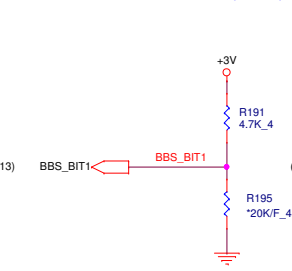
Vender	Size	P/N
Winbond	16MB	AKE3DZN0N01 - IC FLASH(8P) W25Q128FVSIQ(SOIC)
GGD	16MB	AKE3DF00Q00 - IC FLASH(8P)GD25B128CSIGR(SOP)
Socket		DFHS08FS023

0803 Change BIOS ROM size from 8MB to 16MB

### NO REBOOT IF SAMPLED HIGH

HIGH:TOP SWAP ENABLED(CRB)

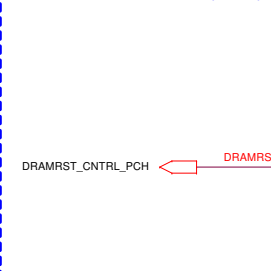
LOW: Disable "No Reboot" mode. (Default)



### ESPI/LPC SELECT STRAP

HIGH:ESPI is selected for EC.

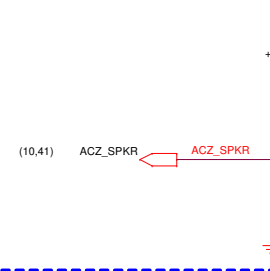
LOW:LPC is selected for EC. (Default)



### TOP SWAP OVERRIDE STRAP

HIGH:TOP SWAP ENABLED(CRB)

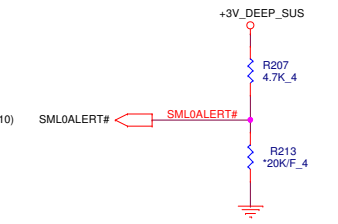
LOW:TOP SWAP DISABLED(DEFAULT)



### TLS CONFIDENTIALITY ENABLED

HIGH:T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)

LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)



### RESERVED

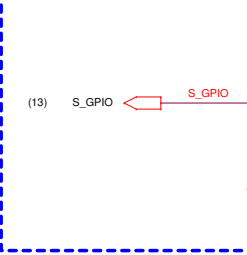
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.



### BOOT SELECT STRAP

HIGH:LPC

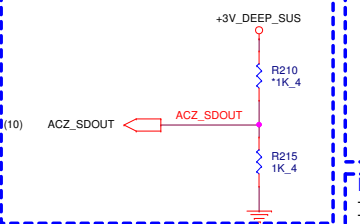
LOW: SPI. (Default)



### TLS CONFIDENTIALITY ENABLED

HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.(CRB)

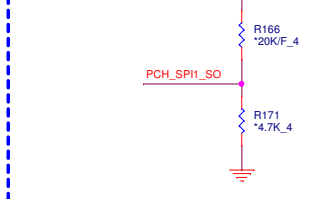
LOW: security measures defined in the Flash Descriptor. (Default)



### PCH Strap Pin

#### RESERVED

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



#### ESPI FLASH SHARING MODE

HIGH:SLAVE ATTACHEHD FLASH SHARING

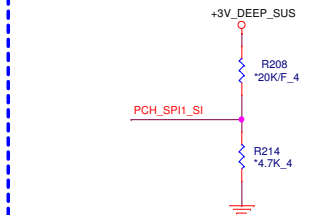
LOW: 0: MASTER ATTACHED FLASH SHARING

This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

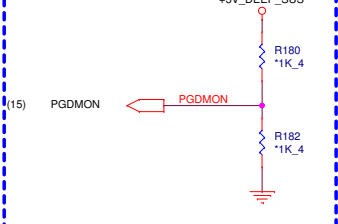


#### RESERVED

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

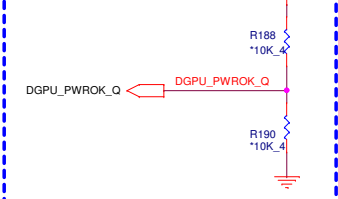


#### DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW



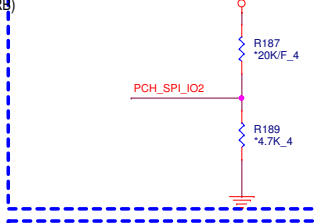
#### DFX TEST MODE

XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



#### RESERVED

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



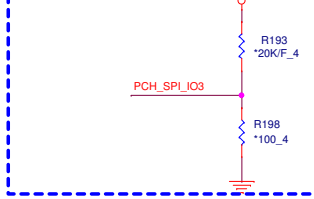
#### RING OSCILLATOR BYPASS

DGPU\_HOLD\_RST#



#### RESERVED

This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



#### XTAL INPUT FREQUENCY[0]

GPU\_EVENT#



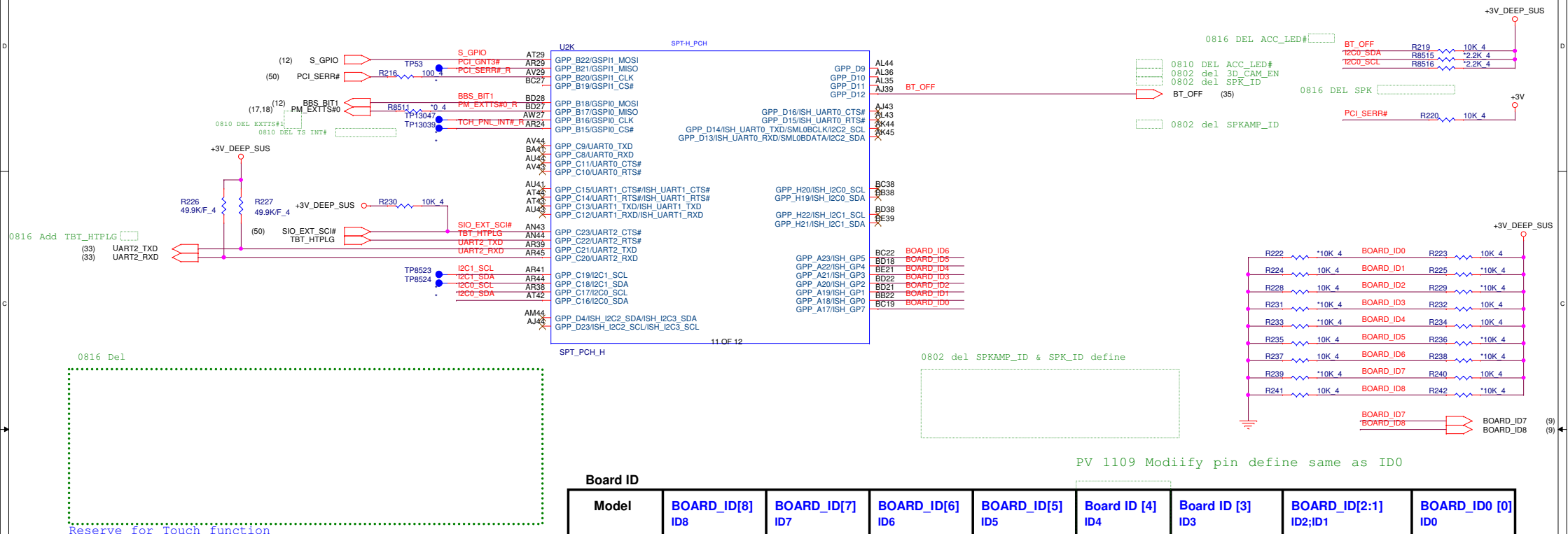
#### XTAL INPUT FREQUENCY[1]

DGPU\_PWR\_EN

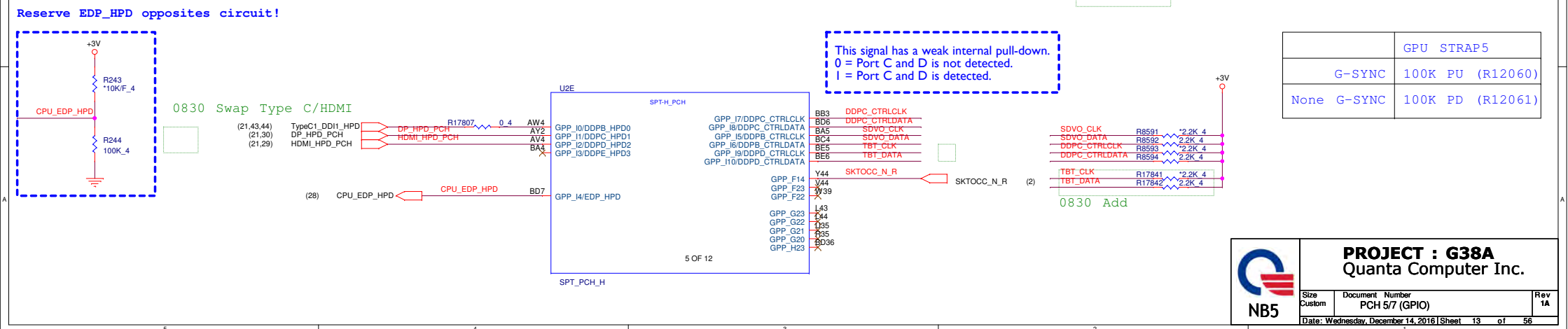


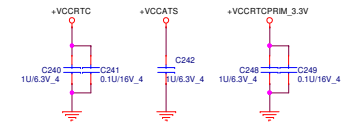
PROJECT : G38A  
Quanta Computer Inc.

Size	Document Number	Rev
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Board ID								
Model	BOARD_ID[8] ID8	BOARD_ID[7] ID7	BOARD_ID[6] ID6	BOARD_ID[5] ID5	Board ID [4] ID4	Board ID [3] ID3	BOARD_ID[2:1] ID2;ID1	BOARD_ID0 [0] ID0
Definition	0 : Reserve	0 : old HDD port (SATA1B)  1: New HDD port (SATA16)	0 : Normal CAM 1 : IR CAM	0 : Normal type C 1 : Intel TBT	0 : White KB 1 : RGB KB	0 : w/o subwoofer 1 : with subwoofer	00 : N17E-G2 (230W) 01 : N17E-G1 (200W) 10 : N17P-G1 (150W) 11 : N17P-G0 (150W)	0 : NL 5 1 : NL 5 A

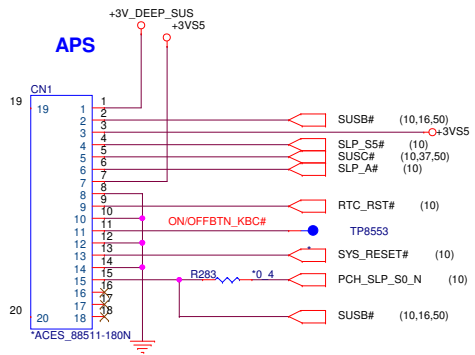




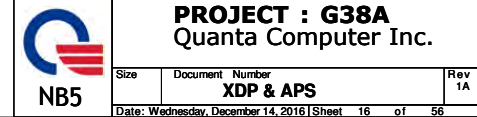
(9,10,12,13,16) +3V\_DEEP\_SUS 

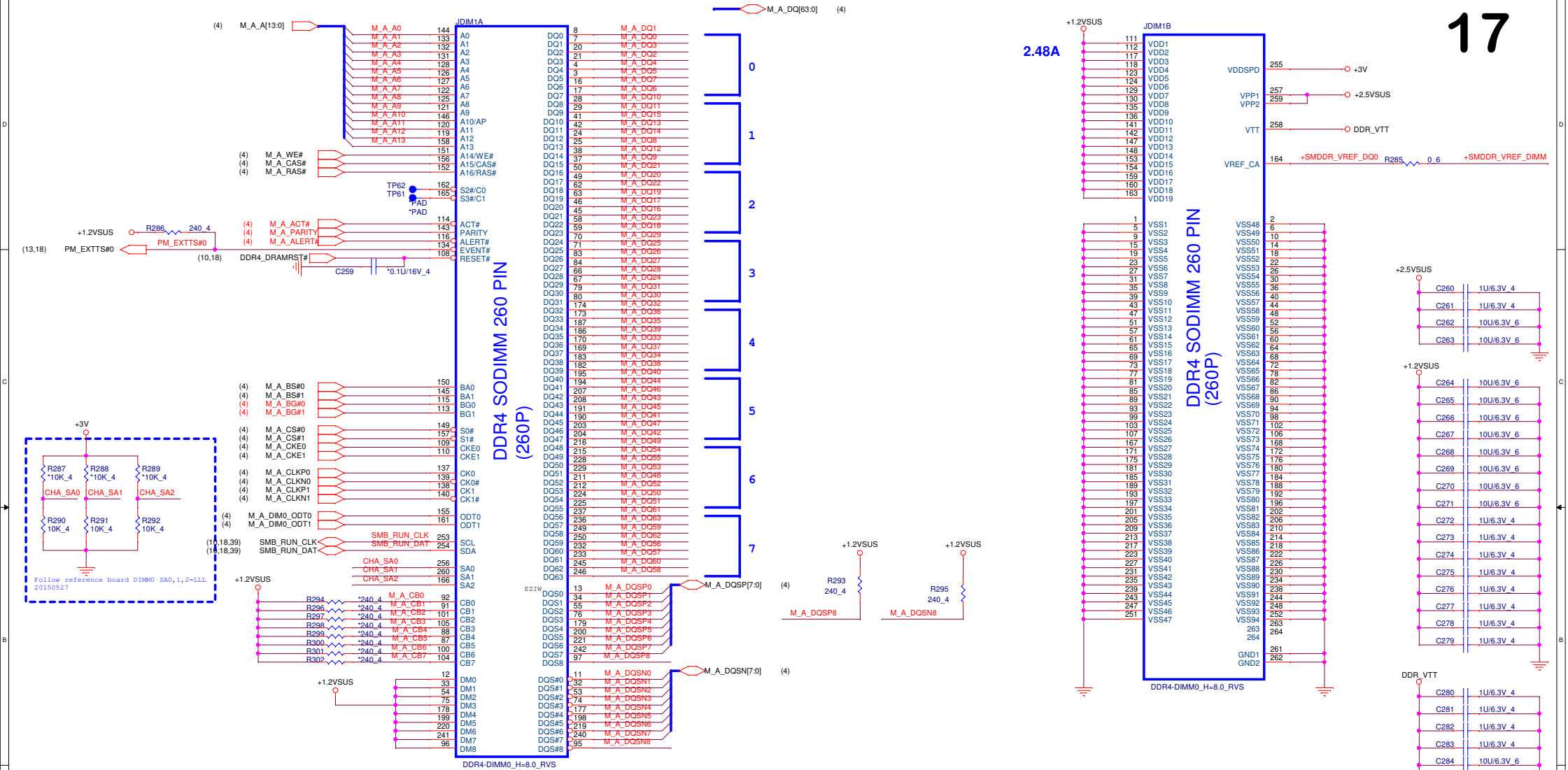


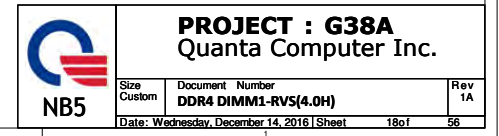


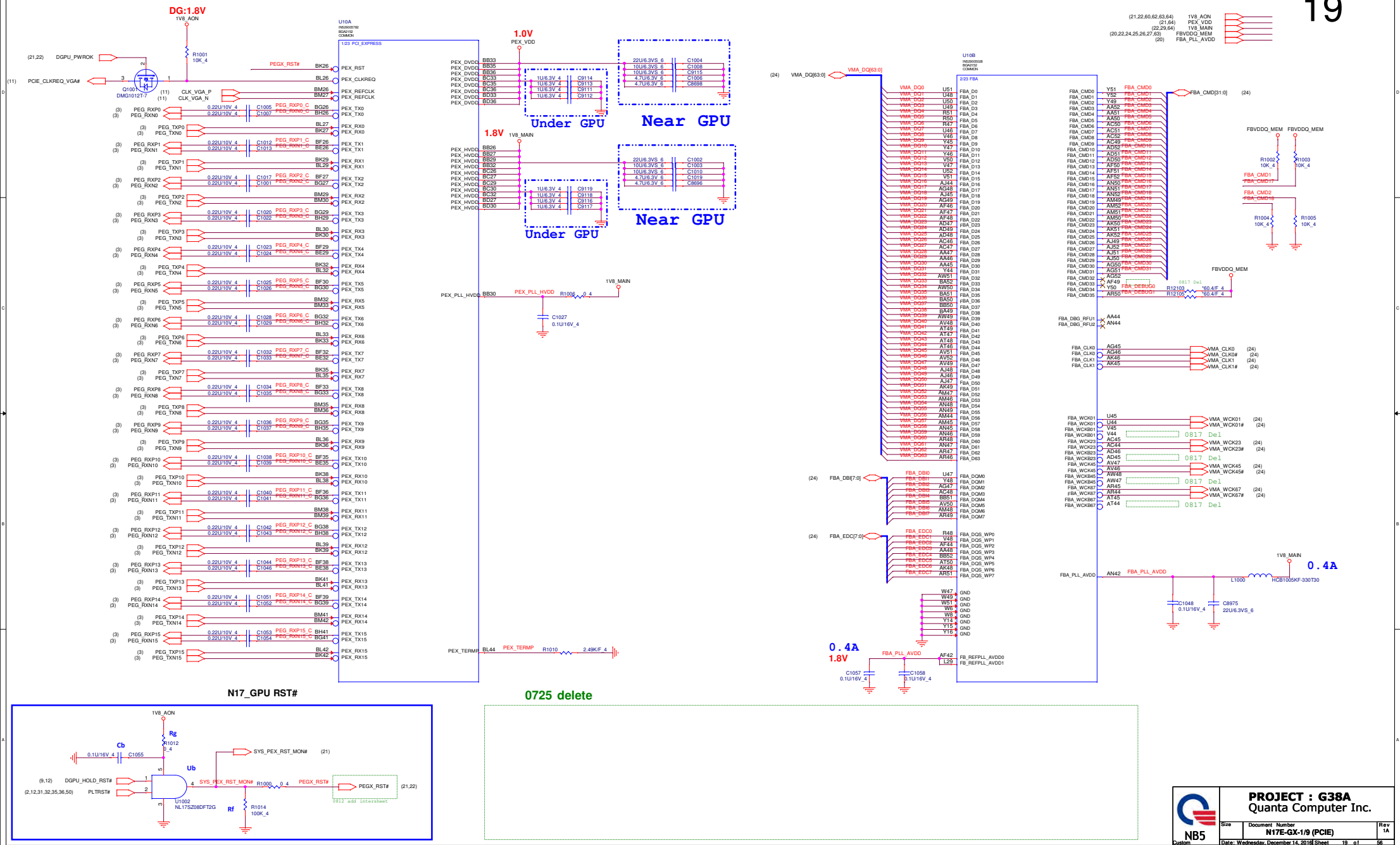


(9,10,12,13,14) +3V\_DEEP\_SUS 



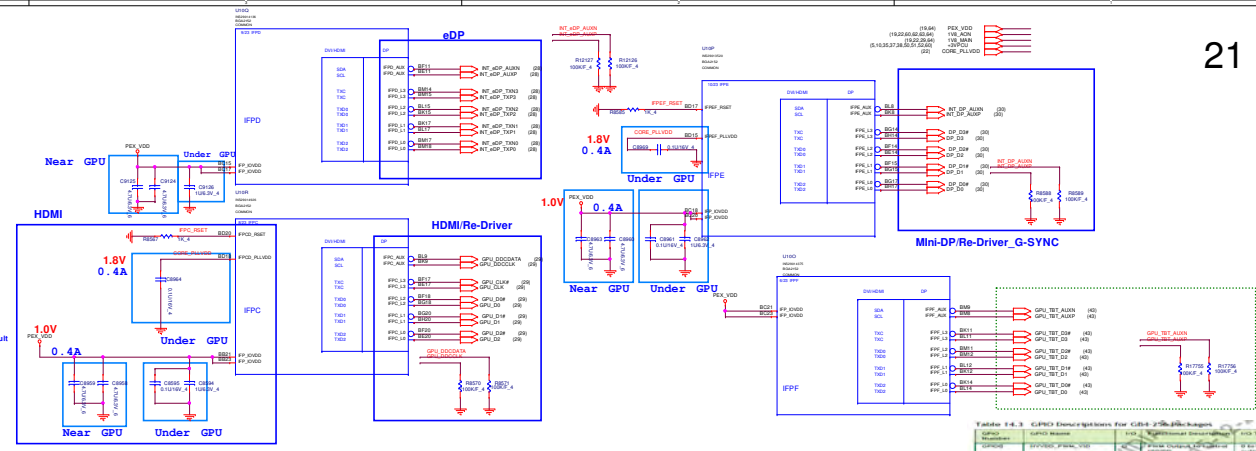




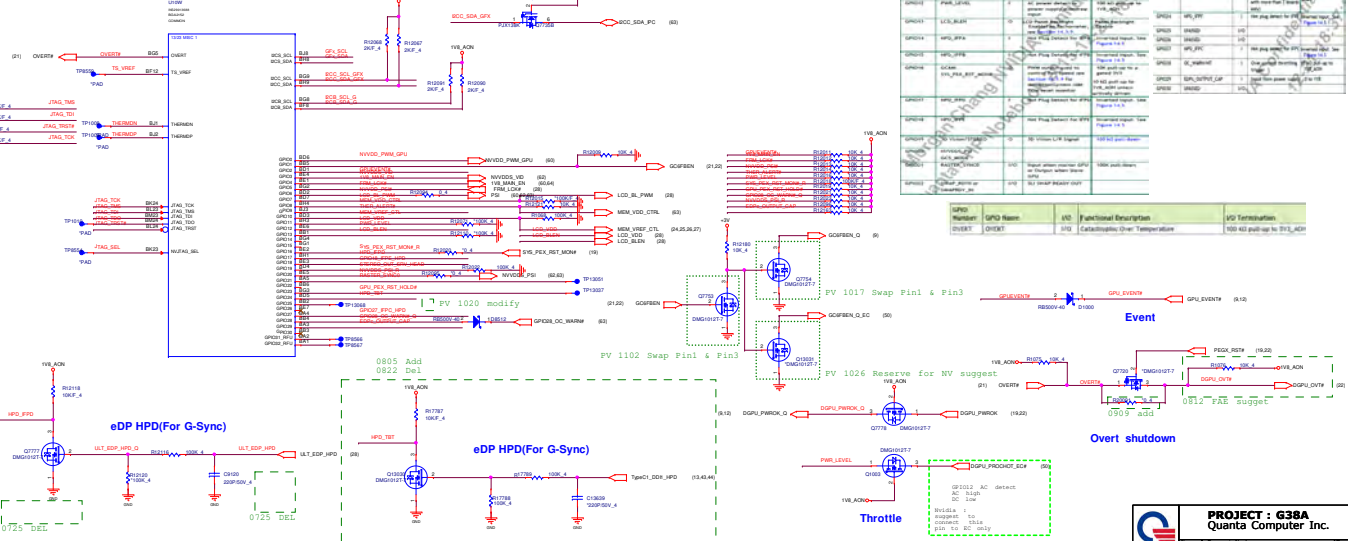
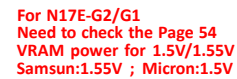


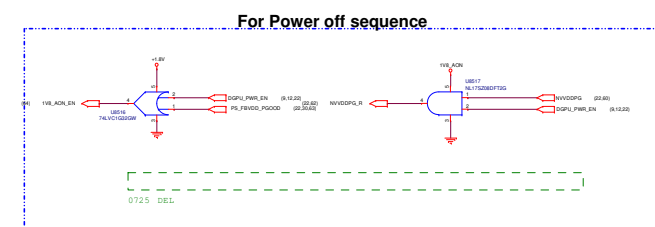
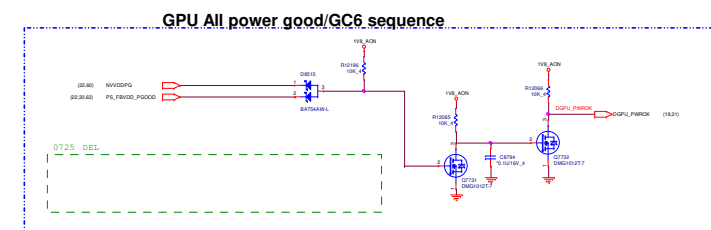
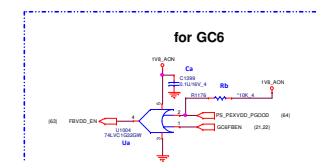
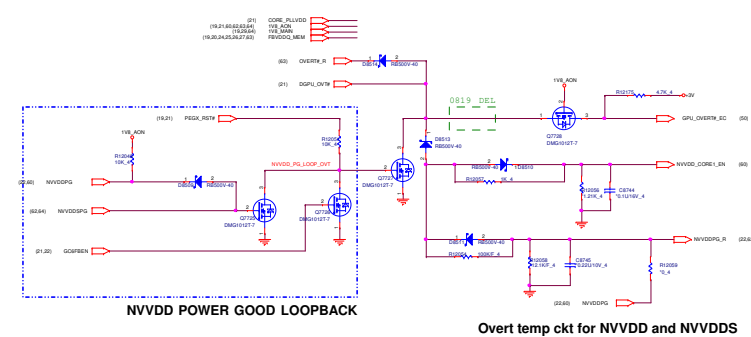
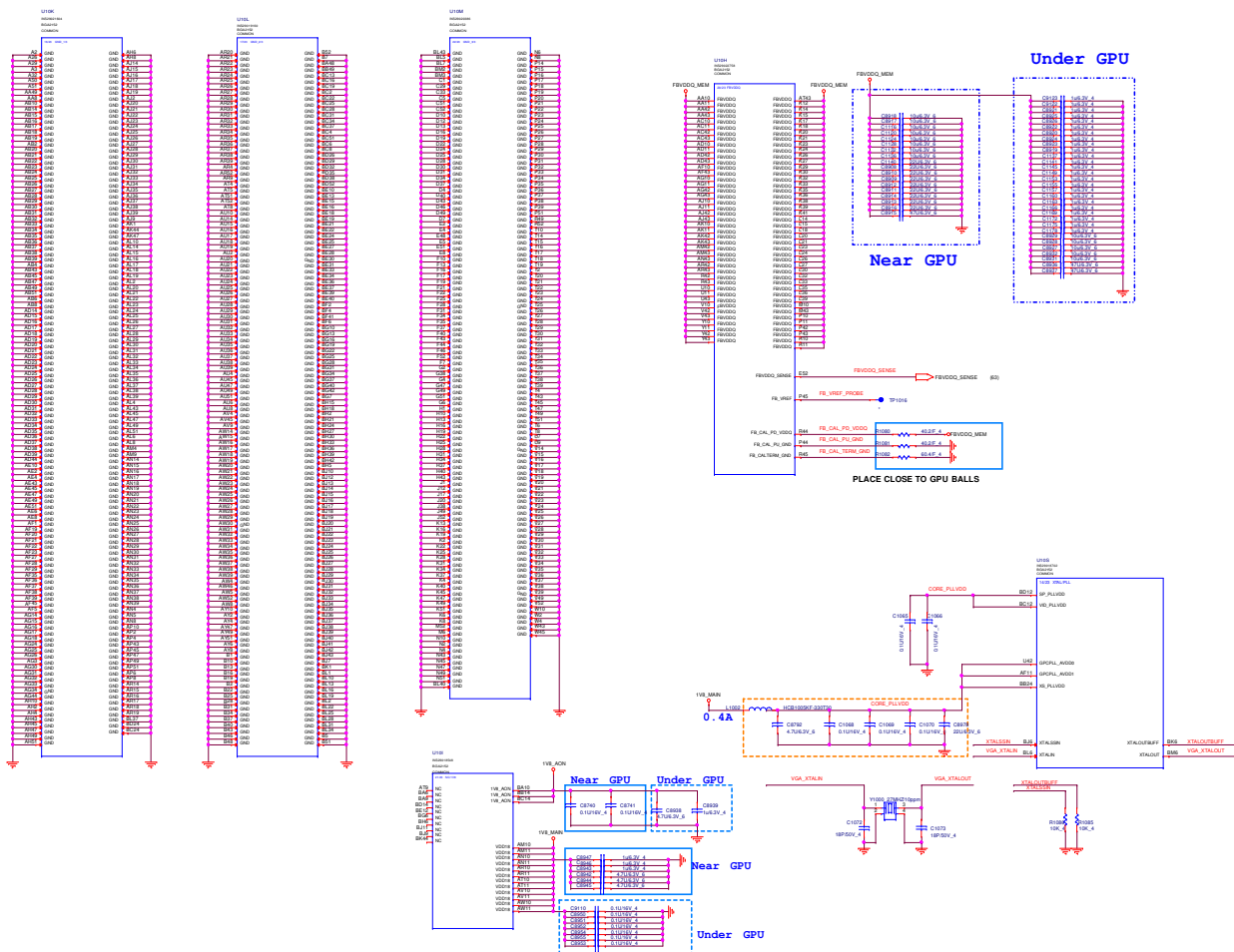


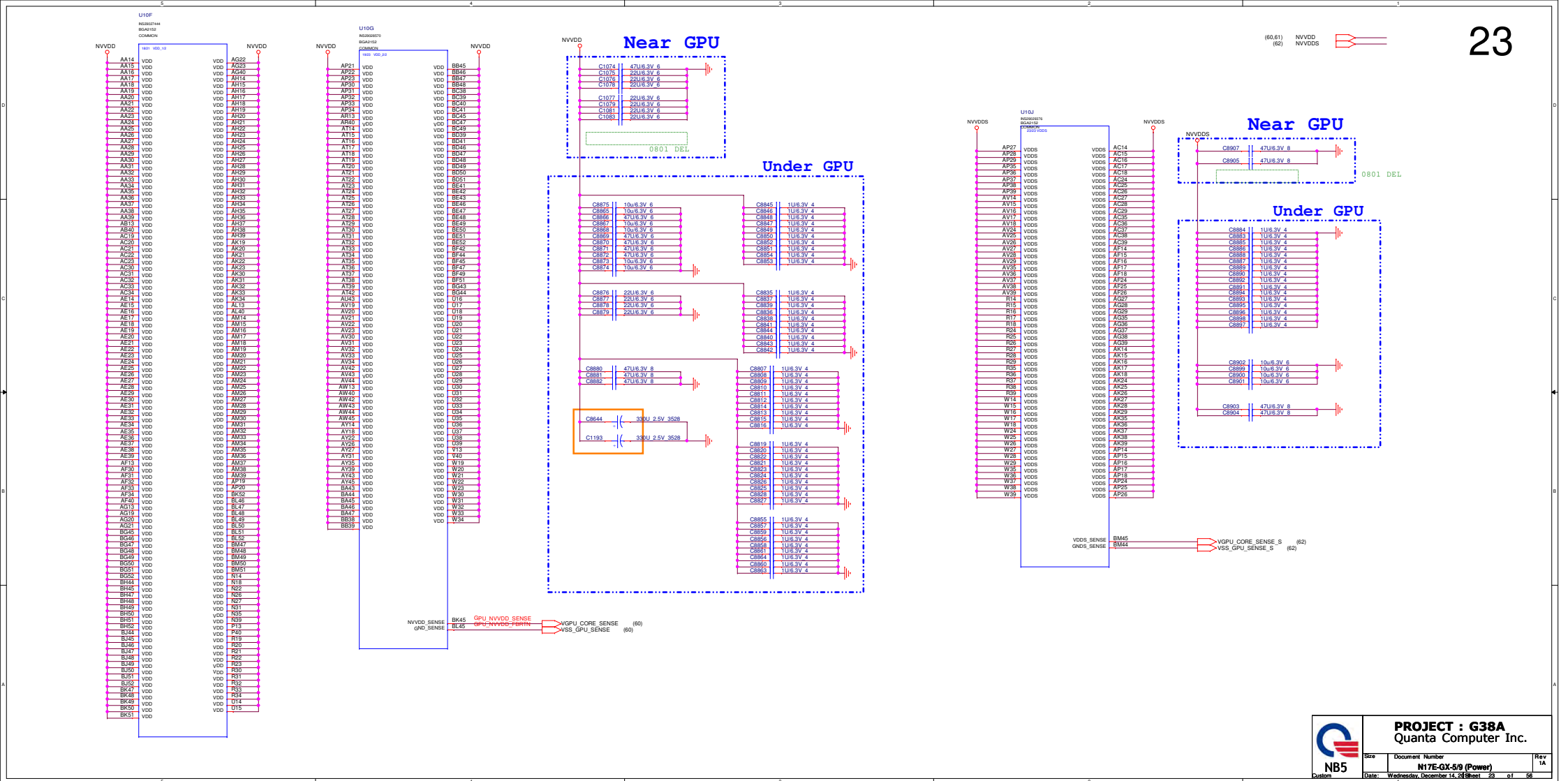


[illegible]

	Vender	Size	P/N
N17E-G2	WINBOND	8Mb	AKE\$GGN0N00
N17E-G1	Macronix	8Mb	AKE\$GFP0Z01

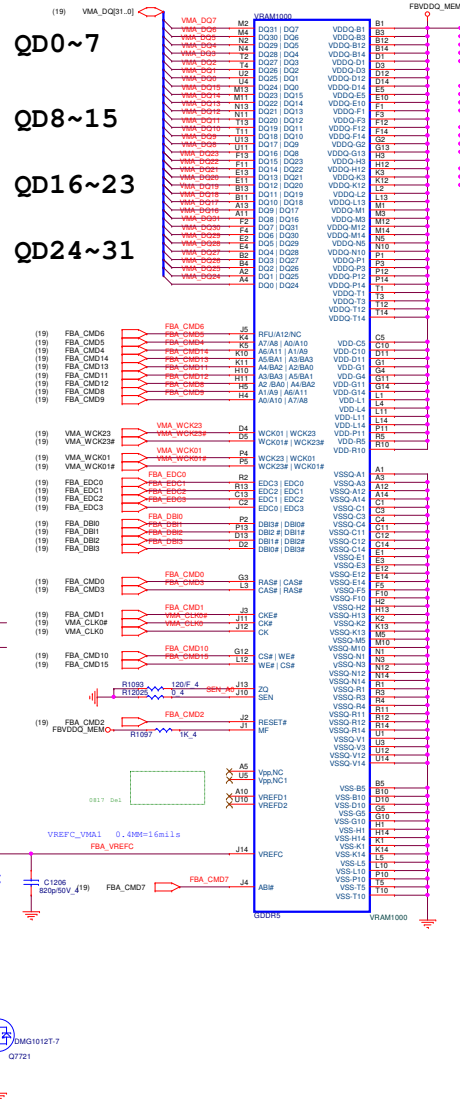






Channel 0  
<0~31>

MF=1 mirrored

Channel 1  
<32~63>

MF=0 Non-mirrored

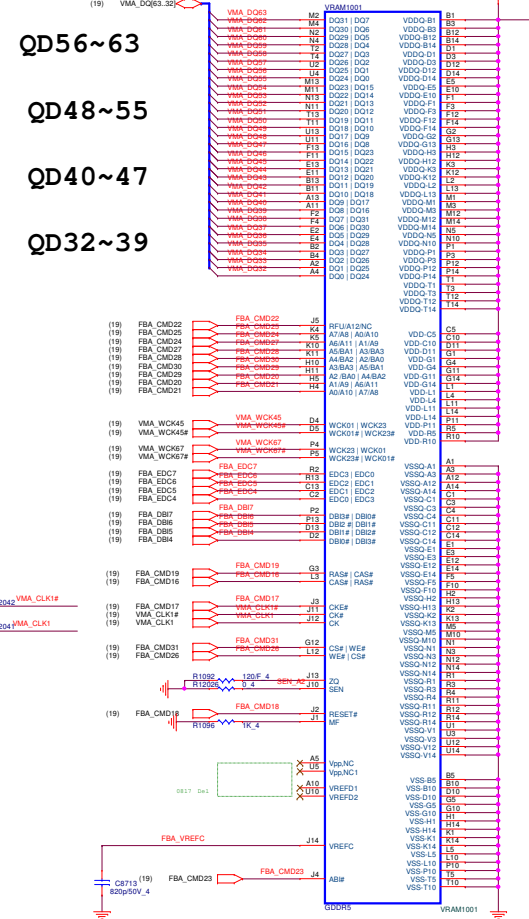


Table 7-5. GDDR5 Mode F Mapping

G03-256	Channel 0 0_31	G03-256	Channel 1 32_63
CM00	CA3*	CM016	CA3*
CM01	CKE	CM017	CKE
CM02	RST*	CM018	RST*
CM03	RA3*	CM019	RA3*
CM04	A1_A9	CM020	A1_A9
CM05	A0_A10	CM021	A0_A10
CM06	A12_RFU	CM022	A12_RFU
CM07	AB*	CM023	AB*
CM08	A6_A11	CM024	A6_A11
CM09	A7_A8	CM025	A7_A8
CM10	WE*	CM026	WE*
CM11	A5_BA1	CM027	A5_BA1
CM12	A4_BA2	CM028	A4_BA2
CM13	A7_BA0	CM029	A7_BA0
CM14	A3_BA3	CM030	A3_BA3
CM15	C3*	CM031	C3*

Notes:  
1. CPU debug pins: not connected to DRAM. See section 7.1.11.

Channel 1  
<0-31>Channel 0  
<0-31>

MF=1 mirrored

MF=0 Non-mirrored

QD0~7

QD8~15

QD16~23

QD24~31

QD56~63

QD48~55

QD40~47

QD32~39

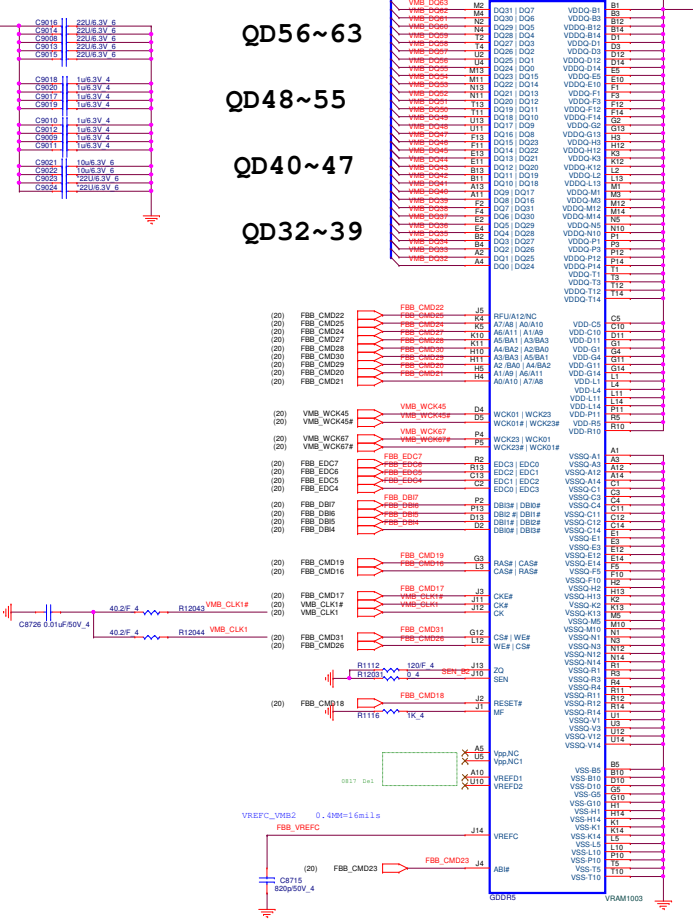
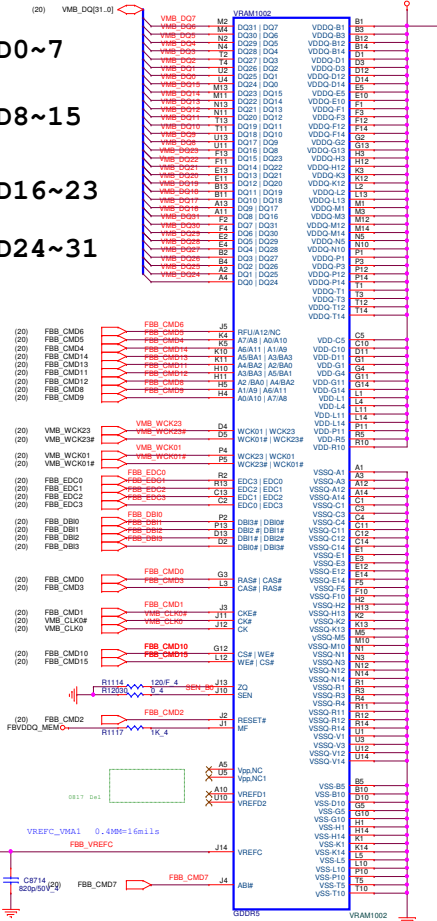


Table 7-5. GDDR5 Mode F Mapping

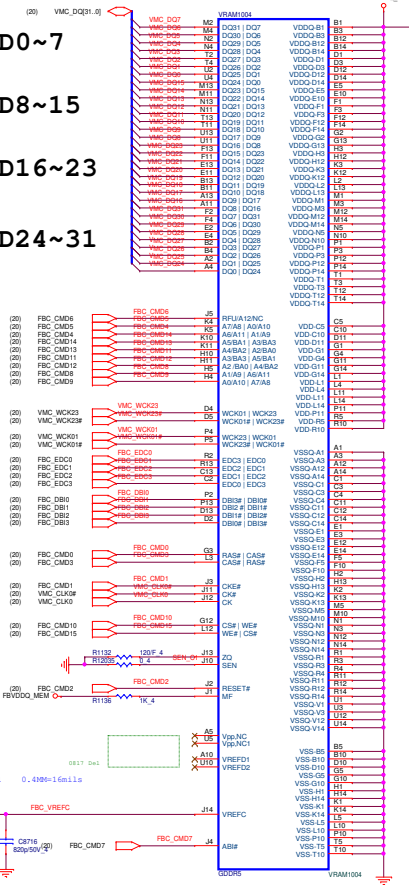
G83-256	Channel 0 0..31	G83-256	Channel 1 32..63
CM00	CAS*	CM016	CAS*
CM01	CKE	CM017	CKE
CM02	RST*	CM018	RST*
CM03	RAS*	CM019	RAS*
CM04	A1_A9	CM020	A1_A9
CM05	A10_A19	CM021	A10_A19
CM06	A12_A19	CM022	A12_A19
CM07	A8*	CM023	A8*
CM08	A8_A11	CM024	A8_A11
CM09	A7_A8	CM025	A7_A8
CM10	WFF	CM026	WFF
CM11	A5_BA1	CM027	A5_BA1
CM12	A4_BA2	CM028	A4_BA2
CM13	A7_BA0	CM029	A7_BA0
CM14	A3_BA3	CM030	A3_BA3
CM15	C3*	CM031	C3*

Notes:  
1. CPU daisy chain: not connected to DRAM. See section 7.1.13.



Channel 0  
<0-31>

MF=0 Non-mirrored

QD0~7  
QD8~15  
QD16~23  
QD24~31Channel 1  
<0-31>

MF=0 Non-mirrored

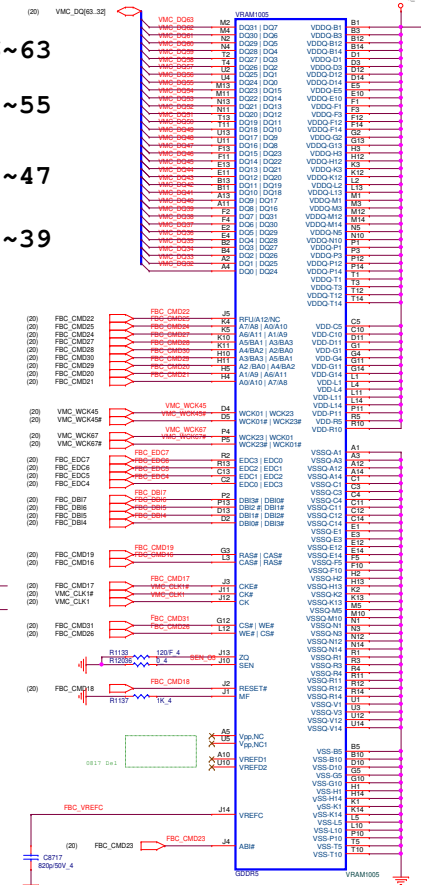
QD56~63  
QD48~55  
QD40~47  
QD32~39

Table 7-5. GDDR5 Mode F Mapping

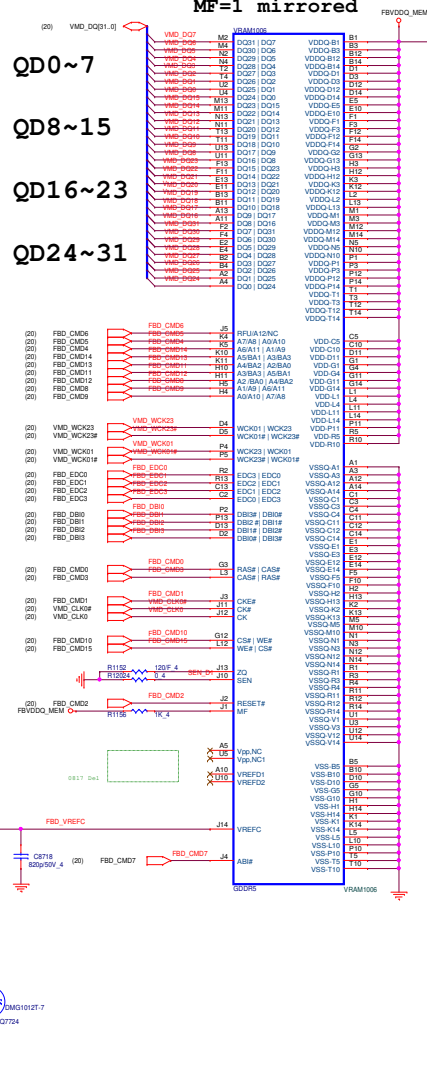
G83-256	Channel 0 0..31	G83-256	Channel 1 32..63
CM00	CAS*	CM016	CAS*
CM01	CKE	CM017	CKE
CM02	BS*	CM018	BS*
CM03	RAS*	CM019	RAS*
CM04	A1_A9	CM020	A1_A9
CM05	A0_A10	CM021	A0_A10
CM06	A12_RFU	CM022	A12_RFU
CM07	AB*	CM023	AB*
CM08	AA_A11	CM024	AA_A11
CM09	A7_A8	CM025	A7_A8
CM010	WE*	CM026	WE*
CM011	A5_BA1	CM027	A5_BA1
CM012	A4_BA2	CM028	A4_BA2
CM013	A2_BA0	CM029	A2_BA0
CM014	A3_BA3	CM030	A3_BA3
CM015	CS*	CM031	CS*
CM032	FBVDDQ		
CM033	FBVDDQ		
CM034	FBVDDQ		
CM035	FBVDDQ		

Notes:  
1. GPO debug pins: not connected to DRAM. See section 7.1.1.3.



Channel 0  
<0-31>

MF=1 mirrored

Channel 1  
<0-31>

MF=0 Non-mirrored

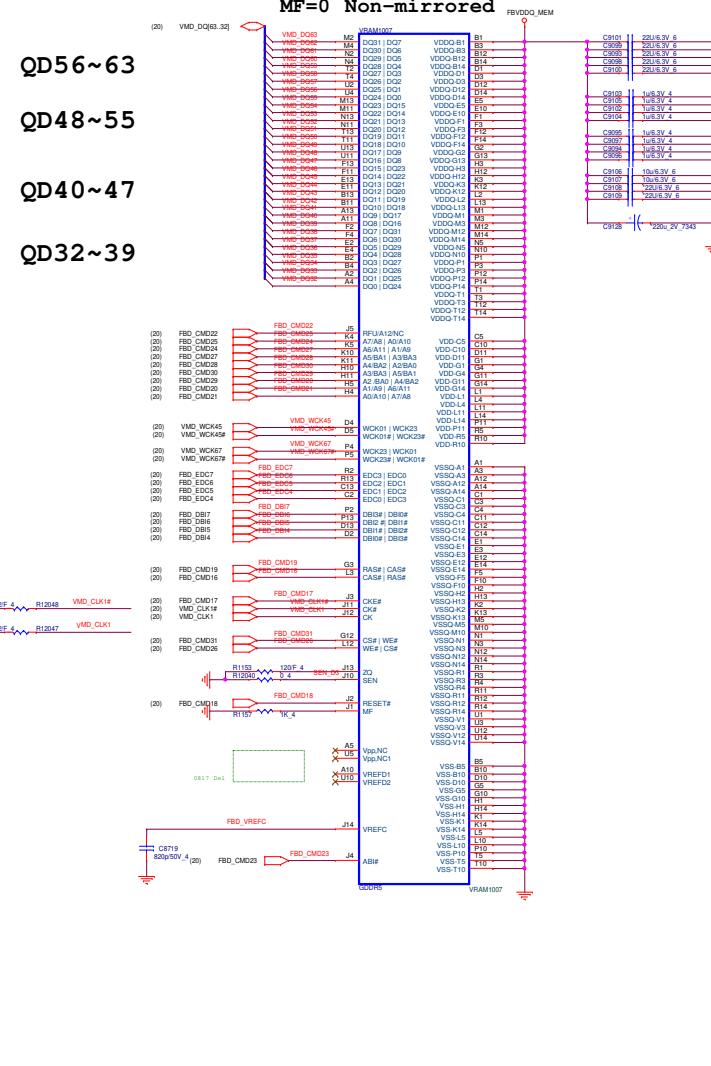
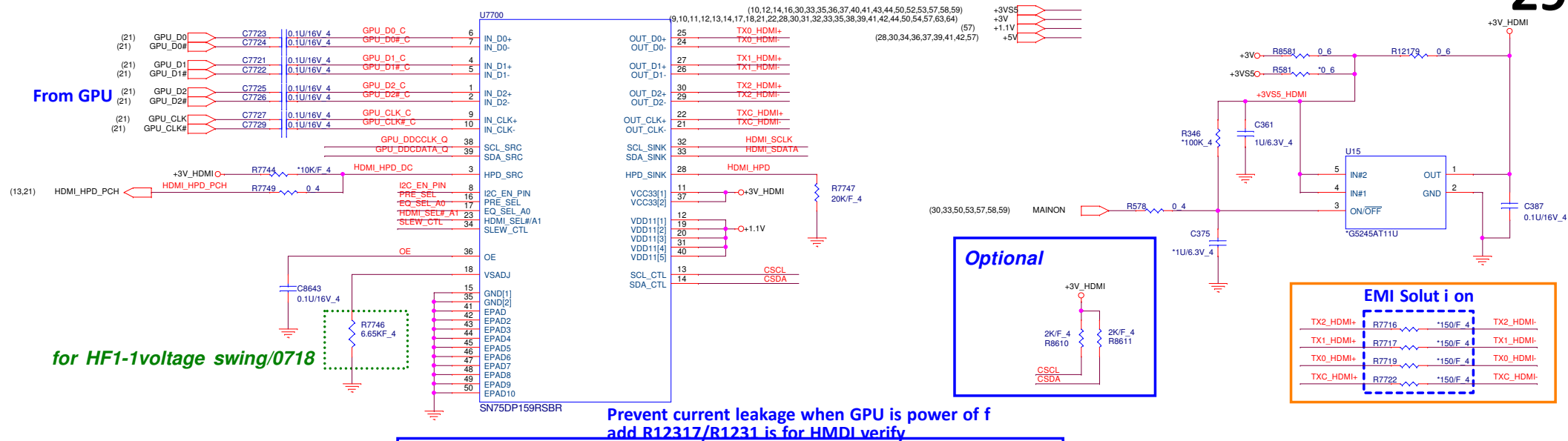


Table 7-5. GDDR5 Mode F Mapping

G33-256	Channel 0 0..31	G33-256	Channel 1 32..63
CM00	CAS*	CM016	CAS*
CM01	CKE	CM017	CKE
CM02	RST*	CM018	RST*
CM03	RAS*	CM019	RAS*
CM04	A1_A9	CM020	A1_A9
CM05	A0_A10	CM021	A0_A10
CM06	A12_RFU	CM022	A12_RFU
CM07	AB*	CM023	AB*
CM08	AB_A11	CM024	AB_A11
CM09	A7_A8	CM025	A7_A8
CM10	WE*	CM026	WE*
CM11	AS_BA1	CM027	AS_BA1
CM12	AA_BA2	CM028	AA_BA2
CM13	A2_BA3	CM029	A2_BA3
CM14	A3_BA3	CM030	A3_BA3
CM15	C*	CM031	C*

Notes:  
1. GPU debug pins: not connected to DRAM, see section 7.1.13.





### SN75DP159RSBR strap

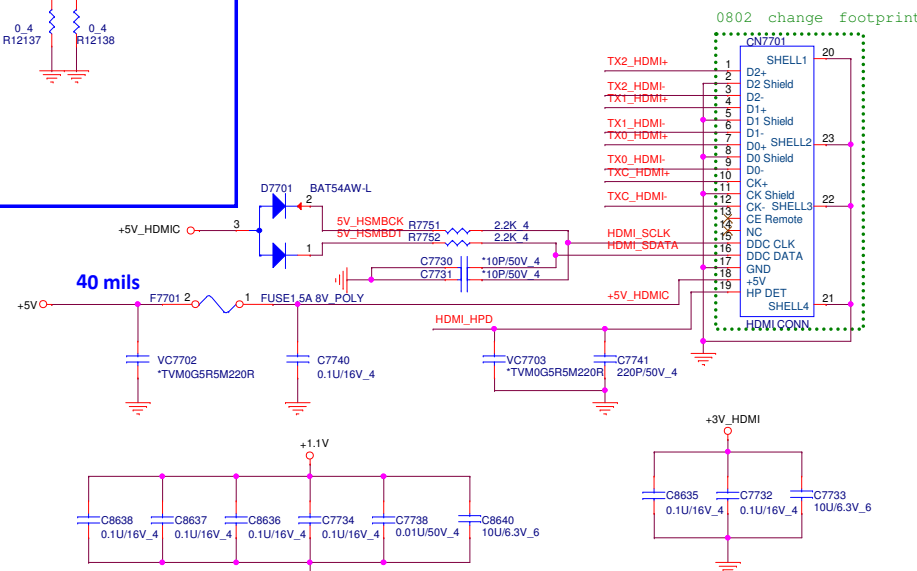
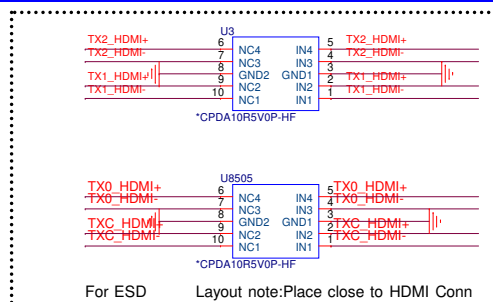
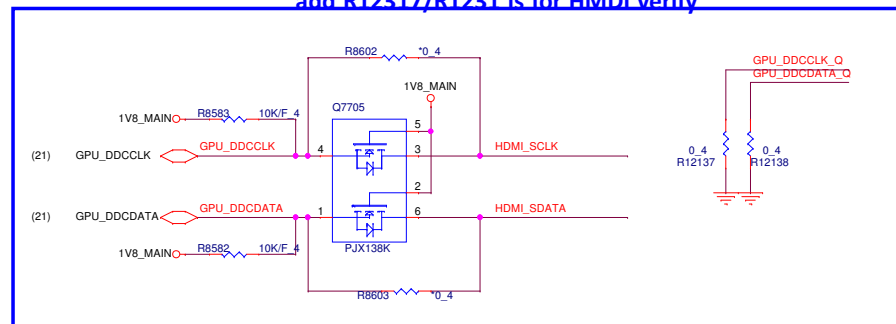
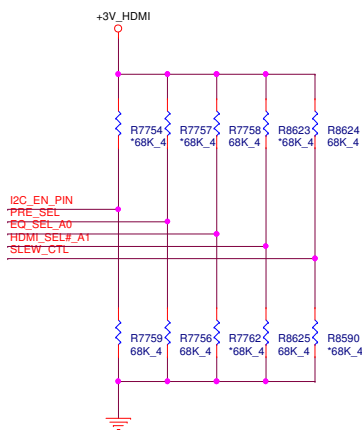
I2C\_EN/PIN = High: puts device into I2C control mode  
I2C\_EN/PIN = Low: puts device into pin strap mode

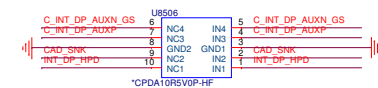
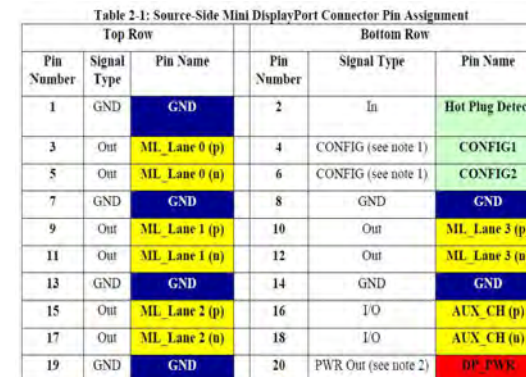
De-emphasis pin strap when I2C\_EN/PIN = Low.  
PRE\_SEL = L: - 2 dB de-emphasis  
PRE\_SEL = No Connect: 0 dB  
PRE\_SEL = H: Reserved

Input Receive Equalization pin strap when I2C\_EN/PIN = Low  
EQ\_SEL = L: Fixed EQ at 7.5 dB  
EQ\_SEL = No Connect: Adaptive EQ  
EQ\_SEL = H: Fixed at 14 dB

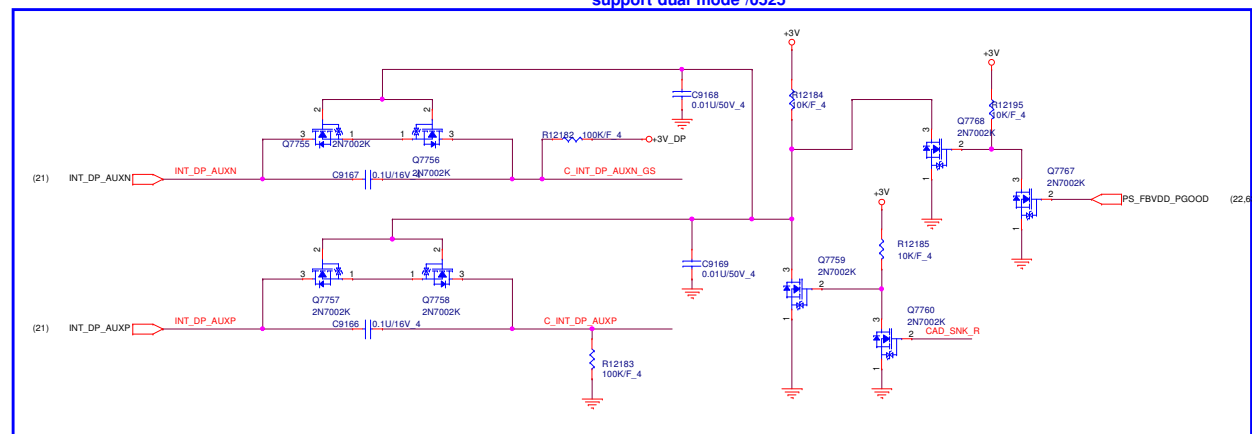
HDMI\_SEL when I2C\_EN/PIN = Low  
HDMI\_SEL = High: Device configured for DVI  
HDMI\_SEL = Low: Device configured for HDMI

Slew rate control when I2C\_EN/PIN = Low.  
SLEW\_CTL = H, fastest data rate  
SLEW\_CTL = L, 5 ps slow  
SLEW\_CTL = No Connect, 10 ps slow





For ESD                  Layout note:Place close to mini display Conn



SSEQ0,SSEQ1 : USB receiver equalizer gain  
for upstream facing SSTXP/N  
F,F(Default)  
When I2C\_EN is not '0' SSEQ0 sets I2C address

DPEQ0,DPEQ1 : DP Receiver equalization gain  
F,F(Default)  
When I2C EN is not '0' DPEQ0 sets I2C address

9. Power Sequence

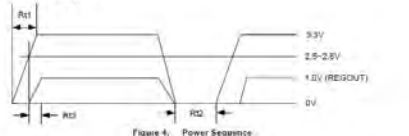
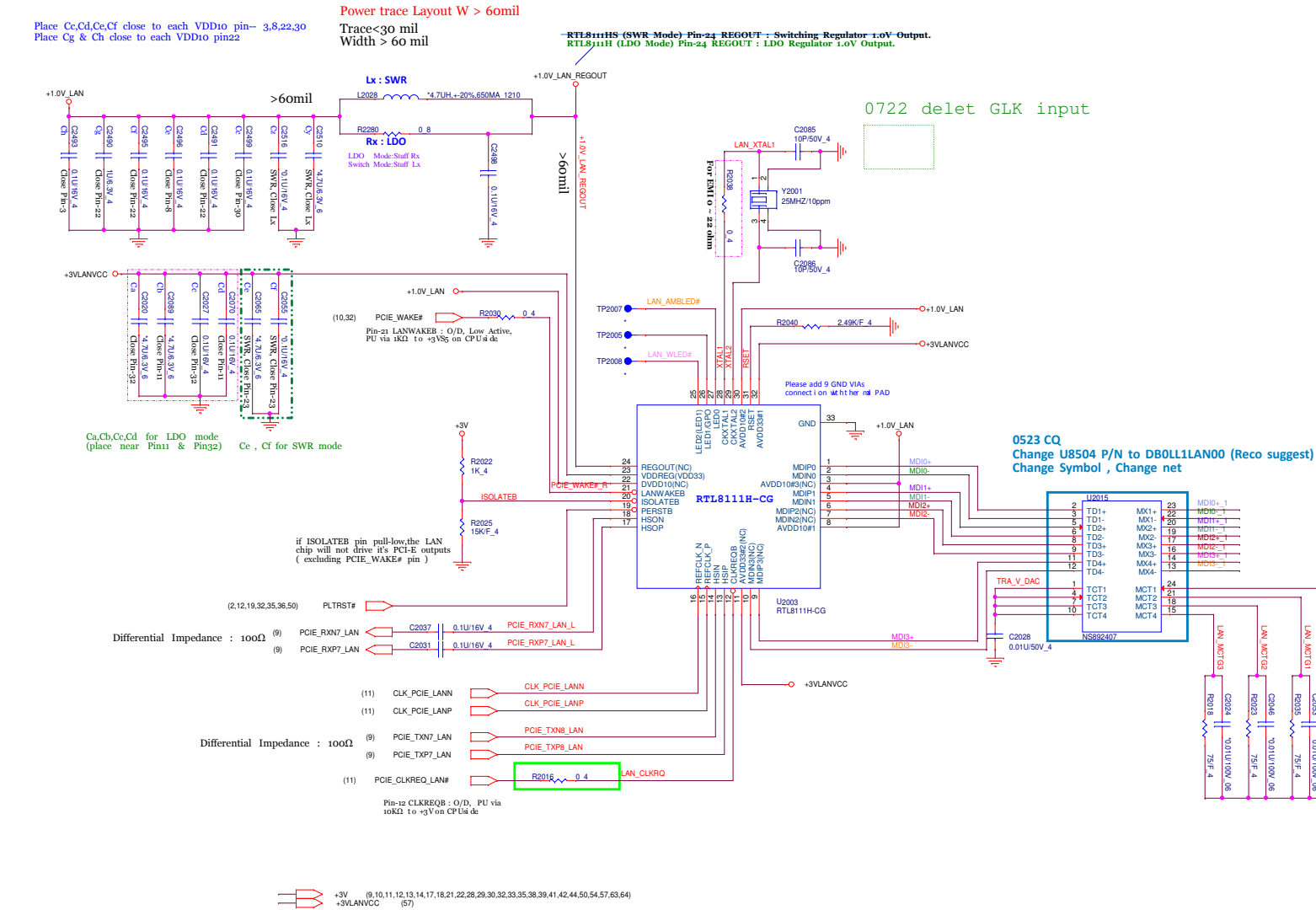


Table 16: Power Sequence Parameter

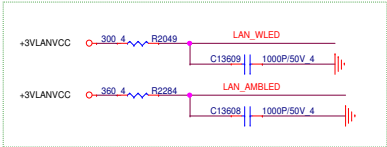
Symbol	Description	Min	Typical	Max	Units
R1	3.3V Rise Time	0.1	-	100	ms
R2	3.3V Off Time	10	-	-	ms
R3	1.0V (REGOUT) Settle Time	-	-	15	ms

Note: See the following section for power sequence requirements.

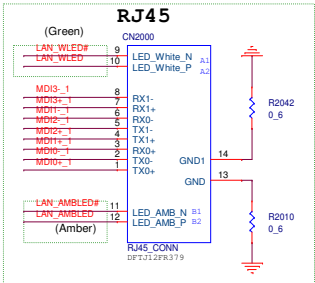


0722 delet GLK input

0803 modify



LAN CONN



0825 modify

0825 modify

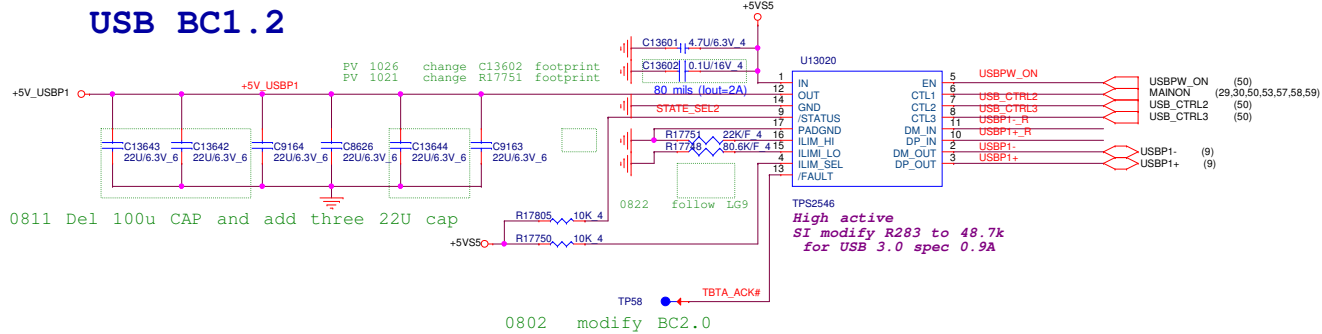
0803 change footprint

RTL8111GS : Switching Regulator  
RTL8111G : LDO Regulator

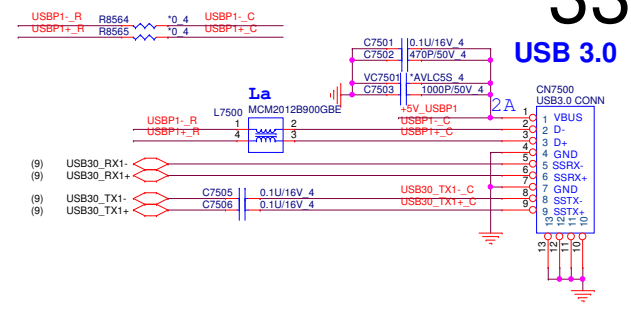




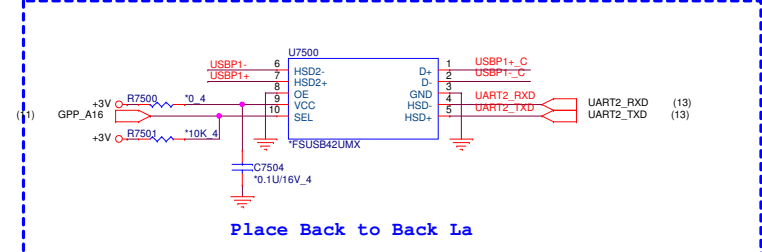
## USB BC1.2



## USB 2.0/3.0 Combo

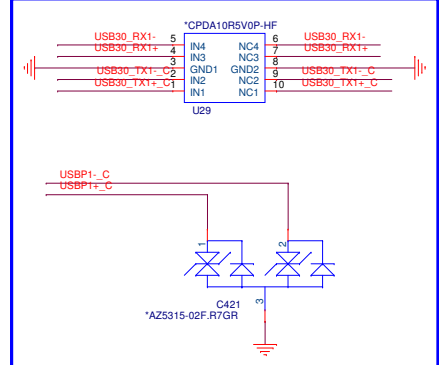
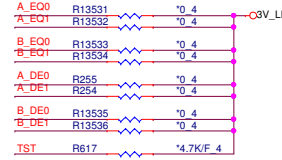
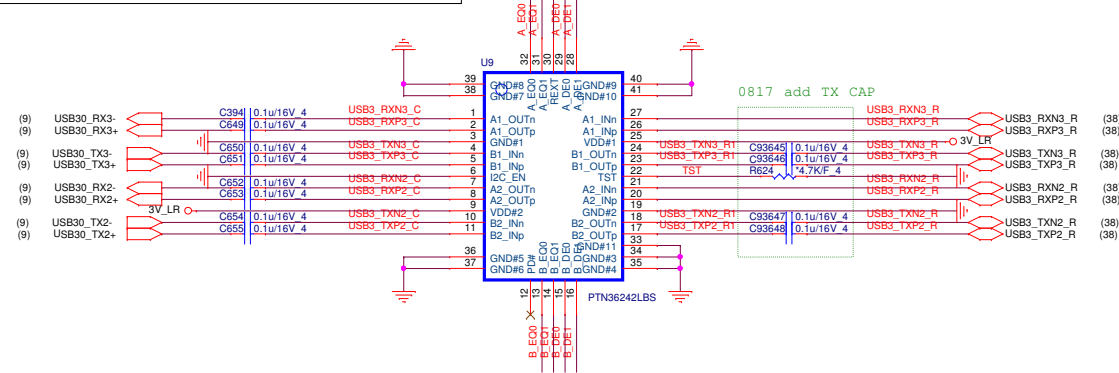
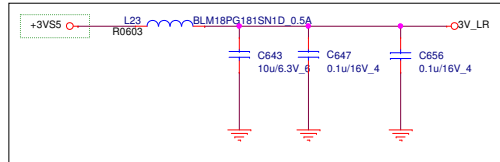


## UART for Win7 WHQL DEBUG



## USB3 Re-Driver

0812 change power rail



A_EQ0	A_EQ1		A_DE0	A_DE1	
0	0	9dB	0	0	-3.5dB
0	1	3dB	0	1	no de-emphasis
1	0	6dB	1	0	-7dB
1	1	7.5dB	1	1	-5dB

TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing

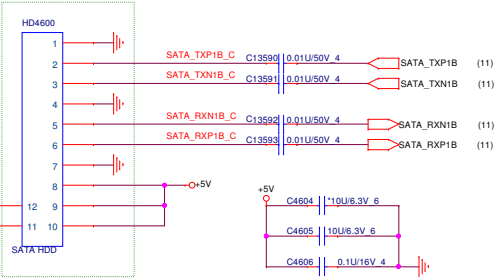
**PROJECT : G38A**  
Quanta Computer Inc.

Size Custom Document Number **USB3.0/DB**

Date: Wednesday, December 14, 2016 Sheet 33 of 56

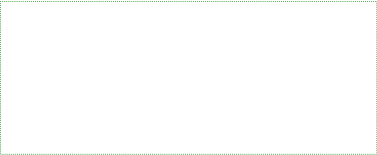
Rev 1A

HDD



0825 Swap pin

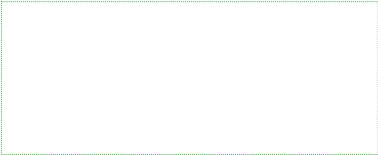
0722 delete SATA redriver IC



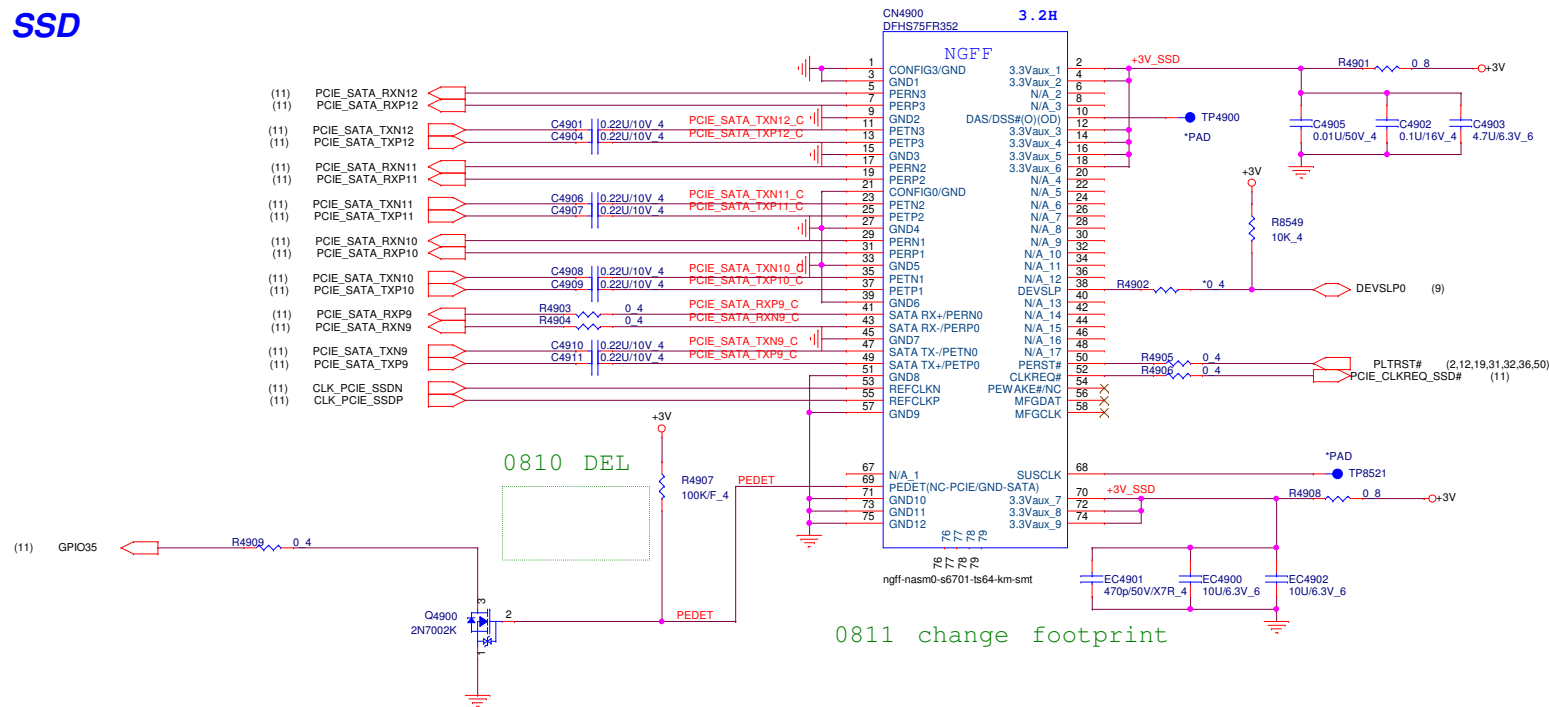
(9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,35,38,39,41,42,44,50,54,57,63,64)  
(28,29,30,36,37,39,41,42,57)  
(5,10,35,37,38,50,51,52,60)

+3V  
+5V  
+3VPCU

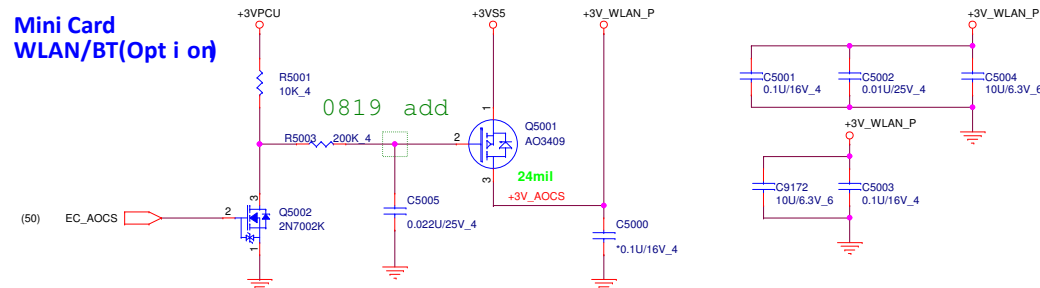
0718 delete 3D CAM



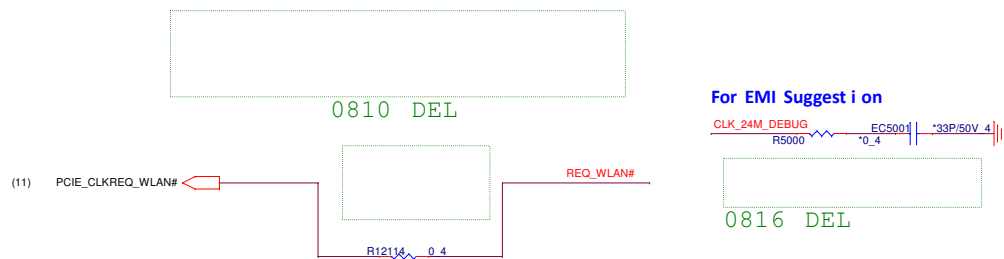
(22,58,64) +1.8V



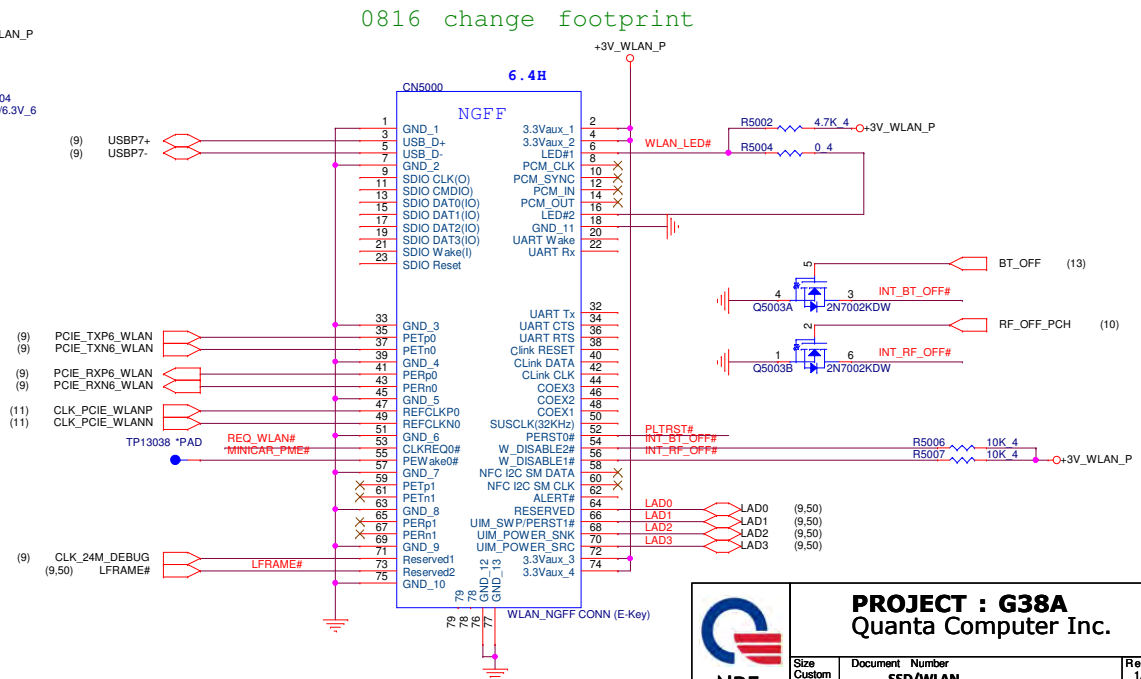
### Mini Card WLAN/BT(Opt i on)



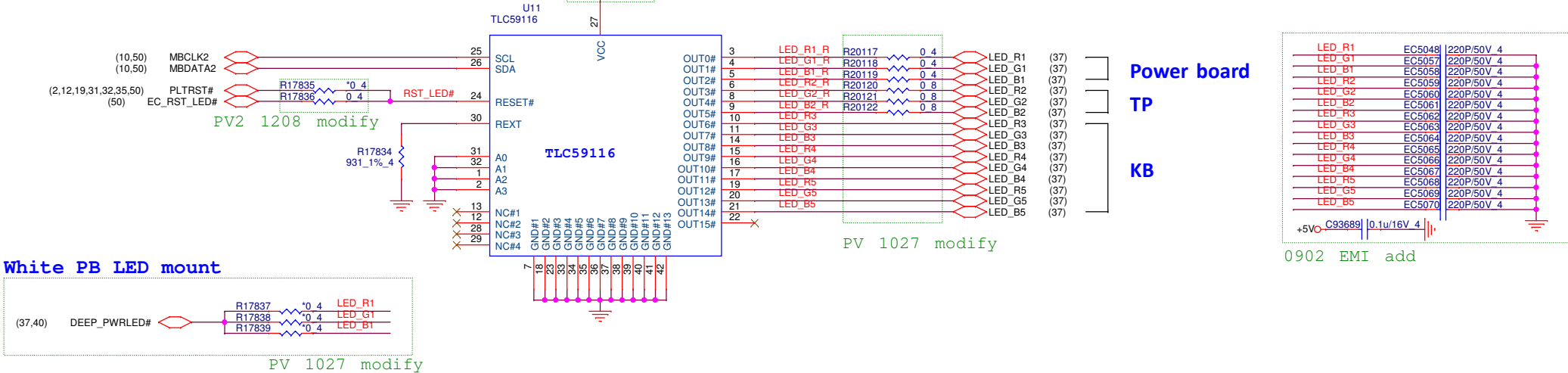
### Support Wake Function (Reserve)



For EMI Suggest i on



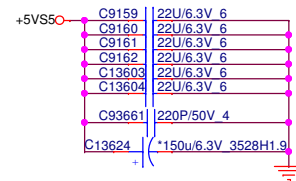
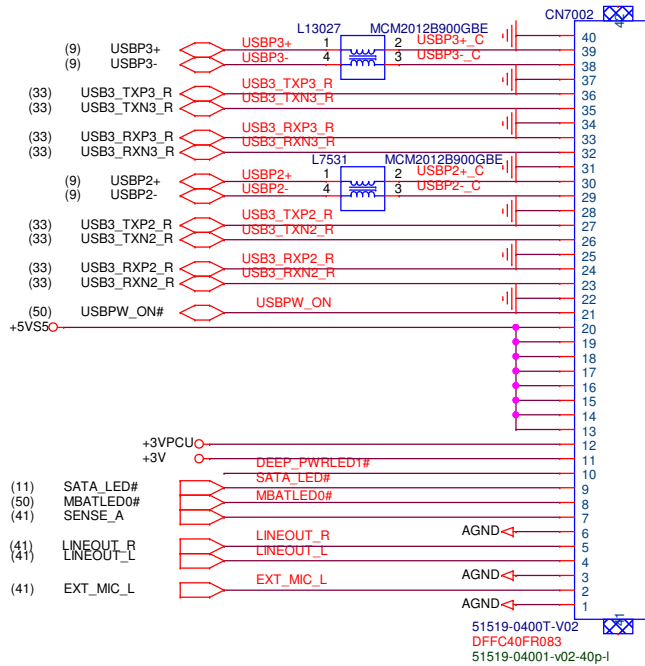
RGB KB LED Driver



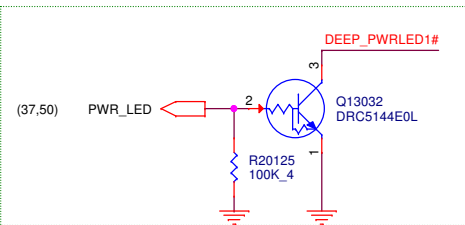
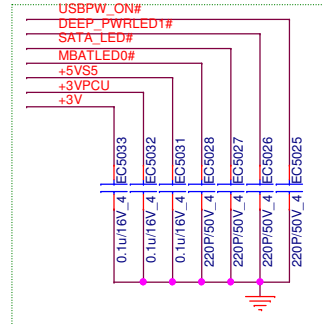


## Daughter Board

0803 change footprint



0807 EMI Stuff



PV 1102 add

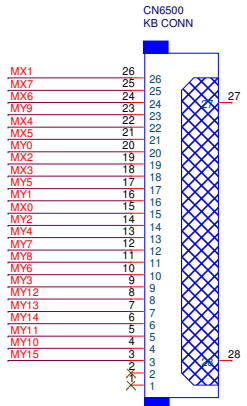
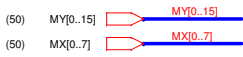


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Quanta Computer Inc.

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	TPM/G-Sensor/IR CAM	1A
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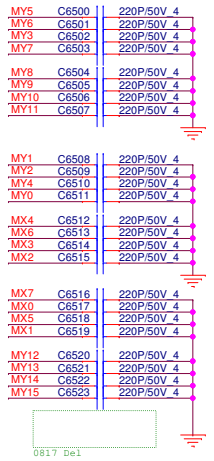
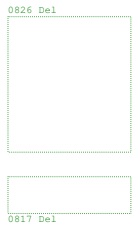


KEYBOARD Con.



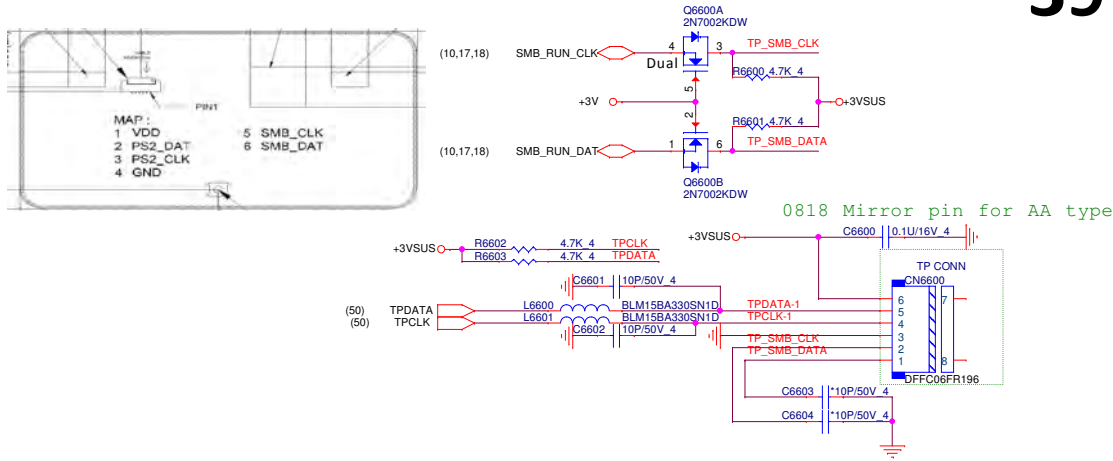
0803 change footprint  
0817 Modify pin define

KEYBOARD PULL-UP

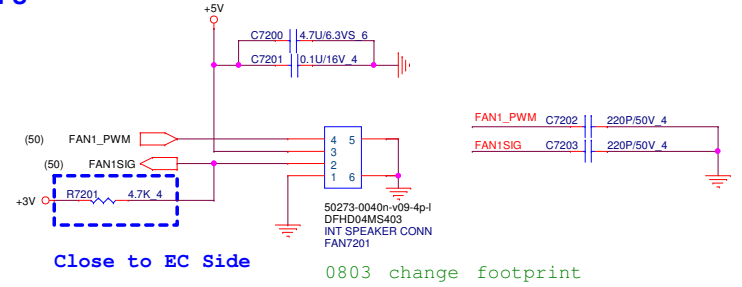


Touch Pad Connector AA type

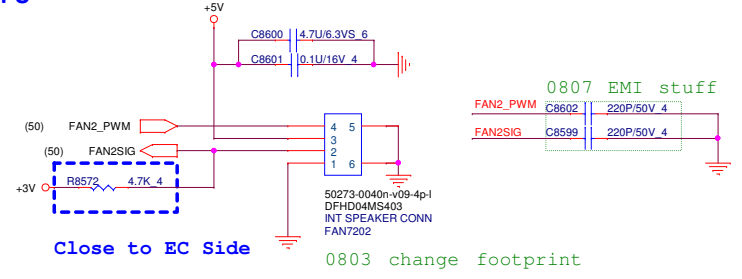
39



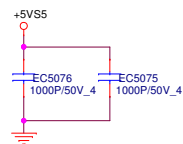
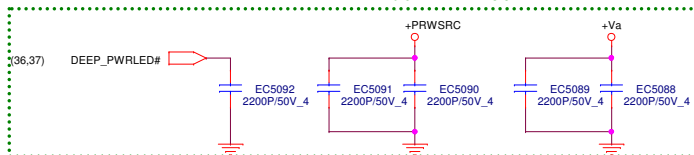
FAN1 for CPU



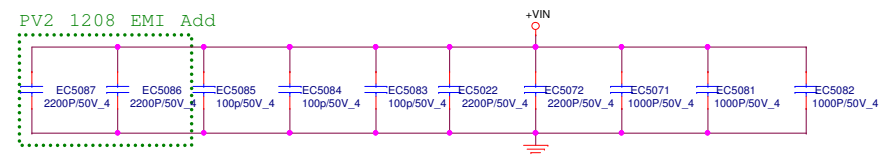
FAN2 for GPU



## PV2 1208 EMI Add



## PV2 1208 EMI Add



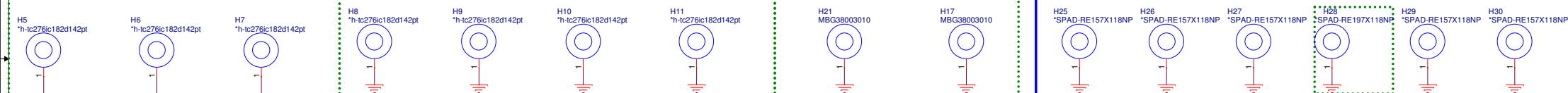
## GPU BTK Hole

## CPU BTK Hole

## WLAN NUT

## SSD NUT

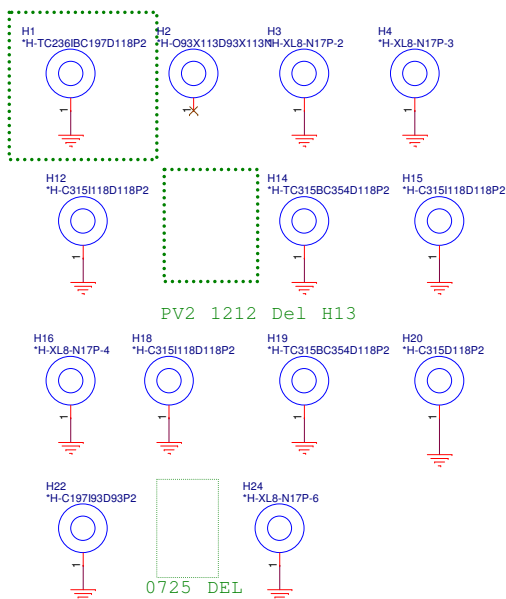
## EMI PAD



0909 modify

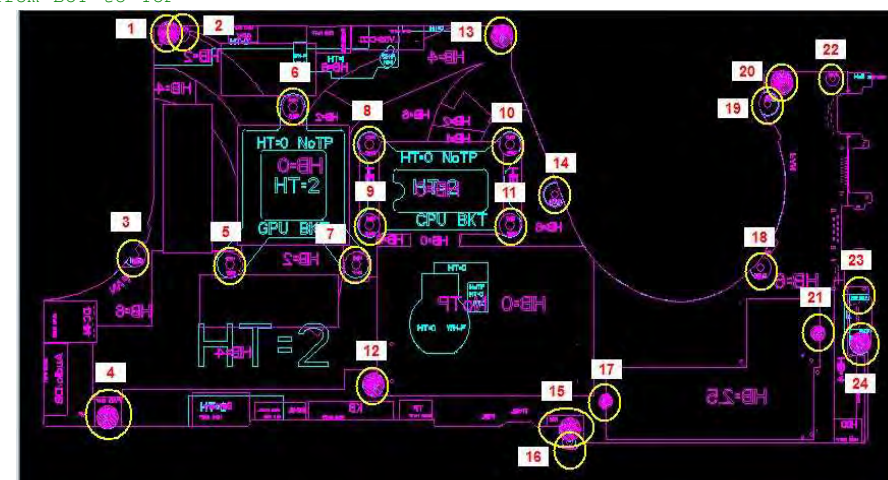
0909 modify


PV 1021 change from BOT to TOP

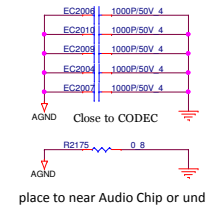


PV2 1212 Del H13

0725 DEL



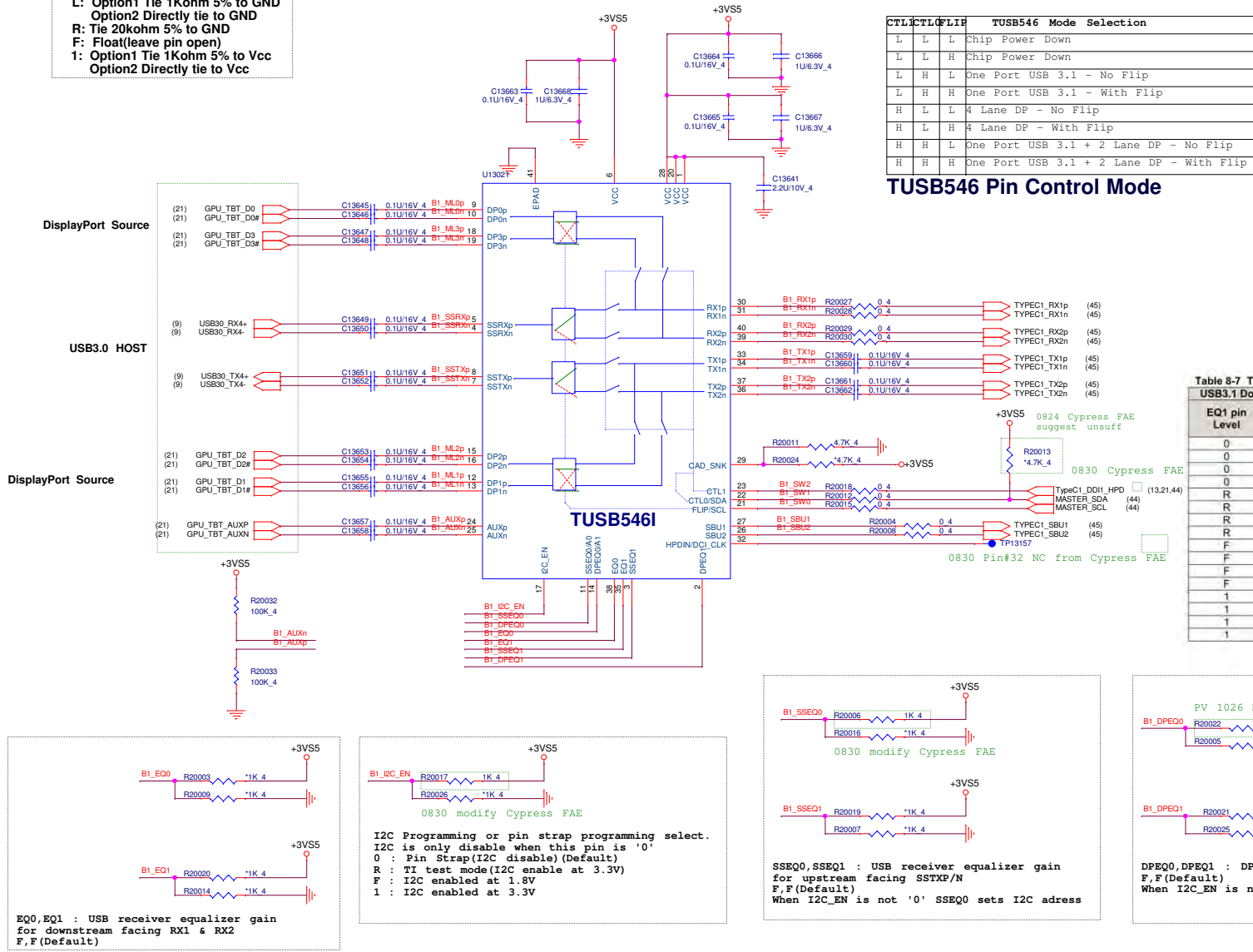
	<b>PROJECT : G38A</b>		
	Quanta Computer Inc.		
	Size Custom	Document Number <b>RF Solution/HOLE</b>	Rev 1A
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R364	R363	R373	R372	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

4 Level Input:  
L: Option1 Tie 1Kohm 5% to GND  
Option2 Directly tie to GND  
R: Tie 20kohm 5% to GND  
F: Float(leave pin open)  
1: Option1 Tie 1Kohm 5% to Vcc  
Option2 Directly tie to Vcc



CTL1	CTL2	FLIP	TUSB546 Mode Selection
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	One Port USB 3.1 - No Flip
L	H	H	One Port USB 3.1 - With Flip
H	L	L	4 Lane DP - No Flip
H	L	H	4 Lane DP - With Flip
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flip
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flip

### TUSB546 Pin Control Mode

CTL1	FLIP	AUX Select
H	L	AUXP->SBU1, AUXN->SBU2
H	H	AUXP->SBU2, AUXN->SBU1
L>2ms	X	One Port USB 3.1 - No Flip

### AUX Pin Control Mode

Table 8-7 TUSB546 Receiver Equalization GPIO Control

USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Port			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @2.5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @2.5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @2.5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	F	10	F	F	10	F	F	10
F	1	11	F	1	11	F	1	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

## CC+PD

0824 add

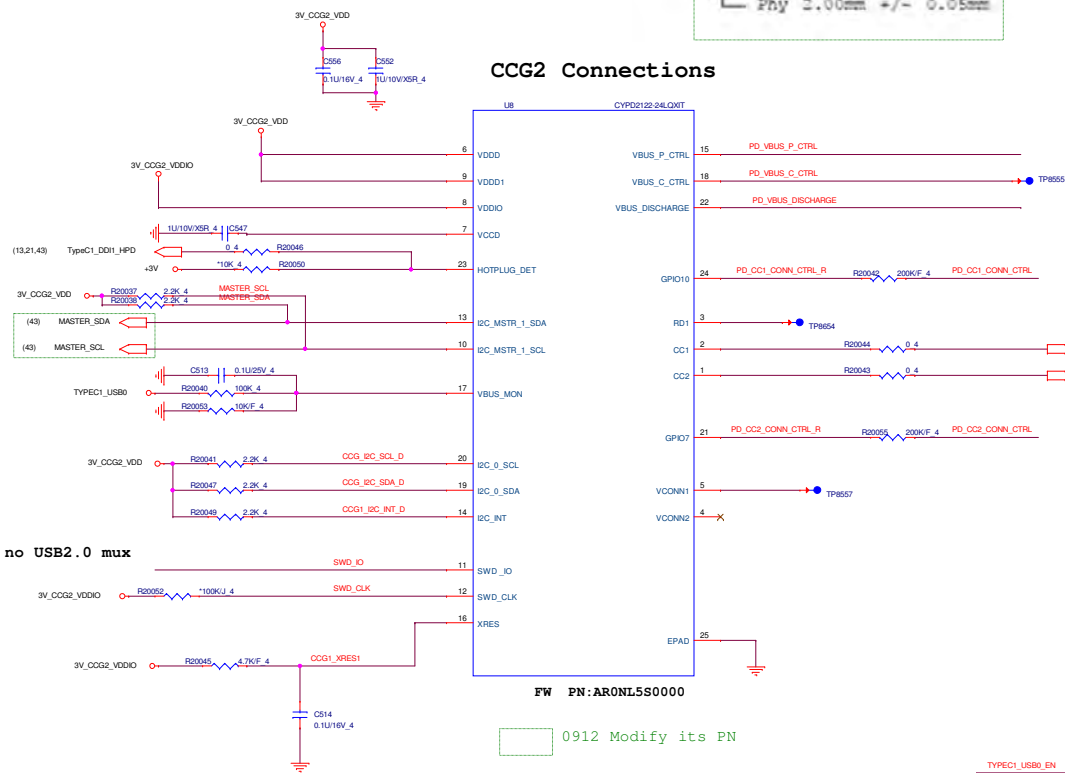
3V\_CCG2\_VDD  
 CCG1\_XRES1  
 SWD\_CLK  
 SWD\_IO

The Test Points :

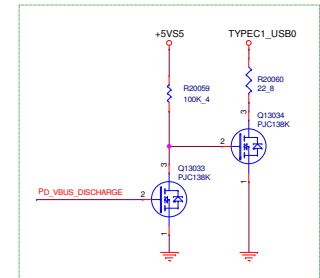
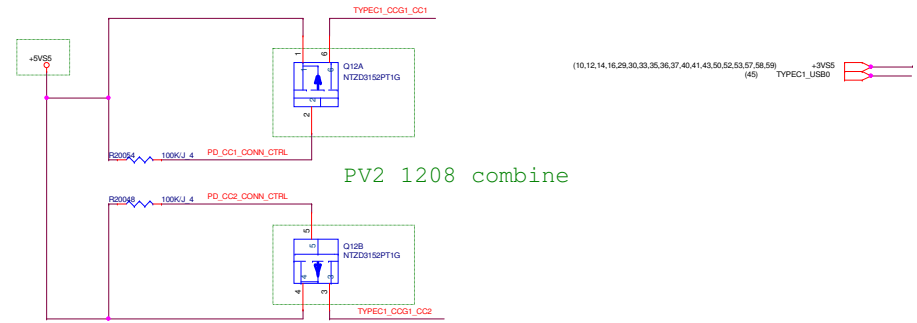
Pitch 2.54mm +/- 0.05mm

Phy 2.00mm +/- 0.05mm

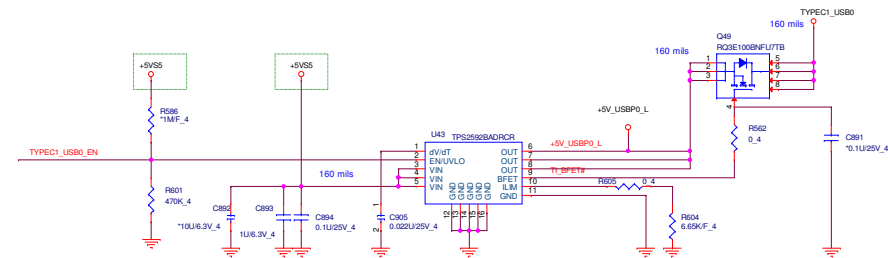
## CCG2 Connections



PV2 1208 combine



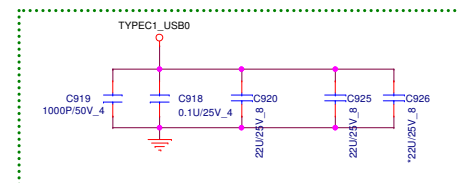
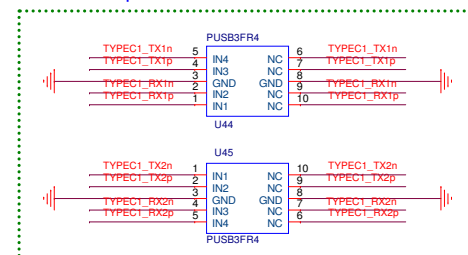
0816 add



$$R_{lim} = (I_{lim} - 0.7) / (3 * 0.00001)$$

fix 0.9A





TYPEC1\_USB0

CN13005

TYPEC1\_USB0

D6

1 2 P4SMAFJ20A

(43) TYPEC1\_RX1p (43) TYPEC1\_RX1n

USBP6+ C USBP6- C

A2 TX1P RX1P B10 TYPEC1\_RX1p (43)

A9 TX1N RX1N B9 TYPEC1\_RX1n (43)

A6 DP1 DN2 B7 USBP6- C

A7 DN1 DP2 B6 USBP6+ C

(43) TYPEC1\_RX2n (43) TYPEC1\_TX2p

A10 RX2N TX2N B3 TYPEC1\_TX2n (43)

A11 RX2P TX2P B2 TYPEC1\_TX2p (43)

(43) TYPEC1\_SBU1 (43) TYPEC1\_SBU2

A8 RFU1 RFU2 B8 TYPEC1\_SBU2 (43)

(44) TYPEC1\_CCG1\_CC1 (44) TYPEC1\_CCG1\_CC2

A5 CC1 CC2 B5 TBTA\_CC2

GND#5 1

GND#6 2

GND#7 3

GND#8 4

GND#9 5

GND#10 6

GND#11 7

GND#12 8

GND#13 9

GND#14 10

GND#15 11

GND#16 12

A12 GND#1

B1 GND#2

B12 GND#3

\*EGA10402V05AH D13028

\*EGA10402V05AH D4

u631-ult1123-1a503-7h-24p-smt

```
0802 modify footprint, follow S400
```



Size	Document Number	Re
	<b>AR - TBT (USB2 &amp; DP Part)</b>	1.
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**Quanta Computer Inc.**

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	TPM/G-Sensor/IR CAM	1A
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**Quanta Computer Inc.**

Size	Document Number TPM/G-Sensor/IR CAM	Rev 1A
Date: Wednesday, December 14, 2011 Sheet 47 of 56		



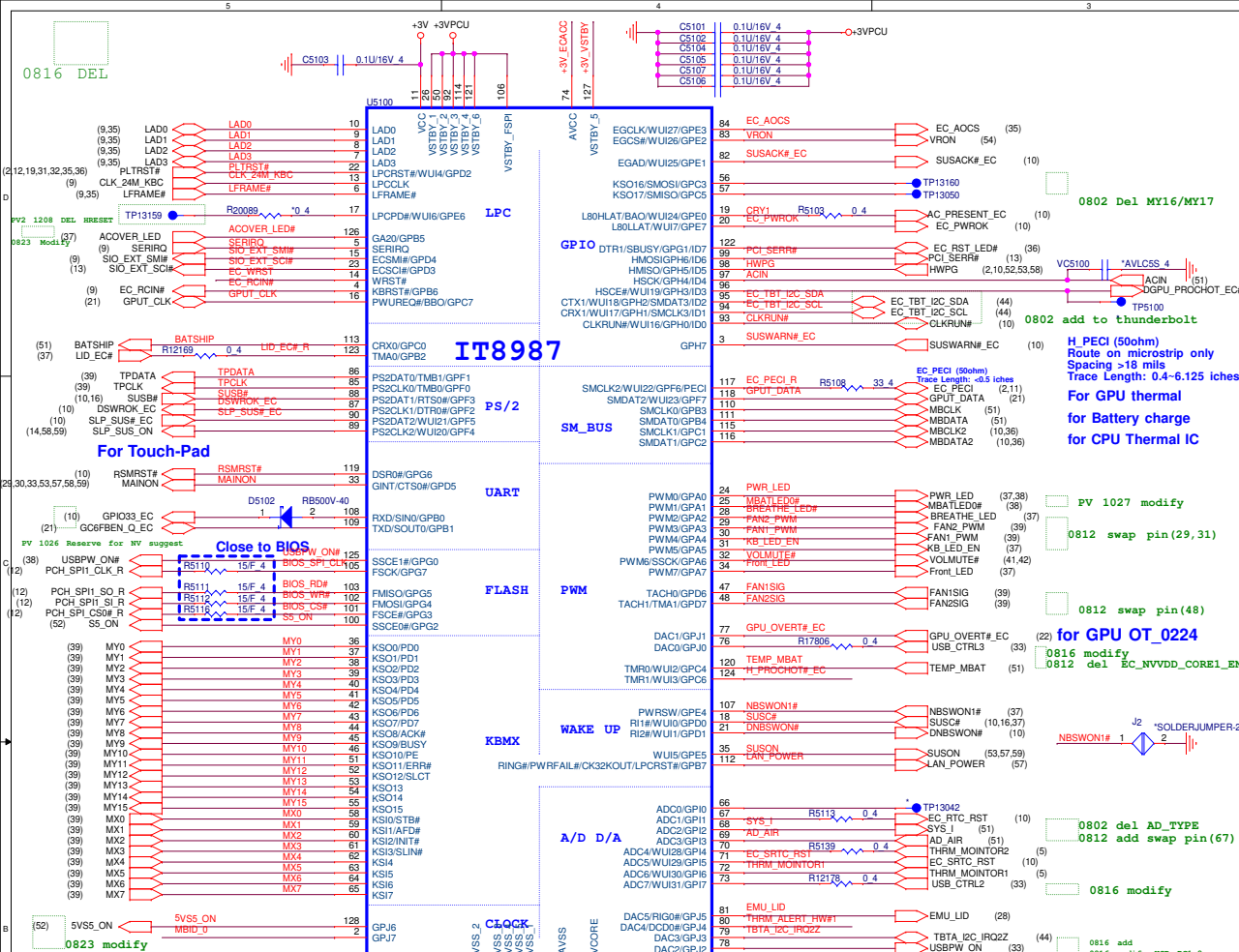
**PROJECT : G38A**  
**Quanta Computer Inc.**

Size	Document Number TPM/G-Sensor/IR CAM	Rev 1A
Date: Wednesday, December 14, 2011 Sheet 48 of 56		



**PROJECT : G38A**  
**Quanta Computer Inc.**

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Date: Wednesday, December 14, 2011 Sheet 49 of 56		



0802 Del MY16/MY17

add to thunderbolt

H\_PECI (50ohm)  
Route on microstrip only  
Spacing >18 mils  
Trace Length: 0.4~6.125 inches

For GPU thermal  
for Battery charge  
for CPU Thermal IC

PV 1027 modifv

```
0812 swap pin(29,31)
```

```
0812 swap pin(48)
```

for GPU OT 0224

```
816 modify
```

J2 \*SOLDERJUMPER-2

```
*****0802 del AD TYPE
```

0816 modi fix

```
0816 add
```

```
0816 add
0816 modify USB BC1.2
```

50V\_4

A diagram showing a protein structure with a red arrow pointing to a specific residue. The protein is represented by a blue line with yellow circles, and the red arrow points to a specific residue on the line.

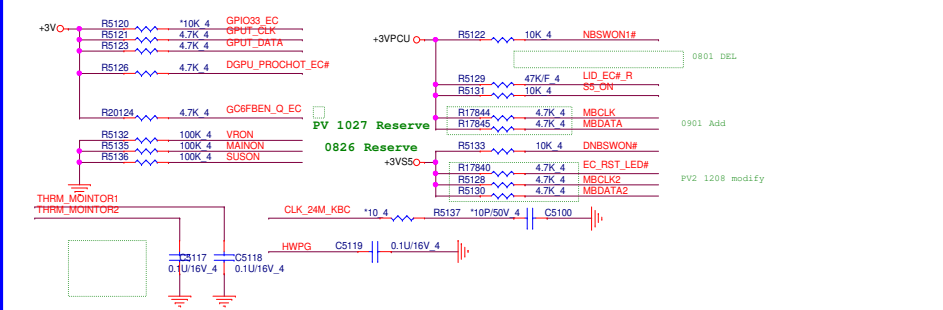
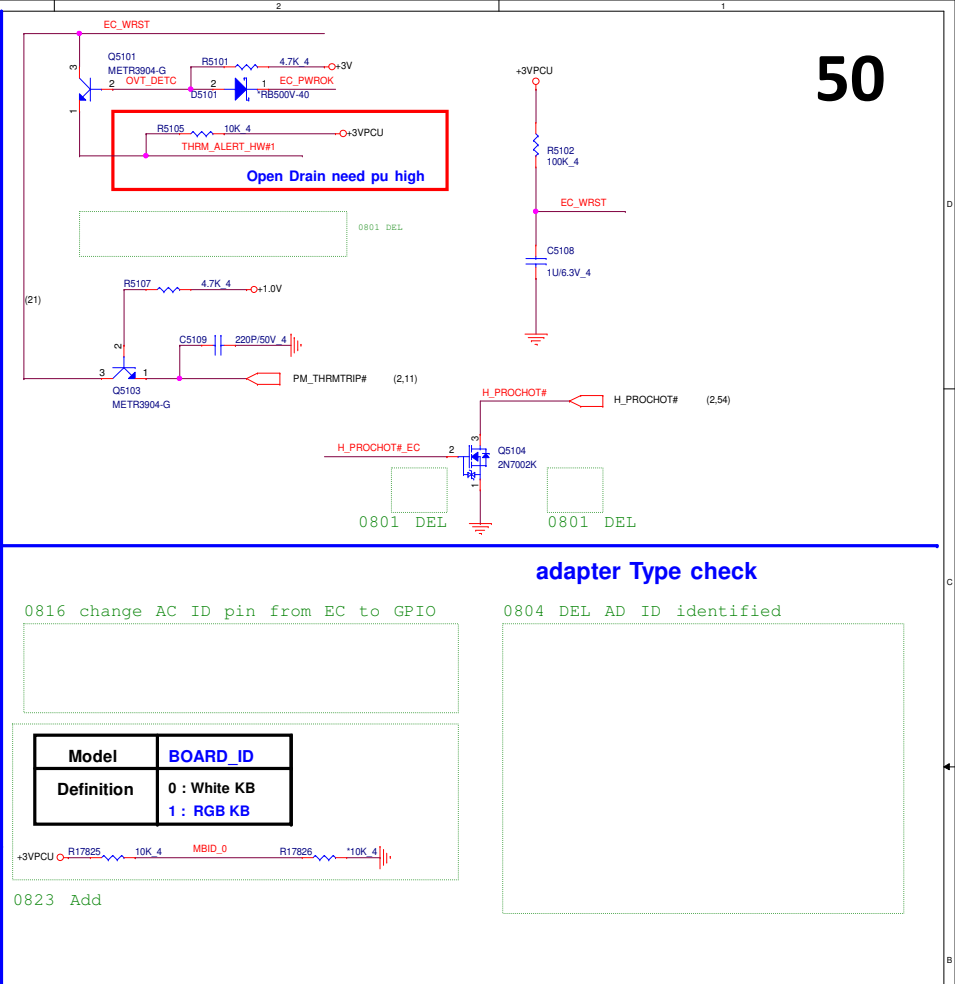
.....

QUOTE# 74

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L

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(9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,35,38,39,41,42,44,54,57,63,64)

**Need to CLOSE to EC pin**

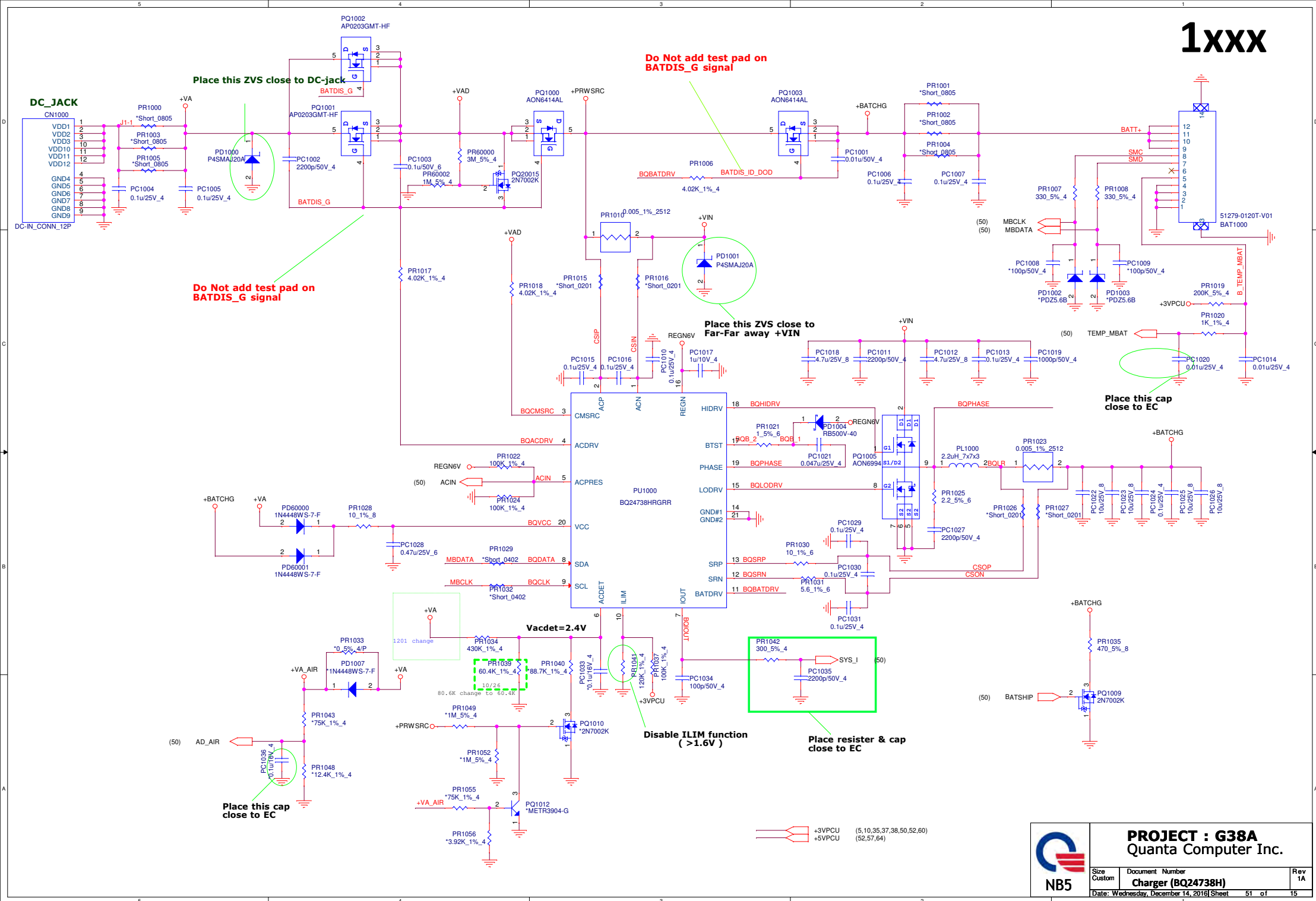


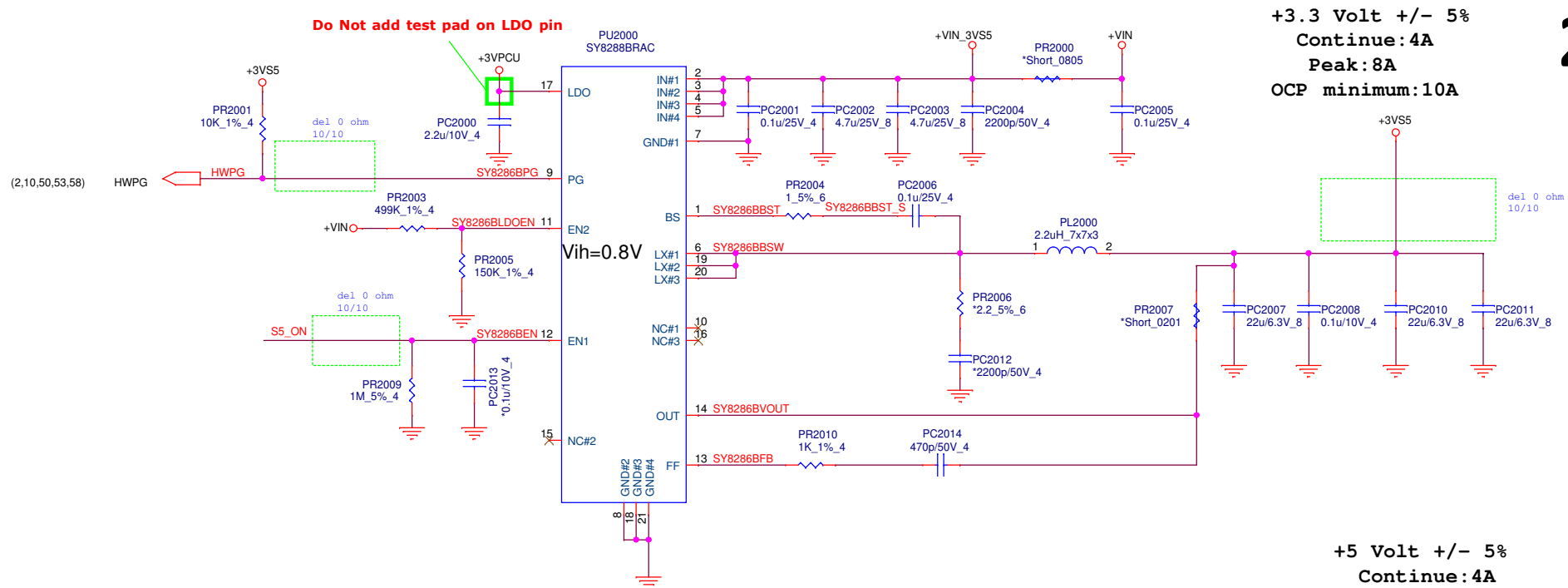
<b>Model</b>	<b>BOARD_ID</b>
<b>Definition</b>	0 : White KB 1 : RGB KB

	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
AC IN: AC mode Operation	H	L	<b>H</b>
AC remove: AC mode to DC mode	L	L	<b>L</b>
DC mode recover from PROCHOT	L	H	<b>H</b>

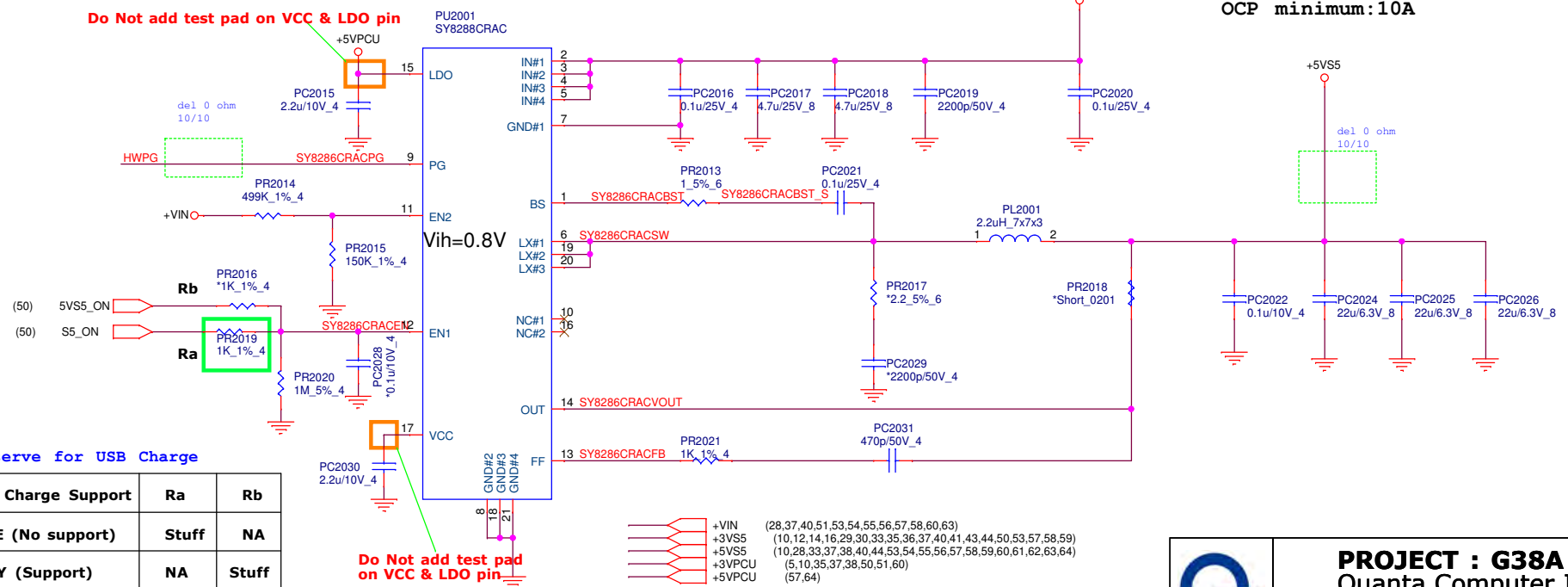


# 1xxx





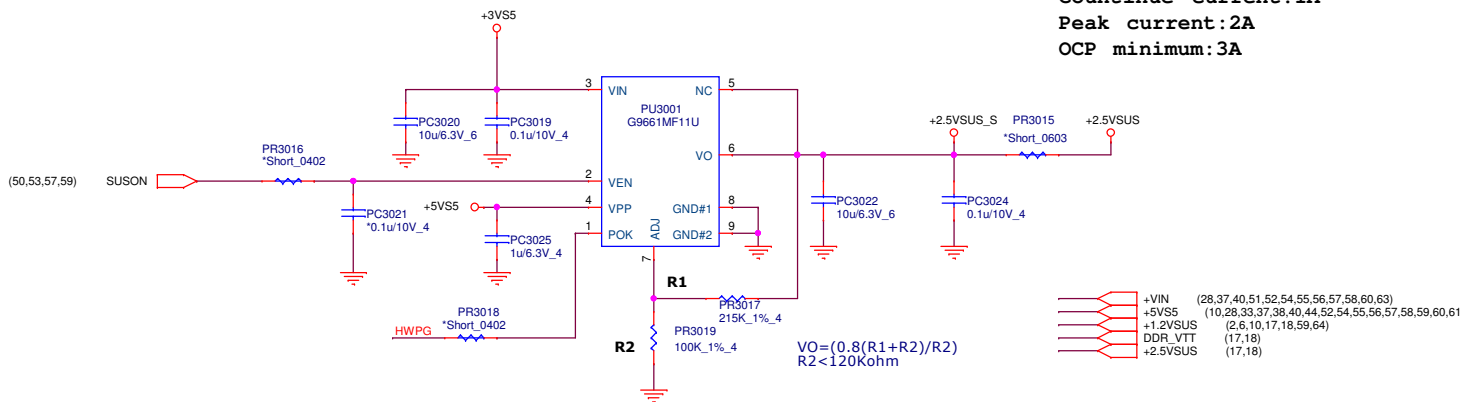
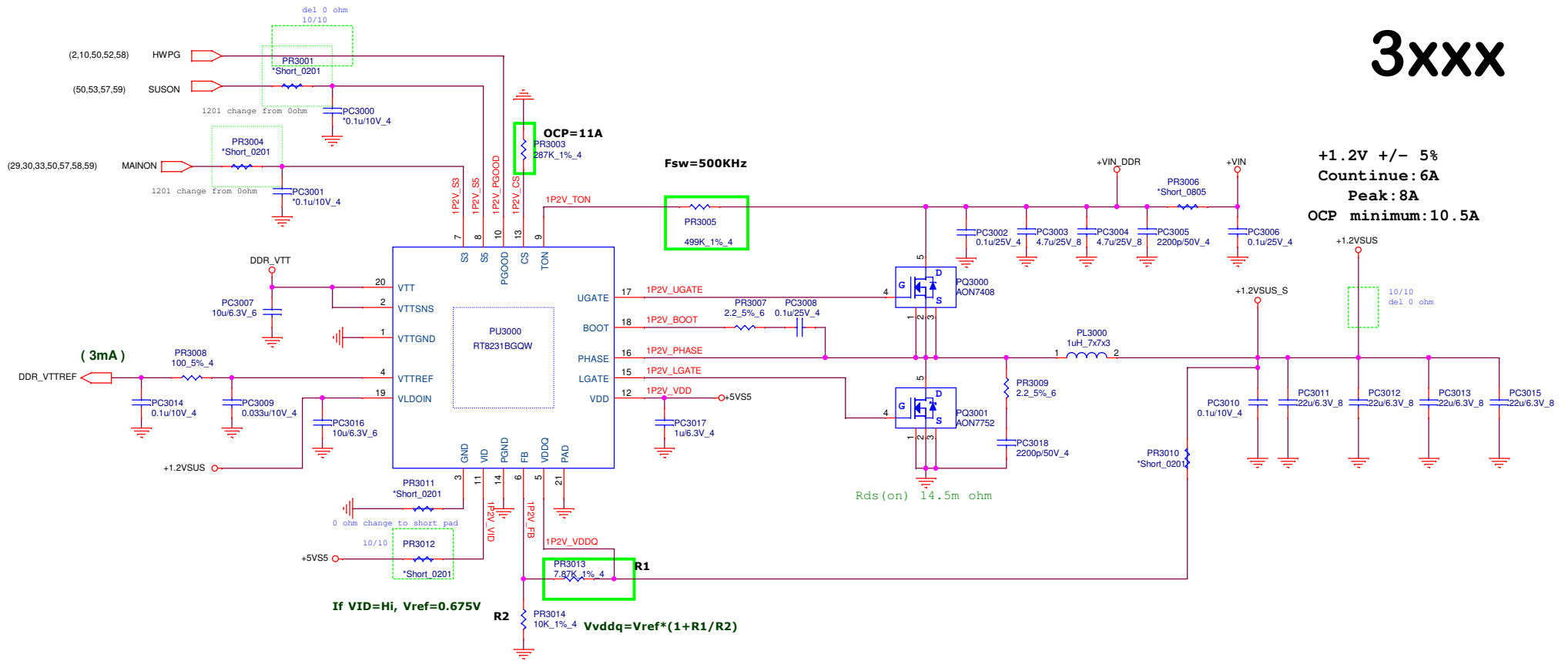
**2xxx**



**PROJECT : G38A**  
Quanta Computer Inc.

Reserve for USB Charge		
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

# 3xxx



0.61

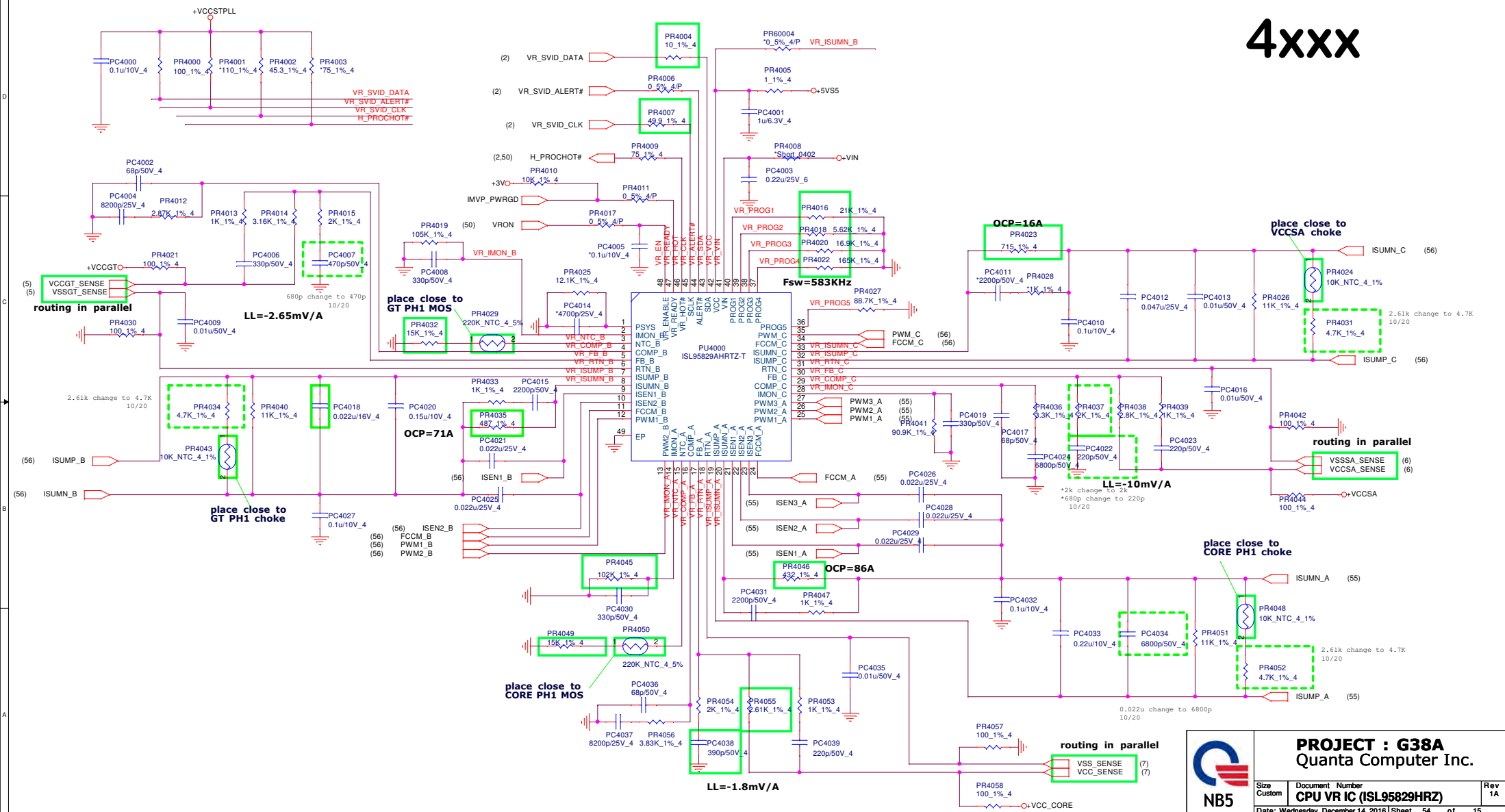
**PROJECT : G38A**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>DDR3 (RT8231B)</b>	<b>1A</b>

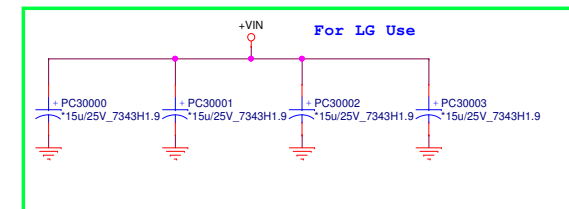
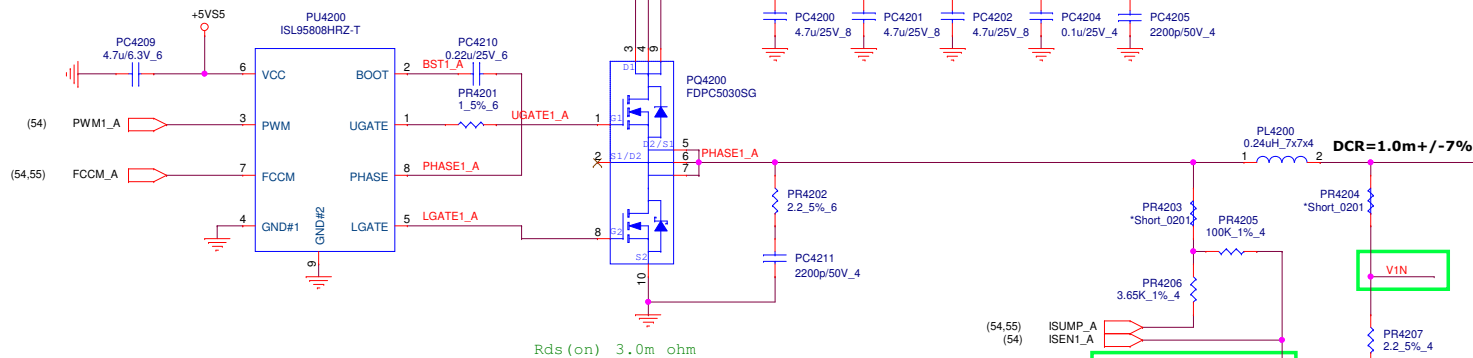
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NB5

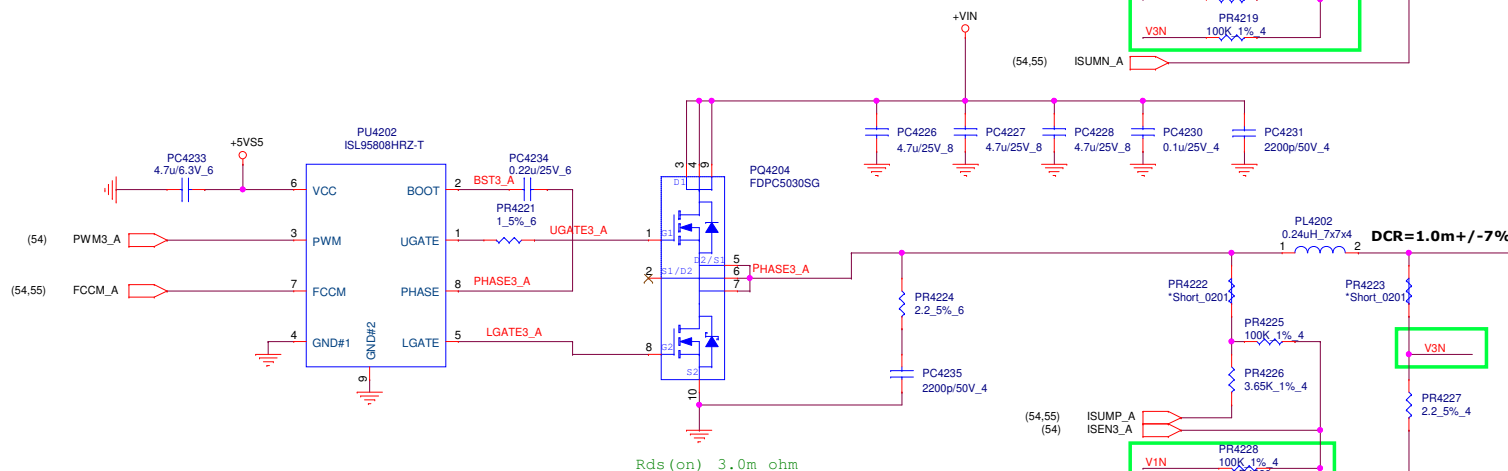
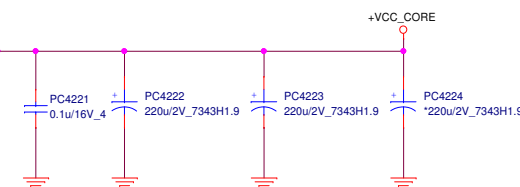
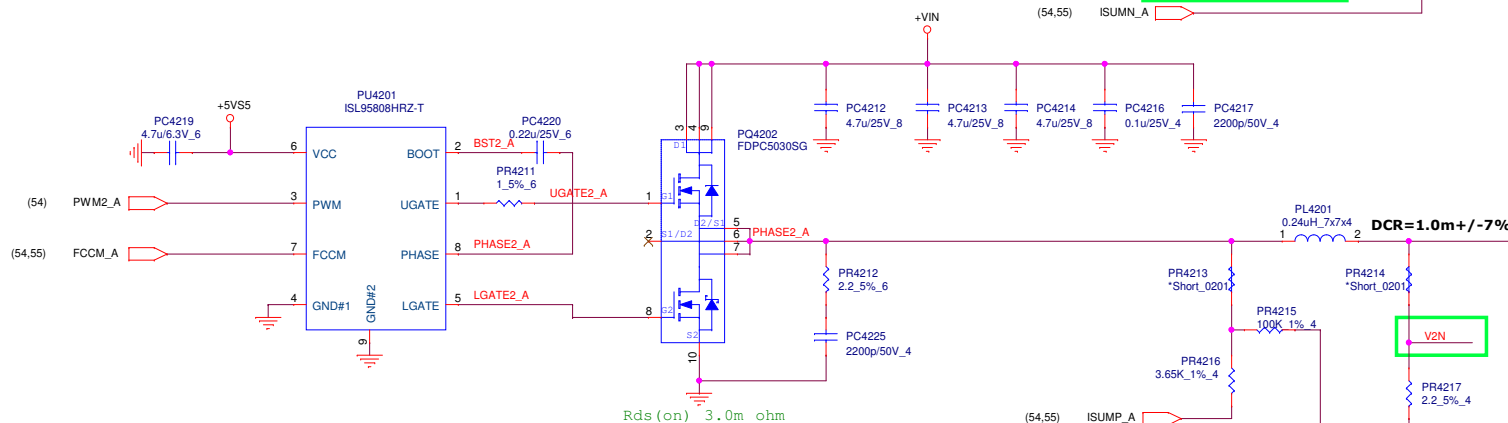
4xxx



# 4xxx



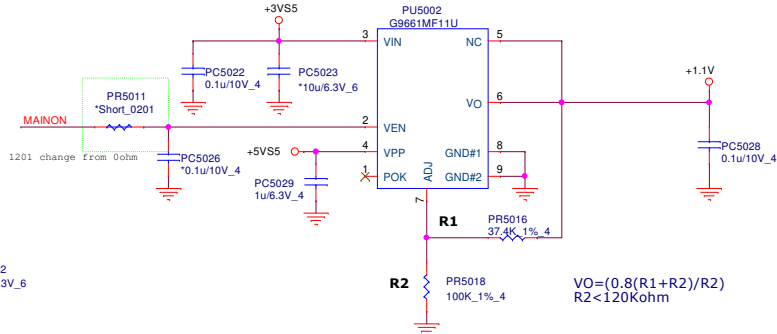
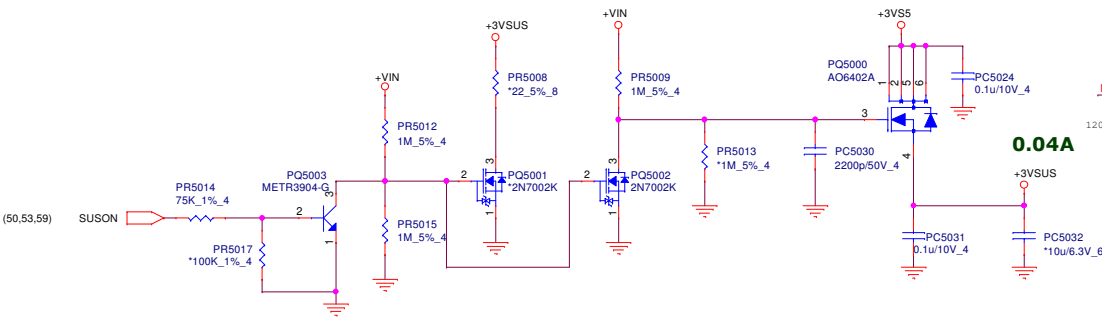
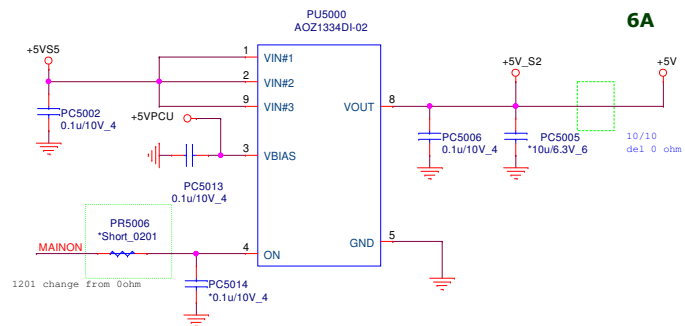
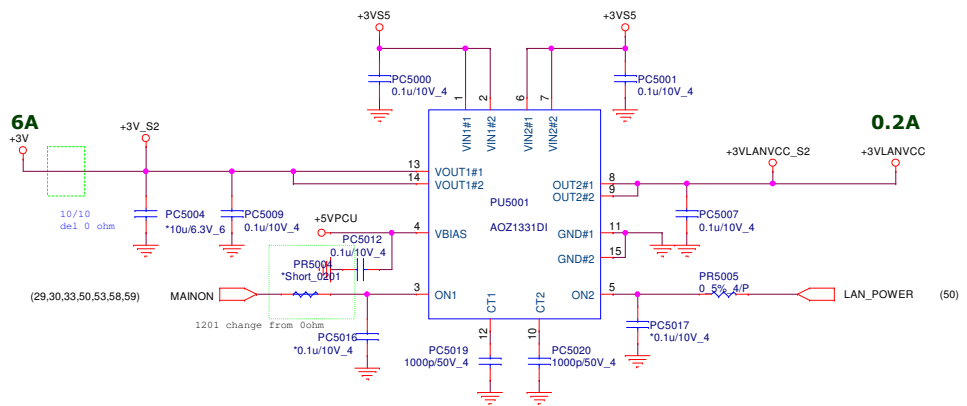
**H-line42 (45W)**  
**TDC: 50A**  
**Iccmax: 68A**  
**OCP: 86A**  
**Loadline = -1.8 mV/A**








5xxx



- +3V (9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,35,38,39,41,42,44,50,54,63,64)
- +5V (28,29,30,34,36,37,39,41,42)
- +3VS5 (10,12,14,16,29,30,33,35,36,37,40,41,43,44,50,52,53,58,59)
- +5VS5 (10,28,33,37,38,40,44,52,53,54,55,56,58,59,60,61,62,63,64)
- +3VSUS (39)
- +3VLANVCC (31)



**PROJECT : G38A**  
Quanta Computer Inc.

Size Custom	Document Number <b>Load switch IC (AOZ1331D)</b>	Rev 1A
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## Volume Segment

**Vcc\_ST: 0.12A**

**Vcc\_PLL: 0.12A**

**<= 10ms, full load ready**

(Vcc\_ST+Vcc\_PLL)

**Imax:0.24A**

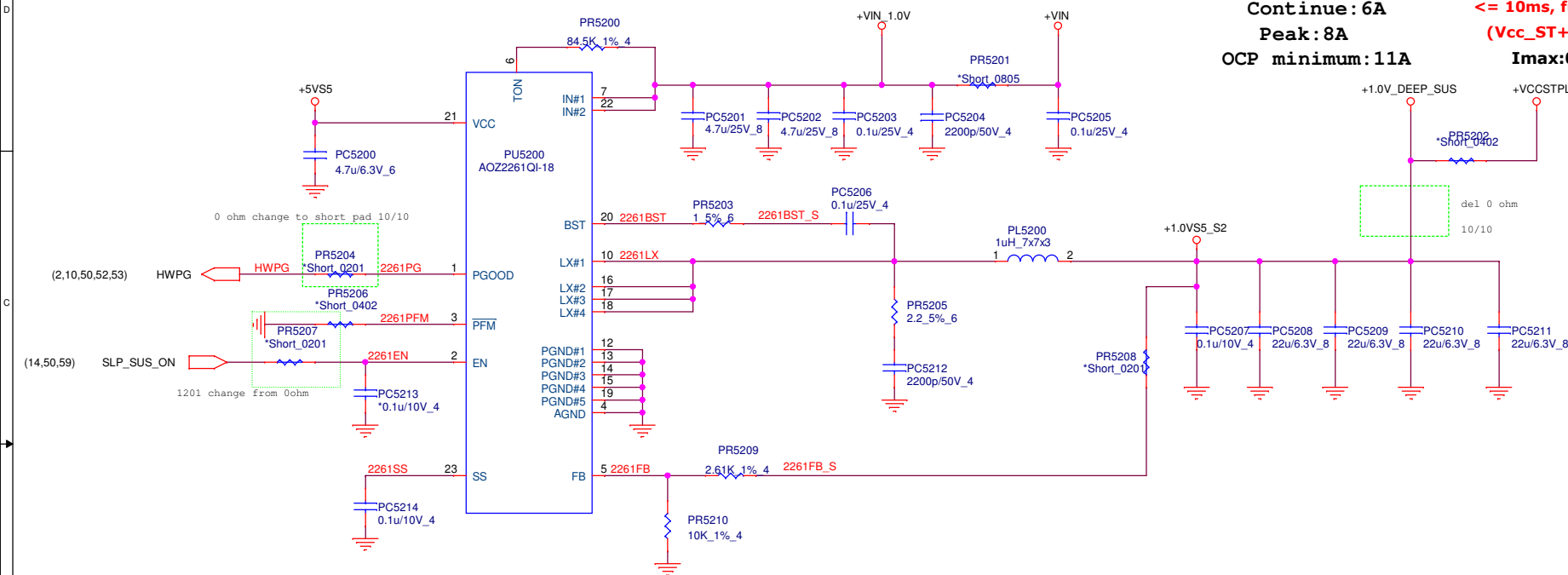
(V1.00A+V1.00\_MODPHY+VccPRIM\_CORE)

**+1.0VS5 Volt +/- 5%**

Continue: 6A

Peak : 8A

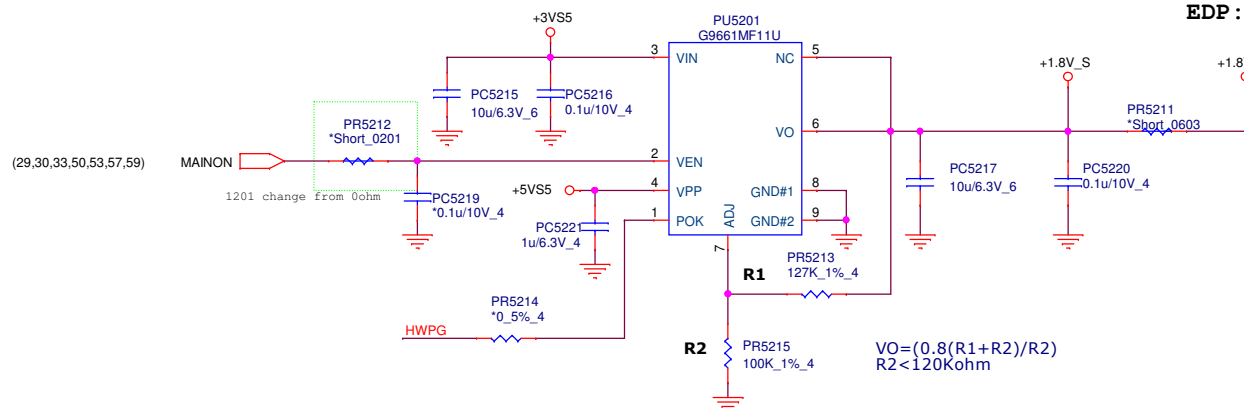
OCP minimum:11A



**+1.8V    +/- 5%**

TDC:1A

EDP : 2A



—	+VIN	(28,37,40,51,52,53,54,55,56,57,60,63)
—	+3VS5	(10,12,14,16,29,30,33,35,36,37,40,41,43,44,50,52,53,57,59)
—	+5VS5	(10,28,33,37,38,40,44,52,53,54,55,56,57,59,60,61,62,63,64)
—	+1.0V_DEEP_SUS	(10,11,14,59)
—	+1.8V	(22,64)
—	+VCCSTPLL	(2,6,54)
—	+1.1V	(29,57)



**PROJECT : G38A**  
Quanta Computer Inc.

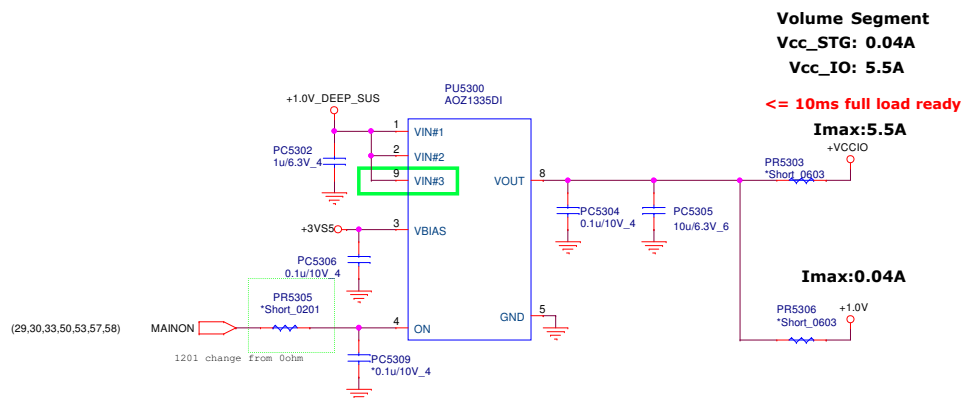
Size	Custom
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Document Number	<b>+1.0_DEEP_SUS</b>
-----------------	----------------------

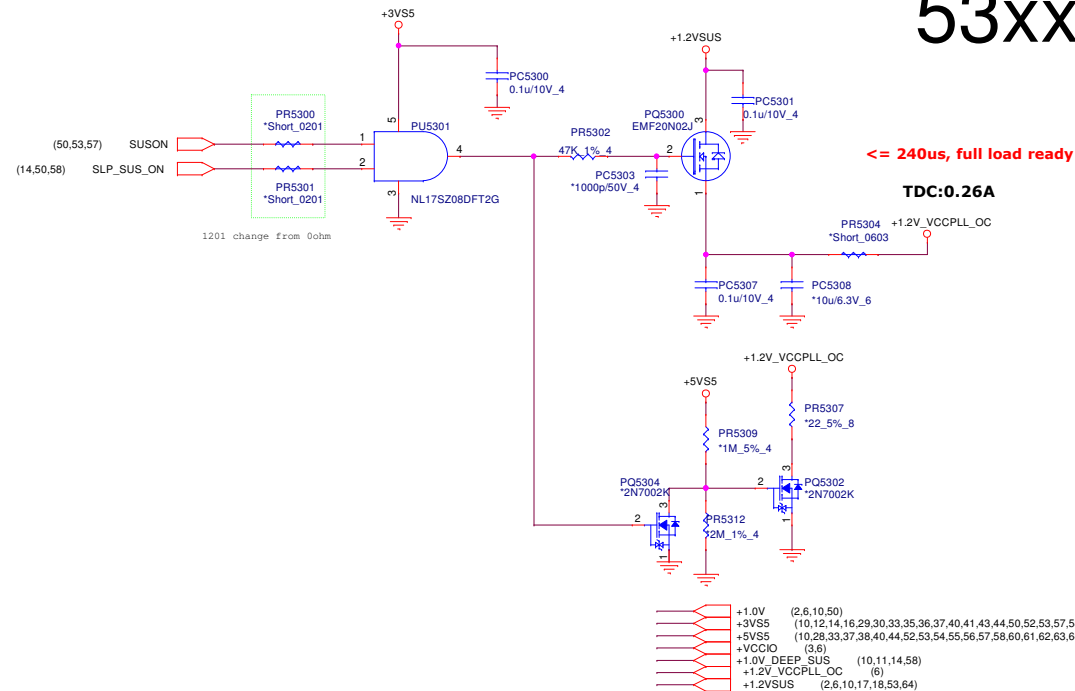
Rev	1A
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# 53xx



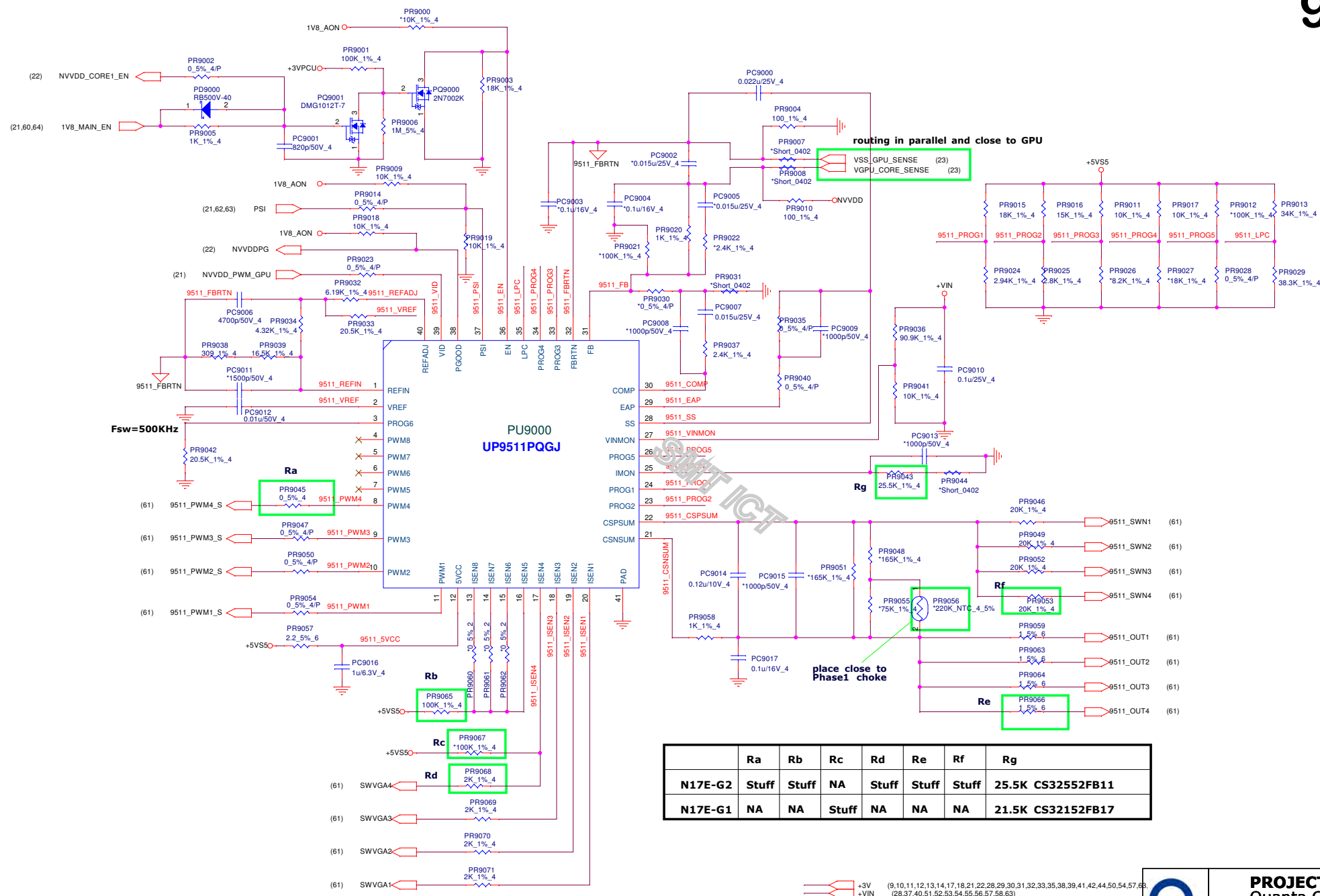
Reserve for separating +1.0V and VCCIO






**PROJECT : G38A**  
Quanta Computer Inc.

Size Custom	Document Number <b>+1.0V/+VCCSTPLL/+VCCIO</b>	Rev 1A
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	Ra	Rb	Rc	Rd	Re	Rf	Rg
N17E-G2	Stuff	Stuff	NA	Stuff	Stuff	Stuff	25.5K CS32552FB11
N17E-G1	NA	NA	Stuff	NA	NA	NA	21.5K CS32152FB17

- +3V (9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,35,38,39,41,42,44,50,54,57,63)
- +VIN (28,37,40,51,52,53,54,55,56,57,58,63)
- +SVS5 (10,28,33,37,38,40,44,52,53,54,55,56,57,58,59,61,62,63,64)
- 1V8\_AON (19,21,22,62,63,64)
- NVDD (23,61)
- 1V8\_MAIN\_EN (21,60,64)



**PROJECT : G38A**  
Quanta Computer Inc.

Size Custom	Document Number <b>+VGACORE (RT8813C)</b>	Rev 1A
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**For Acoustic**

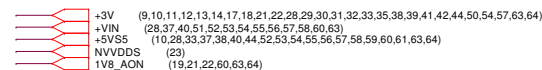


**N17E-G2 (82W)**  
**EDP: 85A**  
**EDP peak: 203A**  
**OCP minimum 245A**

**N17E-G1 (65W)**  
**EDP: 60A**  
**EDP peak: 127A**  
**OCP minimum 197A**

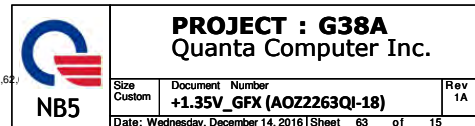


Size Custom	Document Number <b>+VCORE (NCP81151)</b>	Rev 1A
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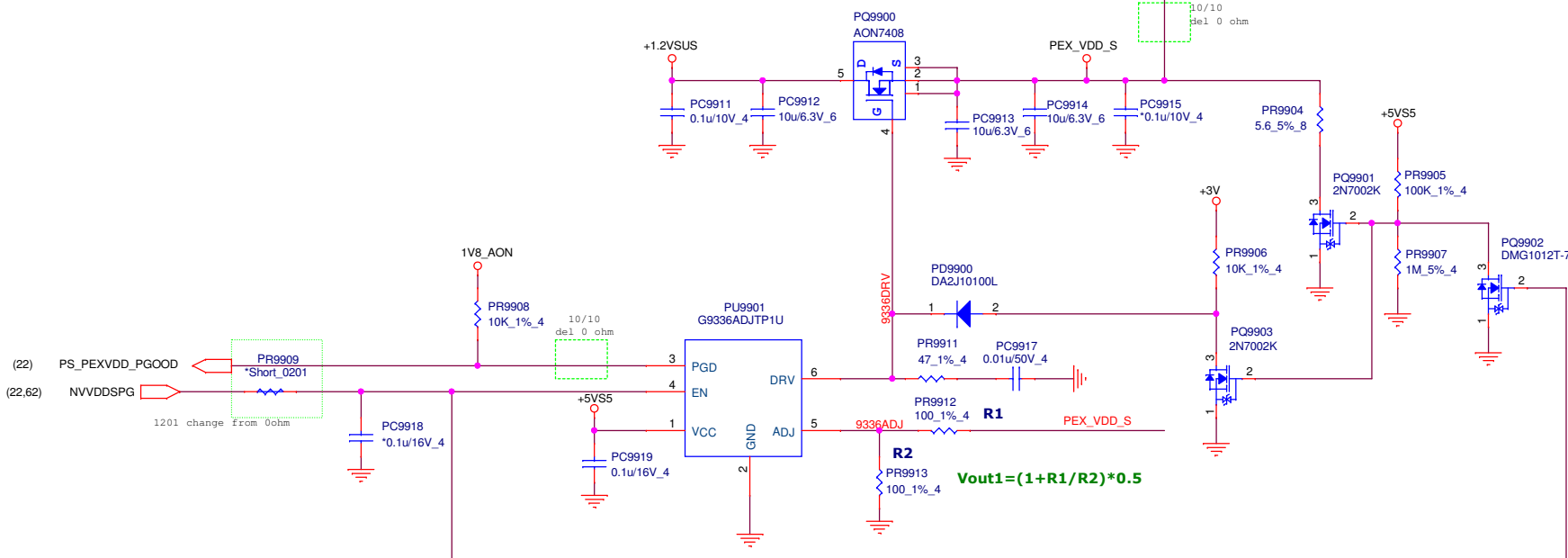
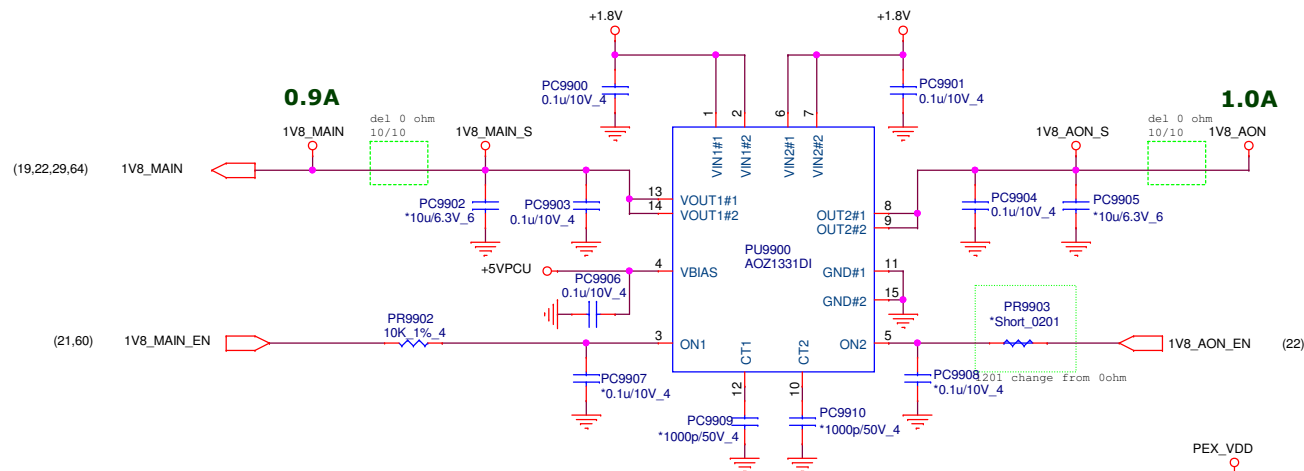
1.35V/1.55V +/- 5%  
**N17E-G2 (82W)**  
 EDP: 25A  
 EDP: peak: 30.6A  
 OCP minimum: 40A

**N17E-G1 (65W)**  
 EDP: 19.8A  
 EDP: peak: 32.2A  
 OCP minimum: 42A





# 99xx



+VIN	(28,37,40,51,52,53,54,55,56,57,58,60,63)
+3VS5	(10,12,14,16,29,30,33,35,36,37,40,41,43,44,50,52,53,57,58,59)
+5VS5	(10,28,33,37,38,40,44,52,53,54,55,56,57,58,59,60,61,62,63)
1V8_MAIN	(19,22,29,64)
1V8_AON	(19,21,22,60,62,63)
+1.2VSUS	(2,6,10,17,18,53,59)
PEX_VDD	(19,21)

**PROJECT : G38A**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>+3V/+1.05V_GFX(AOZ1331DI)</b>	Rev 1A
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