

LCFC Confidential


DG421/DG521/DG721 MB Schematics Document

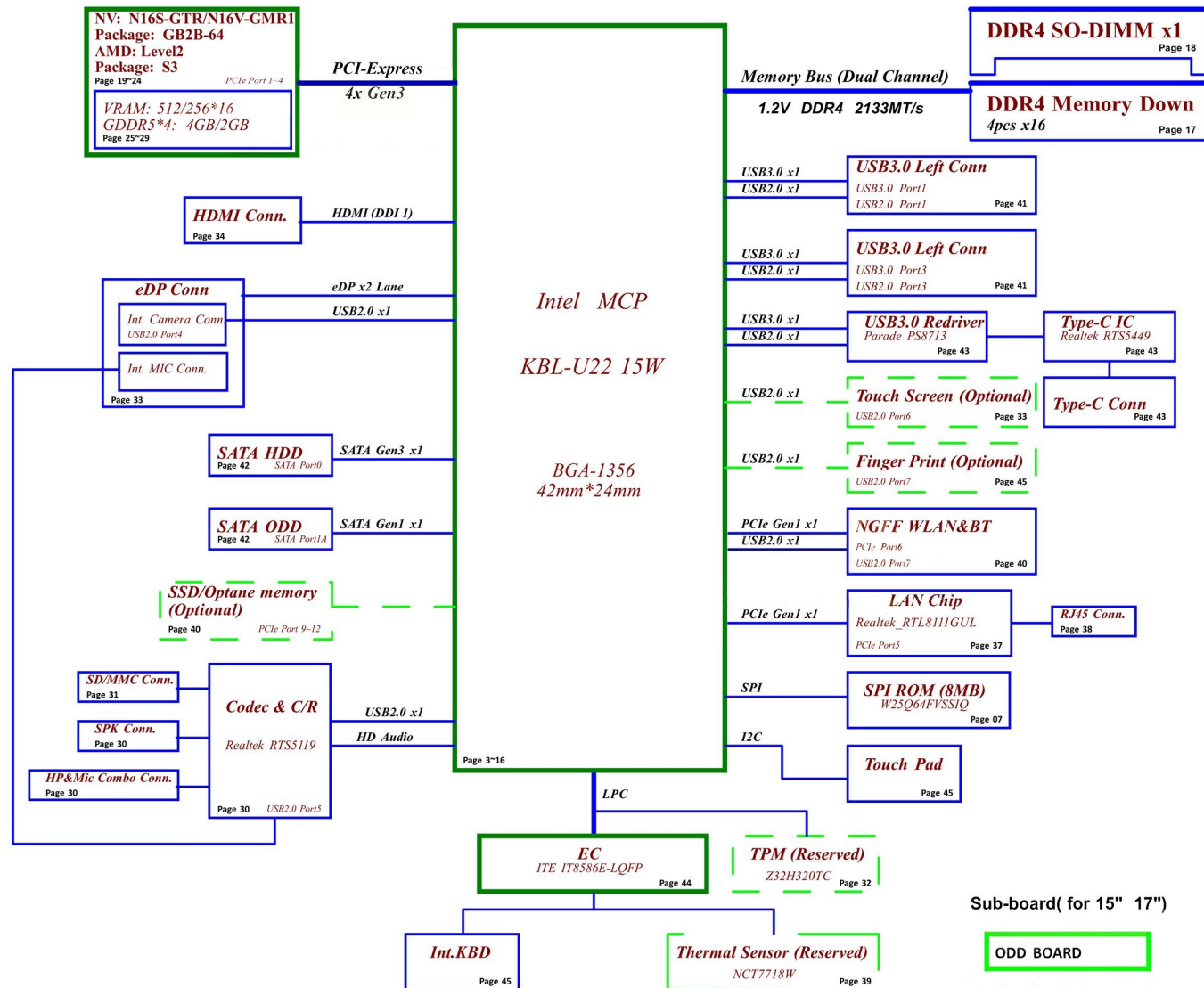
Kabylake-U22 with DDR4 + Nvidia N16S-GTR/N16V-GMR1 GPU

2017-01-18

REV:1.0

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function
USB3.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 NC
	5 NC
	6 NC
USB2.0	1 USB3.0 Conn Left
	2 USB Type-C
	3 USB3.0 Conn Left
	4 Finger Print
	5 Cardreader
	6 Touch Panel
	7 Bluetooth
	8 Camera
	9 NC
	10 NC
PCIE	1~4 X4 PCIE DGPU
	5 LAN
	6 WLAN
	7 SATA HDD
	8 SATA ODD
	9~12 X4 PCIE Optane Memory
	0 HDD
	1A ODD
SATA	1B used as PCIE
	2 used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
DIS@	For GPU part
OPT@	For NV GPU part
PX@	For AMD GPU part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAM rank part
DUALRANK@	For dual VRAM rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part

SMBUS Control Table

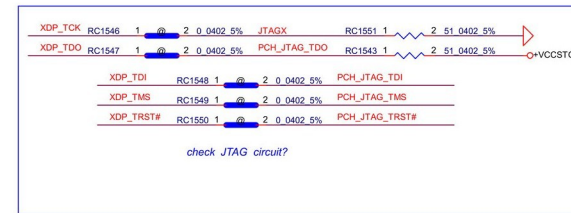
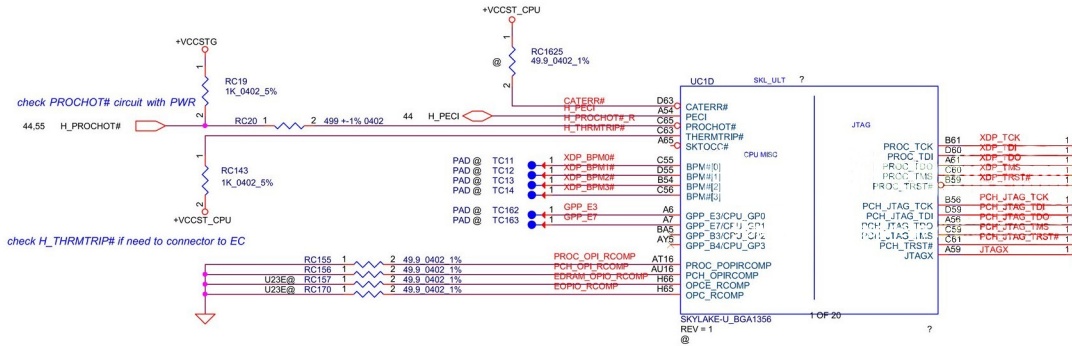
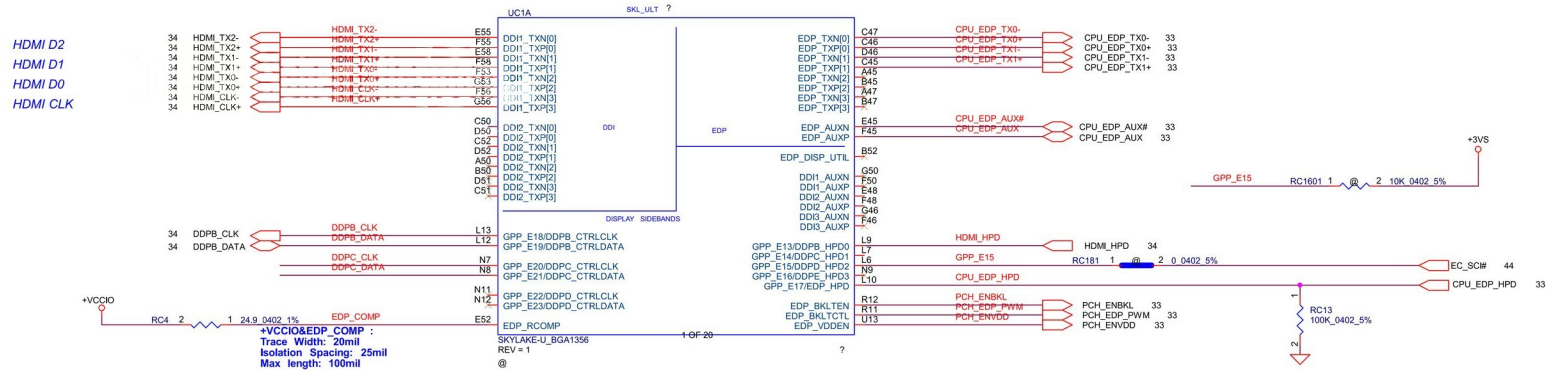
	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1	IT8586E	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_DA1	+3VL_EC										
EC_SMB_CK2	IT8586E	X	X	V	V +3VL_EC	X	V	X	X	V	X
EC_SMB_DA2	+3VS										
EC_SMB_CK3	IT8586E	X	X	X	V	X	X	V	X	X	X
EC_SMB_DA3	+3VL_EC										
PCH_SMB_CLK	PCH	X	X	X	X	X	V	X	V	X	V
PCH_SMB_DATA	+3VALW_PCH										

EC SMBus1 address	EC SMBus2 address	EC SMBus3 address	PCH SM Bus address
Device Address	Device Address	Device Address	Device Address
Smart Battery need to update	Thermal Sensor(NCT7718W) 1001_100xb	PMIC need to update	DDR4 SODIMM need to update
Charger 0001 0010 b	PCH need to update	DGPU need to update	Wlan Reserved

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HDMI D2
HDMI D1
HDMI D0
HDMI CLK




DDP_CTRLDATA strapping sampled on the rising edge of PWROK

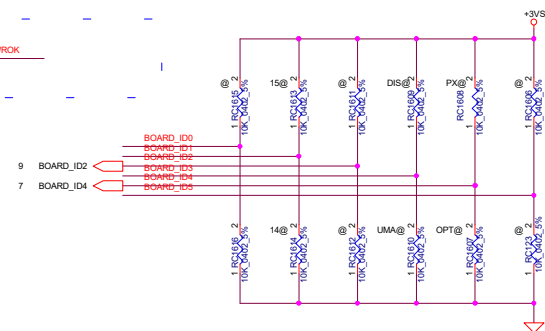
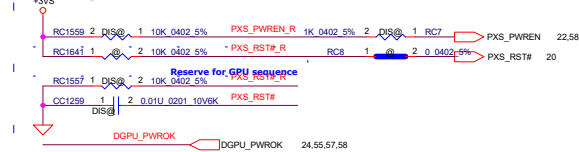
Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC



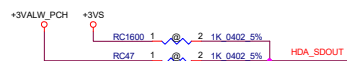
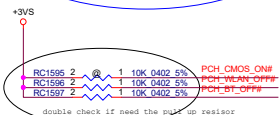
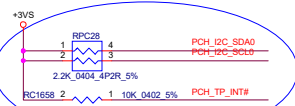
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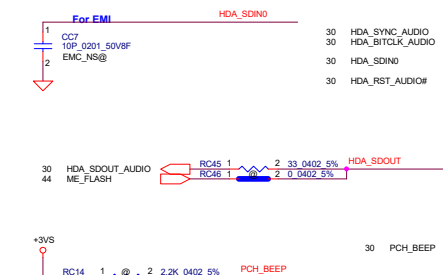
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	MCP (DDR4)		
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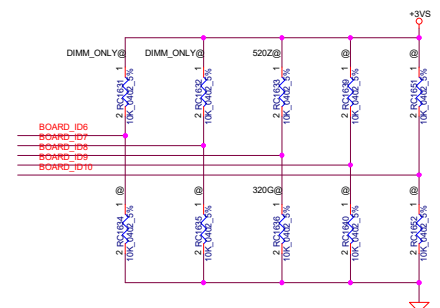
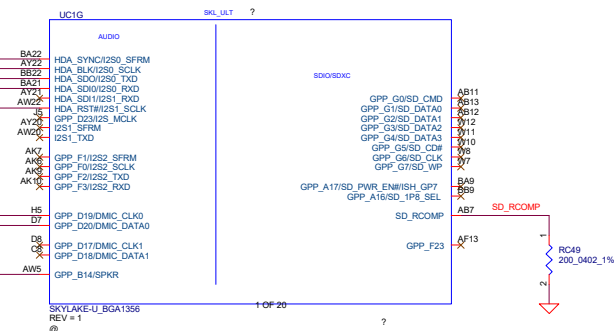
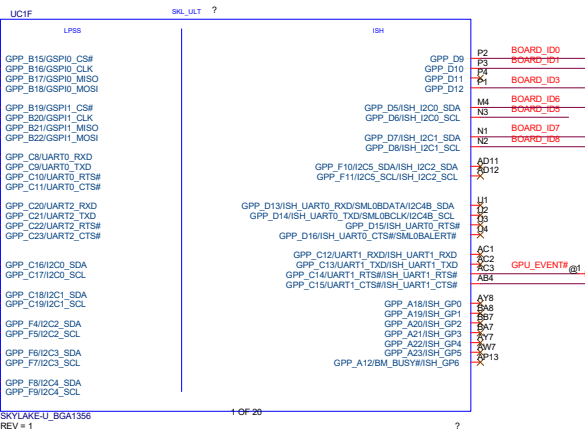
Board ID	Description	Stuff R
Board_ID[0:1]	00 14"	RC1616 RC1616
	01 15"	RC1616 RC1616
	10 17"	RC1615 RC1616
	11 Reserved	RC1615 RC1613
Board_ID2	0 Reserved	RC1612
Board_ID3	1 Reserved	RC1611
	0 UMA	RC1610
	1 DIS	RC1609
Board_ID4	0 NV GPU	RC1607
	1 AMD GPU	RC1608
Board_ID5	0 Reserved	RC1213
	1 Reserved	RC1606



HDA_SDO This signal has a weak internal pull-down.
 0 = Enable security measures defined in the Flash Descriptor.
 1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.

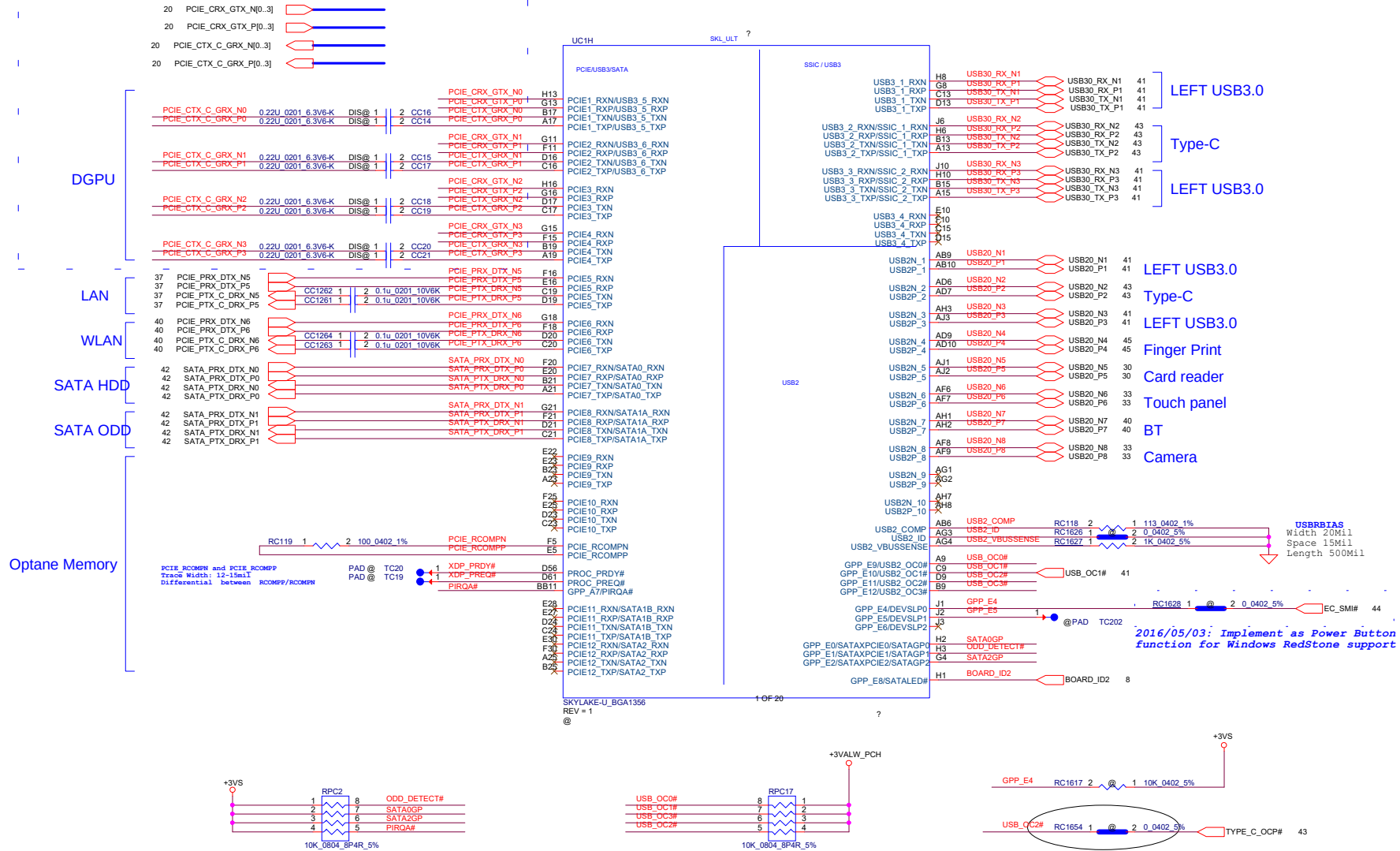


Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable "Top Swap" mode. (Default) ★ 1 = Enable "Top Swap" mode.	0	Rising edge of PCH_PWROK
GPIO1 MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable "No Reboot" mode. (Default) ★ 1 = Enable "No Reboot" mode	0	Rising edge of PCH_PWROK
GPIO1 MOSI /GPP_B22	Boot BIOS Strap Bit	Internal PD 0 = SPI (Default) ★ 1 = LPC	0	Rising edge of PCH_PWROK



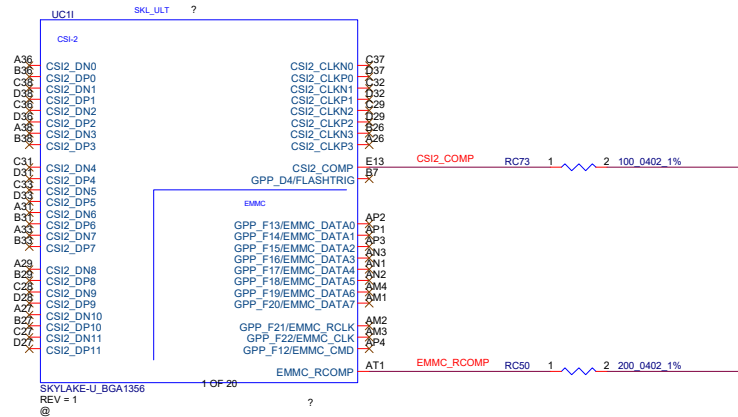
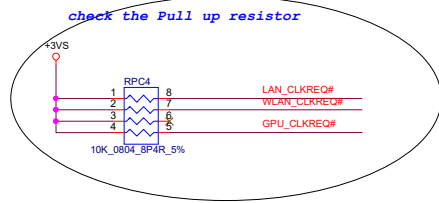
Board ID	Description		Stuff R	
Board ID [6,7]	00	Samung SGB 2400 MT/s	RC1634	RC1635
	01	Hynix SGB 2400 MT/s	RC1634	RC1632
	10	Micron SGB 2400 MT/s	RC1631	RC1635
	11	SO-DIMM Only	RC1631	RC1632
Board_ID8	0	320G	RC1636	
	1	520Z	RC1633	
Board_ID9	0	Reserved	RC1640	
	1	Reserved	RC1639	
Board_ID10	0	Reserved	RC1652	
	1	Reserved	RC1651	

@DIS For NV and AMD GPU SKU



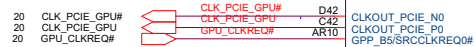
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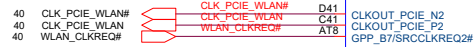
@DIS For NV and AMD GPU SKU

PCIE CLK0 DGPU

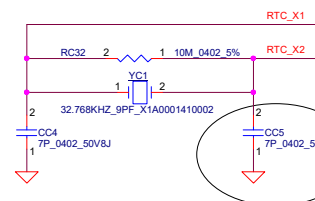
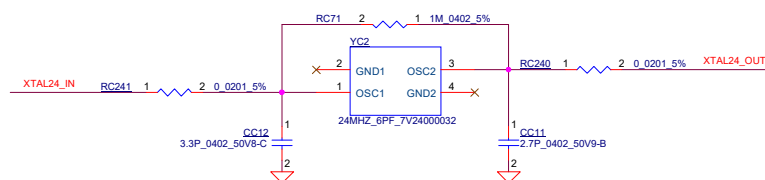
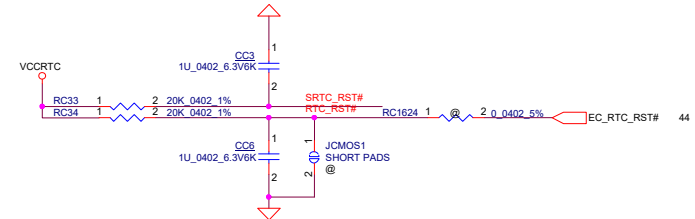
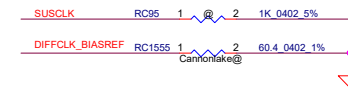
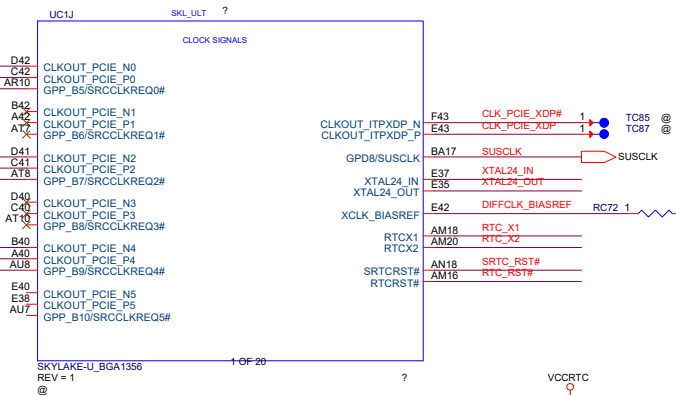
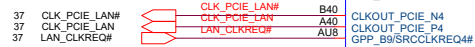


Optane memory

PCIE CLK5 WLAN



PCIE CLK4 LAN

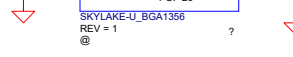
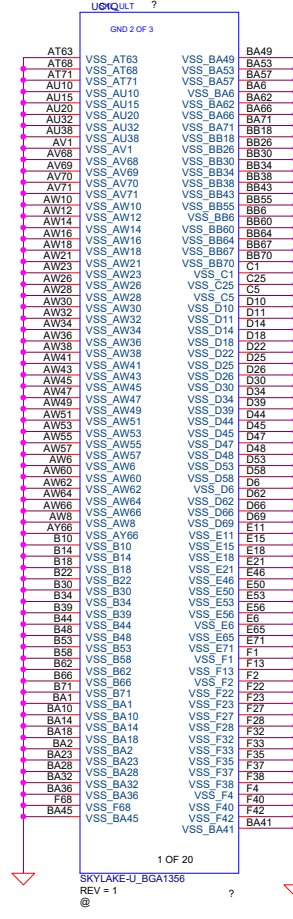


when single end external clock generator used, this pin should be grounded



need to use 38.4MHz (30ohm) for Cannonlake-u

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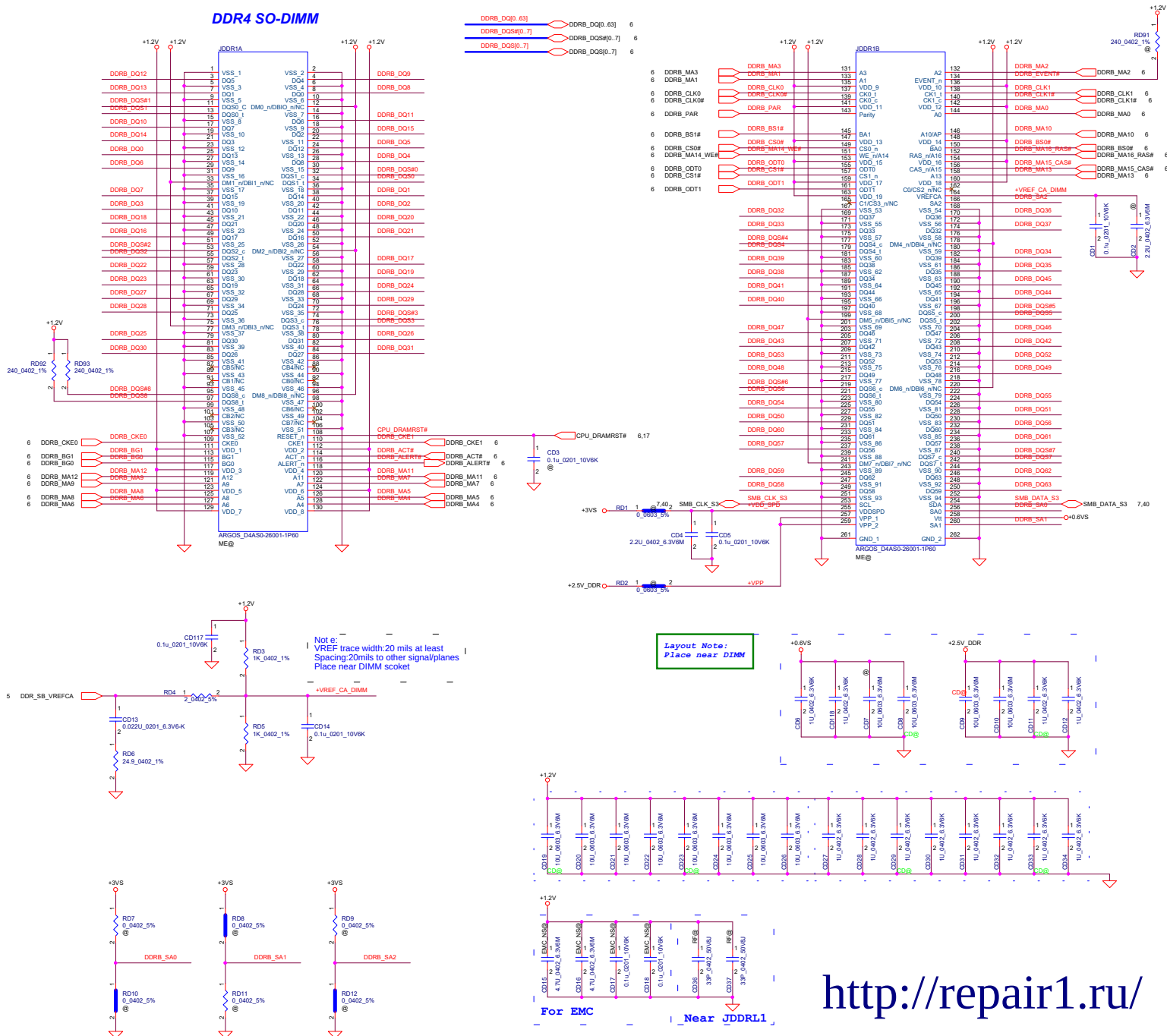
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DDR4 SO-DIMM



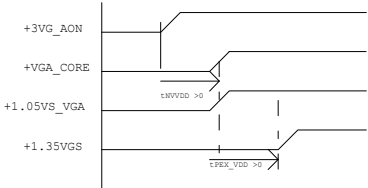
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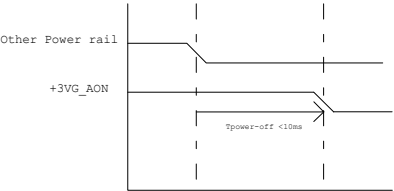
N16x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing--3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

N15V-GM Power Sequence



1. all power rail ramp up time should be larger than 40us-4ms



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

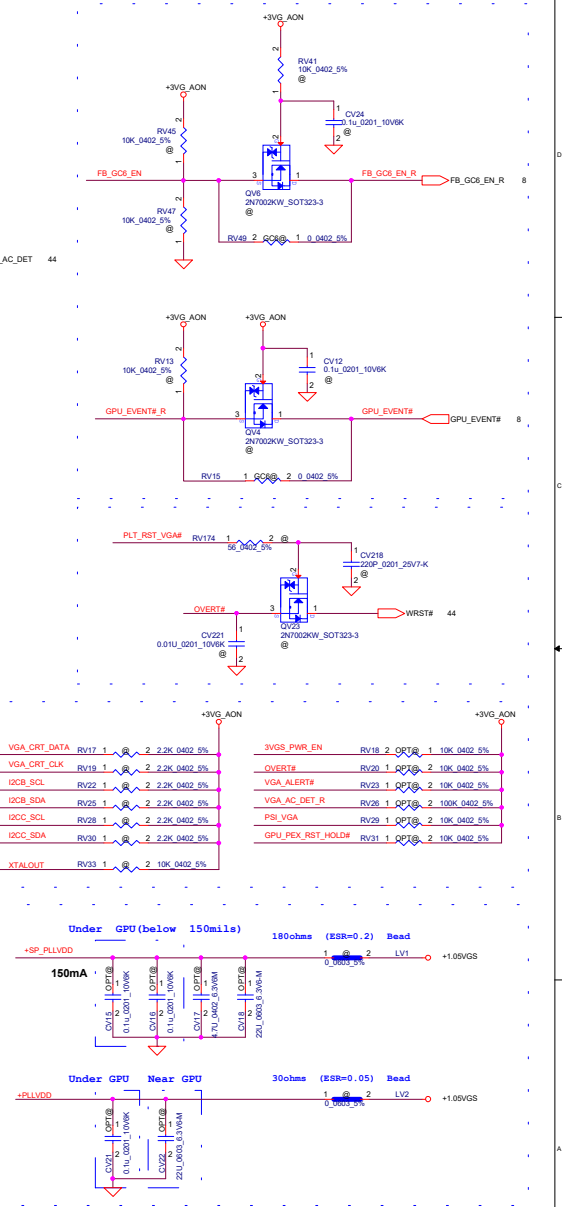
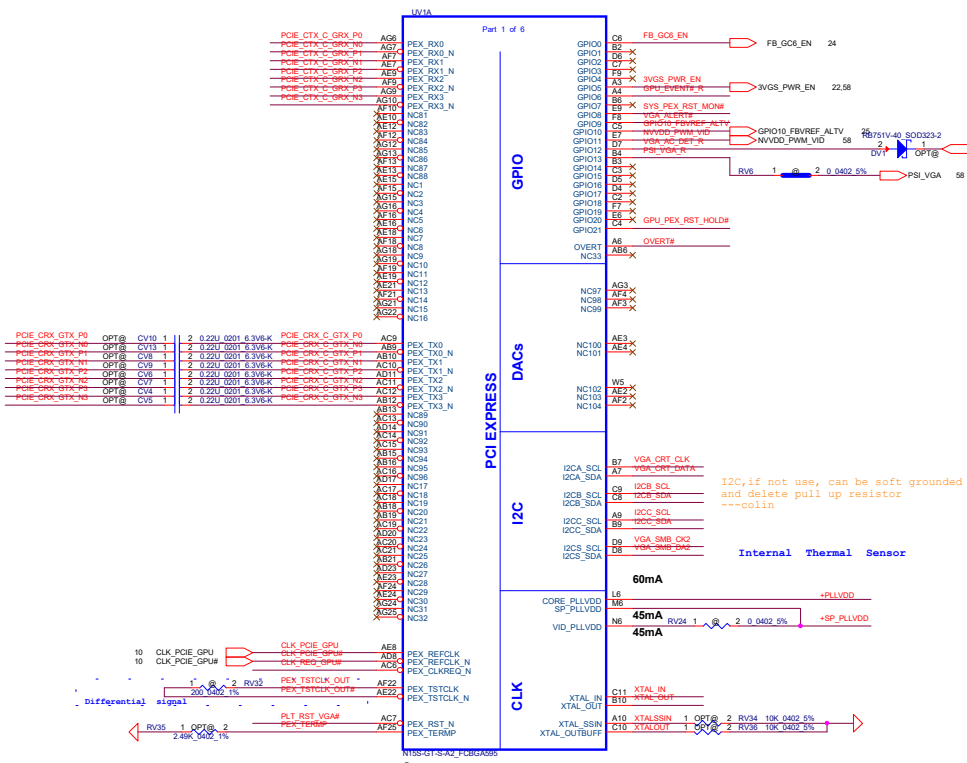
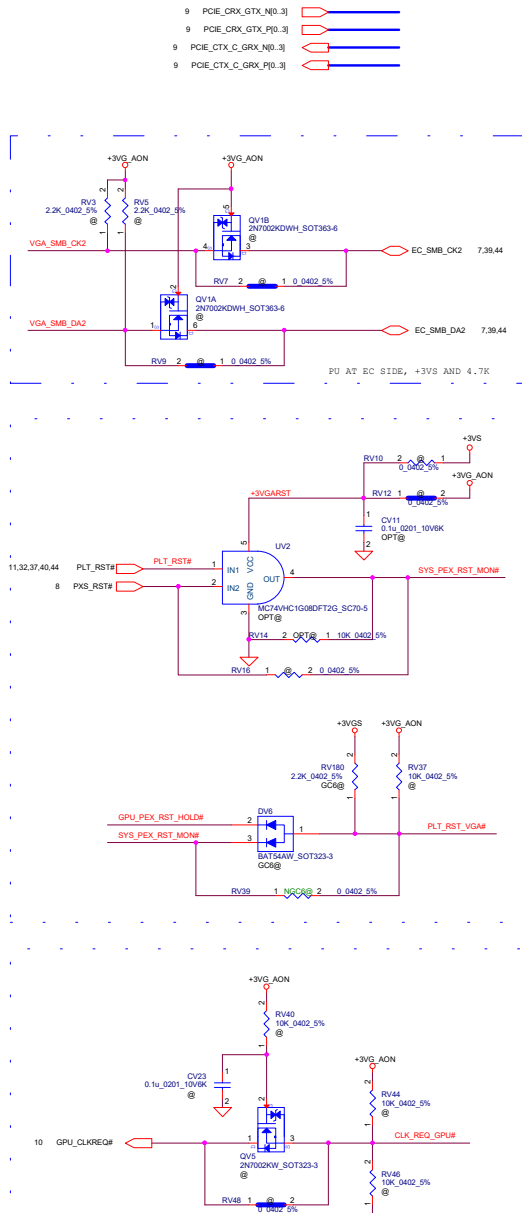
Products	GPU (W)	Mem (W)	Min Core Clk (MHz)	(V)	(A)	(W)	FBVDD (1.35V) (A)	(W)	FBVDDQ (GPU+Mem) (1.35V) (A)	(W)	(1.05V) (6) (mA)	(W)	Other (3.3V) (mA)	(W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS				
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

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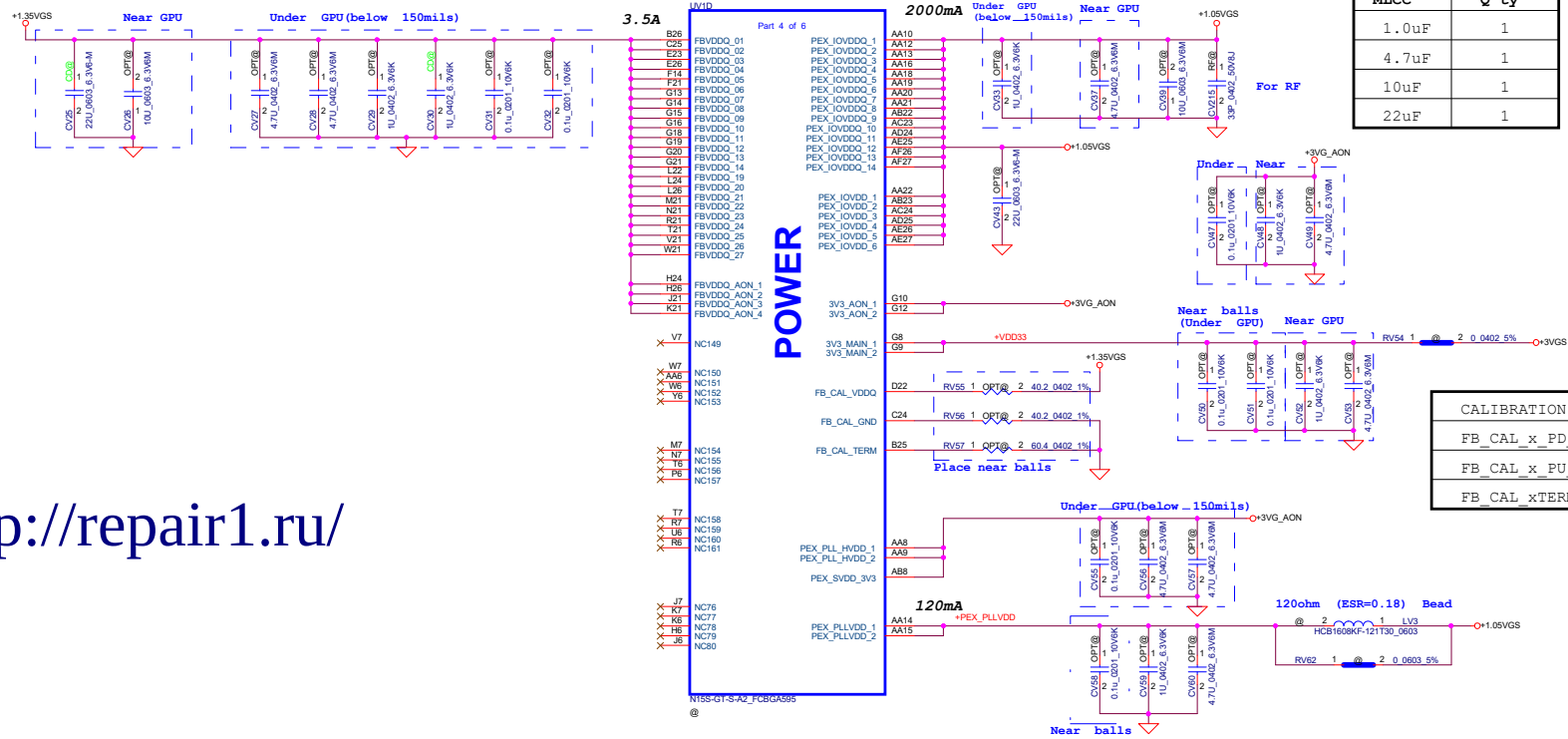
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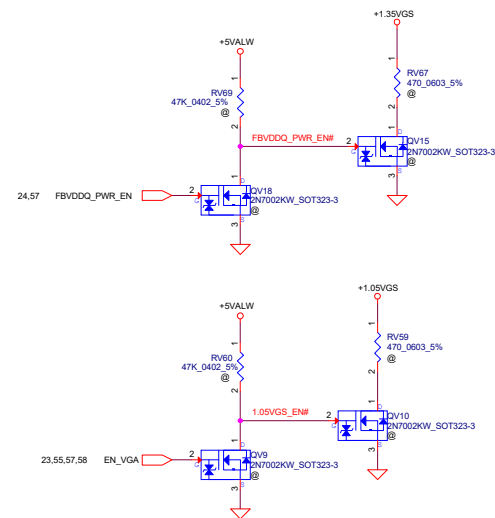
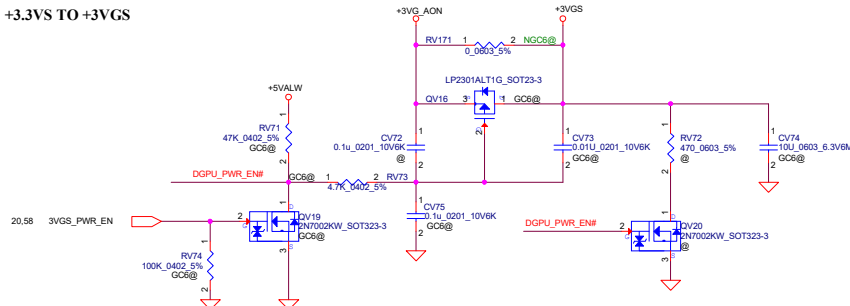
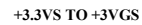
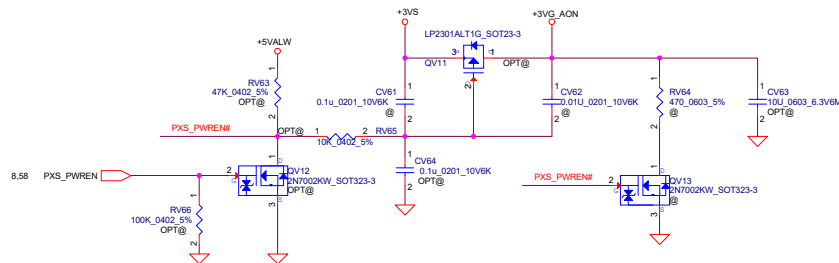
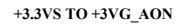
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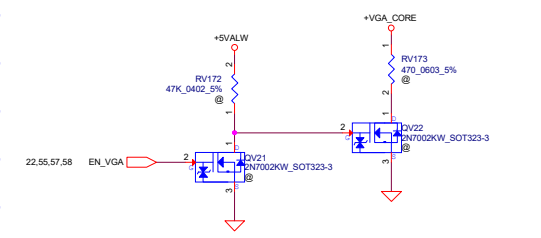
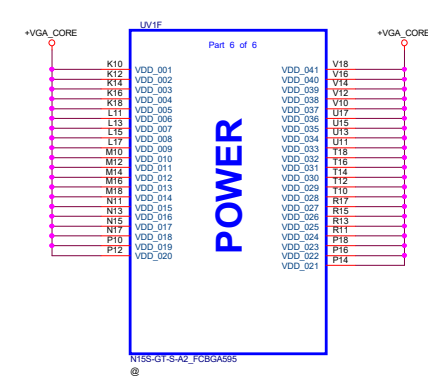
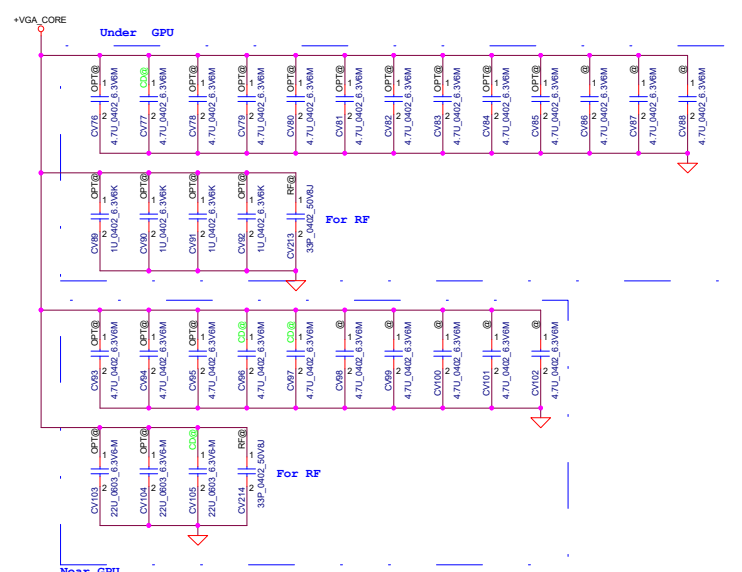
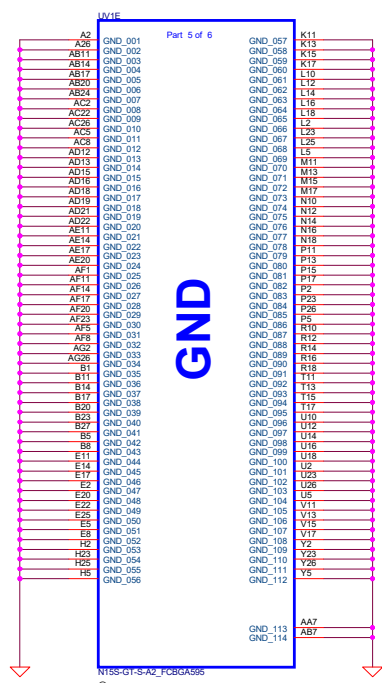


PEX_I0VDD/Q	Decoupling
MLCC	Q'ty
1.0uF	1
4.7uF	1
10uF	1
22uF	1

CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm



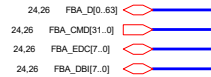
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Issued Date		Deciphered Date		N16X Power			
2015/08/20		2016/08/20		Size Document Number DC421		Rev 1.0	
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Date		Sunday, January 23, 2017		Sheet		22 of 60	



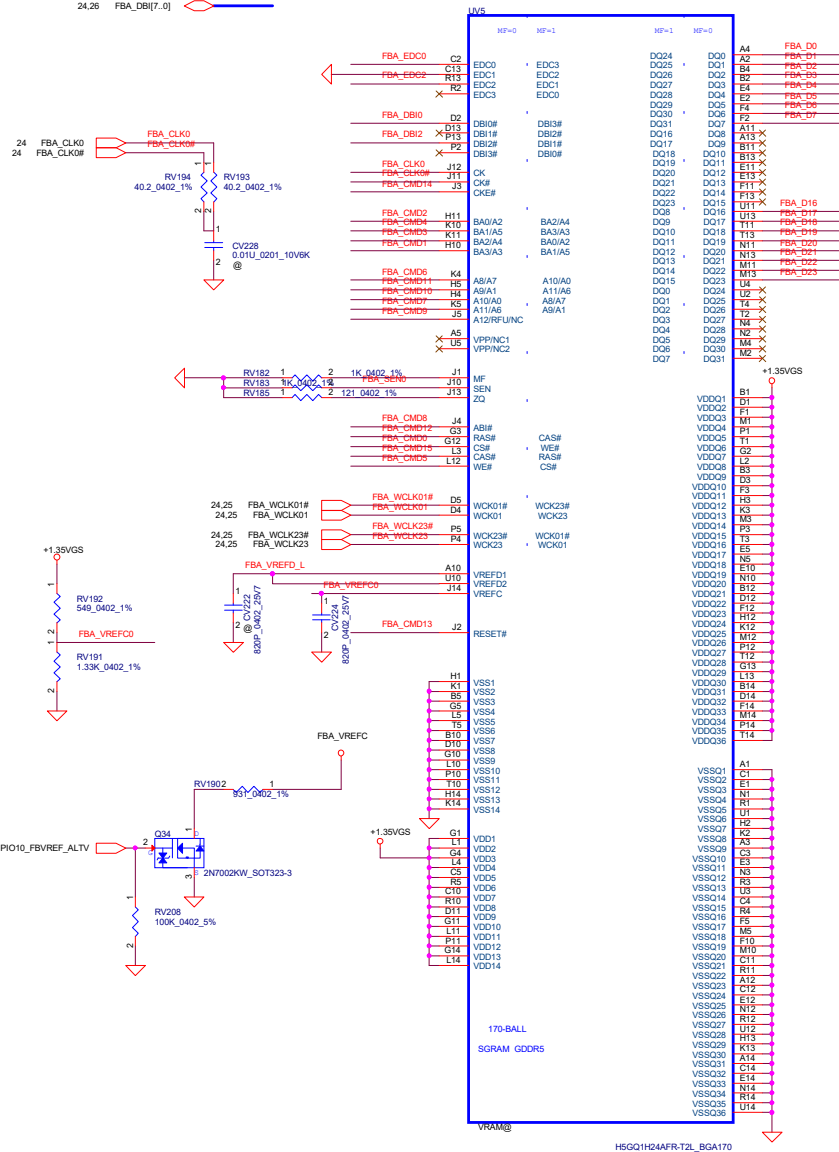
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Security Classification		LC Future Center Secret Data		Title	
Issued Date		2015/08/20		Deciphered Date	
		2016/08/20		N16X_+VGA CORE, GND	
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Size		Document Number		Rev	
		DG421		1.0	
Date		Sunday, January 22, 2017		Sheet 23 of 60	

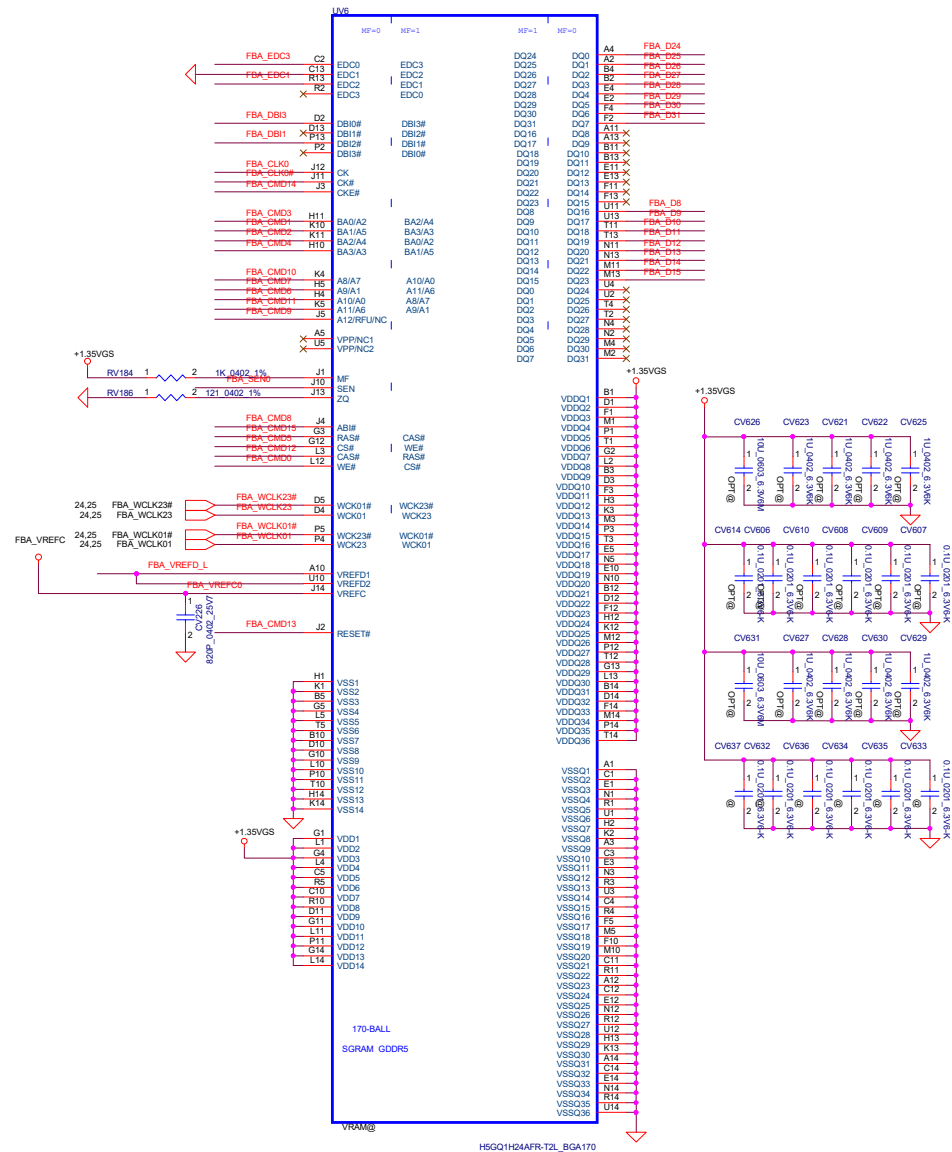
Lower 32 bits



MF=0 No Mirror



MF=1 Mirror



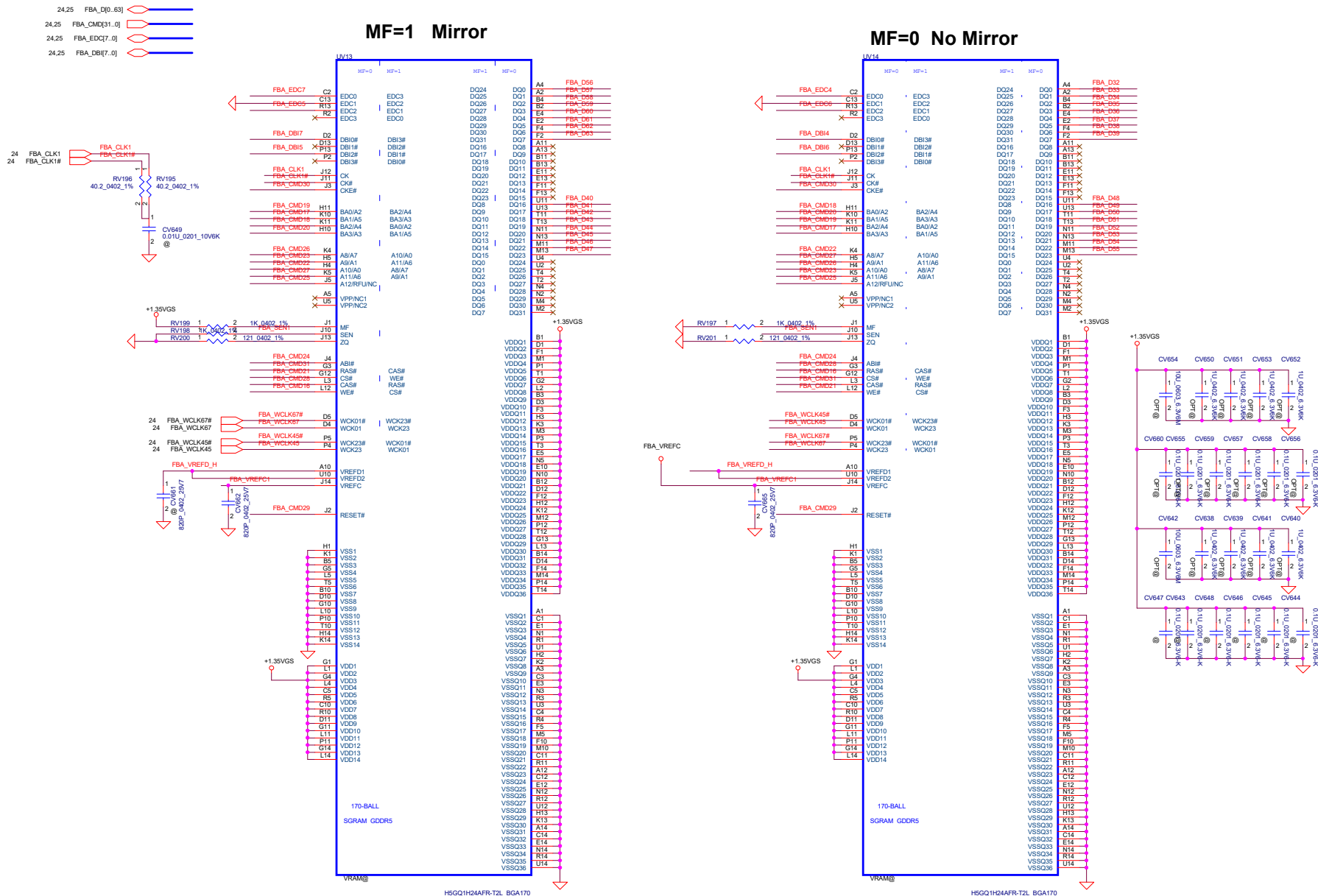
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Security Classification		LC Future Center Secret Data		Title	
Issued Date		Deciphered Date		N16X GDDR5_Rank0 [31-0] LCFC	
2015/08/20		2016/08/20			
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Size		Document Number		Revision	
		DC421		1.0	
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upper 32 bits

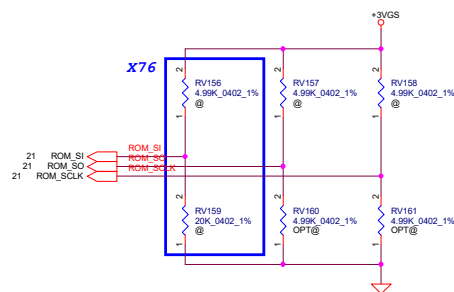
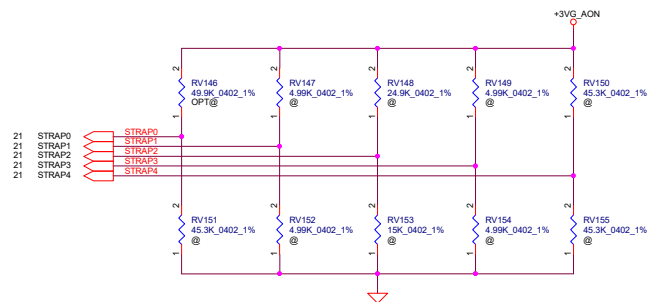
MF=1 Mirror

MF=0 No Mirror



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Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	N16X_GDDR5_Rank0_64333 	
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Date:	Sunday, January 22, 2017	Sheet	6 of 60		



Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	


PCIE_CFG	
0	(Default)
1	

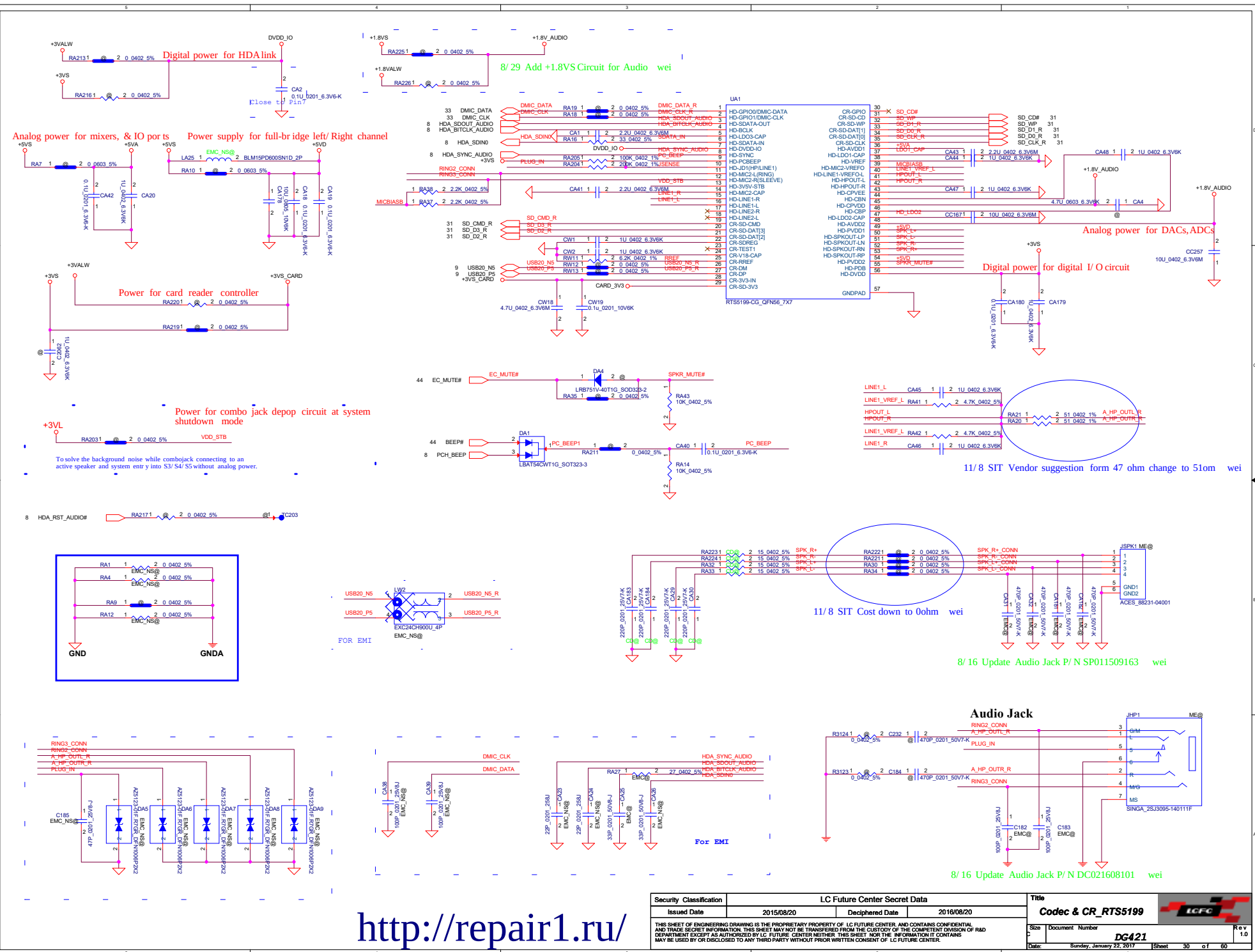
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

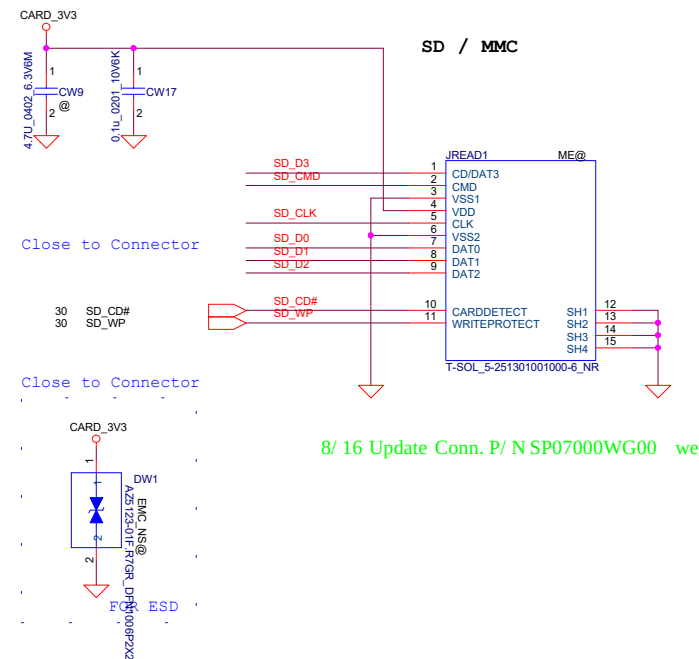
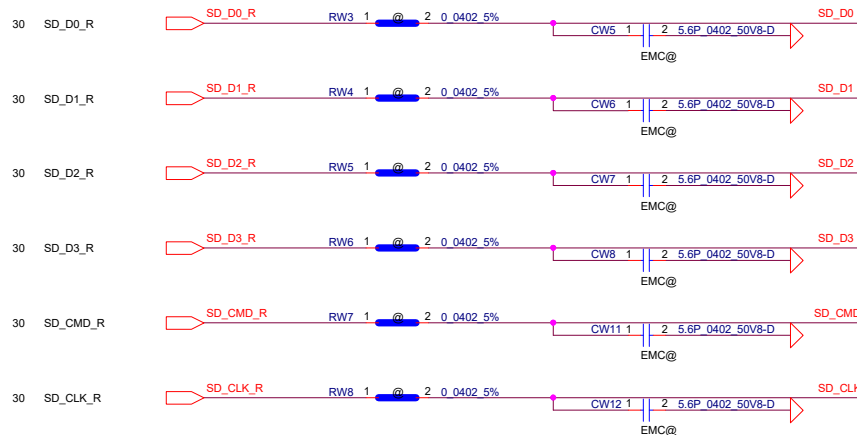
GPU	Configuration	FB Memory (DDR3L)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR N16V-GMR1	2G VRAM	Samsung 2500MHz K4G41325FE-HC28 256M x 16	0x7	PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff	Un-stuff
		H5GC4H24AJR-T2C 256M x 16	PD 45.3K							
		Hynix 2500MHz H5GC4H24AJR-T2C 256M x 16	0x6							
		PD 34.8K								
		Micron 2500MHz EDW4032BABG-60-F 256M x 16	0x4							
		PD 24.9K								
	4G VRAM	Samsung 2500MHz K4G80325FB-HC03 512M x 16	0x0							
		PD 4.99K								
		H5GC8H24MJR-T2C 512M x 16	0x5							
		PD 30.1K								
		Hynix 2500MHz MT51J256M32HF-60:A 512M x 16	0x1							
		PD 10K								

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						Size			Document Number		
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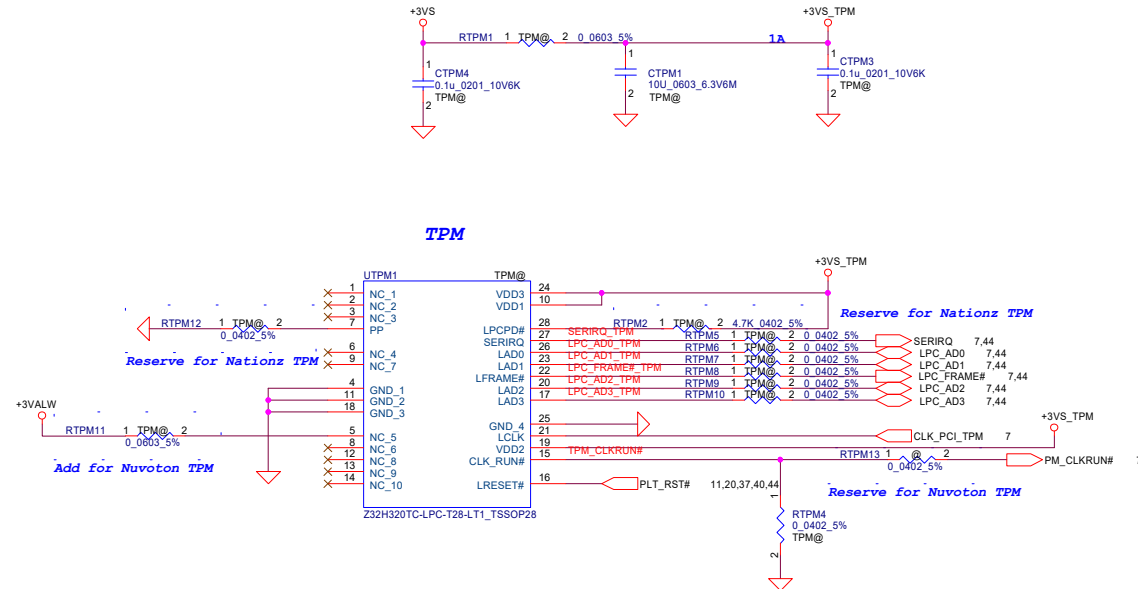


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Issued Date	2015/08/20	Deciphered Date	2016/08/20	Cardreader	
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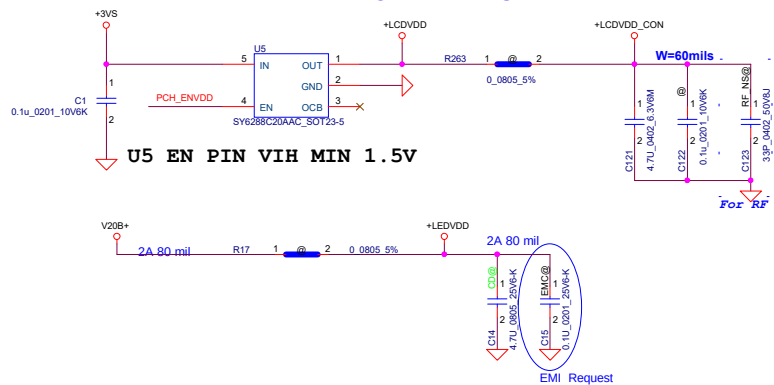


	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

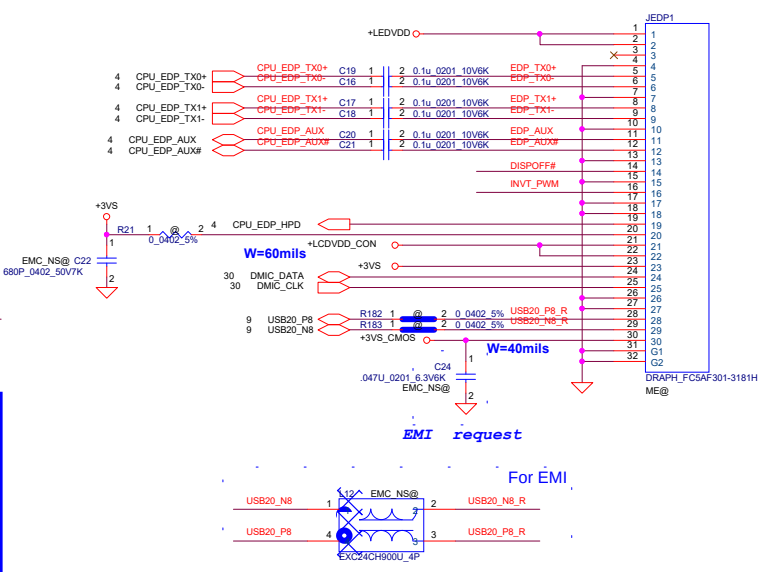
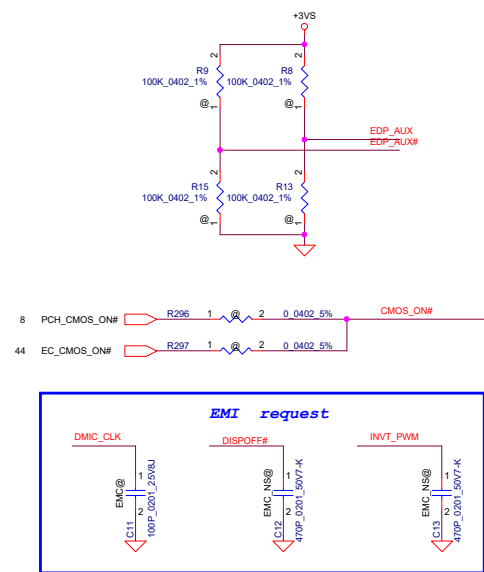
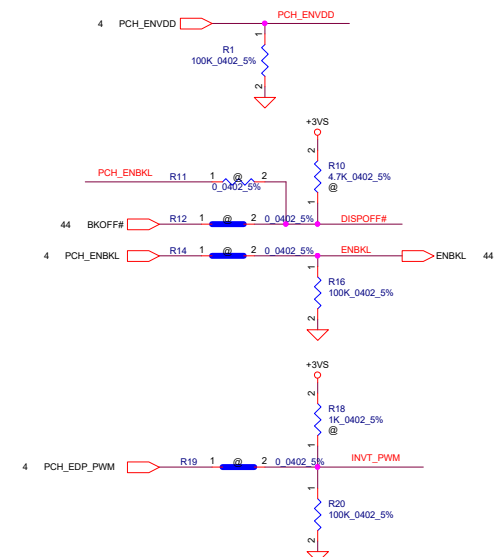
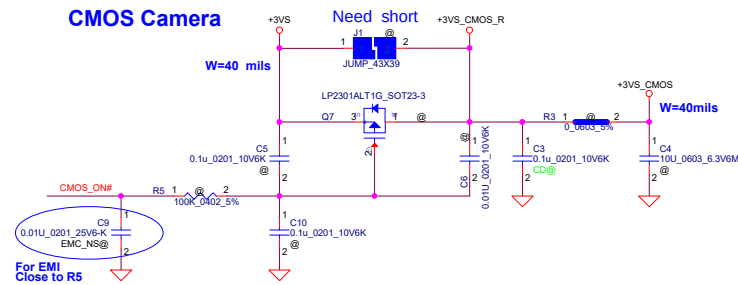
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LCD POWER CIRCUIT

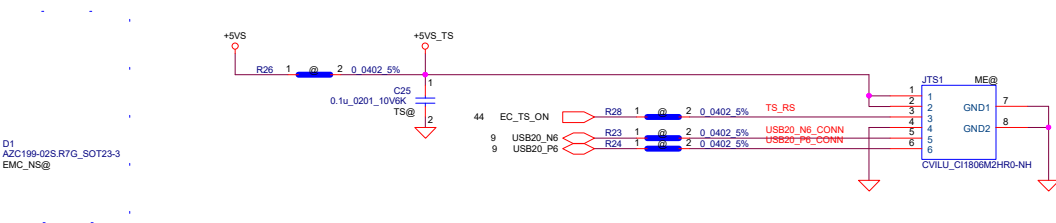
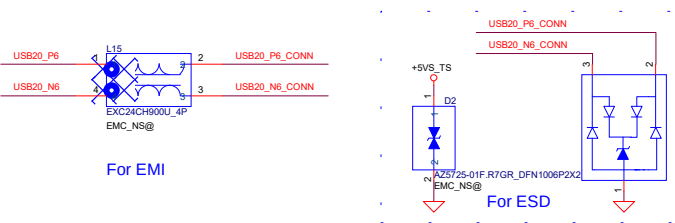


CMOS Camera



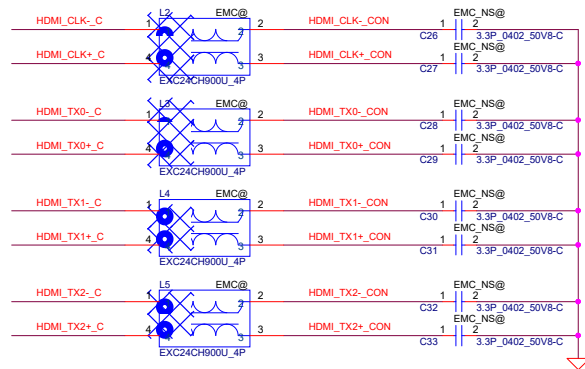
Touch Screen

Touch Screen

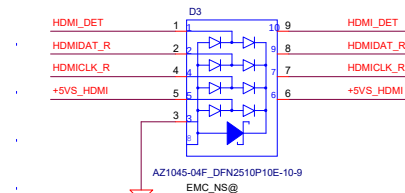
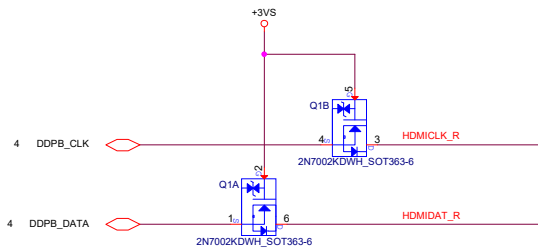
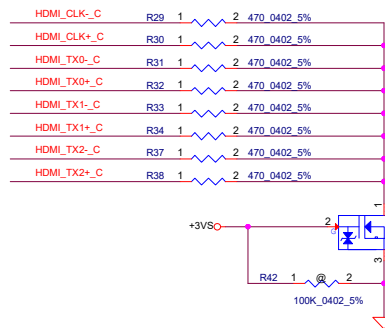


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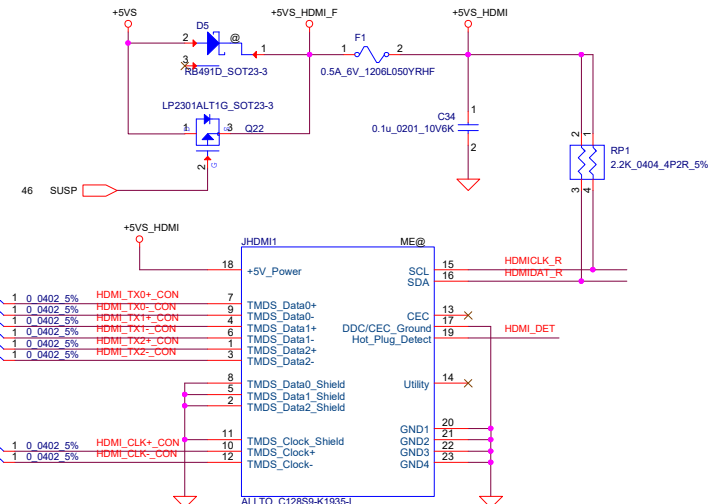
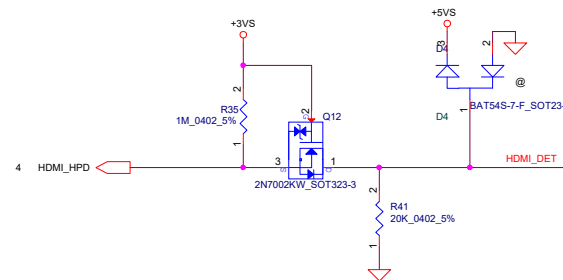
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	eDP/CMOS/Touch screen	
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For EMC

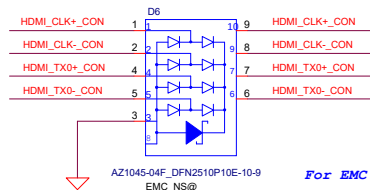


For EMC

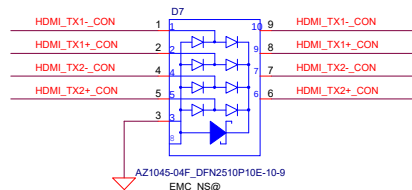


8/16 Update HDMIConn.P/N DC021608081 wei

Close to JHDMI1




For EMC




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Title			LCFC	
HDMI_CONN				
Size	Document	Number	Rev	
Custom		DG421	1.0	
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Issued Date	2015/08/20	Deciphered Date	2016/08/20				
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				Custom	DG421	1.0	
Date:				Sunday, January 22, 2017	Sheet	35 of 60	

Security Classification				LC Future Center Secret Data				Title			
Issued Date		2015/08/20		Deciphered Date		2016/08/20		Blank			
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Date: Sunday, January 22, 2017										Sheet 36 of 60	

+3VALW TO +3VALW_LAN

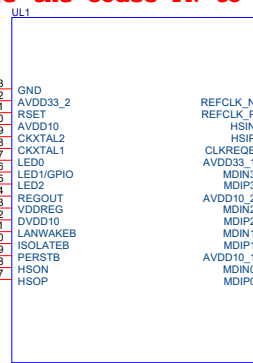
+3VALW_LAN rising t ime (10 %~90 %):
0.5ms spec 10 0m s

Need short

width : 40 mils

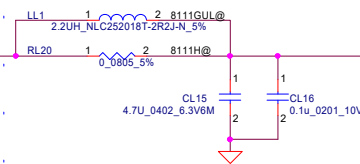
Close to Pin11 Close to Pin32 Close to Pin11 Close to Pin32

manual change the Codec PN to RTL8111GUL-CG



RTL8111GUL-CG QFN 32P
8111GUL@

For RTL8111GUL(SWR mode, reserved)
For RTL8111H (LDO mode)



Layout Note: LL1 must be
within 200mil to Pin24,
CL15,CL16 must be within
200mil to LL1
+LAN_REGOUT: Width =60mil

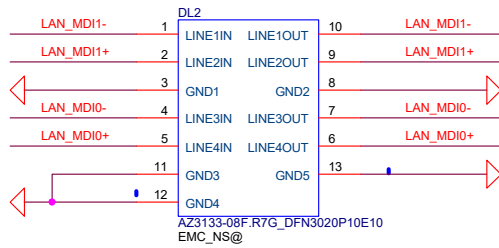
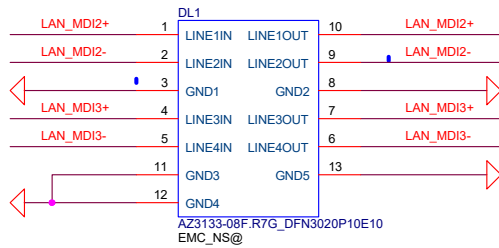
Close to Pin3, 8, 22, 30

Close to Pin22(Reserved)

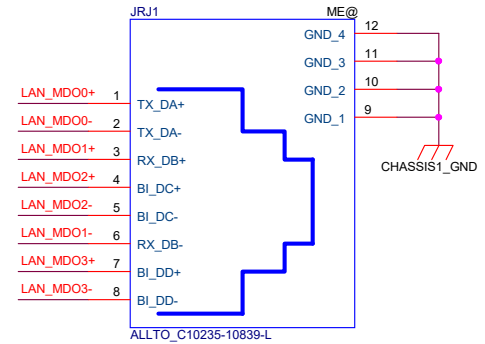
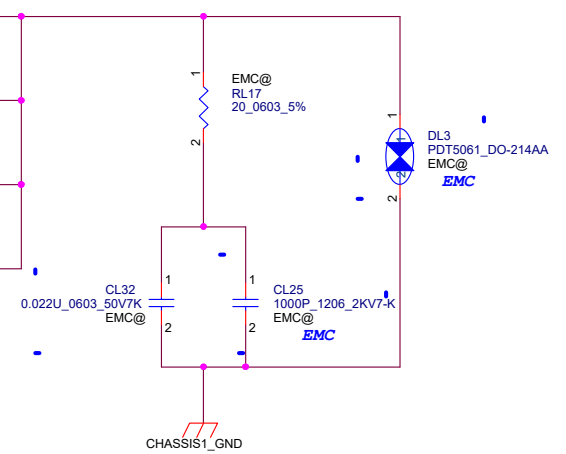
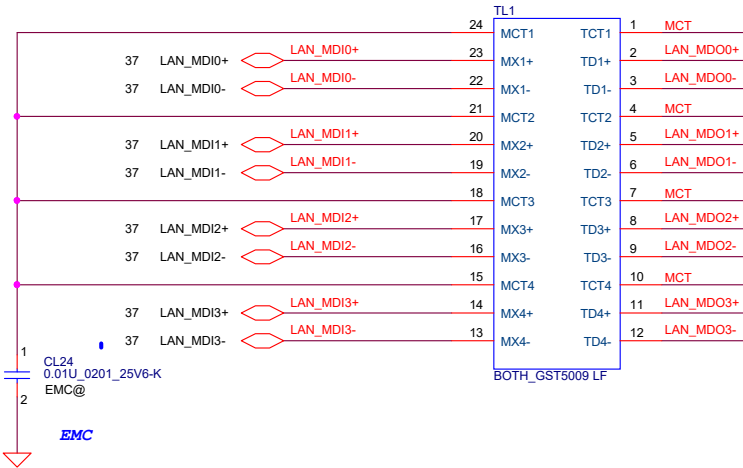
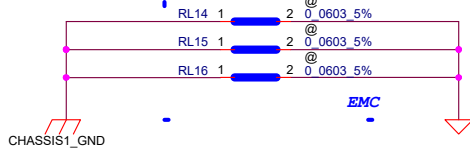
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Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	LAN_RTL8111H_CG	
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DL1/DL2
1'S PN:SC300003M00



Place Close to TL1

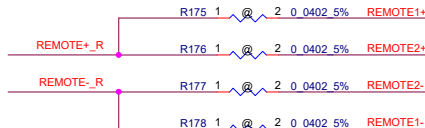
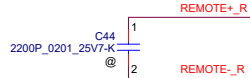


8/16 Update RJ45 P/ NDC021608091 wei

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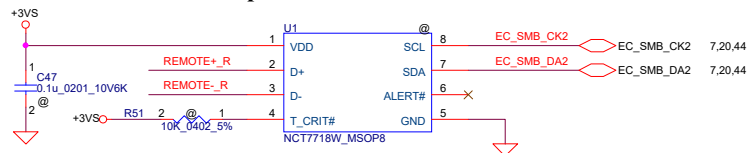
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	LAN_Transformer	
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Close to U1



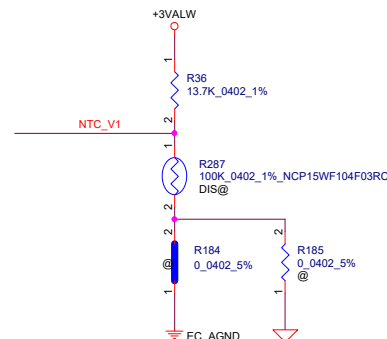
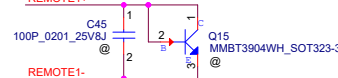
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM



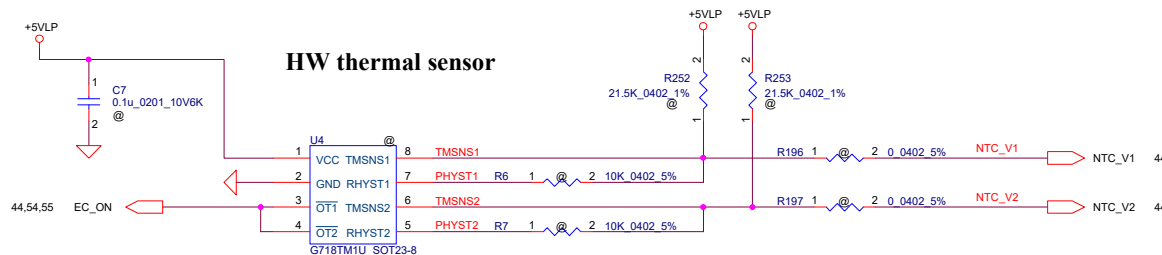
Address 1001_101xb

Near GPU&VRAM



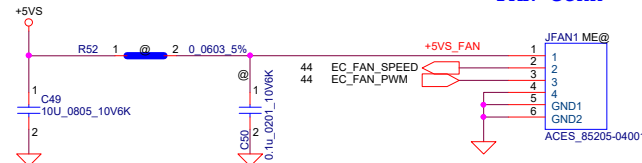
for layout optimized, change the EC_AGND to GND

HW thermal sensor



over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C

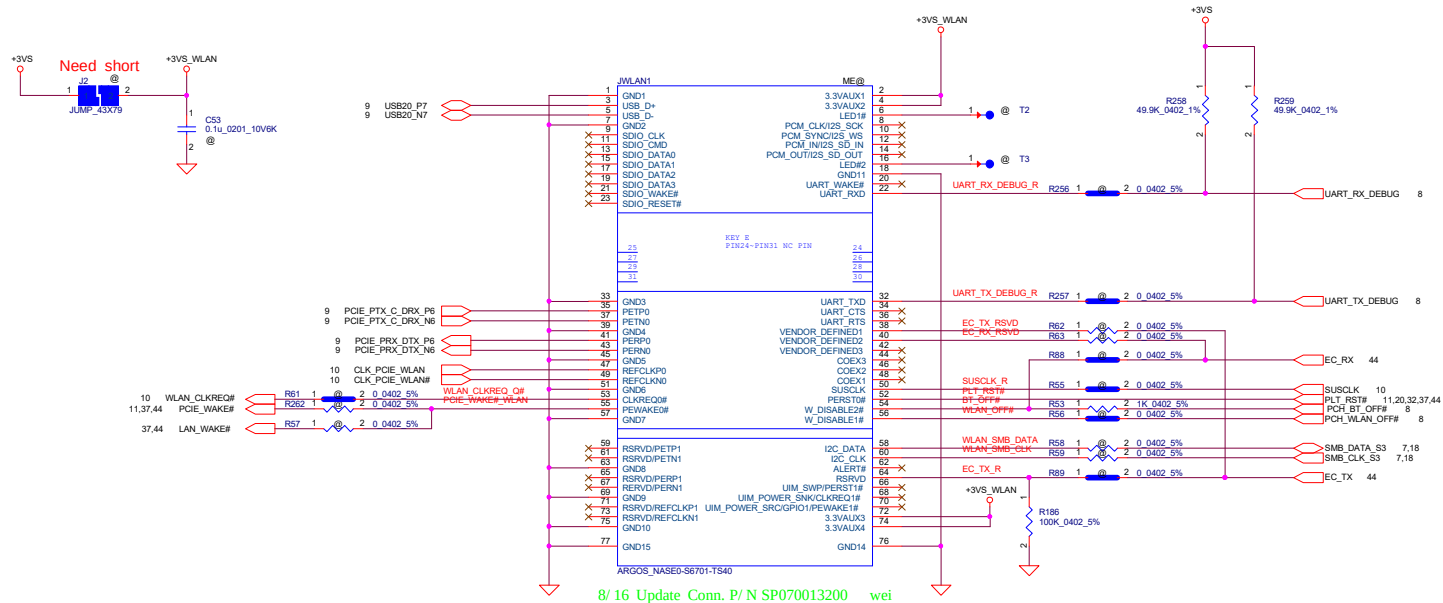
FAN Conn



<http://repair1.ru/>

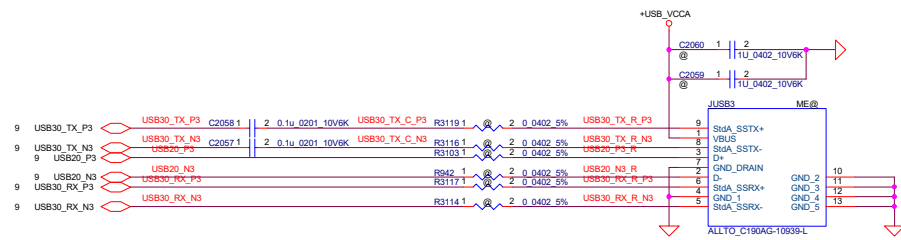
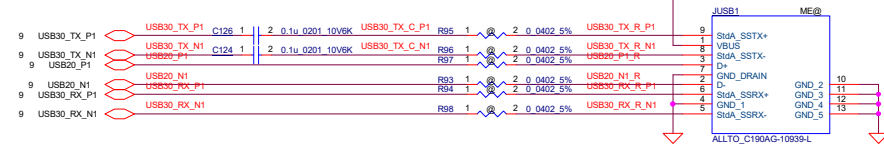
Security Classification	LC Future Center Secret Data			Title	Thermal sensor/FAN Conn	
Issued Date	2016/08/16	Deciphered Date	2017/08/15	Size	Document Number	Rev
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				Date:	Sunday, January 22, 2017	Sheet 39 of 60



Mini-Express Card(WLAN/WiMAX)



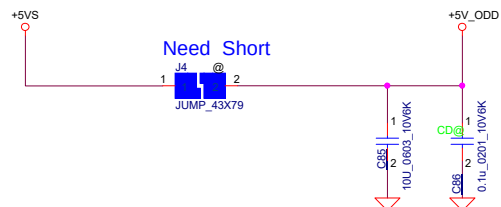
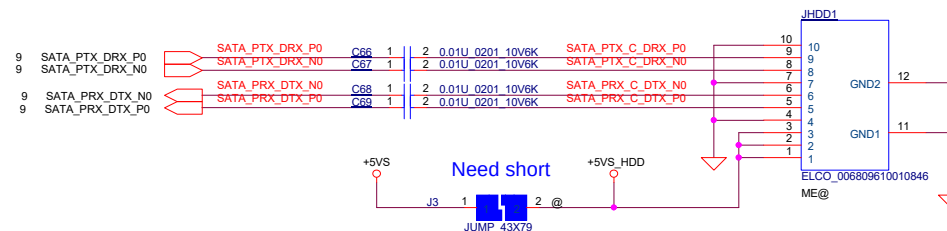
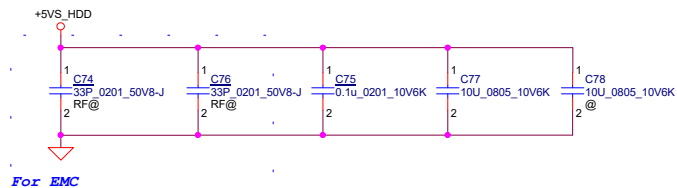
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Issued Date		Deciphered Date		NGFF WLAN&SSD	
2015/08/20		2016/08/20		Size	
Document Number		Rev		1.0	
Date		Sunday, January 22, 2017		Sheet 40 of 60	

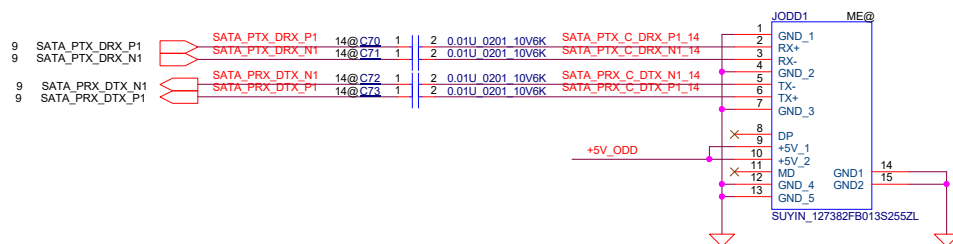
[illegible]

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Size		Document Number		DC421		Revision		1.0	
Date		Sunday, January 22, 2017		Sheet		41		of 60	

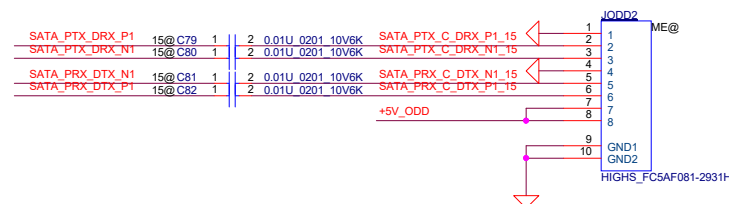
SATA HDD Conn.



FOR 14" SATA ODD Conn.




FOR 15" 17" SATA ODD FFC Conn



8/ 16 Update Conn. P/ N SP01001YV00 wei

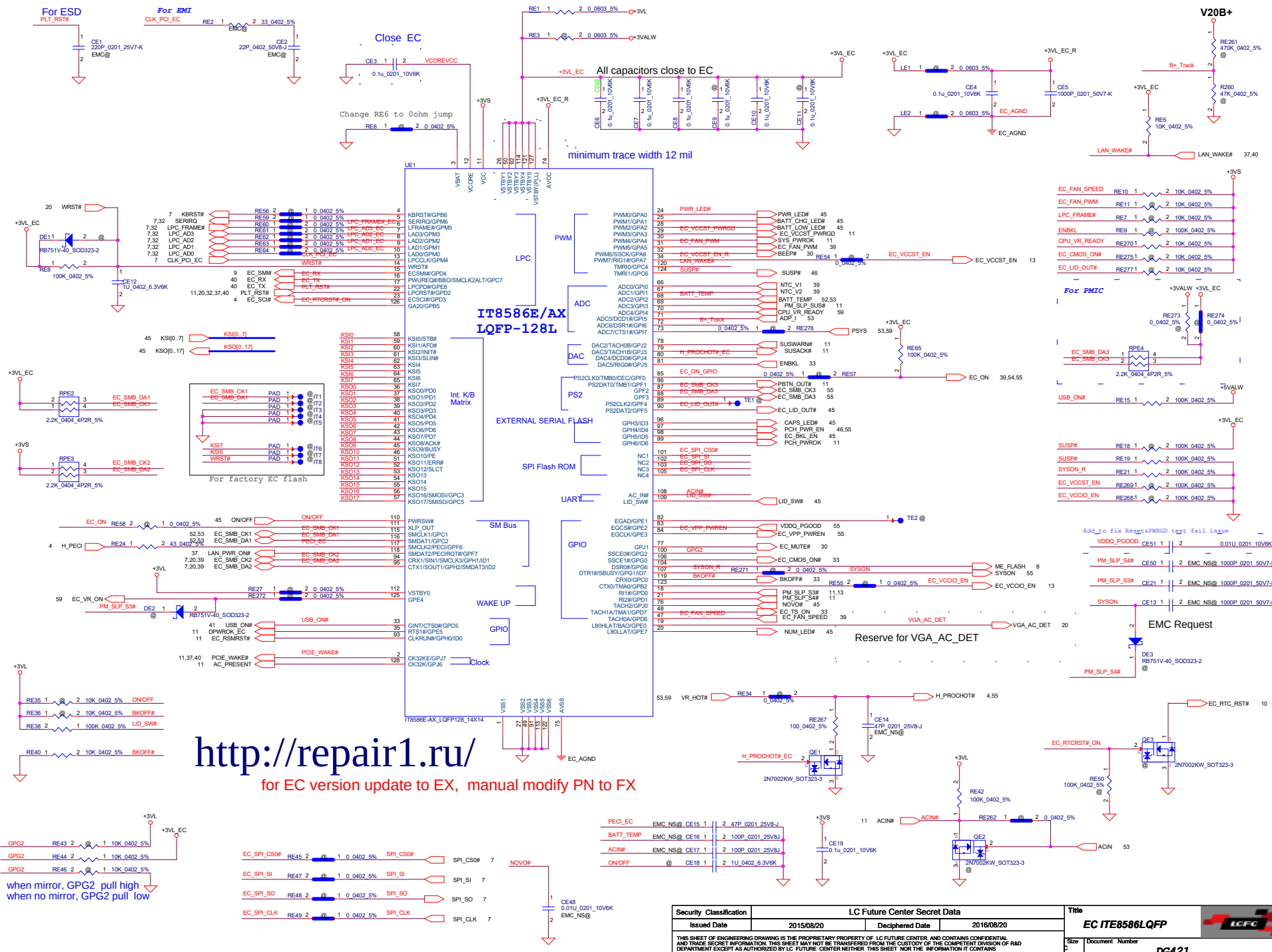
<http://repair1.ru/>

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	HDD/ODD CONN	
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Size Custom	Document Number			DG421	
Date:	Sunday, January 22, 2017			Sheet	42 of 60



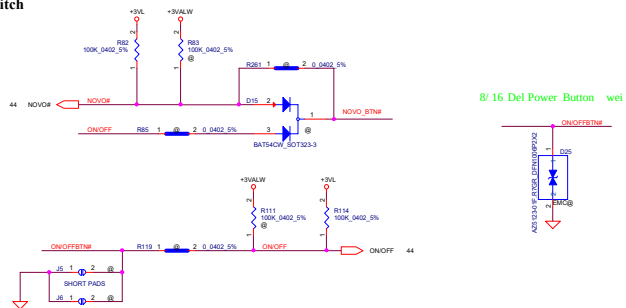
<http://repair1.ru/>

for EC version update to EX, manual modify PN to FX

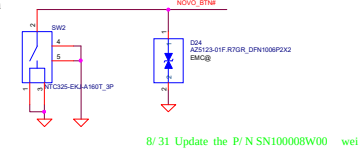


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Size	Document Number		Rev		
	DG421		1.0		
Date:	Sunday, January 22, 2017		Sheet	44	of 60

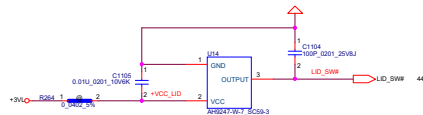
ON/OFF switch



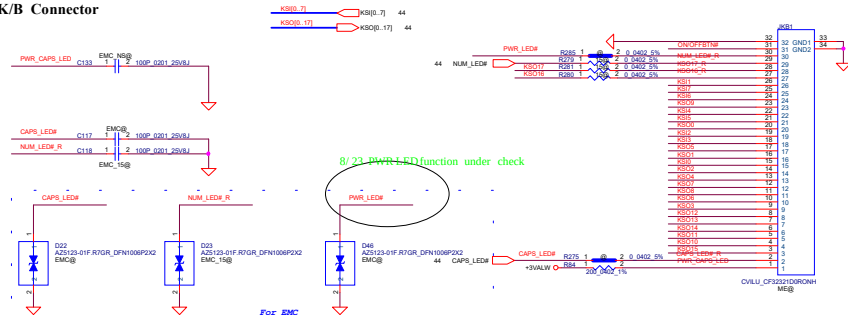
Novo button



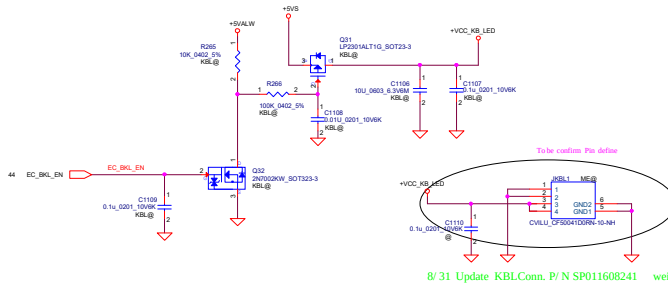
LID switch



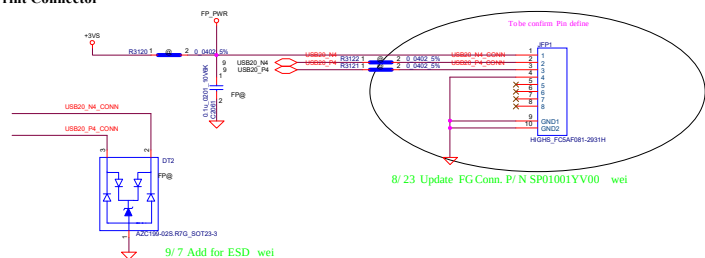
K/B Connector



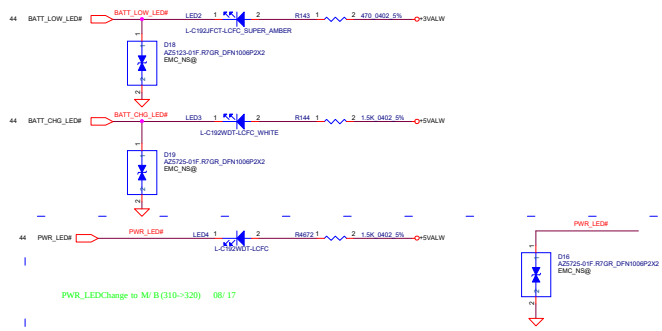
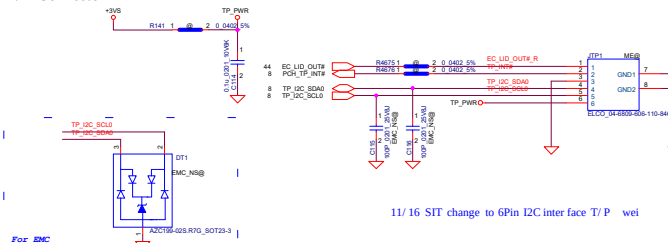
KB Backlight Connector



Finger Print Connector



TP/B Connector



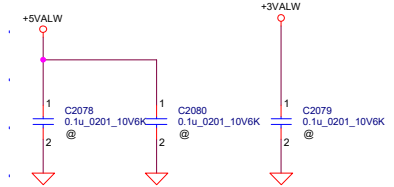
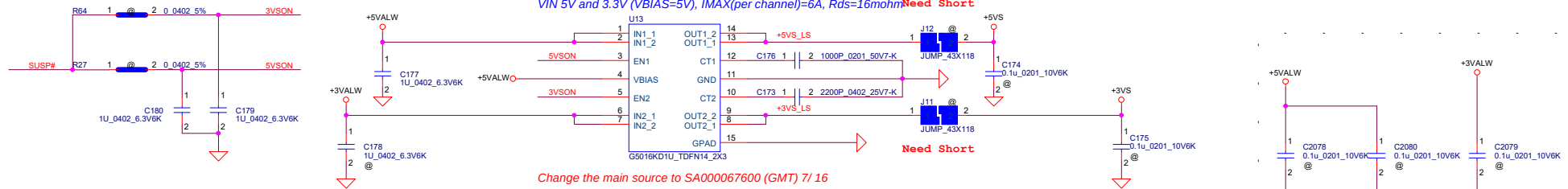
<http://repair1.ru/>

Security Classification		L.C Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	KBD/PWR/IO/LED/TP Conn.	
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		Date		Monday, January 22, 2017	
		Sheet		46 of 60	

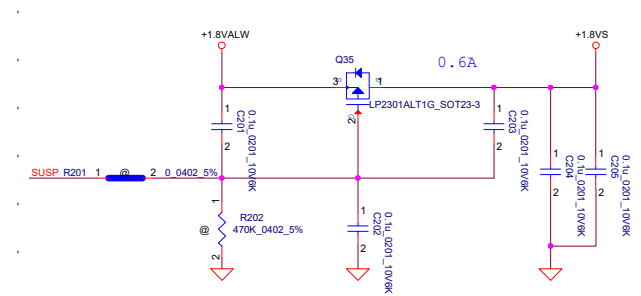
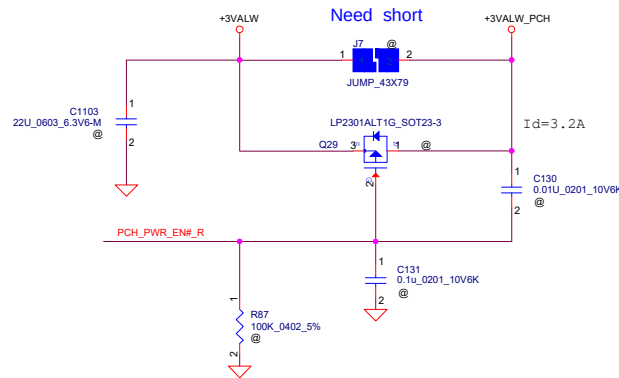
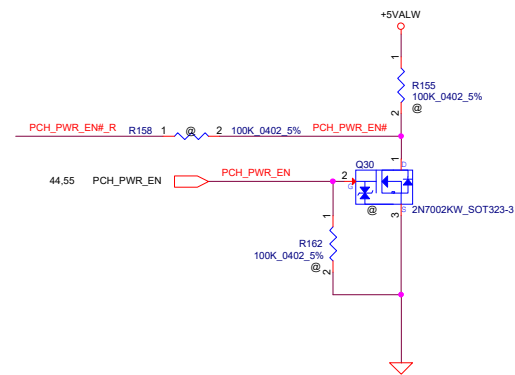
Load Switch
+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

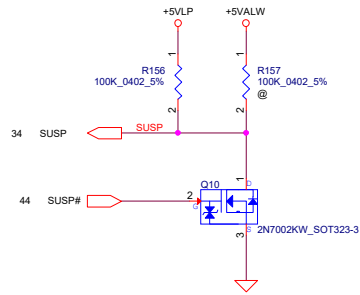
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



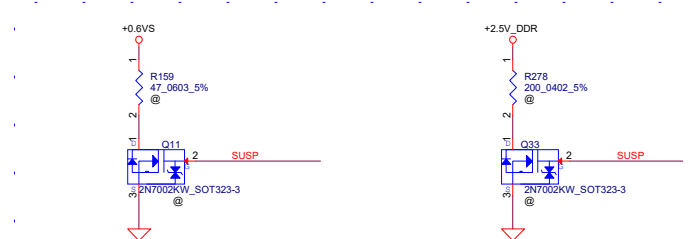
EMC



8/ 29 Add +1.8VS Circuit for Audio wei



For DisCharge

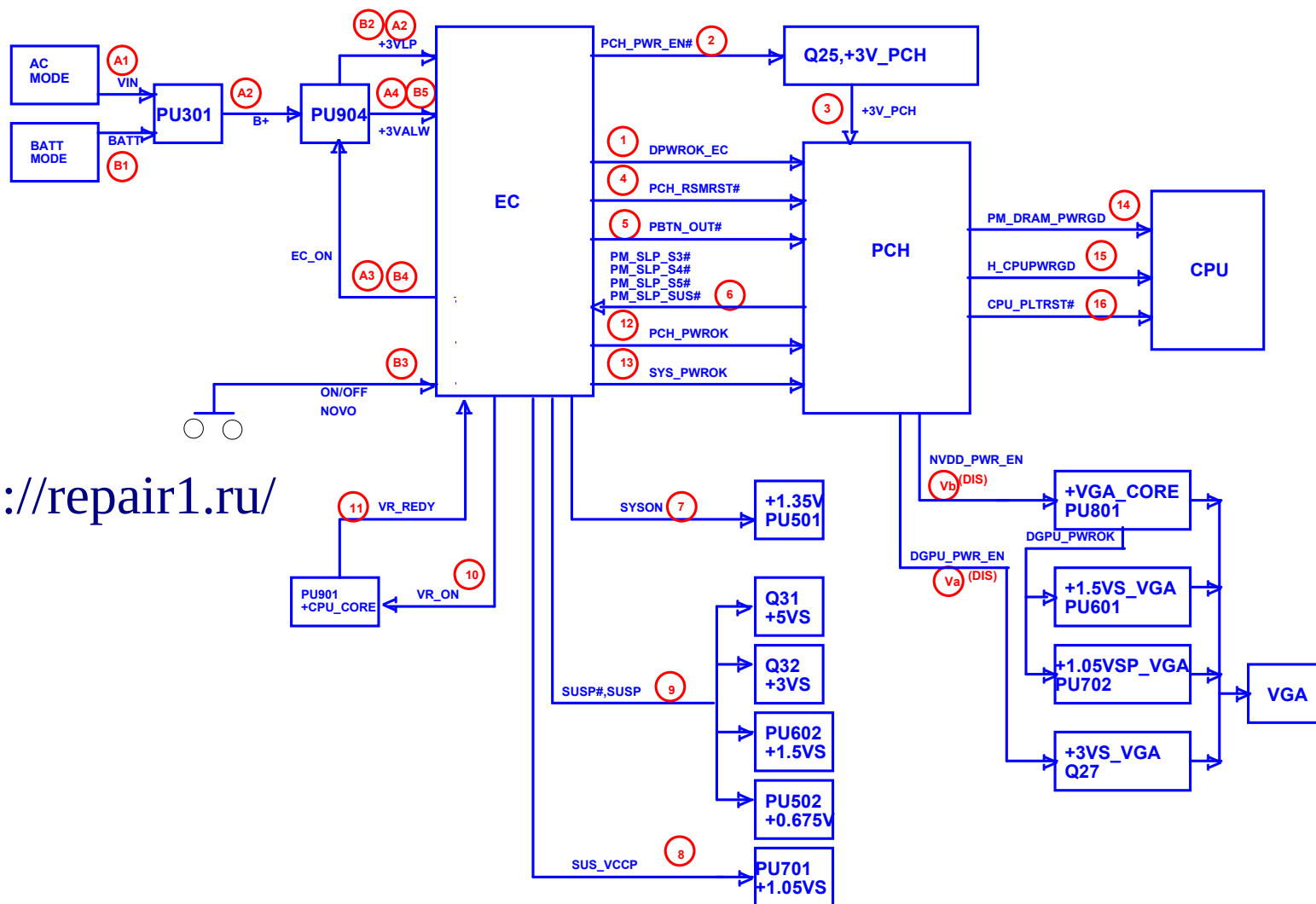


08/ 29: Need double check enable signal and the resistance

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Security Classification	LC Future Center Secret Data			Title	DC V to VS INTERFACE	
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				Date:	Sunday, January 22, 2017	Sheet 46 of 60

<http://repair1.ru/>

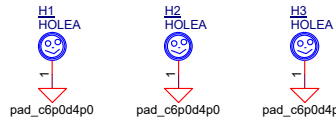


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20
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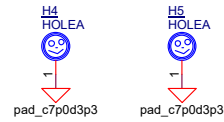
Title		Power sequence block	
Size	Document	Number	Rev
Custom		DG421	1.0
Date:	Sunday, January 22, 2017	Sheet	47 of 60

Security Classification				LC Future Center Secret Data				Title			
Issued Date		2015/08/20		Deciphered Date		2016/08/20		Virtual symbol			
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Size Document Number								DG421		Rev 1.0	
Date: Sunday, January 22, 2017								Sheet 48 of 60			

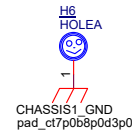
CPU Thermal Holex3



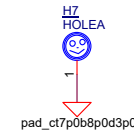
GPU Thermal Holex2



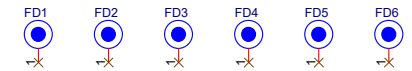
Close to RJ45



Close to Audio jack



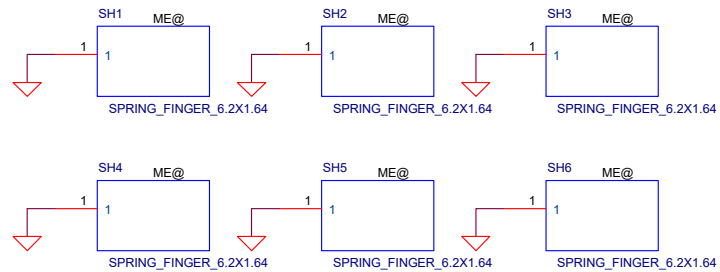
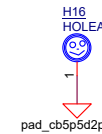
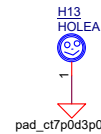
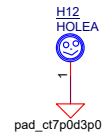
PCB Federal Mark PAD



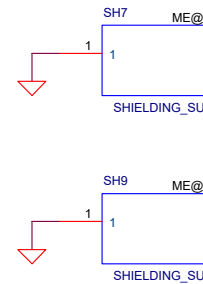
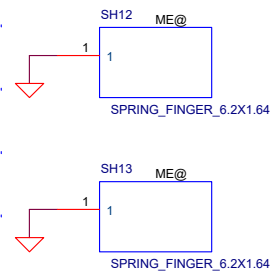
DC-IN x2



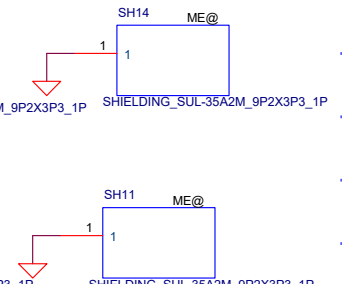
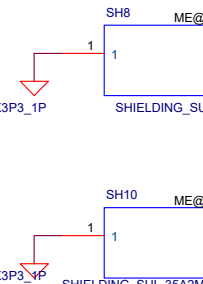
WLAN Standoff



USB3.0 Shielding

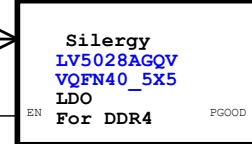
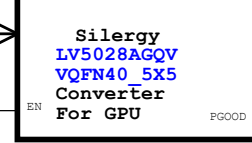
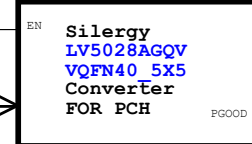
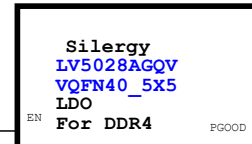
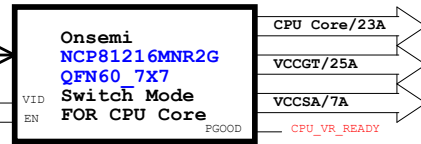
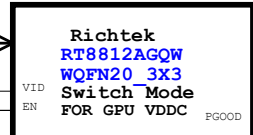
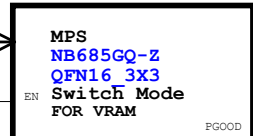
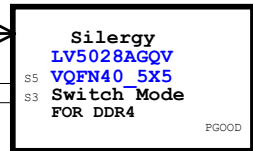
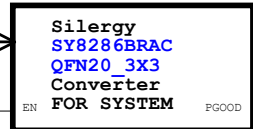
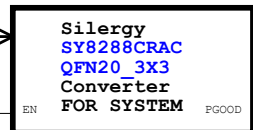
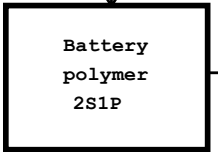
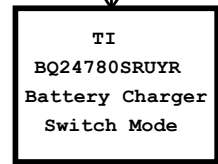
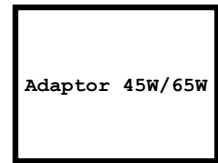


DDR4 Shielding

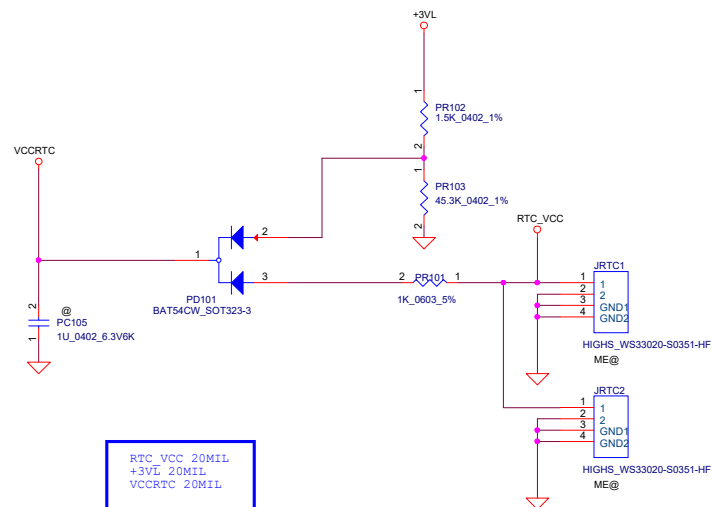
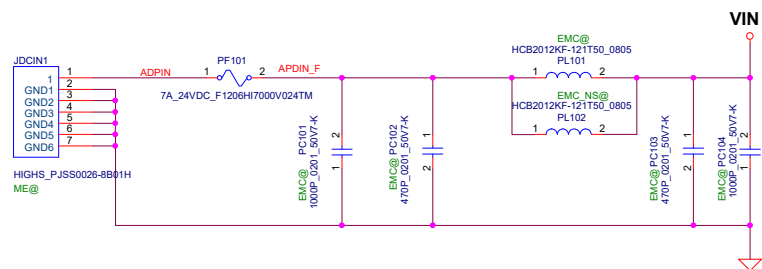


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					DG421
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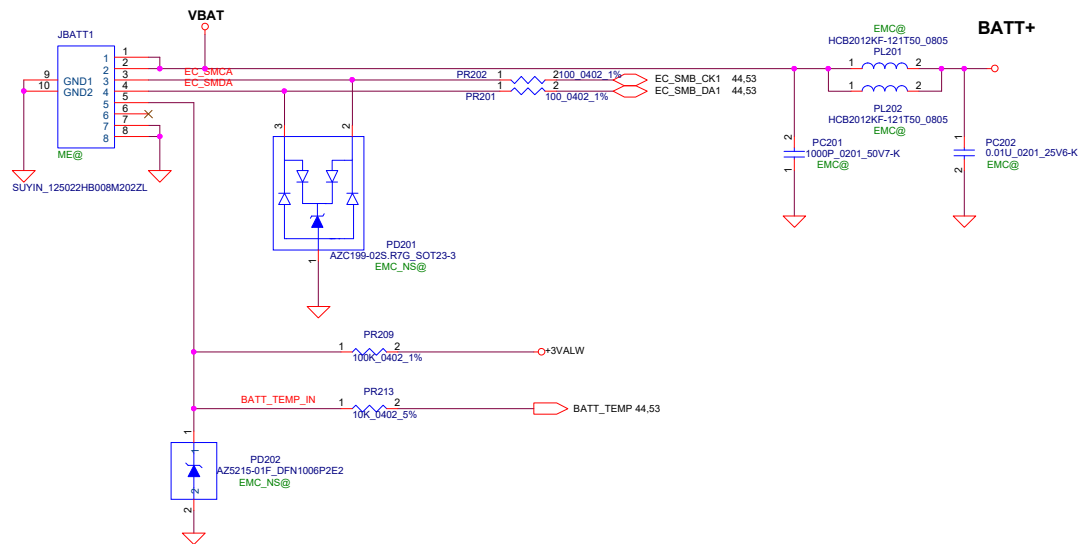


RTC VCC 20MIL
+3V_L 20MIL
VCCRTC 20MIL

No charge RTC with 35mm cable
RTC Battery for GCM BOM
(2nd source and quoted price)

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Security Classification	LC Future Center Secret Data			Title
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR-DCIN / RTC charger
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				Document Number DG421
				Rev 1.0
				Date: Sunday, January 22, 2017
				Sheet 51 of 60



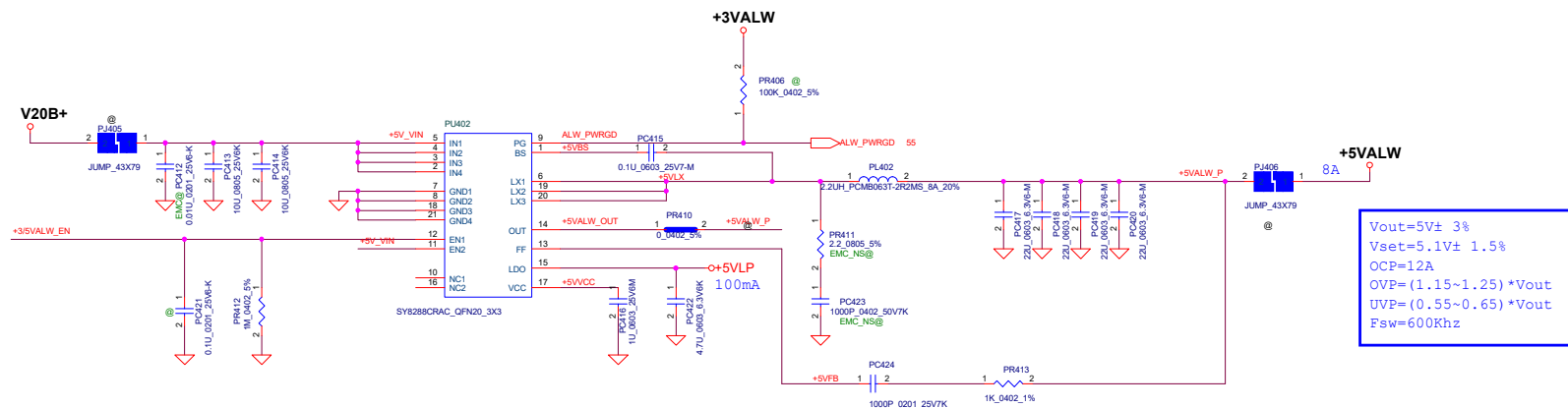
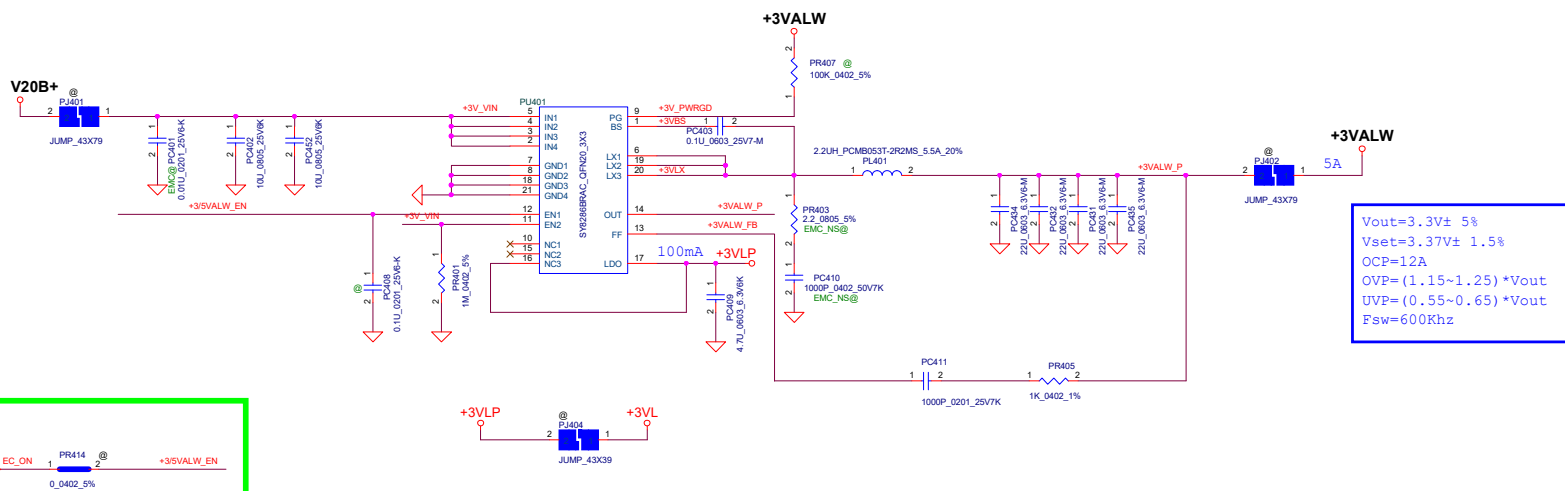
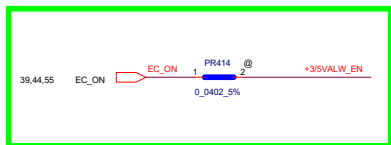
2S1P polymer battery
voltage level: +6V ~
8.4 V

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Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR-BATTERY CONN/OTP	
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				Date: Sunday, January 22, 2017	Rev 1.0
				Sheet 52 of 60	

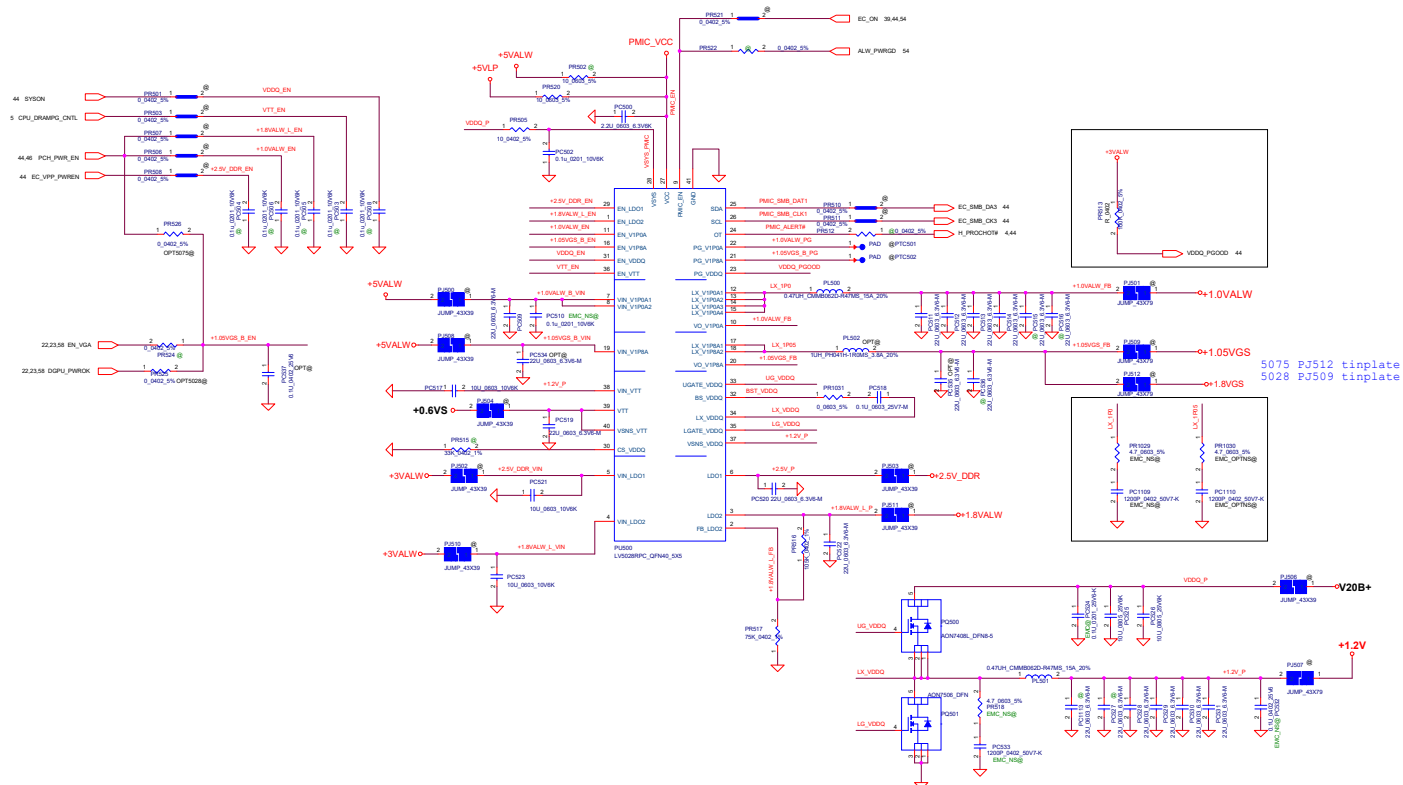
PR313 PR315 :432K and 64.9k
change to 43k and 7.15k.
vin detect volatage level:16.8V
PC309:0.1u change to 0.01u
decrease ACDET deassert time

<http://repair1.ru/>




<http://repair1.ru/>

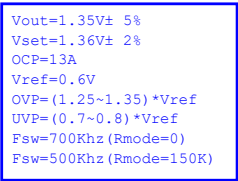
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				Sunday, January 22, 2017	1.0
				Sheet	54 of 60





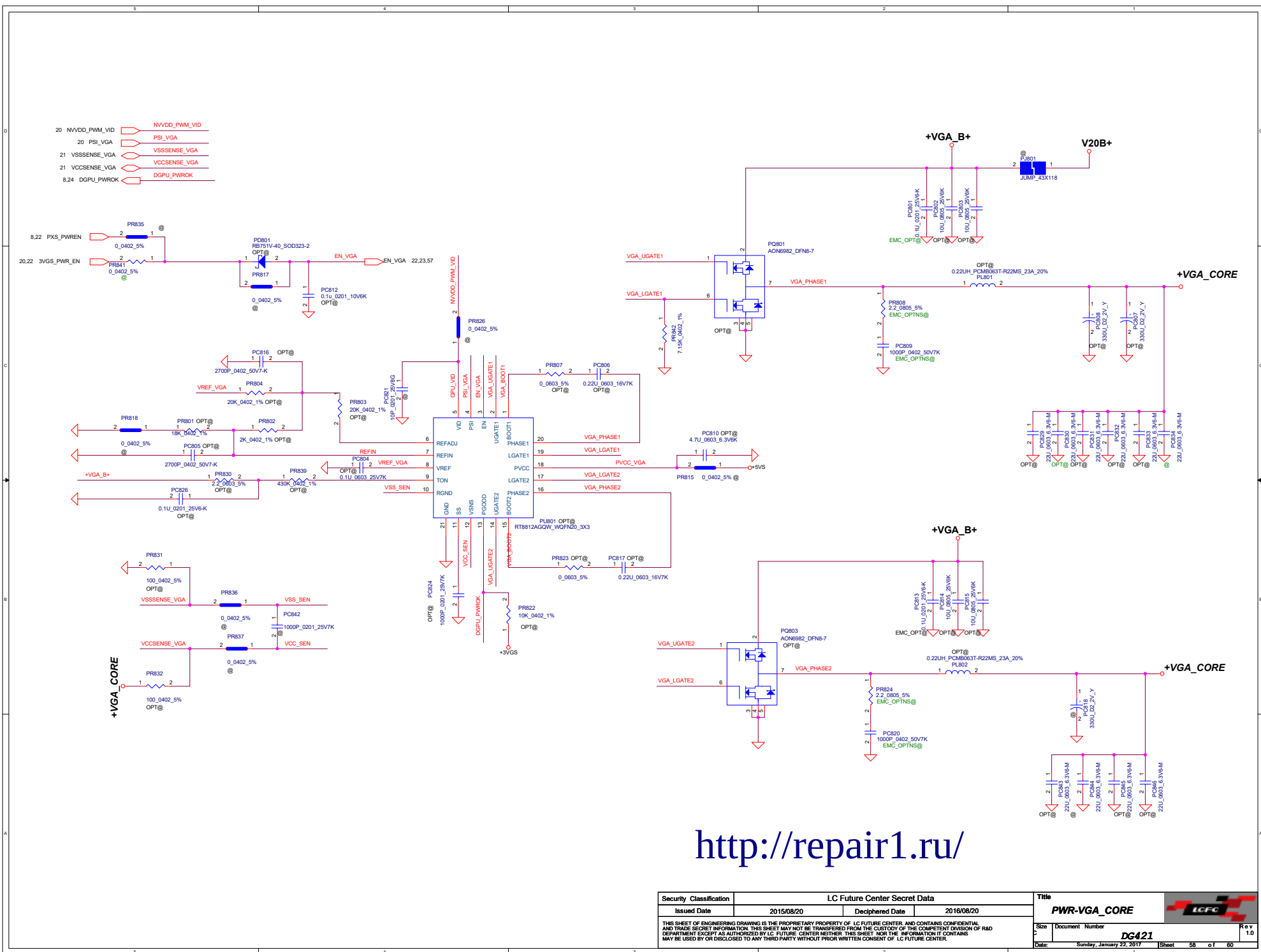
<http://repair1.ru/>

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RVboot	Core	GT	SA
14K	0V	0V	1.05V



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