

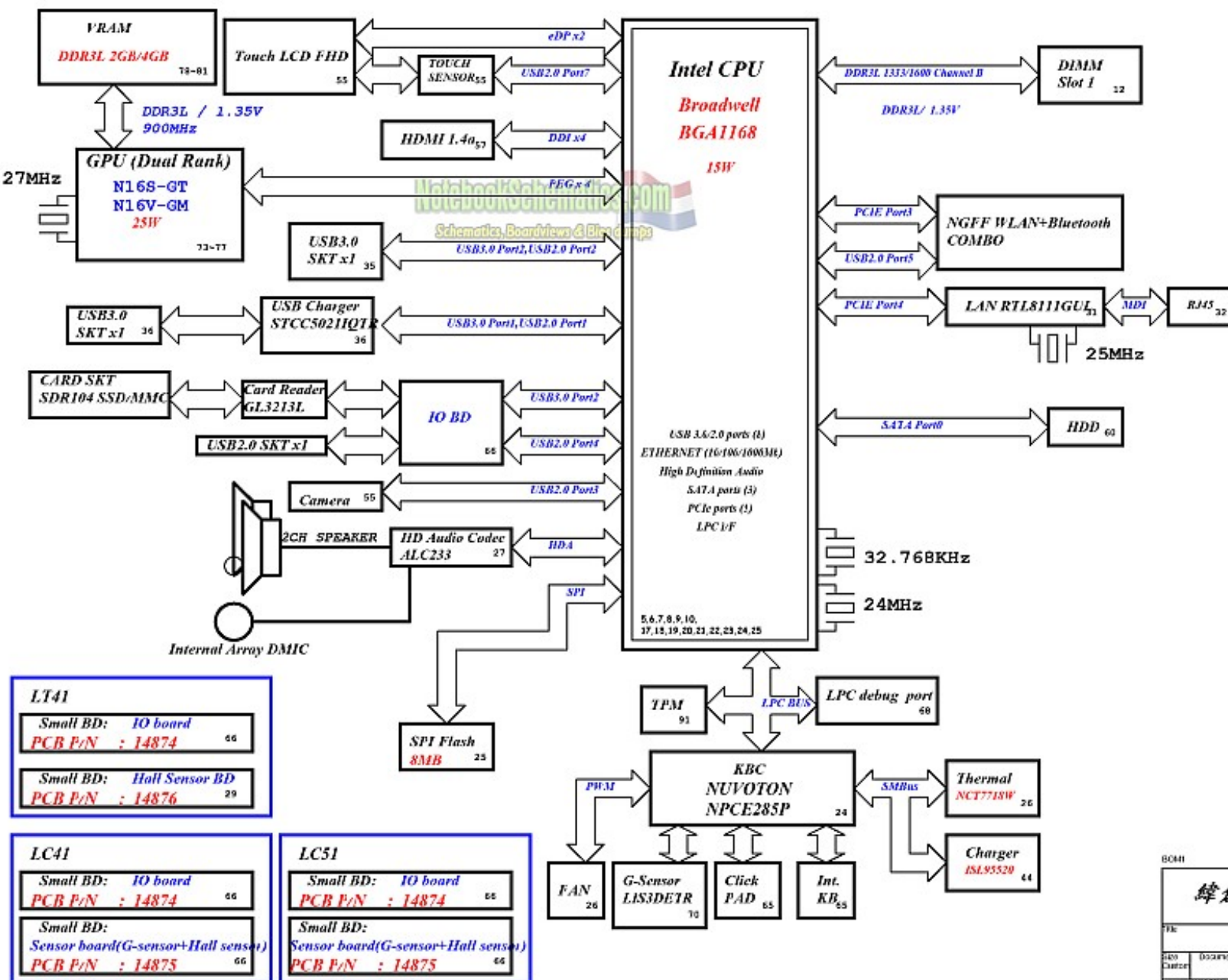
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Schematics Document

BOM1

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Title			
Cover Page			
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LT41 Board Block Diagram

Project code : 4PD03N010001
PCB P/N : 14217



CHARGER	
ISL95520	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
TP551275	45
INPUTS	OUTPUTS
DCBATOUT	5V_Charger
	3D3V_S5
CPU DC/DC	
TP551624	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
SYS8208A	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
TP551716	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
SYSTEM DC/DC	
INPUTS	OUTPUTS
SYSTEM DC/DC	
RT9198	51
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0
RT8812A	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
Switches	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D35V_S0	1D35V_VGA_S0
1D05V_VTT	1D05V_VGA_S0
PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

LT41	
Small BD: IO board	66
PCB P/N : 14874	
Small BD: Hall Sensor BD	29
PCB P/N : 14876	
LC41	
Small BD: IO board	66
PCB P/N : 14874	
Small BD: Sensor board(G-sensor+Hall sensor)	66
PCB P/N : 14875	

LC51	
Small BD: IO board	66
PCB P/N : 14874	
Small BD: Sensor board(G-sensor+Hall sensor)	66
PCB P/N : 14875	

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,.....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

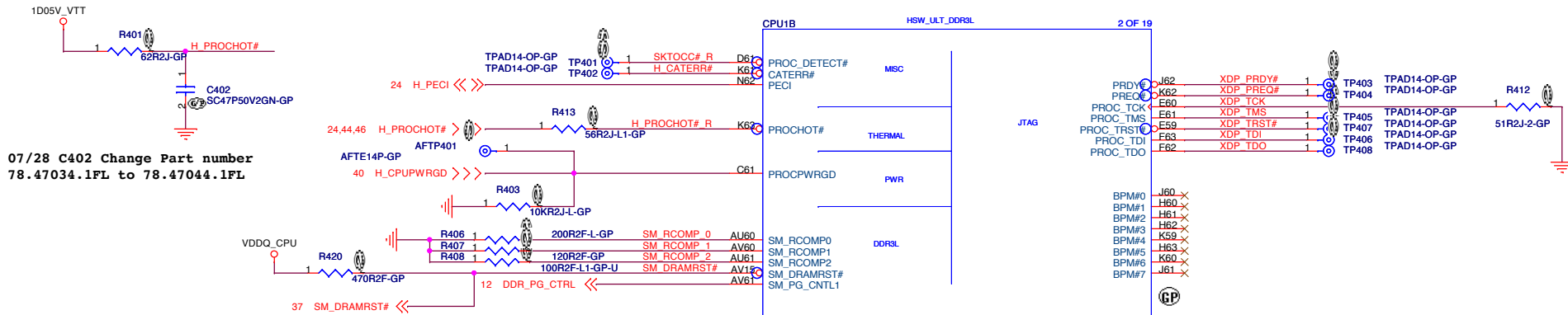
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SSID = CPU

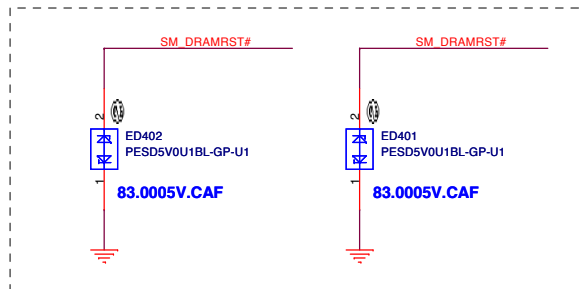
SC

071.BROAD.0M0U	IC CPU Broadwell 2+2U D-0 4MB 2c BGA 1.6GHz 15W 1333DDR ES-2	934843 QGHA
071.BROAD.0N0U	IC CPU Broadwell 2+2U D-0 4MB 2c BGA 1.6GHz 15W 1600DDR ES-2	934844 QGHB
071.BROAD.0P0U	IC CPU Broadwell 2+2U D-0 4MB 2c BGA 1.8GHz 15W 1600DDR ES-2	934842 QGH9



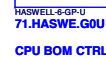
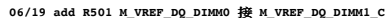
ESD Request

CPU BOM CTRL



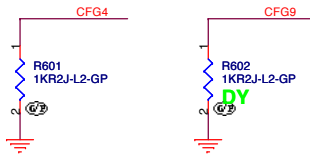
06/19 Delete ESD

12/18 add ED4003, ED4004 83.0005V.CAF
一個放前端,一個放後端

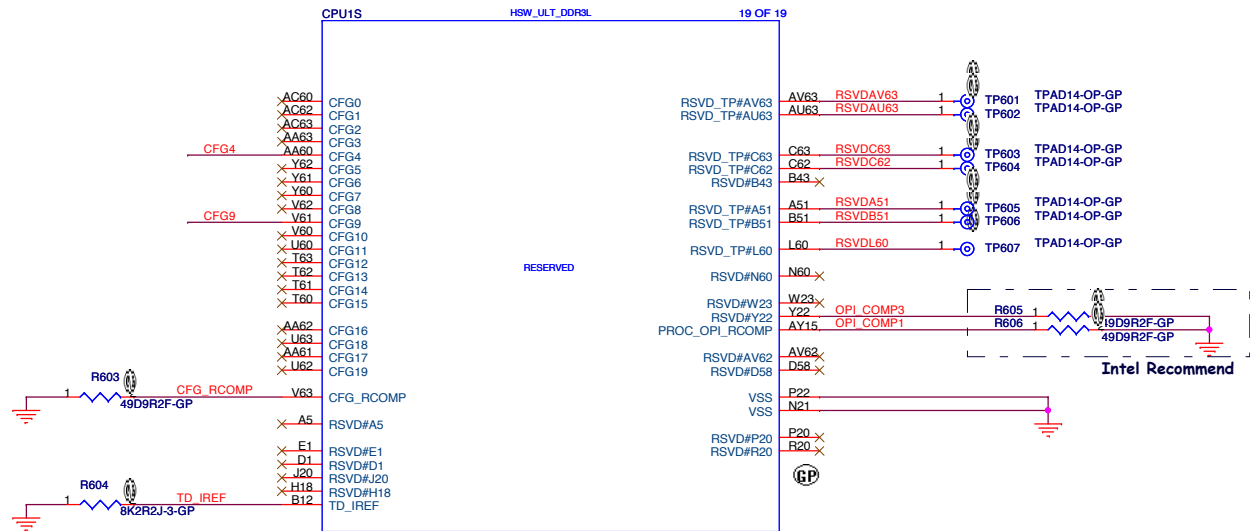


SSID = CPU

eDP Enable	1:Disable
CFG4	0:Enable



Signal Name	Description	Direction/Buffer Type
CFG[19:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none">• CFG[3:0]: Reserved configuration lane. A test point may be placed on the board for these lanes.• PCI Express* Static x16 Lane Numbering Reversal.—• CFG[4]: eDP enable<ul style="list-style-type: none">— 1 = Disabled— 0 = Enabled• [19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	
continued...		



71.HASWE.G0U

HASWELL-6-GP-U

CFG9:

CPU BOM CTRL

NO SVID PROTOCOL CAPABLE VR CONNECTED

CFG9

1: VRS SUPPORTING SVID PROTOCOL ARE PRESENT
0: NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY

HARRIS_BEACH_REFRESH
REV 0.7
PBA: G52502-004

7.4

Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left unconnected

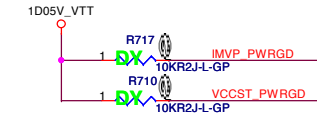
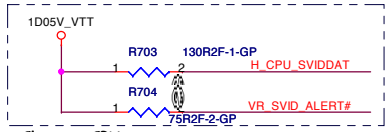
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CPU (CFG)			
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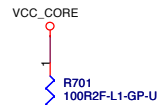
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08/06 Change PG701-PG706 Close GAP

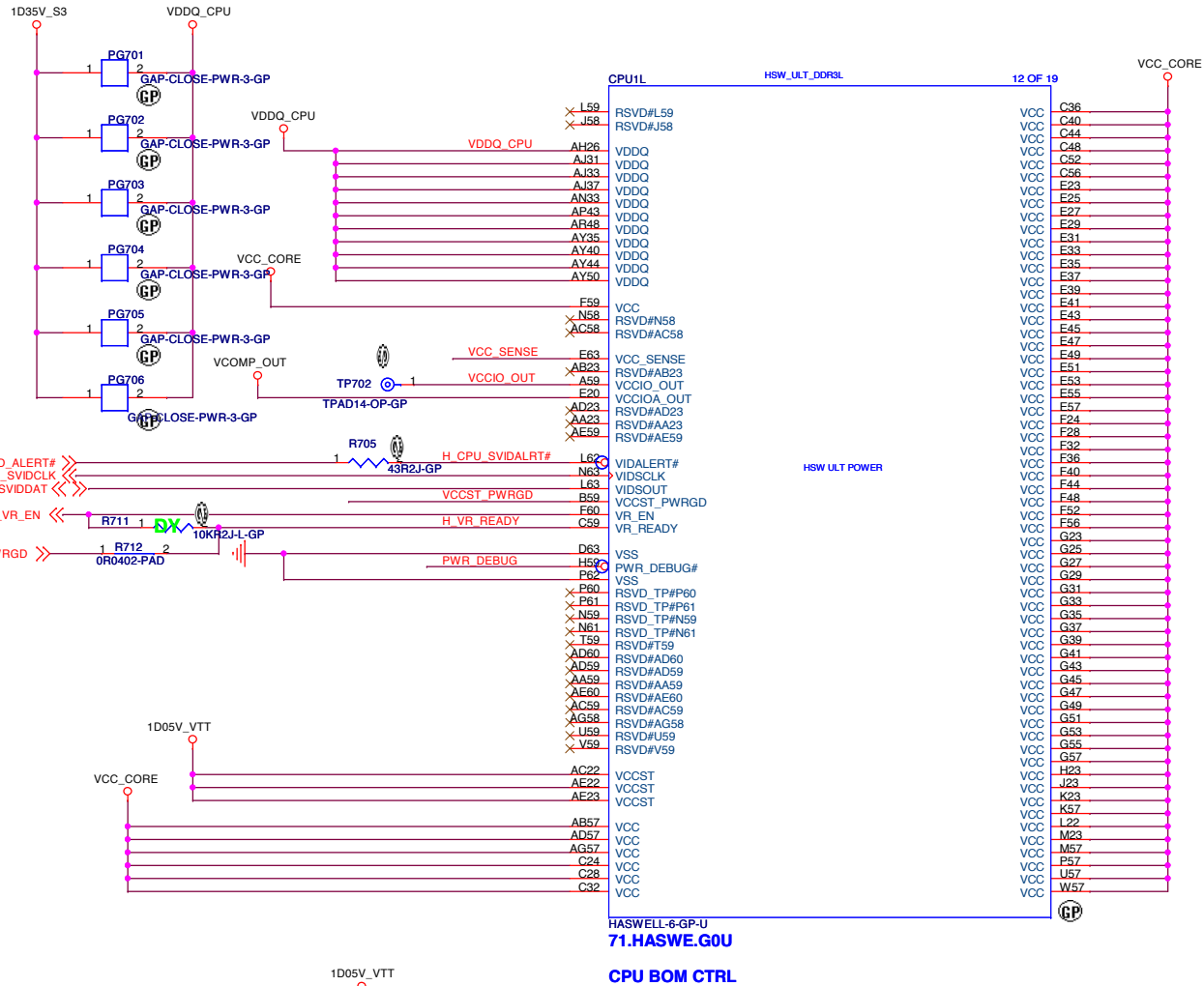
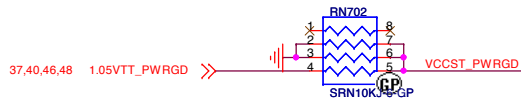
12/11 PG701-PG706 Change Part number
ZZ.CLOSE.001(上綠漆)



Follow Intel CRB



R901 close to CPU



SA
C703, C715 放置 AC22 AE22 AE23

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SSID = CPU

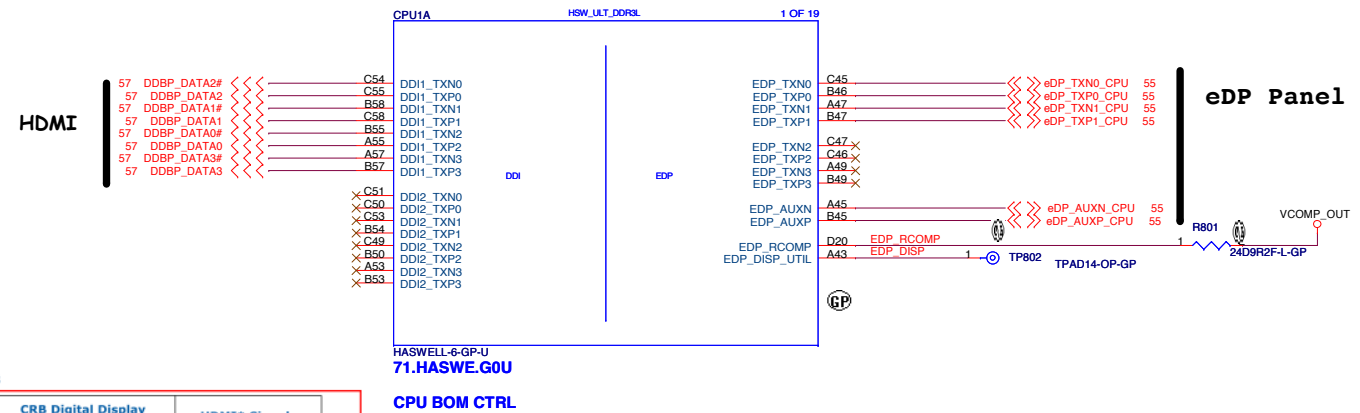
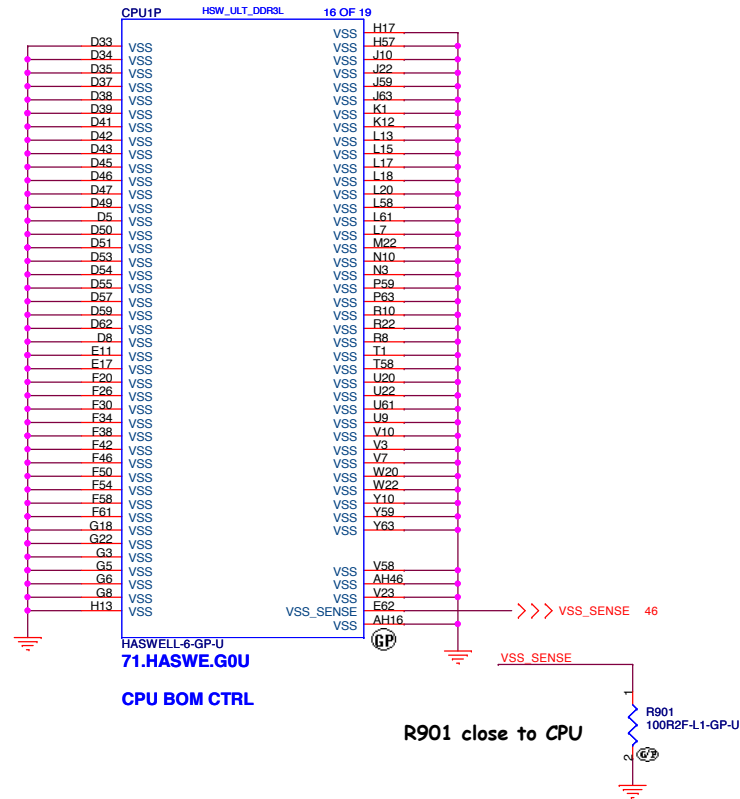


Table 19-1. Mapping of HDMI* signals for DDI ports

Port	Digital Display Interface Pins	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIx_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CLK
Port 2	DDI2_TXP[0]	DDI2_LANE0_DP	HDMIx_TX2_DP
	DDI2_TXN[0]	DDI2_LANE0_DN	HDMIx_TX2_DN
	DDI2_TXP[1]	DDI2_LANE1_DP	HDMIx_TX1_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMIx_TX1_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMIx_TX0_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMIx_TX0_DN
	DDI2_TXP[3]	DDI2_LANE3_DP	HDMIx_CLK_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 2	DDPC_HPD	DDI2_HPD_Q
	HDMI DDC lines for Port 2	DDPC_CTRLCLK	DDI2_CTRL_CLK

SSID = CPU



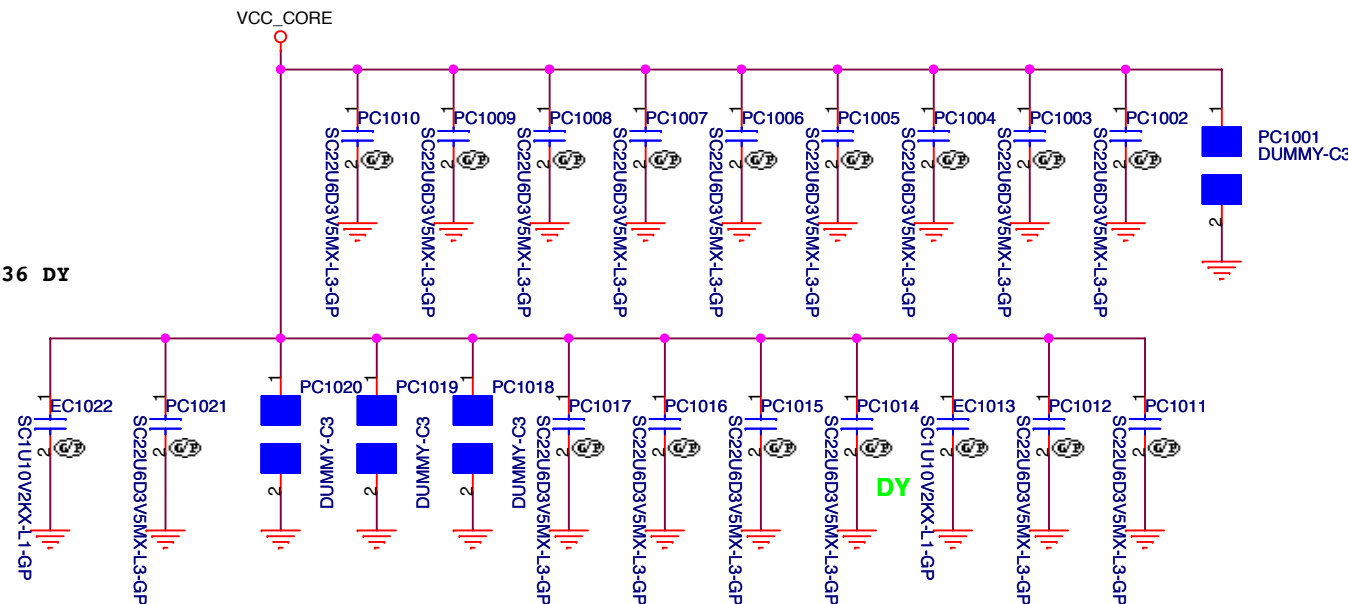
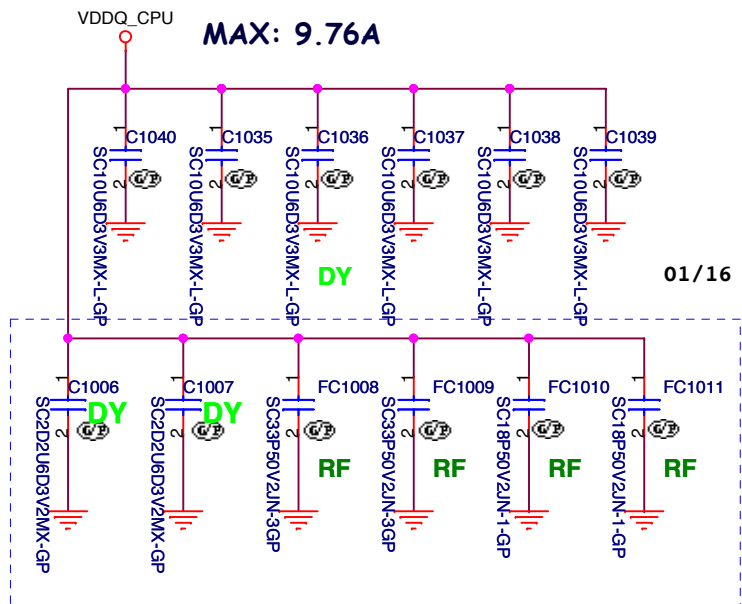
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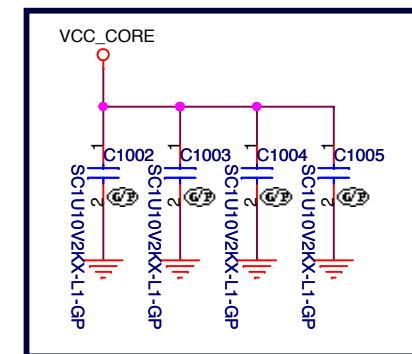
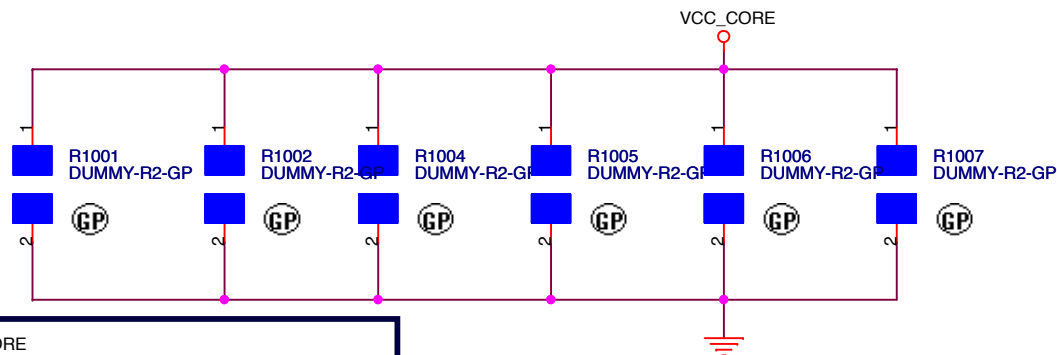
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Size A3	Document Number LT41	Rev -1

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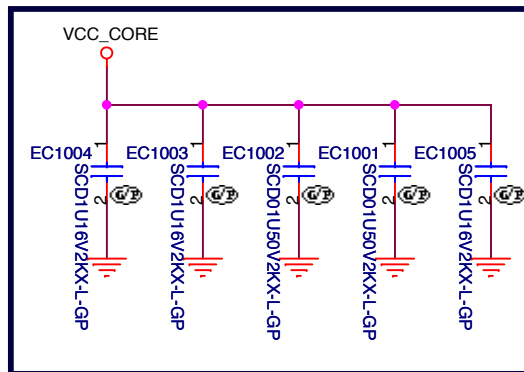


For Intel Recommend EE Part
 10/19 Change C1008, C1009 to RC1008, RC1009 (2.2uF to 33pF)
 10/19 add RC1010, RC1011 18pF

12/18 PC1013 改為EC1013 FOR EMI, 1uF 上件
 12/18 PC1022 改為EC1022 FOR EMI, 1uF 上件



For Intel Recommend EE Part



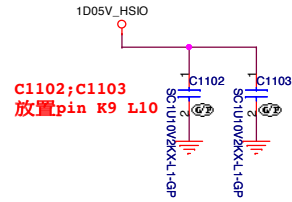
For EMC Recommend

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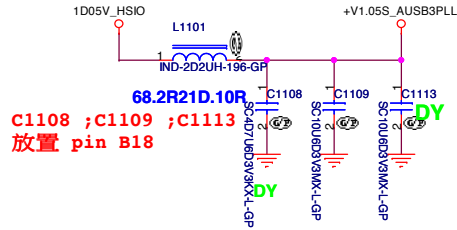
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU (Power CAP1)		
Size A4	Document Number LT41	Rev -1
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擺放電容的位置請參考Page 21
每個位置如下

MAX: 1.92A

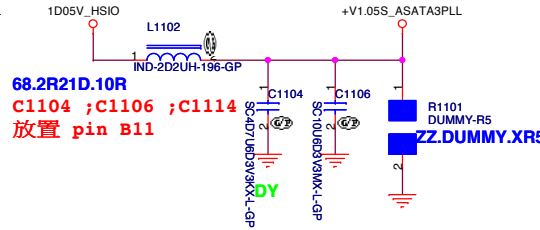


C1102;C1103
放置 pin K9 L10



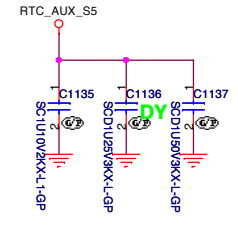
C1108 ;C1109 ;C1113
放置 pin B18

01/16 C1108 DY



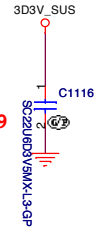
C1104 ;C1106 ;C1114
放置 pin B11

01/16 C1104 DY

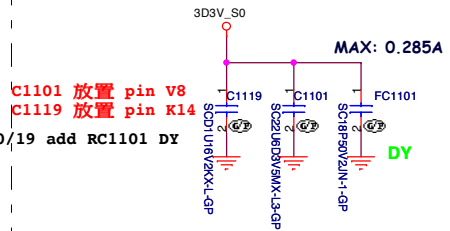


C1135;C1136;C1137
放置 pin AG10

MAX: 3.51A

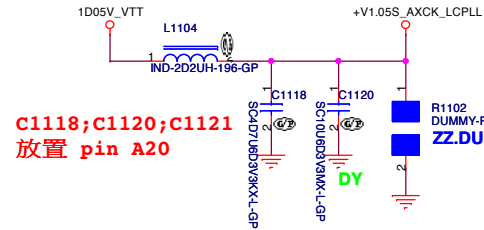


C1116放置 pin AC9

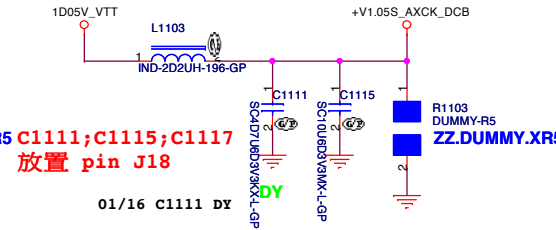


C1101 放置 pin V8
C1119 放置 pin K14

10/19 add RC1101 DY

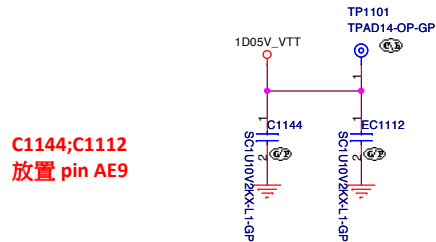


C1118;C1120;C1121
放置 pin A20



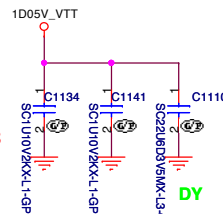
C1111;C1115;C1117
放置 pin J18

01/16 C1111 DY



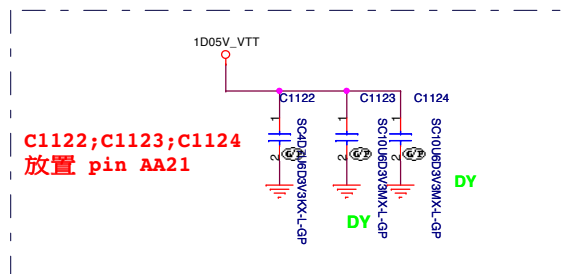
C1144;C1112
放置 pin AE9

12/18 C1112 改為EC1112 FOR EMI, 1uF 上件



C1110 放置 pin J11
C1134 C1141 放置 pin J11, AE8

01/16 C1110 DY



C1122;C1123;C1124
放置 pin AA21

01/16 C1123 DY

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SSID = MEMORY

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D				
C				
B				
A				

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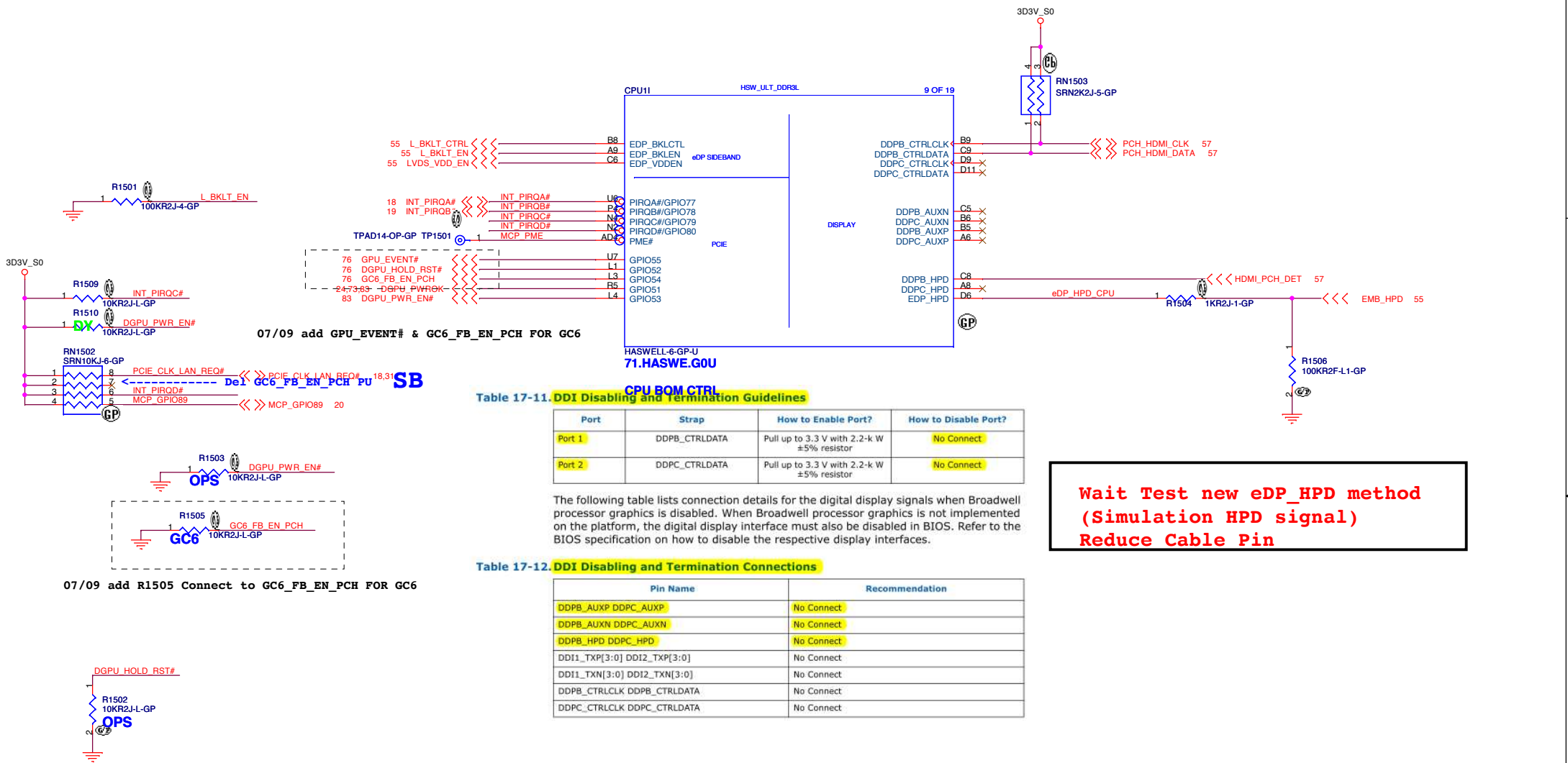


Table 17-11. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k W $\pm 5\%$ resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k W $\pm 5\%$ resistor	No Connect

The following table lists connection details for the digital display signals when Broadwell processor graphics is disabled. When Broadwell processor graphics is not implemented on the platform, the digital display interface must also be disabled in BIOS. Refer to the BIOS specification on how to disable the respective display interfaces.

Table 17-12. DDI Disabling and Termination Connections

Pin Name	Recommendation
DDPB_AUXP DDPC_AUXP	No Connect
DDPB_AUXN DDPC_AUXN	No Connect
DDPB_HPD DDPC_HPD	No Connect
DDI1_TXP[3:0] DDI2_TXP[3:0]	No Connect
DDI1_TXN[3:0] DDI2_TXN[3:0]	No Connect
DDPB_CTRLCLK DDPC_CTRLCLK	No Connect
DDPB_CTRLCLK DDPC_CTRLDATA	No Connect

Wait Test new eDP_HPD method
(Simulation HPD signal)
Reduce Cable Pin

BOM1

SSID = PCH

USB2.0 Table

Pair	Device
0	USB3.0 Port 1 (USB_OC#0)
1	USB3.0 Port 2 (with Debug Function) (USB_OC#1)
2	NC
3	Camera
4	USB2.0 Port 4 (USB_OC#2)
5	WLAN(Bluetooth)
6	NC
7	Panel Touch

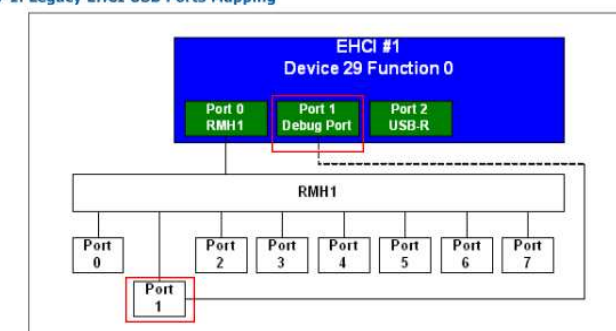
USB3.0 Table

Pair	Device
1	USB3.0 Charger Port 1
2	USB3.0 Port 2
3	Reserved
4	USB3.0 Card Reader Port 2

USB3.0 SKT1

USB3.0 SKT2

Figure 15-1. Legacy EHCI USB Ports Mapping



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Title

CPU (PCI/USB)

Size
A3

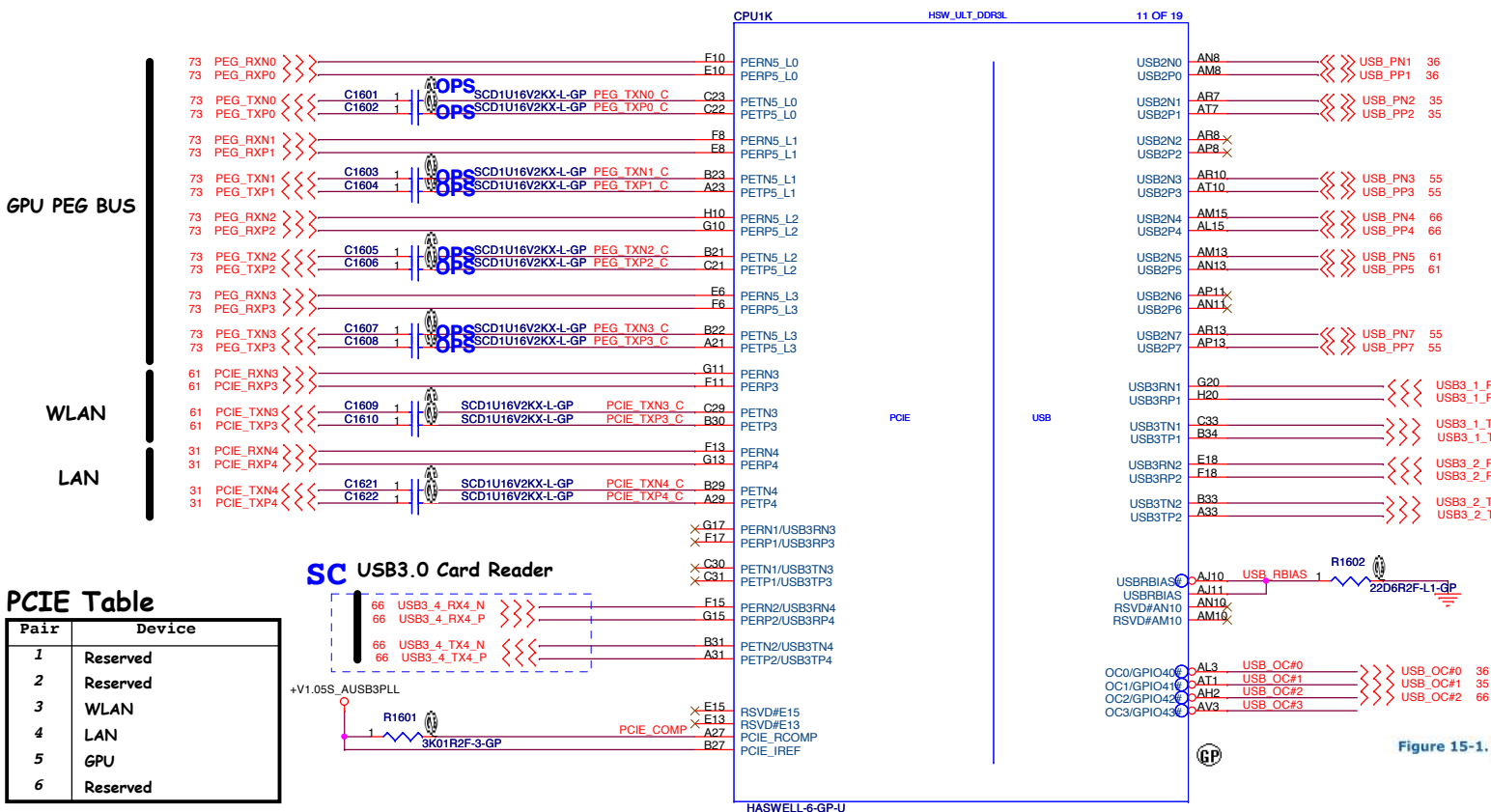
Document Number

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71.HASWE.G0U

CPU BOM CTRL

PCIe Table

Pair	Device
1	Reserved
2	Reserved
3	WLAN
4	LAN
5	GPU
6	Reserved

SC USB3.0 Card Reader

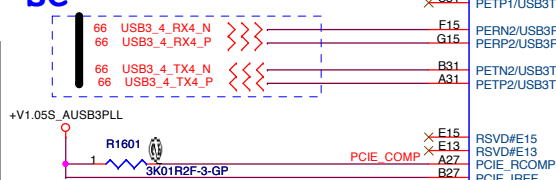
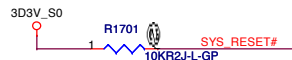


Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0 SSD	PCIe* Port 5 Lane 1 SSD	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3

SSID = PCH

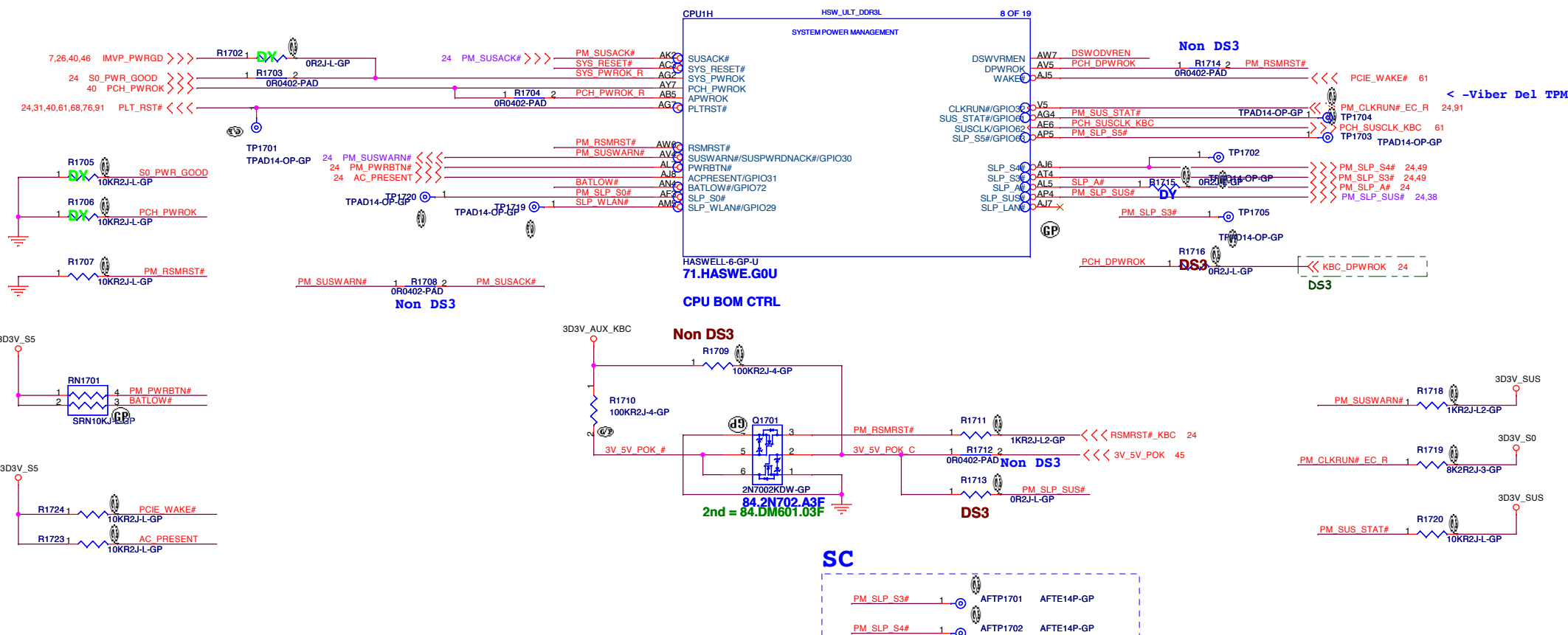
Follow Intel CRB



Bit	Description
31:3	Reserved
2	<p>WAKE# Pin Deep Sx Enable (WAKE_PIN_DSX_EN) - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case). When this bit is '0':</p> <ul style="list-style-type: none"> Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time. Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled. <p>NOTE: Deep Sx disabled configuration must leave this bit at '0'.</p>

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

The diagram illustrates the connection of the DSWODVREN signal to the RTC_AUX_S5 pin. The DSWODVREN signal is connected to the R1722 pin of the 330KR2J-L-GP component. The R1721 pin of the same component is connected to the RTC_AUX_S5 pin. The component is also connected to ground via the R1722 pin.



BOM1

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (DMV/FDI/PM)

Size

Document Number

LT41

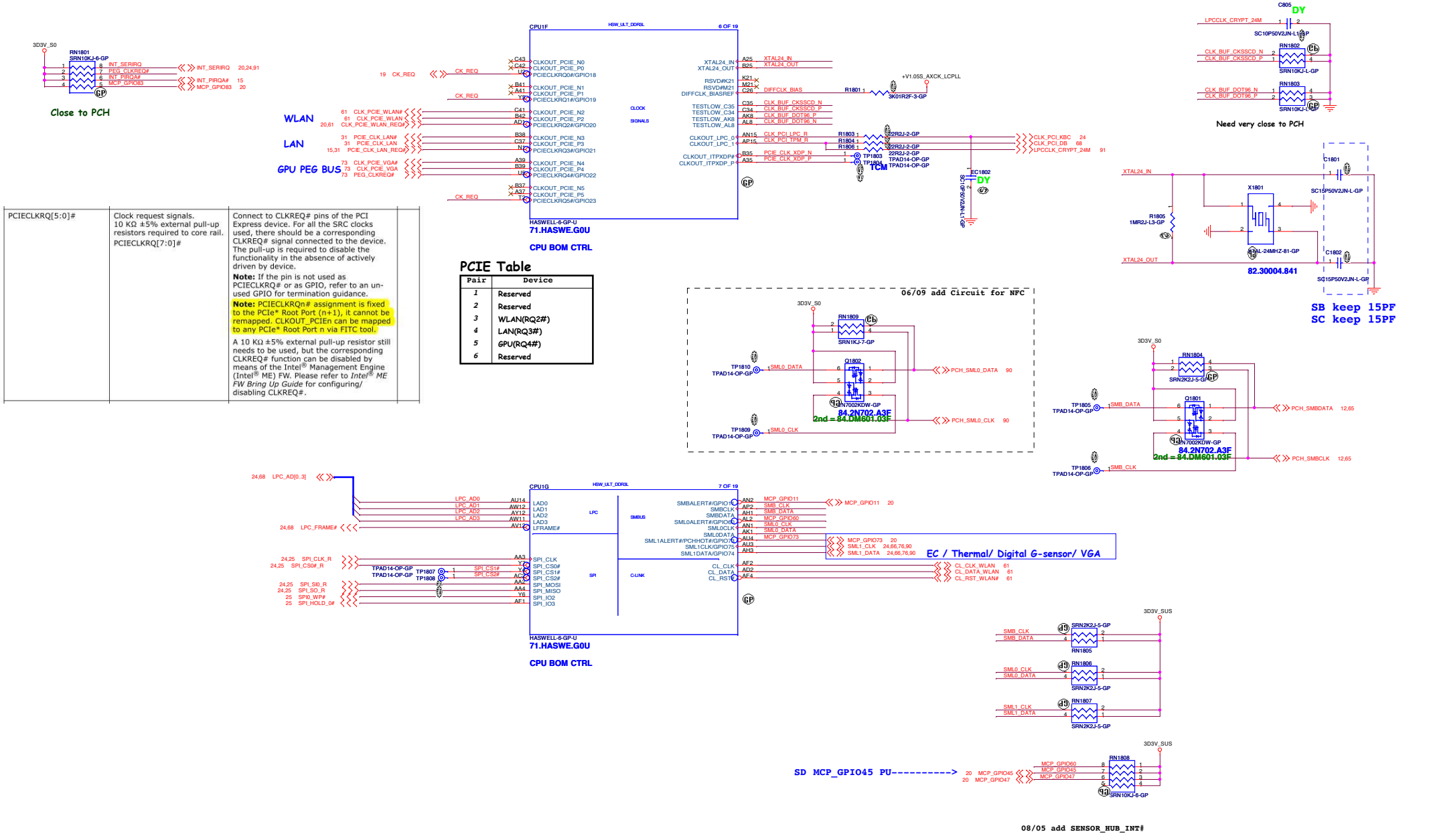
Date: Tuesday, January 20, 2015

Sheet 17 of 102

Rev

10

SSID = PCH



SSID = PCH

X1901 32D768KHZ BDW U SPEC:

32 Real Time Clock (RTC) Design Guidelines

Note: Unless otherwise indicated, this content pertains to Broadwell-U, Broadwell-Y and Broadwell-E chip platforms. Information relating specifically to one platform only (Broadwell-U, Broadwell-Y or Broadwell-E) will be marked with "BDW-U", "BDW-Y" or "BDW-E" in paragraph margins as appropriate.

Note: Has Crystal 32K ± 100ppm

The PCH contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

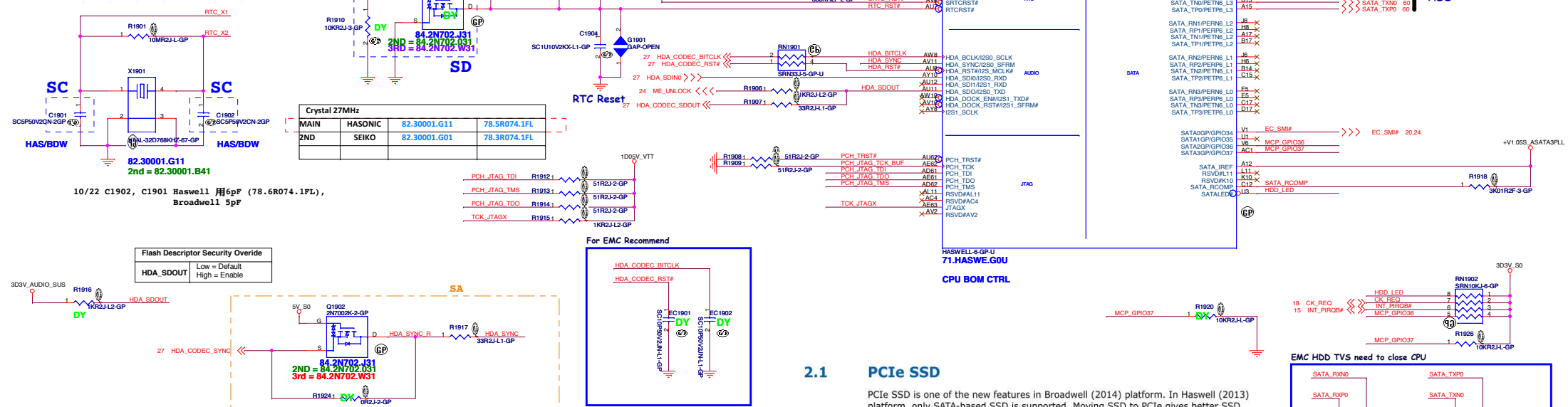


Table 1-3. Broadwell U PCH-LP SKUs—Flexible I/O Map

SKU	High Speed I/O Ports													
	Port 1	Port 2	Port 3	Port 4	Port 5	Port 6	Port 7	Port 8	Port 9	Port 10	Port 11	Port 12	Port 13	Port 14
Premium	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	SATA 6Gb/s Port 3	SATA 6Gb/s Port 2	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD							PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	PCIe* Port 6 Lane 2	PCIe* Port 6 Lane 3
Base	USB 3.0 Port 1	USB 3.0 Port 2	USB 3.0 Port 3	USB 3.0 Port 4	PCIe* Port 3	PCIe* Port 4	PCIe* Port 5 Lane 0	PCIe* Port 5 Lane 1	PCIe* Port 5 Lane 2	PCIe* Port 5 Lane 3	PCIe* Port 6 Lane 0 SSD	PCIe* Port 6 Lane 1 SSD	SATA 6Gb/s Port 1	SATA 6Gb/s Port 0
			PCIe* Port 1 SSD	PCIe* Port 2 SSD										

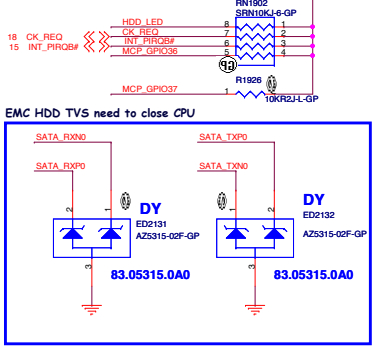
2.1

PCIe SSD

PCIe SSD is one of the new features in Broadwell (2014) platform. In Haswell (2013) platform, only SATA-based SSD is supported. Moving SSD to PCIe gives better SSD performance over previous generation. M.2 Socket 2 supports both SATA and PCIe based SSDs. Figure below shows the configuration of High Speed I/Os in 2013/2014 PCH. The Haswell board can be made ready for both, the optional PCIe SSD and SATA SSD, by routing PCIe Port 6 Lane 0 and Lane 1 to the M.2 Socket 2 connector. For details on M.2 signals and pins for SATA and PCIe, please refer to Documentation Table below, M.2 row.

2-1. Configuration of High Speed I/Os in 2013/2014

USB3 P1	USB3 P2	PCIe P1 NAND	PCIe P2 NAND	PCIe P3 GbE	PCIe P4 GbE	PCIe P5 L0 NAND	PCIe P5 L1 NAND	PCIe P5 L2	PCIe P5 L3	PCIe P6 L0 NAND	PCIe P6 L1 NAND	PCIe P6 L2	PCIe P6 L3
Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7	Lane 8	Lane 9	Lane 10	Lane 11	Lane 12	Lane 13	Lane 14



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File CPU (RTC/LPC/SATA/HDA)
Size Custom Document Number LT41 Rev -1
Date: Tuesday, January 20, 2015 Sheet 19 of 102

SSID = PCH

Thermal

Thermal
NCT7718: 1
Thermal VD : 0

NCT7718&TV

SKU	Fun./Location	7718/TV
SKU1,2	R2037	ASM
SKU3	R2036	ASM

SB

08/06 add SENSOR_HUB_INT#

08/14 add NFC Detect pin

08/05 add SENSOR_HUB_INT#

Default:Low

UMA&OPS

DGPU_PRST#

UMA: 1
Optimus(Muxless) : 0

UMA&OPS

SKU	Fun./Location	UMA/DIS
SKU1	R2013	ASM
SKU2~5	R2014	ASM

CPU1J

HSW_ULT_DDR3L

10 OF 19

CPU/

MISC

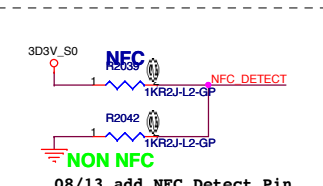
GPIO

SERIAL IO

HASWELL-6-GP-UJ
71.HASWE.G0U

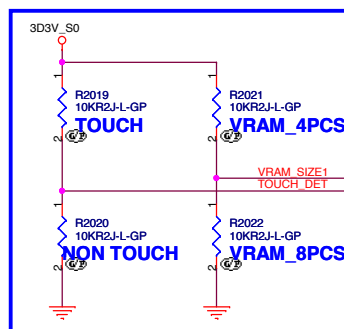
CPU BOM CTRL

6SPI0_MOSI_BB50_R(SSD_PWR)
PU RESERVED
PD SPI BUS



08/13 add NFC Detect Pin

TOUCH&VRAM



VRAM SINGLE&DUAL

Fun./Location	SINGLE	DUAL
R2021	ASM	DY
R2022	DY	ASM

TOUCH

Fun./Location	TOUCH	NON TOUCH
R2019	ASM	DY
R2020	DY	ASM

VRAM 900MHZ&1000MHZ

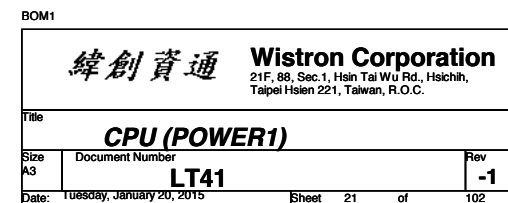
Fun./Location	900MHZ	1000MHZ
R2032	ASM	DY
R2033	DY	ASM

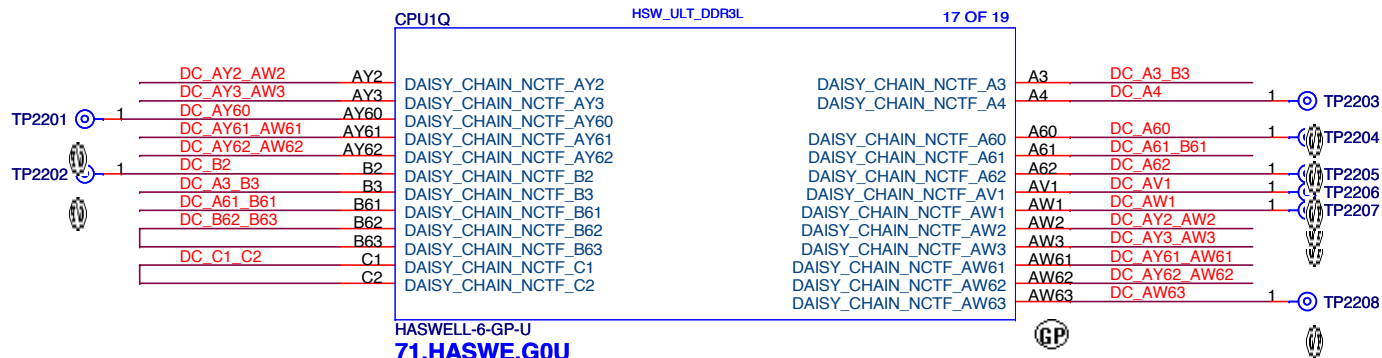
BOM1

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Title	CPU (GPIO/MISC)	
Size	Document Number	Rev
Custom	LT41	-1
Date	Tuesday, January 20, 2015	Sheet 20 of 102

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to [Section 41.3, "Loop Inductance Reduction Decoupling" on page 532.](#)





CPU BOM CTRL

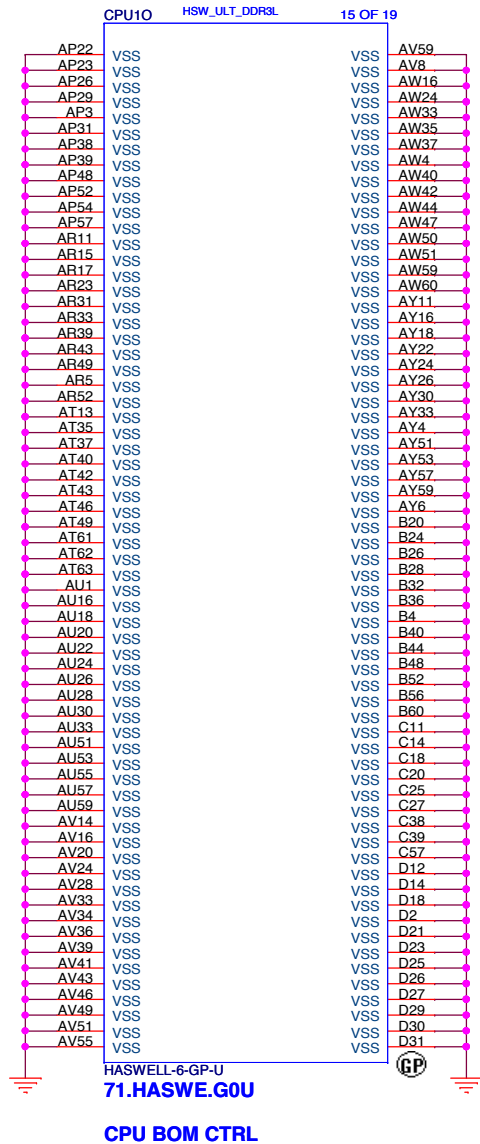
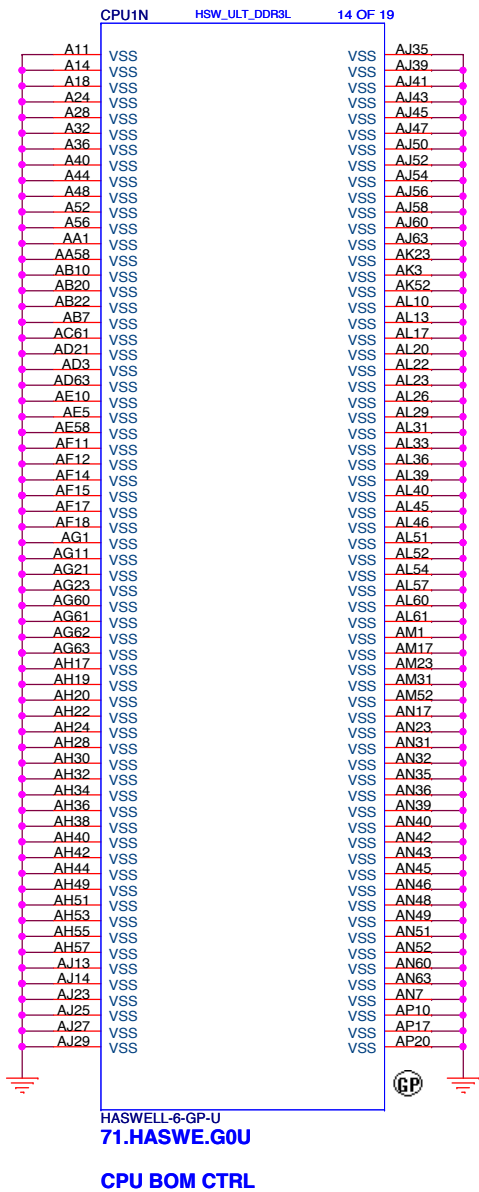


CPU BOM CTRL

BOM1

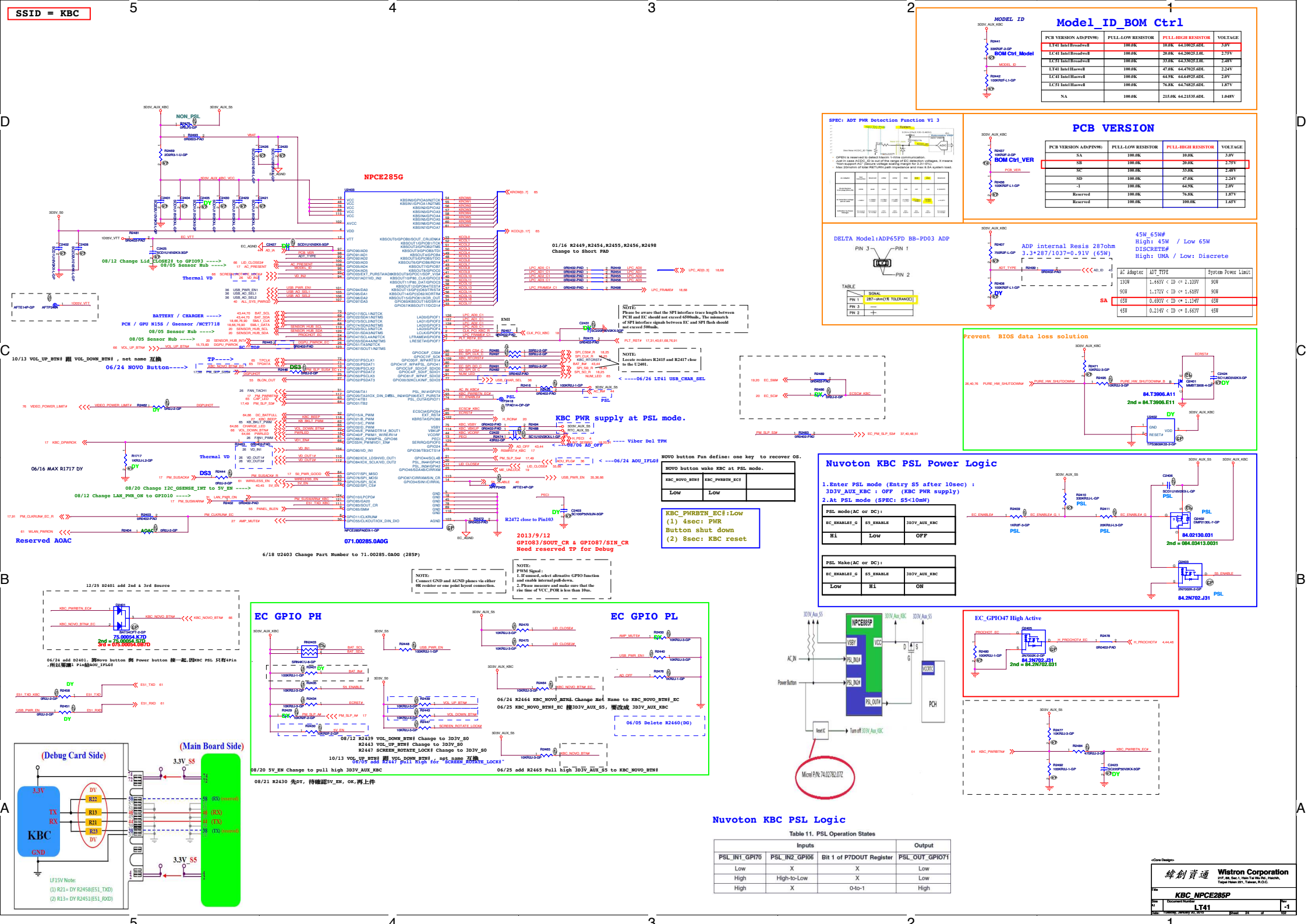
緯創資通		Wistron Corporation	
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Title			
CPU (RSVD)			
Size	Document Number	Rev	
Custom	LT41	-1	
Date:	Tuesday, January 20, 2015	Sheet	22 of 102

SSID = PCH



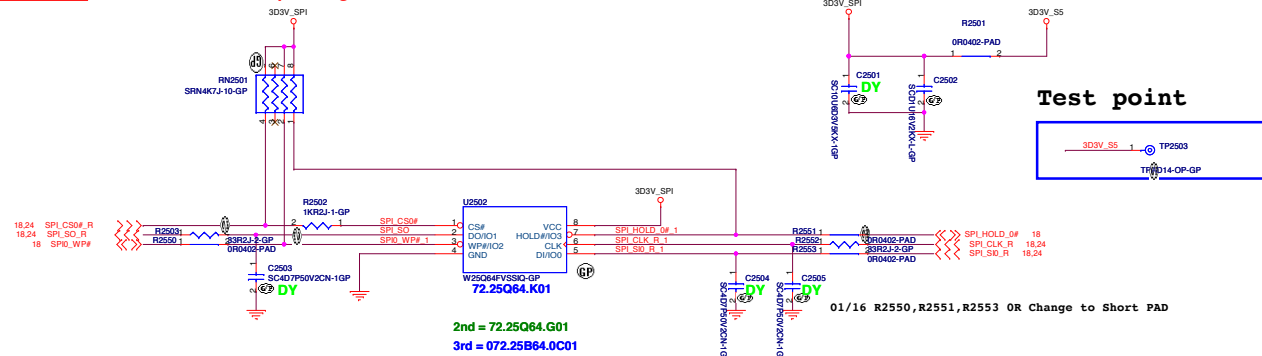
BOM1

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Title			
CPU (VSS)			
Size	Document Number		Rev
Custom	LT41		-1
Date:	Tuesday, January 20, 2015		Sheet 23 of 102



SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil

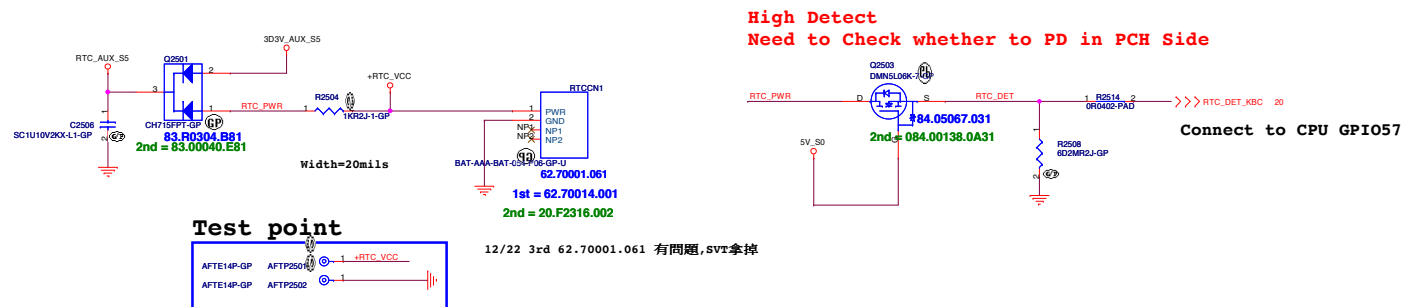


U2502			
Main	Winbond	W25Q64FV	72.25Q64.K01
SC	GIGADEVICE	GD25B64BSIGR	072.25B64.0001
SD	MICRON	N25Q64A13ESEC0F	72.25Q64.G01

Don't use MXIC 72.25647.00A

SSID = RBATT

SSID = RBATT



SSID = Thermal

Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

2.System Sensor, Put on palm rest

Close to Thermal sensor

3D3V_AUX_KBC

TBD

Note: Need R1717 PD: Enable Thermal VD Fun.
Note: (1) VD_IN1 for System sensor
(2) VD_IN2 for CPU sensor

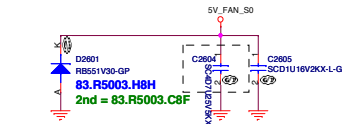
Close to CPU chips

Close to KBC chips

Thermal config

Function LOCATION	Thermal VD	NCT7718W
U2601	DY	ASM
Q2601	DY	ASM
Q2602	DY	ASM
RN2601	DY	ASM
R2601	DY	ASM
R2605	DY	ASM
C2601	DY	ASM
C2602	DY	ASM
C2603	DY	ASM
R2610	ASM	DY
R2619	ASM	DY
R2615	ASM	DY
R2616	ASM	DY
R2612	ASM	DY
R2620	ASM	DY
R2624	ASM	DY
R2625	ASM	DY
C2615	ASM	DY
C2617	ASM	DY
C2616	ASM	DY
C2618	ASM	DY
D2603	ASM	DY
R1717	ASM	DY

Layout 15 mil



07/31 C2604 Change part number 78.47523.5BL to 78.47522.L4L,
值为4.uF, 0805, 不同的是25V

24 FAN1_PWM >>>

FAN_TACH1_C

5V_FAN_S0

3D3V_S0

R2614

10KR2J-L-GP

5V_FAN_S0

R2613

10KR2J-L-GP

83.R5003.H8H

2nd = 83.R5003.C8F

10/27 R2617 DY改上件

12/18 R2617 Change to Short PAD

DY

R2618

OR2J-L-GP

3D3V_S0

1 R2617

OR2J-L-GP

3D3V_S0

R2624

2KR2F-3-GP

DY

R2625

2KR2F-3-GP

DY

R2603

BAW56-5-GP

DY

83.00056.Q11

2nd = 75.00056.07D

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24.40.78 PURE_HW_SHUTDOWN# <<<

R2606

10KR2J-L-GP

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84.2N702.J31

2ND = 84.2N702.031

3rd = 84.2N702.W31

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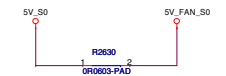
DY

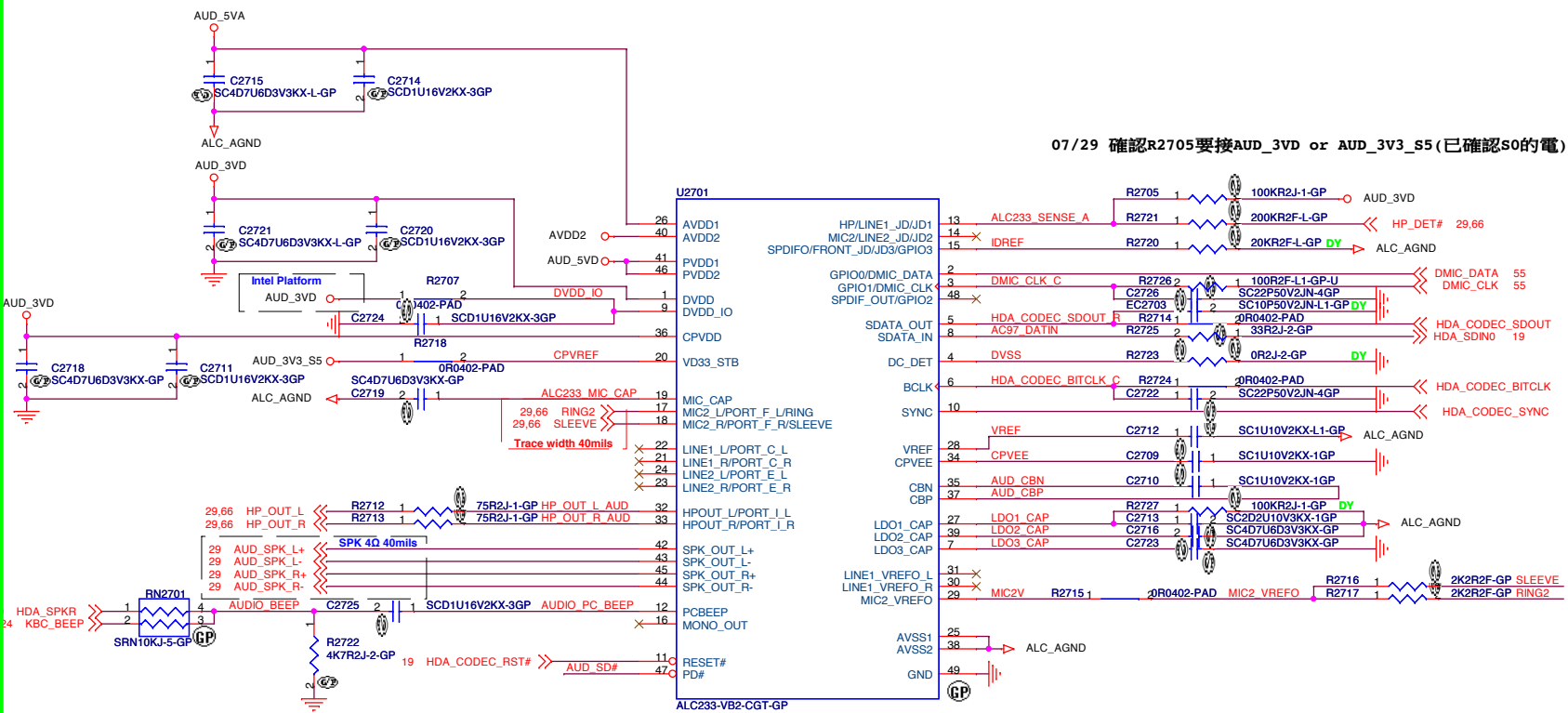
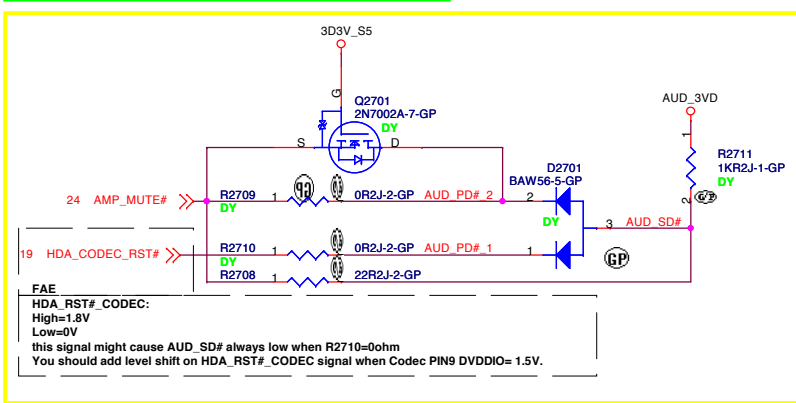
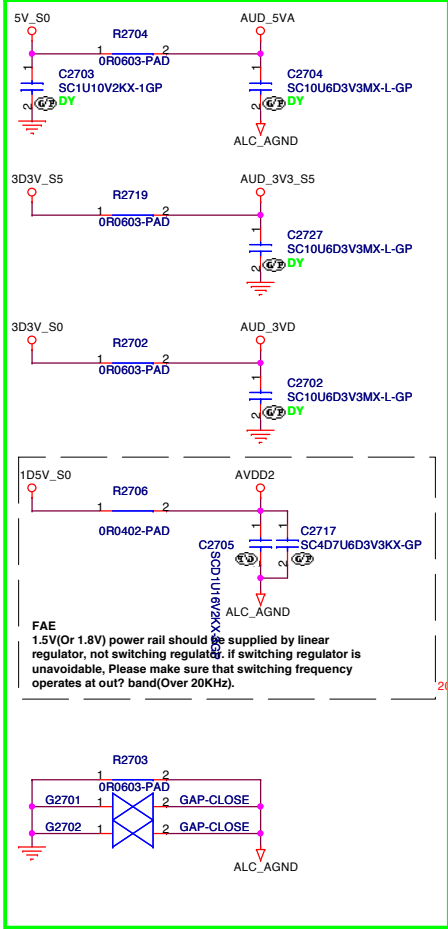
T8=85 degree

ALERT# /T CRIT#
Pull-up Resistor

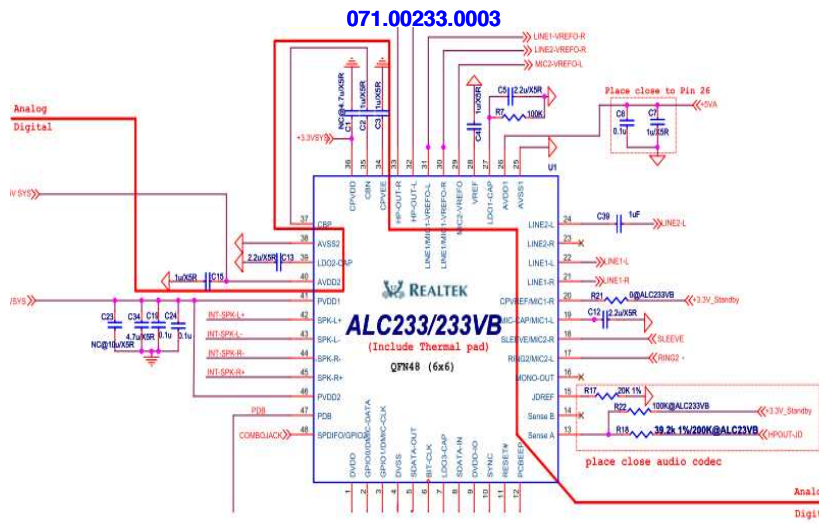
R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
77°C	87°C	97°C	107°C	117°C	
79°C	89°C	99°C	109°C	119°C	
81°C	91°C	101°C	111°C	121°C	
83°C	93°C	103°C	113°C	123°C	
85°C	95°C	105°C	115°C	125°C	

T_CRIT temperature strapping point





07/29 確認R2705要接AUD_3VD or AUD_3V3_S5(已確認S0的電)



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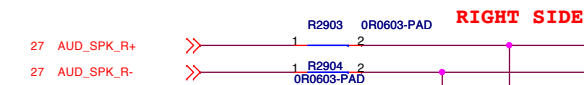
Title			
027 Audio Codec ALC233-VB2-CGT			
Size A3	Document Number		Rev
	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet 27 of	102



BOM1

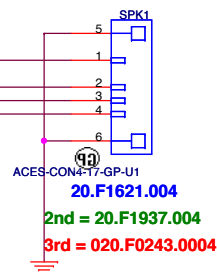
<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia,</div>		<div>Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			
Audio Codec ALC233(Reserved)			
Size	Document Number		Rev
A2	LT41		-1
Date	Tuesday, January 20, 2015		Sheet 26 of 102

INTERNAL STEREO SPEAKERS



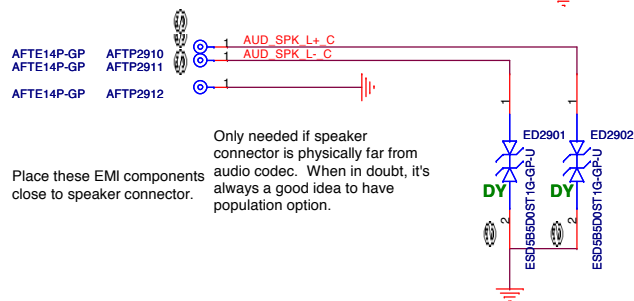
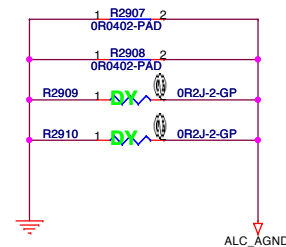
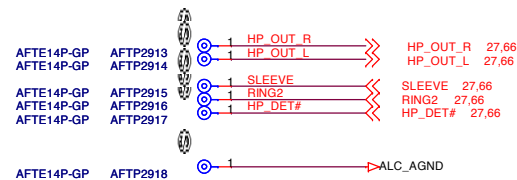
Place these EMI components close to speaker connector.

Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.



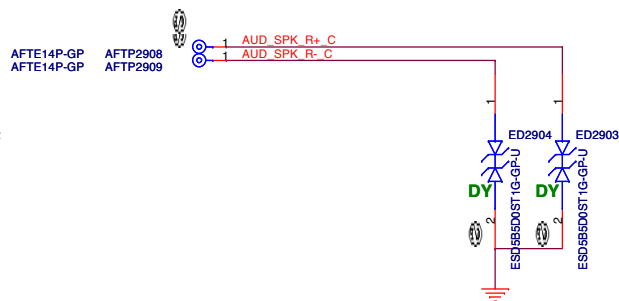
08/12 SPK1 20.F2348.007 Change to 20.F1621.004

06/12 SPK1 原本為4Pin, 換7 pin 接 Hall Sensor 訊號



Place these EMI components close to speaker connector.

Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.

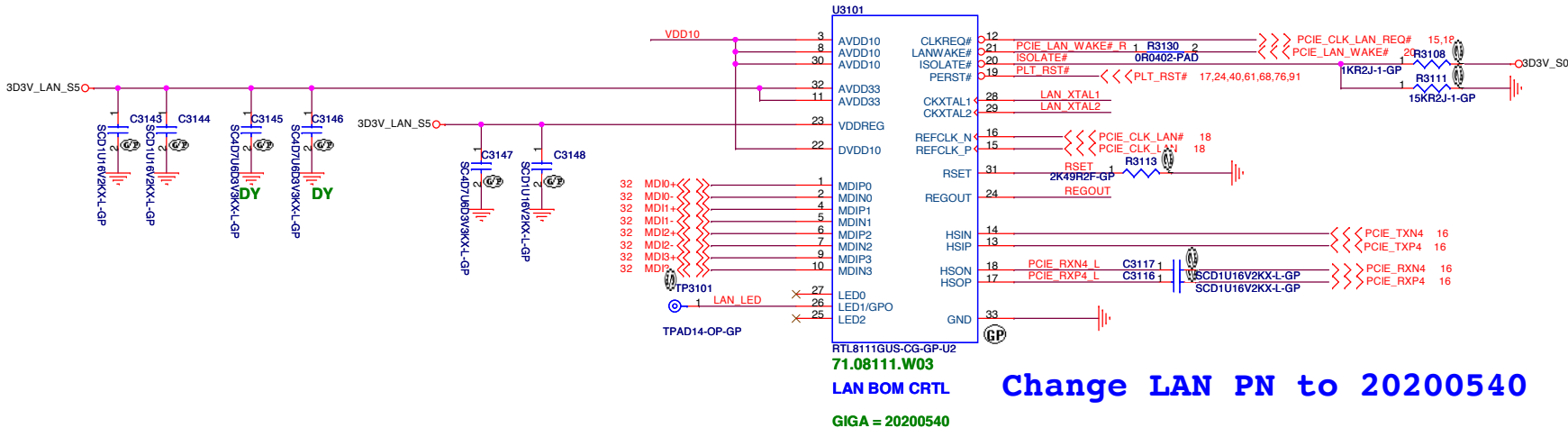
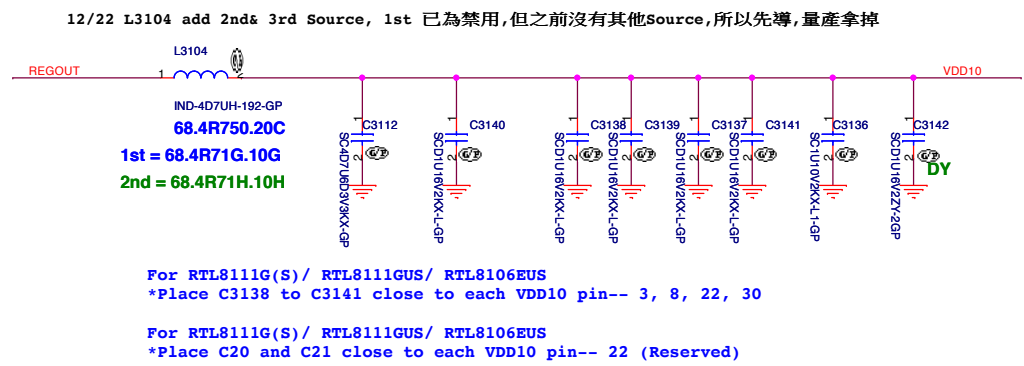
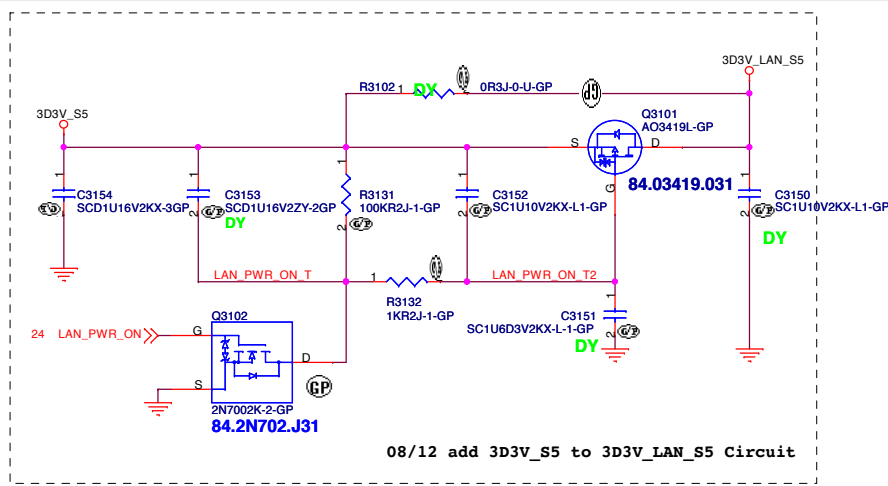


BOM1

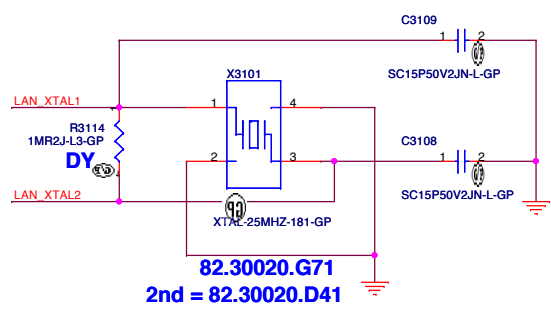
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
MIC/SPEAKER/AUDIO JACK			
Size	Document Number		Rev
Custom	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet 29 of	102

5	4	3	2	1
D				D
C				C
B				B
A				A
			BOM1	
			<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>	
			<div>Title</div> <div>Audio Jack_ (Reserved)</div>	
			<div>Size</div> <div>Custom</div>	<div>Document Number</div> <div>LT41</div>
			<div>Date:</div> <div>Tuesday, January 20, 2015</div>	<div>Rev</div> <div>-1</div>
			<div>Sheet</div> <div>2</div>	<div>30 of 102</div> <div>1</div>



25MHz XTAL



Crystal 27MHz			
MAIN	HASONIC	82.30020.G71	78.15034.L1L
2ND	HARMONY	82.30020.D41	78.18034.1FL

LAN and Transformer Config:

LAN/Transformer	
RTL8111GUL 1000M 20200540	
1000M Transformer 068.IH219.3001	Main source
1000M Transformer 68.89246.301	2nd source

BOM1

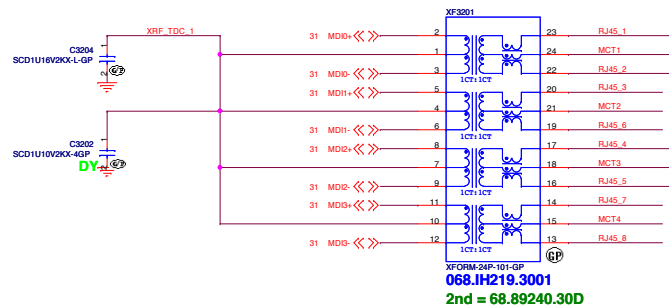
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN RTL8111GUL**

Size A3 Document Number: **LT41** Rev: **-1**

Date: Tuesday, January 20, 2015 Sheet 31 of 102

10/100M/1000M Lan Transformer

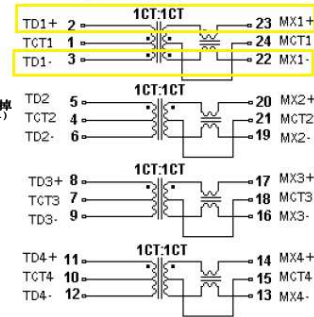


1000M Lan Transformer pin define

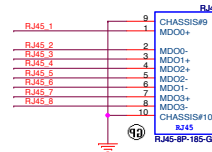
Part Number	Insertion Loss (dB Max) 1-100MHz	Return loss (dB MIN @100MHz)			
IH-106-A	-1.0	-18	-14.4	-13.1	

SCHEMATICS :

Pin Define



LAN Connector



022.10001.00A1

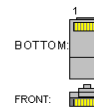
2nd = 022.10001.0571

08/13 RJ45 22.10019.141 Change to 022.10001.00A1

RJ45 Pin define

Pin	Description	10base-T	100Base-T	1000Base-T
1	Transmit Data+ or BiDirectional	TX+	TX+	BL_DA+
2	Transmit Data- or BiDirectional	TX-	TX-	BL_DA-
3	Receive Data+ or BiDirectional	RX+	RX+	BL_DB+
4	Not connected or BiDirectional	n/c	n/c	BL_DC+
5	Not connected or BiDirectional	n/c	n/c	BL_DC-
6	Receive Data- or BiDirectional	RX-	RX-	BL_DB-
7	Not connected or BiDirectional	n/c	n/c	BL_DD+
8	Not connected or BiDirectional	n/c	n/c	BL_DD-

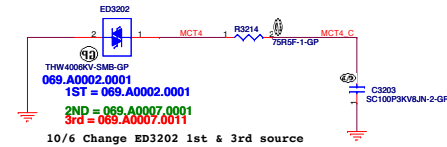
The connector is 8 pin RJ45 (8P8C) male



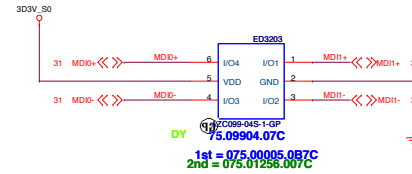
The associated connector is 8 pin RJ45 (8P8C) female



10/100/1000 LAN surge circuit For test stuff

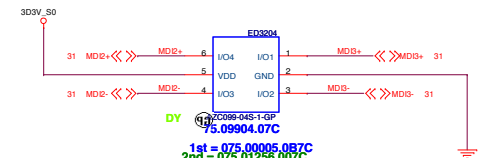


10/6 Change ED3202 1st & 3rd source



1st = 075.00005.087C

2nd = 075.01256.007C



1st = 075.00005.087C

2nd = 075.01256.007C

8/25 將ED3203,ED3204 屬性ESD STUFF OPTION 改成DY, 上件會無法Wake on Lan

10/13 ED3203,ED3204 改成跟ED3501一樣, 增加三個Source

10/23 將3rd Source拿掉 75.09904.07C, 因為已有案子50米網線測不過(Part number跟ED3501一樣,BOM別帶錯)

10/23 ED3203, ED3204 ESD STUFF OPTION改 DY,不上件

LAN and Transformer Config:

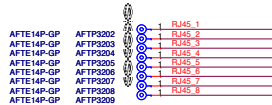
LAN/Transformer	
RTL8111GUL 1000M 20200540	
1000M Transformer 068.IH219.3001	Main source
1000M Transformer 68.89246.301	2nd source

12/18 3rd 068.24101.3041 是Wendell的料,EMI測試不通過,所以拿掉

12/18 2nd 68.89246.301 為要成料,新導入,(原本為68.89246.301)

1000M Transformer PN:

068.01010.3001 (AZ chip)



06/13 Delete LAN_AGND

AZ&NON AZ

Function LOCATION	AZ	NON AZ
ED3102	DY	ASM
R3114	DY	ASM
ED3103	ASM	DY
ED3104	ASM	DY
ED3105	ASM	DY
ED3106	ASM	DY
ED3107	ASM	DY
ED3108	ASM	DY
R3112	ASM	DY
R3115	ASM	DY
R3116	ASM	DY
R3117	ASM	DY
R3118	ASM	DY
R3119	ASM	DY
R3120	ASM	DY

BOM1

緯創資通 Wistron Corporation
21F, 6F, Sec. 1, Hsin Ta Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

LAN CONNECTOR		
Size	Document Number	Rev
A2	LT41	-1
Date:	Tuesday, January 20, 2015	Sheet 32 of 102

5	4	3	2	1
D				D
C				C
B				B
A				A

BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
CARD Reader		
Size	Document Number	Rev
A4	LT41	-1
Date: Tuesday, January 20, 2015		Sheet 33 of 102

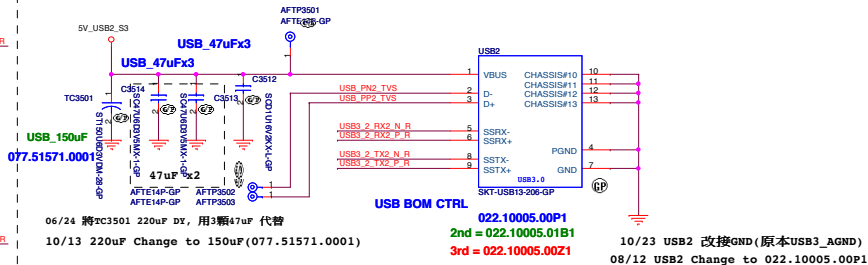
	5	4	3	2	1
D					
C					
B					
A					

BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div>			
<div>USB2.0 CONN</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A3</div>	<div>LT41</div>		<div>-1</div>
<div>Date:</div>	<div>Tuesday, January 20, 2015</div>		<div>Sheet 34 of 102</div>



12/22 增加AFTP3506 測點

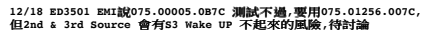


```
12/23 增加LC41& LC51 USB CONN, 沒削型的CONN
      1st 022.10005.01U1
      2nd 022.10005.01W1
      3rd 022.10005.01V1
```



06/25 ED3501 VDD change Net Name to 5V_USB1_S3

12/24 ED3501 只導1st 075.00005.0B7C, 其他2nd & 3rd 不導人, 會有Wake up 不起來的風險



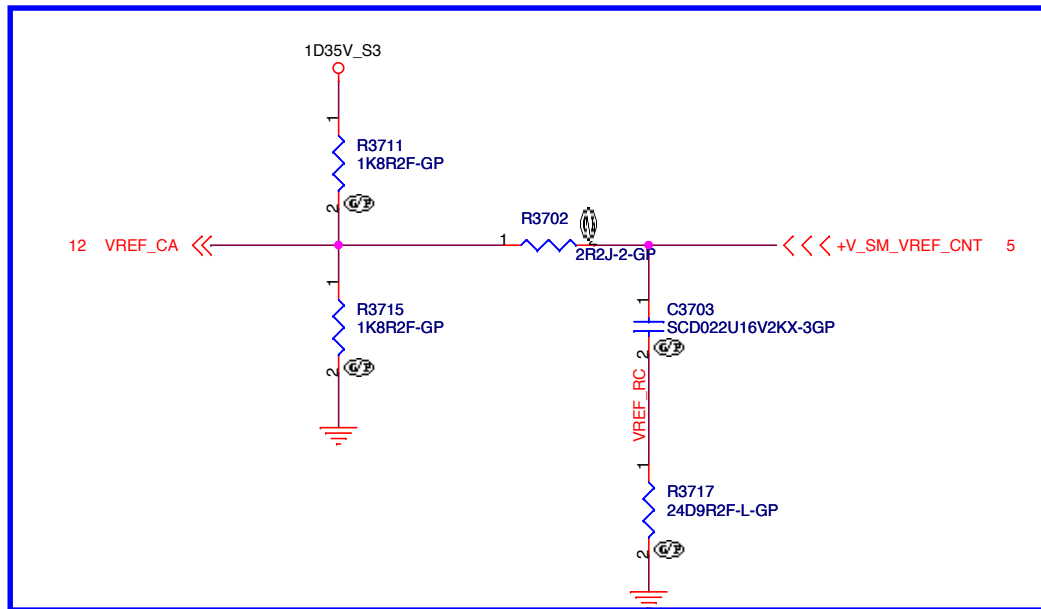
10/28 1st 75.00005.C7C改為 075.00005.0B7C
6/17 ED3501 Change Part Number to 75.09904.07C
與 ED3602 合併,共用一顆ESD

BOM1

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB3.0 CONN
-------	--------------------

Size A2	Document Number LT41	Rev -1
Date: Tuesday, January 20, 2015	Sheet 35 of	102



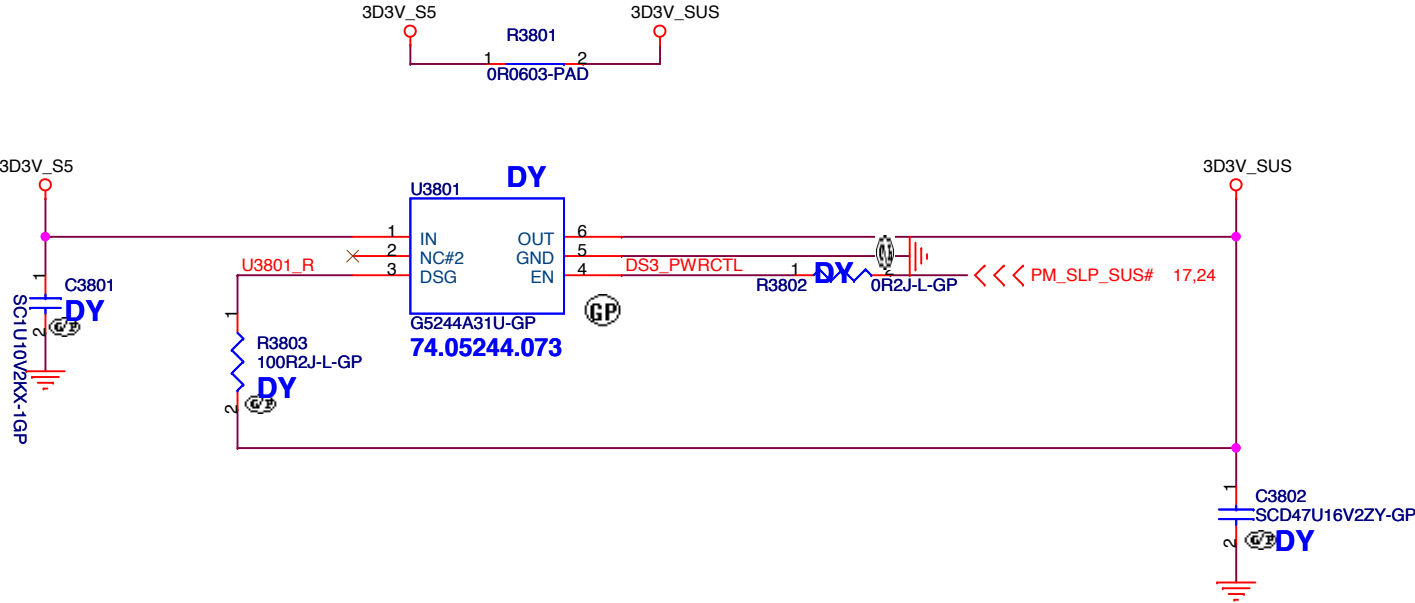
For Intel Recommend Close to DIMM

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ADAPTER OCP / S3 reduction	
Size Custom	Document Number LT41
Date: Tuesday, January 20, 2015	Rev -1
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DS3

Function LOCATION	DS3	NON DS3
R3801	DY	ASM
R1712	DY	ASM
R1709	DY	ASM
R1714	DY	ASM
C3802	ASM	DY
R1713	ASM	DY
R1716	ASM	DY
R2444	ASM	DY
R2446	ASM	DY
R2487	ASM	DY
R3802	ASM	DY
R3803	ASM	DY
U3801	ASM	DY
C3801	ASM	DY



BOM1

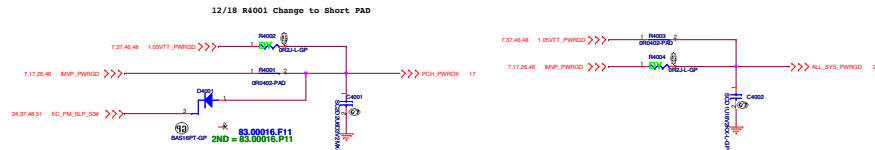
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title (Reserved)		
Size A4	Document Number LT41	Rev -1
Date: Tuesday, January 20, 2015	Sheet 38 of 102	

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

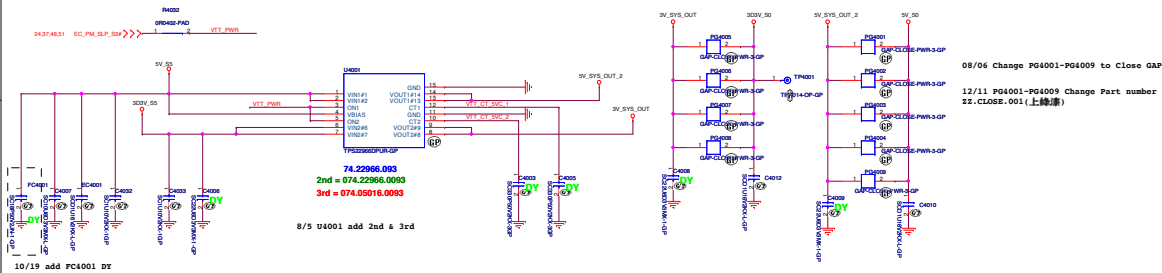
BOM1

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
1D05 M			
Size	Document Number		Rev
Custom	LT41		-1
Date:	Tuesday, January 20, 2015		Sheet 39 of 102

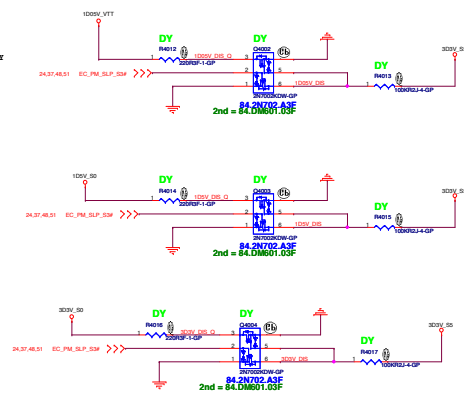
Power Sequence



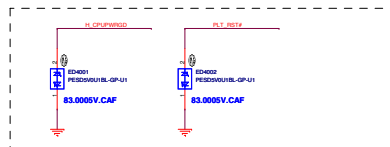
Run Power



Discharge circuit



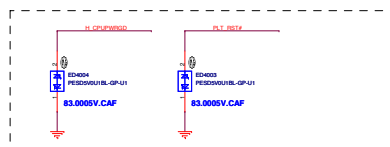
10/17 Delete 放電線路



10/16 add ED4001, ED4002

10/27 EMI上錯料, (083.00105.00AF)才是對的, 先把原來的DY

12/18 ED4001, ED4002 change Part Number to 83.0005V.CAF



12/18 add ED4003, ED4004 83.0005V.CAF

5	4	3	2	1
D				D
C				C
B				B
A				A

BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title	
Connected Standby1	
Size	Document Number
A	LT41
Date:	Rev
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Sheet	41 of 102

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>			
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title					
<div>Connected Standby2</div>					
Size	Document Number		Rev		
A	LT41		-1		
Date:	Tuesday, January 20, 2015	Sheet 42 of	102		



Pin#	Symbol	Comments
1	BATT+	Battery Positive Power
2	BATT+	Battery Positive Power
3	Clock	SMBus clock interface I/O pin
4	Data	SMBus data interface I/O pin
5	Detection	Connect to 10kohm resistor
6	RTC	Support RTC power or reserved
7	GND -	Common Ground Power
8	GND -	Common Ground Power

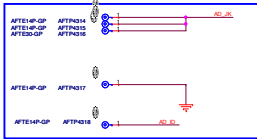
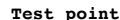
It is required to follow Lenovo common connector requirement for both battery side and system side

Adaptor in to generate DCBATOUT

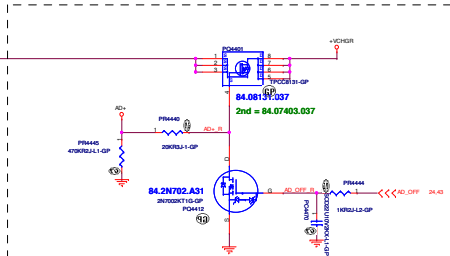
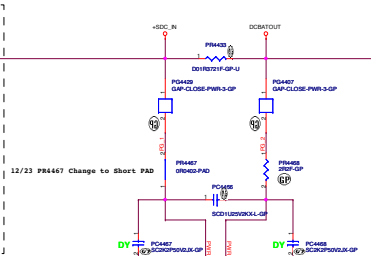
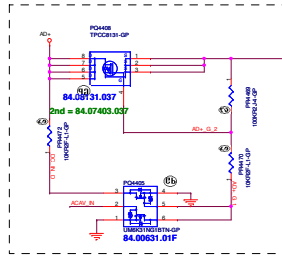


MB_Side		Cable
		Max. Current
Pin 1	AD JK F	UL10064A WG28# (3A)
Pin 2	AD JK F	UL10064A WG28# (3A)
Pin 3	AD ID	UL10064A WG28# (3A)
Pin 4	GND	UL10064A WG26# (3.8A)
Pin 5	GND	UL10064A WG26# (3.8A)

印字面在下



 Wistron Corporation 21F, 21F, Sec. 1, Hsin Yi Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.	
DCIN JACK & BATT Conn	
LT41	
Date: _____	Rev: -1



06/25 PQ4408 & PQ4411 Change to 84.08065.B37

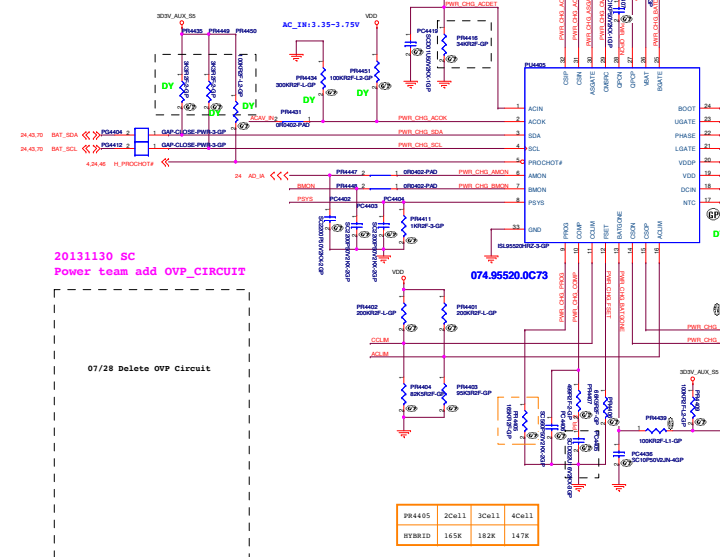
08/06 Delete PQ4411, PQ4408, PR4441, PR4422, PR4420, PR4422, PC4469 Power Team Change solution

08/06 Delete PQ4401, PC4408 Power Team Change solution

07/28 PR4416 39.2Kohm to 34Kohm 64.34025.6DL

V_{CDDET} : Greater than 2.633 V
Less than 3.5 V

06/26 Change PR4435, PR4449, PR4450 to DT

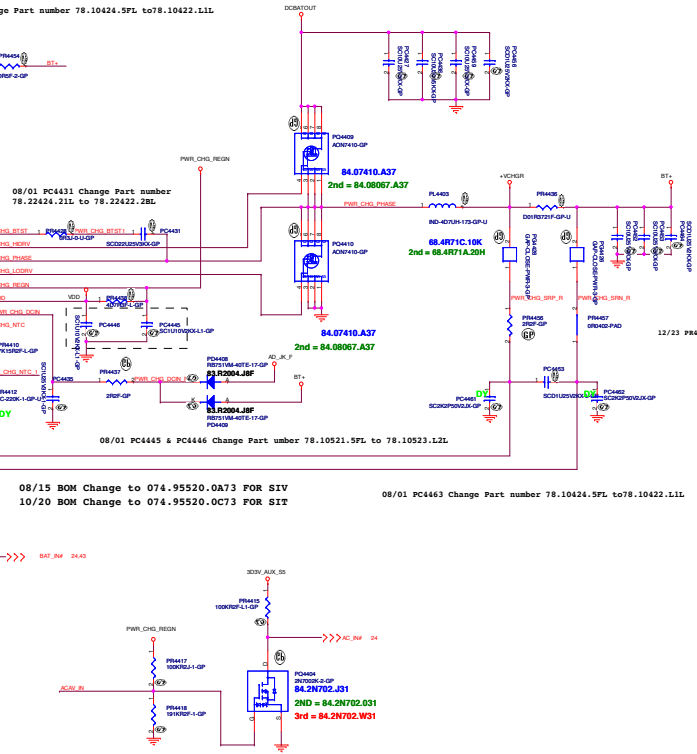


20131130 SC
Power team add OVP_CIRCUIT

07/28 Delete OVP Circuit

PR4405	20k11	20k11	40k11
HYBRID	165K	182K	147K

07/29 PC4405 Change part number 78.22322.2FL to 78.22321.2FL,
值都為0.022uF, 0402, 不同的是25V與16V



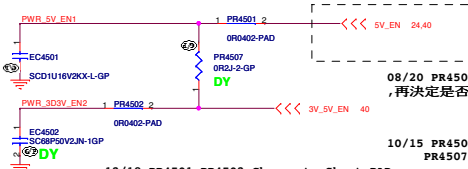
08/01 PC4466 Change Part number 78.10424.5FL to 78.10422.LLL

08/01 PC4431 Change Part number 78.22424.2LL to 78.22422.2BL

08/01 PC4445 & PC4466 Change Part number 78.10521.5FL to 78.10523.L2L

08/15 BOM Change to 074.95520.0A73 FOR SIV
10/20 BOM Change to 074.95520.0C73 FOR SIT

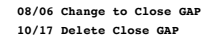
08/01 PC4463 Change Part number 78.10424.5FL to 78.10422.LLL



10/15 PR4501 原本為0R,改為錫短路ZZ.00RES.021
PR4507 原本為錫短路ZZ.00RES.021,改為0R

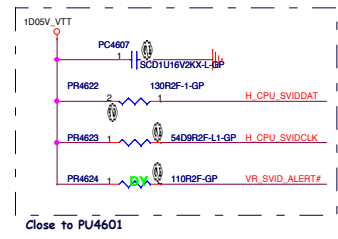
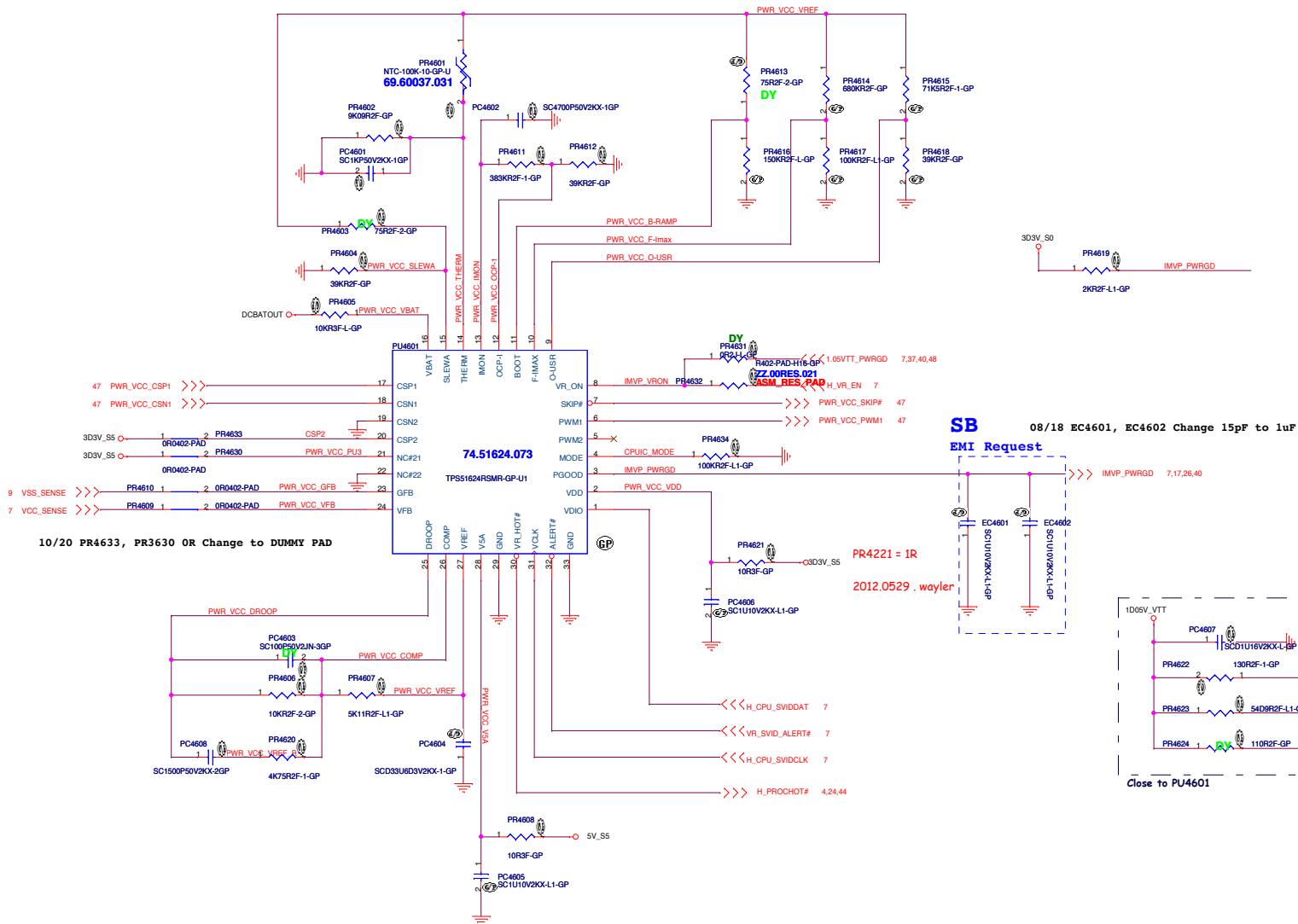
Figure 10 shows the connection for PWR_DCBATOUT_3D3V. It consists of three parallel branches, each containing a PG4504 component. The left terminal of each component is connected to DCBATOUT (labeled '1'), and the right terminal is connected to PWR_DCBATOUT_3D3V (labeled '2'). A ground symbol (GP) is connected to the right terminal of each component. The label 'GAP-CLOSE-PWR-3-GP' is placed next to each component.

12/11 Change Part number ZZ.CLOSE.001(上綠漆)

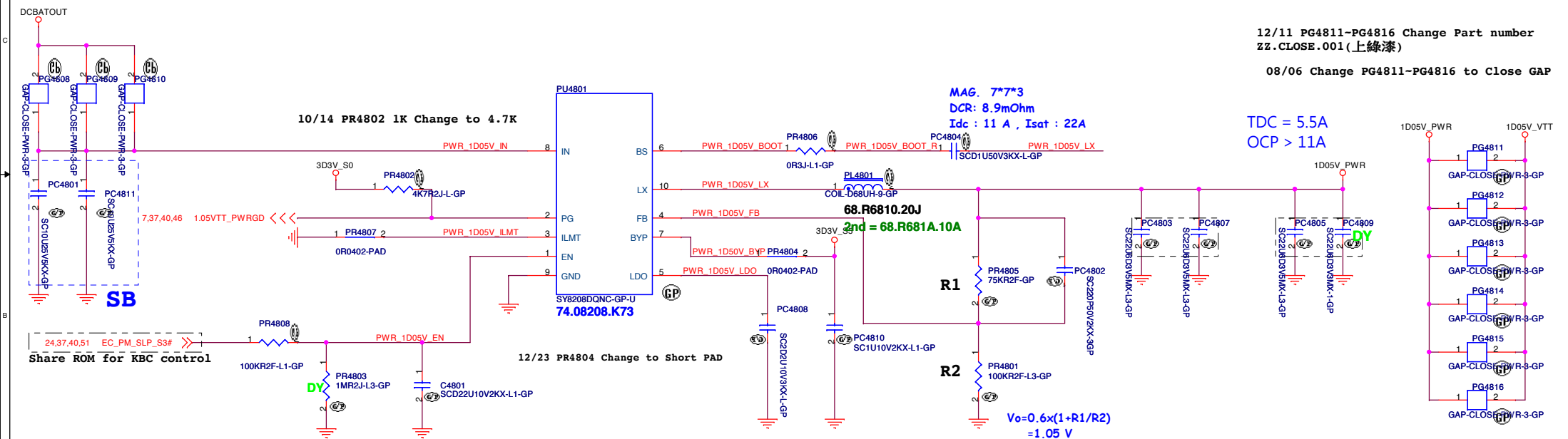


Title			
TPS51275 5V/3D3V			
Size A2	Document Number		Rev
	LT41		-1
Date:	Tuesday, January 20, 2015		Sheet 45 of 102

SSID = CPU.Regulator



SY8208D for 1D05V



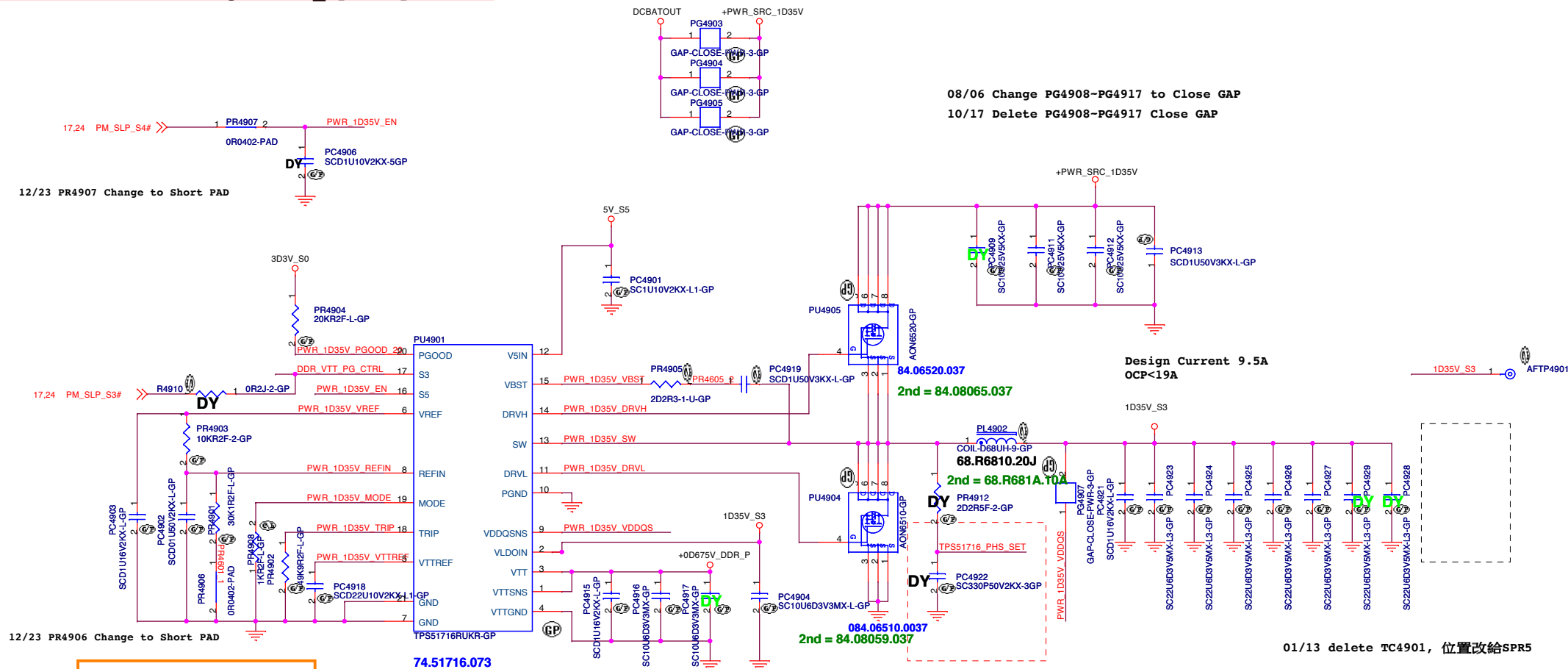
<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
DC to DC 1D05V(SY8208)			
Size A3	Document Number		Rev
	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet 48 of	102

SSID = PWR.Plane.Regulator 1p35v0p675v



20131007

20131014

084.06510.0037
2nd = 84.08059.037

84.06520.037

2nd = 84.08065.037

PL4902
COIL-D68UH-9-GP
68.R6810.20J
2nd = 68.R681A.10A

Design Current 9.5A
OCP<19A

01/13 delete TC4901, 位置改給SPR5

S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

MODE Selection

MODE NO.	RESISTANCE BETWEEN MODE AND GND (kΩ)	CONTROL MODE	SWITCHING FREQUENCY (kHz)	DISCHARGE MODE
3	33	D-CAP2	500	Non-Tracking
2	22		670	
1	12		670	Tracking
0	1		500	

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

TPS51716(VDDQ VTT)Size
A3

Document Number

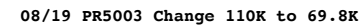
LT41

Date: Tuesday, January 20, 2015

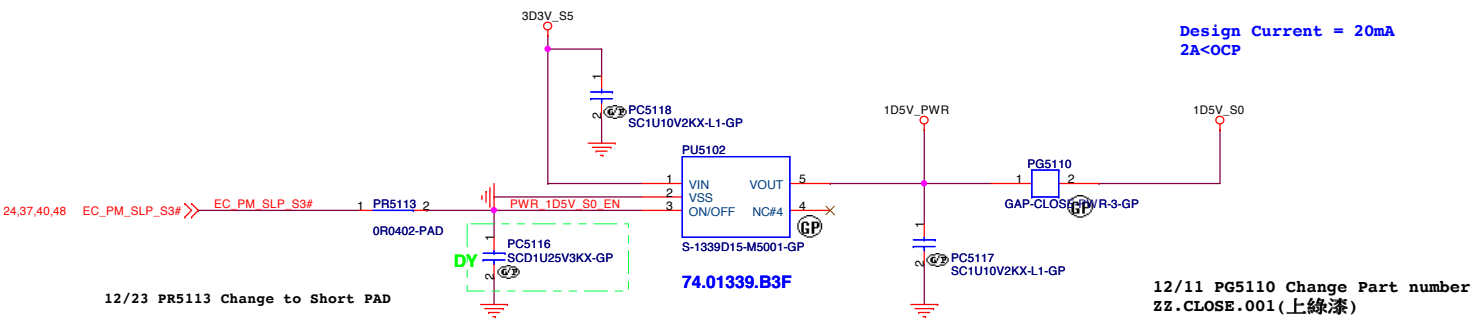
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Rev	1
-----	---

08/12 Pin-8 of Pu5001 connect to net "15V PWR"



RT9198 for 1D5V_S0



12/23 PR5113 Change to Short PAD

12/11 PG5110 Change Part number
ZZ.CLOSE.001 (上綠漆)

10/28 74.09198.B7F (鎖料) 改 74.01339.B3F

5	4	3	2	1
D				D
C				C
B				B
A				A

BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
Title			
Reserved			
Size	Document Number		Rev
A2	LT41		-1
Date	Tuesday, January 20, 2015		
Sheet 62		of 102	



BOM1	
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec-1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>	
Title	
CRT Board Connector	
Size	Document Number
Custom	LT41
Date: Tuesday, January 20, 2015	
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Rev -1	

D

D

C

C

B

B

A

A

BOM1

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

LT41

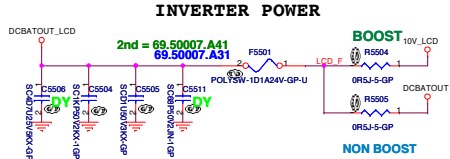
Rev

-1

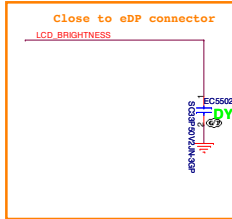
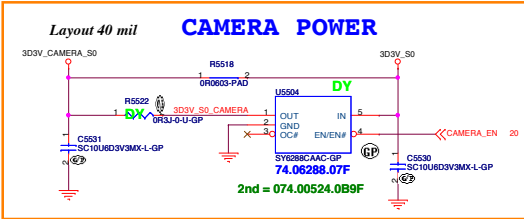
Date: Tuesday, January 20, 2015

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SSID = VIDEO



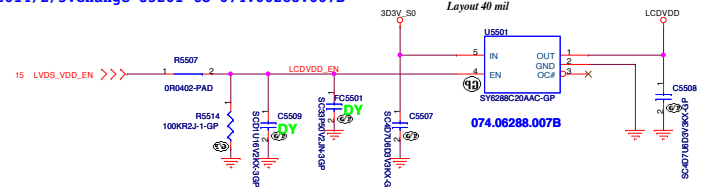
07/04 R5504 BOOST, R5504 NON BOOST



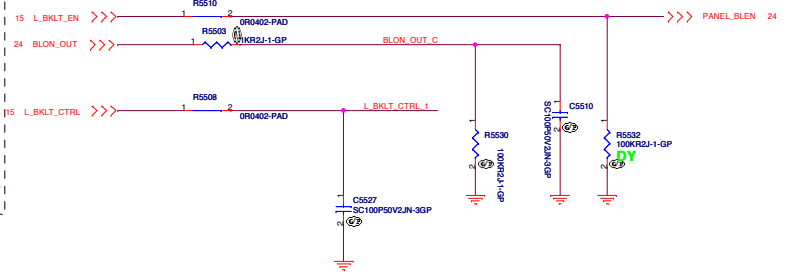
SSID = VIDEO

LCD POWER (Do Not use SW 74.09724.09F)

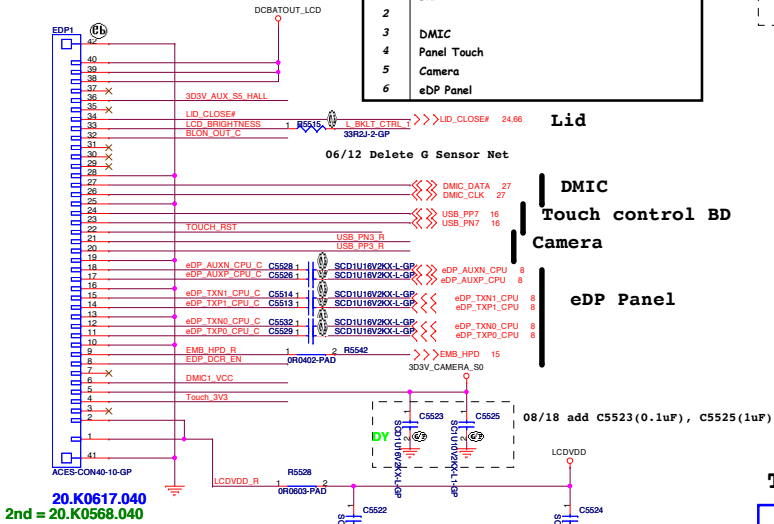
2014/2/5:Change U5201 to 074.06288.007B



Panel BL brightness/Power En/BL En



eDP connector



ESD Request

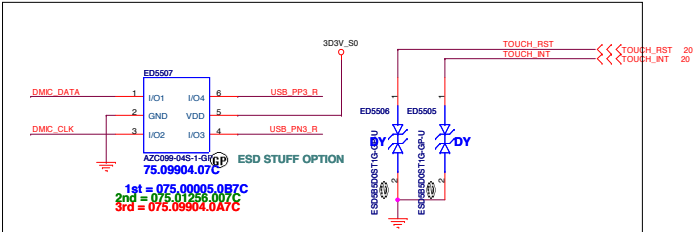
10/16 add ED5507

10/17 change ED5507 從6pin 改為10 pin(EMI要求)

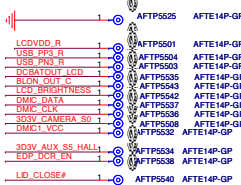
10/20 change ED5507 從10pin 改為6 pin(EMI要求)

12/18 ED5507 Change to DY

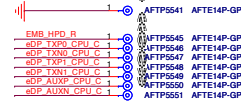
12/24 ED5507 Change to ESD STUFF OPTION,
重點: 1st 075.00005.0B7C 在ED5507不導入。
只導 075.01256.007C 及 075.09904.0A7C



Test point

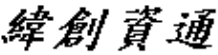


10/20 AFTP5503, AFTP5504 USB_PN3, USB_PP3 change to USB_PN3_R, USB_PP3_R



5	4	3	2	1
D				D
C				C
B				B
A				A

BOM1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number LT41		Rev -1
Date:	Tuesday, January 20, 2015		Sheet 56 of 102

5	4	3	2	1
D				D
C				C
B				B
A				A

BOM1

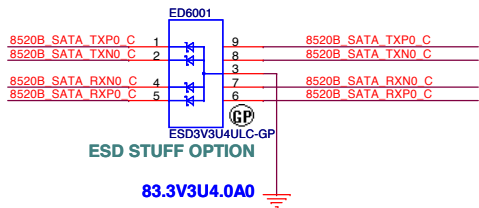
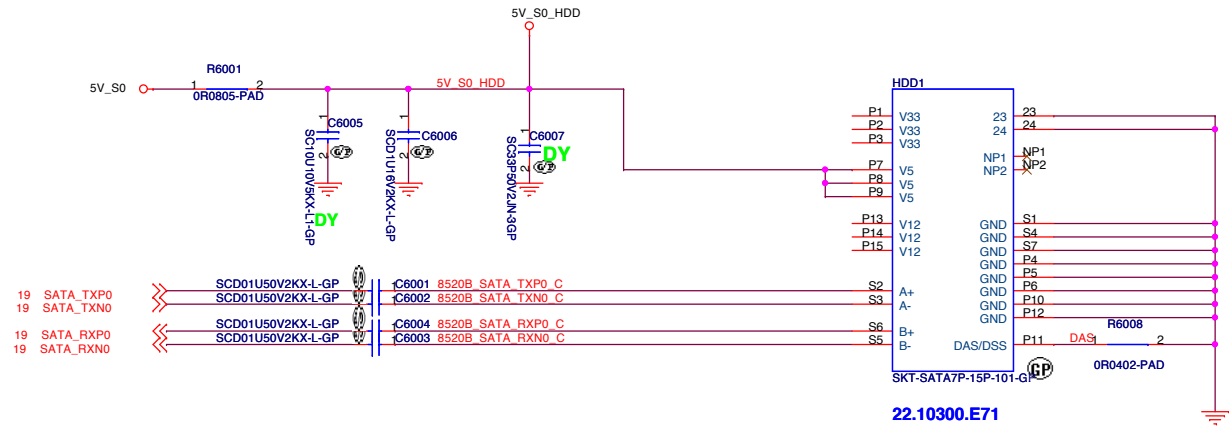
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LT41</div>	Rev <div>-1</div>
Date: Tuesday, January 20, 2015		Sheet 58 of 102

SSID = Wireless

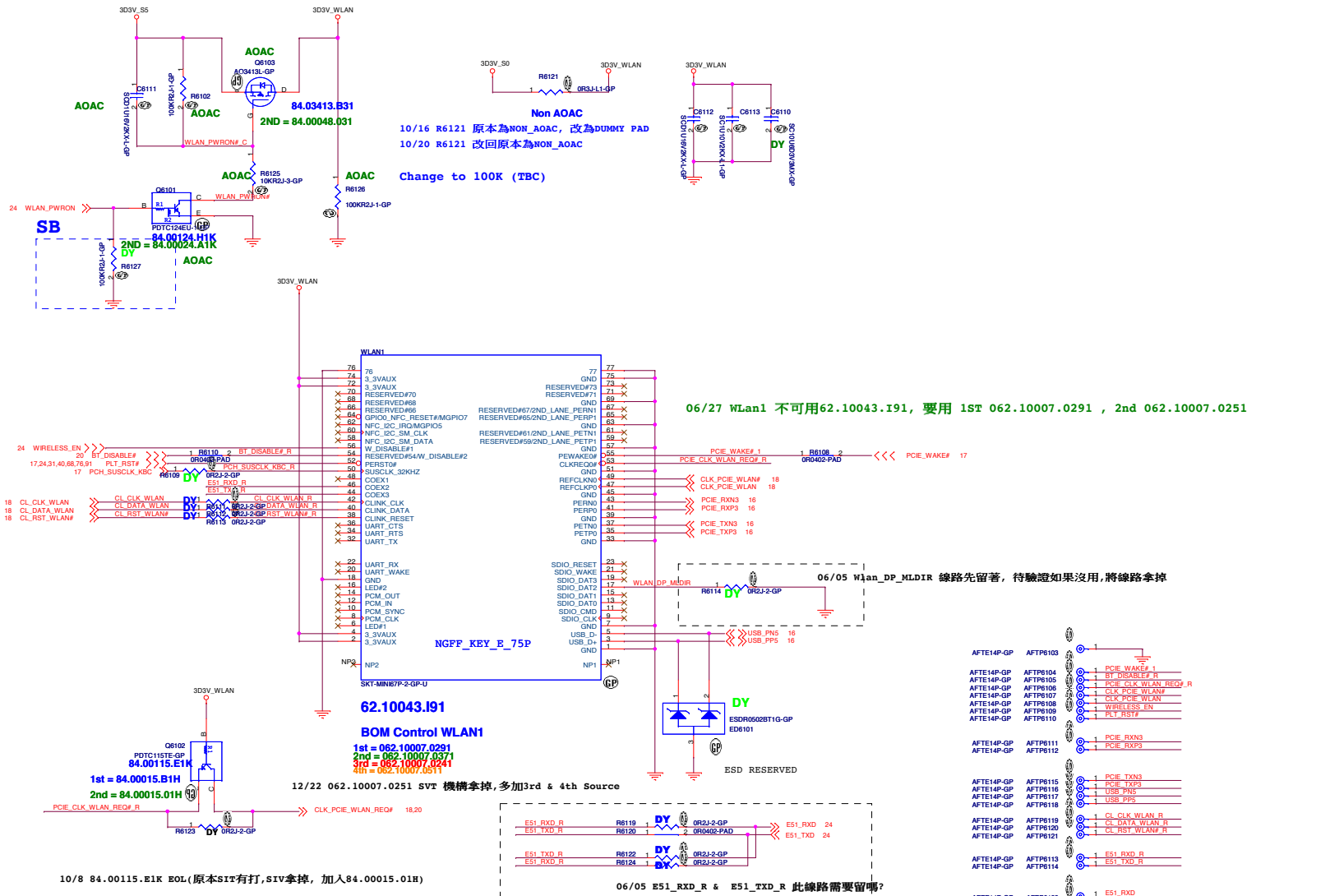
BOM1

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
NGFF SATA		
Size	Document Number	Rev
A3	LT41	-1
Date: Tuesday, January 20, 2015		Sheet 59 of 102

SSID = SATA



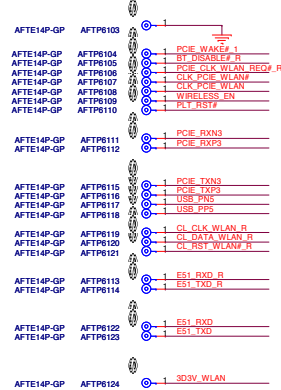
BOM1



06/27 WLAN1 不可用62.10043.I91, 要用 1st 062.10007.0291 , 2nd 062.10007.0251

06/05 Wlan_DP_MLDIR 線路先留著, 待驗證如果沒用,將線路拿掉

06/05 E51_RXD_R & E51_TXD_R 此線路需要留嗎?



07/29 AFTP6124 Change to 3D3V_WLAN

5					4					3					2					1				
D																								
C																								
B																								
A																								

BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
Title			
<div>Reserved</div>			
Size	Document Number		Rev
Custom	LT41		-1
Date:	Tuesday, January 20, 2015		Sheet 62 of 102

(Blanking)

BOM1

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A3

Document Number

LT41

Date: Tuesday, January 20, 2015

Sheet 63 of 102

Rev

-1

The schematic diagram illustrates the electrical connection for the KBC_PWRBTN# signal. On the left, the KBC_PWRBTN# signal line (24) is connected to a network of components. This network includes a switch labeled 'FLEX GAP-OPEN' (G6405), a diode (G6402), and another diode (G6403). The signal then passes through a series of components, including a resistor (R6412) and a capacitor (C6401), before reaching the AFT14P-GP connector. The diagram also shows the connection to the AFT14P-GP connector and the AFT14P-GP connector.

24 KBC_PWRBTN# <<<

R6417 100R2J-2-GP

KBC_PWRBTN#_R3

FLEX

05402 05C1KP50V2KX-1GP

FLEX

62.40012.041

SW-TACT-72-GP-U3

PWRSH1

08/14 PWRSH1 Change to PWRSH1

10/14 PWRSH1 (Pin1,Pin3)KBC_PWRBTN#_R3 SWAP (PIN2,PIN4)GND

2nd = 84.2N702-F3F

FLEX

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward Voltage	V_F	1.7	---	2.3	V	$I_F = 5\text{mA}$

5V_SS

10/14 R6413 510R Change to 910R

TECLA 83.19213.H70

WHITE

2N7020K-2-GP

2N7020J31

1st = 84.2N702.J31

2nd = 84.2N702.W31

24.66

LED1

LED-W-42-GP

U6402

U6403

PB-LED_PWR_1

PB-LED_PWR_2

PWRLED

24.66

08/14 PWRLD1 Change to LED2
12/18 LED2 ~~2x~~083.00270.0B70

5V_SS

R6416

330F0J-3-GP

PWRL_LED360_1

1A

LED2

2K

PWRL_LED360_2

083.00270.0B70

FLEX

2N7002K-2-GP

5V

G

S

84.2N702.J31

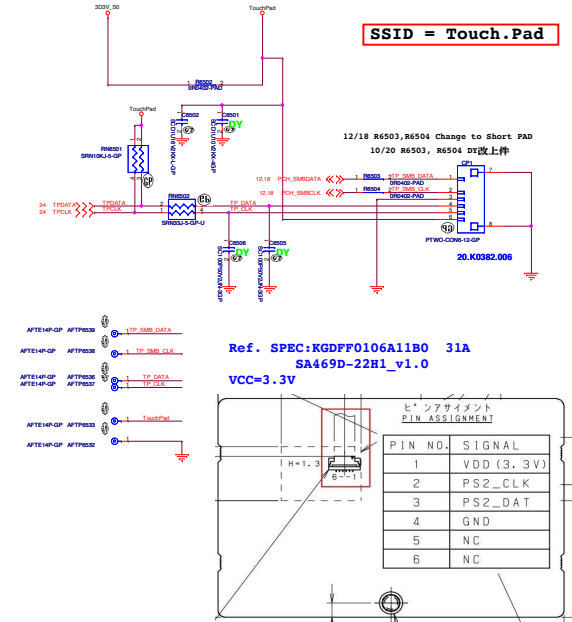
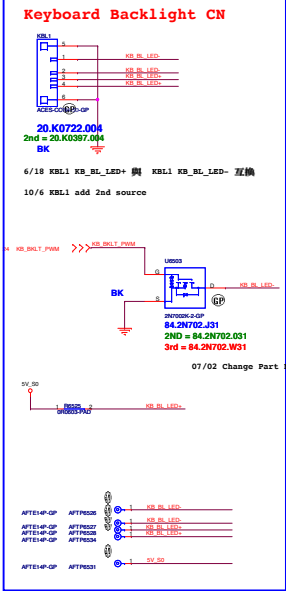
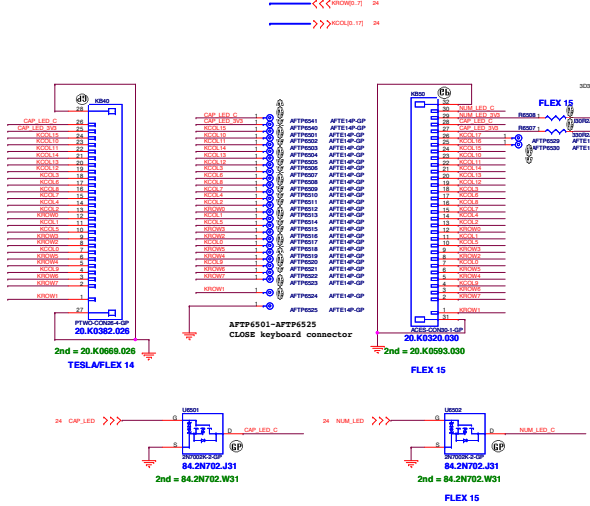
1st = 84.2N702.J31

2nd = 84.2N702.W31

[illegible]

SSID = KBC

Internal KeyBoard Connector



U6203 Keyboard Backlight U6203&BLKB1:

目前spec所看到

14和15的keyboard spec最大為300 mA

84.07002.131

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _{amb} = 25 °C	-	-	60	V
V _{GS}	gate-source voltage	T _{amb} = 25 °C	-	-	±20	V
I _D	drain current	T _{amb} = 25 °C V _{DS} = 10 V	1	-	300	mA
R _{DS(on)}	drain-source on-state resistance	T _J = 25 °C V _{GS} = 10 V I _D = 500 mA	-	1	1.6	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².

15 ON

V_{DS} (V)

I_D (mA)

Power consumption

200 mW

300 mW

400 mW

500 mW

600 mW

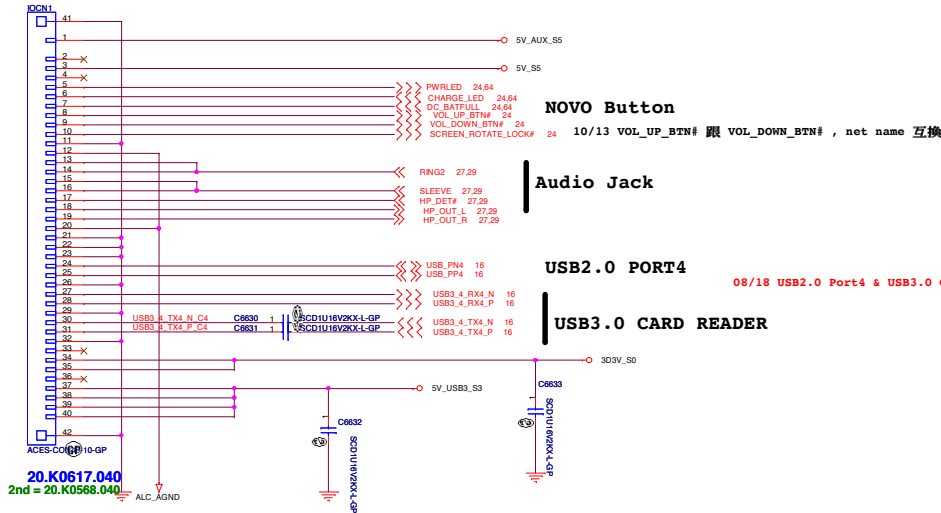
700 mW

800 mW

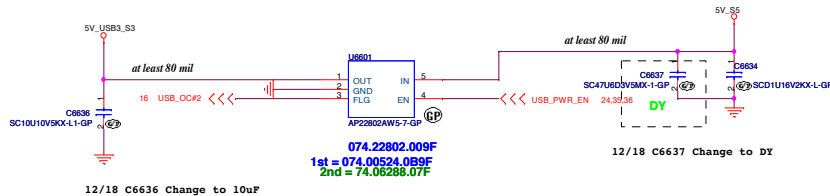
900 mW

1000 mW

IO BD Device	
Item	Device
1	NOVO Button
2	Audio Jack
3	USB Card Reader
4	USB2.0 Port4



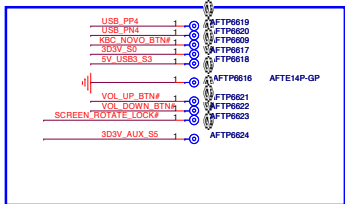
USB 2.0 Power SW



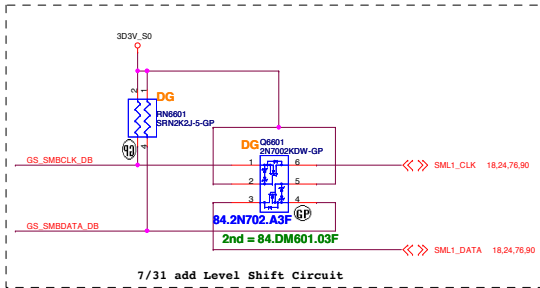
U6301 place near to IOCNI

12/18 074.22802.009F 被禁用
08/05 U6601 add 2nd & 3rd Source

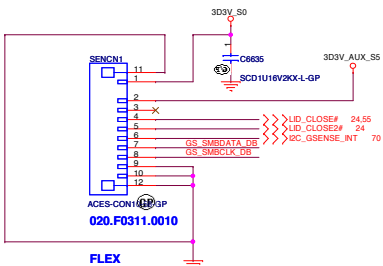
Test point



10/13 VOL_UP_BTN# 跟 VOL_DOWN_BTN#, net name 互换



Flex360 SENSOR BD

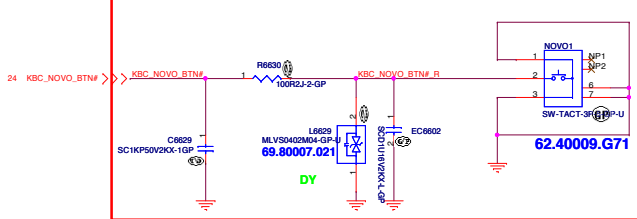


12/25 Sencn1 change Part Number 020.F0311.0010,
(原本20.F1897.010)

Hall sensor

06/12 Delete Hall Sensor CONN, 换7 pin 與SPK 訊號接同一CONN, SPK1

Novo Button



BOM1

緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichu, Taipei Hsien 221, Taiwan, R.O.C.	
Title IO Board Connector	
Size A2	Document Number LT41
Date: Tuesday, January 20, 2015	Sheet 66 of 102

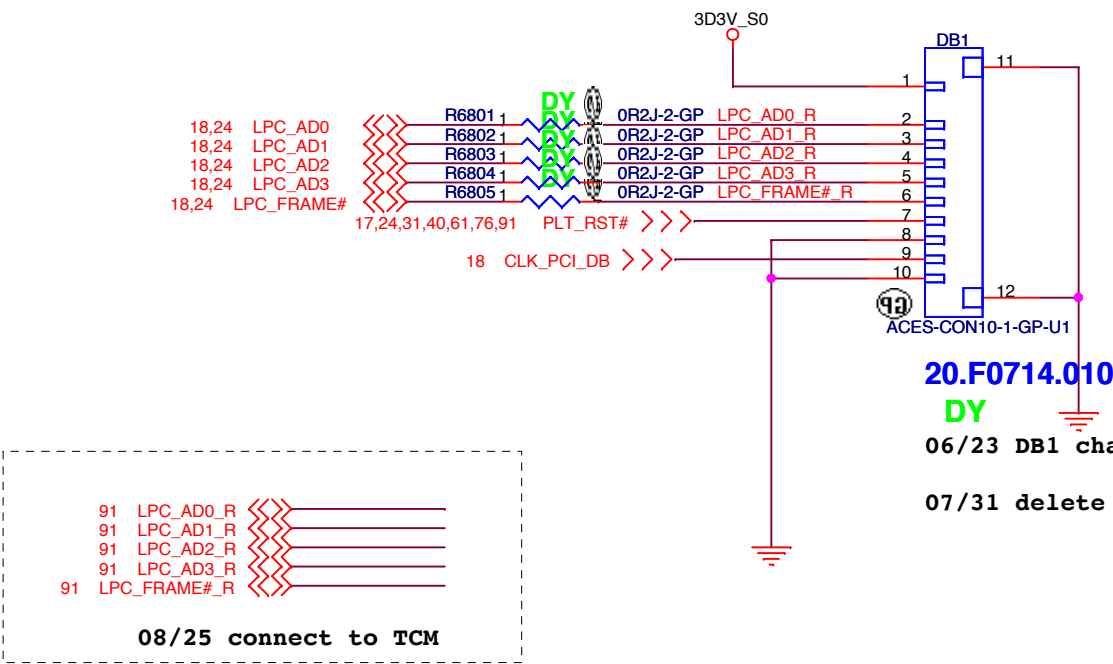
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<

BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
Title			
Reserved			
Size	Document Number		Rev
Custom	LT41		-1
Date:	Tuesday, January 20, 2015		Sheet 67 of 102

Debug Connector



20.F0714.010

DY

06/23 DB1 change to Test point

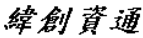
07/31 delete Test point, add Debug CONN

BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Dubug connector</i>			
Size A4	Document Number LT41		Rev -1
Date:	Tuesday, January 20, 2015	Sheet 68 of	102

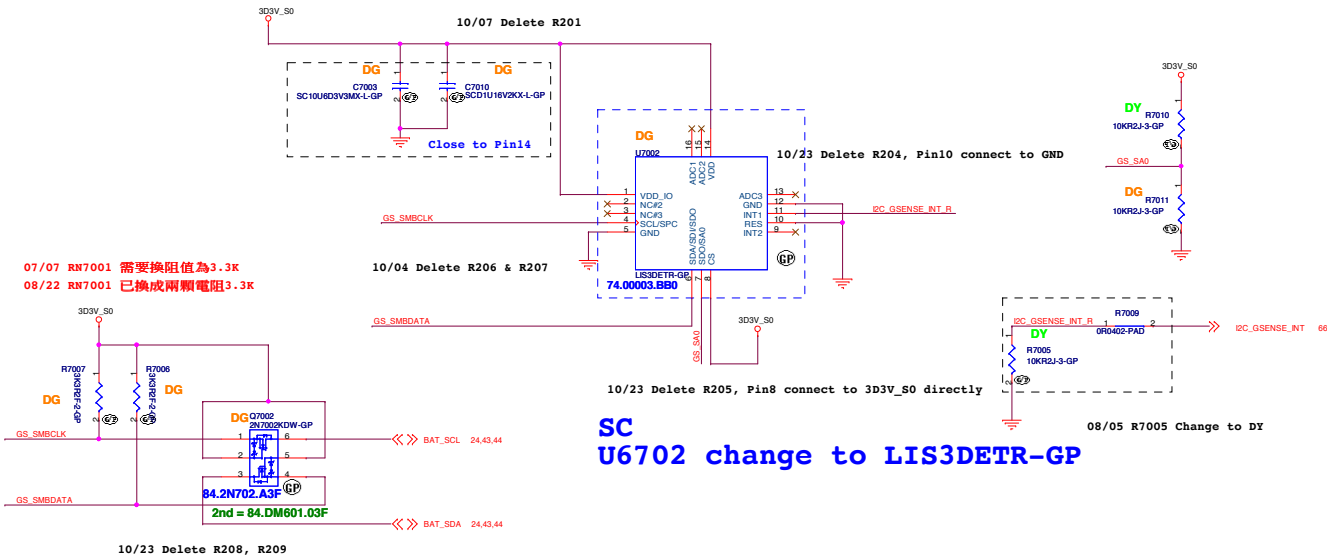
5					4					3					2					1				
D																								
C																								
B																								
A																								

BOM1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Thunderbolt (2/5)			
Size Custom	Document Number LT41		Rev -1
Date: Tuesday, January 20, 2015	Sheet	69	of 102

SC Digital_G-sensor

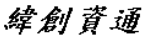
The Slave Address (SAD) associated to the LIS3DH is 001100xb. SDO/SA0 pad can be used to modify less significant bit of the device address. If SA0 pad is connected to voltage supply, LSB is '1' (address 0011001b) else if SA0 pad is connected to ground, LSB value is '0' (address 0011000b). This solution permits to connect and address two different accelerometers to the same I2C lines.



5					4					3					2					1				
D																								
C																								
B																								
A																								

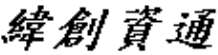
</

BOM1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Thunderbolt (4/5)			
Size Custom	Document Number LT41		Rev -1
Date: Tuesday, January 20, 2015	Sheet	71	of 102

5	4	3	2	1
D				D
C				C
B				B
A				A

BOM1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title Thunderbolt (5/5)		
Size A4	Document Number LT41	Rev -1
Date: Tuesday, January 20, 2015	Sheet 72 of	102

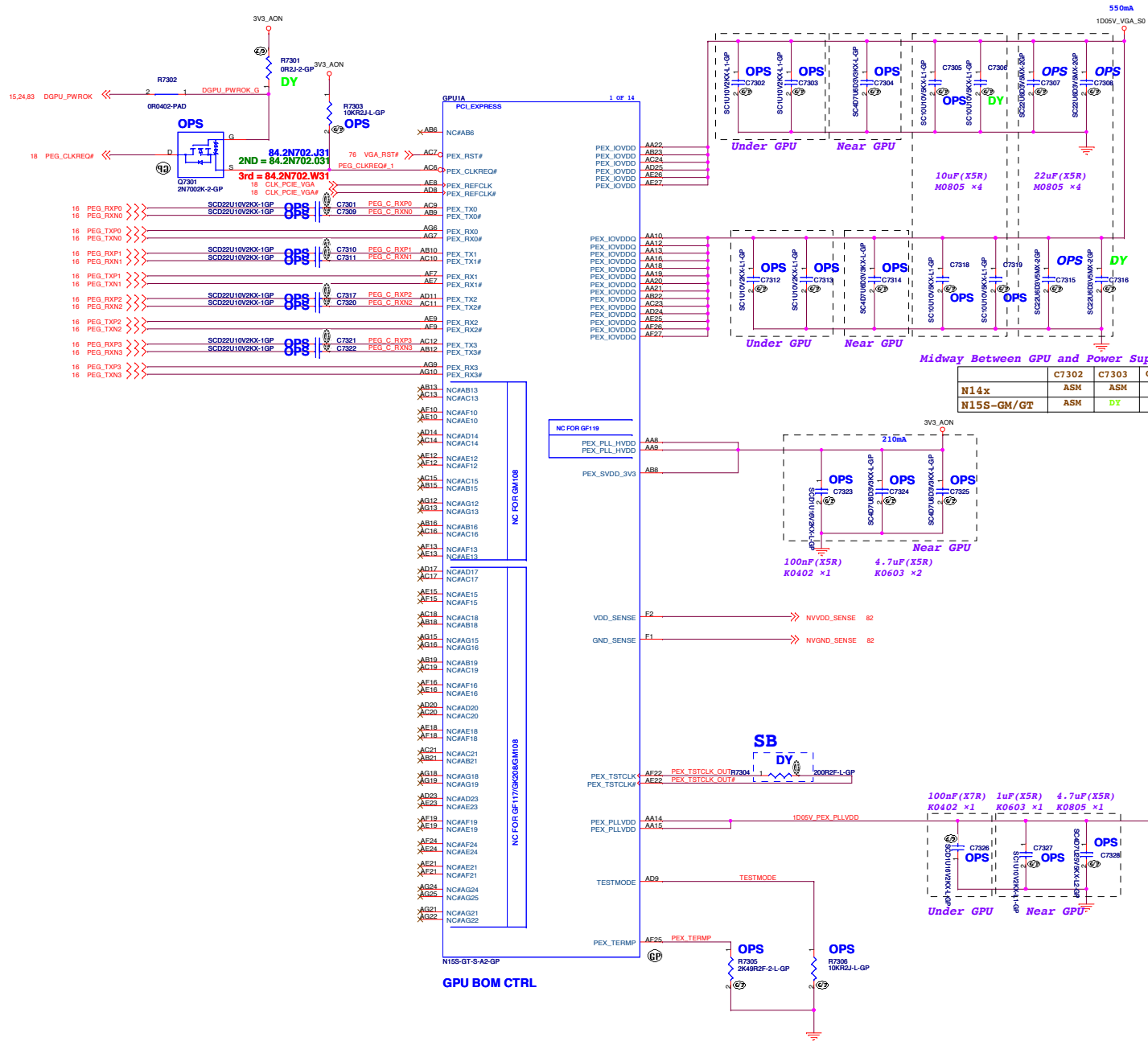
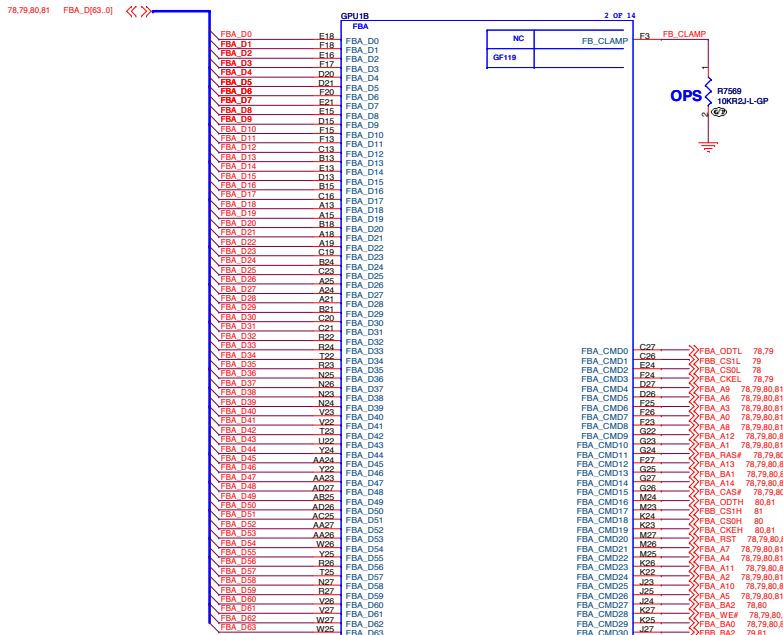


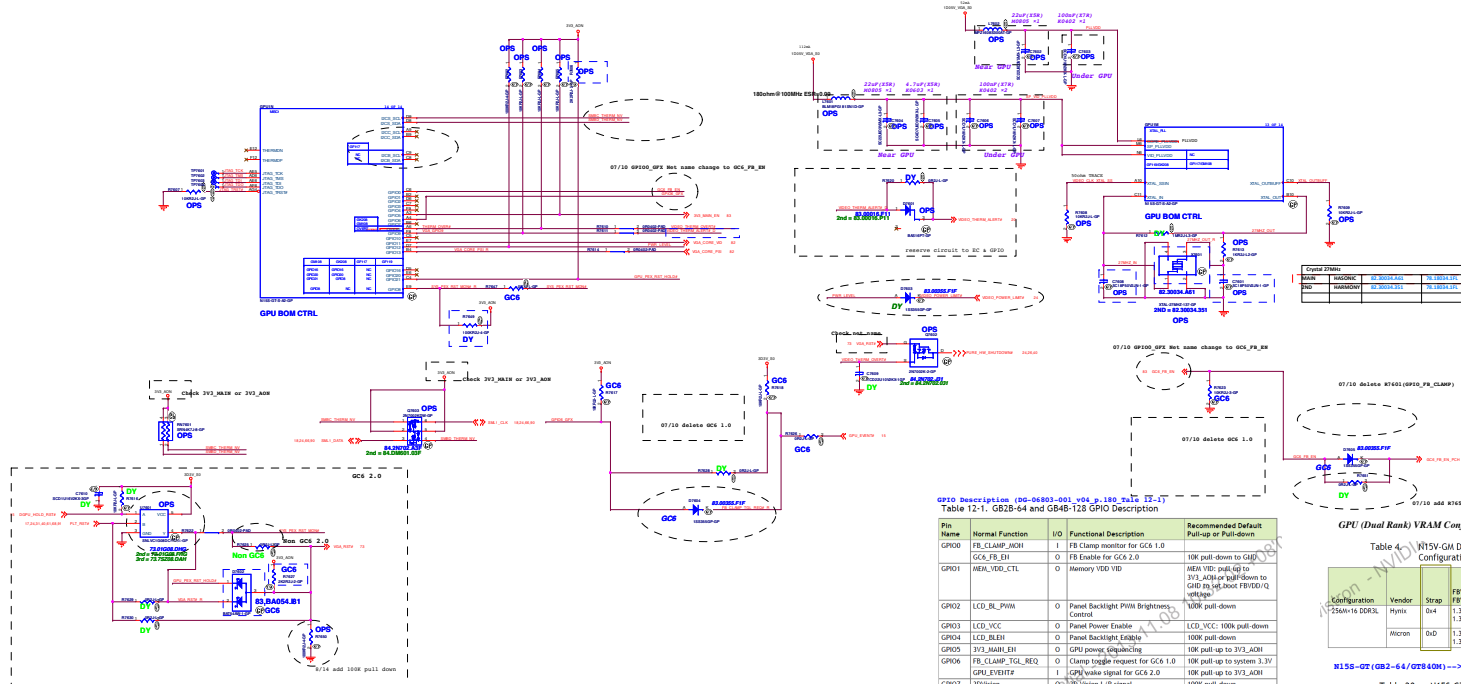
Table 3. PEX_IOVDD/Q Decoupling

Capacitor Type	Typical N14x Population	N15V-GM Population	N155-GV Population	N155-GM/-GT Population	Location
1.0uF	X6S	0402	4	4	Under GPU
4.7uF	X6S	0603	2	2	Under GPU
10uF	X5R	0805	4	4	Near GPU
22uF	X5R	0805	4	4	Near GPU

	C7302	C7303	C7304	C7305	C7306	C7307	C7308	C7312	C7313	C7314	C7318	C7319	C7315	C7316
N14x	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM	ASM
N155-GM/-GT	ASM	DY	ASM	ASM	DY	ASM	DY	DY	DY	DY	DY	DY	DY	DY







GPU Description (RD-0493-001_v04.p.180 to 181 [2-])
Table 12-1. G52B-64 and G54B-128 GPU Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GP00	FB_CLAMP_MON	I	FB Clamp monitor for GCS 1.0	10K pull-down to GND
GP01	GCS_FB_EN	O	FB Enable for GCS 2.0	10K pull-down to GND
GP01	MEM_VDD_CTL	O	Memory VDD VDD	10K pull-down to GND
GP02	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	10K pull-down
GP03	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100K pull-down
GP04	LCD_BLED	O	Panel Backlight Enable	10K pull-down
GP05	3V3_MHL_EN	O	GPU power enable	10K pull-up to 3V3_AON
GP06	FB_CLAMP_TGL_REQ	O	Clamp toggle request for GCS 1.0	10K pull-up to system 3.3V
GP07	GPU_EVENTIF	I	GPU wake signal for GCS 2.0	10K pull-up to 3V3_AON
GP07	SDTRON	O	SD Tron L/E signal	10K pull-down
GP08	SYN_RST_MON	O	System side PCIe reset monitor	10K pull-up to 3V3_AON
GP09	ALERT	I/O	Active Low Thermal alert	10K pull-up to 3V3_AON
GP10	MEM_VREF_CTL	O	Memory VREF Control	10K pull-down
GP11	PWR_VDD	O	GPU Core VDD PWR control signal	10K pull-up to 3V3_AON
GP12	PWR_LEVEL	I	AC power detect or power supply monitor input	10K pull-up to 3V3_AON
GP13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON
GP14	HPD_A	I	Hot Plug Detect for I/Fs used as DisplayPort or for I/Fs when used as Dual Link DVI	See Figure 12-1
GP15	HPD_C	I	Hot Plug Detect for I/Fs	See Figure 12-1
GP16	RESERVED	I	Hot Plug Detect for I/Fs	See Figure 12-1
GP17	HPD_D	I	Hot Plug Detect for I/Fs	See Figure 12-1
GP18	HPD_E	I	Hot Plug Detect for I/Fs	See Figure 12-1
GP19	HPD_F or HPD_B	I	Hot Plug Detect for I/Fs or for I/Fs when used as DisplayPort	See Figure 12-1
GP20	Reserved			

GPU (Dual Rank) VRAM Config:

Table 20. H15V-GM DDR3L Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3L	Hynix	B14	1.35 V / 1.35 V	H5TC4G3AFR-11C	900	N/A	Production ready
	Micron	B10	1.35 V / 1.35 V	MT41K256M16HA-1070E	900	N/A	Production ready

N15S-02 (G52-64/G54B-128) -- SA SR02_3, 4, 5

Table 20. H15S-GT (GM DDR3L Dual-Rank Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/FBVDDQ	Manufacturer Part Number	Max Speed CLK (MHz)	Memory Date Code Minimum	Status
256Mx16 DDR3L	Hynix	B13	1.35 V / 1.35 V	H5TC4G3AFR-11C	900	N/A	Preliminary
	Micron	B14	1.35 V / 1.35 V	MT41K256M16HA-0930E	900	132	Preliminary
	Samsung	B15	1.35 V / 1.35 V	K4H1G164BD-HC1A	900	N/A	Preliminary

Note: For H15S-GT, the maximum allowable memory case temperature is 85 °C.

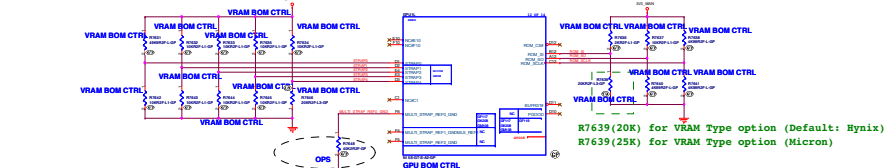
Table 1. N15S-GT -GT GCS pin assignment

GPIO	GCS 1.0 Control Signal	GCS 2.0 Control Signal
GP01	FB_CLAMP_MON	GCS_FB_EN
GP02	FB_CLAMP_TGL_REQ	GPU_EVENTIF
GP04	Reserve	PWR_EN
GP05	Reserve	GPU_RST_MON
GP08	NC	SYN_RST_MON

GCS 1.0/2.0 GPU Support List

GPU	GCS Version
N15V-GM (G52/G54)	No
N15V-GT (G52/G54)	No
N15S-GT (G52/G54)	GCS 1.0 only
N15S-GT (G52/G54)	GCS 2.0 only
N15S-GT (G52/G54)	GCS 2.0 only
N15S-GT (G52/G54)	GCS 2.0 only
N15S-GT (G52/G54)	GCS 2.0 only
N15S-GT (G52/G54)	GCS 2.0 only
N15S-GT (G52/G54)	GCS 2.0 only
N15S-GT (G52/G54)	GCS 2.0 only

< - SA SR02_3, 4, 5



N15S-02
Device ID: 0x1290 (EBC)

VRAM	N15S-02 Hynix 256Mx16 H5TC4G3AFR-11C Device ID: 0x1140 (EBC)	N15S-02 Micron 256Mx16 MT41K256M16HA-0930E Device ID: 0x1140 (EBC)
VRAM_0	0x1140	0x1140
VRAM_1	0x1140	0x1140
VRAM_2	0x1140	0x1140
VRAM_3	0x1140	0x1140
VRAM_4	0x1140	0x1140
VRAM_5	0x1140	0x1140
VRAM_6	0x1140	0x1140
VRAM_7	0x1140	0x1140
VRAM_8	0x1140	0x1140
VRAM_9	0x1140	0x1140
VRAM_10	0x1140	0x1140
VRAM_11	0x1140	0x1140
VRAM_12	0x1140	0x1140
VRAM_13	0x1140	0x1140
VRAM_14	0x1140	0x1140
VRAM_15	0x1140	0x1140

VRAM Bank Voltage: 0.9V

SK01, SK05----->
4GB (VRAM*8)
2GB (VRAM*4) (VRAM1, 2, 5, 6 A8M)

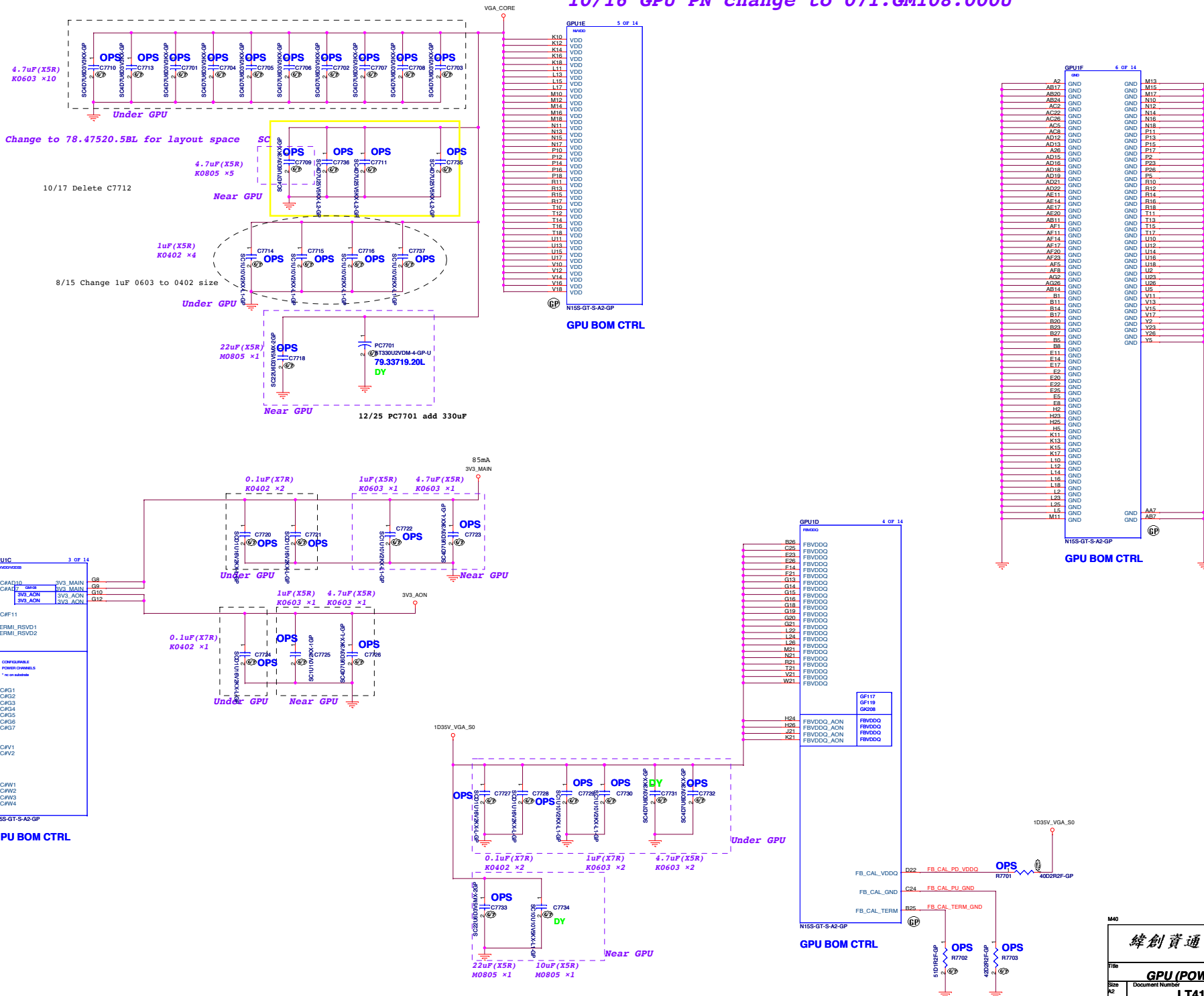
DDR3V Compatible VRAM P/N List

Vendor	Vendor P/N	Lottery P/N	1 chip VRAM Size
Hynix	H5TC4G3AFR-11C	1100957	512MB
Micron	MT41K256M16HA-0930E	1101018	512MB

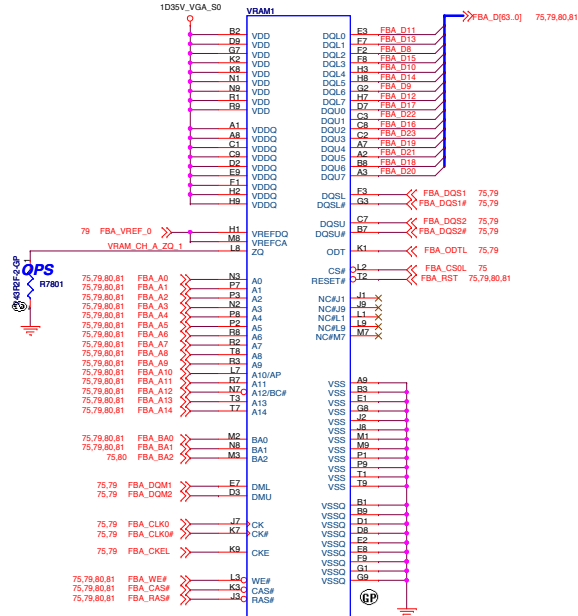
GPU Config:

GPU	SR01	SR02	SR03	SR04	SR05
N15S-02	NA	STUFF	STUFF	STUFF	STUFF
071.0N15S.0C00					

10/16 GPU PN change to 071.GM108.000U

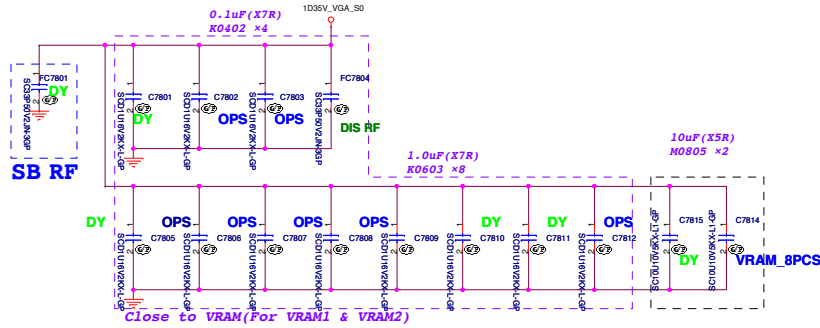


Data Bits 31:0 RANK 0



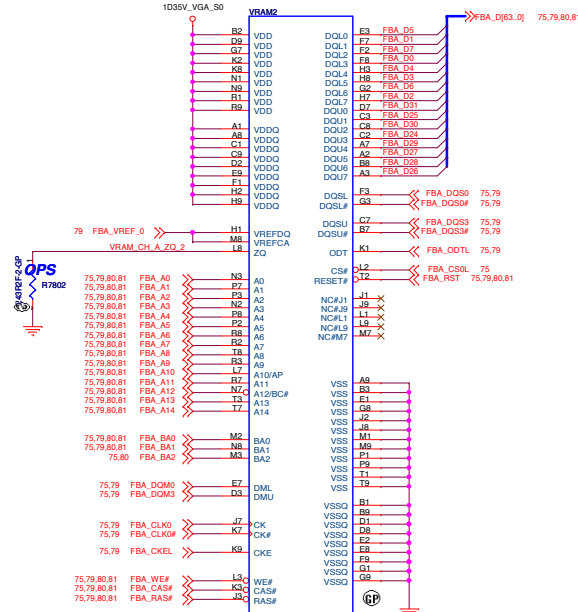
H5TC4G83AFR-11C-GP
72.05463.D0U
VRAM BOM CTRL

10/23 VRAM1-VRAM8 Part Number 72.05463.D0U

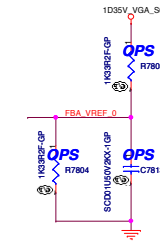


08/18 C7801, C7804, C7805, C7810, C7811 Change to DI

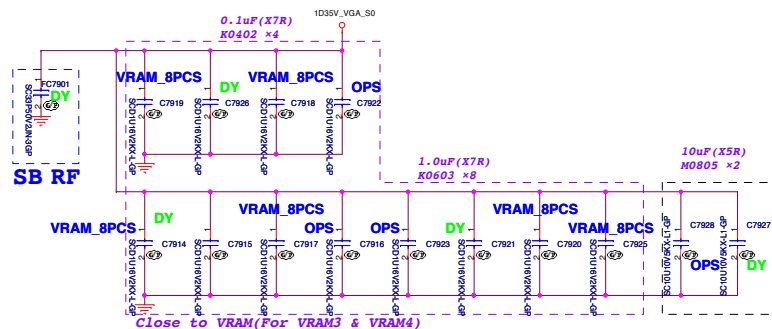
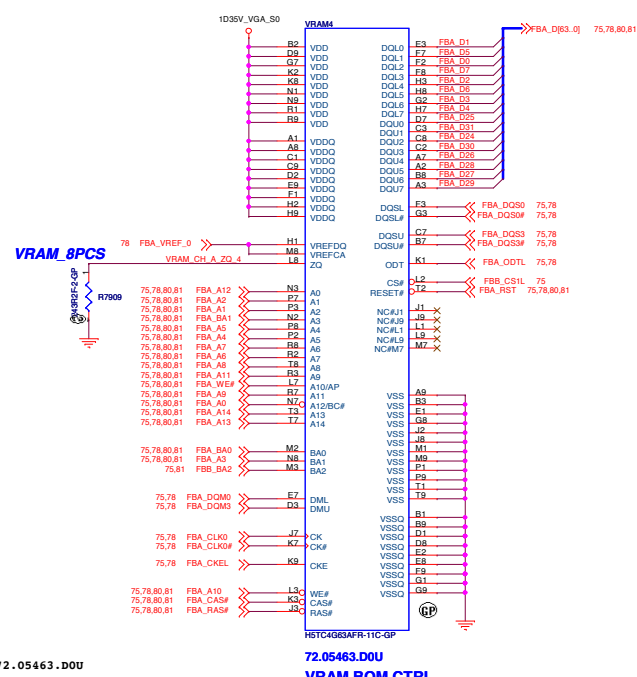
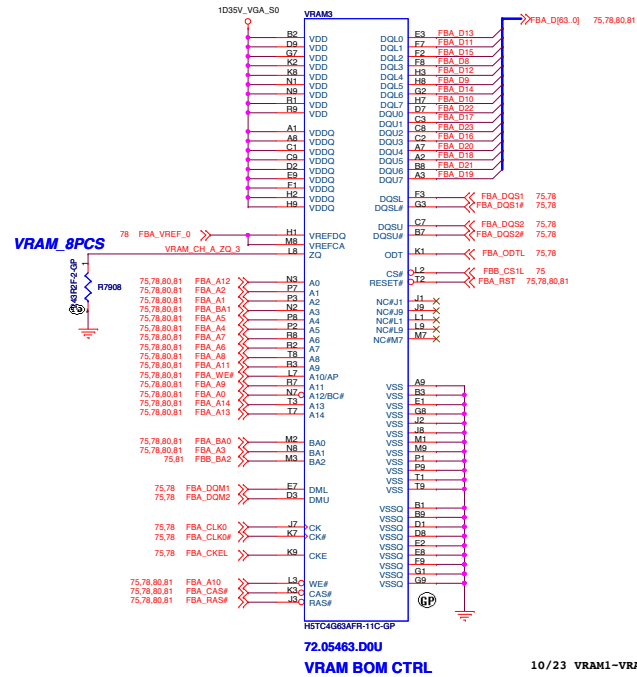
08/18 C7814 Change to VRAM_8PCS



H5TC4G83AFR-11C-GP
72.05463.D0U
VRAM BOM CTRL



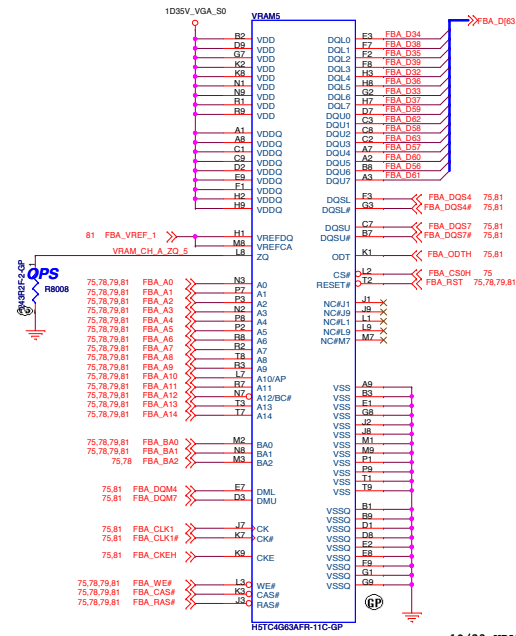
Data Bits 31:0 RANK 1



08/18 C7915, C7921, C7926 Change to DY

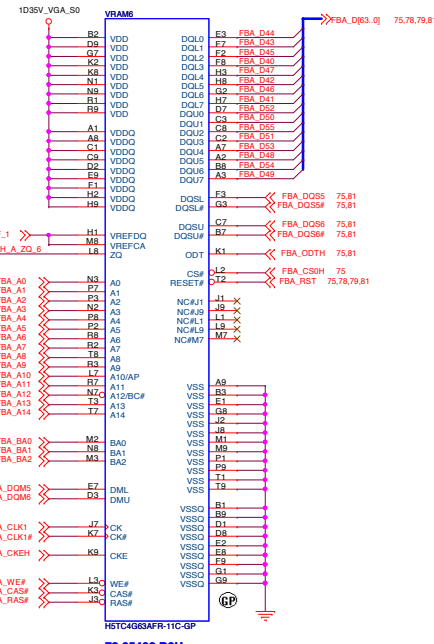
08/18 C7914, C7917, C7918, C7919 ,C7920, C7925 Change to VRAM_8PCS

Data Bits 63:32 RANK 0

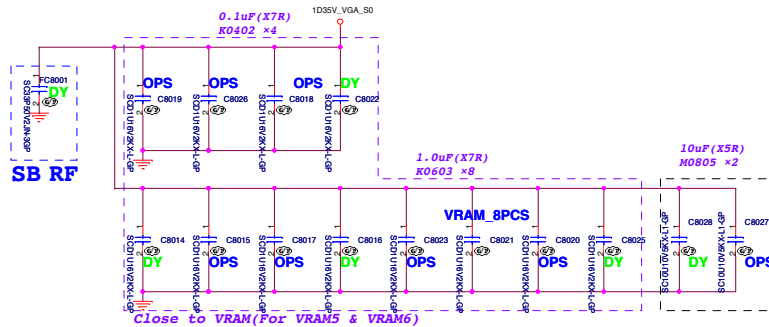


72.05463.D0U
VRAM BOM CTRL

10/23 VRAM1-VRAM8 Part Number 72.05463.D0U

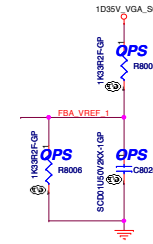


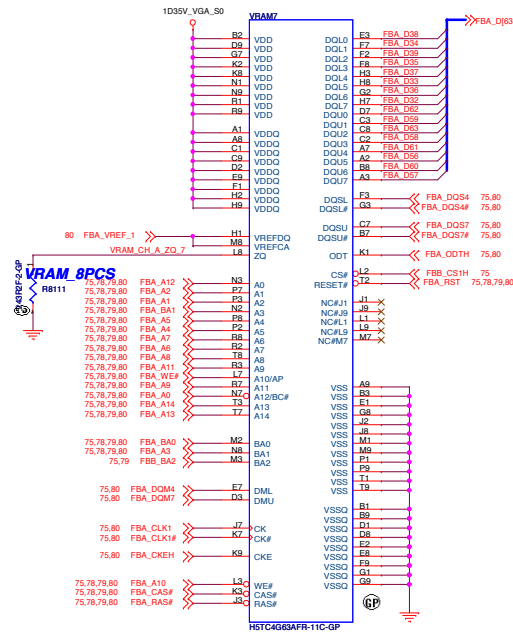
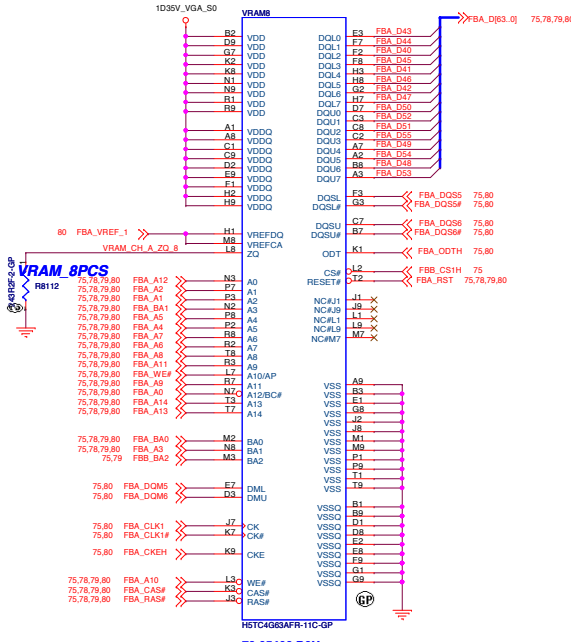
72.05463.D0U
VRAM BOM CTRL



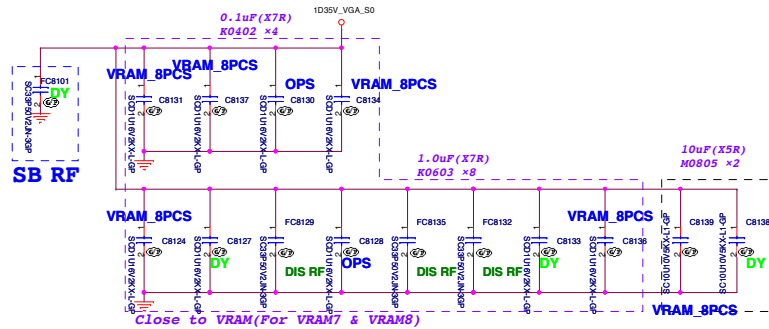
08/18 C8014, C8016, C8022, C8025 Change to DY

08/18 C8021 Change to VRAM_8PCS



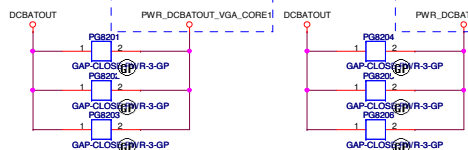
Data Bits 63:32 RANK 172.05463.D0U
VRAM BOM CTRL72.05463.D0U
VRAM BOM CTRL

10/23 VRAM1-VRAM8 改Part Number 72.05463.D0U

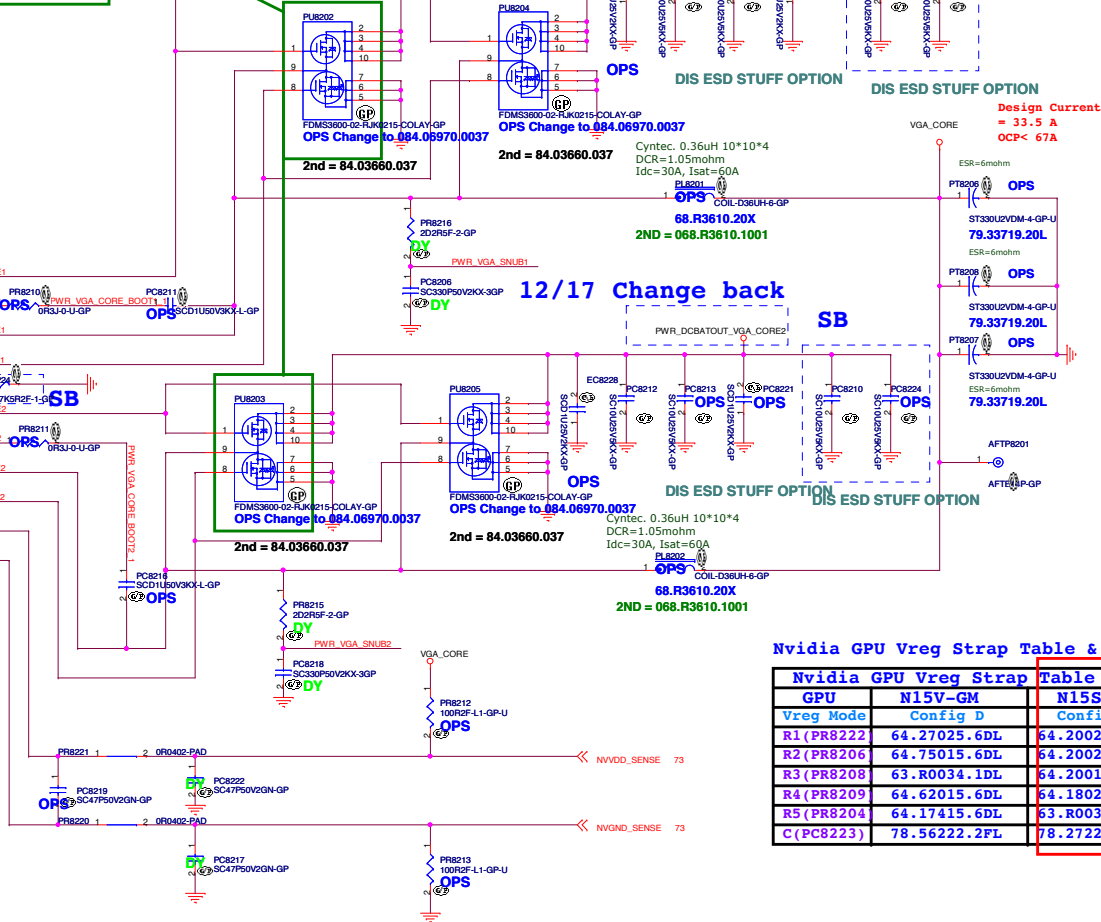


08/18 C8127, C8129, C8132, C8133, C8135 Change to DY

08/18 C8124, C8131, C8134, C8136, C8137, C8139 Change to VRAM_8PCS

06/30 Change PU8202-PU8205 Main Source & 2nd Source**SB**

07/09 3V3_AON Change to 3V3_MAIN

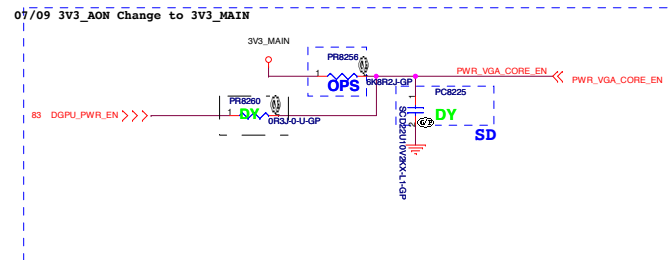


Nvidia GPU Vreg Strap Table & P/N

Nvidia GPU Vreg Strap		Table & P/
GPU	N15V-GM	N15S-GT
Vreg Mode	Config D	Config B
R1(PR8222	64.27025.6DL	64.20025.L0L
R2(PR8206	64.75015.6DL	64.20025.L0L
R3(RP8208	63.R0034.1DL	64.20015.6DL
R4(PR8209	64.62015.6DL	64.18025.6DL
R5(RP8204	64.17415.6DL	63.R0034.1DL
C(PC8223)	78.56222.2FL	78.27224.2FL

GM108 SKU		
Item		N16S-GT-BUS
Device ID		0x1347
Package		GB4B-128K/H2B-64
Internal P/N		GM108-755655,28mm
ROM_SI		Refer to GM108 RAM Straps
ROM_SO		0x0000, 4.99Kohm pull down
ROM_SCLK		0x0 for Optimus, 4.99Kohm pull down
Strap0		Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9KΩ pull-up)
Strap1		
Strap2		Reserved (Keep pull-up and pull-down footprints and leave them so stuffed by default)
Strap3		
Open_VRC SKU		B
NVDDQ Boot Voltage		0.9V

GK208 SKU		
Item		N16V-GM-S
Device ID		0X1299
Package		GB2-64
Internal P/N		GK208-620,28mm
ROM_SI		Refer to GK208s RAM Straps
ROM_SO		0x8, 5k pull up for Optimus09, 10K Pull Up for Discrete SKU
ROM_SCLK		0x1000,0x8, 4.59Kohm pull up
Strap0		User Strap, 0xP, 45Kohm pull up
Strap1		SDP1_PAD_Config, 0x7, 0x00000000
Strap2		Device_ID, 0x1001, 10Kohm pull up
Strap3		0x0 for Optimus, 5kohm pull up low
Strap4		0x0111, 45kohm pull down (NOTE: STRAP3 & STRAP4 are not supported)
Open_VRG_SKU		Config_BSP(S not supported)
NUVDD Boot Voltage		0.9v

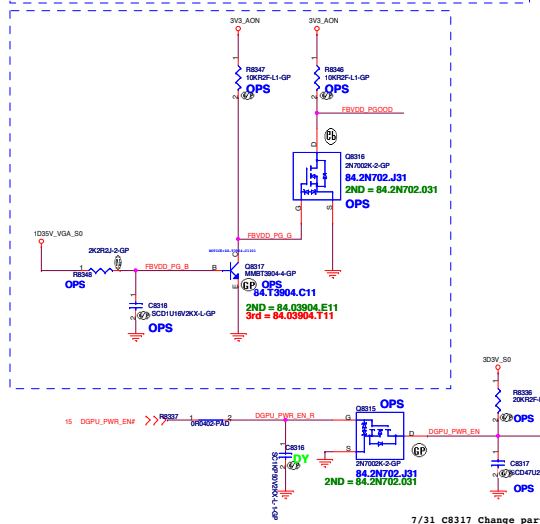
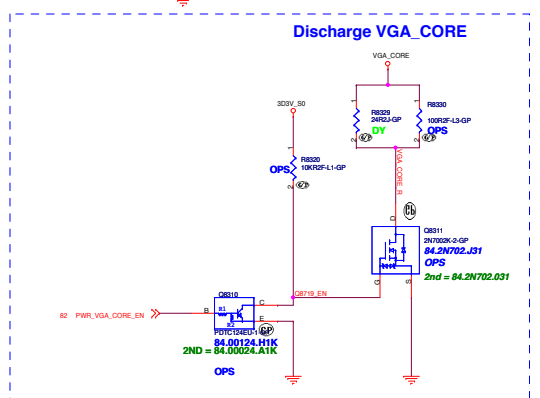
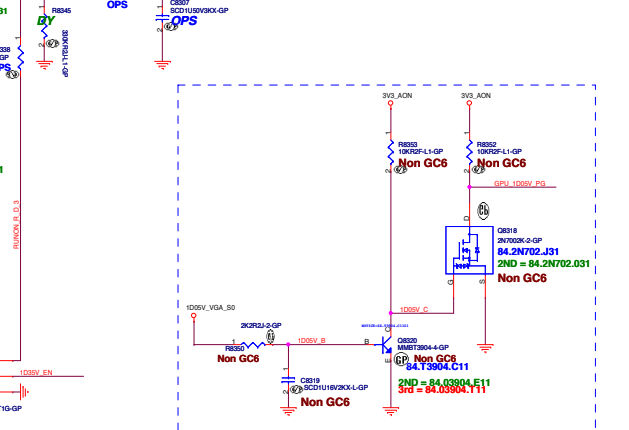
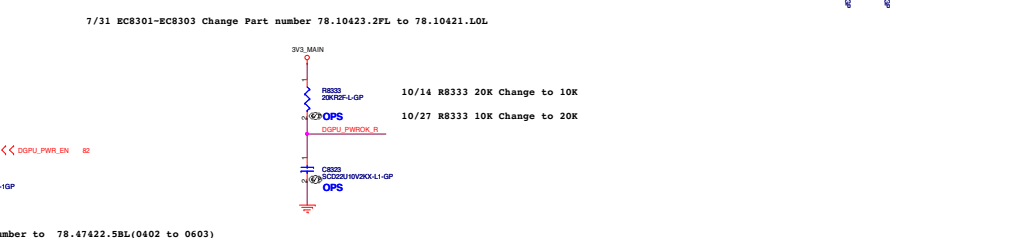
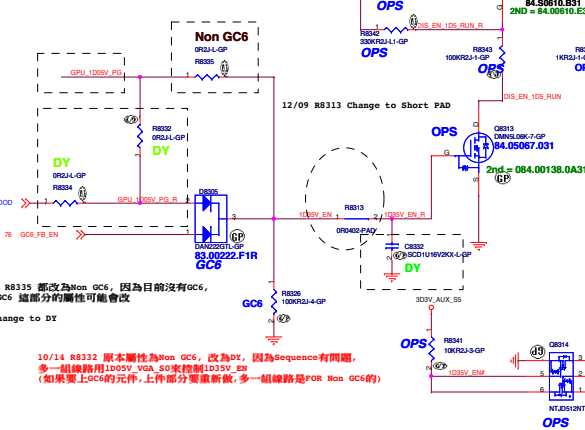
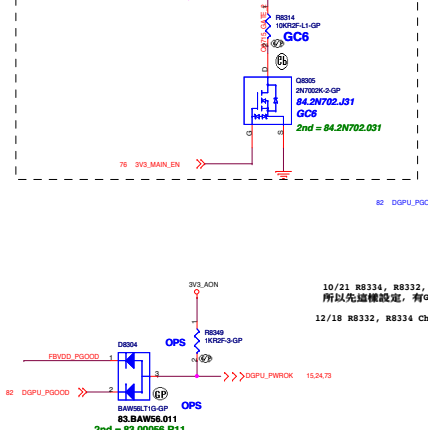


BOM

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8812A VGA CORE
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Size Custom	Document Number LT41	Rev -1
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[illegible][illegible]

2.03F

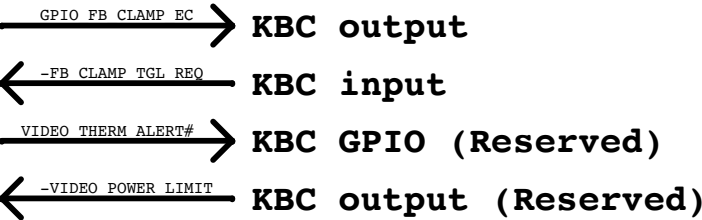
10/14 多一組線路用 ID05V_VGA_S0 來控制 ID35V_En
(如果要用 GC6 的元件, 上件部分要重新做, 多一組線路是 FOR Non GC6 的)
10/21 R8350, C8319, Q8320, Q8318, R8353, R8352 Change to DY
(原本為 Non GC6)
12/18 R8350, C8319, Q8320, Q8318, R8353, R8352 Change to STUFF

ID05V_VGA_S0

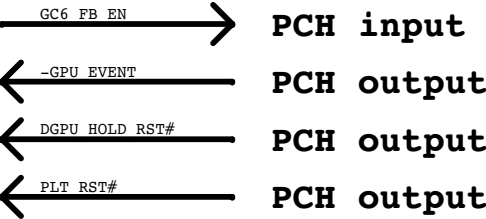
12/11 PG8316-PG8319 Change Part number
ZZ.CLOSE.001(上縁漆)

Undefined Sys <-> GPU IO

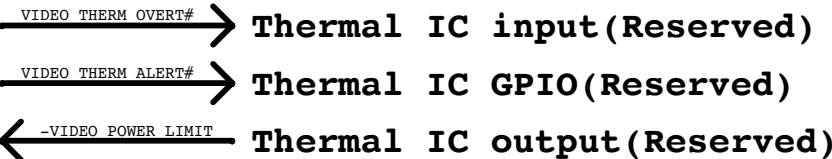
KBC <-> GPU



PCH <-> GPU



Thermal IC <-> GPU



BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Switchable GFX LCD(1/2)			
Size A4	Document Number LT41		Rev -1
Date:	Tuesday, January 20, 2015	Sheet 84 of	102

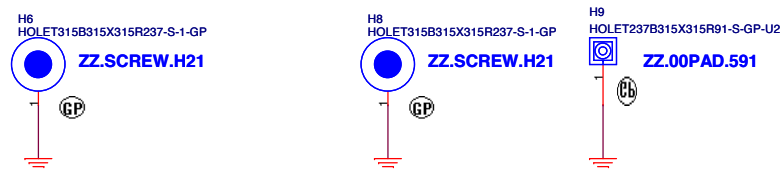
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BOM1

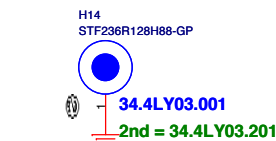
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Title		
Switchable GFX LCD(2/2)		
Size	Document Number	Rev
A4	LT41	-1
Date: Tuesday, January 20, 2015		Sheet 85 of 102

08/14 H6, H8 ZZ.00PAD.591 Change to ZZ.SCREW.H21

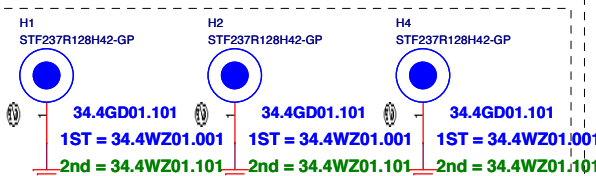
Structure boss



Stand off

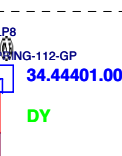
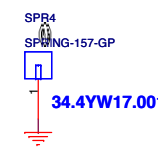
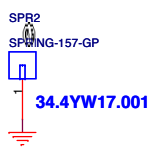
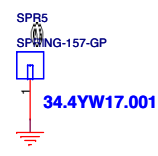
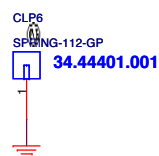
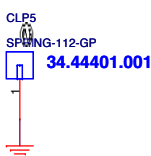
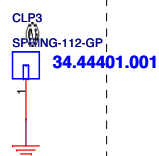
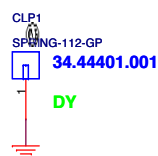
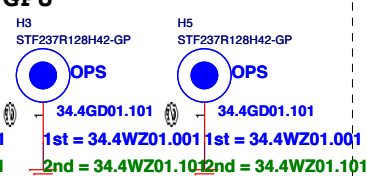


CPU



07/29 H3 Change to OPS

GPU



06/06 Delete Clp3 記得SB版要將CLP 上件
10/22 CLP1, CLP4, CLP7, CLP8 上件(原本為ZZ)
10/22 SPR1 上件(原本為ZZ)
12/18 CLP1 Change to DY
12/18 Delete CLP4, 因為那位置要放SPR4

01/13 add SPR5

08/22 add SPR2

06/18 add SPR1

12/11 SPR2 改上件

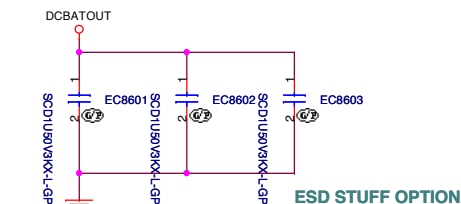
10/20 add CLP7, CLP8

12/23 Delete SPR1

10/17 add EC8604~EC8611 for EMI

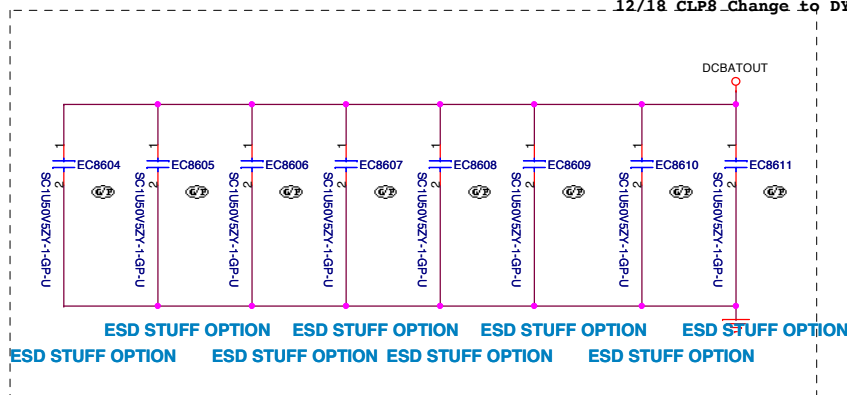
10/23 Delete CLP7

12/18 CLP8 Change to DY



ESD STUFF OPTION ESD STUFF OPTION

06/25 add EC8601, EC8602, EC8603

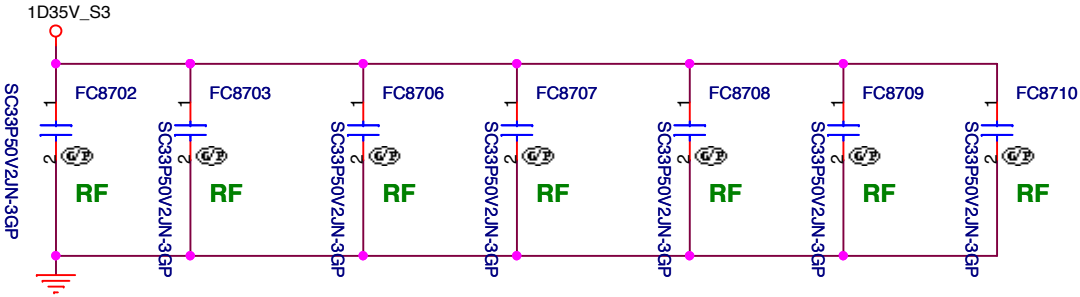
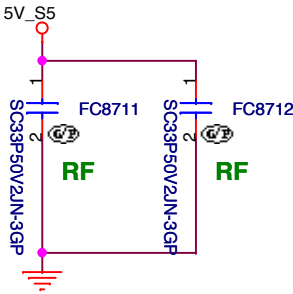
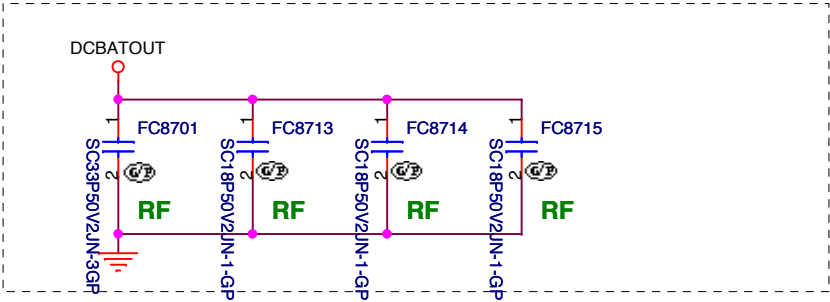


BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	UNUSED PARTS/EMI Capacitors		
Size A3	Document Number	LT41	Rev -1
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10/19 add for RF

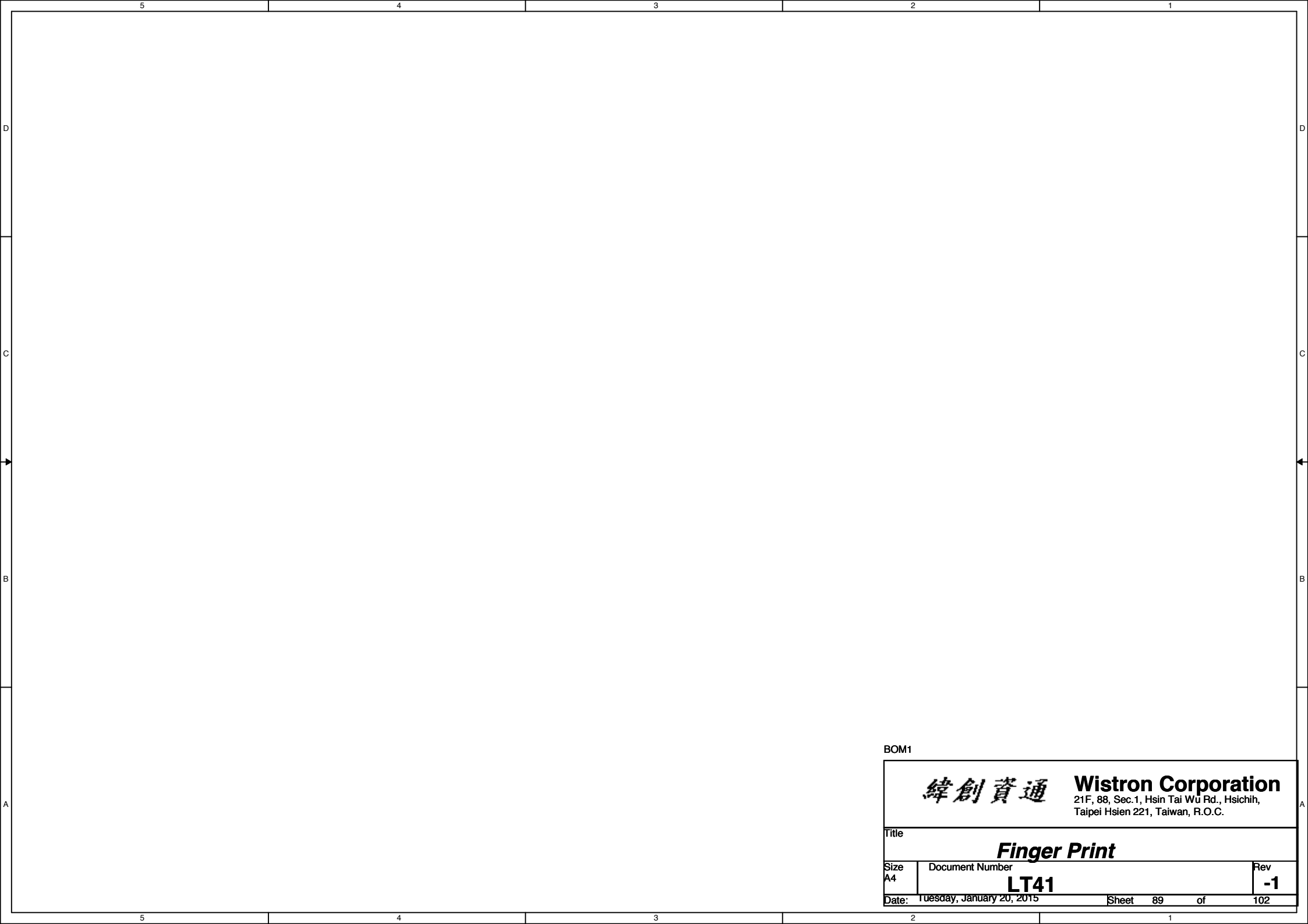


10/23 Delete FC8704,FC8705

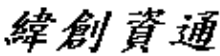
BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			
<div>Reserved</div>			
Size A4	Document Number <div>LT41</div>		Rev <div>-1</div>
Date:	Tuesday, January 20, 2015	Sheet 87 of	102

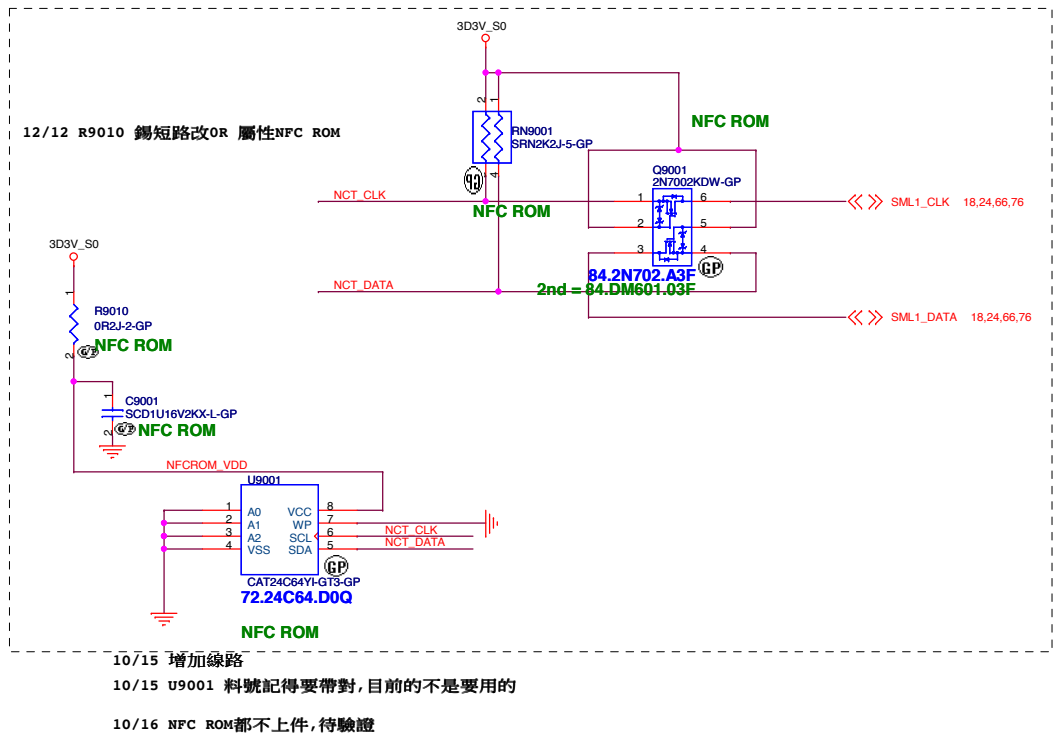
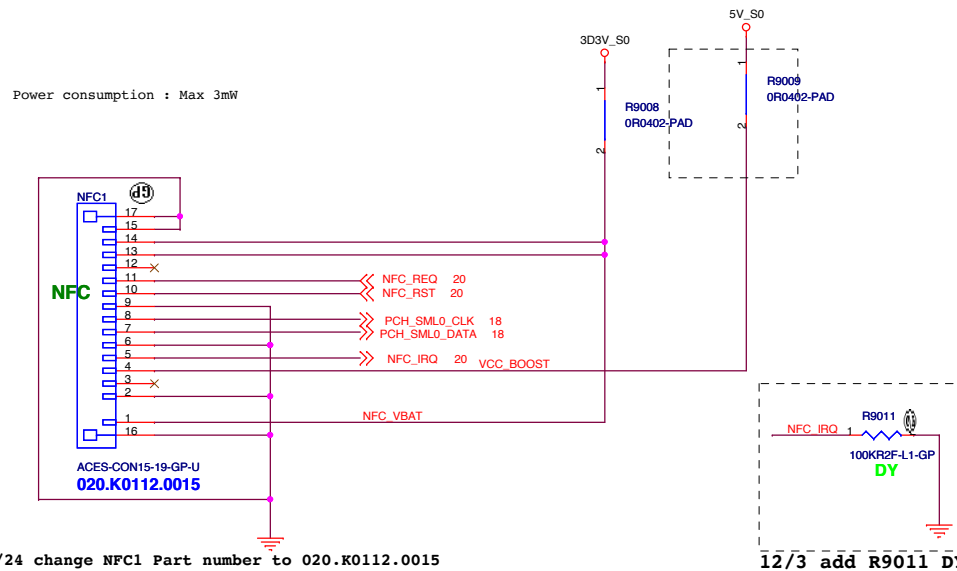
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D																								
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															BOM1									
															<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>									
															<div>Title</div> <div>Reserved</div>									
Size A					Document Number										Rev									
					LT41										-1									
Date: Tuesday, January 20, 2015					Sheet					88					of					102				



BOM1

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <i>Finger Print</i>			
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07/03 add R9009 5V_S0 Connect to NFC CONN Pin12 (SA板 未接)



NFC Module Pin Define



Suggestion Host Pin define Use Sinbon FFC A9152420)

Pin#	Pin Name	Type	Refer	Description
1	VBAT	power	3.3V	Power supply voltage
2	GND	Power	GND	Ground
3	SWP	IO	-	SIM Card data
4	VCC_BOOST	Power	5V	Booster supply
5	IRQ	O	PVDD	Interrupt
6	PMUVCC	Power	connect to outside SE power or GND (no SE)	UICC power input from external PMU
7	I2C_SDA	I/O	PVDD	I2C Serial Data Line
8	I2C_SCL	I/O	PVDD	I2C Serial Clock Line
9	GND	Power	GND	Ground
10	VEN	I	GPIO Control (Normal 3.3V)	Enable/ disable LDO regulator / Reset
11	DWL_REQ	I	GPIO Control (Normal 0V)	Firmware download control pin
12	SIMVCC	Power	1.8V or N.C	Power output to supply the UICC
13	VBAT	Power	3.3V	Power supply voltage
14	PVDD	Power	3.3V	Pad supply voltage
15	GND	Power	GND	Ground

Pin#	Pin Name
15	VBAT
14	GND
13	SWP
12	VCC_BOOST
11	IRQ
10	PMUVCC
9	I2C_SDA
8	I2C_SCL
7	GND
6	VEN
5	DWL_REQ
4	SIMVCC
3	VBAT
2	PVDD
1	GND

BOM1

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
NFC			
Size	Document Number	Rev	
Custom	LT41	-1	
Date:	tuesday, January 20, 2015	Sheet	90 of 102

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B				B
A				A

BOM1

<div>緯創資通</div>		<div>Wistron Corporation</div>			
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title					
<div>Switchable GFX eDP</div>					
Size	Document Number		Rev		
A	LT41		-1		
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D

C

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BOM1

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Wistron Corporation

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Title

Bottom Docking

Size
A

Document Number

LT41

Rev	
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Date: Tuesday, January 20, 2015

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	A	B	C	D	E
4					
3					
2					
1					

BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Inter LAN WG1217LM			
Size	Document Number		Rev
A3	LT41		-1
Date:	Tuesday, January 20, 2015	Sheet 94 of	102

D

C

B

A

BOM1

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN Switch

Size
A

Document Number

LT41

Rev

-1

Date: Tuesday, January 20, 2015

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B				B
A				A

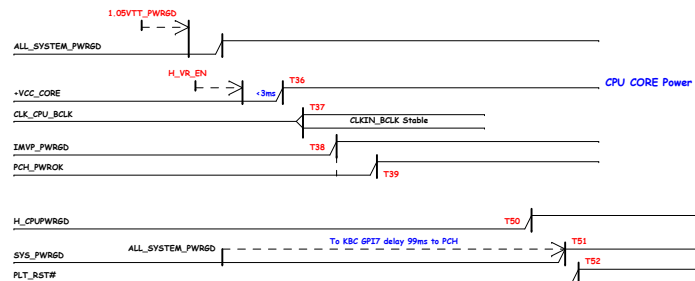
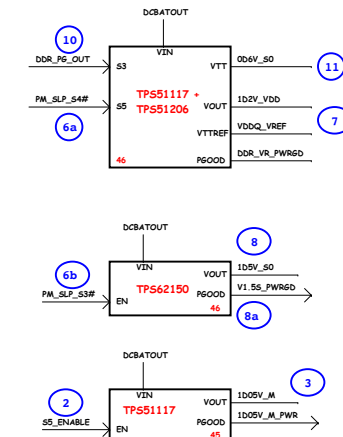
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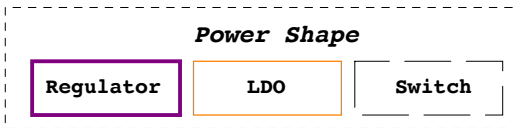
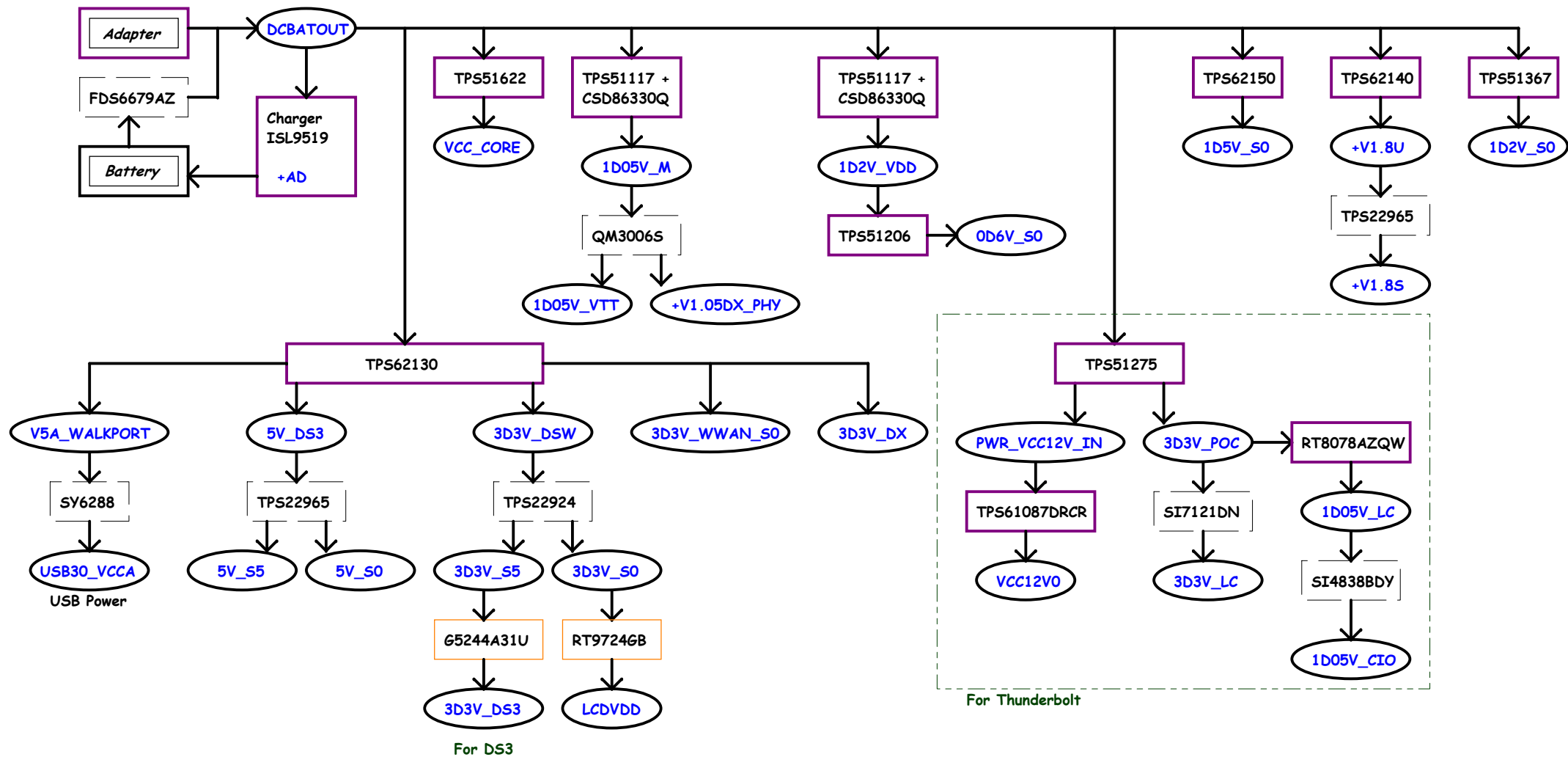
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Title <div>PCH XDP</div>		
Size <div>A4</div>	Document Number <div>LT41</div>	Rev <div>-1</div>
Date: Tuesday, January 20, 2015		Sheet 96 of 102

GPU BOM CTRL			For Detail see P82		
GPU	N16V-GM	N16S-GT			
Lenovo P/N	071.0N16V.000U	071.0N16S.000U			
OPS (UMA:DX)	V	V			
PR8222	64.20025.L0L	64.20025.L0L			
PR8206	64.20025.L0L	64.20025.L0L			
PR8208	64.20015.6DL	64.20015.6DL			
PR8209	64.18025.6DL	64.18025.6DL			
PR8204	63.R0034.1DL	63.R0034.1DL			
PC8223	78.27224.2FL	78.27224.2FL			

VRAM BOM CTRL (Default Setting:900MHZ)									
Lenovo P/N		1101018	1100788	1100897	1101028	1101019	1100661	1100677	
IC Vendor		Micron	Hynix	Hynix	Samsung	Samsung	Micron	Micron	
IC Vendor P/N		MT41J256M16HA-093G:E N15S-GT only	H5TC2G63PFR-11C N15V-GM/N15S-GT	H5TC4G63APR-11C N15V-GM/N15S-GT	K4W2G1646Q-BC1A N15V-GM/N15S-GT	K4W4G1646D-BC1A N15V-GM/N15S-GT	MT41J128M16JT-093G:K N15S-GT only	MT41K256M16HA-107G:E N15V-GM only	
RAM0 VRAM1, VRAM2, VRAM5, VRAM6		Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB	Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB	Stuff with Discrete 2GB/4GB	Stuff with Discrete 1GB	Stuff with Discrete 1GB	
RAM1 VRAM3, VRAM4, VRAM7, VRAM8		Stuff with Discrete 4GB		Stuff with Discrete 4GB		Stuff with Discrete 4GB			
R7642(Strap0-L)			N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L				
R7631(Strap0-H)		N15S-GT:64.49925.6DL	N15S-GT:64.49925.6DL	N16S-GT:64.49925.6DL	N15S-GT:64.49925.6DL	N15V-GM:64.10025.L0L	N15S-GT:64.49925.6DL	N15V-GM:64.10025.L0L	
R7643(Strap1-L)			N15V-GM:64.10025.L0L	N16V-GM:064.45325.06DL		N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7632(Strap1-H)					N15V-GM:64.10025.L0L				
R7644(Strap2-L)						N15V-GM:64.10025.L0L			
R7633(Strap2-H)			N15V-GM:64.10025.L0L	N16V-GM:64.10025.L0L	N15V-GM:64.10025.L0L			N15V-GM:64.10025.L0L	
R7645(Strap3-L)				N16V-GM:64.49915.6DL					
R7635(Strap3-H)			N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7646(Strap4-L)			N15V-GM:64.10025.L0L	N16V-GM:064.45325.06DL	N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7634(Strap4-H)									
R7639(ROM_SI-L)		N15S-GT:64.24925.6DL	N15V-GM:64.10025.L0L	N16S-GT:64.20025.L0L	N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7636(ROM_SI-H)			N15S-GT:64.10025.L0L		N15S-GT:64.20025.L0L		N15S-GT:64.15025.6DL		
R7640(ROM_SO-L)		N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L	N16S-GT:64.49915.6DL	N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7637(ROM_SO-H)				N16V-GM:64.49915.6DL			N15S-GT:64.49915.6DL		
R7641(ROM_SCLK-L)		N15S-GT:64.49915.6DL	N15V-GM:64.10025.L0L	N16S-GT:64.49915.6DL	N15V-GM:64.10025.L0L	N15V-GM:64.10025.L0L		N15V-GM:64.10025.L0L	
R7638(ROM_SCLK-H)				N16V-GM:64.49915.6DL			N15S-GT:64.49915.6DL		

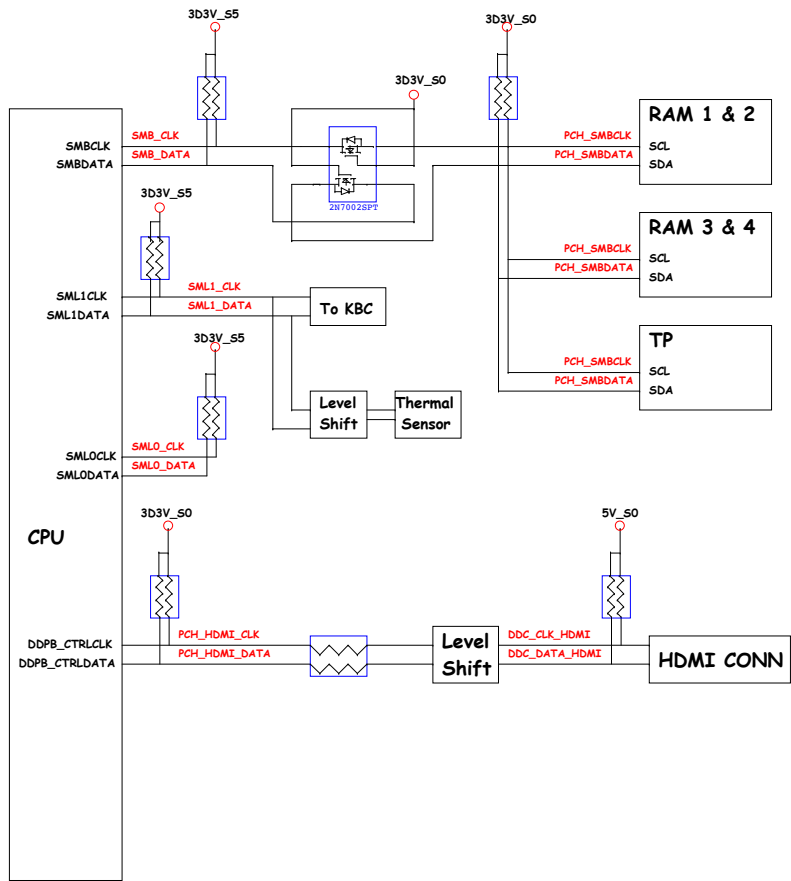
(AC mode)

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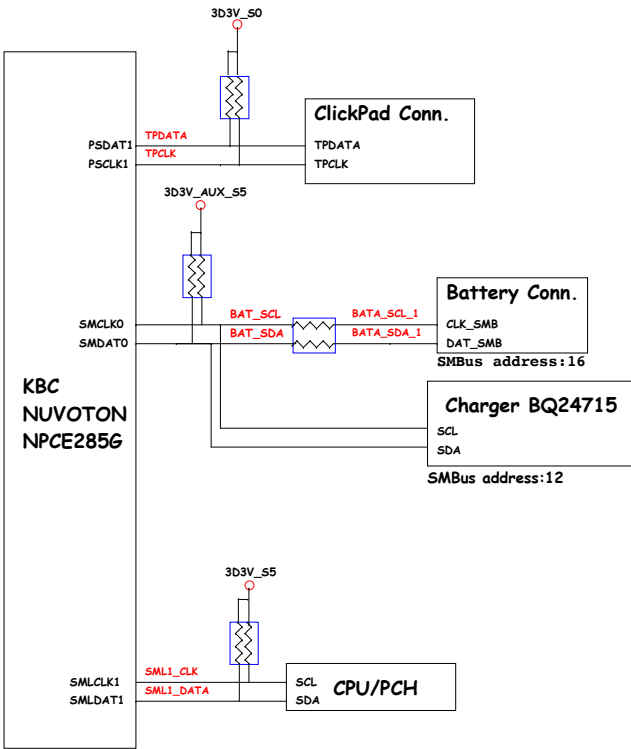


BOM1

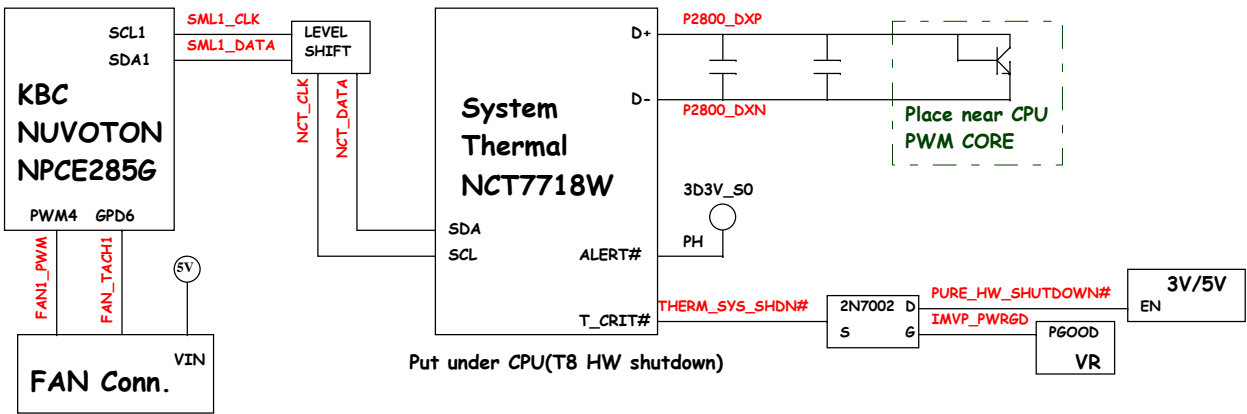
CPU/PCH SMBus Block Diagram



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

