

PCB NO : DAB00080000  
BOM P/N : 431AOM31L01

ZZZ  
PCB 36N LA-K661P REV0 M/B 1 S  
DAB00080000  
PCBR@

ZZZ1  
PCB 36N LA-K661P REV1 M/B 1  
DAB00080010  
PCBR1@

ZZZ2  
PCB 36N LA-K661P REV1 M/B GOLD 1 A31!  
DAB00080011  
PCBR3@

DAB00080012 PCB 36N LA-K661P REV1 M/B TRIPOD 1 A31 !  
DAB00080013 PCB 36N LA-K661P REV1 M/B HANNSTA 1 A31!

ZZZ  
SMT EMC CML 6G EE AK661 GDL55  
X4EAOM31L01  
X4E6G@

ZZZ  
SMT EMC CML 8G EE AK661 GDL55  
X4EAOM31L02  
X4E8G@

# Compal Confidential

## CML-H MB Schematic Document

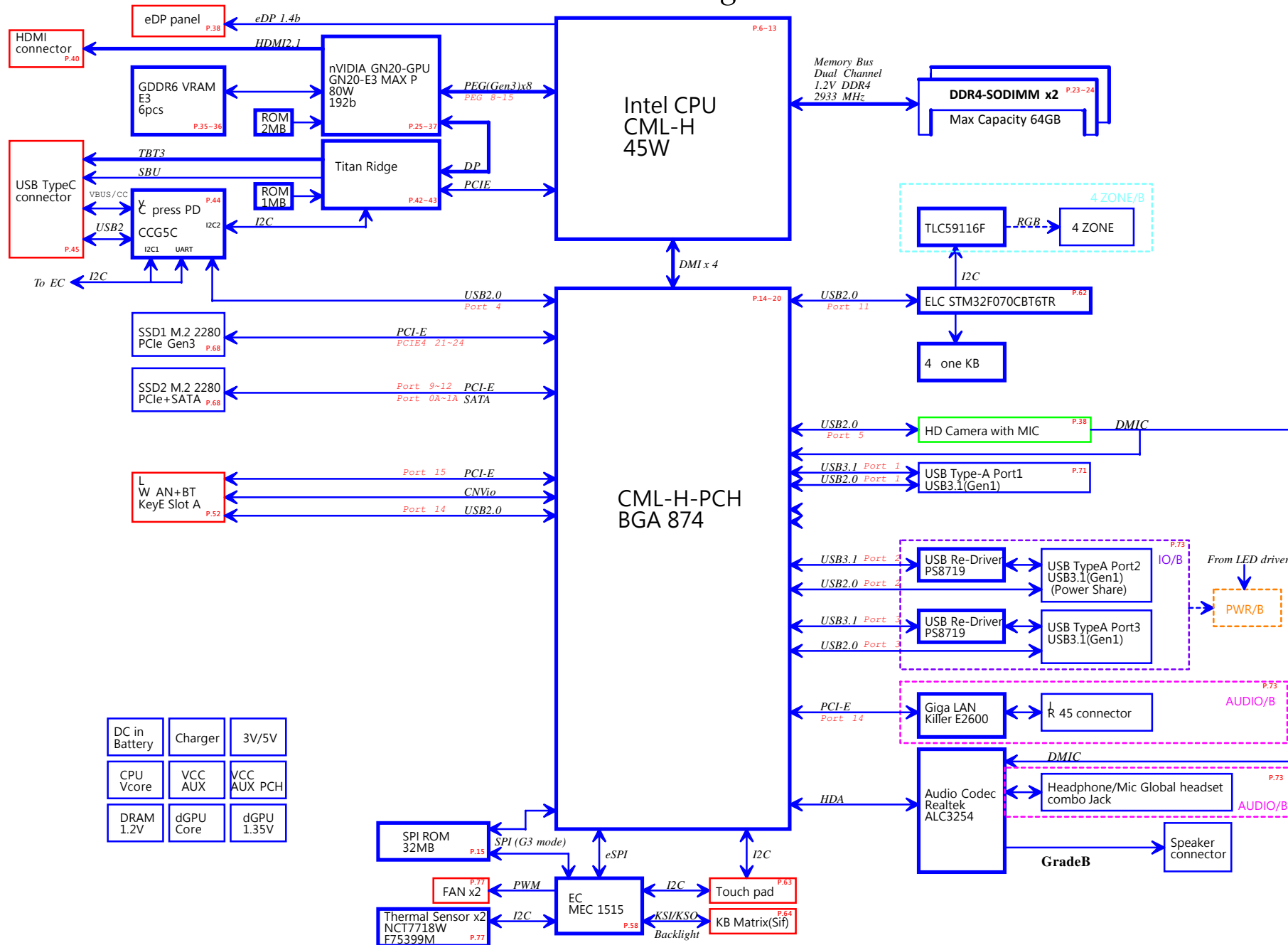
Rev: 1.0

2021.02.08

@ : Un-pop Component  
DIS@/UMA@ : GPU Support  
JP@/PJP@ : JUMP  
  
EMI@/ESD@/RF@ : EMI, ESD and RF Component  
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component  
XDP@ : XDP Component  
CONN@ : Connector Component  
SW@ : Debug PWR But t on  
  
CNV@/@CNV@ : CNVi Support  
G3@ : EC G3 Flash Sharing

|   |  |                           |                 |                          |          |
|---|--|---------------------------|-----------------|--------------------------|----------|
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|   |  | Size                      | Document Number | 0.2                      |          |
|   |  | Custom                    | LA-K661P        |                          |          |
| Date:   |  | Monday, February 08, 2021 |                 | Sheet                    | 1 of 121 |

### Block Diagram



|  |            |                    |            |   |            |
|--|------------|--------------------|------------|---|------------|
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|  |            |                    |            | Date: <u>March 09, 2021</u><br><b>LA-K661P</b>          | <u>0.2</u> |
|  |            |                    |            | Sheet   | 2 of 121   |

Board ID table

| Item | Pull-down | Pull-up | Voltage | Board ID/Model ID |
|------|-----------|---------|---------|-------------------|
| 1    | 100       | 10K     | 3.000   | Pre-EVT           |
| 2    | 100       | 17.8K   | 2.801   | EVT               |
| 3    | 100       | 27K     | 2.598   |                   |
| 4    | 100       | 37.4K   | 2.402   | DVT1              |
| 5    | 100       | 49.9K   | 2.201   | DVT2              |
| 6    | 100       | 64.9K   | 2.001   |                   |
| 7    | 100       | 82.5K   | 1.808   | Pilot             |
| 8    | 100       | 107K    | 1.594   |                   |
| 9    | 100       | 154K    | 1.299   |                   |
| 10   | 100       | 200K    | 1.1     |                   |

Power State

| STATE                | SIGNAL | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V  | +VS | Clock |
|----------------------|--------|---------|---------|---------|-------|-----|-----|-------|
| S0 (Full ON)         |        | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | ON    |
| S3 (Suspend to RAM)  |        | LOW     | HIGH    | HIGH    | ON    | ON  | OFF | OFF   |
| S4 (Suspend to Disk) |        | LOW     | LOW     | HIGH    | ON    | OFF | OFF | OFF   |
| S5 (Soft OFF)        |        | LOW     | LOW     | LOW     | ON    | OFF | OFF | OFF   |

PCH SMBUS Address Table

| PCH_SMBUS Port            | Power Rail | Device | Address |
|---------------------------|------------|--------|---------|
| PCH_SMBCLK<br>PCH_SMBDATA | +3VALW_PCH | JDIMM1 |         |
|                           |            | JDIMM2 |         |

EC SMBUS Address Table


| EC_SMBUS Port                            | Power Rail | Device      | Address |
|--|------------|-------------|---------|
| GPU_THM_SMBCLK<br>GPU_THM_SMBDAT         | +3VS       | Thermal 1   | 0x98h   |
|  |            | Thermal 2   | 0x9Ah   |
|  |            | GPU (GN20E) | 0x9E    |
| PBAT_CHG_SMBCLK<br>PBAT_CHG_SMBDAT       | +3VALW_EC  | BAT         | 0x16    |
|  |            | CHGR        | 0x12    |
| DAT_TP_SIO_I2C_CLK<br>CLK_TP_SIO_I2C_DAT | +TP_VDD    | Touch Pad   | 0x2C    |
|  |            |             |         |
| UPD1_SMBCLK<br>UPD1_SMBDAT               | +3V_VSYS   | CCG5C       | 0x08    |


CML-H-PCH HM470

| HSIO | USB3.2 | PCIe | SATA3 | Function                          |
|------|--------|------|-------|-----------------------------------|
| 0    | 1      |      |       | JUSB                              |
| 1    | 2      |      |       | JUSB                              |
| 2    | 3      |      |       | JUSB                              |
| 3    | 4      |      |       |                                   |
| 4    | 5      |      |       |                                   |
| 5    | 6      |      |       |                                   |
| 6    | 7      |      |       |                                   |
| 7    | 8      |      |       |                                   |
| 8    |        |      |       |                                   |
| 9    |        |      |       |                                   |
| 10   |        |      |       |                                   |
| 11   |        |      |       |                                   |
| 12   |        | 7    |       |                                   |
| 13   |        |      |       |                                   |
| 14   |        | 9    |       |                                   |
| 15   |        | 10   |       | JSSD2 , 2280<br>SATA x2 / PCIe x4 |
| 16   |        | 11   | 0A    |                                   |
| 17   |        | 12   | 1A    |                                   |
| 18   |        | 13   | 0B    |                                   |
| 19   |        | 14   | 1B    | LAN                               |
| 20   |        | 15   |       | WLAN                              |
| 21   |        | 16   |       |                                   |
| 22   |        | 17   |       |                                   |
| 23   |        | 18   |       | TBT                               |
| 24   |        | 19   |       |                                   |
| 25   |        | 20   |       |                                   |
| 26   |        | 21   |       |                                   |
| 27   |        | 22   |       | JSSD1 , 2280<br>PCIe x4           |
| 28   |        | 23   |       |                                   |
| 29   |        | 24   |       |                                   |

| USB2 | Function        |
|------|-----------------|
| 1    | JUSB            |
| 2    | JUSB            |
| 3    | JUSB            |
| 4    | CPU side Type C |
| 5    | HD CAM          |
| 6    |                 |
| 7    |                 |
| 8    |                 |
| 9    |                 |
| 10   |                 |
| 11   | ELC MCU         |
| 12   |                 |
| 13   |                 |
| 14   | Bluetooth       |

Symbol Note :

 Digital Ground

 Analog Ground

60 mils/1A = 1/3 oz  
40 mils/1A = 0.5 oz  
20 mils/1A = 1 oz  
10 mils/1A = 2 oz

Voltage Rails

| Power Plane   | Description                                    | S0  | S0ix | S3  | S4/S5 | DS3 |
|---------------|--|-----|------|-----|-------|-----|
| +19V_VIN      | Adapter power supply                           | N/A | N/A  | N/A | N/A   | N/A |
| +12.6V_BATT+  | Battery power supply                           | N/A | N/A  | N/A | N/A   | N/A |
| +19VB         | AC or battery power rail for power drcut       | N/A | N/A  | N/A | N/A   | N/A |
| +VCC_CORE     | Processor core rail                            | ON  | OFF  | OFF | OFF   | OFF |
| +VCCGT        | Sliced graphics power rail                     | ON  | OFF  | OFF | OFF   | OFF |
| +VCCSA        | System Agent power rail                        | ON  | OFF  | OFF | OFF   | OFF |
| +VCCIO        | IO power rail                                  | ON  | OFF  | OFF | OFF   | OFF |
| +3.3V_BAT_LDO | RTC power                                      | ON  | ON   | ON  | ON    | ON  |
| +RTC_CELL     | +3.3V_BAT_LDO/+3VLP for suspend power          | ON  | ON   | ON  | ON    | ON  |
| +5VALW        | System +5VALW power rail                       | ON  | ON   | ON  | ON*   | ON  |
| +3VALW        | System +3VALW always on power rail             | ON  | ON   | ON  | ON*   | ON  |
| +3VALW_PCH    | +3VALW Primary Power Well for PCH              | ON  | ON   | ON  | ON*   | OFF |
| +3VALW_DSW    | +3VALW power for PCH DSW rails                 | ON  | ON   | ON  | ON*   | ON  |
| +1.8V_PRIM    | System +1.8V power rail                        | ON  | ON   | ON  | ON*   | OFF |
| +1VALW        | System +1.05V power rail                       | ON  | ON   | ON  | ON*   | OFF |
| +1.2V_DDR     | DDR4 +1.2V power rail (VDDQ)                   | ON  | ON   | ON  | OFF   | ON  |
| +0.6V_DDR_VTT | DDR4 +0.6VS power rail for DDR terminator      | ON  | OFF  | OFF | OFF   | OFF |
| +2.5V_MEM     | DDR4 +2.5V power rail (Vpp)                    | ON  | ON   | ON  | OFF   | ON  |
| +VCCST        | Sustain voltage for processor in Standby modes | ON  | ON   | ON  | OFF   | OFF |
| +VCCSTG       | Gated version of VCCST                         | ON  | OFF  | OFF | OFF   | OFF |
| +5VS          | System +5VS power rail                         | ON  | ON   | OFF | OFF   | OFF |
| +3VS          | System +3VS power rail                         | ON  | ON   | OFF | OFF   | OFF |
| +1.8VS        | System +1.8VS power rail                       | ON  | ON   | OFF | OFF   | OFF |
|               |  |     |      |     |       |     |
|               |  |     |      |     |       |     |

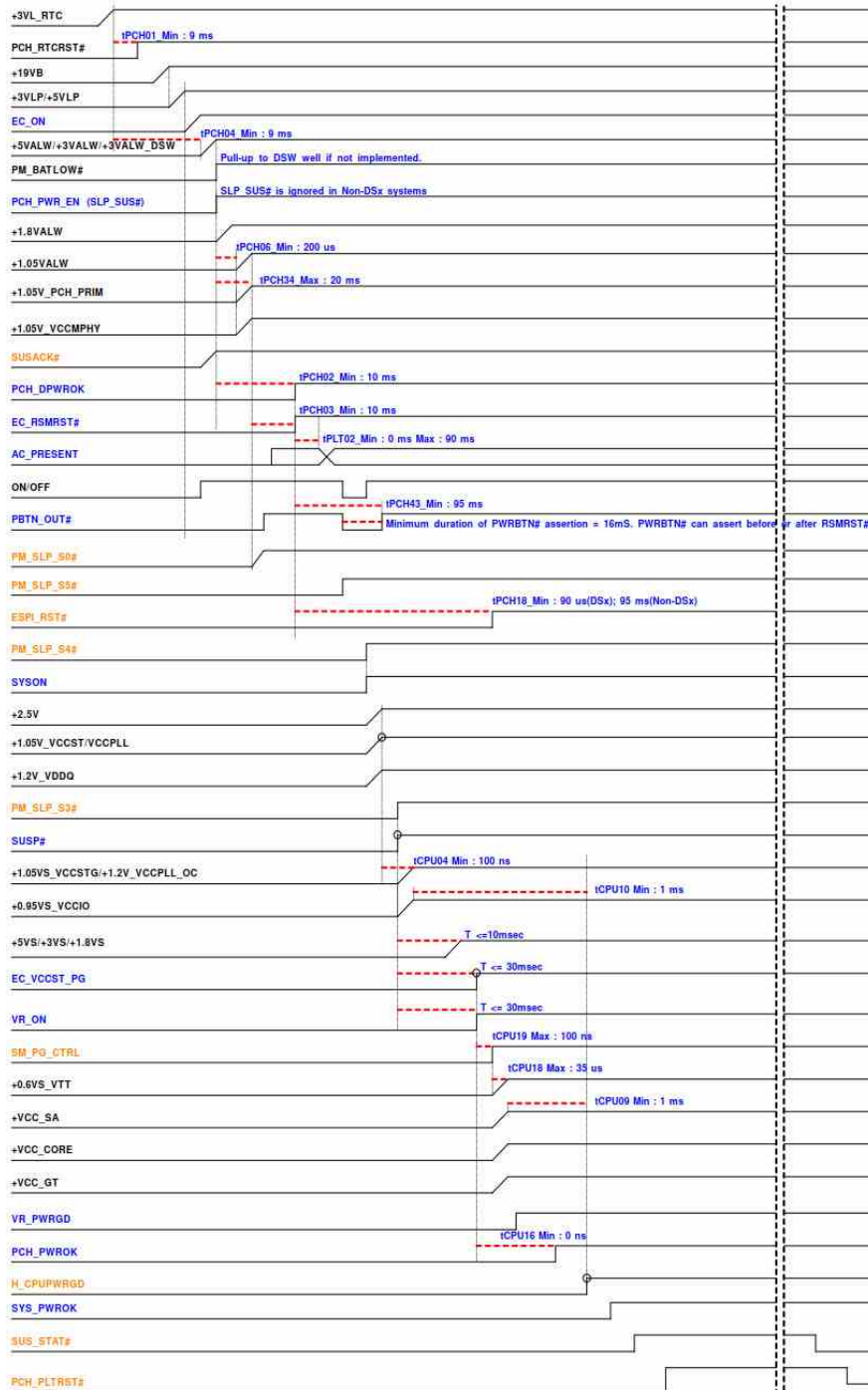


G3-&gt;S0

S0-&gt;S3

S3 -&gt;S0

S0-&gt;S5



|   |  |                           |  |            |  |
|---|--|---------------------------|--|------------|--|
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| 02  |  | 02                        |  | 02         |  |
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| 5   |  | of                        |  | 121        |  |

## CPU R1:

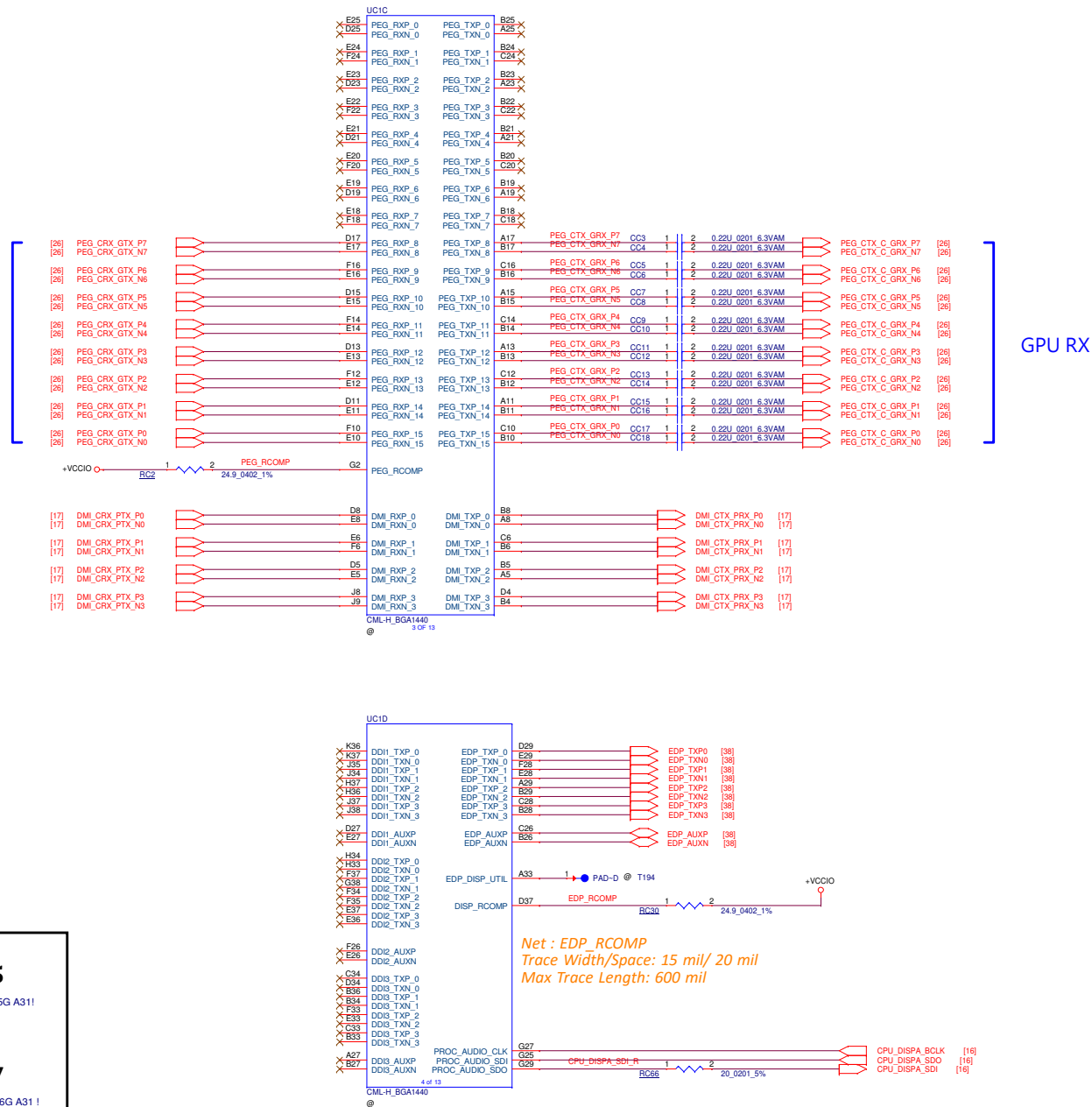
**CPU I7 QS**  
CL8070104399315 SRH8Q R1 2.6G A31 !  
SA0000DW2L  
I7QS@  
9/15 DVT1.1 modify  
follow DVT1.1 proto

**CPU I7 MP**  
CL8070104399317 SRK3Y R1 2.2G A31 !  
SA0000DW2L  
I7MP@  
1/18 DVT2.1 add

## CPU R3:

**CPU I5**  
CL8070104399510 SRH84 R1 2.5G A31 !  
SA0000DCP2L  
SRH84R3@

**CPU I7**  
CL8070104399315 SRH8Q R1 2.6G A31 !  
SA0000DCN2L  
SRH8QR3@



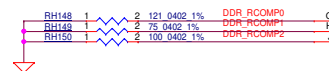
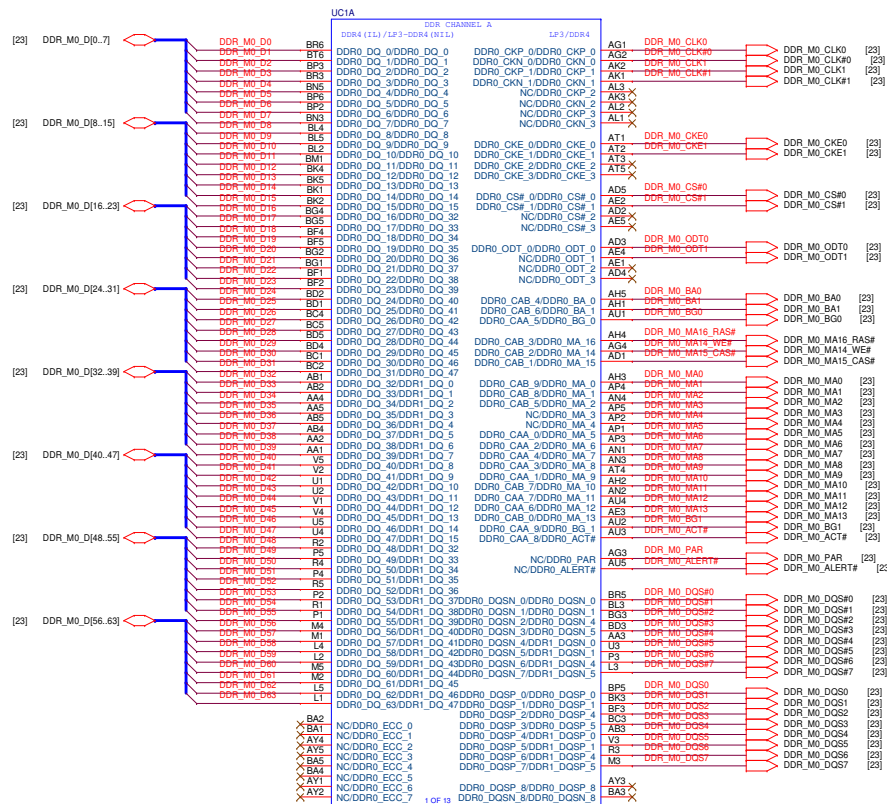
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| Size  |            | Document Number           |            | LA-K661P                 |  |
| Date  |            | Monday, February 06, 2021 |            | Sheet 6 of 121           |  |
| Rev   |            | 0.2                       |            |                          |  |

# Reserve

|   |                           |                 |            |                          |                 |     |
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|   |                           |                 |            |                          | LA-K661P        | 0.2 |
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## CHANNEL-A

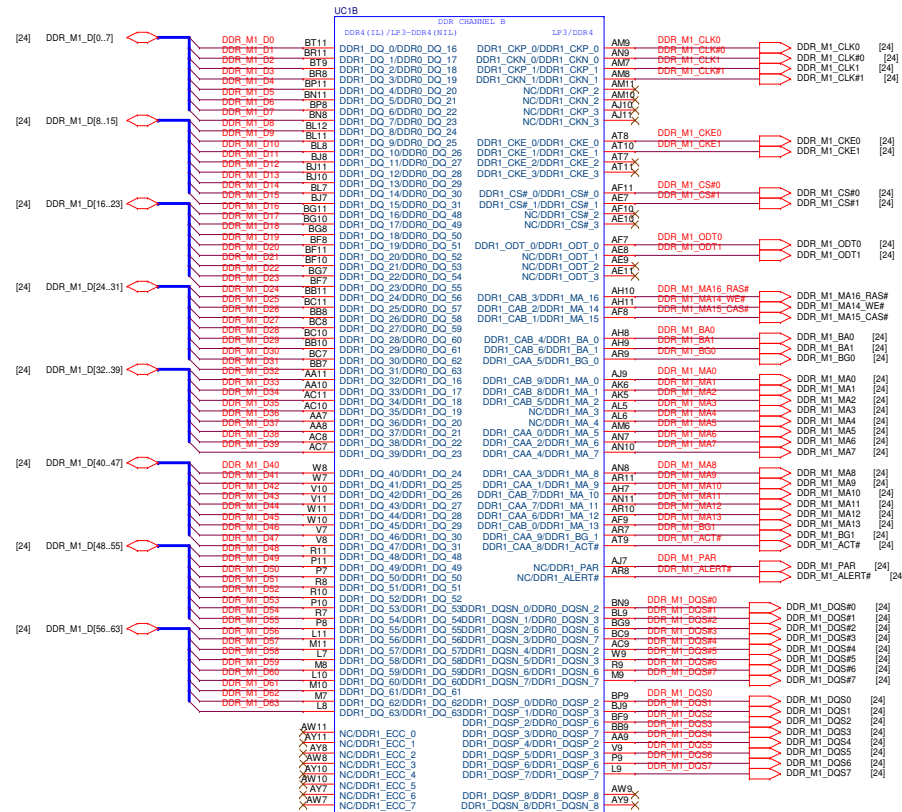
### Interleaved Memory



Net : DDR\_RCOMP0  
Net : DDR\_RCOMP1  
Net : DDR\_RCOMP2  
Trace Width/Space: 15 mil/ 25 mil  
Max Trace Length: 500 mil

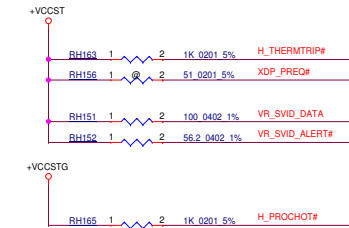
## CHANNEL-B

### Interleaved Memory

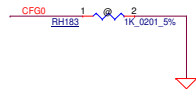


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|   |  |                    |                 | LA-K661P      |                           |                |
|   |  |                    |                 | Date:         | Monday, February 08, 2021 | Sheet 8 of 121 |

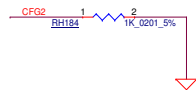




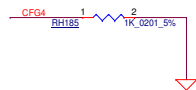
| Stall reset sequence after PCU FLL lock until de-asserted |  |
|---|--|
| CFG0  | ★ 1 = (Default) Normal Operation; No stall.<br>0 = Stall |



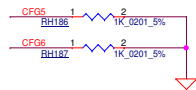
| PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS |  |
|--|--|
| CFG2   | 1: Normal Operation; Lane # definition matches socket pin map definition<br>★ 0: Lane Reversed |



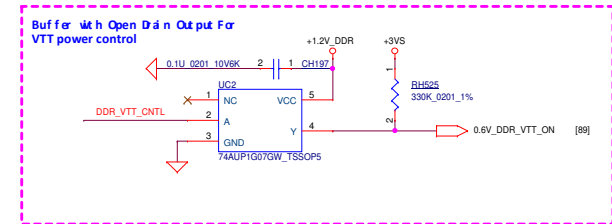
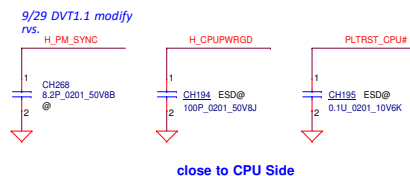
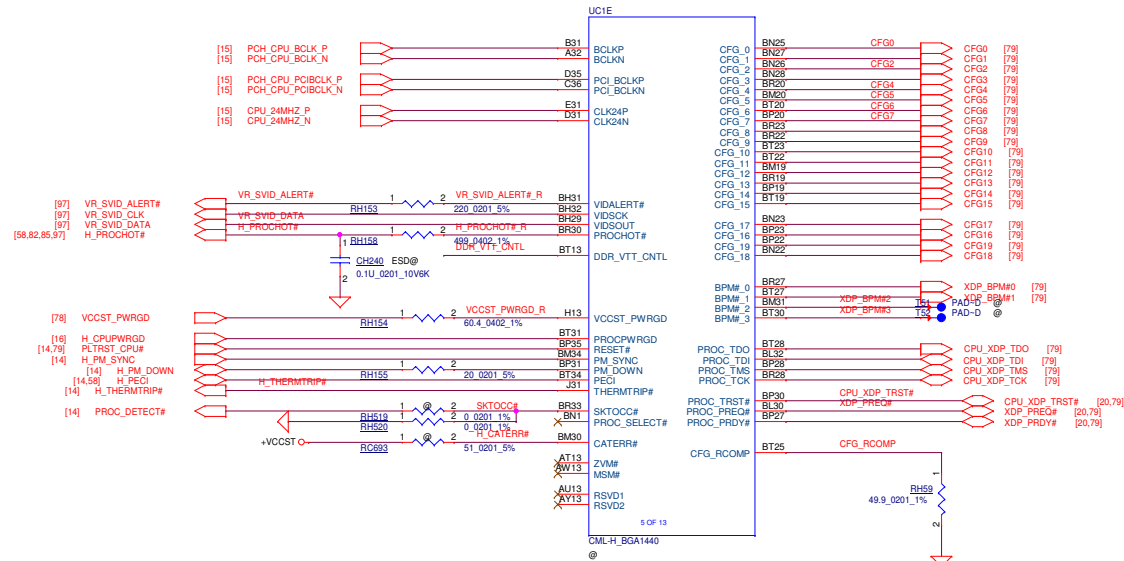
| Display Port Presence Strap |  |
|-----------------------------|--|
| CFG4                        | 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>★ 0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

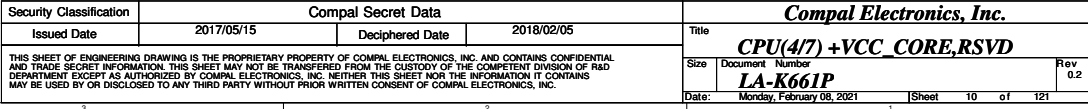


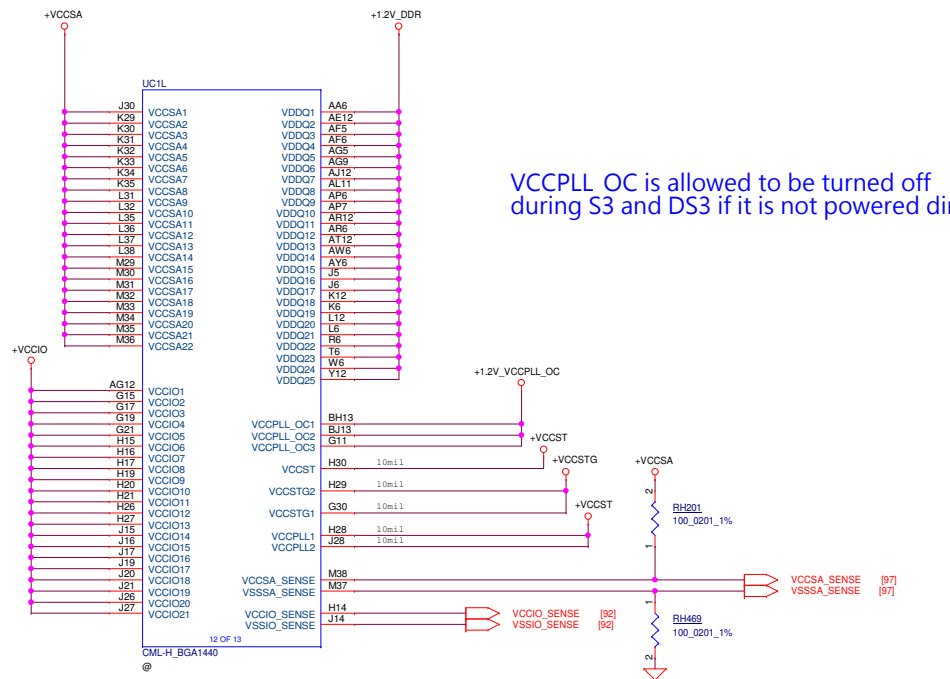
| PCIe Port Bifurcation Straps |  |
|------------------------------|--|
| CFG[6:5]                     | 11: (Default) x16 - Device 1 functions 1 and 2 disabled<br>10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled<br>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)<br>★ 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled |



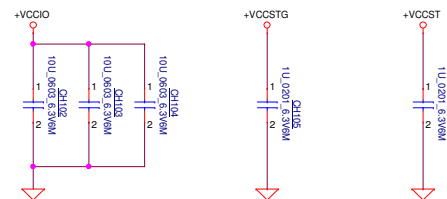
| PEG DEFER TRAINING |  |
|--------------------|--|
| CFG7               | ★ 1: (Default) PEG Train immediately following xRESETB de assertion<br>0: PEG Wait for BIOS for training |





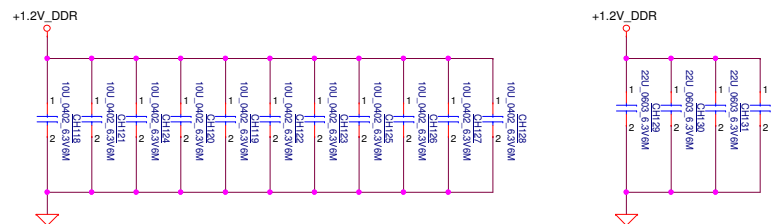


VCCPLL\_OC is allowed to be turned off during S3 and DS3 if it is not powered directly from VDD



Close to H29,G30

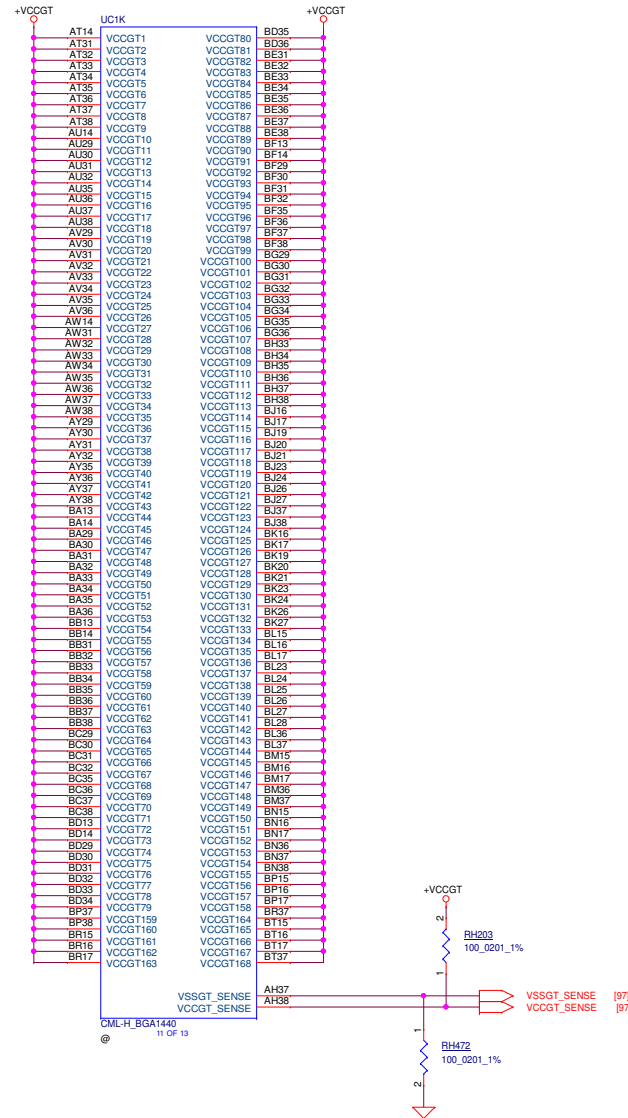
Close to H30



Close to BH13,BJ13,G11

Close to H28, J28

|   |                    |                 |                          |                 |
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| CPU(S7) +VCCSA,+VCCIO   |                    |                 |                          | 0.2             |
| LA-K661P  |                    |                 |                          | Date            |
| Monday, February 05, 2021   |                    |                 |                          | Sheet 11 of 121 |



1. VccGT SENSE / VssGT SENSE Trace Length Match 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC1 RC2 should be placed within 2 inches (50.8 mm) of CPU

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|   |            |                    |            | Date                     | Monday, February 08, 2021 |
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|   |            |                    |            | Rev                      | 0.2                       |

| UC1F |        |         | UC1G |      |         | UC1H    |       |      | F15     |         |      |
|------|--------|---------|------|------|---------|---------|-------|------|---------|---------|------|
| A10  | VSS_1  | VSS_82  | AK4  | AW5  | VSS_163 | VSS_244 | BU15  | BN4  | VSS_325 | VSS_409 | F17  |
| A12  | VSS_2  | VSS_83  | AL10 | AY12 | VSS_164 | VSS_245 | BU18  | BN7  | VSS_326 | VSS_410 | F19  |
| A16  | VSS_3  | VSS_84  | AL12 | AY33 | VSS_165 | VSS_246 | BU22  | BP14 | VSS_327 | VSS_411 | F2   |
| A18  | VSS_4  | VSS_85  | AL14 | AY34 | VSS_166 | VSS_247 | BU25  | BP18 | VSS_328 | VSS_412 | F21  |
| A20  | VSS_5  | VSS_86  | AL33 | BA9  | VSS_167 | VSS_248 | BU29  | BP21 | VSS_329 | VSS_413 | F23  |
| A22  | VSS_6  | VSS_87  | AL34 | BA10 | VSS_168 | VSS_249 | BU30  | BP24 | VSS_330 | VSS_414 | F25  |
| A24  | VSS_7  | VSS_88  | AL4  | BA11 | VSS_169 | VSS_250 | BU31  | BP25 | VSS_331 | VSS_415 | F27  |
| A26  | VSS_8  | VSS_89  | AL7  | BA12 | VSS_170 | VSS_251 | BU32  | BP26 | VSS_332 | VSS_416 | F29  |
| A28  | VSS_9  | VSS_90  | AL9  | BA37 | VSS_171 | VSS_252 | BU33  | BP29 | VSS_333 | VSS_417 | F3   |
| A30  | VSS_10 | VSS_91  | AM1  | BA38 | VSS_172 | VSS_253 | BU34  | BP33 | VSS_334 | VSS_418 | F31  |
| A6   | VSS_11 | VSS_92  | AM12 | BA6  | VSS_173 | VSS_254 | BU35  | BP34 | VSS_335 | VSS_419 | F36  |
| A9   | VSS_12 | VSS_93  | AM2  | BA7  | VSS_174 | VSS_255 | BU36  | BP7  | VSS_336 | VSS_420 | F4   |
| AA12 | VSS_13 | VSS_94  | AM3  | BA8  | VSS_175 | VSS_256 | BK13  | BR12 | VSS_341 | VSS_425 | F5   |
| AA29 | VSS_14 | VSS_95  | AM37 | BA9  | VSS_176 | VSS_257 | BK14  | BR14 | VSS_337 | VSS_421 | F8   |
| AA30 | VSS_15 | VSS_96  | AM38 | BB1  | VSS_177 | VSS_258 | BK15  | BR18 | VSS_338 | VSS_422 | F9   |
| AB33 | VSS_16 | VSS_97  | AM4  | BB12 | VSS_178 | VSS_259 | BK18  | BR21 | VSS_339 | VSS_423 | F9   |
| AB34 | VSS_17 | VSS_98  | AM5  | BB2  | VSS_179 | VSS_260 | BK22  | BR24 | VSS_340 | VSS_424 | G10  |
| AB6  | VSS_18 | VSS_99  | AN12 | BB29 | VSS_180 | VSS_261 | BK25  | BR25 | VSS_342 | VSS_426 | G14  |
| AC1  | VSS_19 | VSS_100 | AN29 | BB3  | VSS_181 | VSS_262 | BK29  | BR26 | VSS_343 | VSS_427 | G16  |
| AC12 | VSS_20 | VSS_101 | AN30 | BB30 | VSS_182 | VSS_263 | BK6   | BR29 | VSS_344 | VSS_428 | G18  |
| AC2  | VSS_21 | VSS_102 | AN6  | BB4  | VSS_183 | VSS_264 | BL13  | BR34 | VSS_345 | VSS_429 | G20  |
| AC3  | VSS_22 | VSS_103 | AP10 | BB5  | VSS_184 | VSS_265 | BL14  | BR36 | VSS_346 | VSS_430 | G22  |
| AC37 | VSS_23 | VSS_104 | AP12 | BB6  | VSS_185 | VSS_266 | BL18  | BR7  | VSS_347 | VSS_431 | G23  |
| AC38 | VSS_24 | VSS_105 | AP12 | BC12 | VSS_186 | VSS_267 | BL19  | BT12 | VSS_348 | VSS_432 | G24  |
| AC4  | VSS_25 | VSS_106 | AP33 | BC13 | VSS_187 | VSS_268 | BL20  | BT14 | VSS_349 | VSS_433 | G26  |
| AC5  | VSS_26 | VSS_107 | AP34 | BC14 | VSS_188 | VSS_269 | BL21  | BT18 | VSS_350 | VSS_434 | G28  |
| AC6  | VSS_27 | VSS_108 | AP8  | BC33 | VSS_189 | VSS_270 | BL22  | BT21 | VSS_351 | VSS_435 | G4   |
| AD10 | VSS_28 | VSS_109 | AR1  | BC34 | VSS_190 | VSS_271 | BL29  | BT24 | VSS_352 | VSS_436 | G5   |
| AD11 | VSS_29 | VSS_110 | AR13 | BC6  | VSS_191 | VSS_272 | BL33  | BT26 | VSS_353 | VSS_437 | G6   |
| AD12 | VSS_30 | VSS_111 | AR14 | BD11 | VSS_192 | VSS_273 | BL38  | BT29 | VSS_354 | VSS_438 | G8   |
| AD29 | VSS_31 | VSS_112 | AR2  | BD12 | VSS_193 | VSS_274 | BL6   | BT32 | VSS_355 | VSS_439 | G9   |
| AD30 | VSS_32 | VSS_113 | AR29 | BD37 | VSS_194 | VSS_275 | BL11  | BT5  | VSS_356 | VSS_440 | H11  |
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| AD8  | VSS_34 | VSS_115 | AR30 | BD7  | VSS_196 | VSS_277 | BLM12 | C13  | VSS_358 | VSS_442 | H18  |
| AD9  | VSS_35 | VSS_116 | AR31 | BD8  | VSS_197 | VSS_278 | BLM14 | C15  | VSS_359 | VSS_443 | H27  |
| AE33 | VSS_36 | VSS_117 | AR32 | BD9  | VSS_198 | VSS_279 | BLM18 | C17  | VSS_360 | VSS_444 | H25  |
| AE34 | VSS_37 | VSS_118 | AR33 | BE1  | VSS_199 | VSS_280 | BLM2  | C19  | VSS_361 | VSS_445 | H32  |
| AE6  | VSS_38 | VSS_119 | AR34 | BE2  | VSS_200 | VSS_281 | BLM21 | C21  | VSS_362 | VSS_446 | H35  |
| AF1  | VSS_39 | VSS_120 | AR35 | BE29 | VSS_201 | VSS_282 | BLM22 | C25  | VSS_363 | VSS_447 | J10  |
| AF12 | VSS_40 | VSS_121 | AR36 | BE3  | VSS_202 | VSS_283 | BLM23 | C27  | VSS_364 | VSS_448 | J18  |
| AF13 | VSS_41 | VSS_122 | AR37 | BE30 | VSS_203 | VSS_284 | BLM24 | C29  | VSS_365 | VSS_449 | J22  |
| AF14 | VSS_42 | VSS_123 | AR38 | BE4  | VSS_204 | VSS_285 | BLM25 | C31  | VSS_366 | VSS_450 | J25  |
| AF2  | VSS_43 | VSS_124 | AR39 | BE5  | VSS_205 | VSS_286 | BLM26 | C37  | VSS_367 | VSS_451 | J32  |
| AF3  | VSS_44 | VSS_125 | AR4  | BE6  | VSS_206 | VSS_287 | BLM27 | C5   | VSS_368 | VSS_452 | J33  |
| AG10 | VSS_45 | VSS_126 | AR4  | BF12 | VSS_207 | VSS_288 | BLM28 | C8   | VSS_369 | VSS_453 | J36  |
| AG11 | VSS_46 | VSS_127 | AT29 | BF33 | VSS_208 | VSS_289 | BLM29 | C9   | VSS_370 | VSS_454 | J4   |
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| AG30 | VSS_49 | VSS_130 | AU10 | BG12 | VSS_211 | VSS_292 | BLM35 | D12  | VSS_373 | VSS_457 | K10  |
| AG6  | VSS_50 | VSS_131 | AU11 | BG13 | VSS_212 | VSS_293 | BLM38 | D14  | VSS_374 | VSS_458 | K11  |
| AG7  | VSS_51 | VSS_132 | AU12 | BG14 | VSS_213 | VSS_294 | BLM5  | D16  | VSS_375 | VSS_459 | K2   |
| AG8  | VSS_52 | VSS_133 | AU33 | BG37 | VSS_214 | VSS_295 | BLM6  | D18  | VSS_376 | VSS_460 | K3   |
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| AH36 | VSS_57 | VSS_138 | AU9  | BH11 | VSS_219 | VSS_300 | BLN14 | D28  | VSS_381 | VSS_465 | K8   |
| AH6  | VSS_58 | VSS_139 | AV37 | BH12 | VSS_220 | VSS_301 | BLN18 | D3   | VSS_382 | VSS_466 | K9   |
| AJ1  | VSS_59 | VSS_140 | AV38 | BH14 | VSS_221 | VSS_302 | BLN19 | D30  | VSS_383 | VSS_467 | L29  |
| AJ13 | VSS_60 | VSS_141 | AW29 | BH2  | VSS_222 | VSS_303 | BN2   | D33  | VSS_384 | VSS_468 | L30  |
| AJ2  | VSS_61 | VSS_142 | AW2  | BH3  | VSS_223 | VSS_304 | BN20  | D6   | VSS_385 | VSS_469 | L33  |
| AJ3  | VSS_62 | VSS_143 | AW2  | BH4  | VSS_224 | VSS_305 | BN21  | D9   | VSS_386 | VSS_470 | L34  |
| AJ37 | VSS_63 | VSS_144 | AW30 | BH5  | VSS_225 | VSS_306 | BN24  | E34  | VSS_387 | VSS_471 | M12  |
| AJ38 | VSS_64 | VSS_145 | AW3  | BH6  | VSS_226 | VSS_307 | BN29  | E35  | VSS_388 | VSS_472 | M13  |
| AJ4  | VSS_65 | VSS_146 | AW4  | BH7  | VSS_227 | VSS_308 | BN30  | E38  | VSS_389 | VSS_473 | N10  |
| AJ5  | VSS_66 | VSS_147 | W1   | BH8  | VSS_228 | VSS_309 | BN31  | E4   | VSS_390 | VSS_474 | N11  |
| AJ6  | VSS_67 | VSS_148 | W2   | BH9  | VSS_229 | VSS_310 | BN34  | E9   | VSS_391 | VSS_475 | N12  |
| W4   | VSS_68 | VSS_149 | W3   | I2   | VSS_230 | VSS_311 | P38   | N3   | VSS_392 | VSS_476 | N2   |
| W5   | VSS_69 | VSS_150 | W34  | I3   | VSS_231 | VSS_312 | P6    | N33  | VSS_393 | VSS_477 | BT8  |
| Y10  | VSS_70 | VSS_151 | W34  | I4   | VSS_232 | VSS_313 | R12   | N34  | VSS_394 | VSS_478 | BR9  |
| Y11  | VSS_71 | VSS_152 | AD7  | I5   | VSS_233 | VSS_314 | R29   | N4   | VSS_395 | VSS_479 |      |
| Y13  | VSS_72 | VSS_153 | AD7  | I6   | VSS_234 | VSS_315 | AV14  | N5   | VSS_396 | VSS_480 | A3   |
| Y14  | VSS_73 | VSS_154 | AD7  | I7   | VSS_235 | VSS_316 | BD38  | N6   | VSS_397 | VSS_481 | A34  |
| Y37  | VSS_74 | VSS_155 | AD7  | I8   | VSS_236 | VSS_317 | R30   | N7   | VSS_398 | VSS_482 | A4   |
| Y38  | VSS_75 | VSS_156 | AD7  | I9   | VSS_237 | VSS_318 | T1    | N8   | VSS_399 | VSS_483 | B3   |
| Y7   | VSS_76 | VSS_157 | AD7  | I10  | VSS_238 | VSS_319 | T10   | N9   | VSS_400 | VSS_484 | B37  |
| Y8   | VSS_77 | VSS_158 | AD7  | I11  | VSS_239 | VSS_320 | T11   | P12  | VSS_401 | VSS_485 | BR38 |
| Y9   | VSS_78 | VSS_159 | AD7  | I12  | VSS_240 | VSS_321 | T12   | P37  | VSS_402 | VSS_486 | BT3  |
| AK29 | VSS_79 | VSS_160 | AD7  | I13  | VSS_241 | VSS_322 | T13   | M14  | VSS_403 | VSS_487 | BT35 |
| AK30 | VSS_80 | VSS_161 | AD7  | I14  | VSS_242 | VSS_323 | T14   | M6   | VSS_404 | VSS_488 | BT36 |
|      | VSS_81 | VSS_162 | AD7  |      | VSS_243 | VSS_324 |       | N1   | VSS_405 | VSS_489 | BT4  |
|      |        |         |      |      |         |         |       | F11  | VSS_406 | VSS_490 | C2   |
|      |        |         |      |      |         |         |       | F13  | VSS_407 | VSS_491 | D38  |
|      |        |         |      |      |         |         |       |      | VSS_408 | VSS_492 |      |

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CML-H\_BGA1440  
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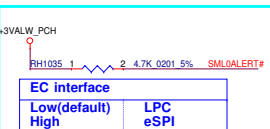
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| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                           |
|---|------------|--------------------|------------|--------------------------|---------------------------|
| Issued Date   | 2017/05/15 | Deciphered Date    | 2018/02/05 | Title                    | CPU(7/7) VSS              |
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|   |            |                    |            | Rev                      | 0.2                       |
|   |            |                    |            | Date                     | Monday, February 08, 2021 |
|   |            |                    |            | Sheet                    | 13 of 121                 |



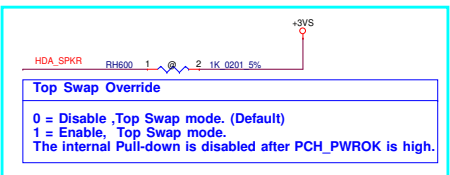
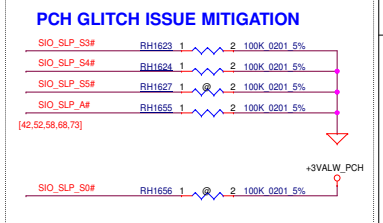
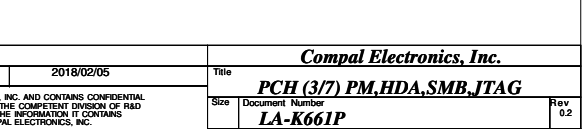
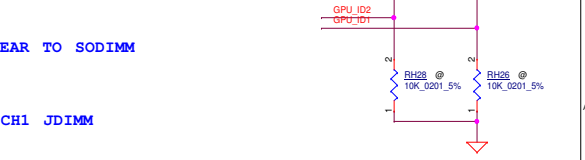
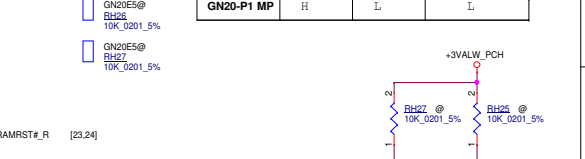
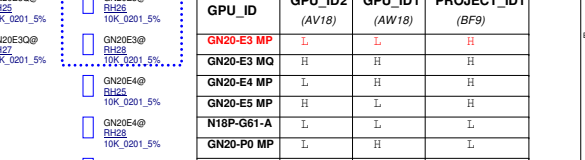
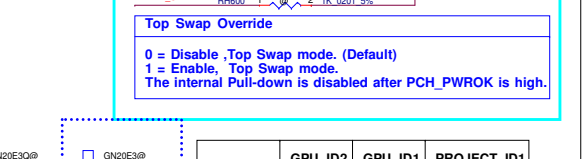
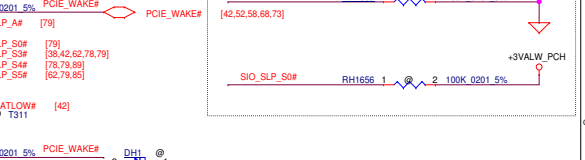
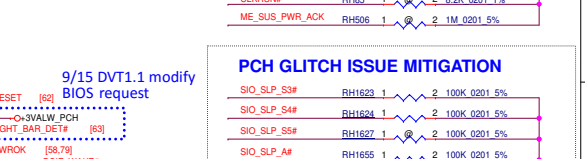
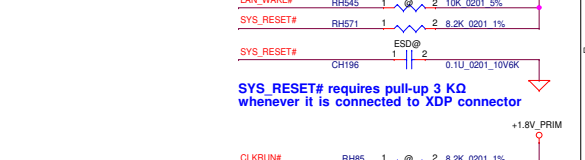
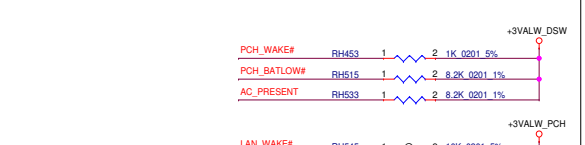
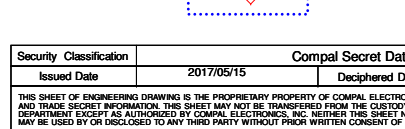
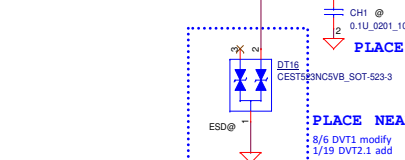
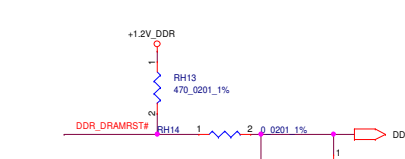
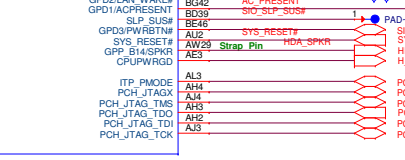
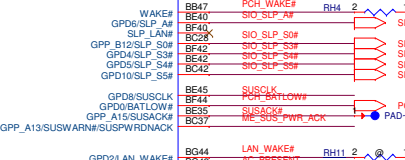
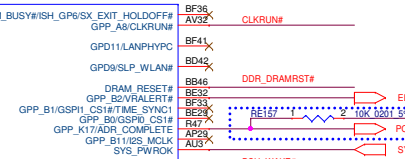
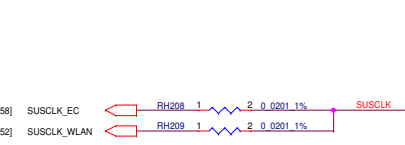
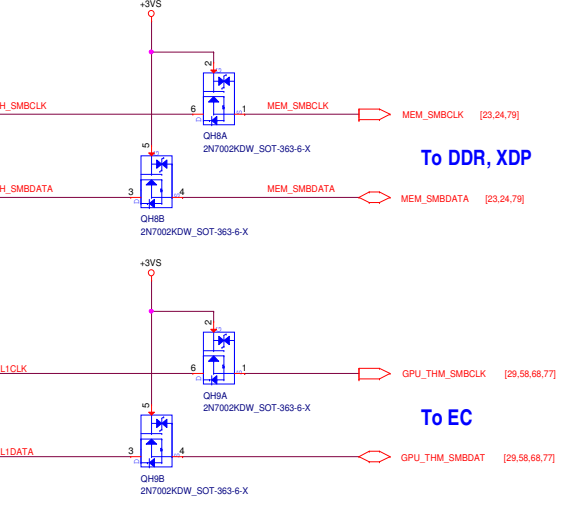
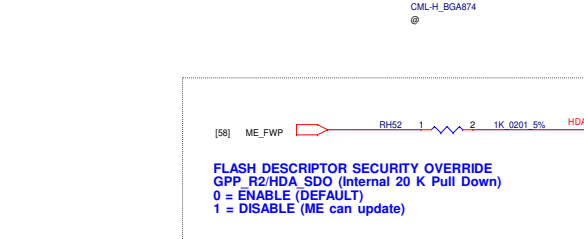
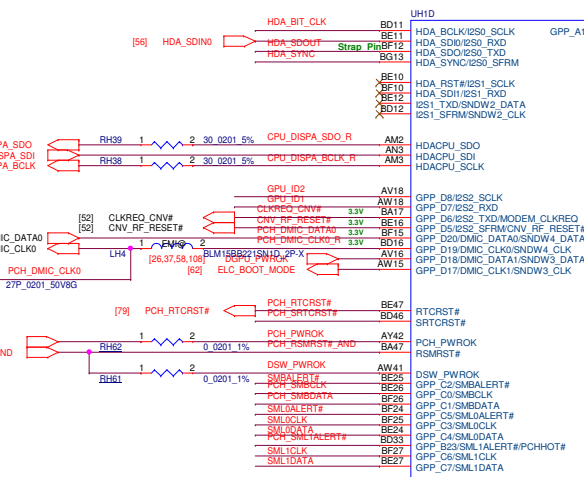
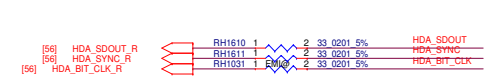
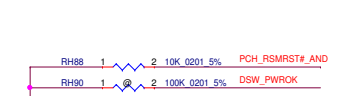
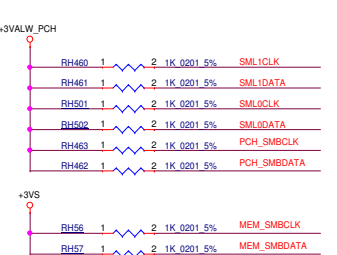
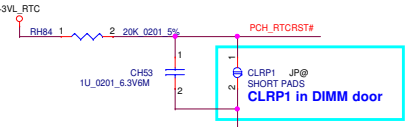
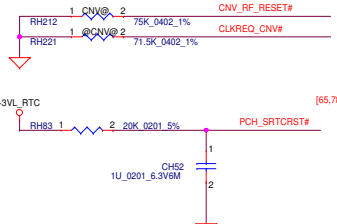






This signal has an internal pull-down.  
0 = Disable Intel DCI-OOB (Default)  
1 = Enable Intel DCI-OOB  
1. The internal pull-down is disabled after RSMRST# de-asserts.  
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.

This signal has a weak internal Pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.  
Notes:  
1. The internal Pull-down is disabled after RSMRST# de-asserts.  
2. This signal is in the primary well.

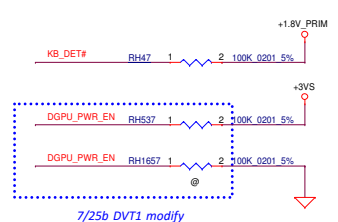
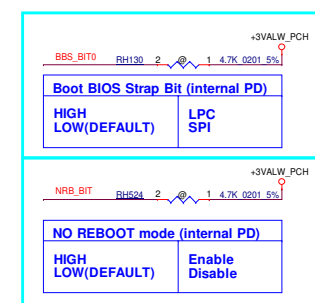
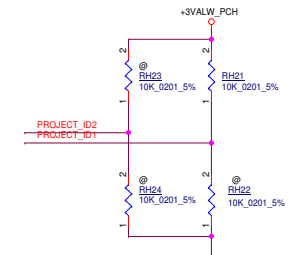


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|------------|----------------|----------------|-------------------|
| GN20-E3 MP | L              | L              | H                 |
| GN20-E3 MQ | H              | H              | H                 |
| GN20-E4 MP | L              | H              | H                 |
| GN20-E5 MP | H              | L              | H                 |
| N18P-G61-A | L              | L              | L                 |
| GN20-P0 MP | L              | H              | L                 |
| GN20-P1 MP | H              | L              | L                 |

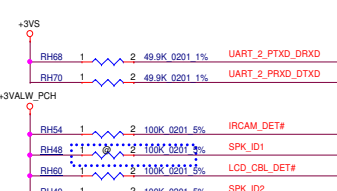




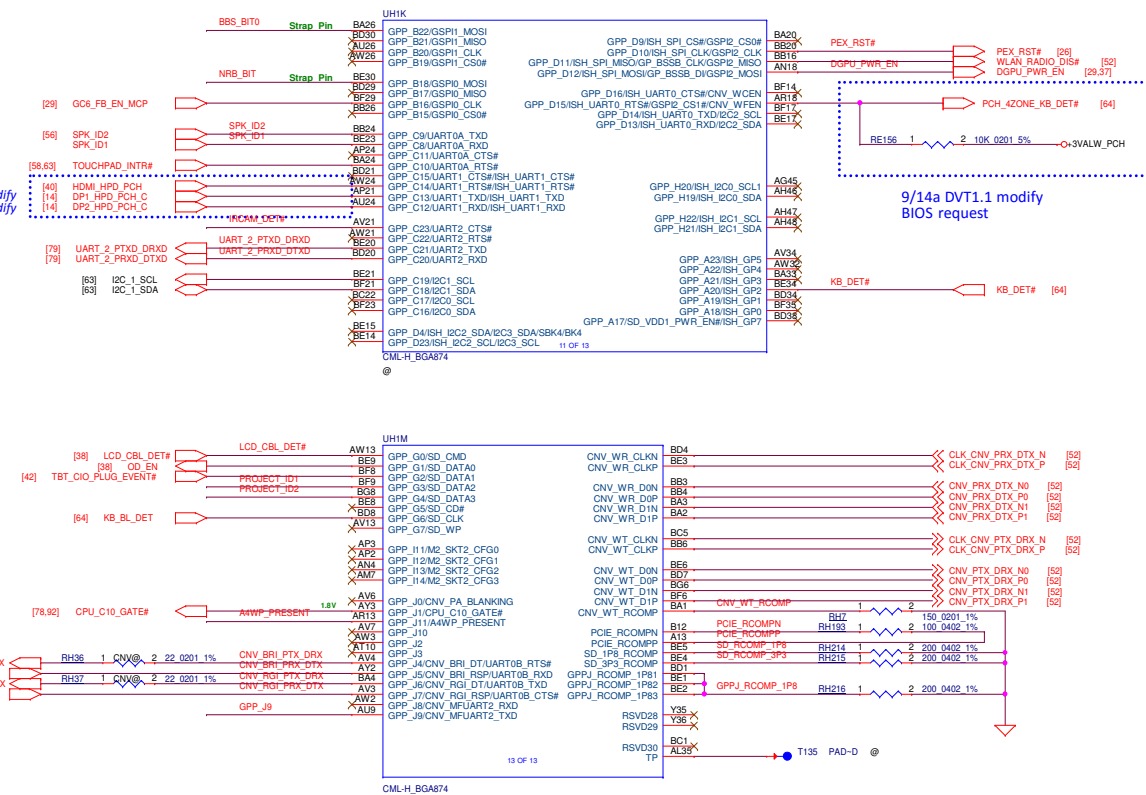
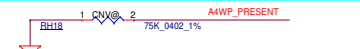
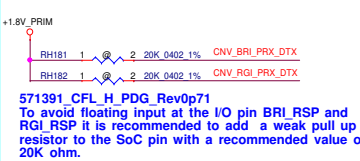
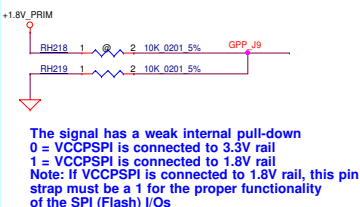
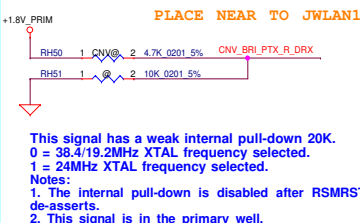
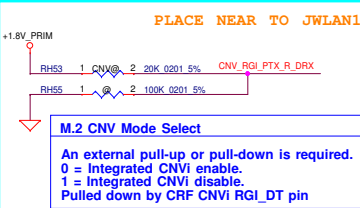
| GPU_ID     | PROJECT_ID1<br>(BF9) | PROJECT_ID2<br>(BG8) |
|------------|----------------------|----------------------|
| GN20-E3 MP | H                    | X                    |
| GN20-E3 MQ | H                    | X                    |
| GN20-E4 MP | H                    | X                    |
| GN20-E5 MP | H                    | X                    |



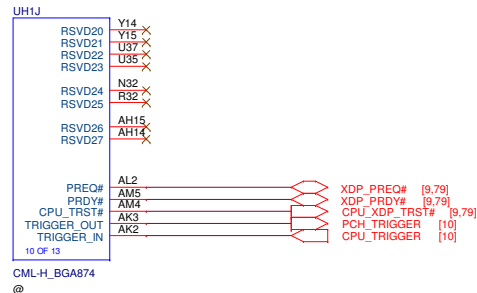
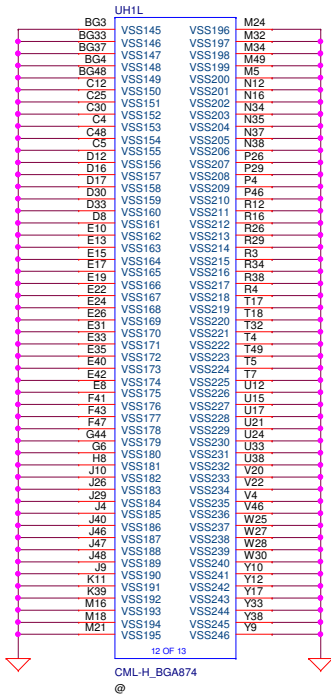
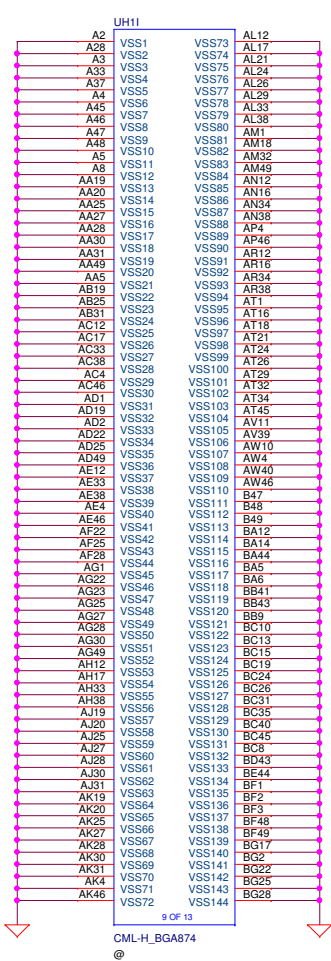
7/25b DVT1.1 modify



9/21 DVT1.1 modify







Main Function:

# Reserve

|   |                    |                 |            |                          |                           |                 |
|---|--------------------|-----------------|------------|--------------------------|---------------------------|-----------------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                           |                 |
| Issued Date   | 2020/03/05         | Deciphered Date | 2017/01/06 | Title                    | RSV                       |                 |
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|   |                    |                 |            |                          | LA-K661P                  | 0.2             |
|   |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 21 of 121 |

Main Function:

Reserve

|  |                    |                 |            |                          |                           |                 |
|--|--------------------|-----------------|------------|--------------------------|---------------------------|-----------------|
| Security Classification  | Compal Secret Data |                 |            | Compal Electronics, Inc. |                           |                 |
| Issued Date  | 2020/03/05         | Deciphered Date | 2019/04/01 | Title                    | RSV                       |                 |
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|  |                    |                 |            |                          | LA-K661P                  | 0.2             |
|  |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 22 of 121 |



Main Func = DDR

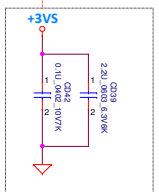
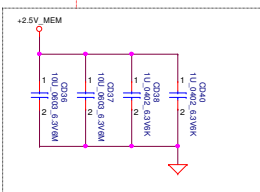
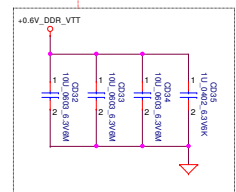
Layout Note:  
Place near JDIMM2.258

Layout Note:  
Place near JDIMM2.257,259

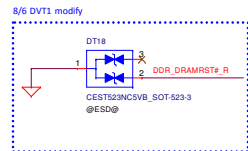
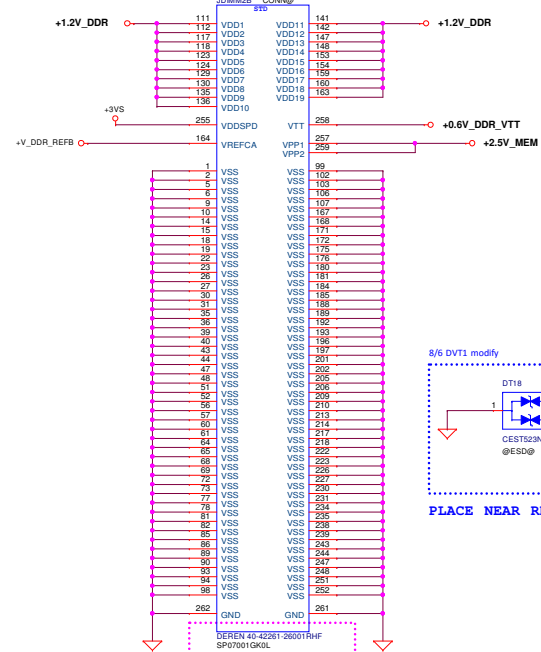
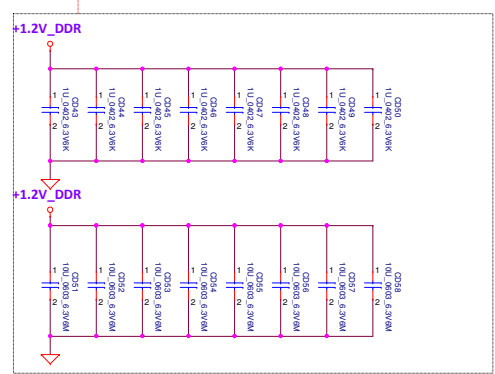
Layout Note:  
Place near JDIMM2.255

Interleaved Memory

STD (4 mm)

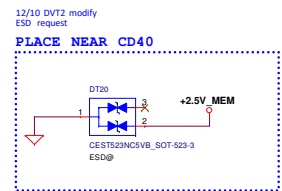
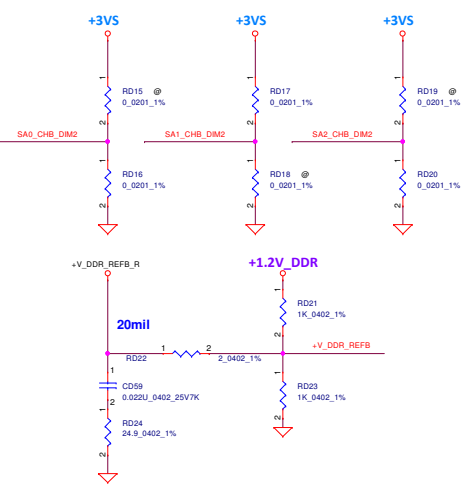


Layout Note:  
Place near JDIMM2

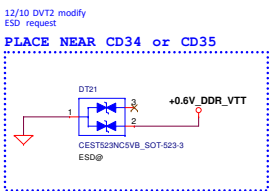


PLACE NEAR RD14 JDIMM

For ECC DIMM



PLACE NEAR CD40

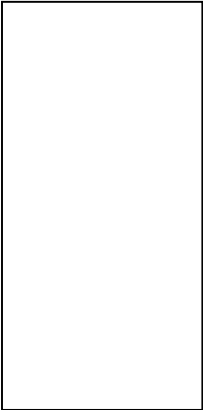


PLACE NEAR CD34 or CD35





VRAM X76:



7/25 DVT1 modify  
follow DVT1 proto plan

7/25 DVT1 modify  
follow DVT1 proto plan

7/25 DVT1 modify  
follow DVT1 proto plan

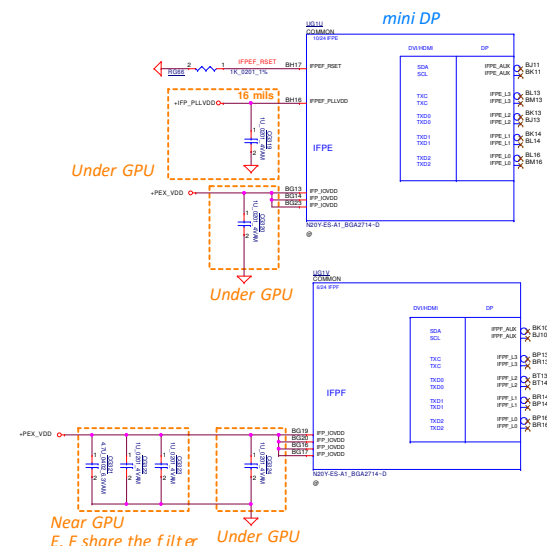
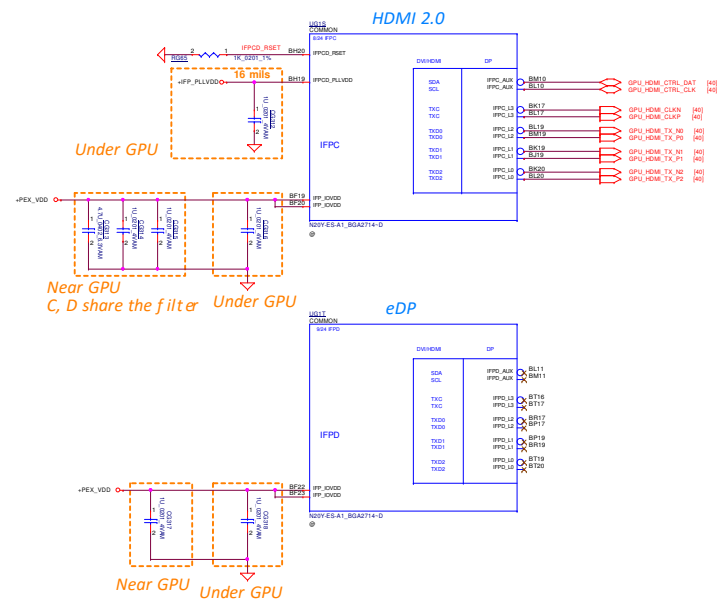
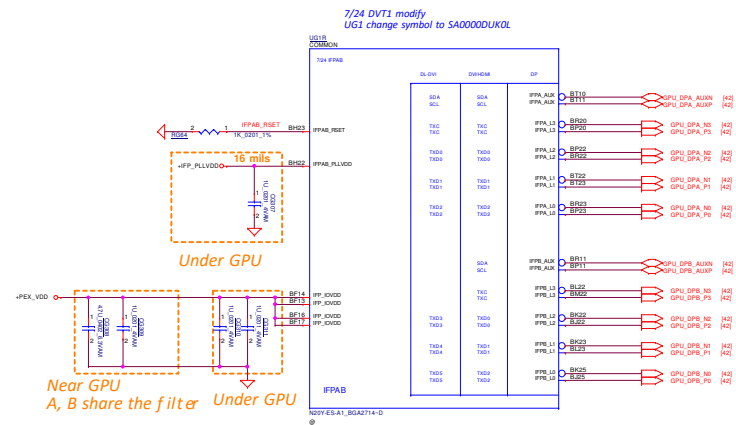
| 8G bit GDDR6   |   |                 |   |               |   |
|----------------|---|-----------------|---|---------------|---|
| Micron 6GB SKU |   | Samsung 6GB SKU |   | Hynix 6GB SKU |   |
| R1             | R3  | R1              | R3  | R1            | R3  |
|                | <div>UML V8GR3g</div> <div>MT81K256M32JE-14A1.2V SA0000BN07L</div> <div>UML V8GR3g</div> <div>MT81K256M32JE-14A1.2V SA0000BN07L</div> <div>UMS V8GR3g</div> <div>MT81K256M32JE-14A1.2V SA0000BN07L</div> <div>UMS V8GR3g</div> <div>MT81K256M32JE-14A1.2V SA0000BN07L</div> <div>UMS V8GR3g</div> <div>MT81K256M32JE-14A1.2V SA0000BN07L</div> <div>UMS V8GR3g</div> <div>MT81K256M32JE-14A1.2V SA0000BN07L</div> |                 | <div>ULM V8GR3g</div> <div>K4Z803258BC-HC14 1.2V SA0000CE2EL</div> <div>ULM V8GR3g</div> <div>K4Z803258BC-HC14 1.2V SA0000CE2EL</div> <div>ULM V8GR3g</div> <div>K4Z803258BC-HC14 1.2V SA0000CE2EL</div> <div>ULM V8GR3g</div> <div>K4Z803258BC-HC14 1.2V SA0000CE2EL</div> <div>ULM V8GR3g</div> <div>K4Z803258BC-HC14 1.2V SA0000CE2EL</div> <div>ULM V8GR3g</div> <div>K4Z803258BC-HC14 1.2V SA0000CE2EL</div> |               | <div>ULM V8GR3g</div> <div>H56C8H44AIR-S2C SA0000UW1L</div> <div>ULM V8GR3g</div> <div>H56C8H44AIR-S2C SA0000UW1L</div> <div>ULM V8GR3g</div> <div>H56C8H44AIR-S2C SA0000UW1L</div> <div>ULM V8GR3g</div> <div>H56C8H44AIR-S2C SA0000UW1L</div> <div>ULM V8GR3g</div> <div>H56C8H44AIR-S2C SA0000UW1L</div> <div>ULM V8GR3g</div> <div>H56C8H44AIR-S2C SA0000UW1L</div> |

| 8G bit GDDR6   |   |                 |   |               |   |
|----------------|---|-----------------|---|---------------|---|
| Micron 8GB SKU |   | Samsung 8GB SKU |   | Hynix 8GB SKU |   |
| R1             | R3  | R1              | R3  | R1            | R3  |
|                | <div>UML V8GR3g</div> <div>MT81K256M32JE-14A1.2V SA0000BN07L</div> <div>UML V8GR3g</div> <div>MT81K256M32JE-14A1.2V SA0000BN07L</div> <div>UMS V8GR3g</div> <div>MT81K256M32JE-14A1.2V SA0000BN07L</div> <div>UMS V8GR3g</div> <div>MT81K256M32JE-14A1.2V SA0000BN07L</div> <div>UMS V8GR3g</div> <div>MT81K256M32JE-14A1.2V SA0000BN07L</div> <div>UMS V8GR3g</div> <div>MT81K256M32JE-14A1.2V SA0000BN07L</div> |                 | <div>ULM V8GR3g</div> <div>K4Z803258BC-HC14 1.2V SA0000CE2EL</div> <div>ULM V8GR3g</div> <div>K4Z803258BC-HC14 1.2V SA0000CE2EL</div> <div>ULM V8GR3g</div> <div>K4Z803258BC-HC14 1.2V SA0000CE2EL</div> <div>ULM V8GR3g</div> <div>K4Z803258BC-HC14 1.2V SA0000CE2EL</div> <div>ULM V8GR3g</div> <div>K4Z803258BC-HC14 1.2V SA0000CE2EL</div> <div>ULM V8GR3g</div> <div>K4Z803258BC-HC14 1.2V SA0000CE2EL</div> |               | <div>ULM V8GR3g</div> <div>H56C8H44AIR-S2C SA0000UW1L</div> <div>ULM V8GR3g</div> <div>H56C8H44AIR-S2C SA0000UW1L</div> <div>ULM V8GR3g</div> <div>H56C8H44AIR-S2C SA0000UW1L</div> <div>ULM V8GR3g</div> <div>H56C8H44AIR-S2C SA0000UW1L</div> <div>ULM V8GR3g</div> <div>H56C8H44AIR-S2C SA0000UW1L</div> <div>ULM V8GR3g</div> <div>H56C8H44AIR-S2C SA0000UW1L</div> |

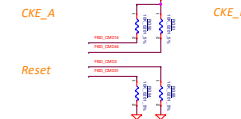
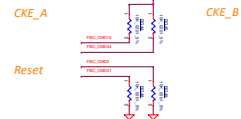
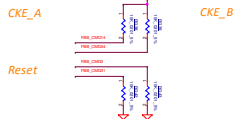
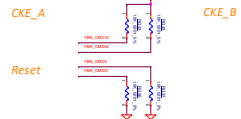
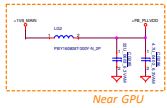
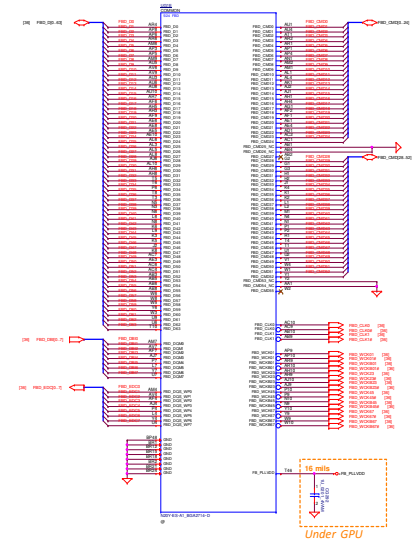
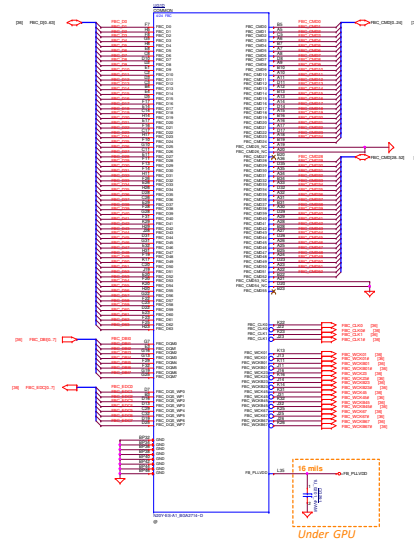
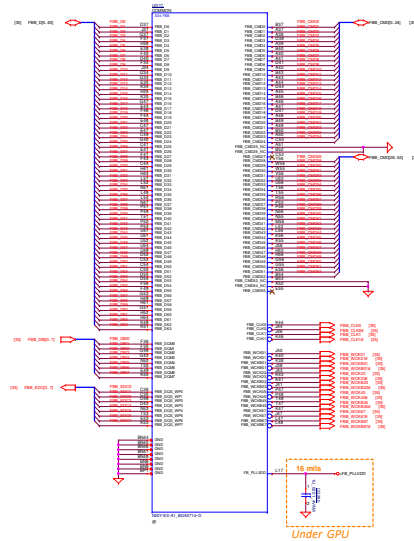
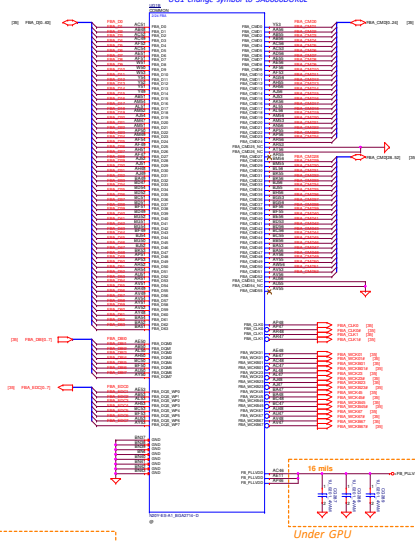
7/25 DVT1 modify  
follow DVT1 proto plan



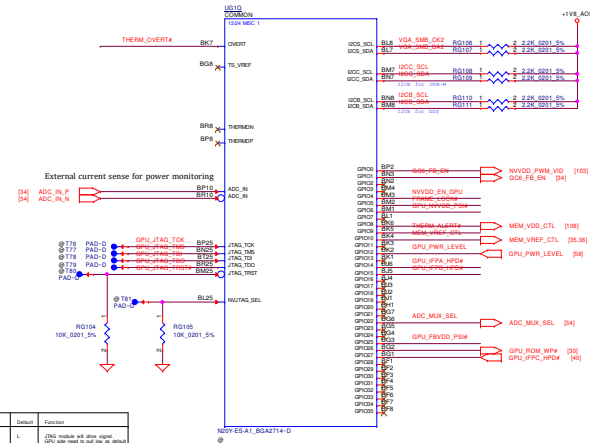




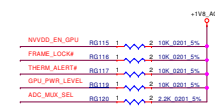
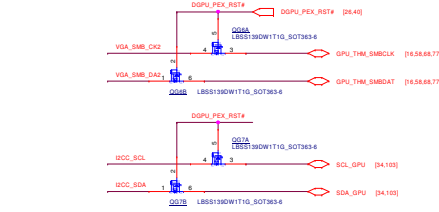
7/24 DVT1 modify  
UG1 change symbol to SA0000DUK0L



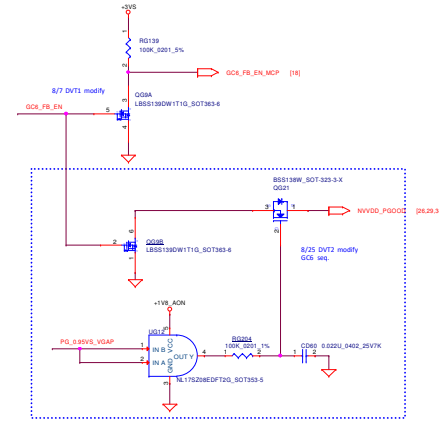
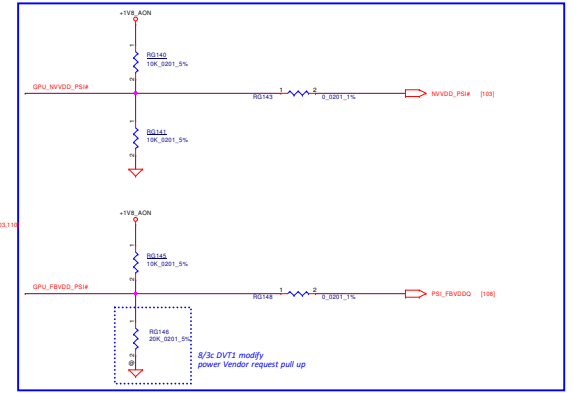
7/24 DVT1 modify  
UG1 change symbol to SA0000DUKOL



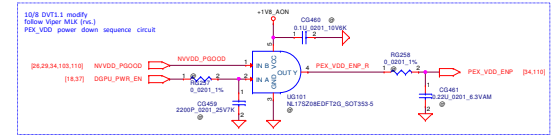
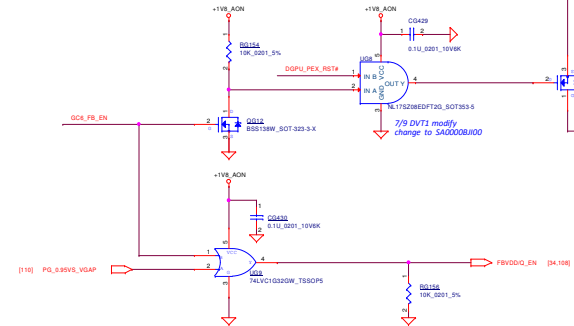
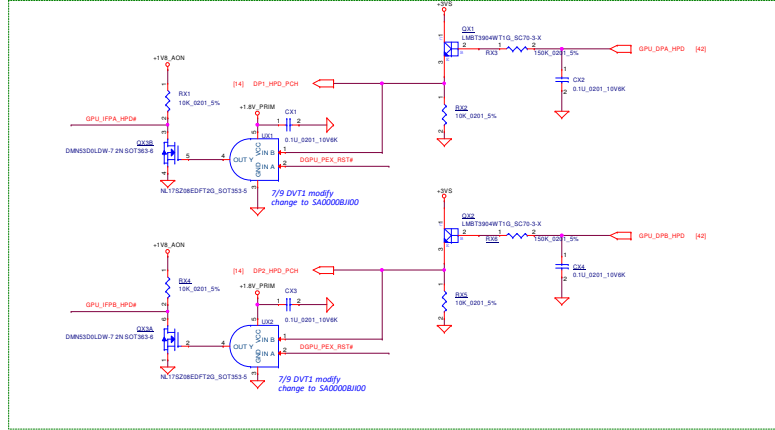
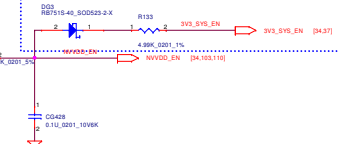
| Part Name | Default             | Function                      |
|-----------|---------------------|-------------------------------|
| JTAG_TCK  | L                   | JTAG module and other signals |
| WDTAG_SEL | L                   | Test Mode -> Disable          |
| W         | Test Mode -> Enable |                               |



GPU to PWR PSI



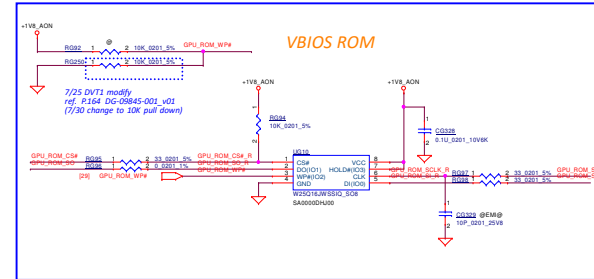
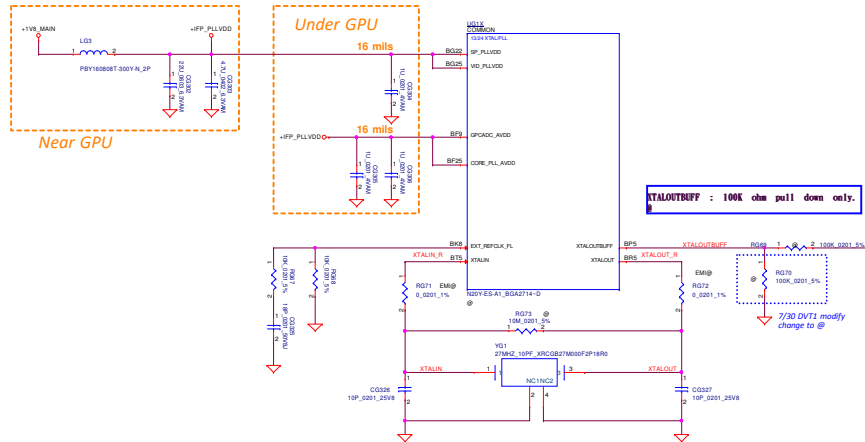
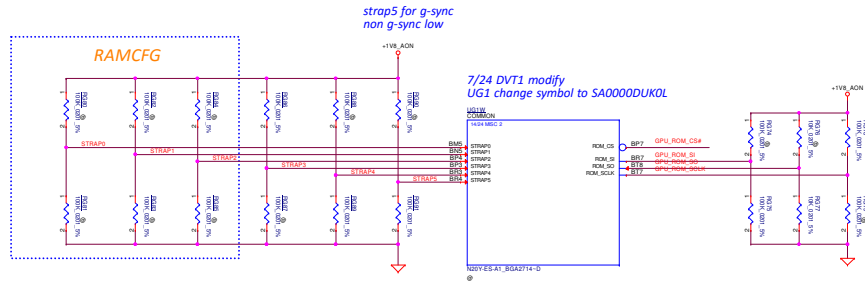
7/25a DVT1 modify  
7/29 DVT1 modify 2.2K 5% change to 1%  
7/23 DVT2 modify  
For 1V8\_MAIN EN to NVVDD\_EN RC delay



|                         |              |                    |            |            |            |
|-------------------------|--------------|--------------------|------------|------------|------------|
| Security Classification | Confidential | Compil Secret Data | 2018/06/07 | 2018/06/07 | 2018/06/07 |
| Issued Date             | 2018/06/07   | Discontinued Date  | 2018/06/07 | 2018/06/07 | 2018/06/07 |
| Rev                     | 1            | Rev                | 1          | Rev        | 1          |
| Rev                     | 1            | Rev                | 1          | Rev        | 1          |
| Rev                     | 1            | Rev                | 1          | Rev        | 1          |

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Compil Electronics, Inc.  
NV(4/8) GPIO  
LA-K661P  
Rev 0.1



| STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE |
|--------|--------|--------|--------------|-----------|----------|------------|
| M      | H      | H      | 1            | 1         | 1        | 1          |
| M      | H      | L      | 1            | 1         | 1        | 0          |
| M      | L      | H      | 1            | 1         | 0        | 1          |
| M      | L      | L      | 1            | 1         | 0        | 0          |
| L      | H      | M      | 1            | 0         | 1        | 1          |
| L      | M      | H      | 1            | 0         | 1        | 0          |
| L      | M      | L      | 1            | 0         | 0        | 1          |
| L      | L      | M      | 1            | 0         | 0        | 0          |
| H      | H      | H      | 0            | 1         | 1        | 1          |
| H      | H      | L      | 0            | 1         | 1        | 0          |
| H      | L      | H      | 0            | 1         | 0        | 1          |
| H      | L      | L      | 0            | 1         | 0        | 0          |
| L      | H      | H      | 0            | 0         | 1        | 1          |
| L      | H      | L      | 0            | 0         | 1        | 0          |
| L      | L      | H      | 0            | 0         | 0        | 1          |
| L      | L      | L      | 0            | 0         | 0        | 0          |

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE

Table 1. GN20-E7 GDDR6 Recommended Memories

| Memory Density | Allowed Memory Configuration | FBVDD/Q           | Vendor  | Manufacturer Part Number | Die Revision | Strap | Memory Speed Grade | Date Code Alert   | Qual Plan | Status               |
|----------------|------------------------------|-------------------|---------|--------------------------|--------------|-------|--------------------|-------------------|-----------|----------------------|
| 16 Gb          | 2Chx32GbMx16                 | 1.35V             | Samsung | K4Z8G32SBC-HC14          | M-die        | 1A    | 14 Gbps            | 20012             | Full      | Production candidate |
|                |                              | 1.25V             | Micron  | TBD                      | TBD          | 1A    | 14 Gbps            | 1940 <sup>1</sup> | Full      | Production candidate |
|                |                              | 1.2V <sup>1</sup> | Hynix   | TBD                      | 1A           | 1A    | 14 Gbps            | 20012             | Full      | Production candidate |
| 8 Gb           | 2Chx25GbMx16                 | 1.35V             | Samsung | K4Z8G25SBC-HC14          | C-die        | 1A    | 14 Gbps            | 20012             | Full      | Production candidate |
|                |                              | 1.25V             | Hynix   | H56C8H24A1R-S2C          | A-die        | 1A    | 14 Gbps            | 1940 <sup>1</sup> | Full      | Production candidate |
|                |                              | 1.2V <sup>1</sup> | Micron  | MT61K25M32JE-14A         | A-die        | 1A    | 14 Gbps            | 1940 <sup>1</sup> | Full      | Production candidate |

Notes:  
<sup>1</sup> Refer to GN20-E GeForce Product Spec for memory voltages and clocks.  
<sup>2</sup> Before the date code is available, the specially screened for 11 Gbps @ 1.2V support Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.  
<sup>3</sup> Before the date code is available, the specially screened for 11 Gbps @ 1.2V support Hynix memory is identified by "HPL" letters inserted before the seven digits in its lot ID.  
<sup>4</sup> For GN20-E7, the maximum allowable memory case temperature is 95 °C.

Table 3. GN20-E3 GDDR6 Recommended Memories

| Memory Density | Allowed Memory Configuration | FBVDD/Q           | Vendor  | Manufacturer Part Number | Die Revision | Strap | Memory Speed Grade | Date Code Alert   | Qual Plan | Status               |
|----------------|------------------------------|-------------------|---------|--------------------------|--------------|-------|--------------------|-------------------|-----------|----------------------|
| 8 Gb           | 2Chx25GbMx16                 | 1.35V             | Samsung | K4Z8G25SBC-HC14          | C-die        | 1A    | 14 Gbps            | 20012             | Full      | Production candidate |
|                |                              | 1.25V             | Hynix   | H56C8H24A1R-S2C          | A-die        | 1A    | 14 Gbps            | 1940 <sup>1</sup> | Full      | Production candidate |
|                |                              | 1.2V <sup>1</sup> | Micron  | MT61K25M32JE-14A         | A-die        | 1A    | 14 Gbps            | 1940 <sup>1</sup> | Full      | Production candidate |

Notes:  
<sup>1</sup> Refer to GN20-E GeForce Product Spec for memory voltages and clocks.  
<sup>2</sup> Before the date code is available, the specially screened for 11 Gbps @ 1.2V support Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.  
<sup>3</sup> Before the date code is available, the specially screened for 11 Gbps @ 1.2V support Hynix memory is identified by "HPL" letters inserted before the seven digits in its lot ID.  
<sup>4</sup> For GN20-E3, the maximum allowable memory case temperature is 95 °C.

Table 2. GN20-E5/E4 GDDR6 Recommended Memories

| Memory Density | Allowed Memory Configuration | FBVDD/Q           | Vendor  | Manufacturer Part Number | Die Revision | Strap | Memory Speed Grade | Date Code Alert   | Qual Plan | Status               |
|----------------|------------------------------|-------------------|---------|--------------------------|--------------|-------|--------------------|-------------------|-----------|----------------------|
| 8 Gb           | 2Chx25GbMx16                 | 1.35V             | Samsung | K4Z8G25SBC-HC14          | C-die        | 1A    | 14 Gbps            | 20012             | Full      | Production candidate |
|                |                              | 1.25V             | Hynix   | H56C8H24A1R-S2C          | A-die        | 1A    | 14 Gbps            | 1940 <sup>1</sup> | Full      | Production candidate |
|                |                              | 1.2V <sup>1</sup> | Micron  | MT61K25M32JE-14A         | A-die        | 1A    | 14 Gbps            | 1940 <sup>1</sup> | Full      | Production candidate |

Notes:  
<sup>1</sup> Refer to GN20-E GeForce Product Spec for memory voltages and clocks.  
<sup>2</sup> Before the date code is available, the specially screened for 11 Gbps @ 1.2V support Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.  
<sup>3</sup> Before the date code is available, the specially screened for 11 Gbps @ 1.2V support Hynix memory is identified by "HPL" letters inserted before the seven digits in its lot ID.  
<sup>4</sup> For GN20-E5/E4, the maximum allowable memory case temperature is 95 °C.

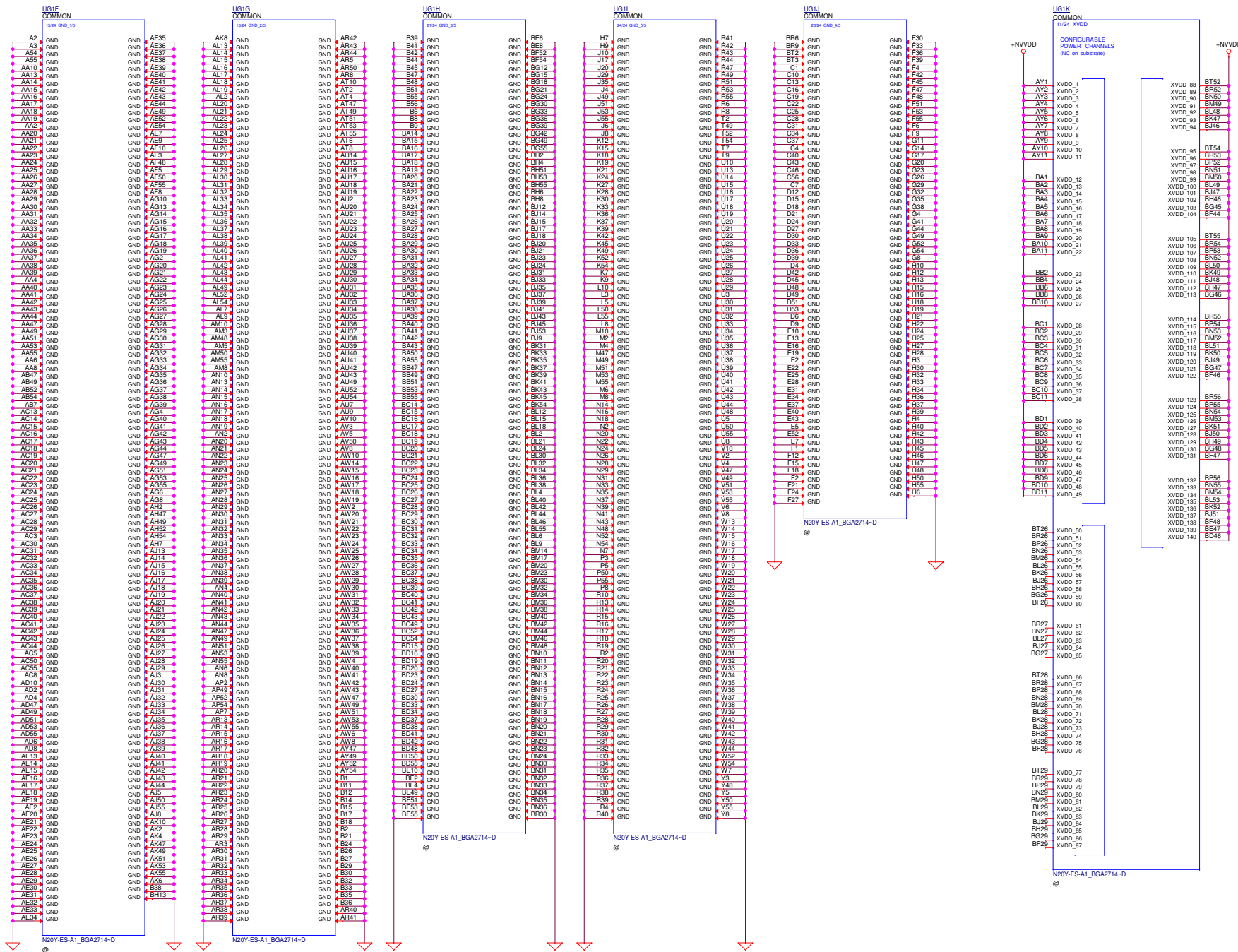
Table 9.3 RAMCFG

| Strap Pins | Strap2 | Strap1 | Strap0 | RAMCFG Setting Number |
|------------|--------|--------|--------|-----------------------|
| L          | L      | L      | L      | 0 (0x0000)            |
| L          | L      | L      | H      | 1 (0x0001)            |
| L          | L      | H      | L      | 2 (0x0002)            |
| L          | L      | H      | H      | 3 (0x0003)            |
| H          | L      | L      | L      | 4 (0x0004)            |
| H          | L      | L      | H      | 5 (0x0005)            |
| H          | L      | H      | L      | 6 (0x0006)            |
| H          | L      | H      | H      | 7 (0x0007)            |
| L          | M      | L      | M      | 8 (0x0008)            |
| L          | M      | L      | H      | 9 (0x0009)            |
| L          | M      | H      | L      | 10 (0x000A)           |
| L          | M      | H      | H      | 11 (0x000B)           |
| M          | L      | L      | L      | 12 (0x000C)           |
| M          | L      | L      | H      | 13 (0x000D)           |
| M          | L      | H      | L      | 14 (0x000E)           |
| M          | L      | H      | H      | 15 (0x000F)           |

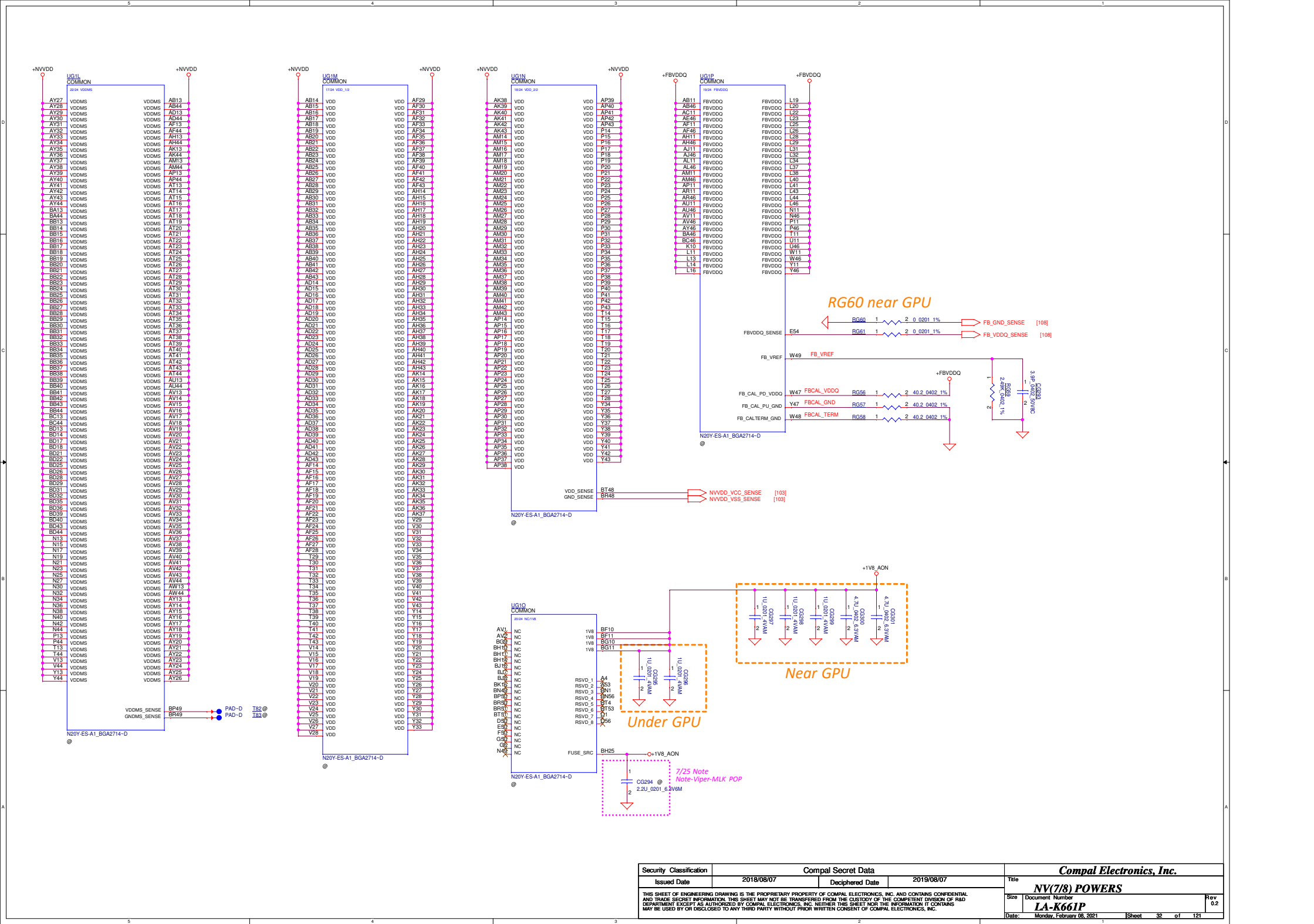
Table 9.3 RAMCFG

| Strap Pins | Strap2 | Strap1 | Strap0 | RAMCFG Setting Number |
|------------|--------|--------|--------|-----------------------|
| M          | L      | M      | M      | 16 (0x0010)           |
| M          | M      | L      | M      | 17 (0x0011)           |
| M          | M      | L      | H      | 18 (0x0012)           |
| M          | M      | H      | M      | 19 (0x0013)           |
| L          | M      | M      | M      | 20 (0x0014)           |
| M          | L      | M      | M      | 21 (0x0015)           |
| M          | M      | L      | L      | 22 (0x0016)           |
| M          | M      | L      | H      | 23 (0x0017)           |
| M          | M      | H      | M      | 24 (0x0018)           |
| M          | M      | H      | H      | 25 (0x0019)           |
| M          | M      | M      | M      | 26 (0x001A)           |

7/24 DVT1 modify  
UG1 change symbol to SA0000DUKOL



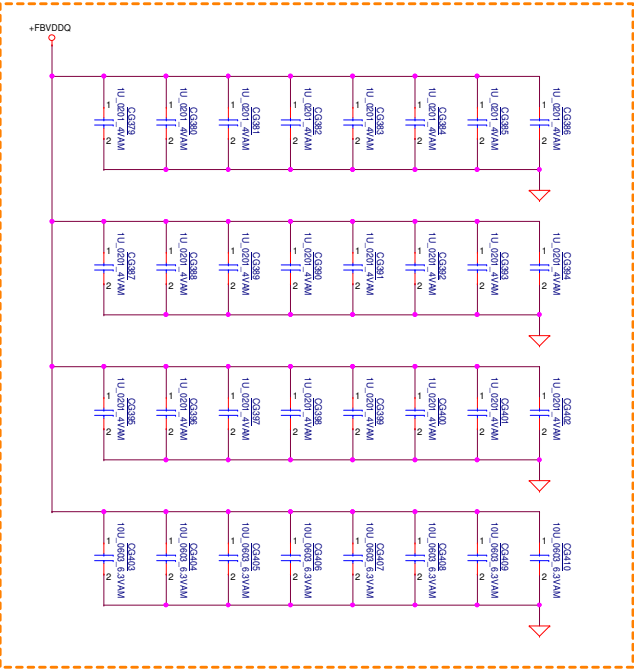




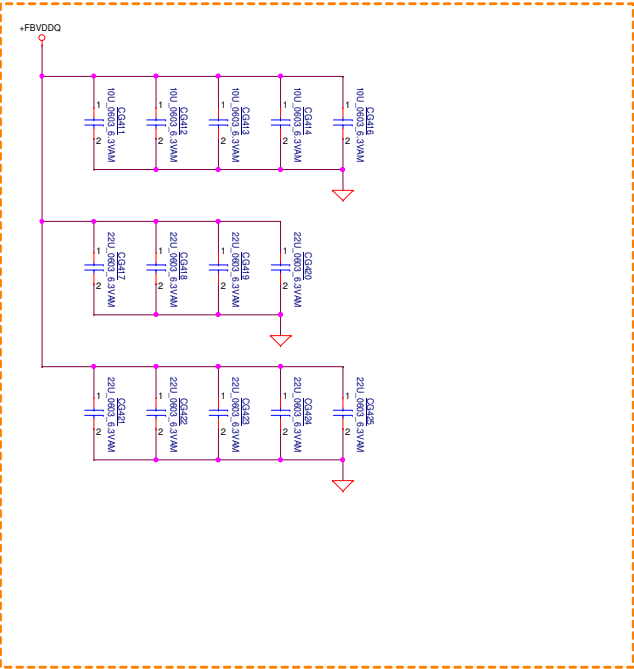


FBVDDQ\_GPU

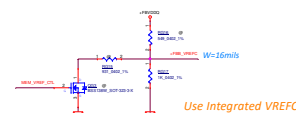
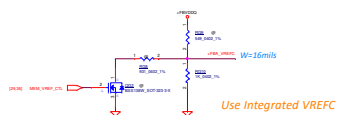
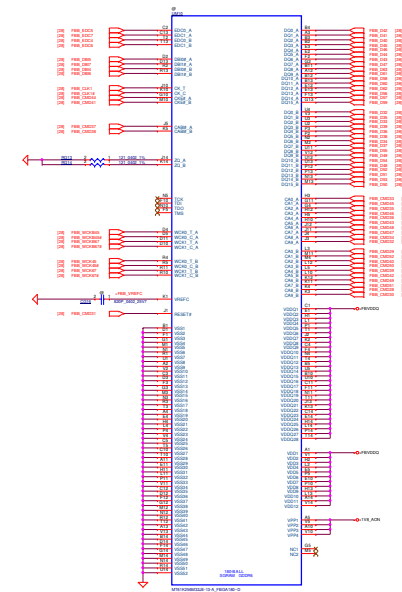
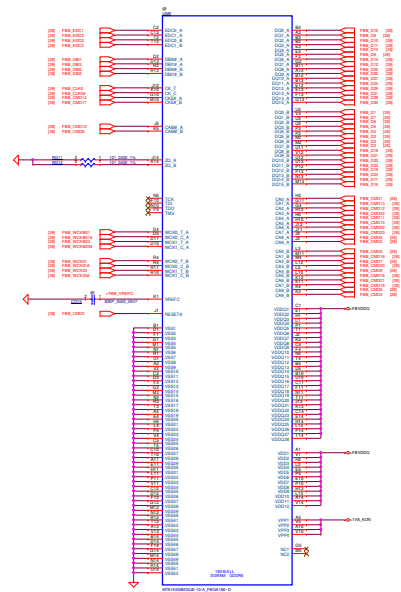
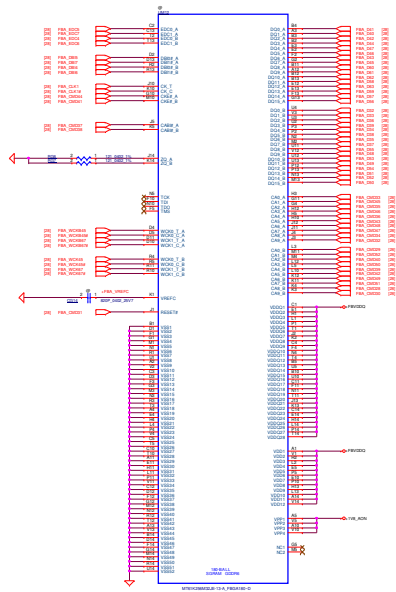
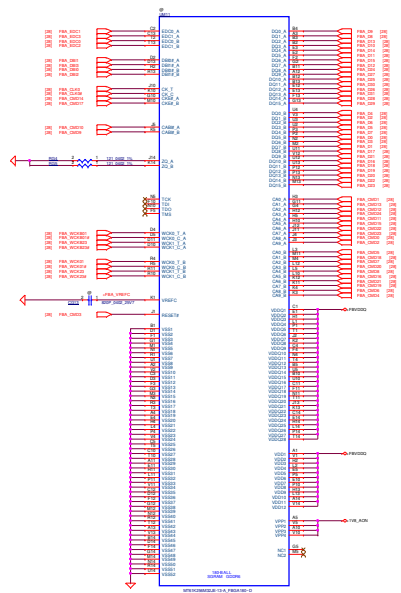
Under GPU



Near GPU





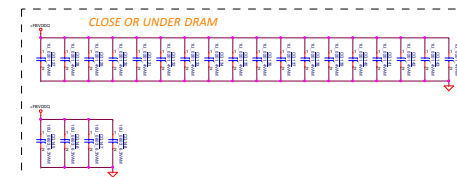
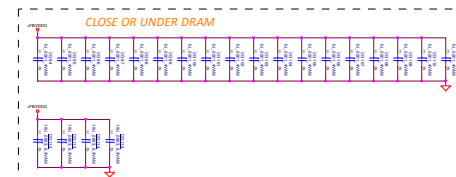
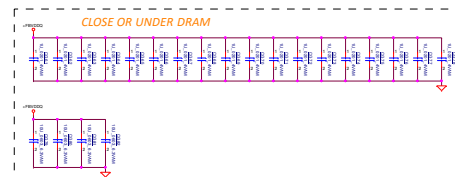
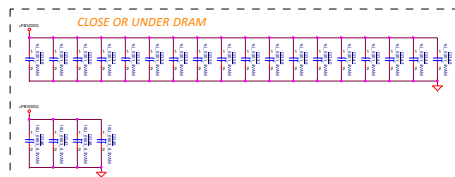
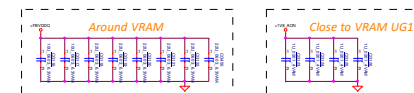
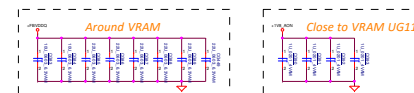
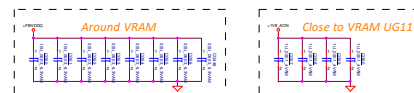
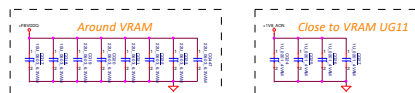


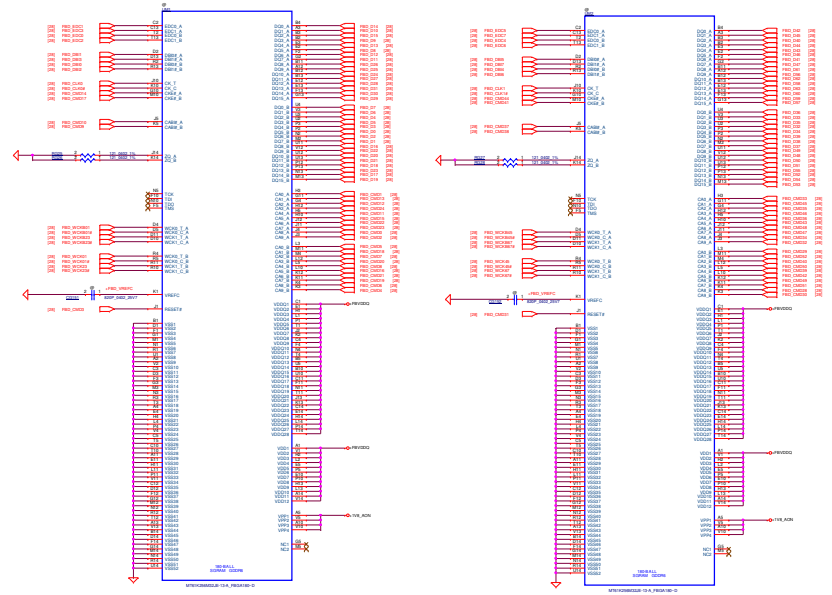
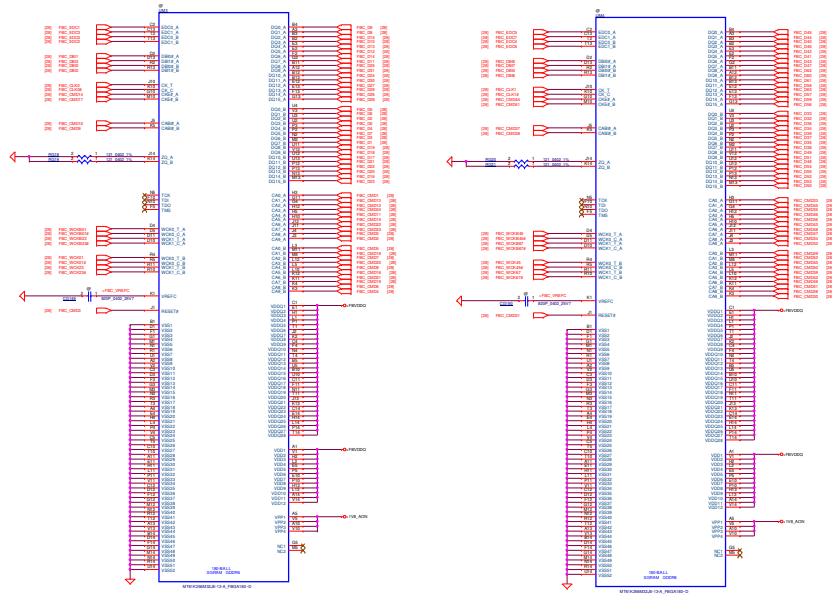
UM11

UM12

UM9

UM10



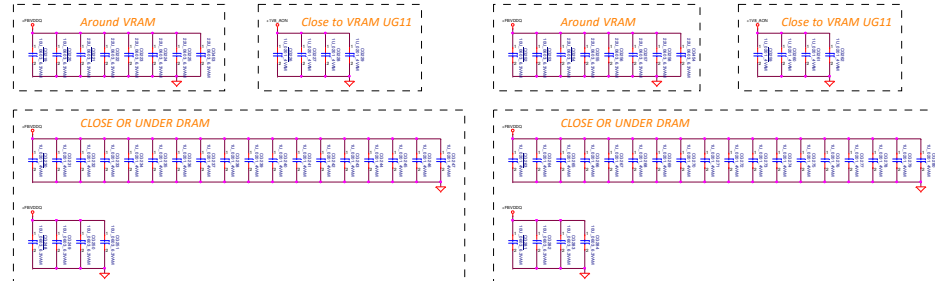
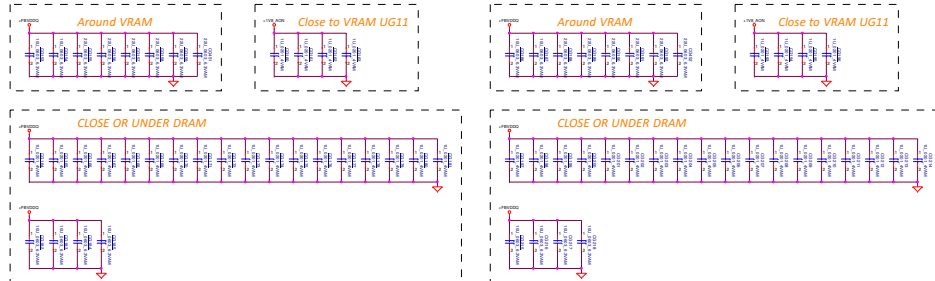


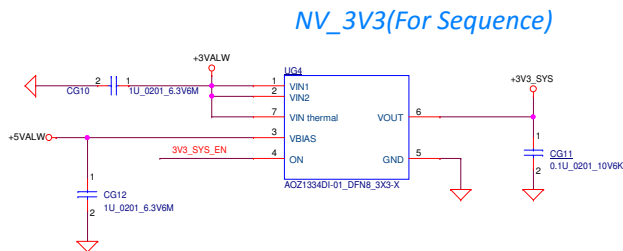
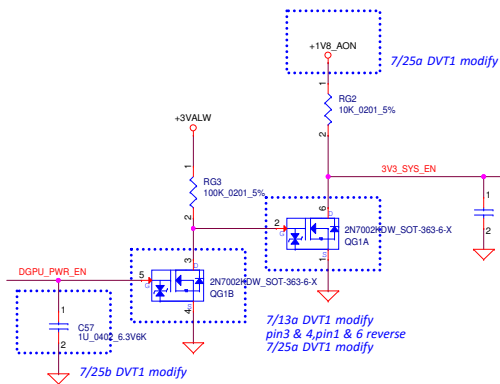
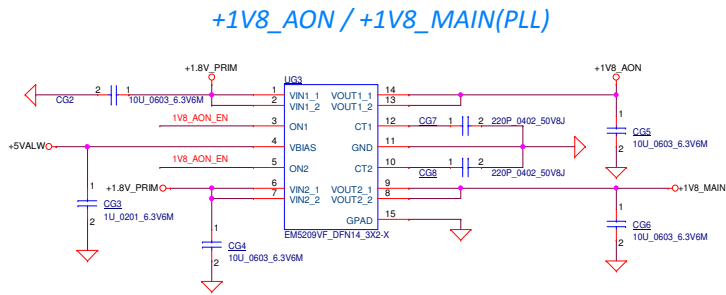
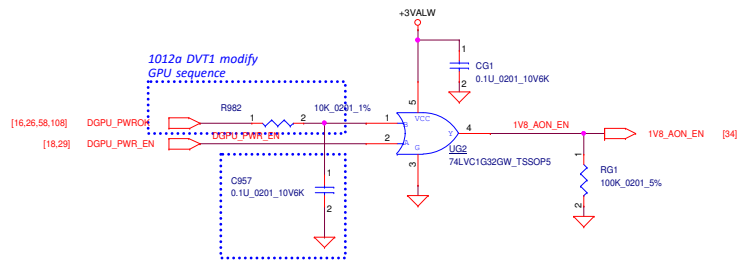
UM3

UM4

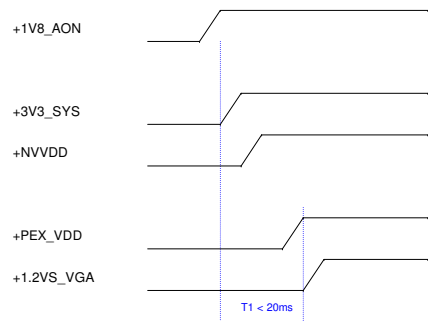
UM1

UM2



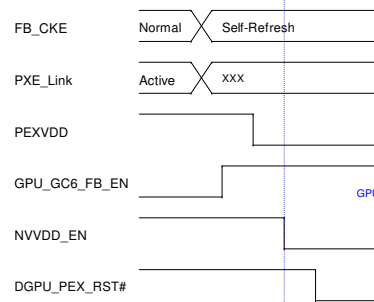


## GPU Power Up Sequence



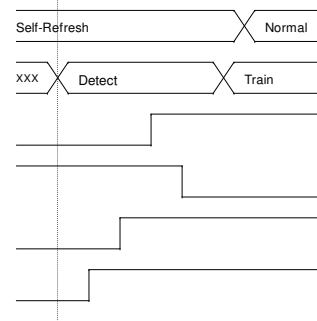
The ramp time for any rail must be more than 40us and less than 2ms.

## GPU GC6 Entry Sequence

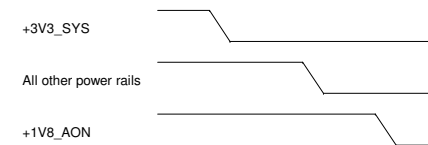


The entire entry/exit sequence must complete within 200 ms.

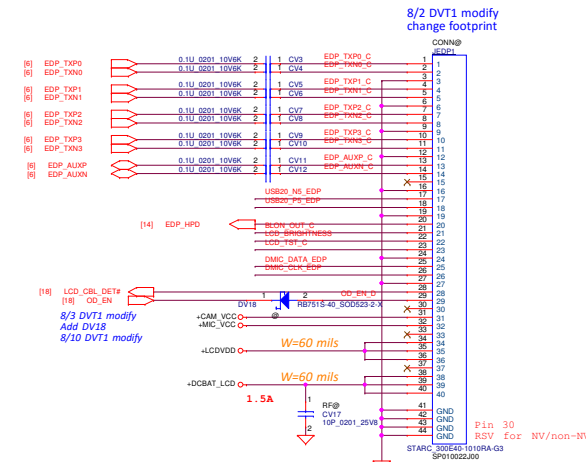
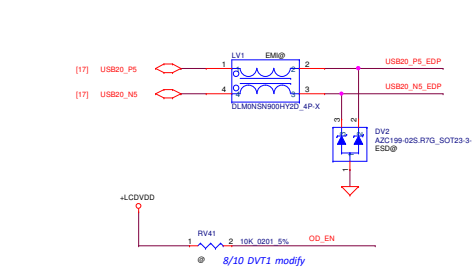
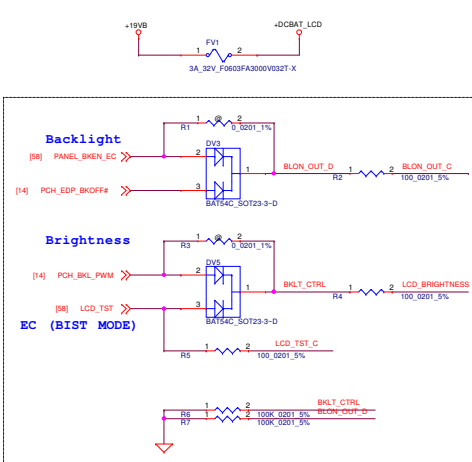
## GPU GC6 Exit Sequence



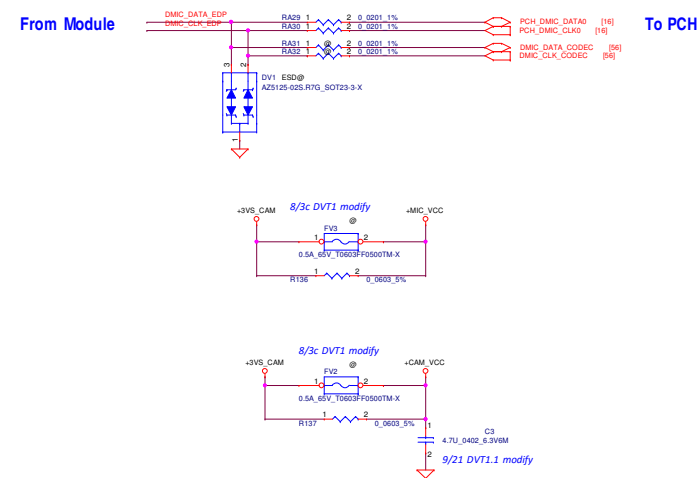
## GPU Power Down Sequence



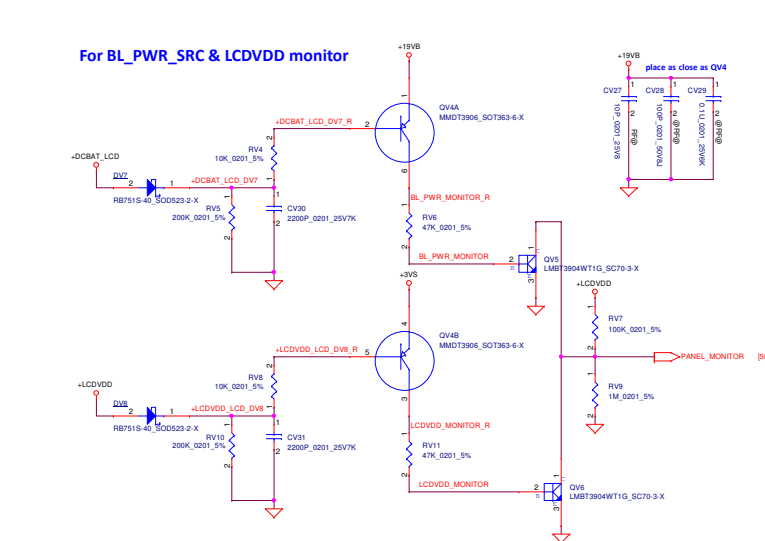
Main Func = LCD



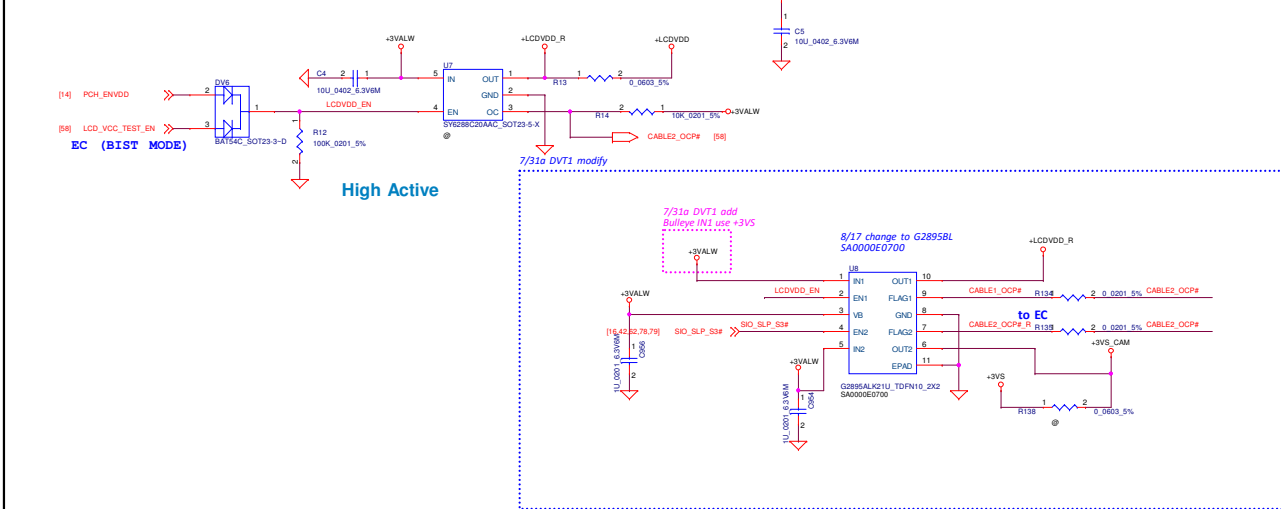
Main Func = DMIC



Main Func = LCDVDD monitor



Main Func = Hinge up protection



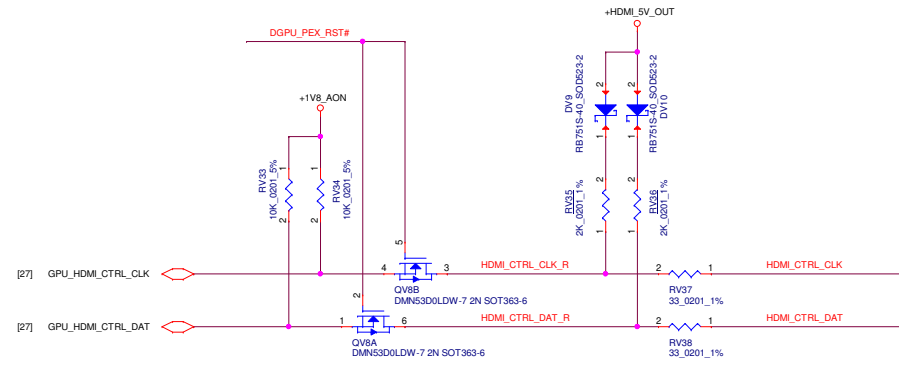
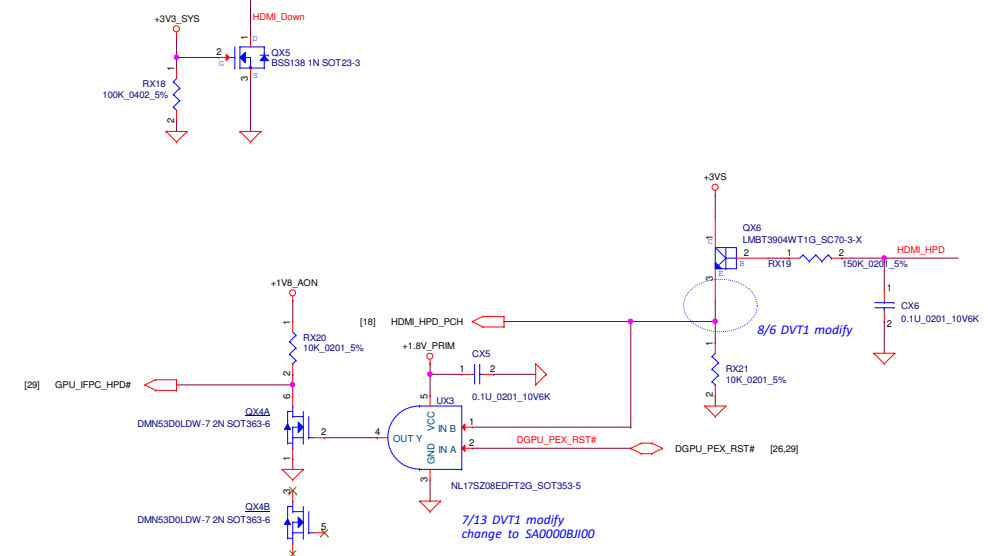
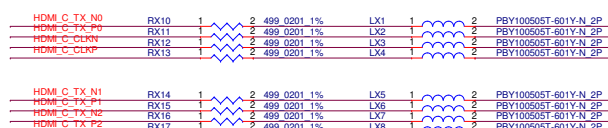
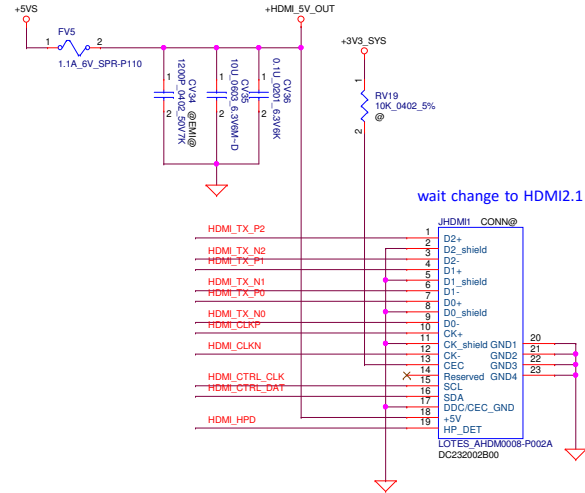
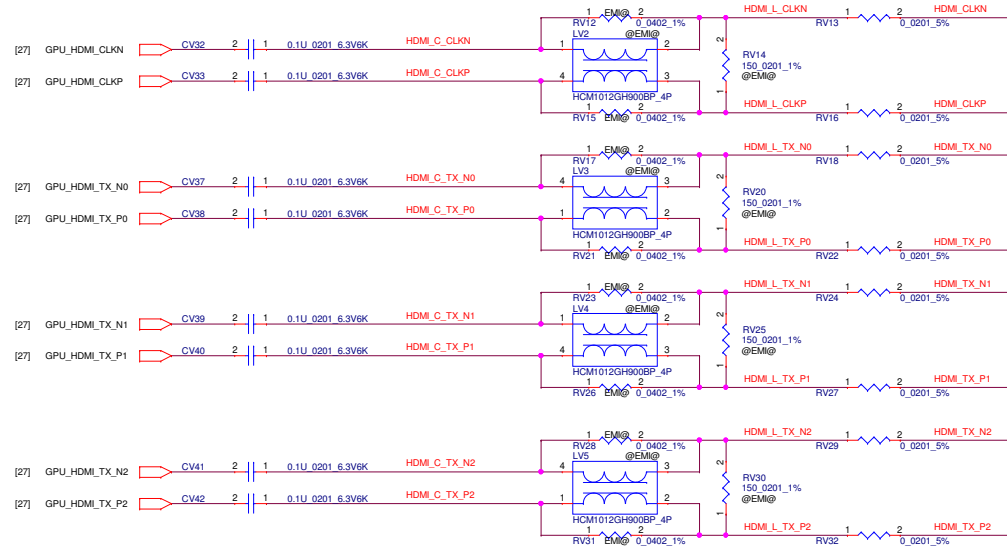
|  |          |                    |          |       |                           |
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| Issued Date  | 20200305 | Deciphered Date    | 20180205 | Size  | 1A-K661P                  |
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|  |          |                    |          |       | 0.2                       |
|  |          |                    |          |       | Date                      |
|  |          |                    |          |       | Monday, February 28, 2021 |
|  |          |                    |          |       | Sheet                     |
|  |          |                    |          |       | 38 of 121                 |

Main Func = DDS

Main Func = eDP MUX

|                           |  |                    |  |             |  |
|---------------------------|--|--------------------|--|-------------|--|
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| Issued Date               |  | Deciphered Date    |  | Rev         |  |
| 2020/03/05                |  | 2019/04/01         |  | eDP MUX/DDS |  |
| Rev                       |  | Documnt            |  | Rev         |  |
| LA-R661P                  |  | Rev                |  | Rev         |  |
| Date                      |  | Date               |  | Date        |  |
| Monday, February 05, 2021 |  | Sheet              |  | 38 of 121   |  |

12/21 DVT2 modify  
change to 0 ohm



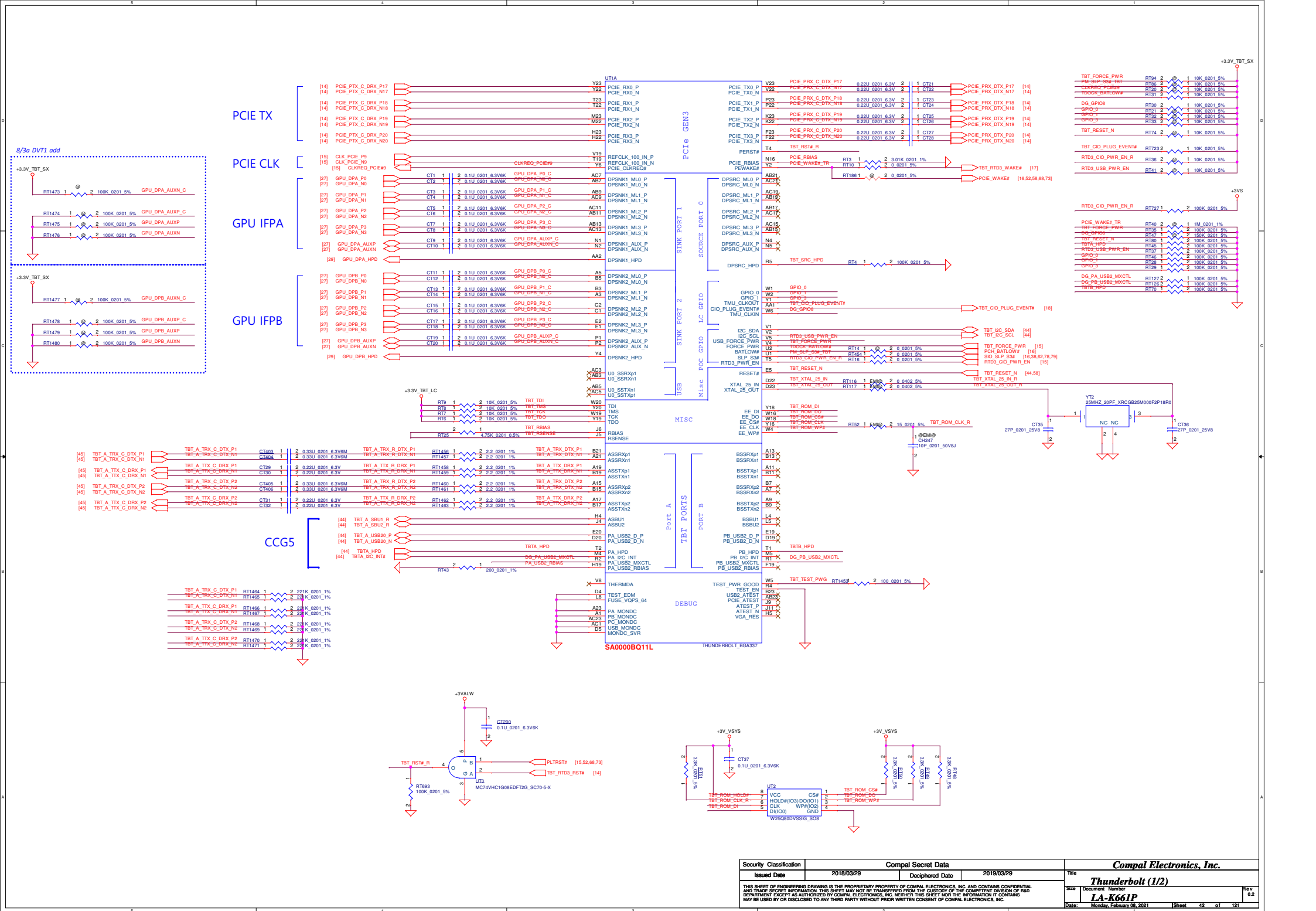
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| Security Classification |  | Compal Secret Data |  | Title                           |  |
| Issued Date             |  | Deciphered Date    |  | HDMI                            |  |
| 2020/03/05              |  | 2018/02/05         |  | Document Number                 |  |
|                         |  |                    |  | LA-K661P                        |  |
|                         |  |                    |  | Rev 0.2                         |  |
|                         |  |                    |  | Date: Monday, February 08, 2021 |  |
|                         |  |                    |  | Sheet 40 of 121                 |  |

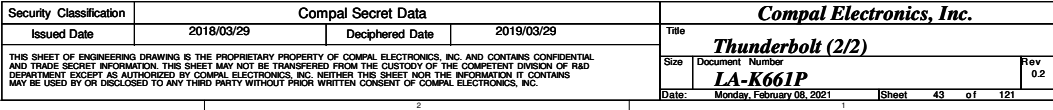


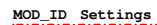
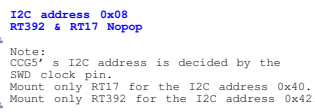
Main Function:

Reserve

|  |                    |                 |            |                          |                           |                 |
|--|--------------------|-----------------|------------|--------------------------|---------------------------|-----------------|
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|  |                    |                 |            |                          | LA-K661P                  | 0.2             |
|  |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 41 of 121 |







| MUX         | Mux MOD_ID Settings |         |   |
|-------------|---------------------|---------|---|
|             | MOD_ID1             | MOD_ID2 | Description   |
| Titan Ridge | L1                  | N/A     | TBT Configuration                                     |
| PS8B02      | L4                  | L0      | PS8B02 Equalizer config #1                            |
| PS8B02      | L4                  | L1 - L3 | Reserved for PS8B02 Equalizer config #2,3,4 reserved  |
| ANX7443     | L5                  | L0      | ANX7443 Equalizer config #1                           |
| ANX7443     | L5                  | L1 - L3 | Reserved for ANX7443 Equalizer config #2,3,4 reserved |
| TUSB546     | L6                  | L0      | TUSB546 Equalizer config #1                           |
| TUSB546     | L6                  | L1 - L3 | Reserved for TUSB546 Equalizer config #2,3,4 reserved |
| TUSB544     | L6                  | L4      | TUSB544 Equalizer config #1                           |
| TUSB544     | L6                  | L5 - L7 | Reserved for TUSB544 Equalizer config #2,3,4 reserved |



Main Function:

# Reserve

|   |                    |                 |            |                          |                           |                 |
|---|--------------------|-----------------|------------|--------------------------|---------------------------|-----------------|
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Main Function:

Reserve

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Main Function:

Reserve

|  |                    |                 |            |                          |                           |                 |
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|  |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 48 of 121 |



Main Function:

# Reserve

|   |                    |                 |            |                          |                           |                 |
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|   |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 49 of 121 |

Main Function:

Reserve

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|  |                    |                 |            |                          | LA-K661P                  | 0.2             |
|  |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 50 of 121 |

Main Function:

Reserve

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|  |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 51 of 121 |



Main Function:

Reserve

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|   |                    |                 |            |                          | LA-K661P                  | 0.2             |
|   |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 53 of 121 |

Main Function:

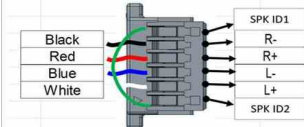
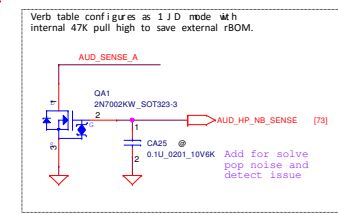
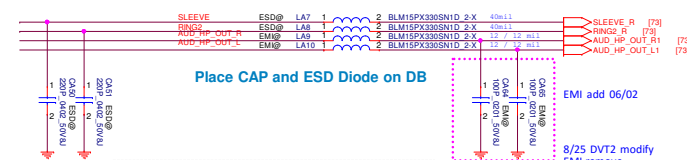
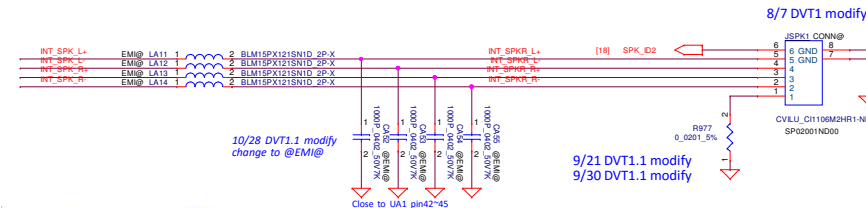
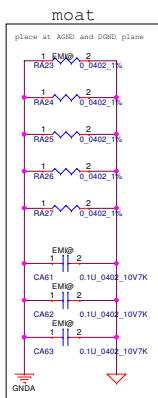
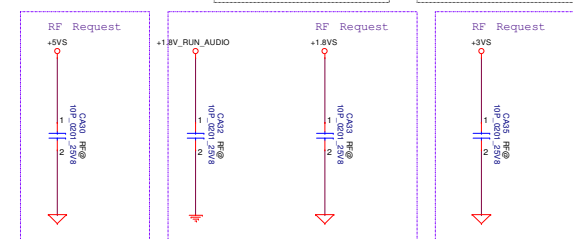
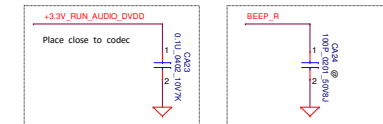
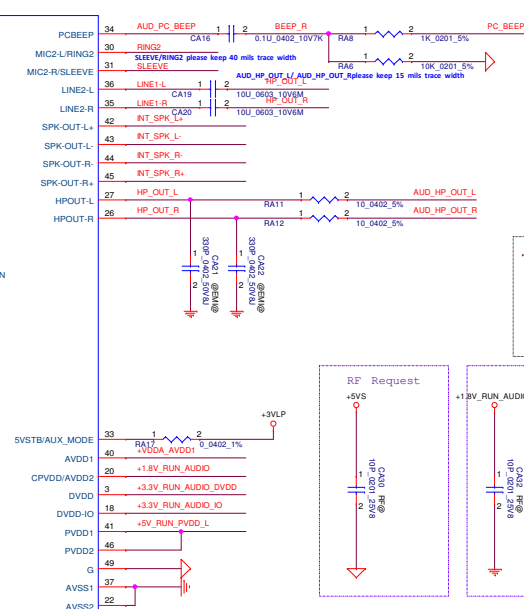
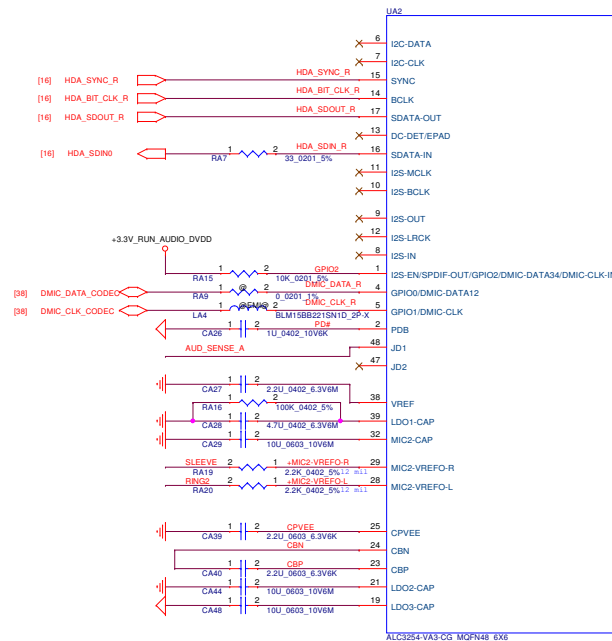
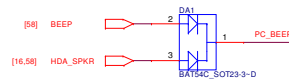
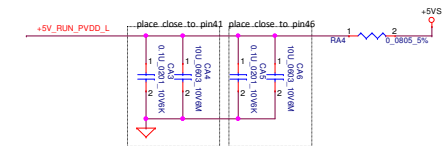
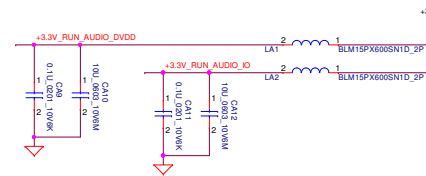
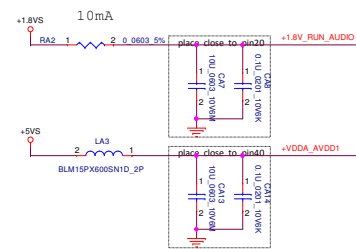
Reserve

|   |                    |                 |            |                          |                           |                 |
|---|--------------------|-----------------|------------|--------------------------|---------------------------|-----------------|
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|   |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 54 of 121 |

Main Function:

Reserve

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|   |                    |                 |            |                          | LA-K661P                  | 0.2             |
|   |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 55 of 121 |



|                   | GPP_C8 (SPK_ID1) | GPP_C9 (SPK_ID2) |
|-------------------|------------------|------------------|
| main source SPK   | 0 (low)          | 0 (low)          |
| second source SPK | 0 (low)          | 1 (high)         |

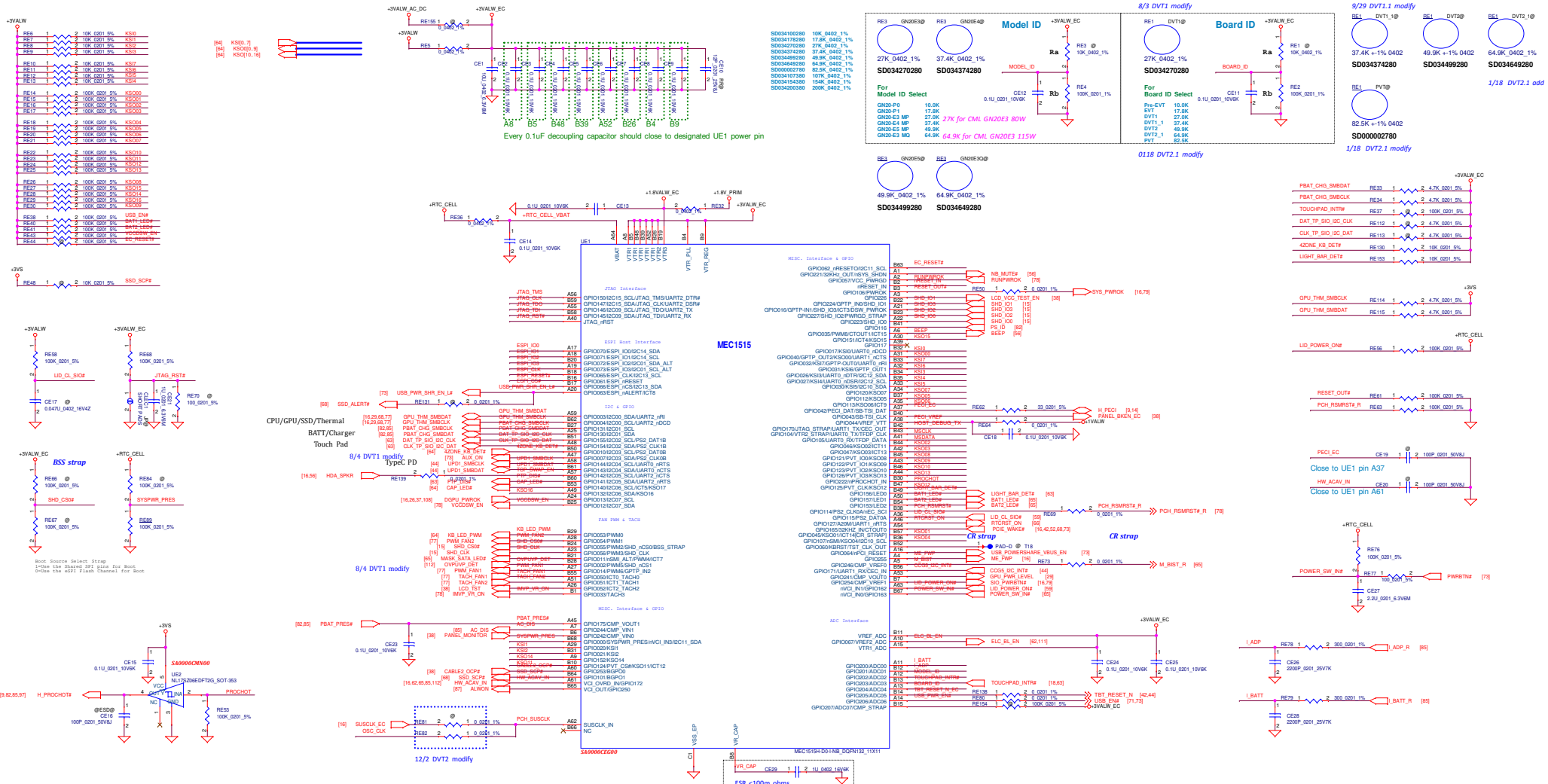
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| Issued Date   | 2020/03/05 | Deciphered Date    | 2018/10/01 | Title                    | Audio Codec ALC3254 |
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|   |            |                    |            |                          | LA-K661P            |
| Date:   | LA-K661P   | Rev                | 0.2        |                          |                     |



Main Function:

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|   |                    |                 |            |                          | LA-K661P                  | 0.2             |
|   |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 57 of 121 |

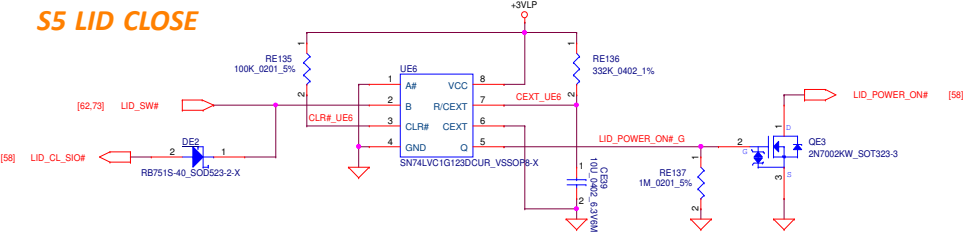
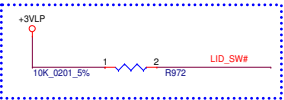


| Pin Name        | Strap Name  | Strap define and value  | IO Power rail |
|-----------------|-------------|---|---------------|
| GPIO170         | JTAG_STRAP  | 1=Use the JTAG Strap Controller for Boundary Scan<br>0=Use the JTAG Tap Controller is used for debug (normal operation)   | VTR1          |
| GPIO104         | VRT2_STRAP  | Strap Level Sense is used to determine if the Shared Flash interface must be configured for 3.3V or 1.8V operation<br>1=3.3V Operation<br>0=1.8V Operation  | VTR1          |
| GPIO405         | CR_STRAP    | Crisis Recovery Strap<br>1=Normal Boot Source<br>0=Use the Private SPI pins to boot from Crisis Recovery flash over Raytheon connector<br>Note: This pin requires an external pull-up for normal operation. | VTR1          |
| GPIO207         | CMP_STRAP   | CMP_STRAP is the Comparator 0 strap pin. This strap must be enabled in EFUSE<br>0=Hardware Default (GPIO input)<br>1=Comparator 0 Enabled   | VTR1          |
| GPIO055/SHD_CS0 | BSS_STRAP_1 | Boot Source Select Strap<br>1=Use the Shared SPI pins for Boot<br>0=Use the SPI Flash Channel for Boot  | VTR2          |
| GPIO227/SHD_CS0 | PWRGD_STRAP | Primary Power rails good<br>1 = Primary power rails are good<br>0 = Primary power rails not stable  | VTR2          |

FUNCTION TABLE

| INPUTS |           |   | OUTPUTS          |
|--------|-----------|---|------------------|
| CLR    | $\bar{A}$ | B | Q                |
| L      | X         | X | L                |
| X      | H         | X | L <sup>(1)</sup> |
| X      | X         | L | L <sup>(1)</sup> |
| H      | L         | ↑ |                  |
| H      | ↓         | H |                  |
| ↑      | L         | H |                  |

9/7 DVT2 modify



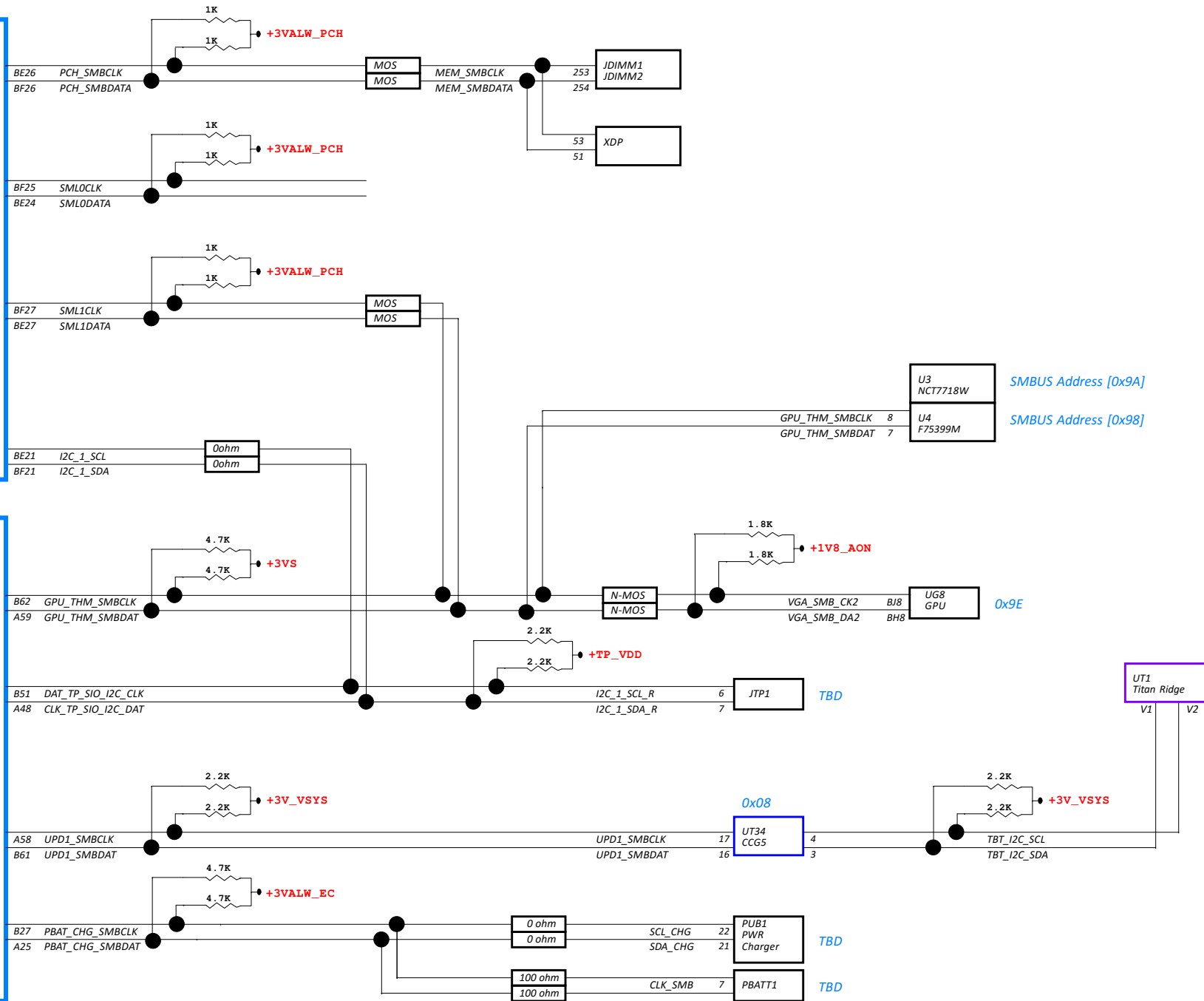
Main Function:

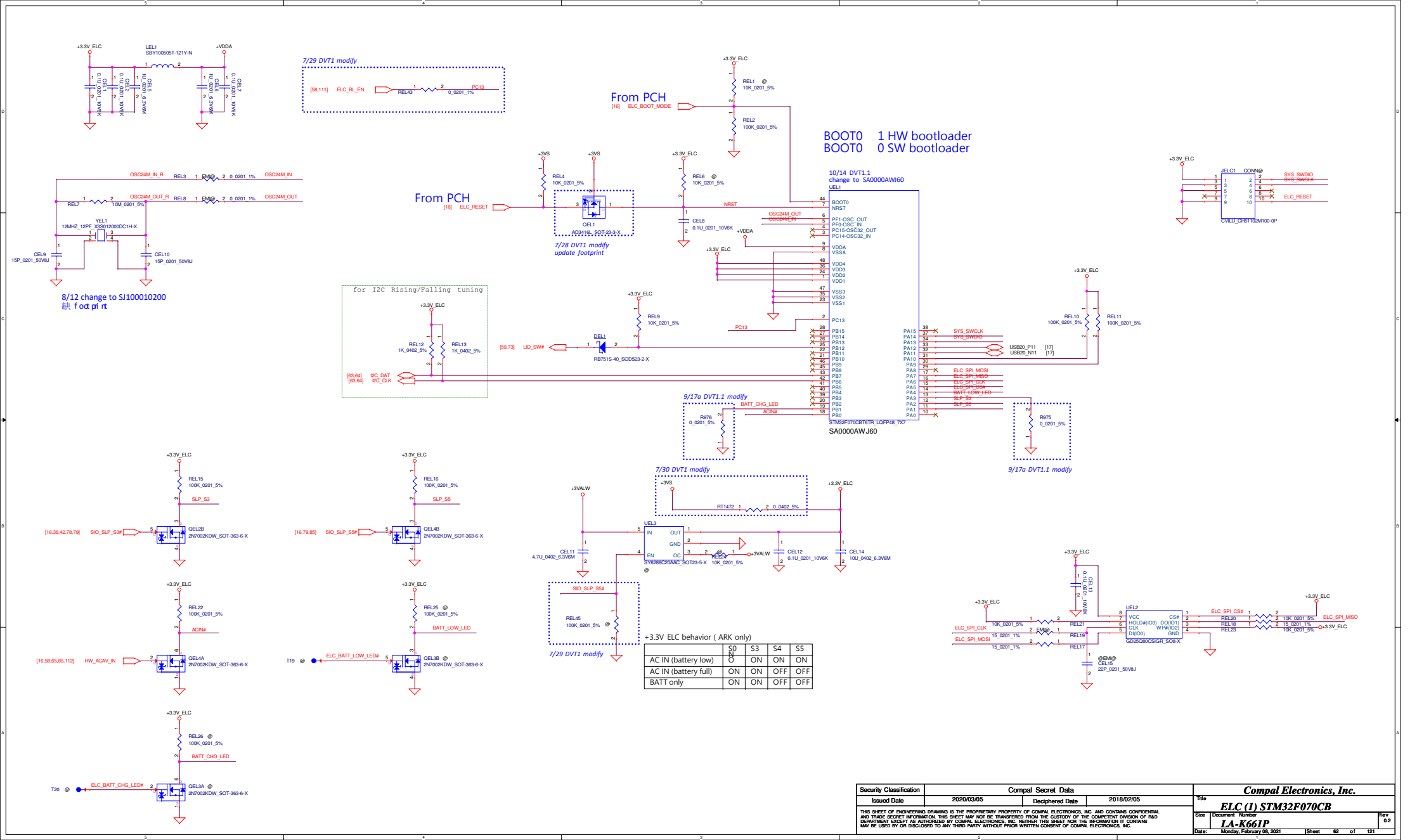
# Reserve

|   |                    |                 |            |                          |                           |                 |
|---|--------------------|-----------------|------------|--------------------------|---------------------------|-----------------|
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|   |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 60 of 121 |

Comet Lake  
PCH-H

MEC1515





Main Func = ELC

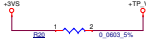
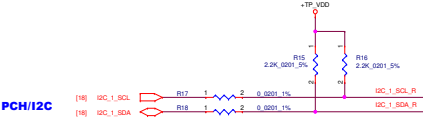
Main Func = Power LED

Main Func = ON/OFF TRON



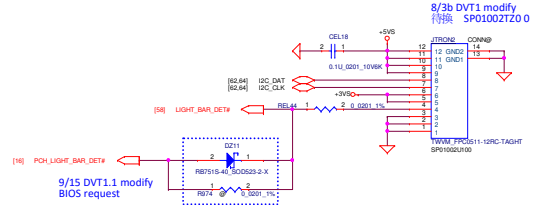
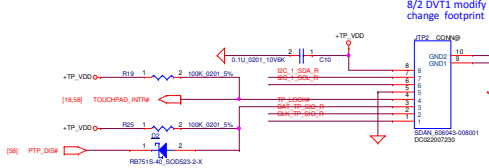
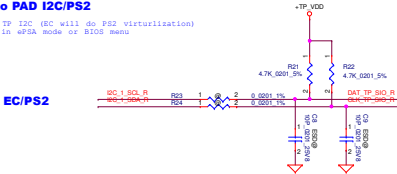
Main Func = Touch pad

**Main Func = Primax Front Lighting**



## Co-lay EC to PAD I2C/PS2

it's used for TP I2C (EC will do PS2 virturalization)  
as control it in ePSA mode or BIOS menu



|   |                    |                 |            |                          |                     |                |
|---|--------------------|-----------------|------------|--------------------------|---------------------|----------------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                     |                |
| Issued Date   | 2020/03/05         | Deciphered Date | 2018/02/05 | Title                    | ELC (2) TP/PWR/TRON |                |
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|   |                    |                 |            |                          | LA-K661P            | 0.2            |
|   |                    |                 |            | Date:                    | Mar 10, 2021        | Sheet 3 of 121 |

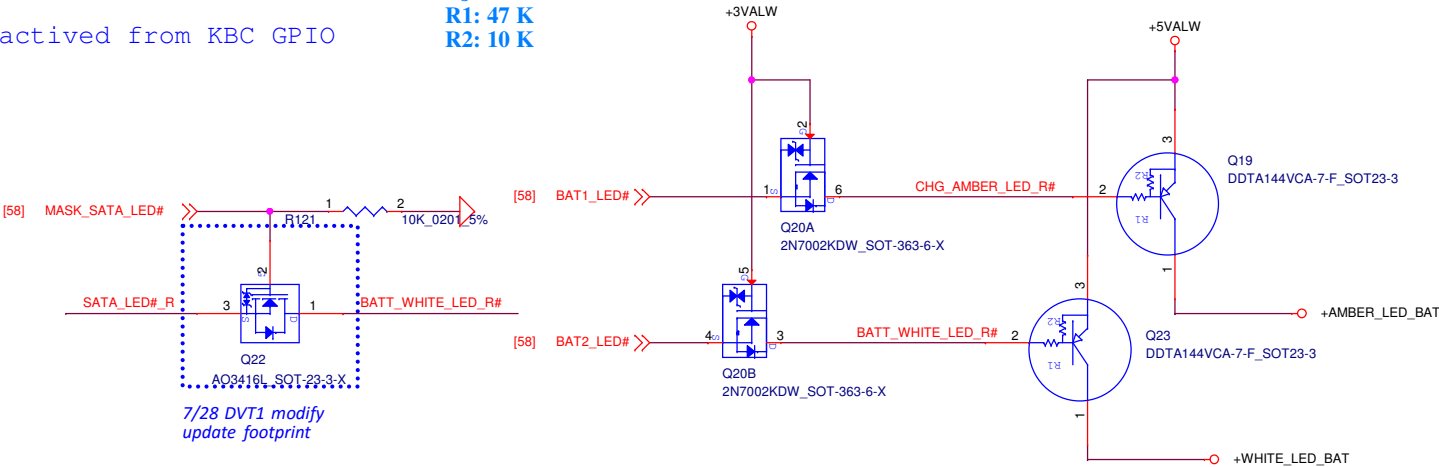




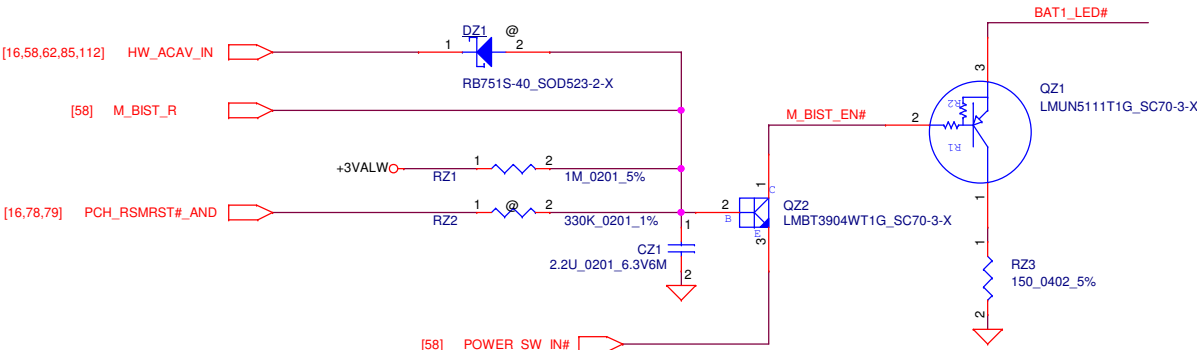
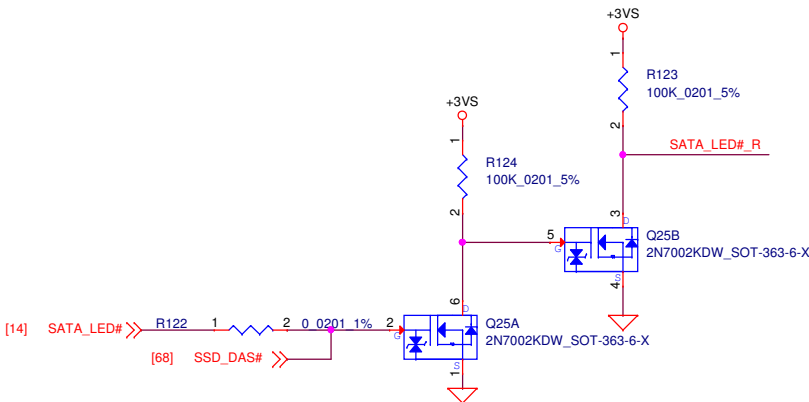
Main Func = Battery LED

Low actived from KBC GPIO

BJT  
R1: 47 K  
R2: 10 K

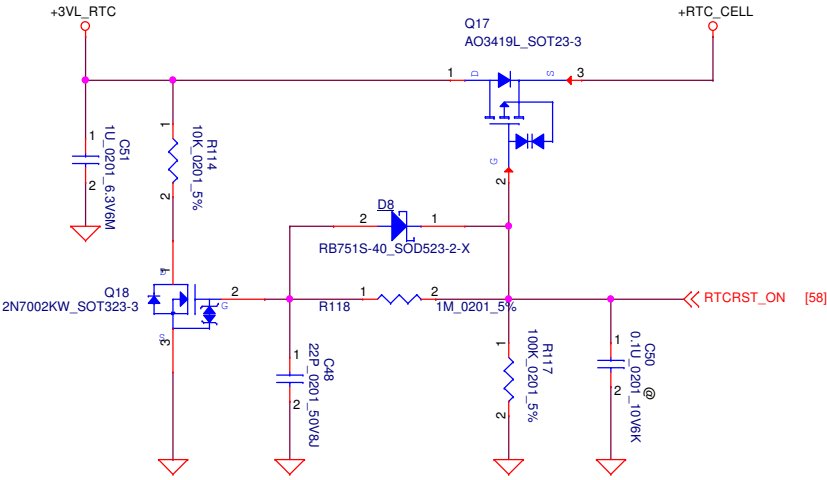


Main Func = M\_BIST



|   |                    |                 |            |                          |                           |
|---|--------------------|-----------------|------------|--------------------------|---------------------------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                           |
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|   |                    |                 |            | Sheet                    | 65 of 121                 |
|   |                    |                 |            | Rev                      | 0.2                       |

Main Func = RTC Gen9

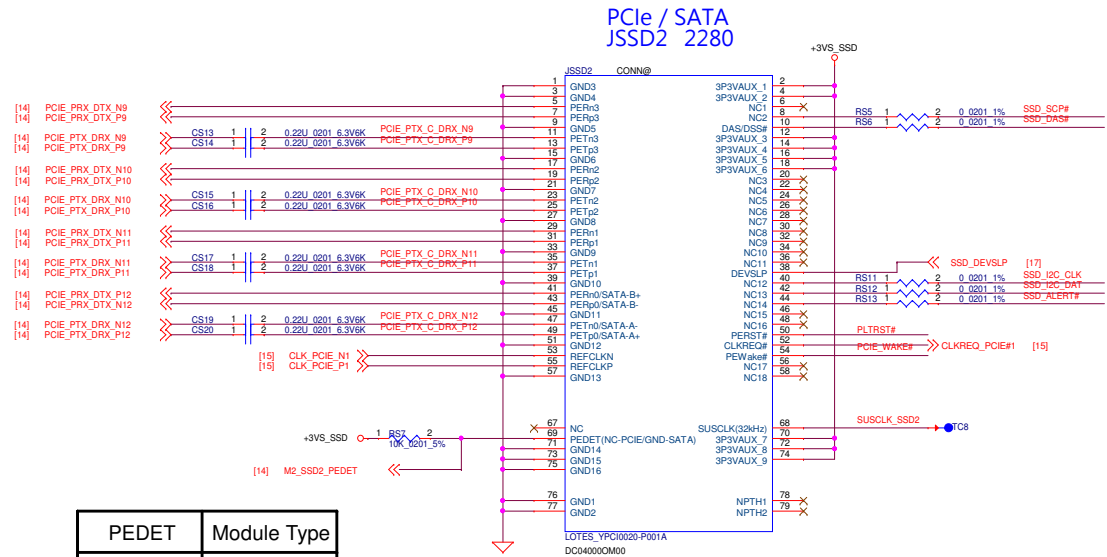
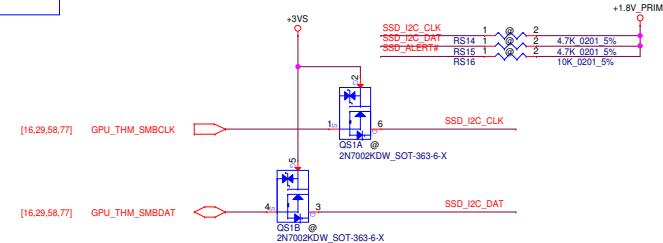
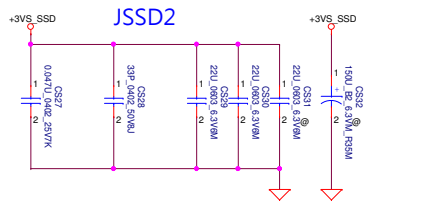


|   |            |                    |            |                          |                           |
|---|------------|--------------------|------------|--------------------------|---------------------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                           |
| Issued Date   | 2020/03/05 | Deciphered Date    | 2019/04/01 | Title                    |                           |
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|   |            |                    |            | Size                     | Rev                       |
|   |            |                    |            | Document Number          | 0.2                       |
|   |            |                    |            | LA-K661P                 |                           |
|   |            |                    |            | Date:                    | Monday, February 08, 2021 |
|   |            |                    |            | Sheet                    | 66 of 121                 |

Main Function:

Reserve

|  |                    |                 |            |                          |                           |                 |
|--|--------------------|-----------------|------------|--------------------------|---------------------------|-----------------|
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|  |                    |                 |            |                          | LA-K661P                  | 0.2             |
|  |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 67 of 121 |



|       |             |
|-------|-------------|
| PEDET | Module Type |
| 0     | SATA        |
|       |             |

|   |                    |                 |            |                                 |                 |            |
|---|--------------------|-----------------|------------|---------------------------------|-----------------|------------|
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|   |                    |                 |            | Size                            | Document Number | Rev        |
|   |                    |                 |            | <b>LA-K661P</b>                 |                 | <b>0.2</b> |
| Date:   |                    |                 |            | Monday, February 08, 2021       | Sheet           | 68 of 121  |

Main Function:

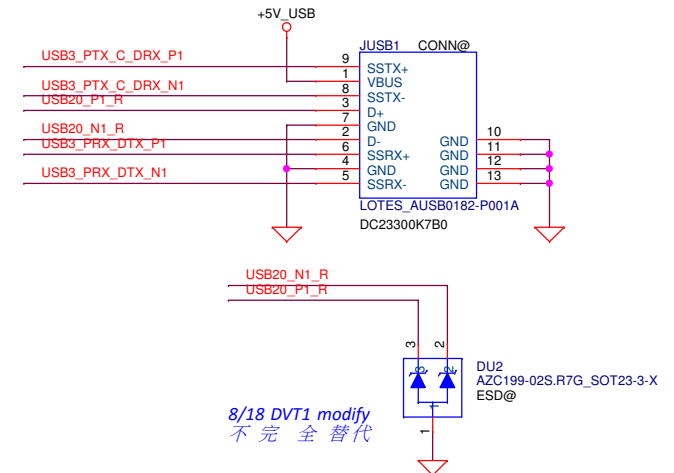
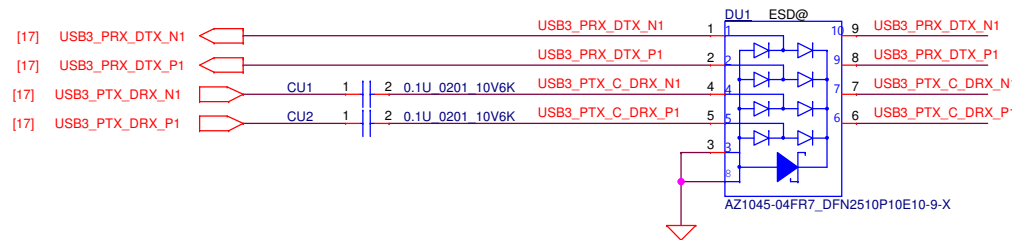
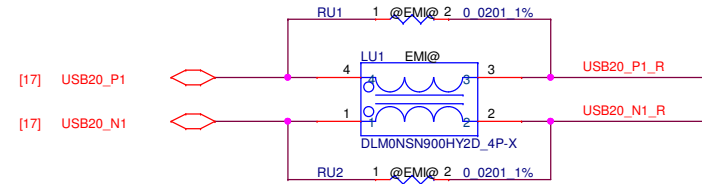
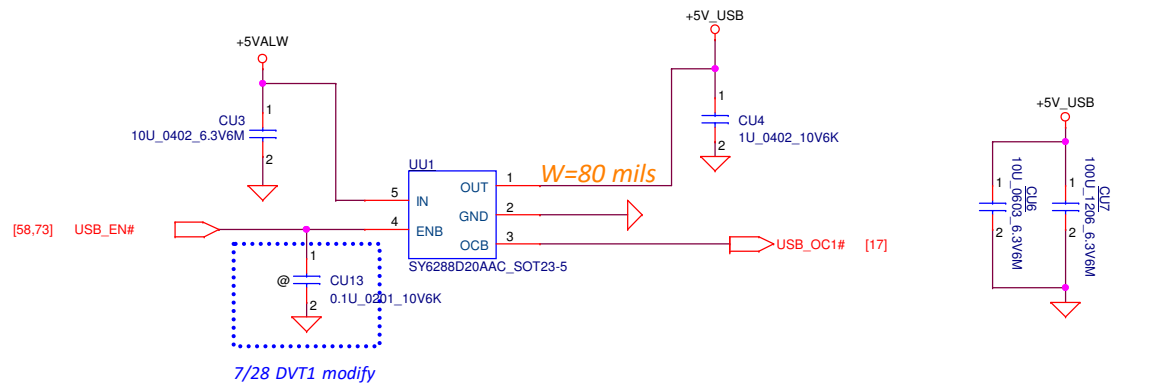
Reserve

|  |                    |                 |            |                          |                           |                 |
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| Security Classification  | Compal Secret Data |                 |            | Compal Electronics, Inc. |                           |                 |
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|  |                    |                 |            |                          | LA-K661P                  | 0.2             |
|  |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 69 of 121 |

Main Function:

# Reserve

|   |                    |                 |            |                          |                           |                 |
|---|--------------------|-----------------|------------|--------------------------|---------------------------|-----------------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                           |                 |
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|   |                    |                 |            |                          | LA-K661P                  | 0.2             |
|   |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 70 of 121 |



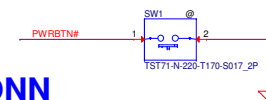
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| Issued Date   | 2020/03/05 | Deciphered Date    | 2017/01/06 | Title                    | USB3.1 TypeA Gen1         |
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|   |            |                    |            | Sheet                    | 71 of 121                 |
|   |            |                    |            | Rev                      | 0.2                       |

Main Function:

Reserve

|  |                    |                 |            |                          |                           |                 |
|--|--------------------|-----------------|------------|--------------------------|---------------------------|-----------------|
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| Issued Date  | 2020/03/05         | Deciphered Date | 2017/01/06 | Title                    | RSV                       |                 |
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|  |                    |                 |            |                          | LA-K661P                  | 0.2             |
|  |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 72 of 121 |





|   |  |                    |  |                                 |  |                 |  |
|---|--|--------------------|--|---------------------------------|--|-----------------|--|
| Security Classification   |  | Compal Secret Data |  | Compal Electronics, Inc.        |  |                 |  |
| Issued Date   |  | 2020/03/05         |  | Deciphered Date                 |  | 2018/02/05      |  |
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|   |  |                    |  | IO Board CONN                   |  |                 |  |
|   |  |                    |  | Size Document Number            |  |                 |  |
|   |  |                    |  | LA-K661P                        |  |                 |  |
|   |  |                    |  | Date: Monday, February 08, 2021 |  | Sheet 73 of 121 |  |
|   |  |                    |  |                                 |  | Rev 0.2         |  |

Main Function:

Reserve

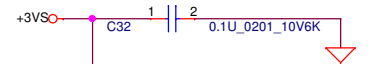
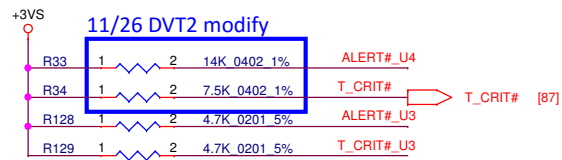
|  |                    |                 |            |                          |                           |                 |
|--|--------------------|-----------------|------------|--------------------------|---------------------------|-----------------|
| Security Classification  | Compal Secret Data |                 |            | Compal Electronics, Inc. |                           |                 |
| Issued Date  | 2020/03/05         | Deciphered Date | 2019/04/01 | Title                    | DOCK(RSVD)                |                 |
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|  |                    |                 |            |                          | LA-K661P                  | 0.2             |
|  |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 74 of 121 |



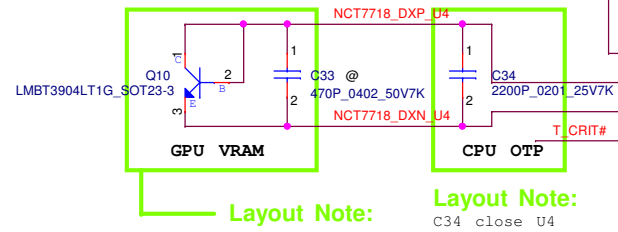
Main Function:

Reserve

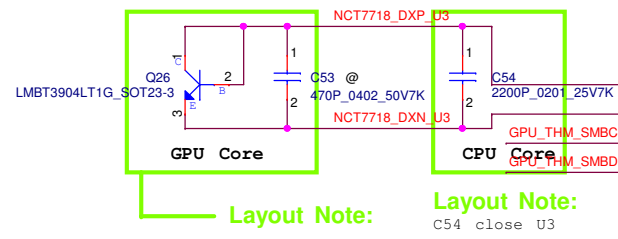
|   |                    |                 |            |                          |                           |                 |
|---|--------------------|-----------------|------------|--------------------------|---------------------------|-----------------|
| Security Classification   | Compal Secret Data |                 |            | Compal Electronics, Inc. |                           |                 |
| Issued Date   | 2020/03/05         | Deciphered Date | 2017/01/06 | Title                    | RSV                       |                 |
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|   |                    |                 |            |                          | LA-K661P                  | 0.2             |
|   |                    |                 |            | Date:                    | Monday, February 08, 2021 | Sheet 76 of 121 |



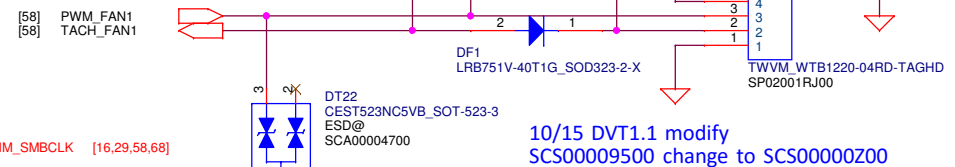
Address 1001100xb (0x98h)



Address 1001101xb (0x9Ah)

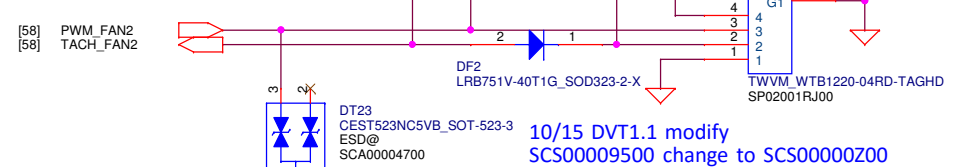


CPU FAN Control



1/8 DVT2.1 modify

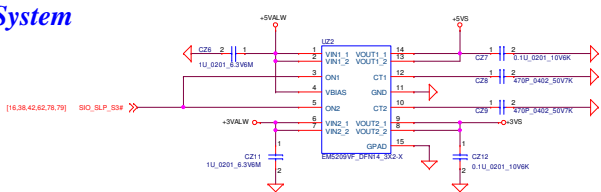
GPU FAN Control



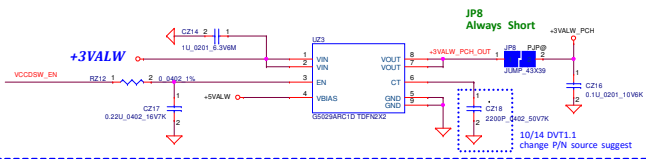
1/8 DVT2.1 modify

|   |            |                    |            |                          |                           |
|---|------------|--------------------|------------|--------------------------|---------------------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |                           |
| Issued Date   | 2020/03/05 | Deciphered Date    | 2018/02/05 | Title                    | FAN/Thermal               |
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|   |            |                    |            | Sheet                    | 77 of 121                 |
|   |            |                    |            | Rev                      | 0.2                       |
|   |            |                    |            | LA-K661P                 |                           |

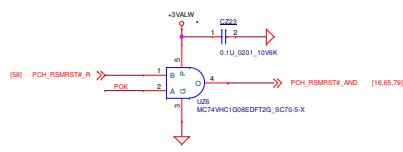
+5VS / +3VS for System



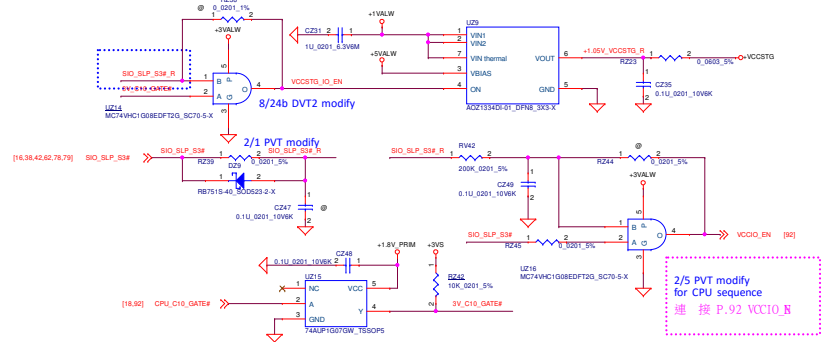
+3VALW TO +3VALW\_PCH



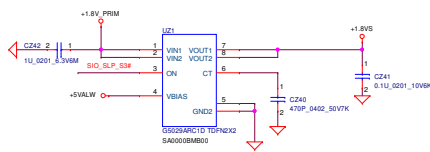
RSMRST circuit



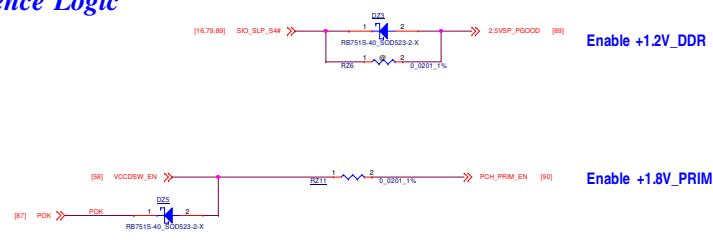
VCCSTG



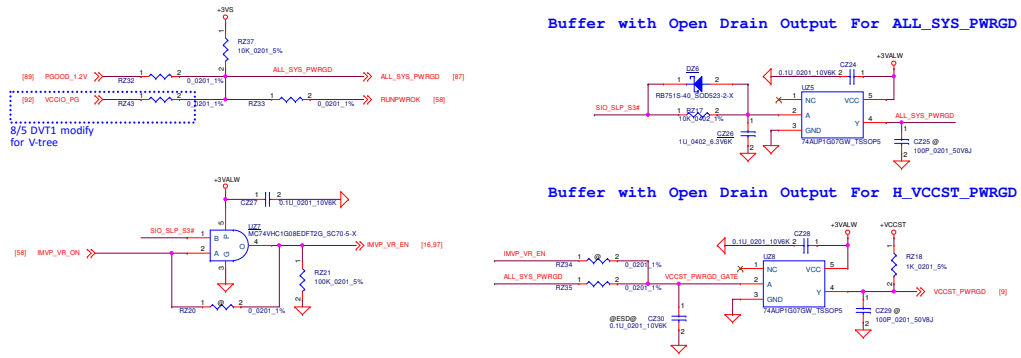
+1.8VS for System



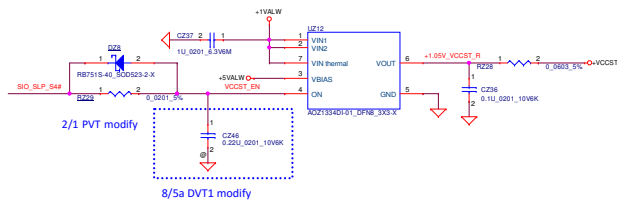
Sequence Logic



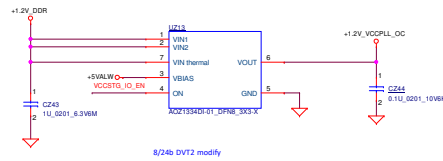
IMVP\_VR\_ON&VCCST\_PWRGD



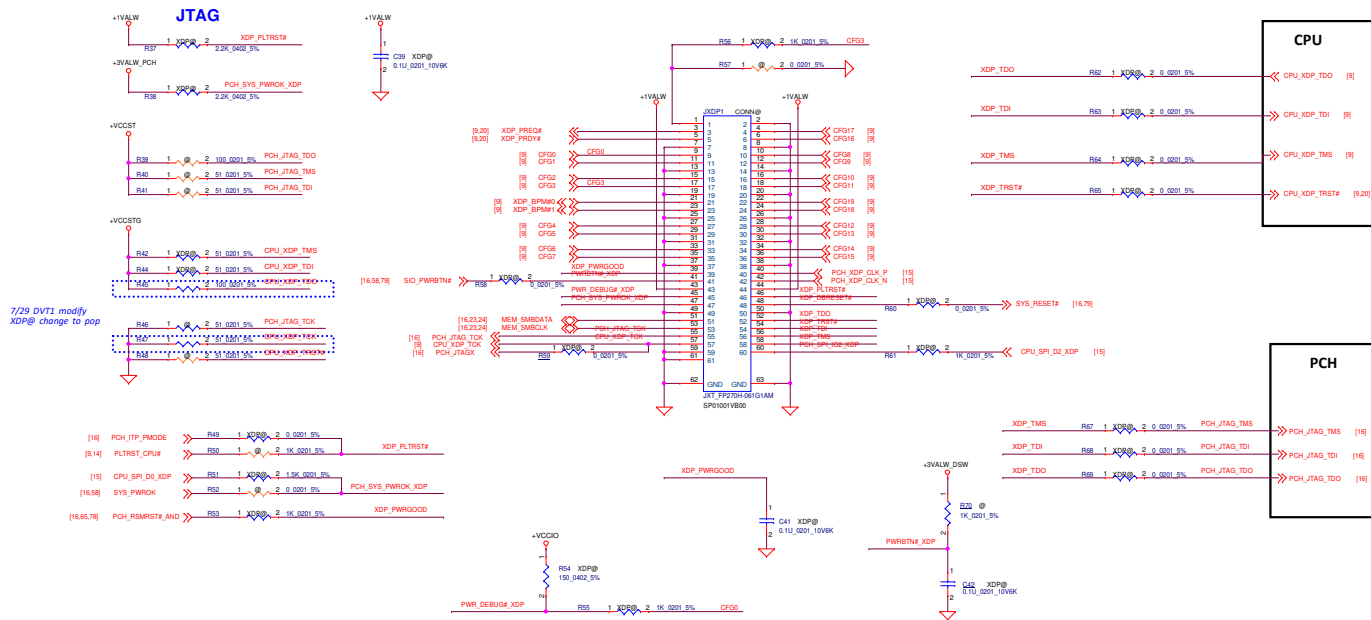
VCCST



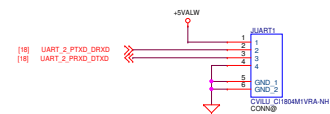
VCCPLL\_OC



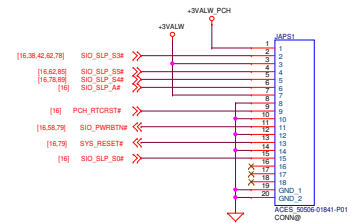
## XDP



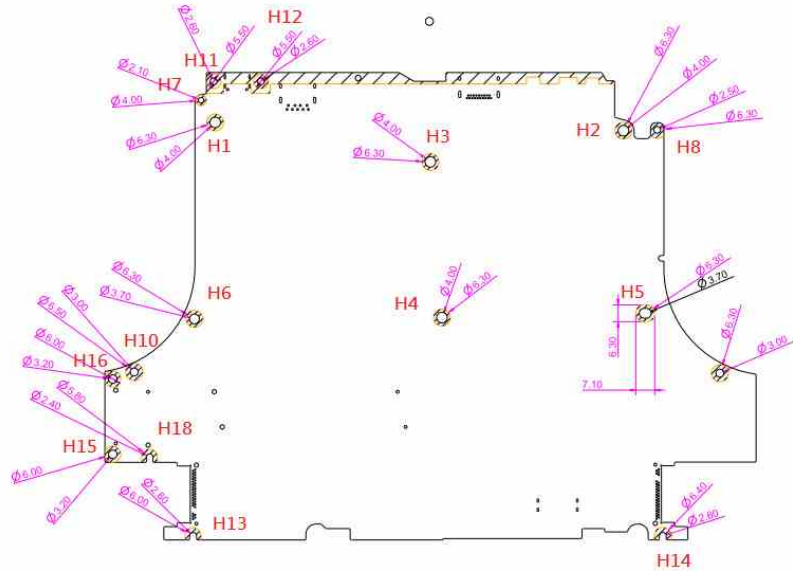
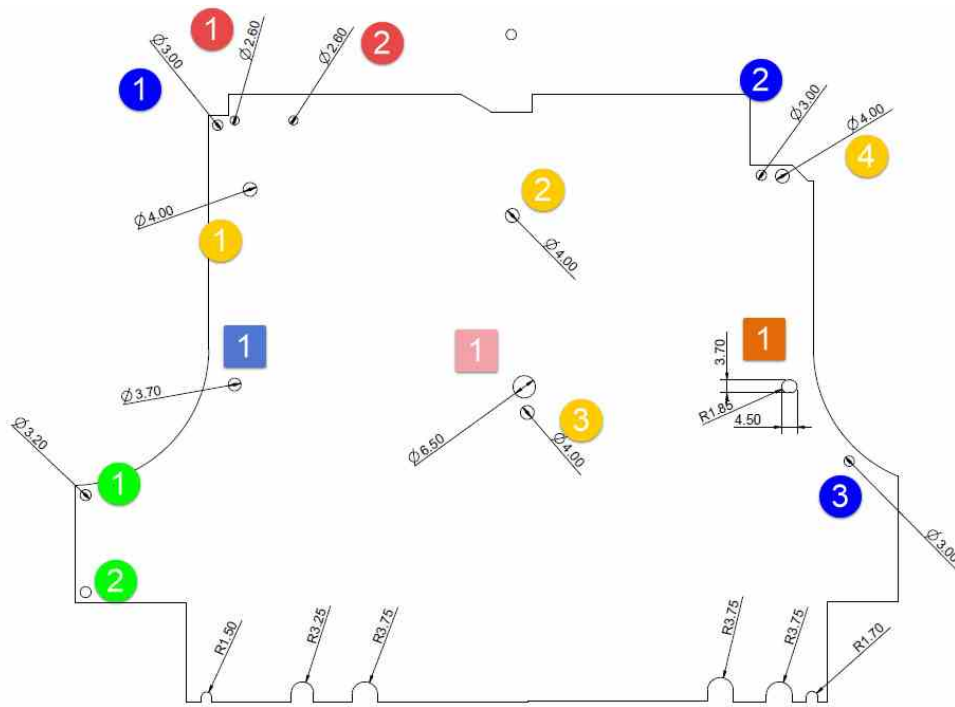
## BIOS UART Debug



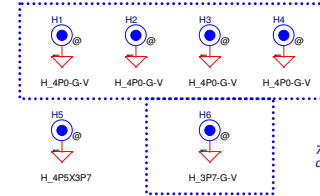
AP S



|   |                           |                    |            |  |                             |
|---|---------------------------|--------------------|------------|--|-----------------------------|
| Security Classification   |                           | Compal Secret Data |            | <b><i>Compal Electronics, Inc.</i></b> |                             |
| Issued Date   | 2020/03/05                | Deciphered Date    | 2018/10/01 | Title                                  | <b><i>Debug APS_DEG</i></b> |
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| Doc No.   | LA-K661P                  | Doc Name           | LA-K661P   | Rev                                    | 01                          |
| Date  | Monday, February 09, 2021 | Drawn              | by         | cl                                     | cl                          |

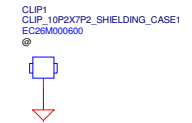


### CPU GPU



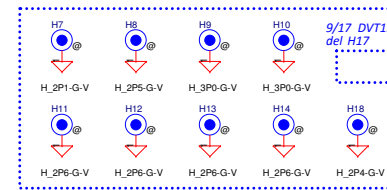
7/23 DVT1 modify  
change to V18D10

### SHIELDING CASE



7/23 DVT1 modify  
change to V18D10

### PTH

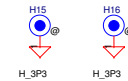


7/23 DVT1 modify  
change to V18D10

12/16 DVT2 modify  
add H17

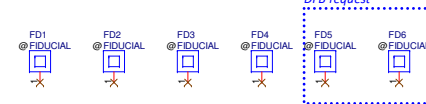


### Stand-off



8/4a DVT1 modify

### Fiducial Mark

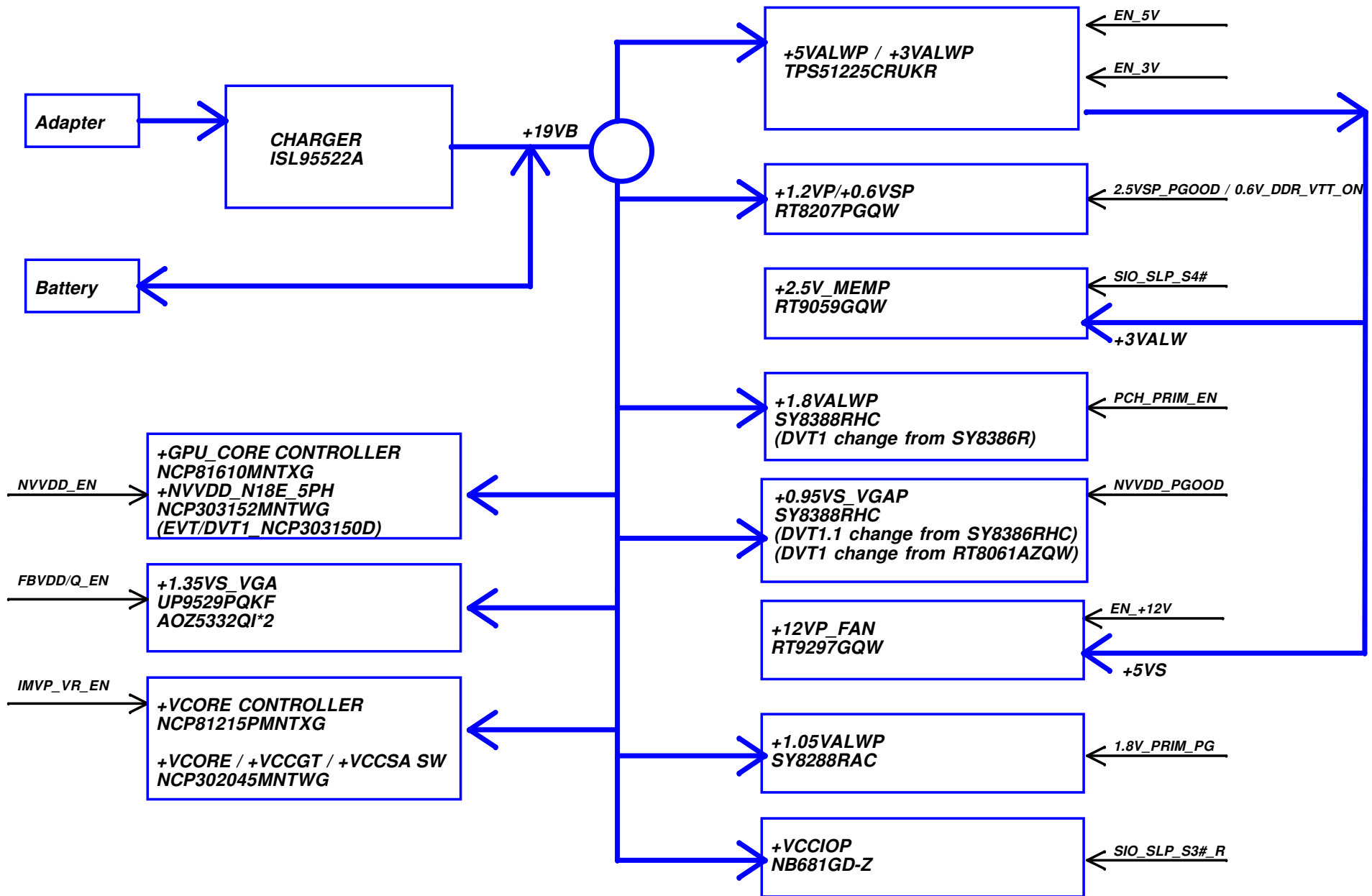


10/12 DVT1.1 modify  
DFB request

|   |            |                    |            |                          |                           |
|---|------------|--------------------|------------|--------------------------|---------------------------|
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|   |            |                    |            | Sheet                    | 80 of 121                 |
|   |            |                    |            | Rev                      | 0.2                       |



# Power block



|   |            |                           |            |                          |  |
|---|------------|---------------------------|------------|--------------------------|--|
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| Size  |            | Document Number           |            | Rev                      |  |
|   |            | LA-K661P                  |            | 0.1                      |  |
| Date  |            | Monday, February 08, 2021 |            | Sheet 81 of 121          |  |

## Main Func = DCIN CONN

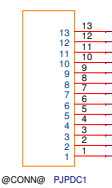
20200731 Modify DC IN Define

### Adapter Connector

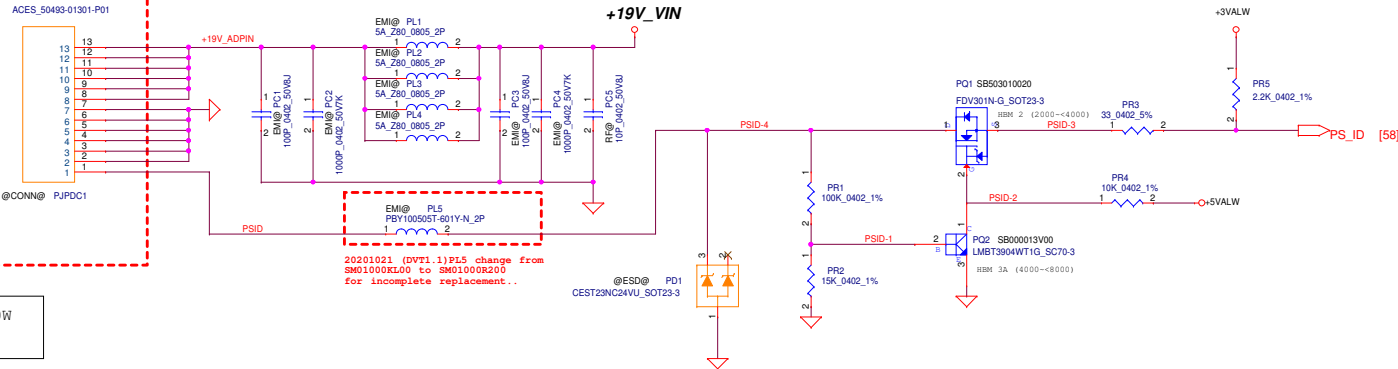
#### Adapter Bot Side

PIN1 PSID  
PIN2 GND  
PIN3 GND  
PIN4 GND  
PIN5 GND  
PIN6 GND  
PIN7 GND  
PIN8 ADPIN  
PIN9 ADPIN  
PIN10 ADPIN  
PIN11 ADPIN  
PIN12 ADPIN  
PIN13 ADPIN  
ACES\_50493-01301-P01

ACES\_50493-01301-P01



Adapter 180W / 240W  
240W/19V=12.63A



20201021 (DVT1.1) PL5 change from SM01000KL00 to SM01000R200 for incomplete replacement..

@ESD@ PD1  
CEST2N2C24VU\_SOT23-3

## Main Func = BATT CONN

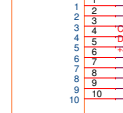
### Battery Connector

#### Battery Bot Side

PIN10 GND  
PIN9 GND  
PIN8 GND  
PIN7 SYS\_PRES#  
PIN6 BATT\_PR#  
PIN5 DAT\_SMB  
PIN4 CLK\_SMB  
PIN3 BATT+  
PIN2 BATT+  
PIN1 BATT+  
SP07001R500

OCTEK WTB-10FPBLAB-U

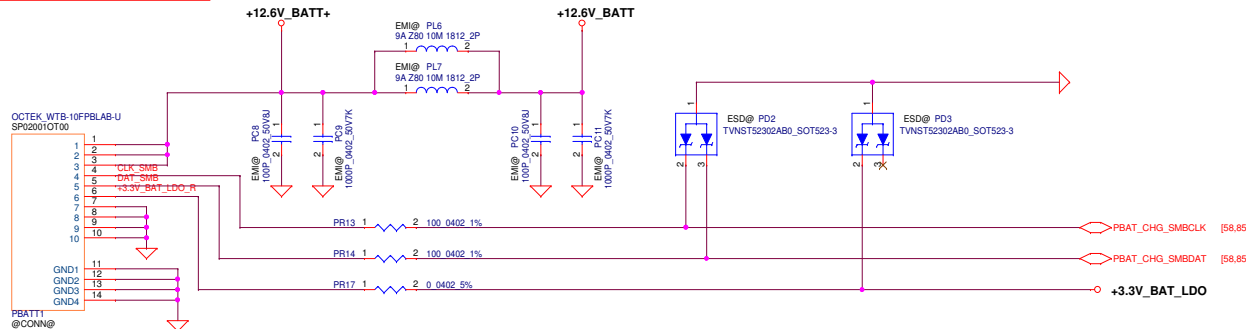
SP02001C700



PBATT1

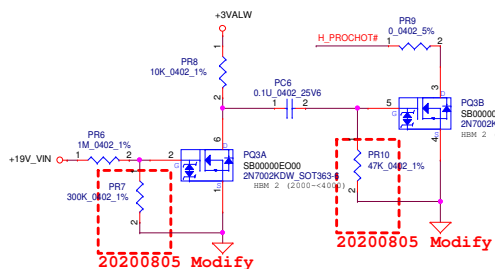
@CONN@

Battery 56W  
56W/11.4V=4.91A  
Battery 86W  
86W/11.4V=7.54A

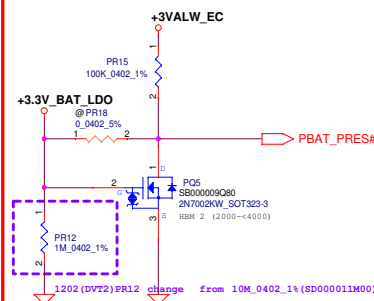
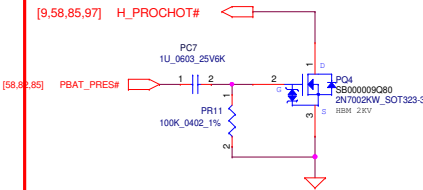


Change PR40 to 0 ohm for EE request  
20200729

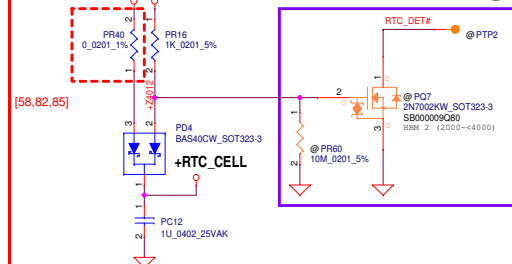
### Adapter protection:



### Battery protection:



### 1125(DVT2) change from +3.3V\_ADP\_DCIN to +3VLP. COIN RTC Battery



|   |  |                    |  |                                  |  |                 |
|---|--|--------------------|--|----------------------------------|--|-----------------|
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| Issued Date   |  | Deciphered Date    |  | Title                            |  |                 |
| 2020/03/05  |  | 2017/01/06         |  | PWR-DCIN / OTP / BATT CONN / RTC |  |                 |
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|   |  |                    |  | Document Number                  |  |                 |
|   |  |                    |  |                                  |  |                 |
|   |  |                    |  | Date: Monday, February 08, 2021  |  | Sheet 82 of 121 |

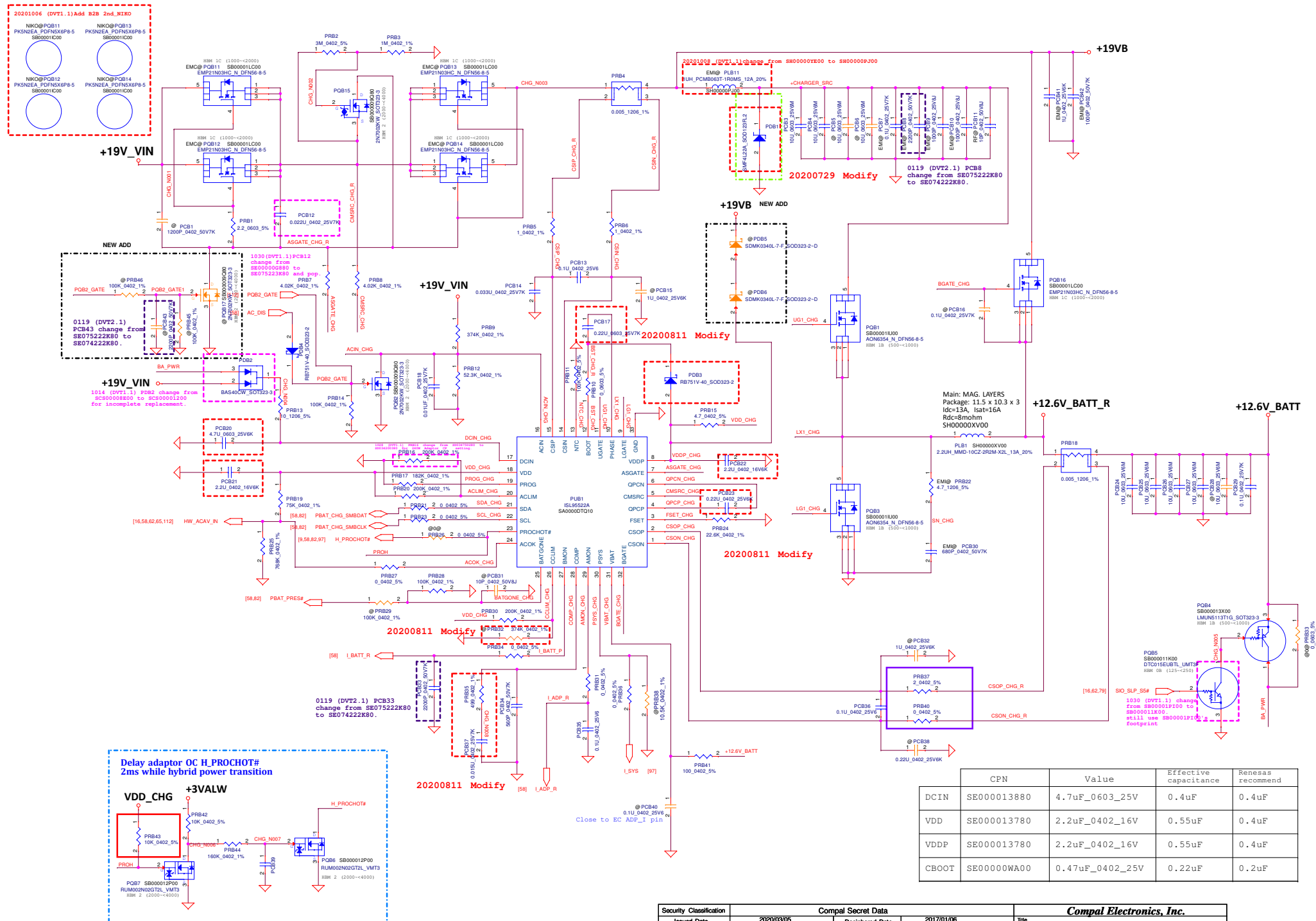
# Reserve for PWR

|   |            |                           |            |                          |           |
|---|------------|---------------------------|------------|--------------------------|-----------|
| Security Classification   |            | Compal Secret Data        |            | Compal Electronics, Inc. |           |
| Issued Date   | 2020/03/05 | Deciphered Date           | 2017/01/06 | Title                    |           |
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|   |            |                           |            | Document Number          | 0.1       |
| Date:   |            | Monday, February 08, 2021 |            | Sheet                    | 83 of 121 |

# Reserve for PWR

|   |            |                    |            |                          |           |
|---|------------|--------------------|------------|--------------------------|-----------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |           |
| Issued Date   | 2020/03/05 | Deciphered Date    | 2017/01/06 | Title                    |           |
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|   |            |                    |            | Document Number          | 0.1       |
| Date: Monday, February 08, 2021   |            |                    |            | Sheet                    | 84 of 121 |

**Main Func = CHARGER**



|       | CPN         | Value           | Effective capacitance | Renesas recommend |
|-------|-------------|-----------------|-----------------------|-------------------|
| DCIN  | SE000013880 | 4.7uF_0603_25V  | 0.4uF                 | 0.4uF             |
| VDD   | SE000013780 | 2.2uF_0402_16V  | 0.55uF                | 0.4uF             |
| VDDP  | SE000013780 | 2.2uF_0402_16V  | 0.55uF                | 0.4uF             |
| CBOOT | SE00000WA00 | 0.47uF_0402_25V | 0.22uF                | 0.2uF             |

# Reserve for PWR

|  |            |                    |            |                                 |                 |
|--|------------|--------------------|------------|---------------------------------|-----------------|
| Security Classification  |            | Compal Secret Data |            | Compal Electronics, Inc.        |                 |
| Issued Date  | 2020/03/05 | Deciphered Date    | 2017/01/06 | Title                           |                 |
| <small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small> |            |                    |            | PWR- Reserve for PWR            |                 |
|  |            |                    |            | Size                            | Rev             |
|  |            |                    |            | Document Number                 | 0.1             |
|  |            |                    |            | LA-K661P                        |                 |
|  |            |                    |            | Date: Monday, February 08, 2021 | Sheet 86 of 121 |

**Main Func = 3VALWP / 5VALWP**

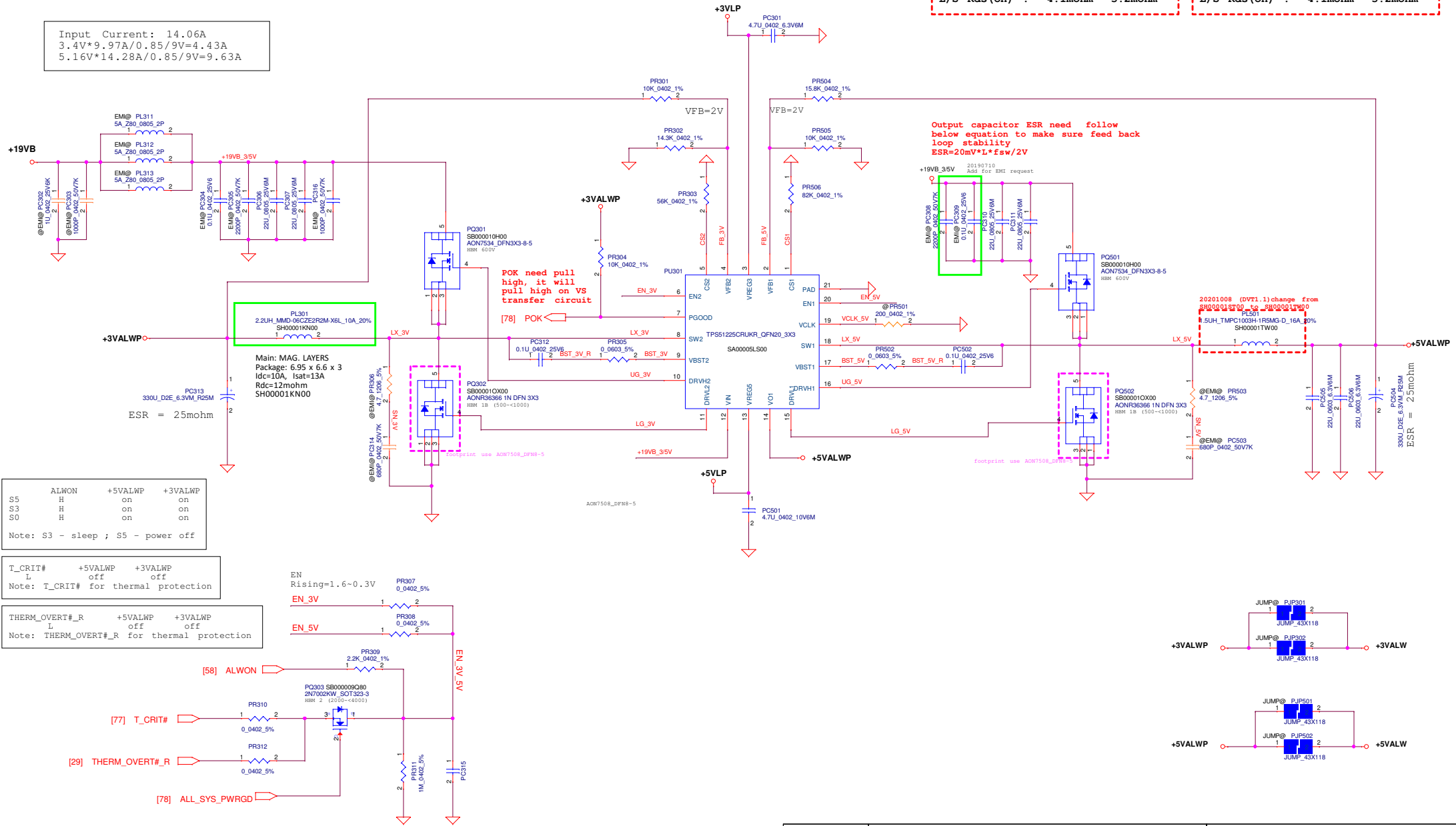
Input Current: 14.06A  
 $3.4V \times 9.97A / 0.85 / 9V = 4.43A$   
 $5.16V \times 14.28A / 0.85 / 9V = 9.63A$

```
3VALWP
Vout=3.4V
TDC 10A
Peak Current 10.83A
OCP current 13 A
OVP=3.824V~3.994V(112.5%~117.5%)
UVP=1.869V~2.209V(55%~65%)
FSW=355kHz
```

| MOS (VGS = 4.5V ) |         |         |
|-------------------|---------|---------|
|                   | TYP     | MAX     |
| H/S Rds (on) :    | 6.7mohm | 8.5mohm |
| L/S Rds (on) :    | 4.1mohm | 5.2mohm |

```
5VALWP
Vout= 5.16V
TDC 11.73A
Peak Current 14.34A
OCP current 17.21A
OVP=5.805V~6.063V(112.5%~117.5%)
UVP=2.838V~3.354V(55%~65%)
FSW=300kHz
```

|                   |         |         |
|-------------------|---------|---------|
| MOS (VGS = 4.5V ) |         |         |
|                   | TYP     | MAX     |
| H/S Rds(on) :     | 6.7mohm | 8.5mohm |
| L/S Rds(on) :     | 4.1mohm | 5.2mohm |



|  |                    |                 |            |                                 |                             |       |           |     |
|--|--------------------|-----------------|------------|---------------------------------|-----------------------------|-------|-----------|-----|
| Security Classification  | Compal Secret Data |                 |            | <b>Compal Electronics, Inc.</b> |                             |       |           |     |
| Issued Date  | 2020/03/05         | Deciphered Date | 2018/12/31 | Title                           | <b>PWR +3.3VALWP+5VALWP</b> |       |           |     |
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|  |                    |                 |            | <b>LA-J743P</b>                 |                             |       |           | 0.1 |
|  |                    |                 |            | Date:                           | Monday, February 08, 2021   | Sheet | 87 of 121 |     |

# Reserve for PWR

|   |            |                    |            |                          |           |
|---|------------|--------------------|------------|--------------------------|-----------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |           |
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|   |            |                    |            | Document Number          | 0.1       |
| Date: Monday, February 08, 2021   |            |                    |            | Sheet                    | 88 of 121 |



# Main Func = 1.2VP / 0.6VSP / 2.5V\_MEMP

Input Current: 1.012A

$$1.203V \times 5.92A / 0.85 / 9V = 0.93A$$

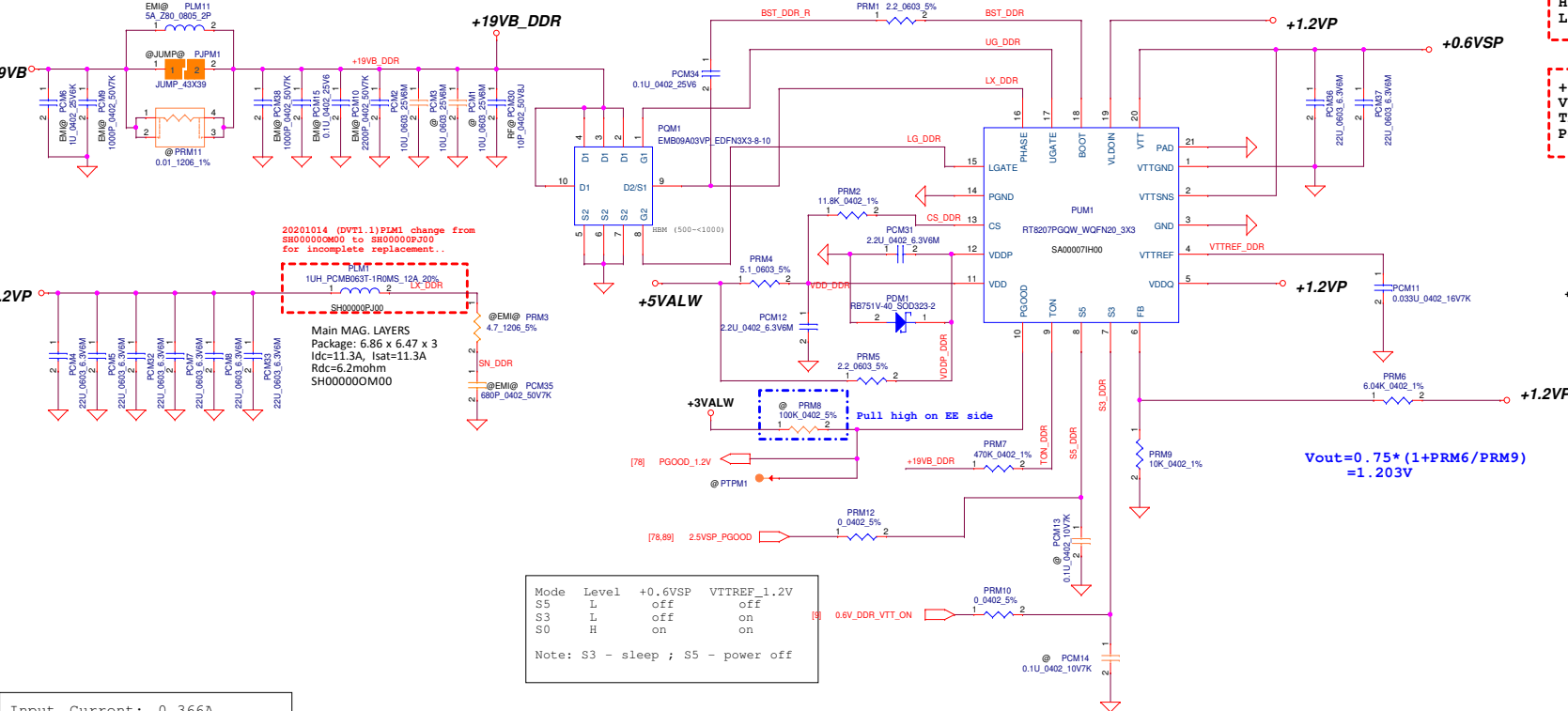
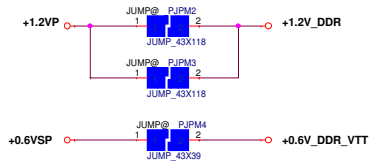
$$0.6V \times 1.05A / 0.85 / 9V = 0.082A$$

Pin19 need pull separate from +1.2VP.  
If you have +1.2V and +0.6V sequence question,  
you can change from +1.2VP to +1.2VS.

+1.2VP  
Vout= 1.203V  
TDC 5.92A  
Peak Current 8.46A  
OCP current 10.12A  
OVP=1.36V~1.44V (113%~120%)  
UVP=0.72V~0.96V (60%~80%)  
FSW= ~538K Hz

MOS (VGS = 4.5V)  
H/S Rds(on) : 11mohm TYP 13mohm MAX  
L/S Rds(on) : 11mohm TYP 13mohm MAX

+0.6VSP  
Vout= 1.203V  
TDC 1.05A  
Peak Current 1.5A

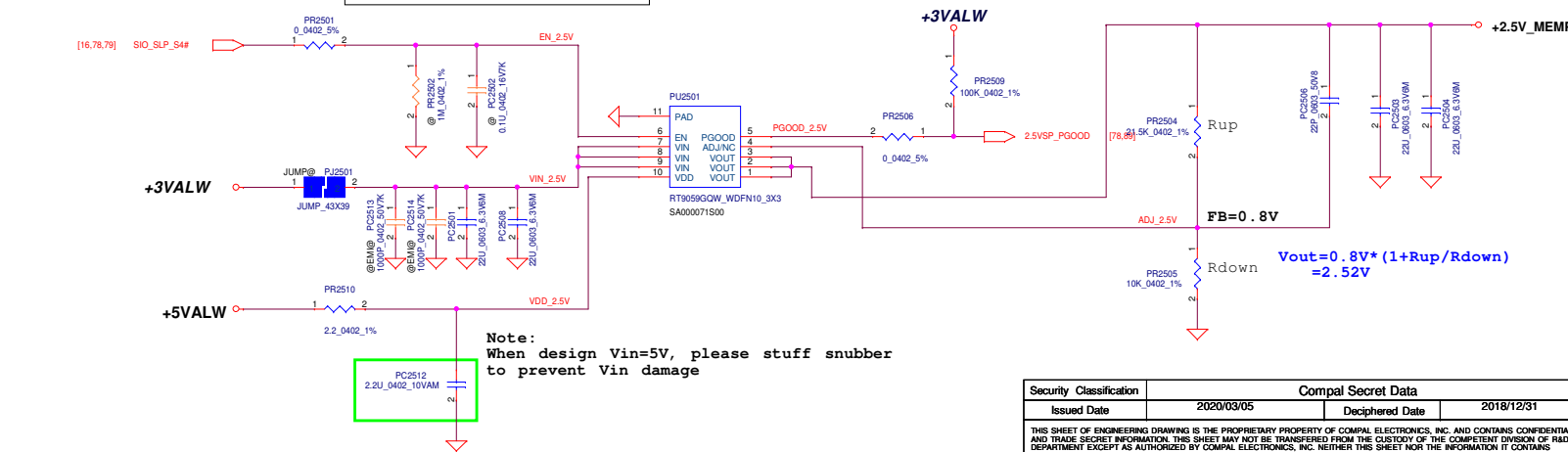


Input Current: 0.366A

$$2.52V \times 0.37A / 0.85 / 3V = 0.366A$$

SIO\_SLP\_S4# +2.5V\_MEMP  
S4 L off  
S3 H on  
S0 H on  
Note: S3 - sleep ; S5 - power off

+2.5V\_MEMP  
Vout= 2.52V  
TDC 0.37A  
Peak Current 0.528A  
Current limit 3.6A



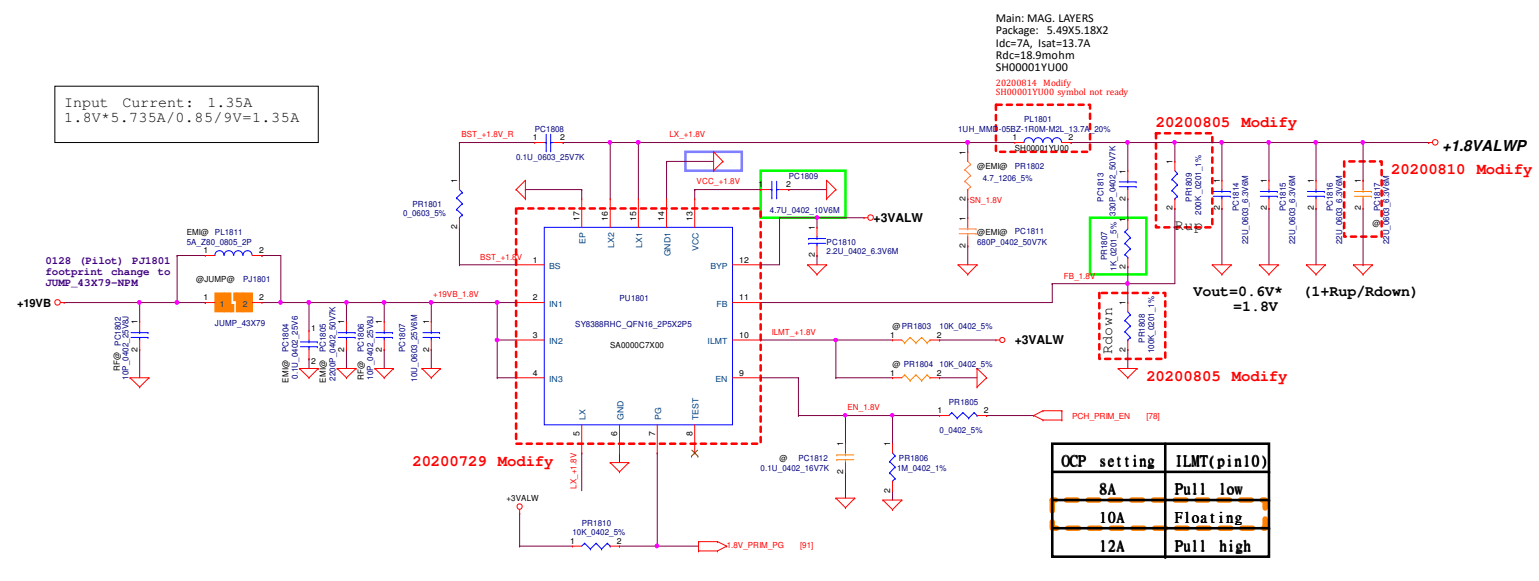
Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage

|   |                    |                          |
|---|--------------------|--------------------------|
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| Deciphered Date   | 2018/12/31         | 2018/12/31               |
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| Title   |                    |                          |
| PWR 1.2VP/0.6VSP/+2.5V  |                    |                          |
| Size  |                    |                          |
| LA-K661P  |                    |                          |
| Date  |                    |                          |
| Monday, February 06, 2021   |                    |                          |
| Sheet   |                    |                          |
| 89 of 121   |                    |                          |
| Rev   |                    |                          |
| 0.1   |                    |                          |

Main Func = 1.8VALWP

Input Current: 1.35A  
 $1.8V \times 5.735A / 0.85 / 9V = 1.35A$

+1.8VALWP  
TDC 5.735A  
Peak Current 7.768A  
Current limit 10A  
OVP=2.106V~2.214V (117%~123%)  
UVP=0.99V~1.17V (55%~65%)  
FSW= 500K Hz

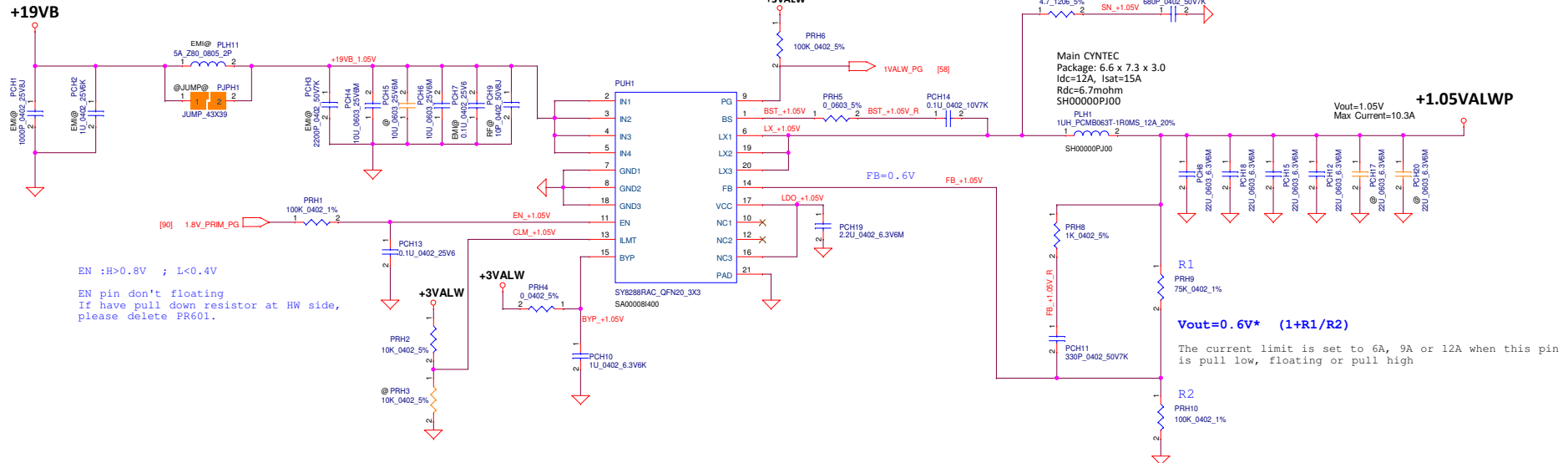


+1.8VALWP → JUMP@ PU1802 JUMP\_43X79 → +1.8V\_PRIM

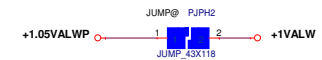
Main Func = 1.05VALWP

Input Current: 0.97A  
 $1.05V \times 8.4A / 0.85 / 9V = 1.15A$

+1.05VALWP  
 TDC 8.4A  
 Peak Current 12A  
 Current limit 16A  
 OVP=1.208V~1.313V(115%~125%)  
 UVP=0.63V~0.735V(60%~70%)  
 FSW= 500K Hz



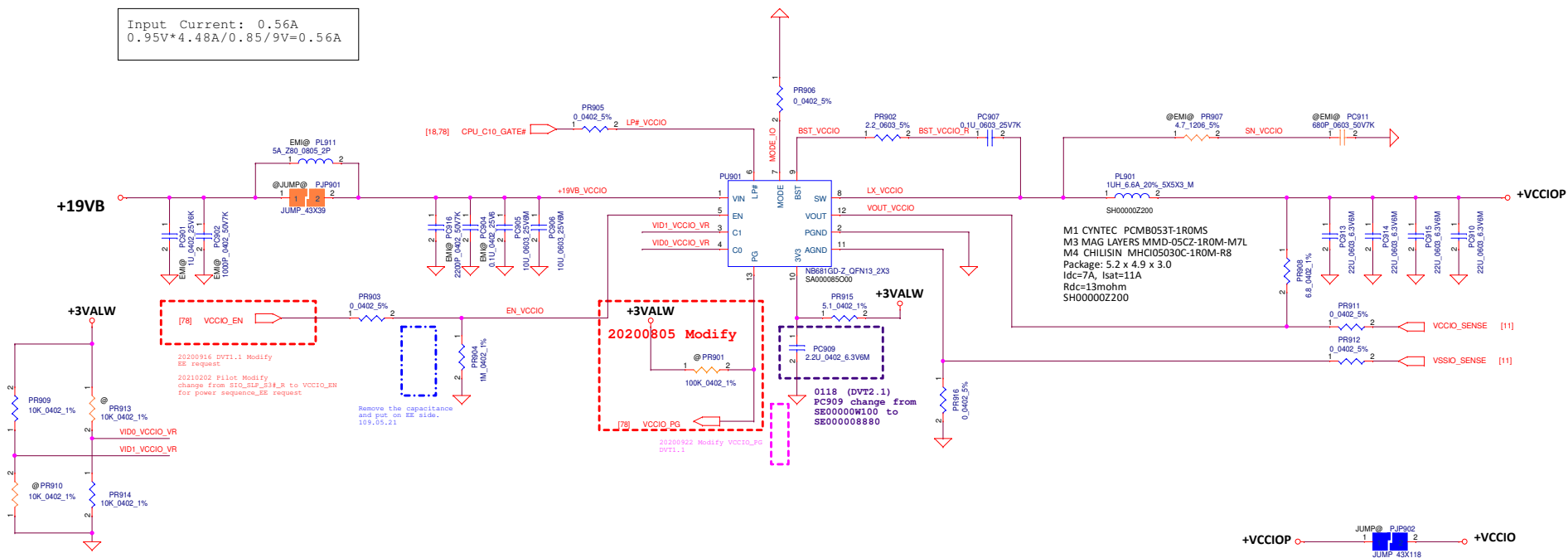
| OCP setting | ILMT(pin13) |
|-------------|-------------|
| 8A          | Pull low    |
| 12A         | Floating    |
| 16A         | Pull high   |



**Main Func = +VCCIOP**

+VCCIOP (0.95V)  
TDC 4.48A  
Peak Current 6.4A  
Current limit 7.6A  
OVP=1.14V~1.28V(120%~135%)  
UVP=0.665V~0.76V(70%~80%)  
FSW= 750K Hz

Input Current: 0.56A  
 $0.95V \times 4.48A / 0.85 / 9V = 0.56A$



Vref mode =GND  
 LP#=0, Vout=0V  
 LP#=1, C1=0, C0=0, Vout=0.85V  
 LP#=1, C1=0, C0=1, Vout=0.875V  
 LP#=1, C1=1, C0=0, Vout=0.95V  
 LP#=1, C1=1, C0=1, Vout=0.975V

|   |  |                    |  |                                 |  |                 |  |
|---|--|--------------------|--|---------------------------------|--|-----------------|--|
| Security Classification   |  | Compal Secret Data |  | Compal Electronics, Inc.        |  |                 |  |
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|   |  |                    |  | PWR+VCCIOP                      |  |                 |  |
|   |  |                    |  | Size                            |  | Document Number |  |
|   |  |                    |  | LA-K661P                        |  | 0.1             |  |
|   |  |                    |  | Date: Monday, February 08, 2021 |  | Sheet 92 of 121 |  |

# Reserve for PWR

|   |            |                    |            |                                 |                 |
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|   |            |                    |            | Size                            | Rev             |
|   |            |                    |            | Document Number                 | 0.1             |
|   |            |                    |            | LA-K661P                        |                 |
|   |            |                    |            | Date: Monday, February 08, 2021 | Sheet 93 of 121 |

# Reserve for PWR

|  |            |                           |            |                          |           |
|--|------------|---------------------------|------------|--------------------------|-----------|
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| Issued Date  | 2020/03/05 | Deciphered Date           | 2017/01/06 | Title                    |           |
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|  |            |                           |            | Document Number          | 0.1       |
| Date:  |            | Monday, February 08, 2021 |            | Sheet                    | 94 of 121 |

# Reserve for PWR

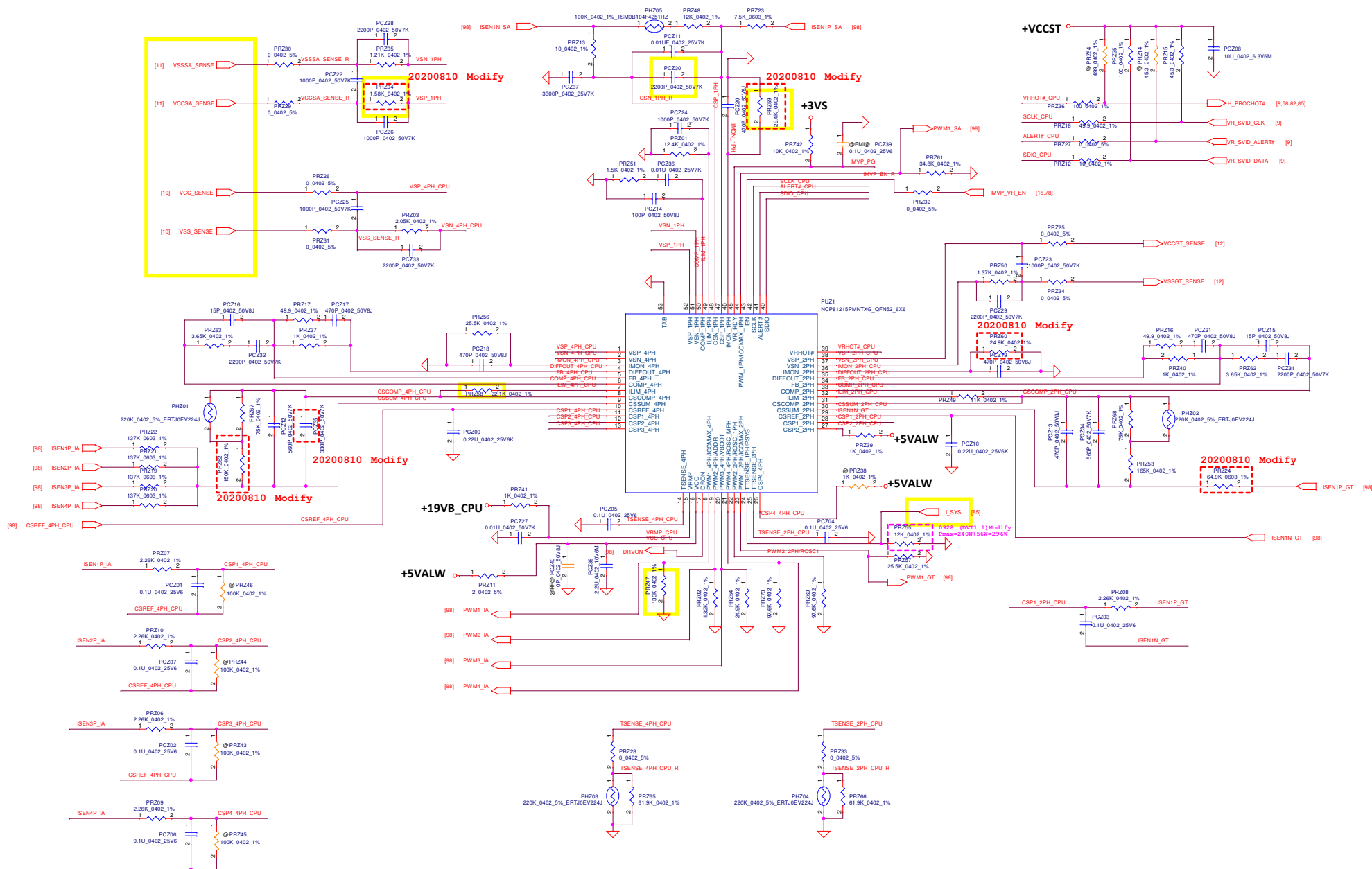
|   |            |                    |            |                                 |                 |
|---|------------|--------------------|------------|---------------------------------|-----------------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc.        |                 |
| Issued Date   | 2020/03/05 | Deciphered Date    | 2017/01/06 | Title                           |                 |
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|   |            |                    |            | Size                            | Rev             |
|   |            |                    |            | Document Number                 | 0.1             |
|   |            |                    |            | LA-K661P                        |                 |
|   |            |                    |            | Date: Monday, February 08, 2021 | Sheet 95 of 121 |

# Reserve for PWR

|   |            |                    |            |                          |           |
|---|------------|--------------------|------------|--------------------------|-----------|
| Security Classification   |            | Compal Secret Data |            | Compal Electronics, Inc. |           |
| Issued Date   | 2020/03/05 | Deciphered Date    | 2017/01/06 | Title                    |           |
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|   |            |                    |            | Document Number          | 0.1       |
| Date: Monday, February 08, 2021   |            |                    |            | Sheet                    | 96 of 121 |



**Main Func = VCORE**

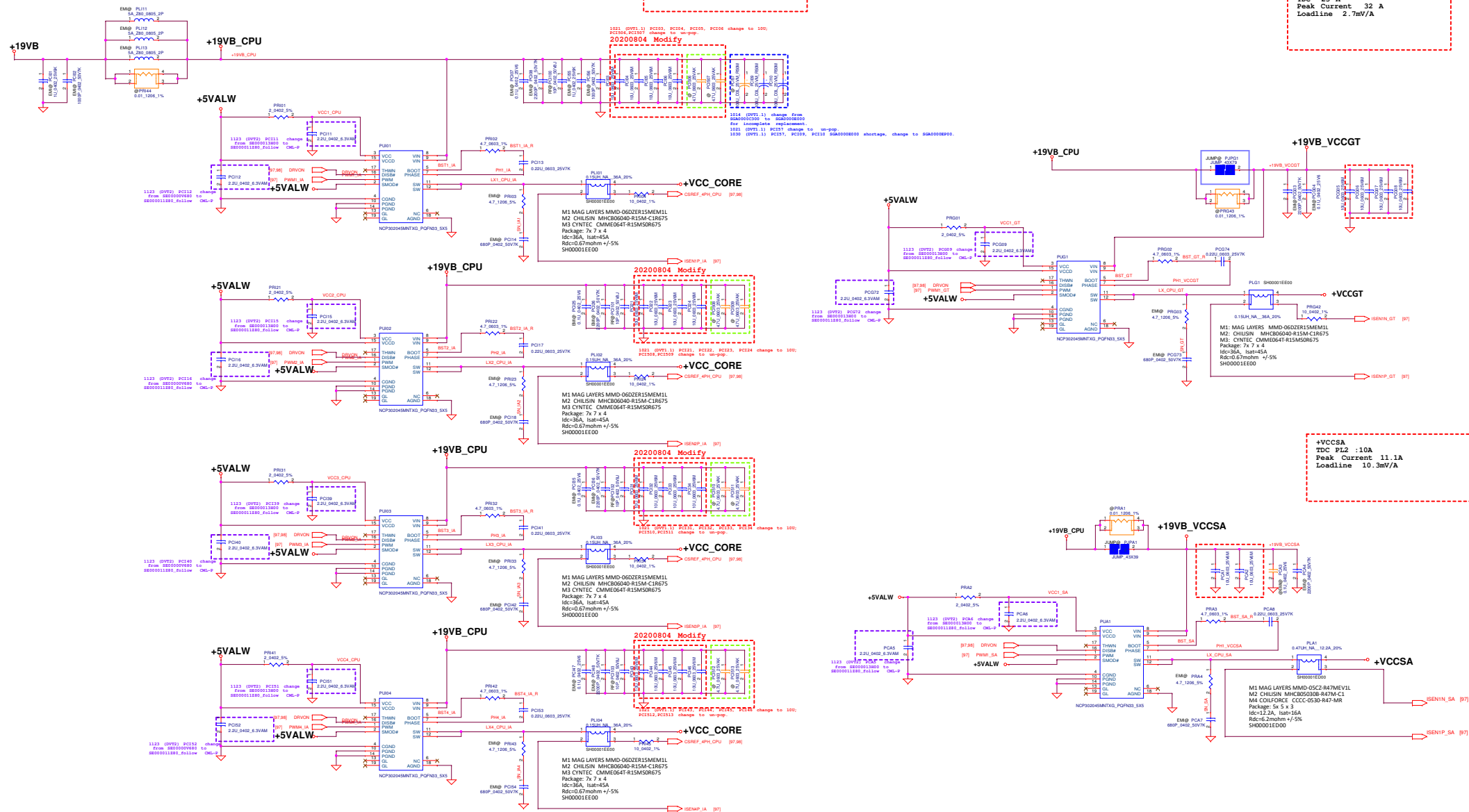


|  |                    |                 |   |       |
|--|--------------------|-----------------|---|-------|
| Security Classification  | Compel Secret Data |                 | <b>Compel Electronics, Inc.</b>           |       |
| Issued Date  | 2020/03/05         | Deciphered Date | 2017/01/06                                | Title |
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|  |                    |                 | Date: Monday, February 08, 1999 97 of 121 |       |

```
Main Func = CPU_CORE_SW
```

```
+VCC_CORE
TDC 125A
Peak Current 165A
Loadline 1.1mV/A
```

```
+VCCGT
TDC 25 A
Peak Current 32 A
Loadline 2.7mV/A
```



|   |                    |                 |  |  |
|---|--------------------|-----------------|--|--|
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|   |                    |                 | Rev 01   |  |

## Reserve for PWR

|   |                    |                 |                          |     |
|---|--------------------|-----------------|--------------------------|-----|
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| Size  | Document Number    |                 | Rev. 01                  |     |
|   | LA-K661P           |                 |                          |     |
|   | 2021               |                 | 1/1                      |     |

# Reserve for PWR

|   |            |                    |            |                                 |                  |
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|   |            |                    |            | Document Number                 | 0.1              |
|   |            |                    |            | Date: Monday, February 08, 2021 | Sheet 100 of 121 |

# +VCC\_CORE

1021 (DVT1.1) change to 330uF  
PC1502 change to 220uF & pop  
PC1503 change to pop

+VCC\_CORE\_intel spec  
470uF\_D2 x4  
47uF\_0805 X 20  
47uF\_0603 X 13  
10uF\_0402 X 32  
1uF\_0201 X 45

+VCCGT\_intel spec  
220uF\_D7 x2  
47uF\_0805 X 3  
22uF\_0603 X 7  
10uF\_0402 X 10  
1uF\_0201 X 12

+VCC\_CORE  
330uF\_D2\_2VM\_R9M X 2  
220uF\_D7\_2.5VM\_R4.5M X 3  
22uF\_0603\_X5R X 33  
10uF\_0402\_X5R X 32  
1uF\_0201\_X5R X 45

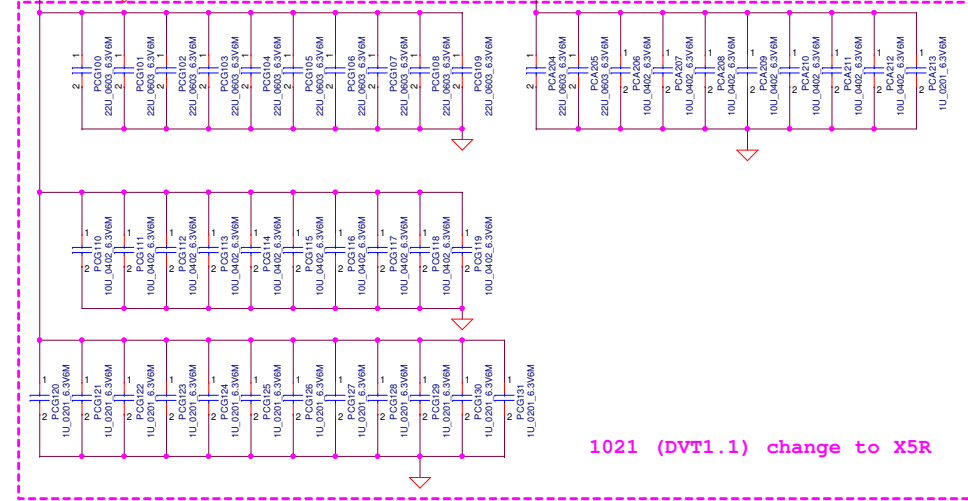
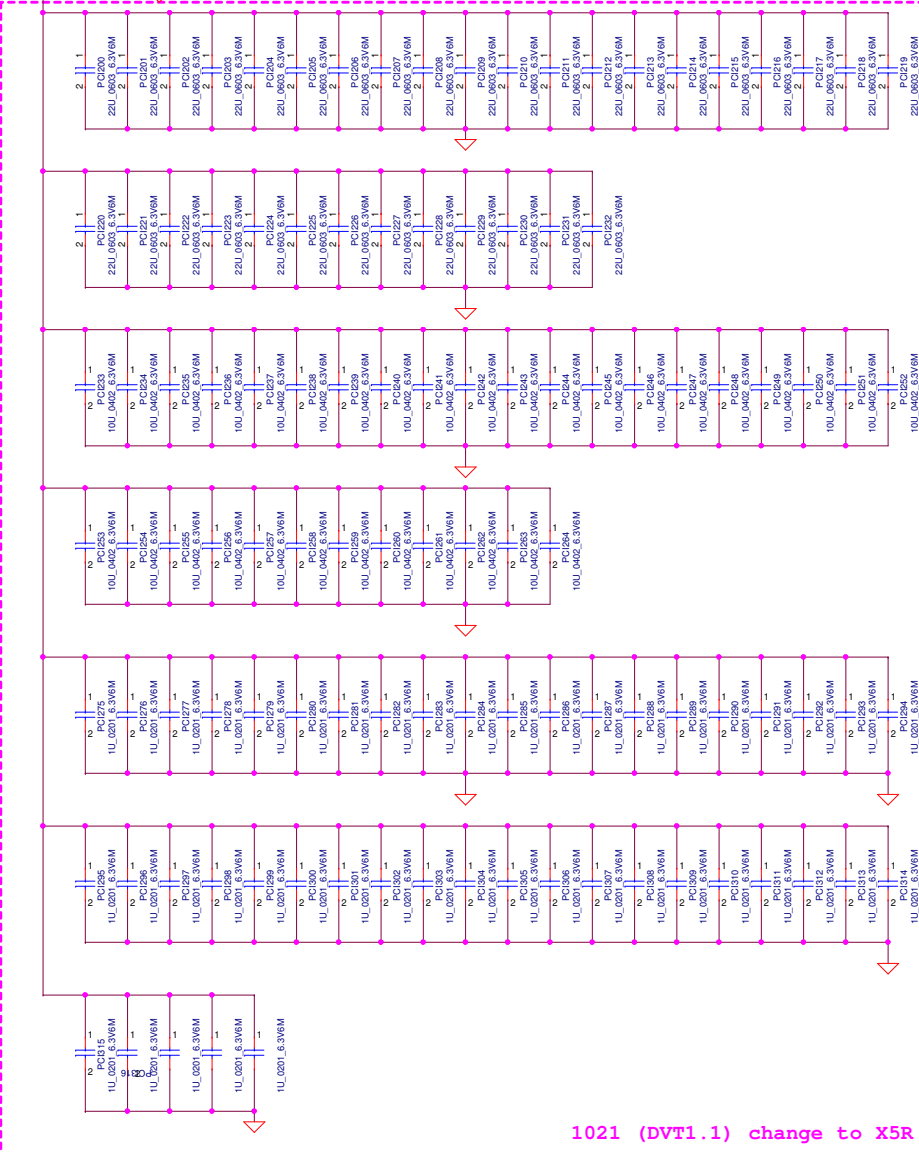
+VCCGT  
220uF\_D7\_2.5VM\_R4.5M X 2  
22uF\_0603\_X5R X 13  
10uF\_0402\_X5R X 10  
1uF\_0201\_X5R X 12

# +VCCGT

# +VCCSA

+VCCSA\_intel spec  
220uF\_D7 x1  
47uF\_0805 X 2  
22uF\_0603 X 2  
10uF\_0402 X 7  
1uF\_0201 X 1

+VCCSA  
22uF\_0603\_X5R X 6  
10uF\_0402\_X5R X 7  
1uF\_0201\_X5R X 1



1021 (DVT1.1) change to X5R

# Reserve for PWR

|   |            |                    |            |                                 |                  |
|---|------------|--------------------|------------|---------------------------------|------------------|
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|   |            |                    |            | Document Number                 | 0.1              |
|   |            |                    |            | Date: Monday, February 08, 2021 | Sheet 102 of 121 |
|   |            |                    |            | LA-K661P                        |                  |

Main Func = VGA CORE

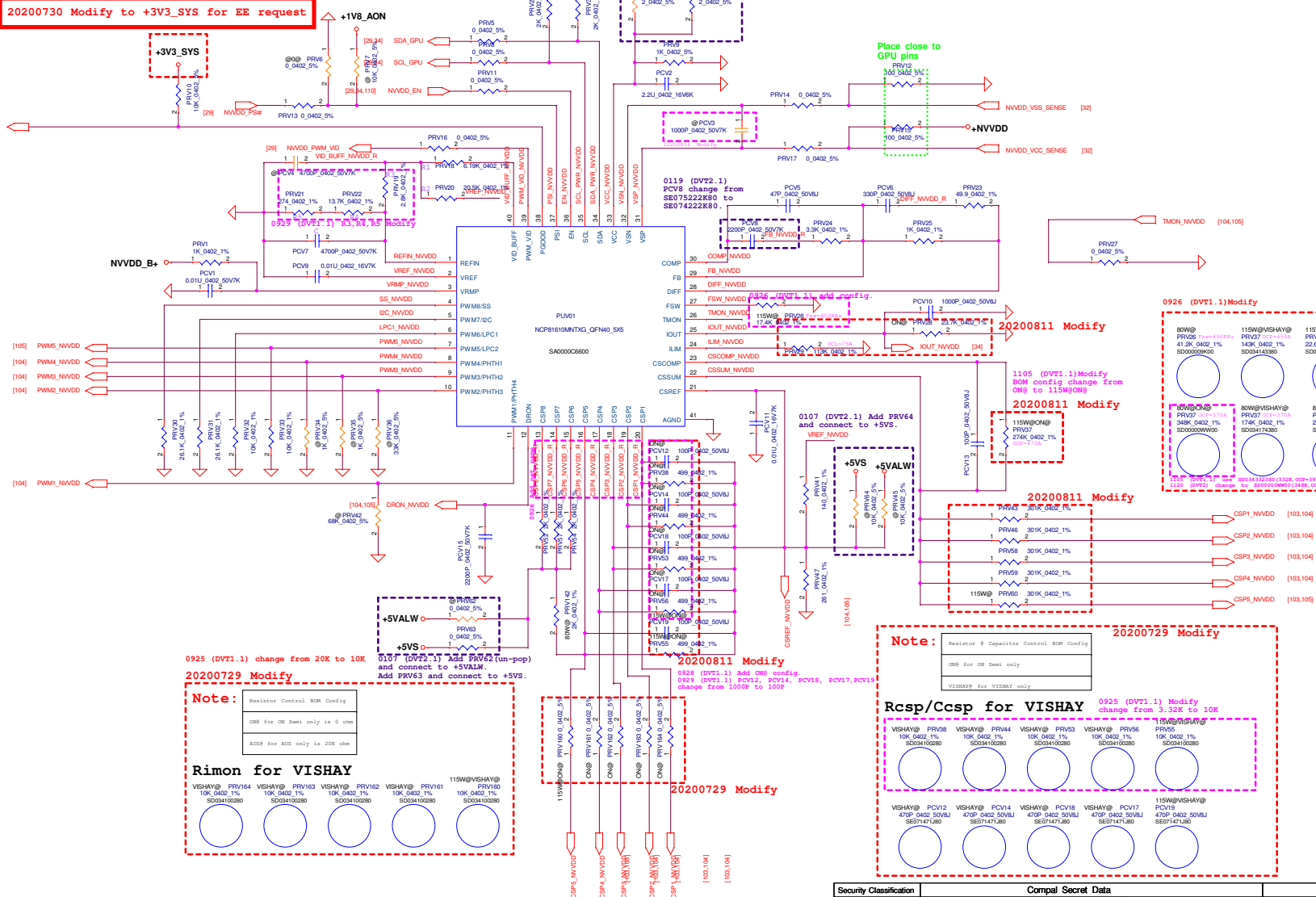
20200803 Modify to +3VALW for EE request

20200730 Modify to +3V3\_SYS for EE request

GN20\_E3  
TGP 115W\_5PH  
EDPc 99A  
EDPp 375A  
Fsw=450K

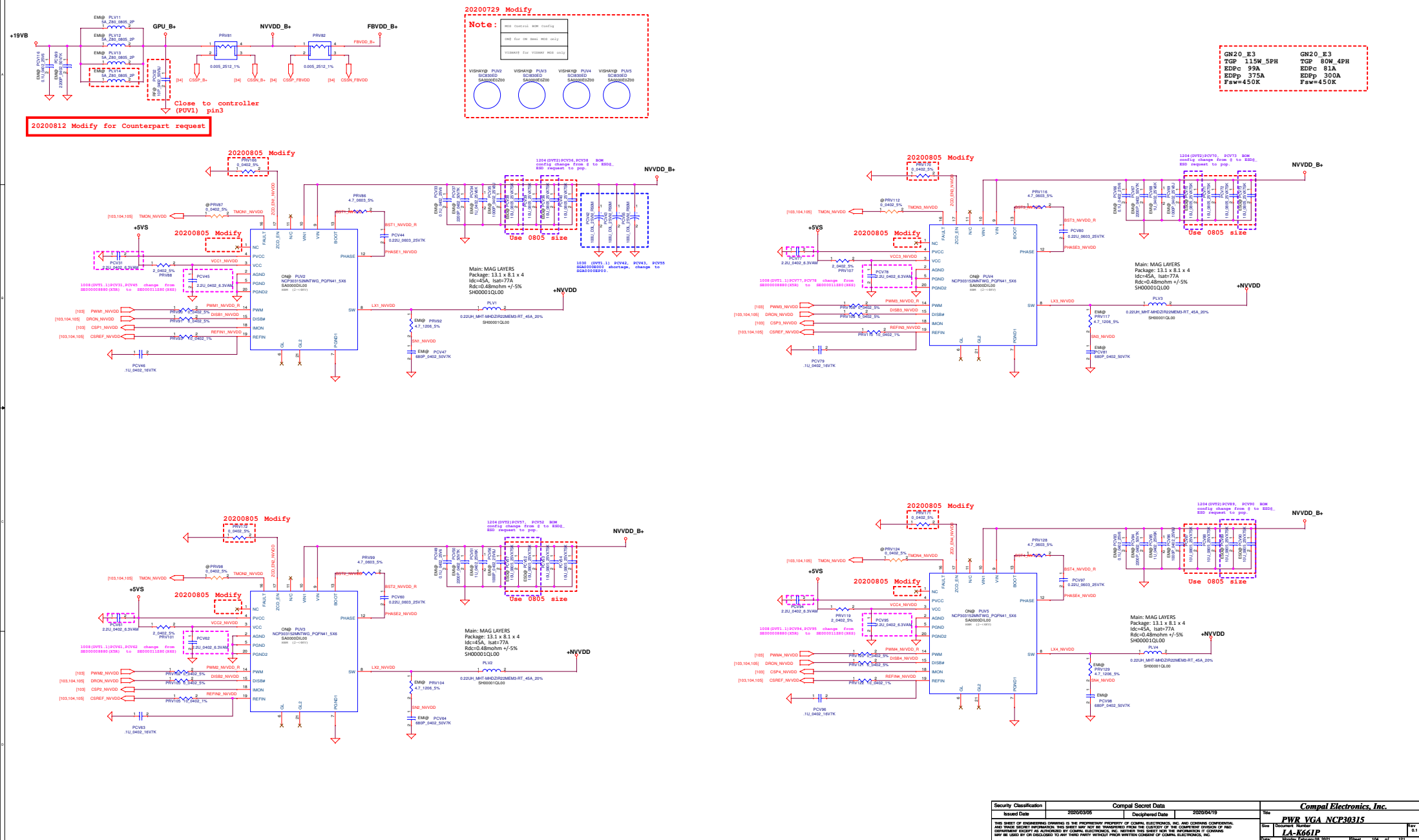
GN20\_E3  
TGP 80W\_4PH  
EDPc 81A  
EDPp 300A  
Fsw=450K

| Config |       |
|--------|-------|
| Vmin   | 0.3   |
| Vmax   | 1.3   |
| Vboot  | 0.75  |
| R1     | 6.19K |
| R2     | 20.5K |
| R3     | 2.8K  |
| R4     | 13.7K |
| R5     | 274   |
| C      | 4.7n  |



| Security Classification   | 2020/03/05 | Compal Secret Data | 2020/04/19 |
|---|------------|--------------------|------------|
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| Compal Electronics, Inc.  |            |                    |            |
| PWR VGA_NCP81611MNTXG   |            |                    |            |
| Rev 0.1   |            |                    |            |
| Date: Monday, February 06, 2021 Sheet 105 of 121  |            |                    |            |

**Main Func = GPU\_CORE SW (1-4PH)**





Main Func = GPU\_CORE SW(5PH)

20200729 Modify

Note:

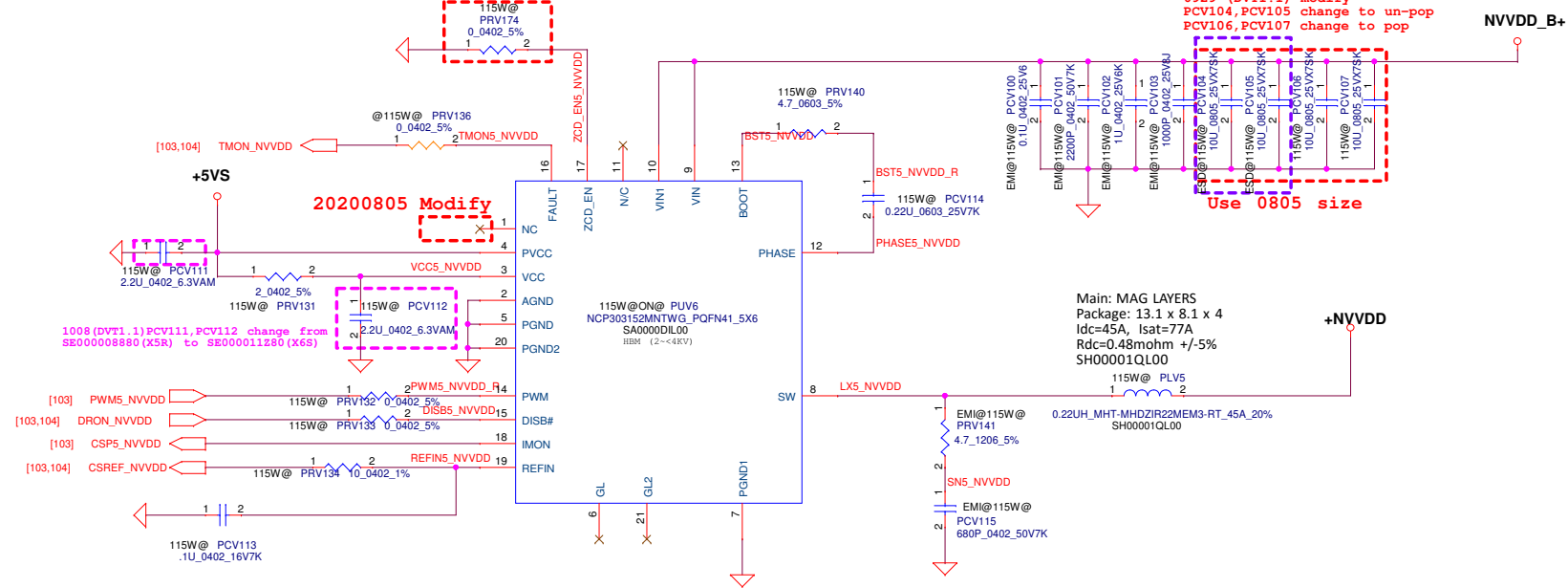
|                          |
|--------------------------|
| MOS Control BOM Config   |
| ON# for ON Semi MOS only |
| AOS# for AOS MOS only    |



20200805 Modify

115W@  
PRV174  
0.0402\_5%

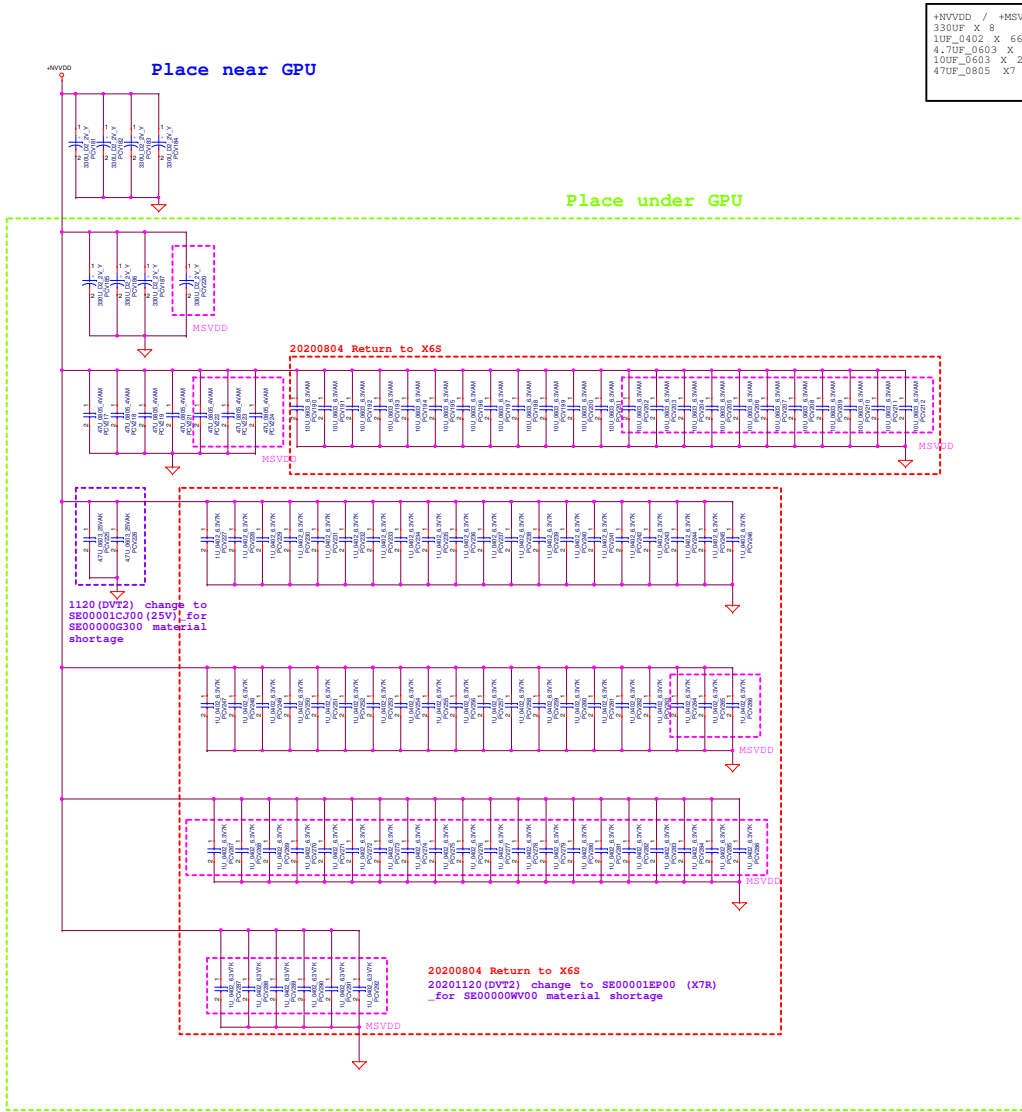
1204(DVT2)PCV104, PC105 BOM config change from @115W# to ESD@115W\_ ESD request to pop.  
0929 (DVT1.1) modify PCV104,PCV105 change to un-pop PCV106,PCV107 change to pop



|   |            |                    |            |                                 |                  |
|---|------------|--------------------|------------|---------------------------------|------------------|
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|   |            |                    |            | LA-K661P                        | Rev 0.1          |
|   |            |                    |            | Date: Monday, February 08, 2021 | Sheet 105 of 121 |

# Reserve for PWR

|   |            |                    |            |                          |     |
|---|------------|--------------------|------------|--------------------------|-----|
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|   |            |                    |            | Document Number          | 0.1 |
| Date: Monday, February 08, 2021   |            | Sheet 106 of 121   |            | LA-K661P                 |     |



+NVVDD / +MSVDD  
330UF X 8  
10UF\_0402 X 66  
4.7UF\_0603 X 2  
10UF\_0603 X 23  
47UF\_0805 X 7

DG-09845-001\_v01  
+NVVDD  
330UF X 3  
10UF\_0402 X 37  
4.7UF\_0603 X 2  
10UF\_0603 X 12  
47UF\_0805 X 4  
  
+MSVDD  
330UF X 1  
10UF\_0402 X 29  
10UF\_0603 X 11  
47UF\_0805 X 2

Main Func =+FBVDDQ

Add PCW42 to GND for EE request  
20200731

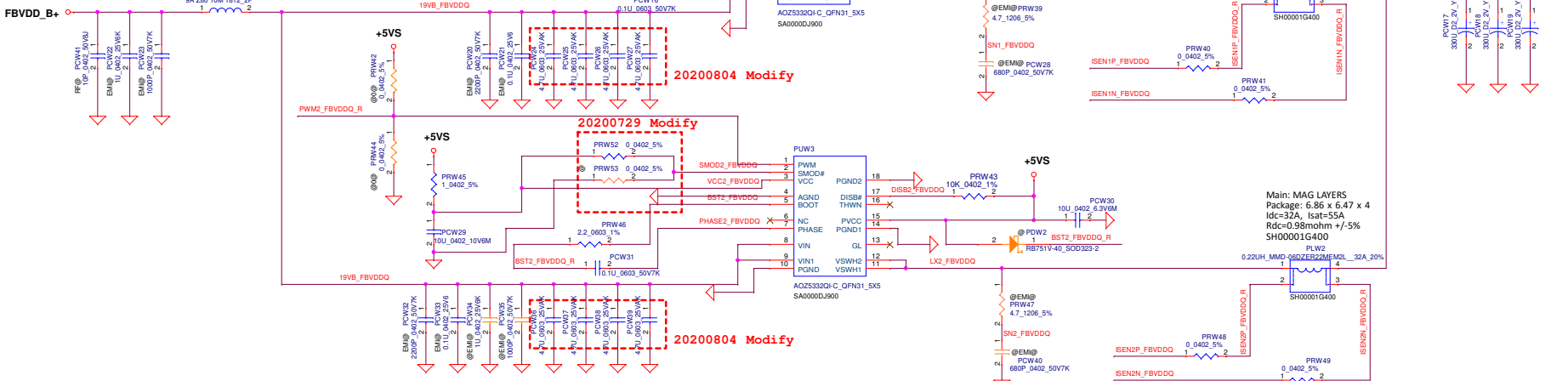
Modify PSI Pull-High directly  
for EE request  
20200804

Change PQW1 for EE request  
20200810

+FBVDDQ  
Vout = 1.25V - 1.35V  
EDPc 25A  
EDPp 33A  
OCP=48.96A  
OVP 2.09 V (155%)  
FSW=300KHz

$$V_{out} = 2 * [(PRW26 / PRW27) / (PRW19 + (PRW26 / PRW27))]$$

P0:high P8:low



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|---|--|--|---------------------------|--|------------------|--|----------------|--|
| Issued Date   |  |  | 2020/03/05                |  | 2020/04/19       |  | PWR +1.35V RAM |  |
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# Reserve for PWR

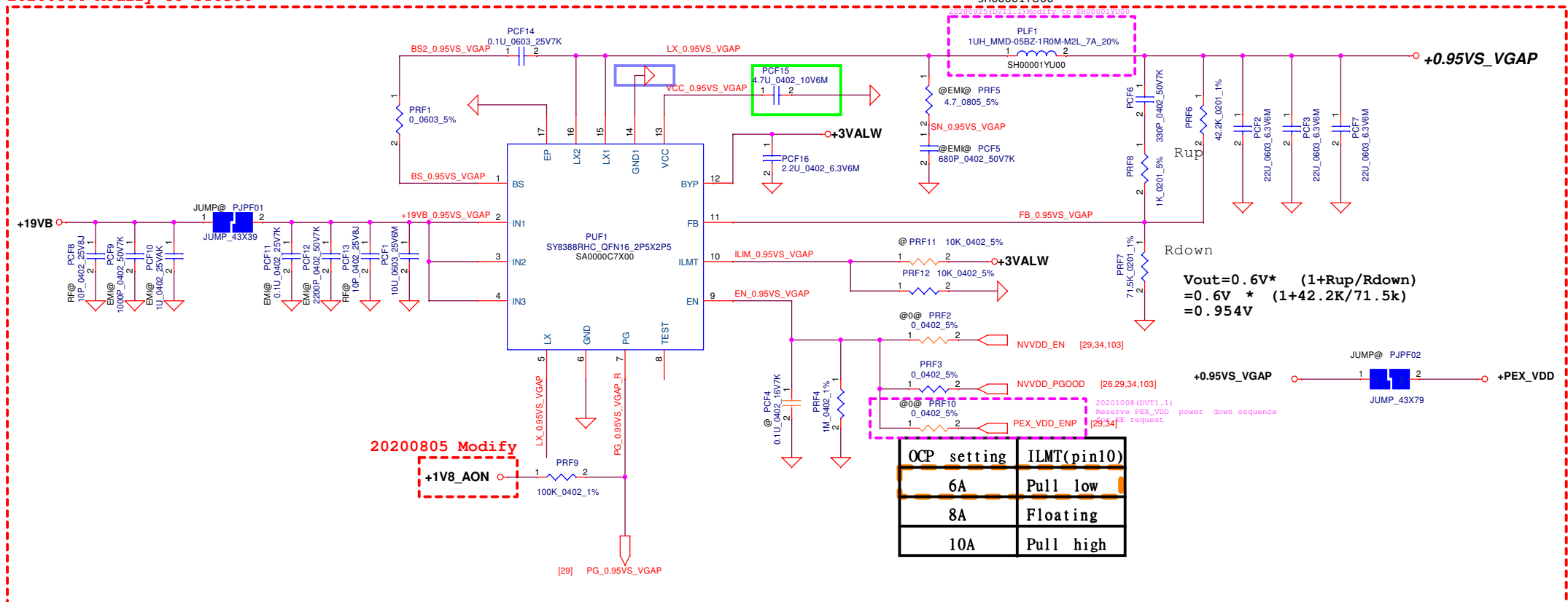
|   |            |                           |            |                          |            |
|---|------------|---------------------------|------------|--------------------------|------------|
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# Main Func =+0.95VS\_VGAP

Input Current: 0.974A  
0.954V\*3.59A/0.85/9V=0.448A

20200925 Modify to SY8388 (DVT1.1)

20200804 Modify to SY8386



+0.95VS\_VGAP  
TDC 3.59A  
Peak Current 4.73A  
OCP Current 6A fix byl C  
Fsw=500KHz

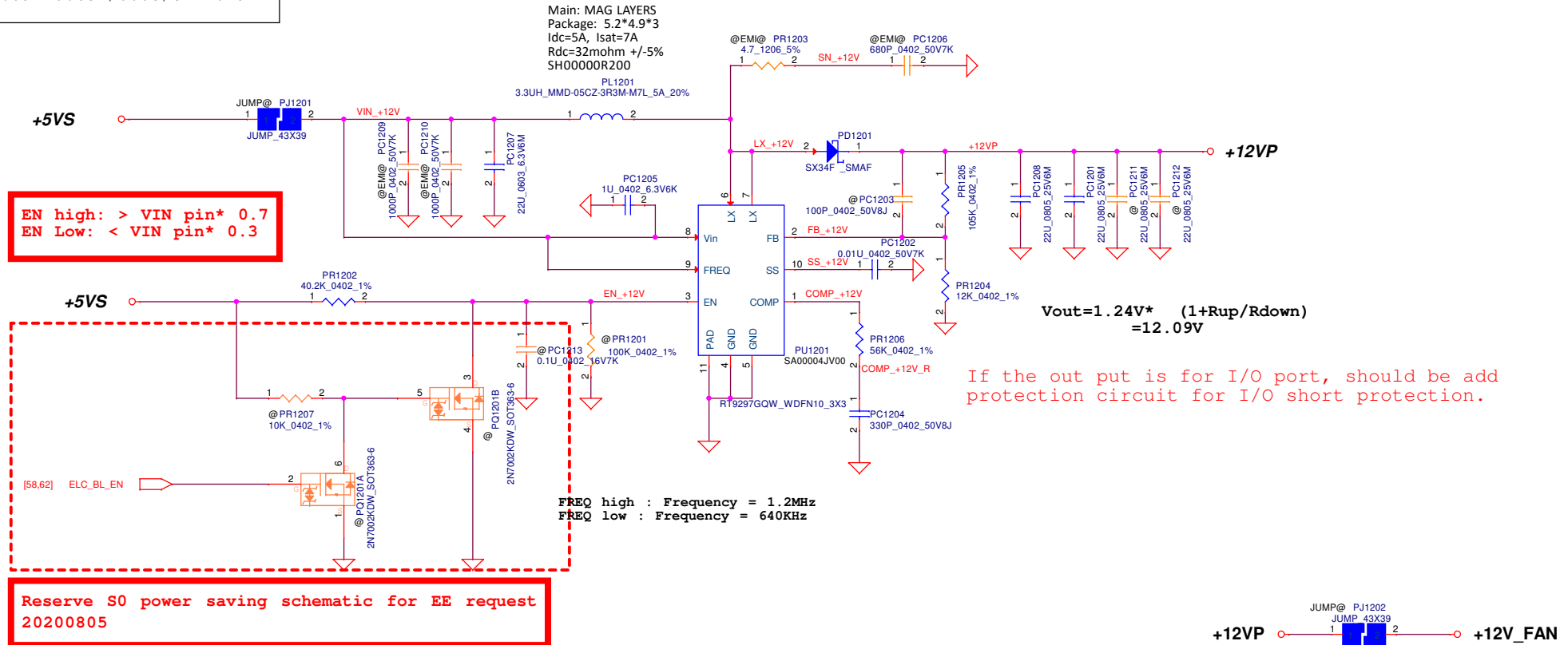
MAG LAYERS  
MMD-05BZ-1R0M-M2L  
Package: 5.49 x 5.18 x 2  
Idc=7A, Isat=13.7A  
Rdc=18.9mohm +/-5%  
SH00001YU00

# Main Func =+12VP\_FAN

Add a switch circuit to turn off the +12V\_VIN if need.

Input Current: 1.792A  
 $12.09V \times 0.63A / 0.85 / 5V = 1.792A$

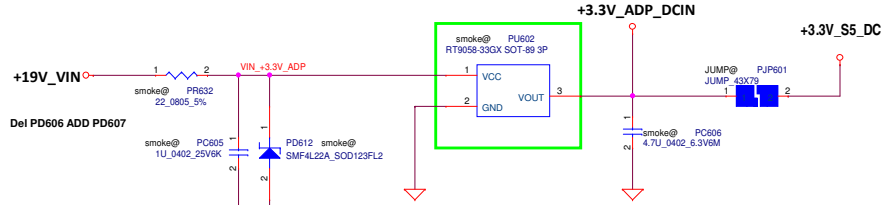
+12VP  
Vout = 12.09 V  
TDC 0.63A  
Peak Current 0.9A  
Current limit 3A  
FSW=1.24MHz



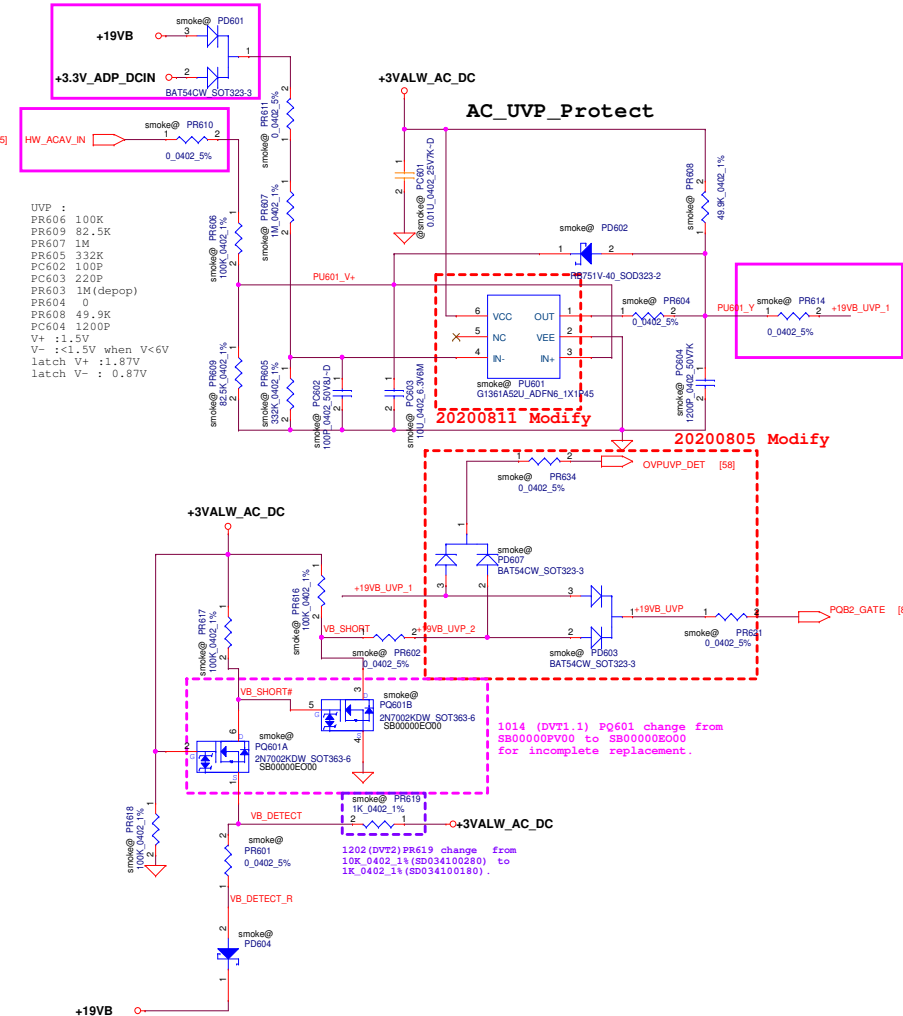
|   |                           |                    |            |                          |  |
|---|---------------------------|--------------------|------------|--------------------------|--|
| Security Classification   |                           | Compal Secret Data |            | Compal Electronics, Inc. |  |
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| Size  | Document                  | Number             | Rev        | LA-K661P                 |  |
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# Main Func = Smokeless UVP

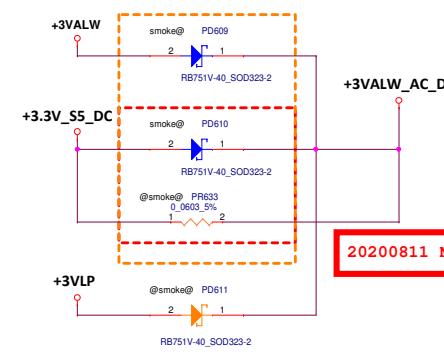
confirm PUS801 and PUS01 compare which is better  
20190515



## AC\_UVP\_Protect Barrel disconnct detect (co-lay unpop)

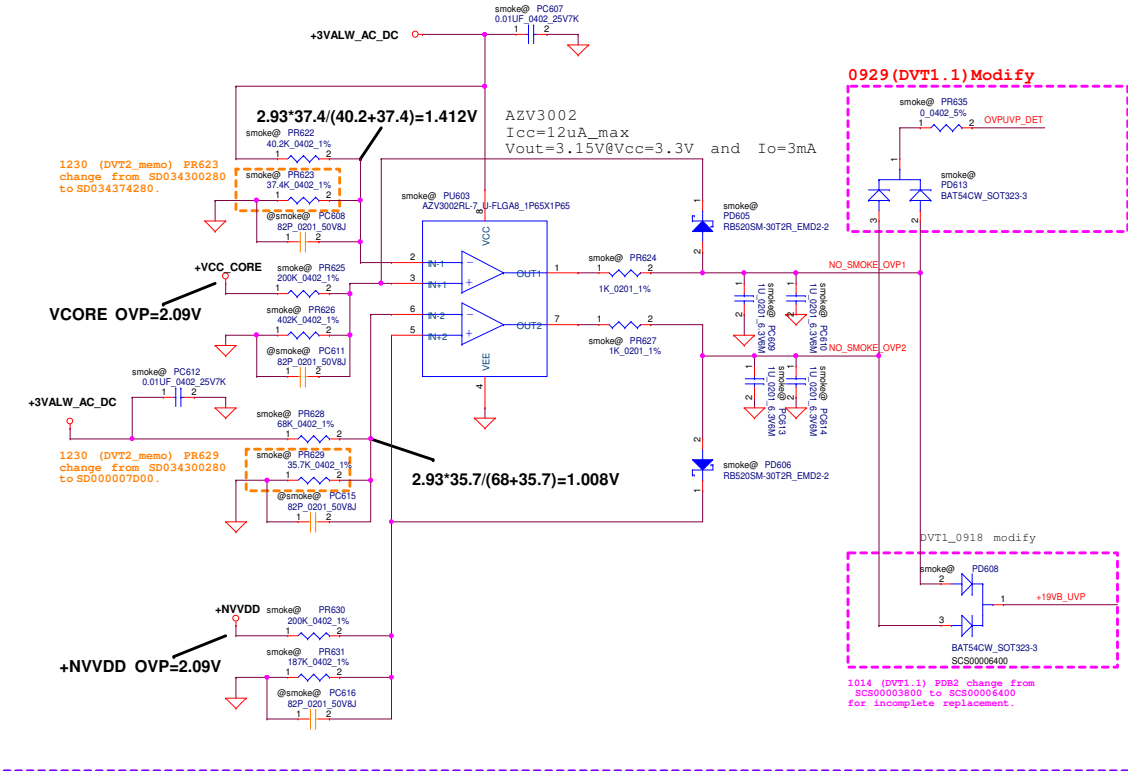


1230 (DVT2\_memo) PD609, PD610 change to pop.  
PR633 change to un-pop



20200811 Modify for Counterpart request

EVT NEW ADD  
1120 (DVT2) OVP circuit un-pop.  
1127 (DVT2) OVP circuit pop.



0929 (DVT1.1) Modify

DVT1\_0918 modify

1014 (DVT1.1) PD601 change from SB000009V00 to SB000009V00 for incomplete replacement.

1014 (DVT1.1) PD602 change from SB000009V00 to SB000009V00 for incomplete replacement.

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# Reserve for PWR

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# Reserve for PWR

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# Reserve for PWR

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# Reserve for PWR

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# Reserve for PWR

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# Reserve for PWR

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## Version Change List ( P. I. R. List )

Page 1

| Item | Page# | Title                      | Date | Request Owner | Issue Description               | Solution Description   | Rev. |
|------|-------|----------------------------|------|---------------|---------------------------------|--|------|
| 1    | 82    | PWR_DCIN / BATT CONN / OTP | 7/29 | EE            |                                 | PR40 change from 1K to 0 ohm                                       | X01  |
| 2    | 85    | PWR_CHARGER (ISL95522A)    | 7/29 | PWR           | For Voltge Spike                | Change PDB1 location to PRB4 pin4                                  | X01  |
| 3    | 90    | PWR_+1.8VALWP              | 7/29 | PWR           | For NV update spec              | Change PU1801 to SY8388<br>Change PL1801                           | X01  |
| 4    | 101   | PWR_+VCORE DECOUPLING      | 7/29 | PWR           | For Intel spec                  | Change CPU capacitor to meet Intel spec                            | X01  |
| 5    | 103   | PWR_GPU_CORE IC            | 7/29 | PWR           | For NVVDD Power stage co-layout |  | X01  |
| 6    | 108   | PWR_GPU_VRAM               | 7/29 | PWR           | Disable DCM Mode                | Change PRW50 And PRW52 to POP<br>Change PRW51 And PRW53 to NON-POP | X01  |
| 7    | 103   | PWR_GPU_CORE IC            | 7/23 | EE            | For EE request                  | Change NVVDD_PGOOD pull high to +3V3_SYS                           | X01  |
| 8    | 82    | PWR_DCIN / BATT CONN / OTP | 7/31 | ME            |                                 | Modify DCIN PIN Defined  | X01  |
| 9    | 108   | PWR_GPU_VRAM               | 8/3  | EE            | For EE request                  | Add PCW42  | X01  |
| 10   | 103   | PWR_GPU_CORE IC            | 8/3  | EE            | For EE request                  | Change SDA_GPU And SCL_GPU pull high to +3VALW                     | X01  |

|   |            |                    |            |         |                           |
|---|------------|--------------------|------------|---------|---------------------------|
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| Issued Date   | 2020/03/05 | Deciphered Date    | 2018/12/31 | PWR PIR |                           |
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| Item | Page# | Title  | Date | Request Owner | Issue Description | Solution Description | Rev. |
|------|-------|--------|------|---------------|-------------------|----------------------|------|
| 1    | 92    | +VCCIO | 0916 | EE            |                   |                      |      |
| 2    |       |        |      |               |                   |                      |      |
| 3    |       |        |      |               |                   |                      |      |
| 4    |       |        |      |               |                   |                      |      |
| 5    |       |        |      |               |                   |                      |      |
| 6    |       |        |      |               |                   |                      |      |
| 7    |       |        |      |               |                   |                      |      |
| 8    |       |        |      |               |                   |                      |      |
| 9    |       |        |      |               |                   |                      |      |
| 10   |       |        |      |               |                   |                      |      |



| Item | Page# | Title                   | Date  | Request Owner | Issue Description                                 | Solution Description   | Rev. |
|------|-------|-------------------------|-------|---------------|---|--|------|
| 1    | 103   | PWR_GPU_CORE IC         | 11/20 | PWR           | Modify for debug                                  | 1. PRV14 pin1 connect net change to VSN_NVVDD;<br>pin2 change to NVVDD_VSS_SENSE.<br>2. PRV17 pin1 connect net change to VSP_NVVDD;<br>pin2 change to NVVDD_VCC_SENSE. | X02  |
| 2    | 107   | PWR_GPU_CORE DECOUPLING | 11/20 | PWR           | PPM request change the meterial for non-tradable. |  |      |
| 3    |       |                         |       |               |   |  |      |
| 4    |       |                         |       |               |   |  |      |
| 5    | 98    | P098-PWR_CPU_CORE_SW    |       |               |   |  |      |
| 6    |       |                         |       |               |   |  |      |
| 7    |       |                         |       |               |   |  |      |
| 8    |       |                         |       |               |   |  |      |
| 9    |       |                         |       |               |   |  |      |
| 10   |       |                         |       |               |   |  |      |

|   |            |                    |            |                                 |  |                  |     |
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