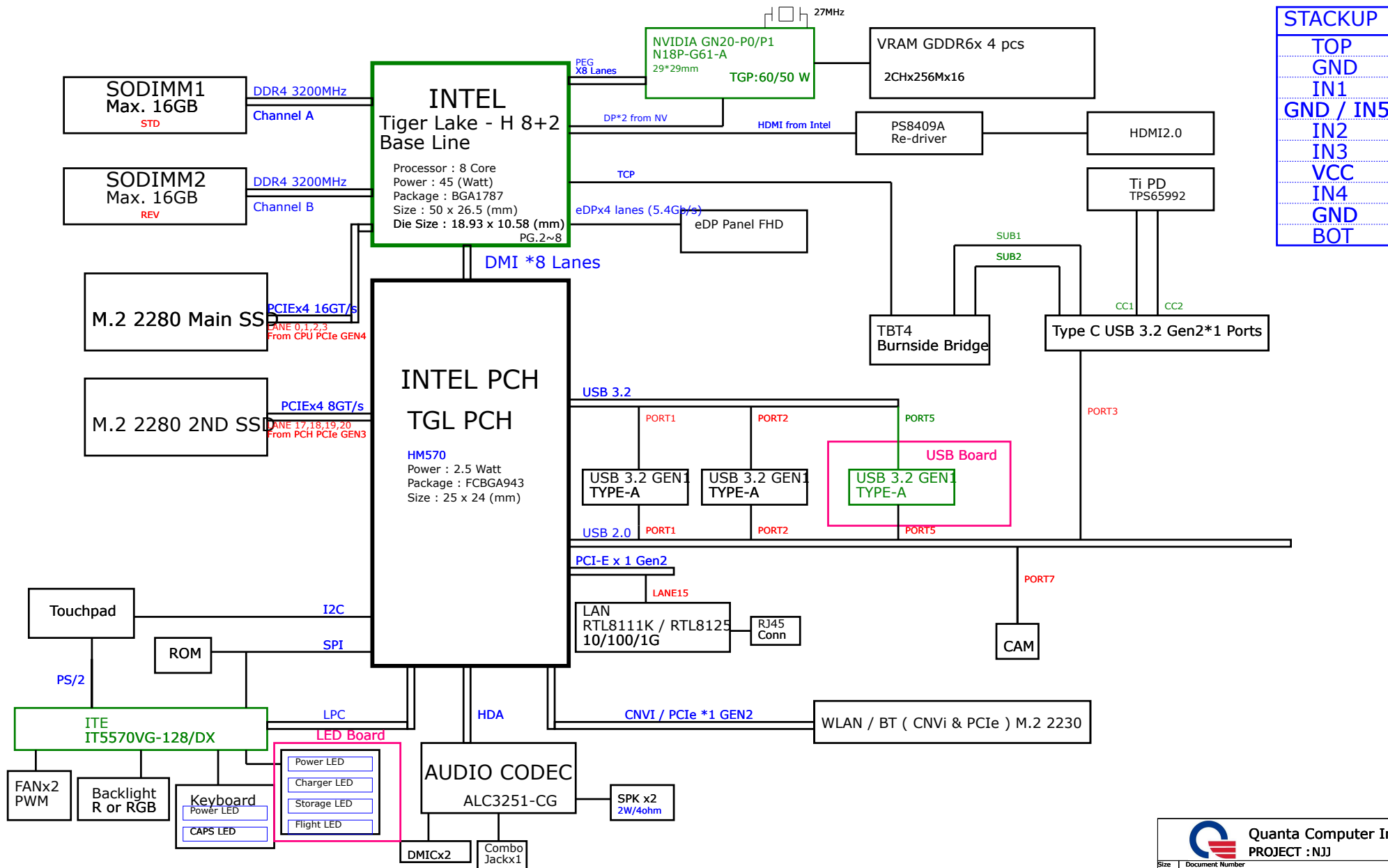


ASUS FX506H GN20-P0/P1 N18P-G61-A Block Diagram

01



Model
FX506HE
FX506HHR

REV

CHANGE LIST

Item	Stage	Page	Owner	Change explanation
01	ER	10	EE	ER01 : U6004 BIOS ROM SI & SO PIN SWAP for no load code issue.
02	ER	36	EE	ER02 : TUI1&TUI2 change power rail from +3V to 51225_LDO3.
03	ER	12	EE	ER03 : PCIe CLK for Main SSD GEN4 change from PCIe7 to PCIe0 follow PDG 6.1.2
04	ER	13	EE	ER04 : PCIe CLKREQ_SSD# change from CLKREQ5# to CLKREQ0#, follow ER03 setting
05	ER	34	EE	ER05 : Add PCIe WLAN support.
06	ER	10	EE	ER06 : C6107 & C6108 chnage from 15P to 12P for X'tal Accuracy.
07	ER	29	EE	ER07 : TQ1&TR35 mount, TR42&TR97 un-mount for Tpw timing issue.
08	ER	30	EE	ER08 : TR58/TR60/TR59/TR61 change from 5% to 1% for ADCIN1/ADCIN2.
09	ER	16	EE	ER09 : VCS5T change to SUSON Power rail. VCS5TG change to RUN_ON Power rail.
10	ER	11	EE	ER10 : Remove excess 0 ohm for CPU_C10_GATE#
11	ER	41	EE	ER11 : HDMI TMD5 Resistor change from 5.1K to 0R, and HL1 change to HCM2012GD500AE base on EA report.
12	ER	14	EE	ER12 : Remove MB ID resistor.
13	ER	11/13	EE	ER13 : DGPU_PWR_EN change GPIO from GPP_110 to GPP_G3; DGPU_HOLD_RST# change from GPP_19 to GPP_G4
14	ER	22	EE	ER14 : DP IN HPD level shift change to MBT3904 and remove pull low 100K, follow Intel CRB circuit.
15	ER	34/42	EE	ER15 : Remove LQ1 and Q6013 for LAN&WLAN not support wake function.
16	ER	12	EE	ER16 : C6109 & C6110 change from 18P to 15P for X'tal Accuracy.
17	ER	22	EE	ER17 : Change VR5146&VR5062 from 1K to 200ohm for meet MMBT3904 spec.
18	ER	37	EE	ER18 : Change AD2,AD3,AD5,AD6,AD7 from BC01025B200 to BC054151200 for EMI request.
19	ER	7	EE	ER19 : C6007&C6009 change from 22uF to 47uF for VRTT
20	ER	22	EE	ER31 : VCS131 change from 220u to 330u for FBVDDQ ripple. Add VCS735 for N18P FBVDDQ ripple.
21	ER	28	EE	ER32 : Change H47 footprint for EMI issue
22	ER	46~56	Power	ER01: Remove output short pad.
23	ER	43~58	Power	ER02: 0ohm change to short pad.
24	ER	55	Power	ER03: Net +1.8V_GPU_AON change to +1.8V_GPU_AON-1.
25	ER	52	Power	ER04: Net +1.8V_GPU_AON change to +1.8V_GPU_AON-1.
26	ER	56	Power	ER05: For 1.8V_GPU timing, PR7008 change 47K & PC7010 change 470P & PC7011 change 6.8nF.
27	ER	49	Power	ER06: For 5V timing, PC1021 change 1000pF
28	ER	52	Power	ER07: For NVDD timing, PR6004 change 130Kohm.
29	ER	55	Power	ER08: PC6520 change to mount for FBVDDQ ripple.
30	ER	56	Power	ER09: Discharge PR7020 net +0.95V_GPU change to +PEX_VDD.
31	ER	44	Power	ER10: Stuff PEC7/PEC11, PE13/PEC14, PEC16/PEC26 to reduce 200~230MHz power broadband noise for H81 SKU.
32	ER	44	Power	ER11: Stuff PER4/PEC12, PER5/PEC15, PER7/PEC27 Snubber circuit to reduce 200~230MHz power broadband noise.
33	ER	45	Power	ER12: Pull high circuit net form VCCAUX_VID0 & VCCAUX_VID1 to RT6543_VID0 & RT6543_VID1.
34	ER	47	Power	ER13: Pull high circuit net form VCCAUX_VID0 & VCCAUX_VID1 to Z264_VID0 & Z264_VID1.
35	ER	45	Power	ER14: PR424 change no-mount for VRTT test result.
36	ER	43	Power	ER15: Change PC15 from no-mount change to 33nF to correct L-DCK matching for H81.
37	ER	43	Power	ER16: Change PR16 499 change to 536ohm to correct DCLL/OCF for H81 & H61.
38	ER	43	Power	ER17: Change PR25 2.49k change to 2.7kohm to correct DCLL/OCF for H61.
39	ER	43	Power	ER18: Change PR32 from 110k to 115kohm to correct IMON for H61.
40	PR	11/28	EE	PR01 : Add PANEL_OD support
41	PR	11/13/30	EE	PR02 : Add PD to EC and PCH I2C
42	PR	30	EE	PR03 : Reserve and un-mount TR99,TR100,TR101 for TBT DC S5 leakage.
43	PR	17	EE	PR04 : VIN/VA+ 0201 CAP change to unmount for Pre QS SMT
44	PR	23	EE	PR05 : VCS131 and VCS735 change from 1.4mm to 1.9mm for shortage issue
45	PR	All	EE	PR06 : 0 ohm to shortpad
46	PR	41	EE	PR07 : HDMI re-driver PS8209 change to PS8409 for Jitter Issue
47	PR	06/38	EE	PR08 : CPU_DP10 HPD add level shifter to EC to wake GPU
48	PR	29/30	EE	PR09 : TCPO_RESET# add AND GATE for TBT timing
49	PR	29/30	EE	PR10 : MOS gate change from LDO_3V3 to +3V_S5
50	PR	29/30	EE	PR11 : +1.8V_S5 enable change from 3V_5VPGD to SLP_SUS# follow PDG
51	PR	38	EE	PR12 : Add AND GATE for RSMRST# and SLP_SUS#
52	PR	36	EE	PR13 : TP_INT# add 1000p for EMI
53	PR	41	EE	PR14 : HR30 mount to enable HDMI Pre-Emphasis
54	PR	28	EE	PR15 : reserve EMIC6057/6058/6059 for eDP signal
55	PR	16	EE	PR16 : C9052 change to 10nF for timing
56	PR	35	EE	PR17 : 2nd SSD change from PCIe21~24 to PCIe17~20
57	PR	30	EE	PR18 : Remove TR76/TR79/TR91 for double pull high
58	PR	30	EE	PR19 : Reserved TQ4/TQ7 correct PIN1&3 to reverse PR
59	PR	37	EE	PR20 : AC2/AC20 change from 100p to 680p for EMI CS test
60				
61	PR	43	Power	PR001: PC15 change to CH3334K1B00 for shortage issue.
62	PR	57	Power	PR002: PU7400 change to JONASN parts for P0P1 SKU.
63	PR	43	Power	PR003: PC15 change to 68nF to correct L-DCK matching for H81.
64	PR	43	Power	PR004: PC15 change to 82nF to correct L-DCK matching for H61.
65	PR	43	Power	PR005: PR25 change to 2.61K to correct DCLL/OCF for H61.
66	PR	43	Power	PR006: PR32 change to 110k to correct IMON for H61.
67	PR	46	Power	PR007: +1.8V_S5 enable change to SLP_SUS# for sequence.
68				
01				
02				
03				
04				
05				
06				
07				
08				
09				
10				
11				

DOC NO.

PROJECT MODEL : BKLK/BKLH

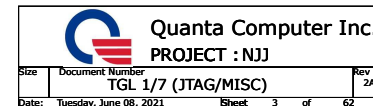
APPROVED BY:

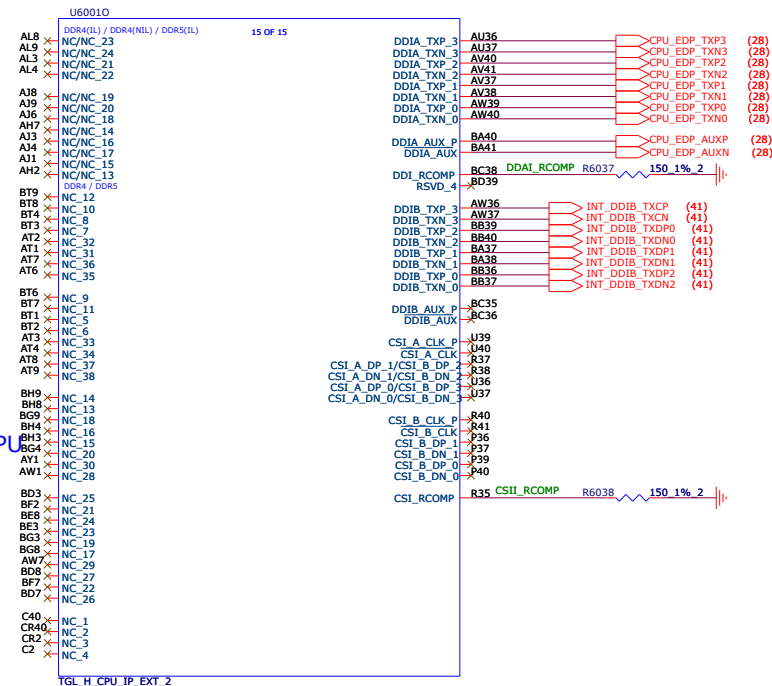
DATE: 2018/01/17

PART NUMBER:

DRAWING BY:

REVISION: 1A

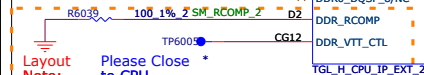




e

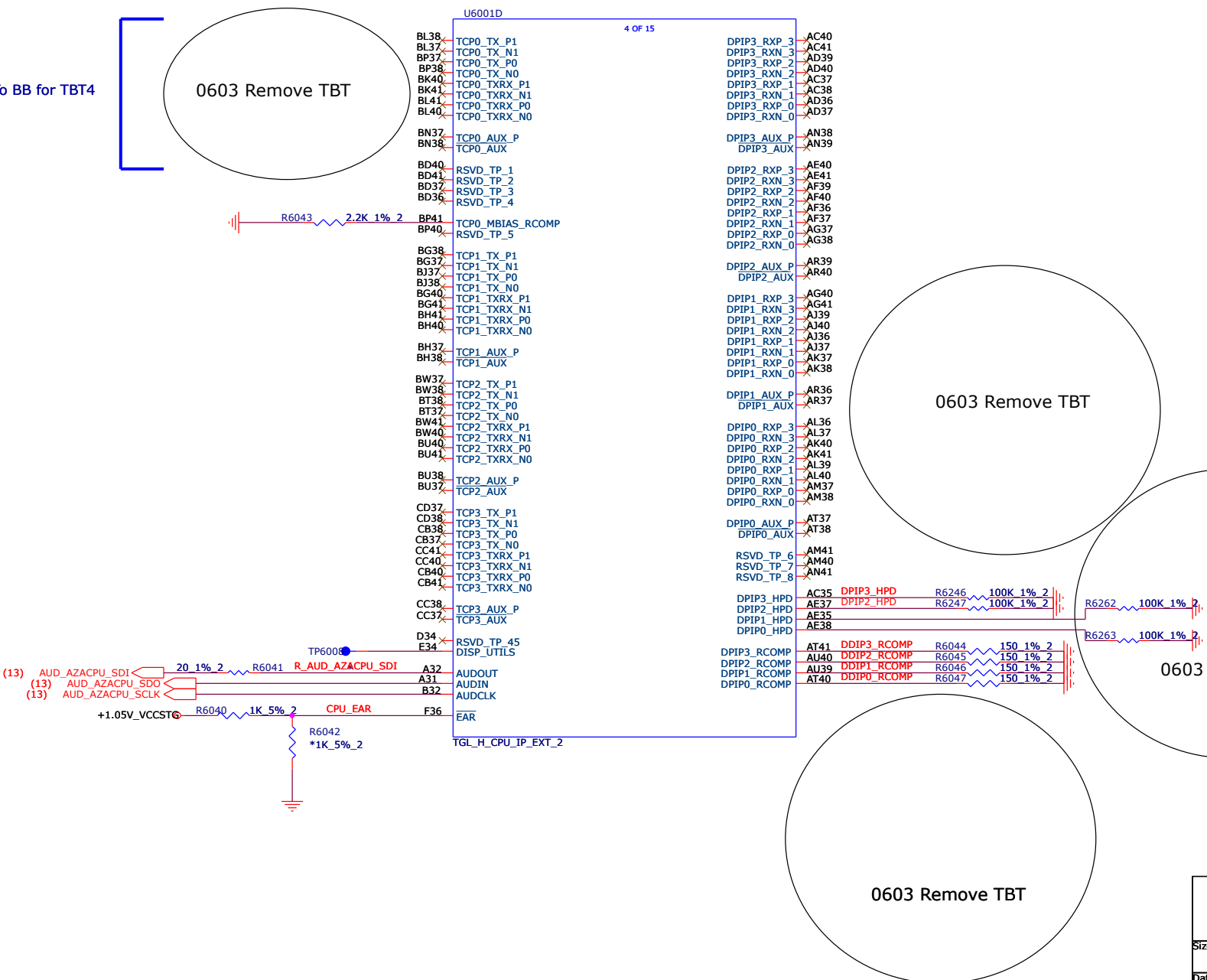
DMI

05



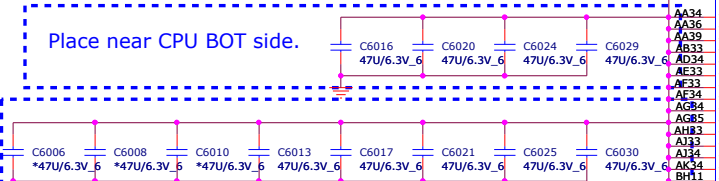
To BB for TBT4

0603 Remove TBT



Follow TGL_H Power Map_1.0(H8+GT1): +VCCIN_AUX=35A

Place near CPU BOT side.

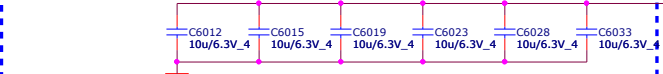


Place under CPU TOP side.



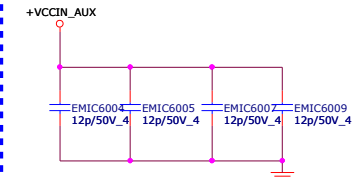
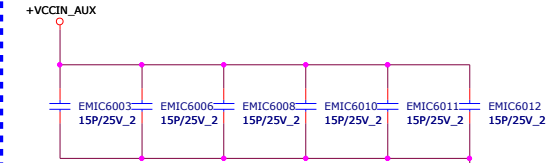
ER19 : C6007&C6009 change from 22uF to 47uF for VRTT

Place under CPU TOP side.



Place under CPU TOP side.

EMC CAPS - PLACE <5MM FROM SOC VCCIN_AUX



12 OF 15

0.97A

0.5A

0.34A

Only to CPU Pull high.

Trace W=10mil

VCCIO_OUT

VCCSTG_12

VCCSTG_OUT1

VCCSTG_OUT23456

VCCSTG_OUT3

VCCSTG_OUT4

VCCSTG_OUT5

VCCSTG_OUT6

VCCIN_AUX_1

VCCIN_AUX_2

VCCIN_AUX_3

VCCIN_AUX_4

VCCIN_AUX_5

VCCIN_AUX_6

VCCIN_AUX_7

VCCIN_AUX_8

VCCIN_AUX_9

VCCIN_AUX_10

VCCIN_AUX_11

VCCIN_AUX_12

VCCIN_AUX_13

VCCIN_AUX_14

VCCIN_AUX_15

VCCIN_AUX_16

VCCIN_AUX_17

VCCIN_AUX_18

VCCIN_AUX_19

VCCIN_AUX_20

VCCIN_AUX_21

VCCSTG_1

VCCSTG_2

VCCSTG_3

VCCSTG_4

VCCSTG_5

VCCSTG_6

VCCSTG_7

VCCSTG_8

VCCSTG_9

VCCSTG_10

VCCSTG_11

VCCSTG_12

VCCSTG_13

VCCSTG_14

VCCSTG_15

VCCSTG_16

VCCSTG_17

VCCSTG_18

VCCSTG_19

VCCSTG_20

VCCSTG_21

VCCSTG_22

VCCSTG_23

VCCSTG_24

VCCSTG_25

VCCSTG_26

VCCSTG_27

VCCSTG_28

VCCSTG_29

VCCSTG_30

VCCSTG_31

VCCSTG_32

VCCSTG_33

VCCSTG_34

VCCSTG_35

VCCSTG_36

VCCSTG_37

VCCSTG_38

VCCSTG_39

VCCSTG_40

VCCSTG_41

VCCSTG_42

VCCSTG_43

VCCSTG_44

VCCSTG_45

VCCSTG_46

VCCSTG_47

VCCSTG_48

VCCSTG_49

VCCSTG_50

VCCSTG_51

VCCSTG_52

VCCSTG_53

VCCSTG_54

VCCSTG_55

VCCSTG_56

VCCSTG_57

VCCSTG_58

VCCSTG_59

VCCSTG_60

VCCSTG_61

VCCSTG_62

VCCSTG_63

VCCSTG_64

VCCSTG_65

VCCSTG_66

VCCSTG_67

VCCSTG_68

VCCSTG_69

VCCSTG_70

VCCSTG_71

VCCSTG_72

VCCSTG_73

VCCSTG_74

VCCSTG_75

VCCSTG_76

VCCSTG_77

VCCSTG_78

VCCSTG_79

VCCSTG_80

VCCSTG_81

VCCSTG_82

VCCSTG_83

VCCSTG_84

VCCSTG_85

VCCSTG_86

VCCSTG_87

VCCSTG_88

VCCSTG_89

VCCSTG_90

VCCSTG_91

VCCSTG_92

VCCSTG_93

VCCSTG_94

VCCSTG_95

VCCSTG_96

VCCSTG_97

VCCSTG_98

VCCSTG_99

VCCSTG_100

VCCSTG_101

VCCSTG_102

VCCSTG_103

VCCSTG_104

VCCSTG_105

VCCSTG_106

VCCSTG_107

VCCSTG_108

VCCSTG_109

VCCSTG_110

VCCSTG_111

VCCSTG_112

VCCSTG_113

VCCSTG_114

VCCSTG_115

VCCSTG_116

VCCSTG_117

VCCSTG_118

VCCSTG_119

VCCSTG_120

VCCSTG_121

VCCSTG_122

VCCSTG_123

VCCSTG_124

VCCSTG_125

VCCSTG_126

VCCSTG_127

VCCSTG_128

VCCSTG_129

VCCSTG_130

VCCSTG_131

VCCSTG_132

VCCSTG_133

VCCSTG_134

VCCSTG_135

VCCSTG_136

VCCSTG_137

VCCSTG_138

VCCSTG_139

VCCSTG_140

VCCSTG_141

VCCSTG_142

VCCSTG_143

VCCSTG_144

VCCSTG_145

VCCSTG_146

VCCSTG_147

VCCSTG_148

VCCSTG_149

VCCSTG_150

VCCSTG_151

VCCSTG_152

VCCSTG_153

VCCSTG_154

VCCSTG_155

VCCSTG_156

VCCSTG_157

VCCSTG_158

VCCSTG_159

VCCSTG_160

VCCSTG_161

VCCSTG_162

VCCSTG_163

VCCSTG_164

VCCSTG_165

VCCSTG_166

VCCSTG_167

VCCSTG_168

VCCSTG_169

VCCSTG_170

VCCSTG_171

VCCSTG_172

VCCSTG_173

VCCSTG_174

VCCSTG_175

VCCSTG_176

VCCSTG_177

VCCSTG_178

VCCSTG_179

VCCSTG_180

VCCSTG_181

VCCSTG_182

VCCSTG_183

VCCSTG_184

VCCSTG_185

VCCSTG_186

VCCSTG_187

VCCSTG_188

VCCSTG_189

VCCSTG_190

VCCSTG_191

VCCSTG_192

VCCSTG_193

VCCSTG_194

VCCSTG_195

VCCSTG_196

VCCSTG_197

VCCSTG_198

VCCSTG_199

VCCSTG_200

VCCSTG_201

VCCSTG_202

VCCSTG_203

VCCSTG_204

VCCSTG_205

VCCSTG_206

VCCSTG_207

VCCSTG_208

VCCSTG_209

VCCSTG_210

VCCSTG_211

VCCSTG_212

VCCSTG_213

VCCSTG_214

VCCSTG_215

VCCSTG_216

VCCSTG_217

VCCSTG_218

VCCSTG_219

VCCSTG_220

VCCSTG_221

VCCSTG_222

VCCSTG_223

VCCSTG_224

VCCSTG_225

VCCSTG_226

VCCSTG_227

VCCSTG_228

VCCSTG_229

VCCSTG_230

VCCSTG_231

VCCSTG_232

VCCSTG_233

VCCSTG_234

VCCSTG_235

VCCSTG_236

VCCSTG_237

VCCSTG_238

VCCSTG_239

VCCSTG_240

VCCSTG_241

VCCSTG_242

VCCSTG_243

VCCSTG_244

VCCSTG_245

VCCSTG_246

VCCSTG_247

VCCSTG_248

VCCSTG_249

VCCSTG_250

VCCSTG_251

VCCSTG_252

VCCSTG_253

VCCSTG_254

VCCSTG_255

VCCSTG_256

VCCSTG_257

VCCSTG_258

VCCSTG_259

VCCSTG_260

VCCSTG_261

VCCSTG_262

VCCSTG_263

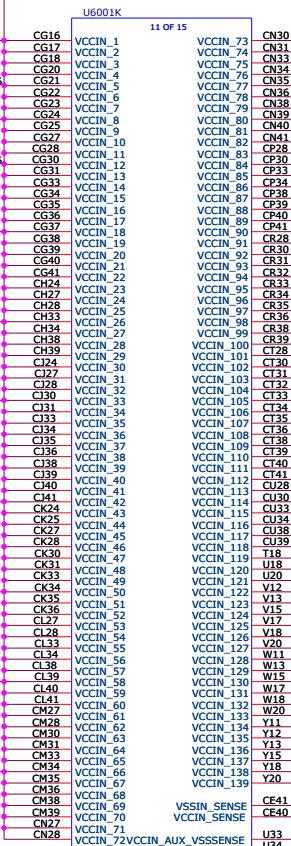
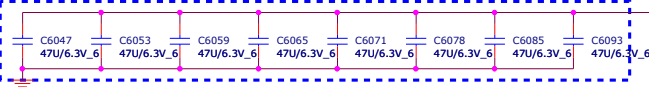
VCCSTG_264

VCCSTG_265

VCCSTG_266

Follow TGL_H Power Map_1.0 to 45W(H8+GT1): +VCCIN=IccMax=87A

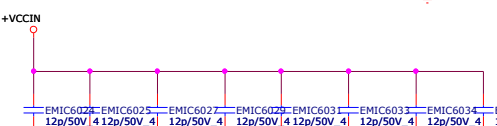
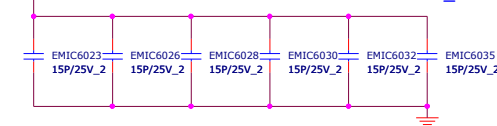
Place under CPU TOP side.



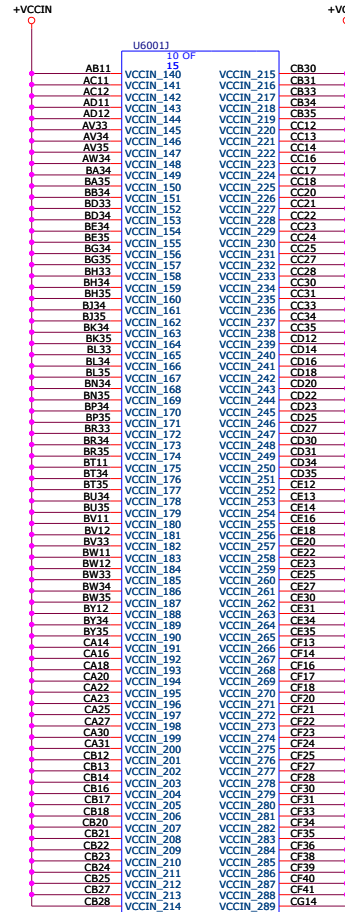
Place under CPU TOP side.

Place under CPU TOP side.

EMC CAPS - PLACE <5MM FROM SOC VCCIN_AUX

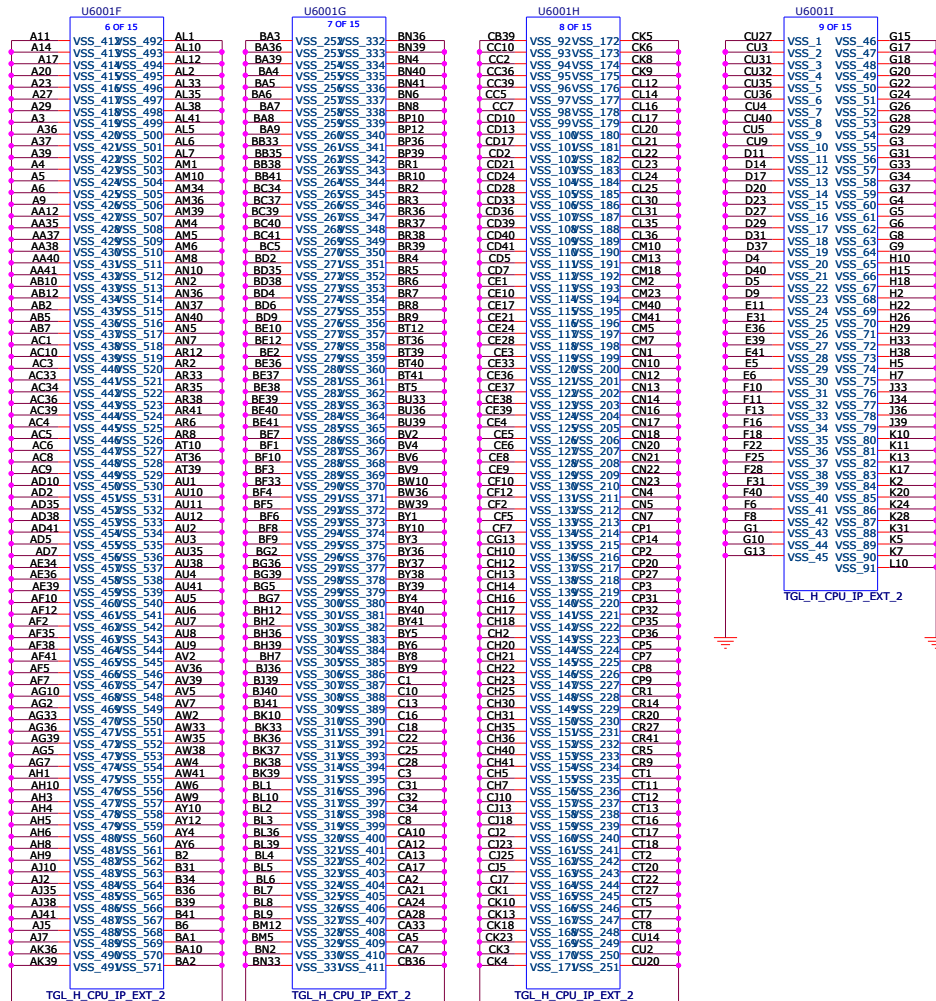


Trace Impedance 50 ohm
Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

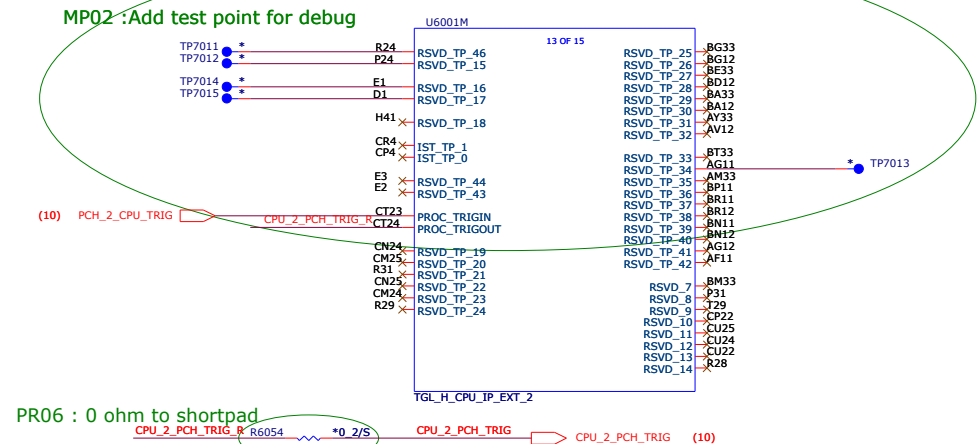


Quanta Computer Inc.
PROJECT : NJJ

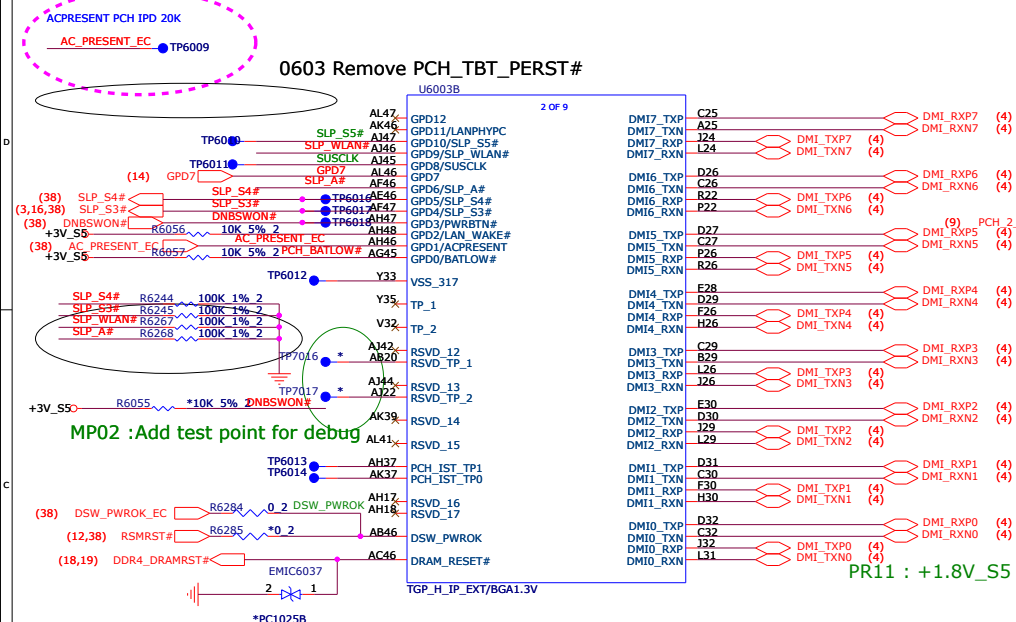
TGL-H Processor (GND)



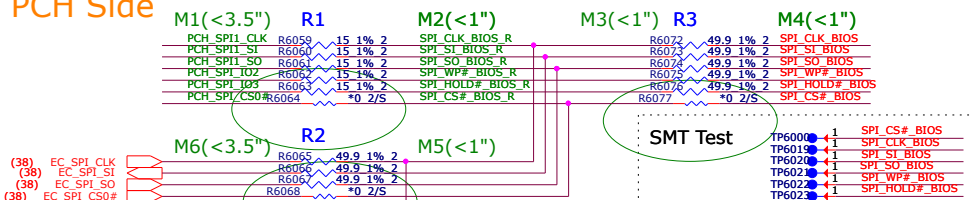
TGL-H Processor (RESERVED, CFG)



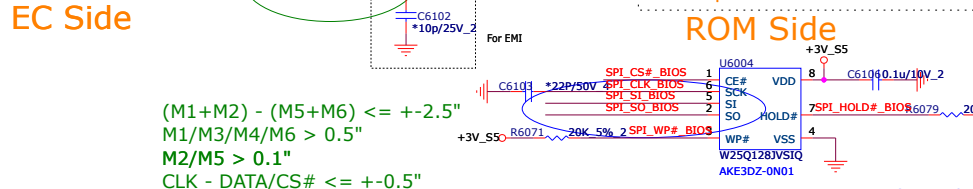
0603 Remove PCH TBT PERST#



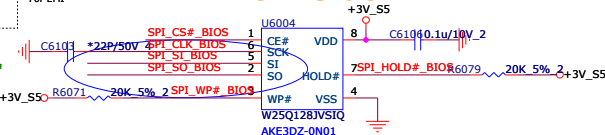
PCH Side



EC Side

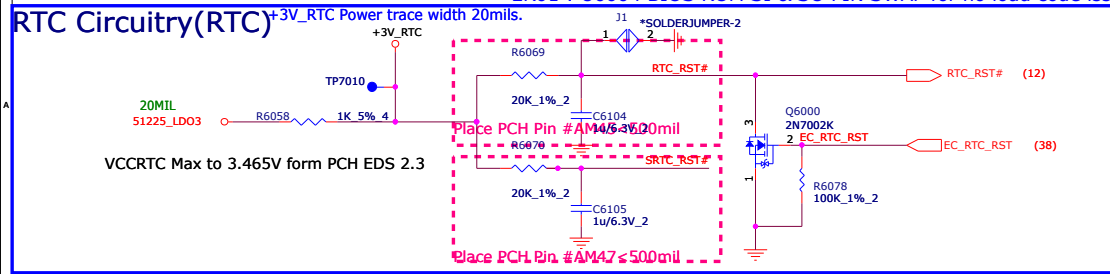


ROM Side



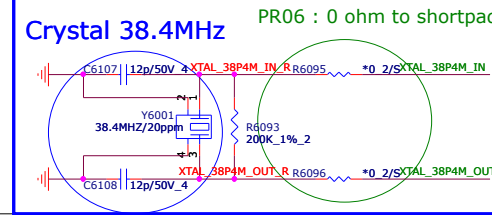
ER01 : U6004 BIOS ROM SI & SO PIN SWAP for no load code issue.

RTC Circuitry(RTC)

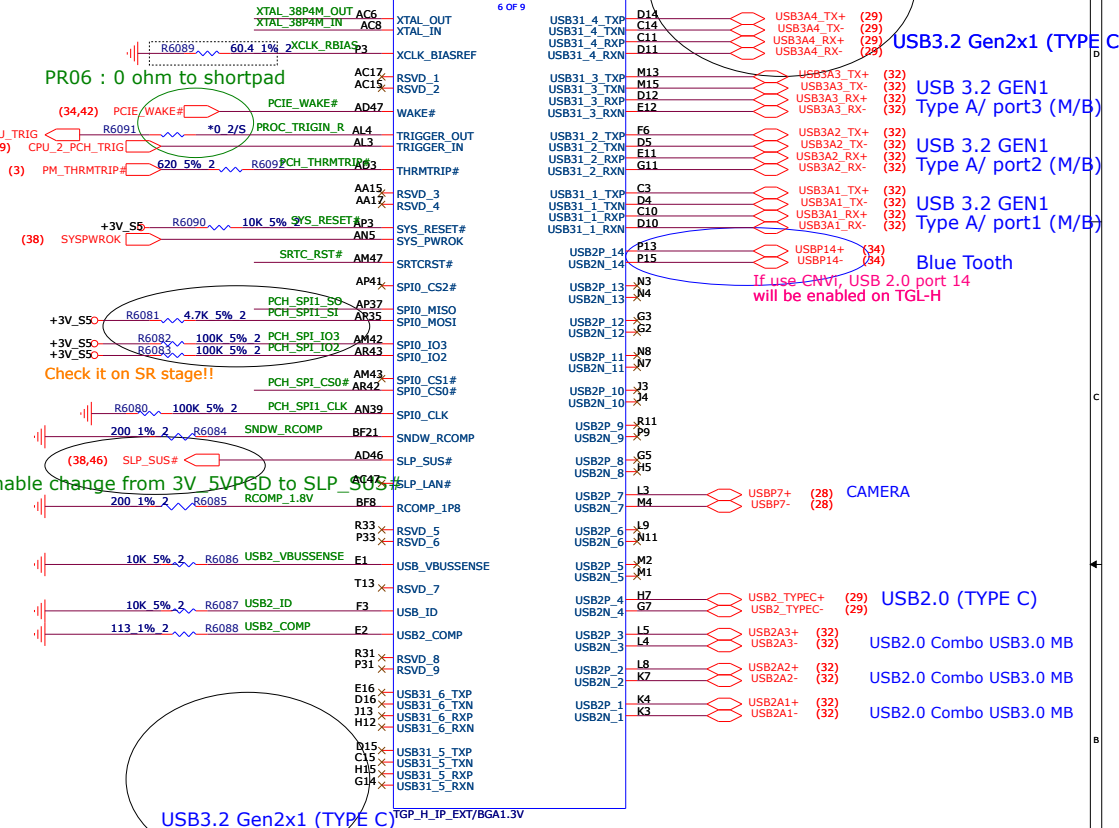


ER06 : C6107 & C6108 chnage from 15P to 12P for X'tal Accuracy.

Crystal 38.4MHz



0603 Add USB3 for Type C

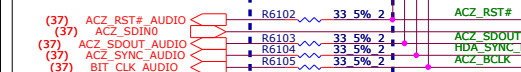


(38) GPIO33_EC R6099 1K 5% 2ACZ_SDOUT
EC Drive High for OVERRIDE

PR01 : Add PANEL_OD support



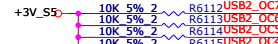
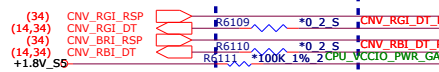
Please near PCH <500mil



TO CPU VIN_AUX
Change INT_HDMI_HPD nat name.... tomm

HPDA --> eDP
HPDB --> INT_HDMI2.0
HPDC --> NA

Please near PCH <500mil



0603 Remove R6256 and TCP0_HPD



U6003C
3 OF 9
AW21 GPP_S7/SNDW4_DATA/DMIC_DATA0
AY20 GPP_S6/SNDW4_CLK/DMIC_CLKA0
BB20 GPP_S5/SNDW3_DATA/DMIC_DATA1
BC20 GPP_S4/SNDW3_CLK/DMIC_CLKA1
BD19 GPP_S3/SNDW2_DATA/DMIC_CLKB1
BE20 GPP_S2/SNDW2_CLK/DMIC_CLKB0
BD18 GPP_S1/SNDW1_DATA
GPP_S0/SNDW1_CLK
AW47 GPP_R19/ISH_GP5
AY45 GPP_R18/ISH_GP4
BA45 GPP_R17/ISH_GP3
BA48 GPP_R16/ISH_GP2
BA47 GPP_R15/ISH_GP1
BC49 GPP_R14/ISH_GP0
AV45 GPP_R13/ISH_GP7
GPP_R12/CLKOUT_48
AR39 GPP_R11/SX_EXIT_HOLDOFF#/ISH_GP6
GPP_R10/ISH_UART0_RTS#/GSP12_CS1#
AU42 GPP_R9/PCIE_LNK_DOWN
BD46 GPP_R8/I2S1_SCLK
AT38 GPP_R7/I2S1_SFRM
BG45 GPP_R6/I2S1_TXD
BF44 GPP_R5/HDA_SDI1/I2S1_RXD
BG44 GPP_R4/HDA_RST#
DE43 GPP_R3/HDA_SDI0/I2S0_RXD/HDACPU_SDI
DE43 GPP_R2/HDA_SDI0/I2S0_TXD/HDACPU_SDO
DE42 GPP_R1/HDA_SYNC/I2S0_SFRM
GPP_R0/HDA_BCLK/I2S0_SCLK/HDACPU_BCLK

AT15 GPP_K11
AR7 GPP_K10/DSP_HPDC/DISP_MISC
AT14 GPP_K9/CORE_VID1
AR8 GPP_K8/CORE_VID0
AT7 GPP_K7/DSP_HPDB/DISP_MISC
GPP_K6/DSP_HPDA/DISP_MISC
GPP_K5/ADR_COMPLETE
AT13 GPP_K4/GSXCLK
AU5 GPP_K3/GSXRESET#
AP15 GPP_K2/GSXIN
AU4 GPP_K1/GSXLOAD
AU3 GPP_K0/GSXOUT

BA2 GPP_J9
BA1 GPP_J8
AU9 GPP_J7/CNV_MFUART2_TXD
GPP_J6/CNV_MFUART2_RXD
GPP_J5/CNV_RGI_RSP/UART0_CTS#
AW4 GPP_J4/CNV_RGI_DT/UART0_TXD
AV4 GPP_J3/CNV_BRI_RSP/UART0_RXD
GPP_J2/CNV_BRI_DT/UART0_RTS#
GPP_J1/CPU_C10_GATE#
GPP_J0/CNV_PA_BLANKING

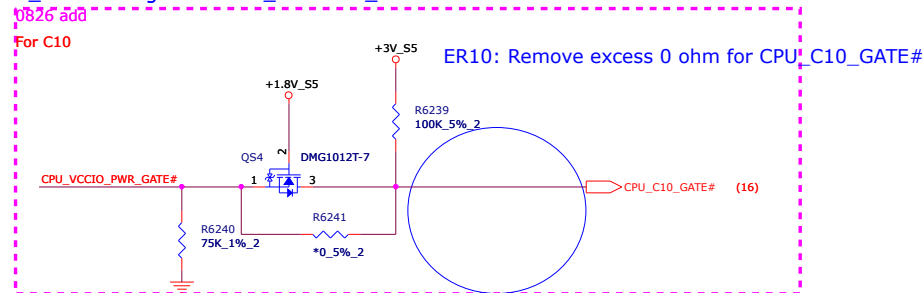
AM7 GPP_I14/USB_OC7#/I2C5_SCL
AP13 GPP_I13/USB_OC6#/I2C5_SDA
AK11 GPP_I12/USB_OC5#/I2C4_SCL
AM13 GPP_I11/USB_OC4#/I2C4_SDA
AL9 GPP_I10
AM8 GPP_I9
AM15 GPP_I8/DDPC_CTRLDATA
AJ6 GPP_I7/DDPC_CTRLCLK
AJ8 GPP_I6/DDPB_CTRLDATA
AH9 GPP_I5/DDPB_CTRLCLK
AK15 GPP_I4/DDSP_HPDA/DISP_MISC4
GPP_I3/DDSP_HPDC/DISP_MISC3
GPP_I2/DDSP_HPDC/DISP_MISC2
GPP_I1/DDSP_HPDC/DISP_MISC1
GPP_I0/PMCALERT#

TGP_H_IP_EXT/BGA1.3V



0603 R6257/GPP_I0 pull-up to +3V_S5.

ER13 : DGPU_PWR_EN change GPIO from GPP_I10 to GPP_G3;
DGPU_HOLD_RST# change from GPP_I9 to GPP_G4



ER10: Remove excess 0 ohm for CPU_C10_GATE#

GPP_H23/TIME_SYNC0
GPP_H22/ISH_I2C1_SCL
GPP_H21/ISH_I2C1_SDA
GPP_H20/ISH_I2C0_SCL
GPP_H19/ISH_I2C0_SDA
GPP_H18/SML4ALERT#
GPP_H17/SML4DATA
GPP_H16/SML4CLK
GPP_H15/SML3ALERT#
GPP_H14/SML3DATA
GPP_H13/SML3CLK
GPP_H12/SML3ALERT#
GPP_H11/SML2DATA
GPP_H10/SML2CLK
GPP_H9/SRCLKREQ15#
GPP_H8/SRCLKREQ14#
GPP_H7/SRCLKREQ13#
GPP_H6/SRCLKREQ12#
GPP_H5/SRCLKREQ11#
GPP_H4/SRCLKREQ10#
GPP_H3/SRCLKREQ9#
GPP_H2/SRCLKREQ8#
GPP_H1/SRCLKREQ7#
GPP_H0/SRCLKREQ6#

GPP_F22/VNN_CTRL
GPP_F21/EDP_BKLT_CTRL
GPP_F20/EDP_BKLTEN
GPP_F19/EDP_VODEN
GPP_F18/M2_SKT2_CFG3
GPP_F17/M2_SKT2_CFG2
GPP_F16/M2_SKT2_CFG1
GPP_F15/M2_SKT2_CFG0
GPP_F14/P5_ON#

GPP_F13/SATA_SDATAOUT0
GPP_F12/SATA_SDATAOUT1
GPP_F11/SATA_SLOAD
GPP_F10/SATA_SLOCK
GPP_F9/SATA_DEVSUP7
GPP_F8/SATA_DEVSUP6
GPP_F7/SATA_DEVSUP5
GPP_F6/SATA_DEVSUP4
GPP_F5/SATA_DEVSUP3
GPP_F4/SATA_XPCIE7/SATAGP7
GPP_F3/SATA_XPCIE6/SATAGP6
GPP_F2/SATA_XPCIE5/SATAGP5
GPP_F1/SATA_XPCIE4/SATAGP4
GPP_F0/SATA_XPCIE3/SATAGP3

GPP_E12/USB_OC3#
K47 USB2_OC2#
GPP_E11/USB_OC2#
GPP_E10/USB_OC1#
GPP_E9/USB_OC0#
GPP_E8/SATALED#/SP1_CS1#

GPP_E7/CPU_GP1
GPP_E6/SATA_DEVSUP2
GPP_E5/SATA_DEVSUP1
GPP_E4/SATA_DEVSUP0
GPP_E3/CPU_GP0
GPP_E2/SATA_XPCIE2/SATAGP2
GPP_E1/SATA_XPCIE1/SATAGP1
GPP_E0/SATA_XPCIE0/SATAGP0

AY12 DGPU_PWROK_Q (22)
BD10 R6121 10K 5% 2 +3V
BB6 GPP_H18 (14)
BD5 GPP_H15 (14)
BE1 GPP_H12 (14)
BD4 GPP_H14/SML3DATA
BE4 GPP_H13/SML3CLK
BA11 GPP_H12/SML3ALERT#
AW9 GPP_H11/SML2DATA
BG5 GPP_H10/SML2CLK
BG6 GPP_H9/SRCLKREQ15#
BD8 GPP_H8/SRCLKREQ14#
BD7 GPP_H7/SRCLKREQ13#
BE7 GPP_H6/SRCLKREQ12#
BC7 GPP_H5/SRCLKREQ11#
BC1 GPP_H4/SRCLKREQ10#
BC2 GPP_H3/SRCLKREQ9#
BC3 GPP_H2/SRCLKREQ8#
AR11 GPP_H1/SRCLKREQ7#
BA7 GPP_H0/SRCLKREQ6#

VNN_CTRL TP6025 *
PCH_BRIGHT (28)
PCH_BLON (38)
EDP_VDD_EN (28)

SKTOCC_N (3)

R6242 10K 5% 2 +3V
TP_INTH# R6116 10K 5% 2 +3V
WIFI_WAKE# (42)
TP_INTH# (36)

R6117 10K 5% 2 +3V_S5
R6118 10K 5% 2 +3V_S5
R6119 10K 5% 2 +3V_S5
R6120 10K 5% 2 +3V_S5

SATA_ACT# (33)
DEVSLP1 (34) DEVSLP: PCH Q/D Output; DEV IPU

SATAPCIE[7:0]: BIOS Enable PCH IPU 20K
PCH SATAPCIE
H-->PCIE
L-->SATA
BISO PSCSP_Px_STRP = 1

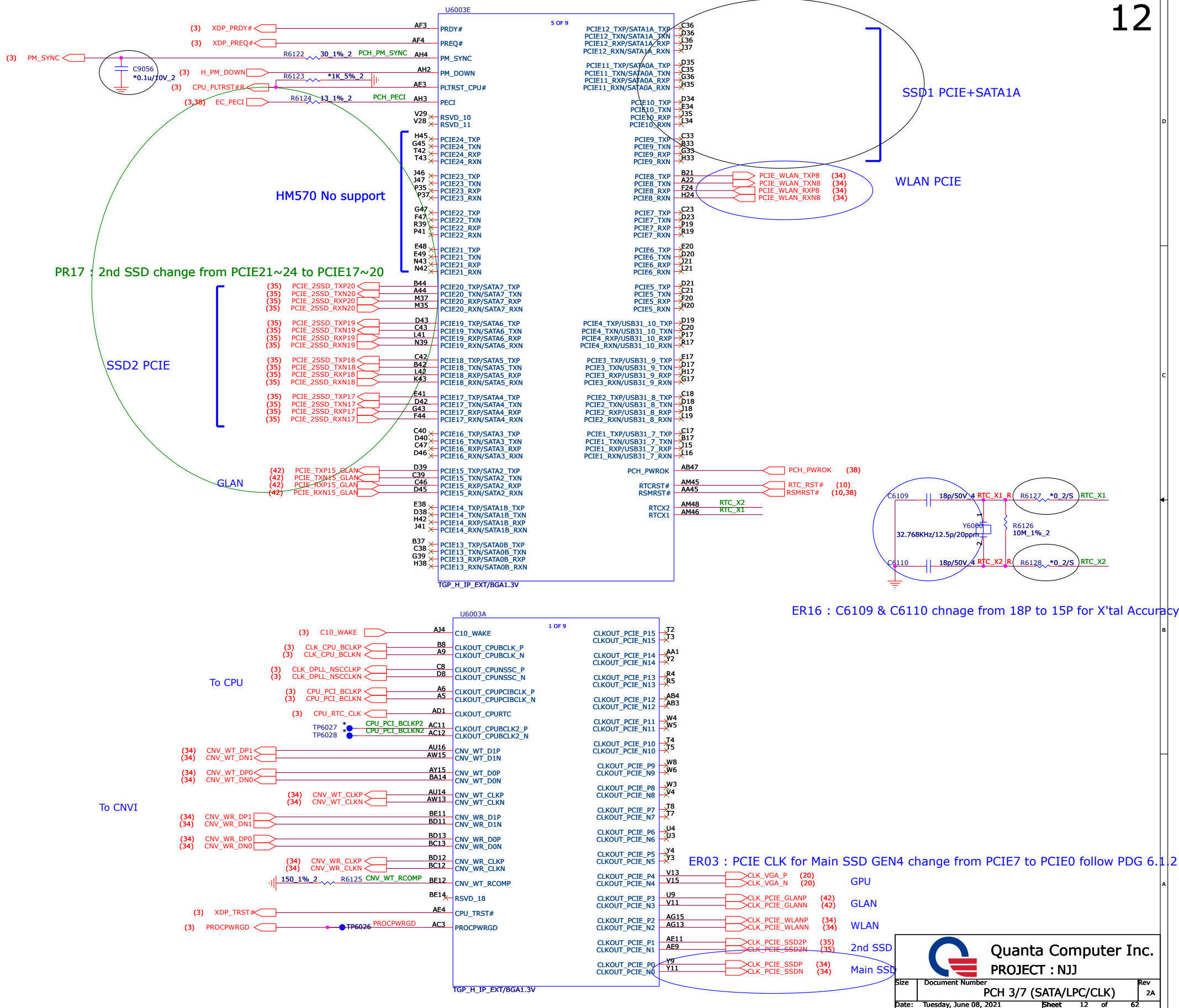
SATAPCIE[7:0]: BIOS Enable PCH IPU 20K
PCH SATAPCIE
H-->PCIE
L-->SATA
BISO PSCSP_Px_STRP = 1

0603 Remove R6269 / TBT_FORCE_PWR

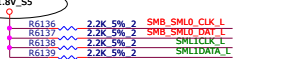
0603 Remove PDEC_I2C_IRQ#_PCH

0603 R6257/GPP_I0 pull-up to +3V_S5.

0603 R6257/GPP_I0 pull-up to +3V_S5.



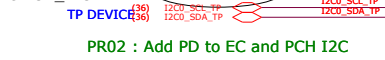
Change 3.3V to 1.8V



Change GPIO to F1 function pin



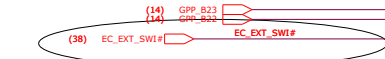
0603 Remove PCH_I2C1



PR02 : Add PD to EC and PCH I2C



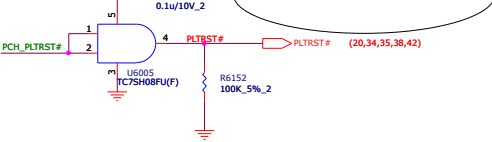
DDR4 Thermal



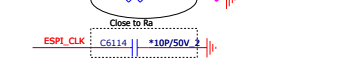
ER04 : PCIE_CLKREQ_SSD# change from CLKREQ5# to CLKREQ0#, follow ER03 setting



0603 Remove TBT_PERST#



ESPI_CS#



0603 Remove TBT_LXS0_TXD



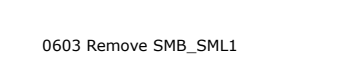
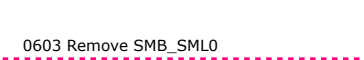
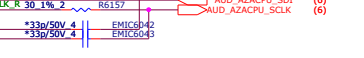
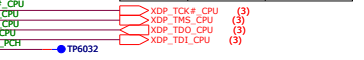
Check GPIO to F3 function pin



ER13 : DGPU_PWR_EN change GPIO from GPP_I10 to GPP_G3; DGPU_HOLD_RST# change from GPP_I9 to GPP_G4



ENTER ModSEXIT Mods	
MS_NOTIFY#	0
MS_NOTIFY#	1

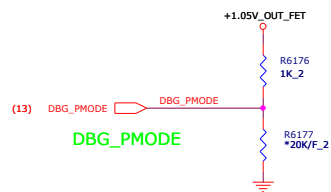
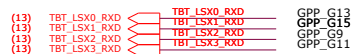
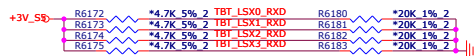


TBT LSX PINS VCCIO CONFIGURATION

High: 3.3V

Low: 1.8V

All INTERNAL PD 20K



ITP PMODE
High: DFXTESTMODE DISABLED(DEFAULT)
Low: DFXTESTMODE ENABLED
(WEAK INTERNAL PU 20K)

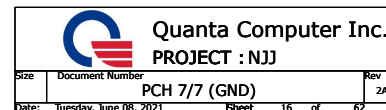
MD ID

ER12: Remove MB ID resistor.

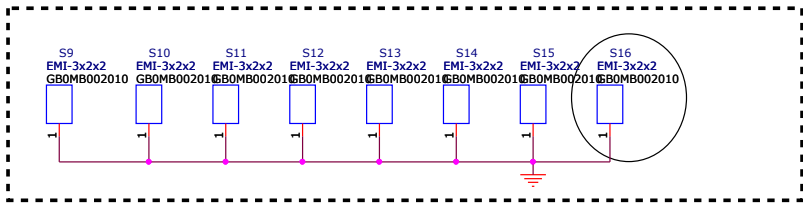
HM570 PCH-H Strapping Table

Pin Name	Strap description	Sampled	Configuration	xxx PCH STRAPS SETTING STATUS
GPP_B14 (SPKR)	Top Swap Override	PCH_PWROK	0 = *Disable Top Swap (IPD 20K) Default 1 = Enable Top Swap Mode	+3V_SS R6192 *4.7K 5% 2W R6193 *20K 5% 2W GPP_B14 (13)
GPP_B18 (GSPiO_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (IPD 20K) Default 1 = Enable No Reboot Mode	+3V_SS R6196 *4.7K 5% 2W R6197 *20K 5% 2W GPP_B18 (13)
GPP_C2 (SMBALERT#)	TLS Confidentiality	RSMRST#	0 = *Disable Intel ME Cryp to TLS(IPD 20K) Default 1 = Enable Intel ME Cryp to TLS to support AMT TLS	+3V_SS R6198 *4.7K 5% 2W R6199 *20K 5% 2W GPP_C2 (13)
GPP_B22 (GSPi1_MOSI)	Boot BIOS Strap Bit BBS	PCH_PWROK	This strap has a 20 kohm +-30% internal pull-down. 0=>BIOS fetches are routed to SPI (MAF) or the eSPI Flash Channel (SAF) 1=>BIOS fetches are routed to the eSPI Peripheral Channel	+3V_SS R6200 *4.7K 5% 2W R6201 *20K 5% 2W GPP_B22 (13)
GPP_C5 (SML0ALERT#)	eSPI or LPC	RSMRST#	This strap has a 20 kohm internal pull-down 0 = Enable eSPI. (Default) 1 = Disable eSPI	+3V_SS R6200 *4.7K 5% 2W R6201 *20K 5% 2W GPP_C5 (13)
GPP_H12 (SML3ALERT#)	eSPI Flash Sharing Mode	RSMRST#	This strap has a 20 kohm +-30% internal pull-down. 0=>Master Attached Flash Sharing (MAFS) enabled (Default) 1=>Slave Attached Flash Sharing (SAFS) enabled	+3V_SS R6186 *4.7K 5% 2W R6187 *20K 5% 2W GPP_H12 (11)
GPP_H15 (SML3ALERT#)	Reserved	RSMRST#	This signal has an internal PD 20K 0=> JTAG ODT is disabled 1=> JTAG ODT is enabled	+3V_SS R6188 *4.7K 5% 2W R6189 *20K 5% 2W GPP_H15 (11)
GPP_B23 (SML1ALERT# /PCHHOT#)	Reserved	RSMRST#	This signal has an internal PD 20K 0 = 38.4 MHz clock (direct from crystal) (default) 1 = 19.2 MHz clock (derived from 38.4 MHz crystal)	+3V_SS R6190 *4.7K 5% 2W R6191 *20K 5% 2W GPP_B23 (13)
GPP_H18 (SML4ALERT#)	Reserved	RSMRST#	This strap has a 20 kohm +-30% internal pull-down 0=> VCCSPI at 3.3 V (Default) 1=> VCCSPI at 1.8 V	+3V_SS R6194 *4.7K 5% 2W R6195 *20K 5% 2W GPP_H18 (11)
HDA_SDO (I2S0_TXD)	Flash Descriptor Security Override / Intel ME Debug Mode	PCH_PWROK	0 = *Enable security in the Flash Description (IPD 20K) Default 1 = Disable Flash Descriptor Security (Override)	FLASH_OVRD_EC...Page 11
GPP_I6 (DDPB_CTRLDATA)	Display Port B Detected	PCH_PWROK	0 = *Port B is not detected (IPD 20K) (Default) 1 =Port B is detected	(11,41) INT_DDIB_SCL R6206 2.2K 5% 2W R6207 2.2K 5% 2W +3V (11,41) INT_DDIB_SDA
GPP_I8 (DDPC_CTRLDATA)	Display Port C Detected	PCH_PWROK	0 = *Port C is not detected (IPD 20K) (Default) 1 =Port C is detected	(11) INT_HDMI_SCL1 R6208 2.2K 5% 2W R6209 2.2K 5% 2W +3V (11) INT_HDMI_SDA1
GPP_I2 (CNV_BRI_DT/UART0_RTS#)	XTAL Frequency Select	RSMRST#	An external pull-up is required on this strap since 38.4MHz XTAL is not supported on the PCH. 0 = *38.4MHz XTAL frequency selected. (IPD 20K) (Default) 1 = 24MHz XTAL frequency selected.	+1.8V_SS R6184 *4.7K 5% 2W R6204 20K 5% 2W CNV_RBI_DT (11,34)
GPP_I4 (CNV_RGI_DT/UART0_TXD)	M.2 CNV Mode Select	RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVI enable. (Default) 1 = Integrated CNVI disable.	+1.8V_SS R6185 10K 5% 2W R6205 *100K 1% 2W CNV_RGI_DT (11,34)
GPP_I9	1.8V VCCPSPI	RSMRST#	0 = *VCCSPI is connected to 3.3V rail. (IPD 20K) (Default) 1 = VCCSPI is connected to 1.8V rail	
GPD7	Reserved	DSW_PWROK	This strap has a 20 kohm +-30% internal pull-down. This strap should sample LOW. There should NOT be any onboard device driving it to opposite direction during strap sampling.	+3V_SS R6202 *4.7K 5% 2W R6203 20K 5% 2W GPD7 (10)

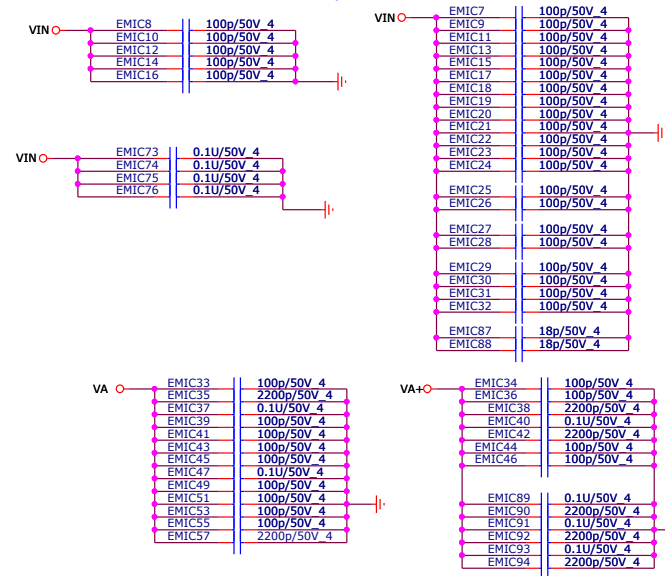




SMT GASKET-BOT



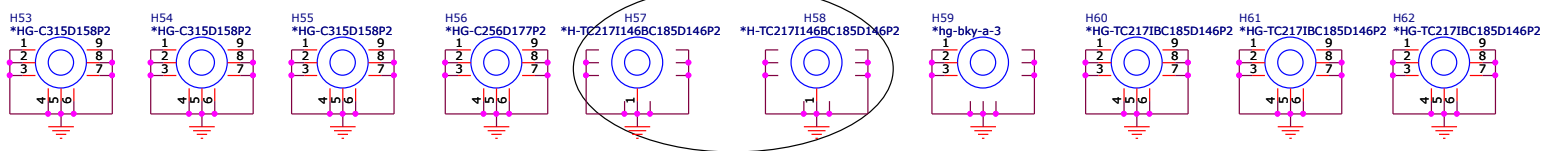
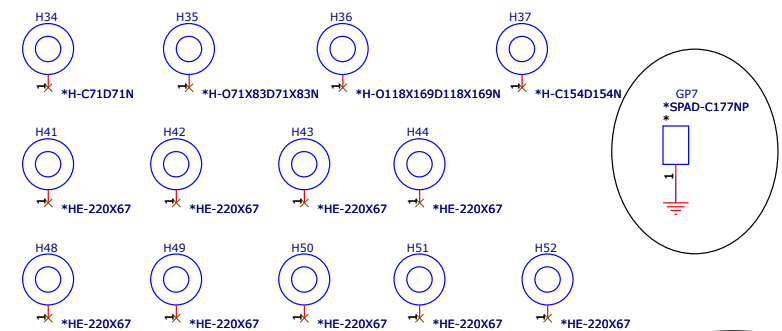
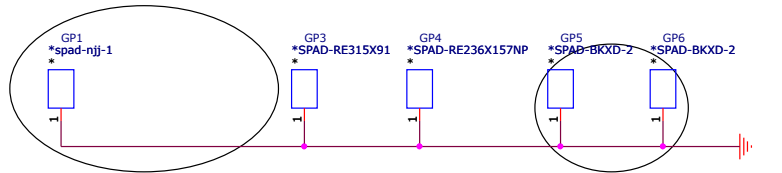
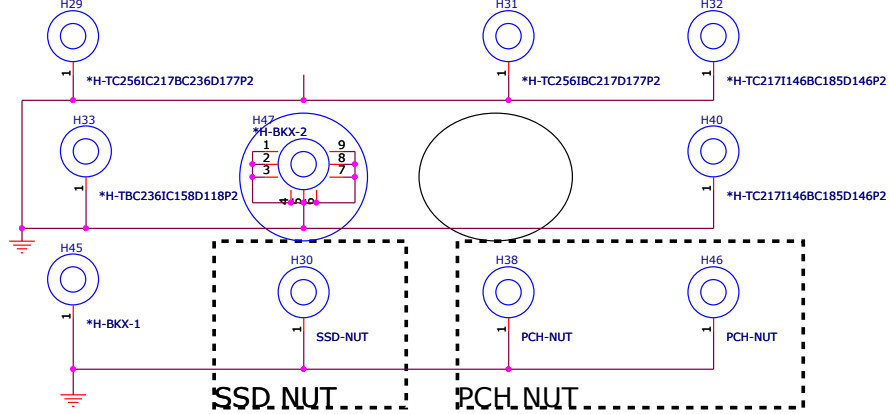
placement on TOP SIDE VIN Plane



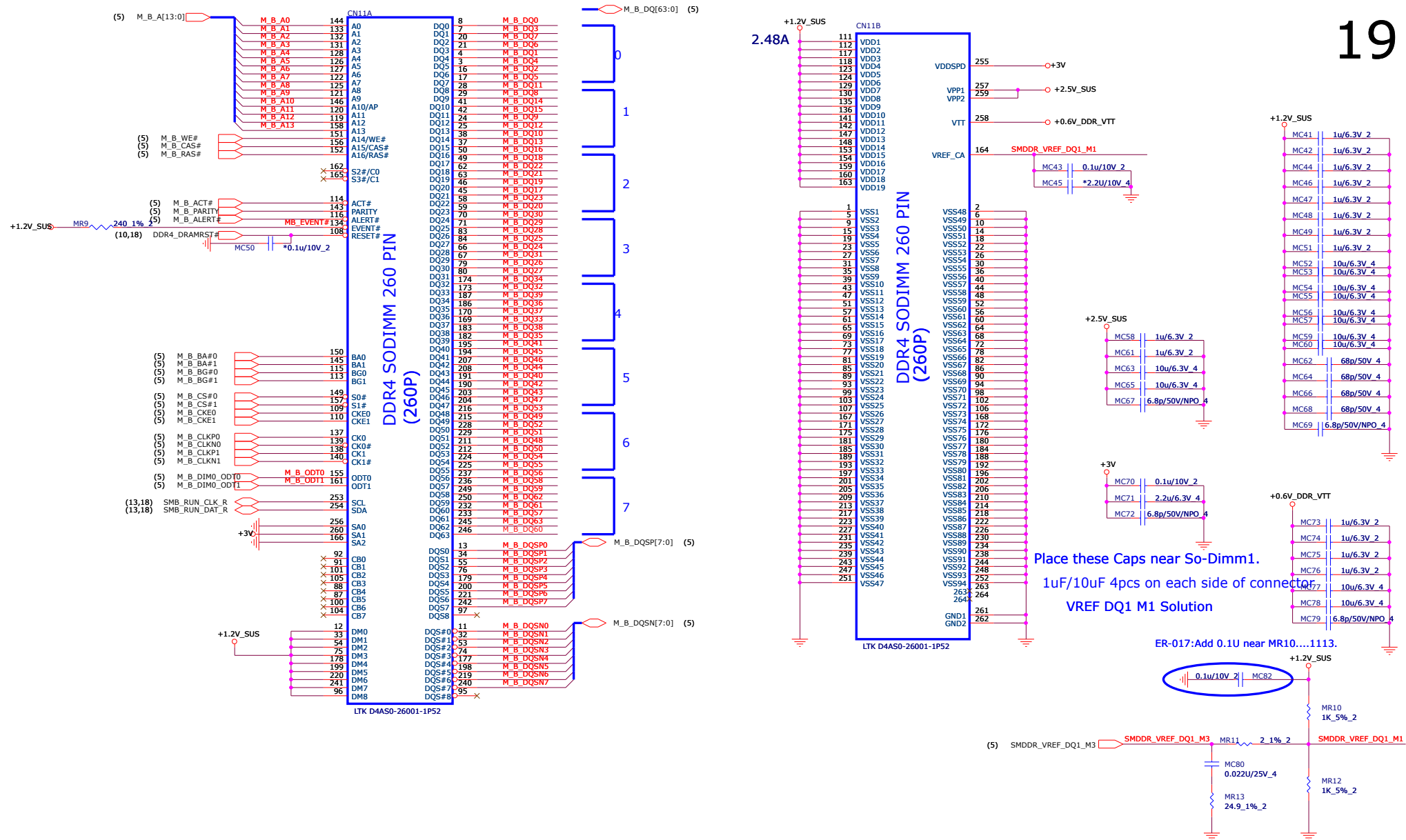
PR04 : VIN/VA+ 0201 CAP chnage to unmount for Pre QS SMT

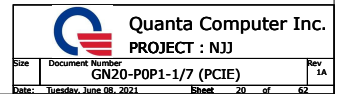
placement on TOP SIDE VA+ Plane

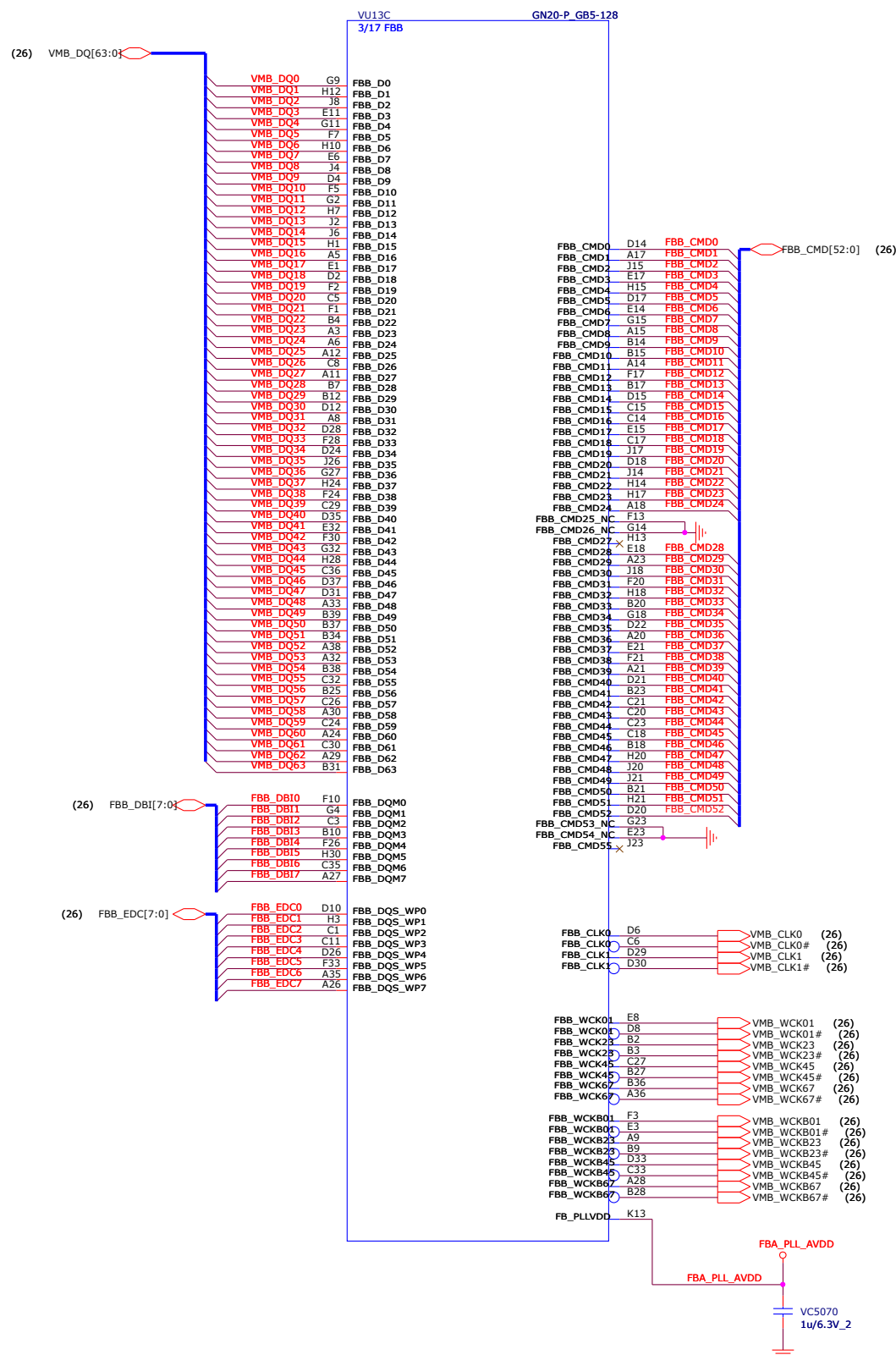
ER32: Change H47 footprint for EMI issue

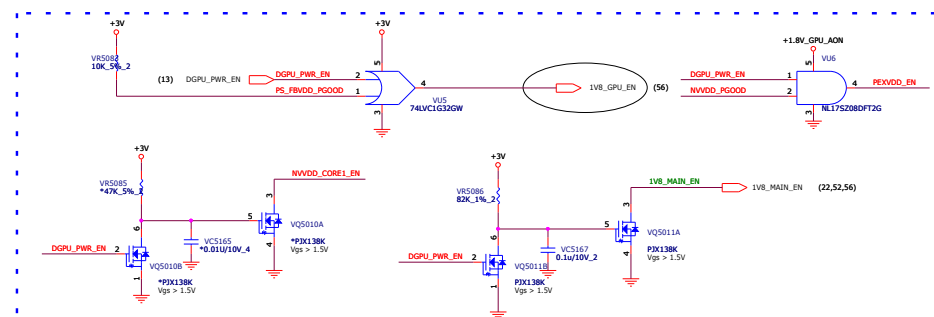
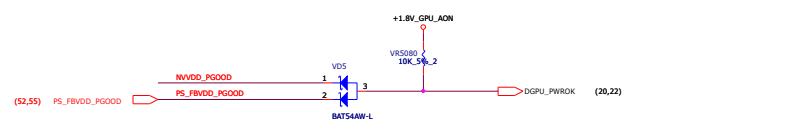
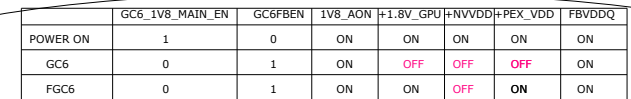
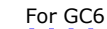


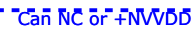


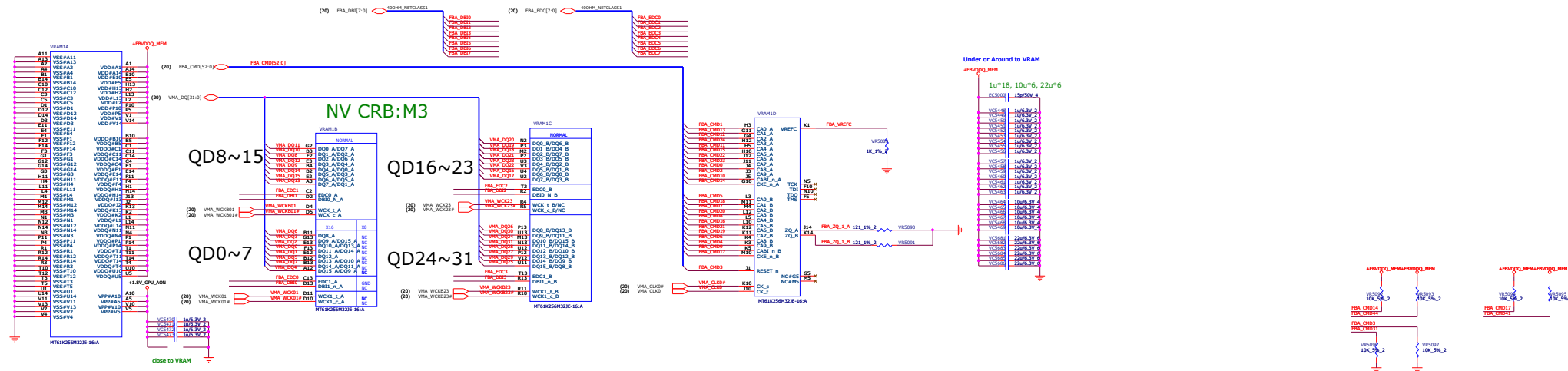




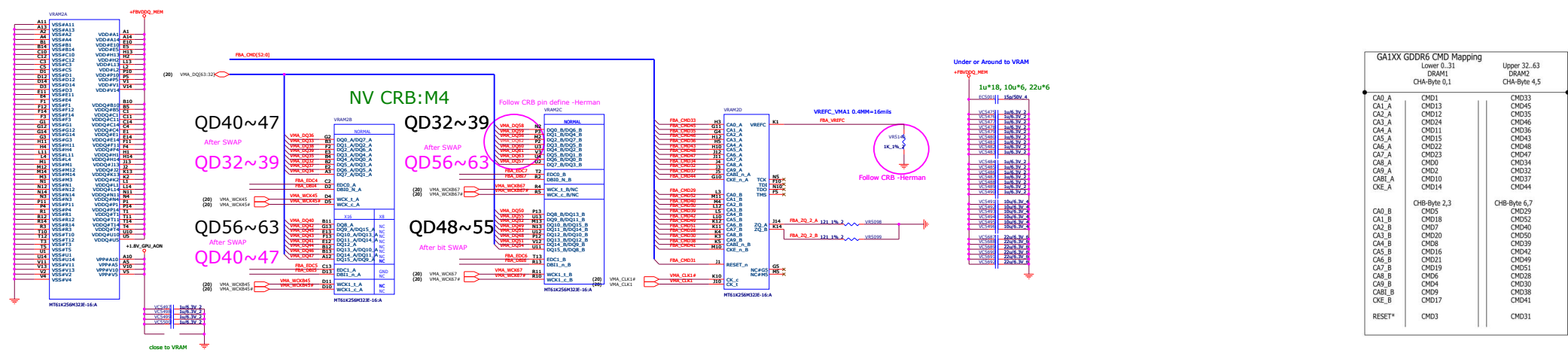


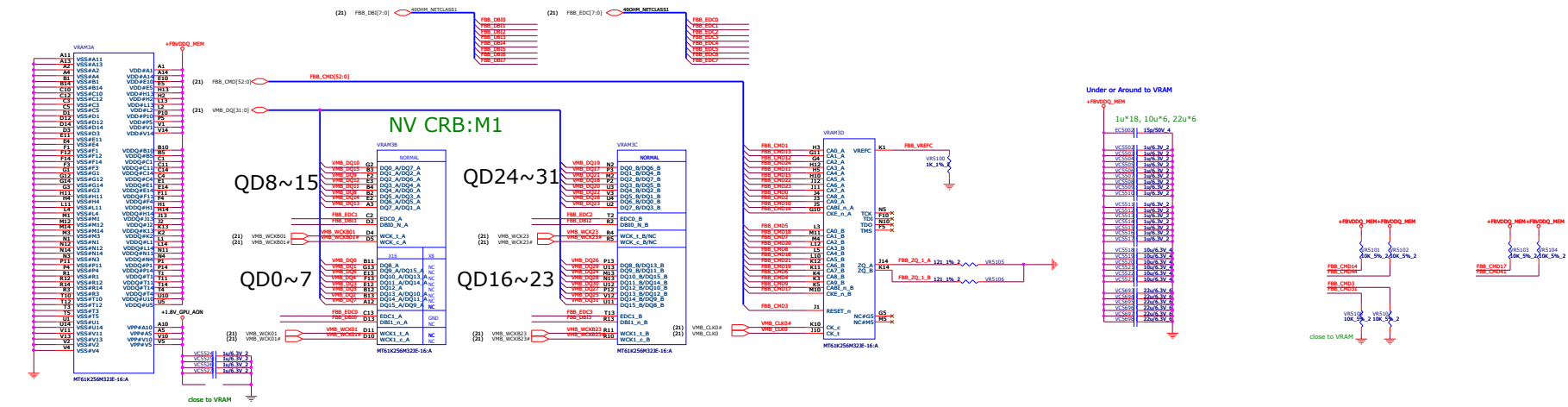




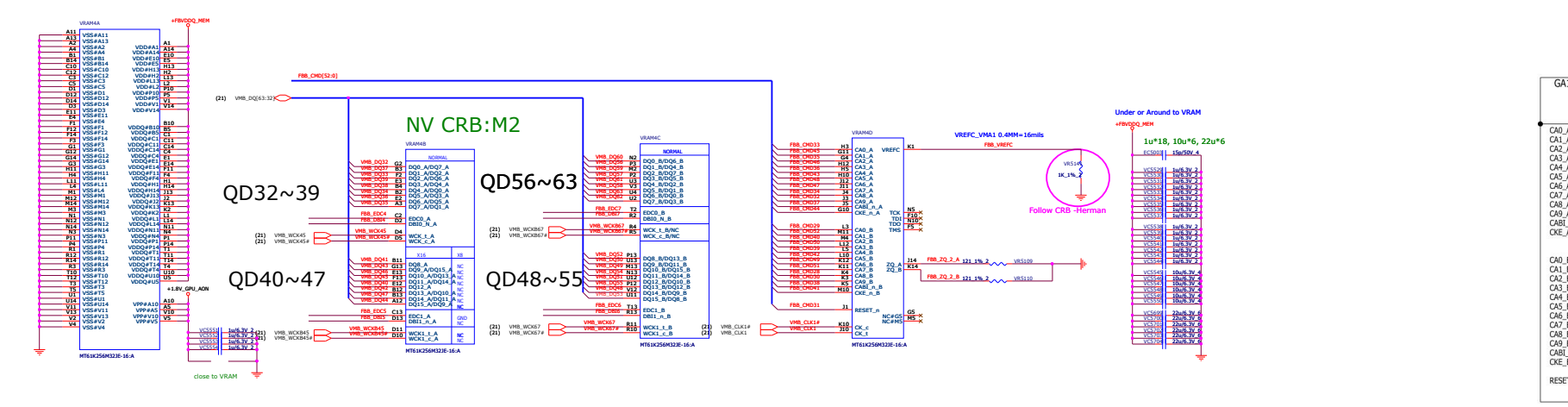


MEMORY: FBA Partition 63..32

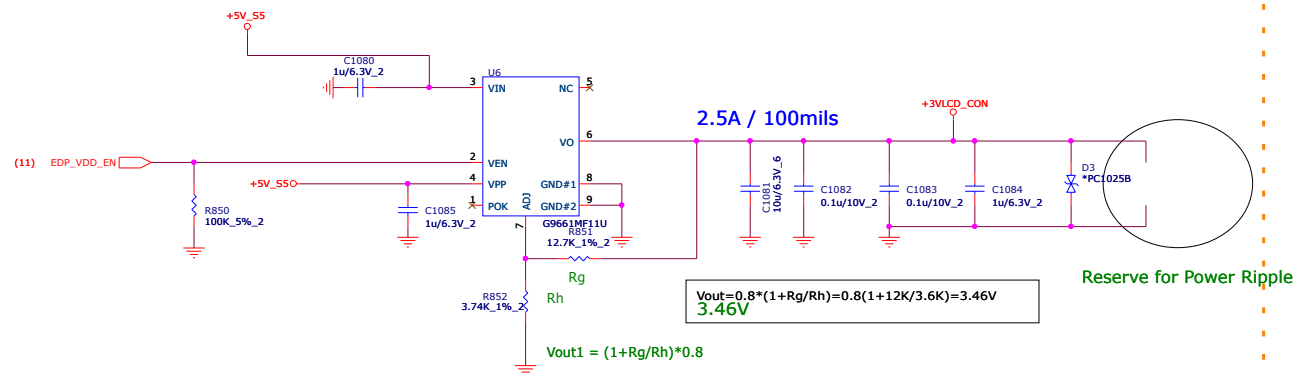
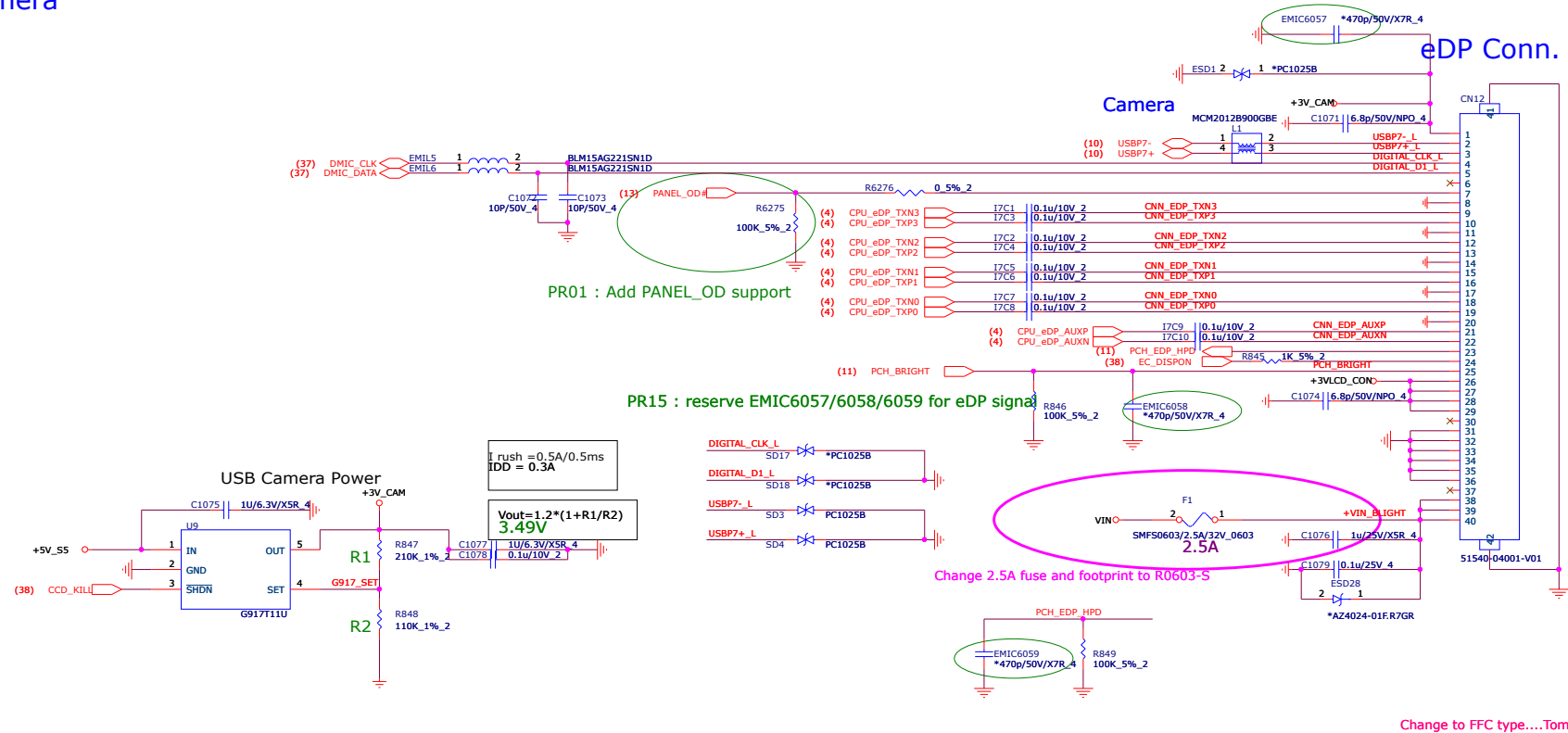


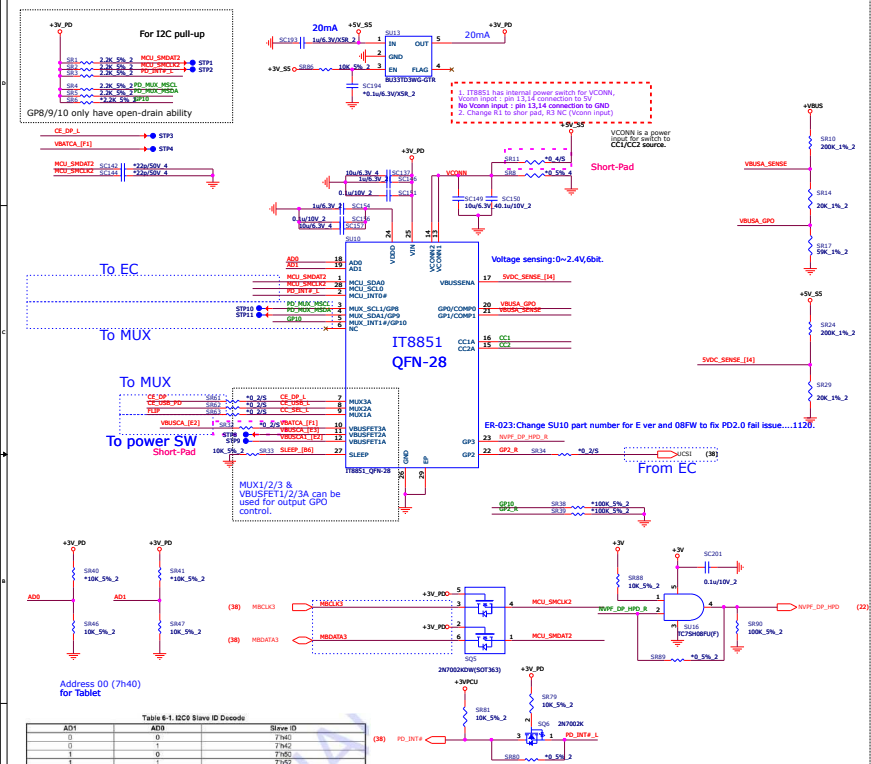


MEMORY: FBB Partition 63..32

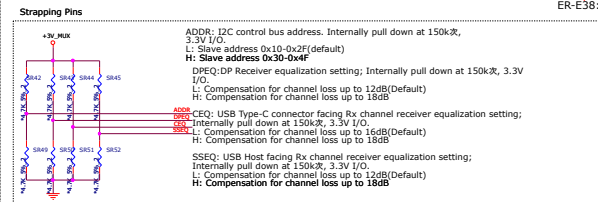
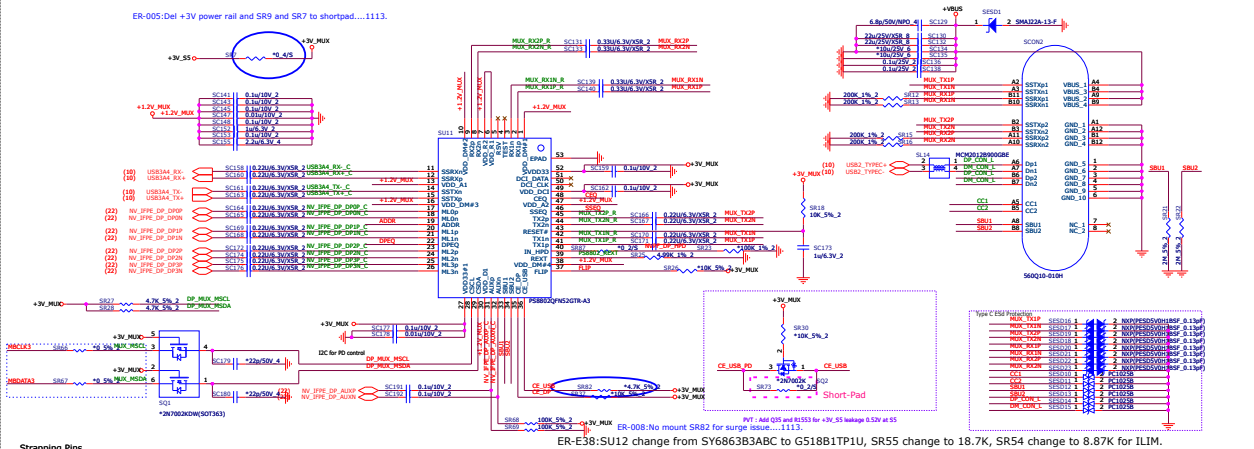


GA10X GDDR CMD Mapping		Upper 32.63
DRAM1		DRAM2
CHA-Byte 0, 1		CHA-Byte 4, 5
CA0_A	OMD1	OM033
CA1_A	OMD13	OM045
CA2_A	OMD12	OM035
CA3_A	OMD24	OM046
CA4_A	OMD20	OM036
CA5_A	OMD15	OM043
CA6_A	OMD22	OM047
CA7_A	OMD23	OM048
CA8_A	OMD0	OM034
CA9_A	OMD2	OM032
CABL_A	OMD10	OM037
CKE_A	OMD14	OM044
CHB-Byte 2,3		CHB-Byte 6,7
CA0_B	OMD5	OM029
CA1_B	OMD18	OM052
CA2_B	OMD7	OM040
CA3_B	OMD20	OM051
CA4_B	OMD8	OM039
CA5_B	OMD16	OM042
CA6_B	OMD17	OM049
CA7_B	OMD19	OM051
CA8_B	OMD6	OM028
CA9_B	OMD4	OM030
CABL_B	OMD9	OM038
CKE_B	OMD17	OM041
RESET*	OMD3	OM031





DP MUX



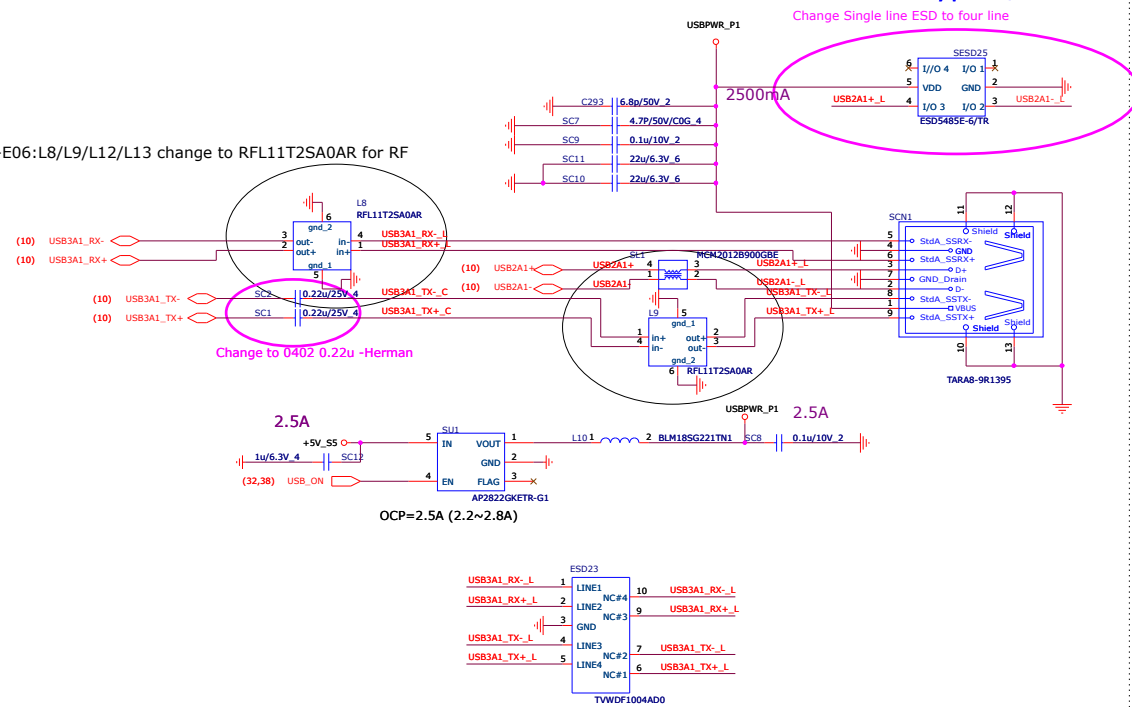
0603 +1.2V_MUX Power from Page HDMI

CE_DP	CE_USB	FLIP	
L	H	L	SSRX/TX to TX1/RX1
L	H	L	SSRX/TX to TX2/RX2
H	L	L	ML0 to RX2, ML1 to TX2, ML2 to TX1, ML3 to RX1
H	L	L	ML3 to RX2, ML2 to TX2, ML1 to TX1, ML0 to RX1
H	H	L	SSRX to RX1, SSTX to TX1, ML0 to RX2, ML1 to TX2
H	H	H	SSRX to RX2, SSTX to TX2, ML0 to RX1, ML1 to TX1

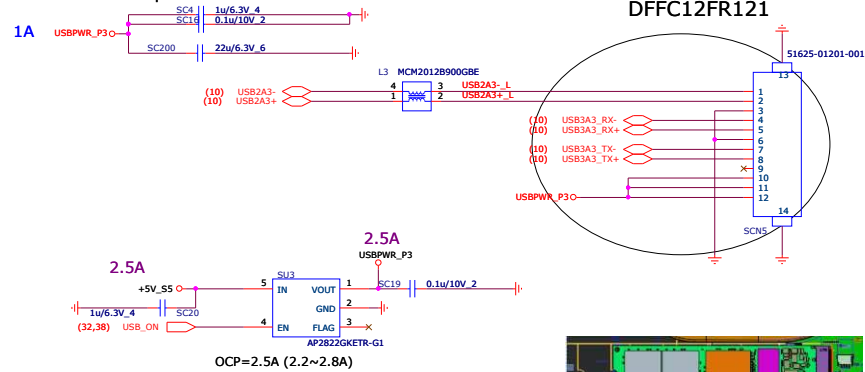
USB 3.2 GEN1 Type A/ PORT1

USB 2.0 PORT1

PR-E06:L8/L9/L12/L13 change to RFL11T2SA0AR for RF

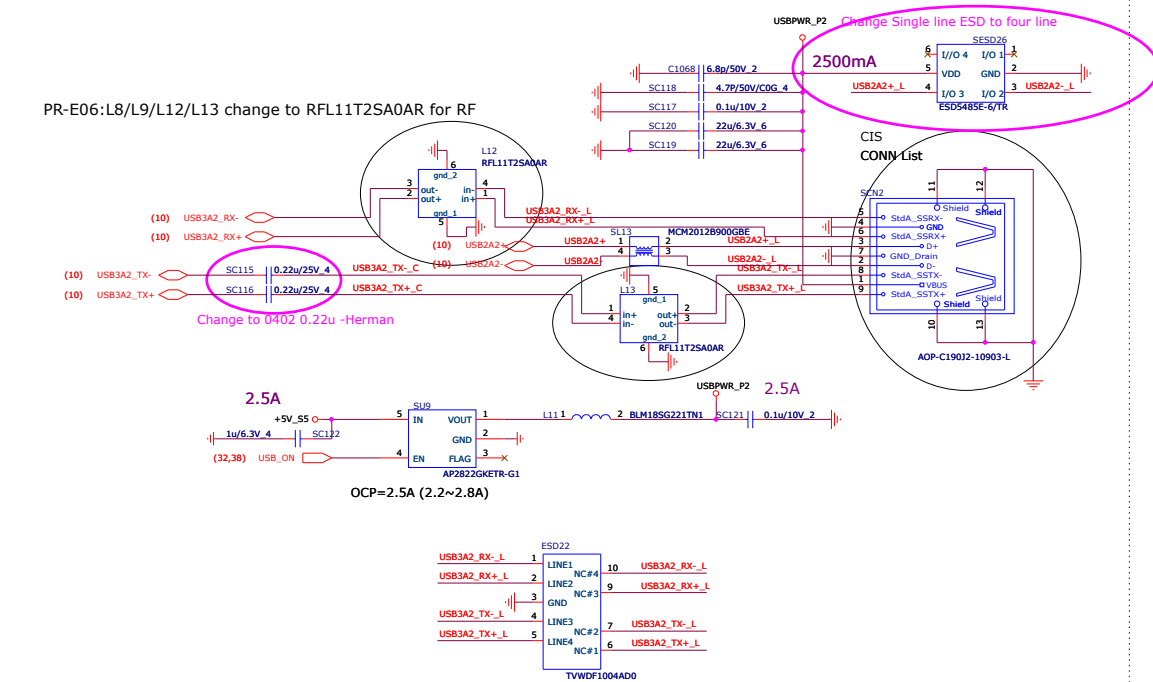


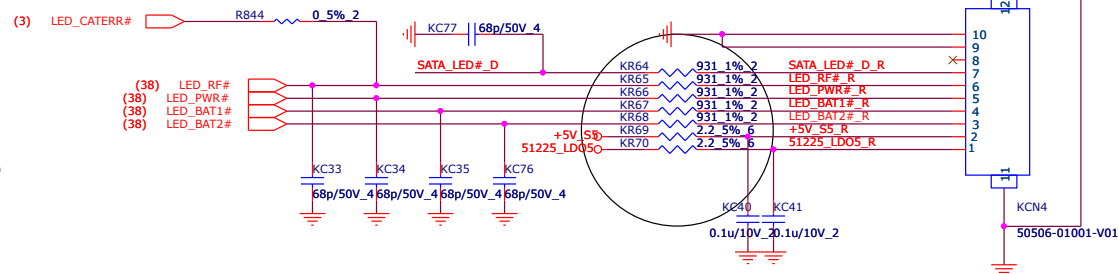
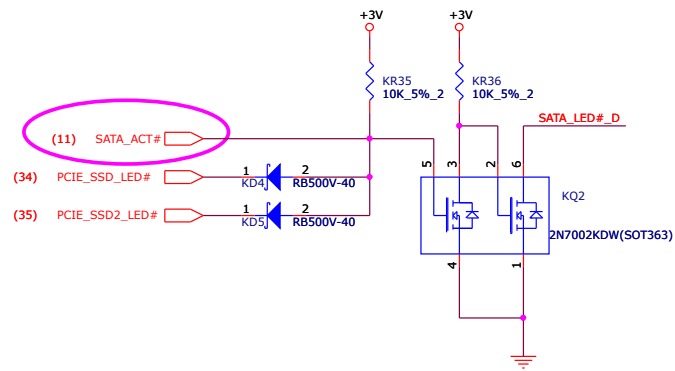
USB2.0 port



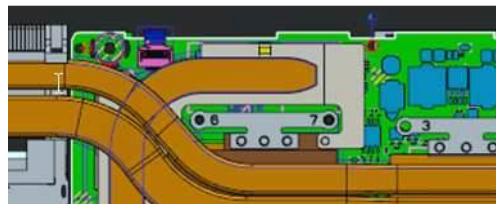
USB 3.2 GEN1 Type A/PORT2

PR-E06:L8/L9/L12/L13 change to RFL11T2SA0AR for RF



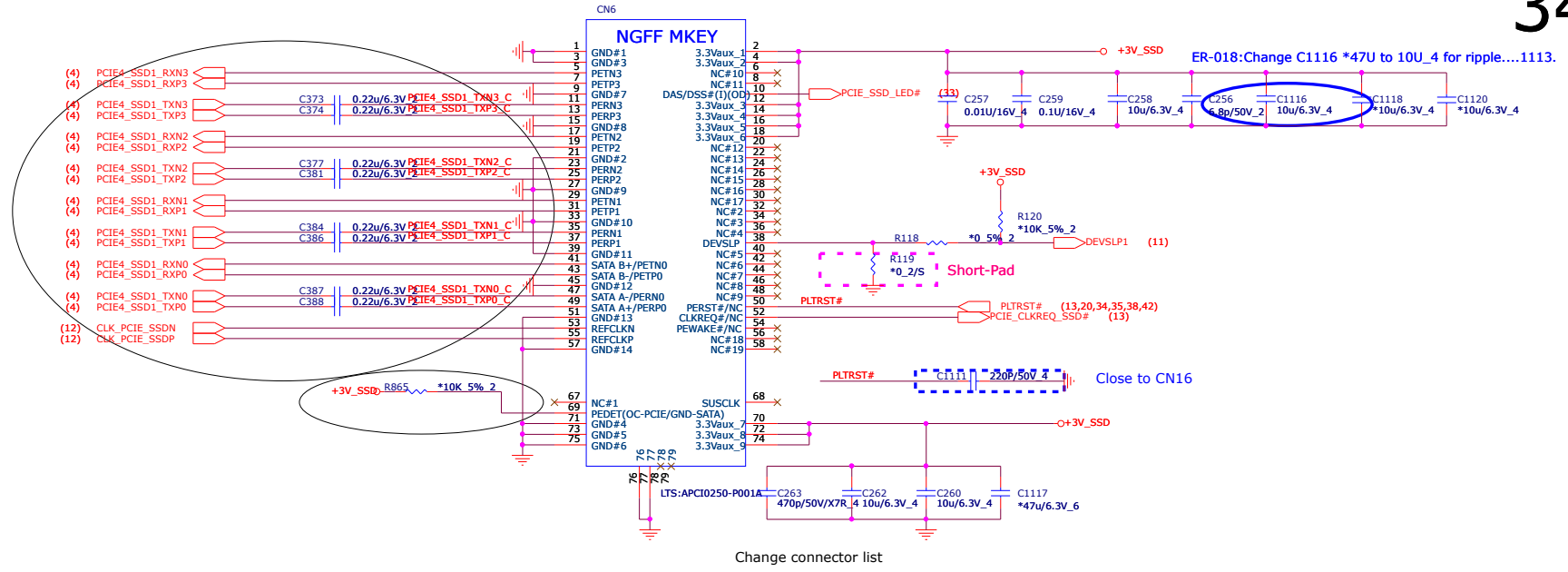


ER-E34:KR64, KR65, KR66, KR67, KR68 change from 390 to 931 ohm for brightness



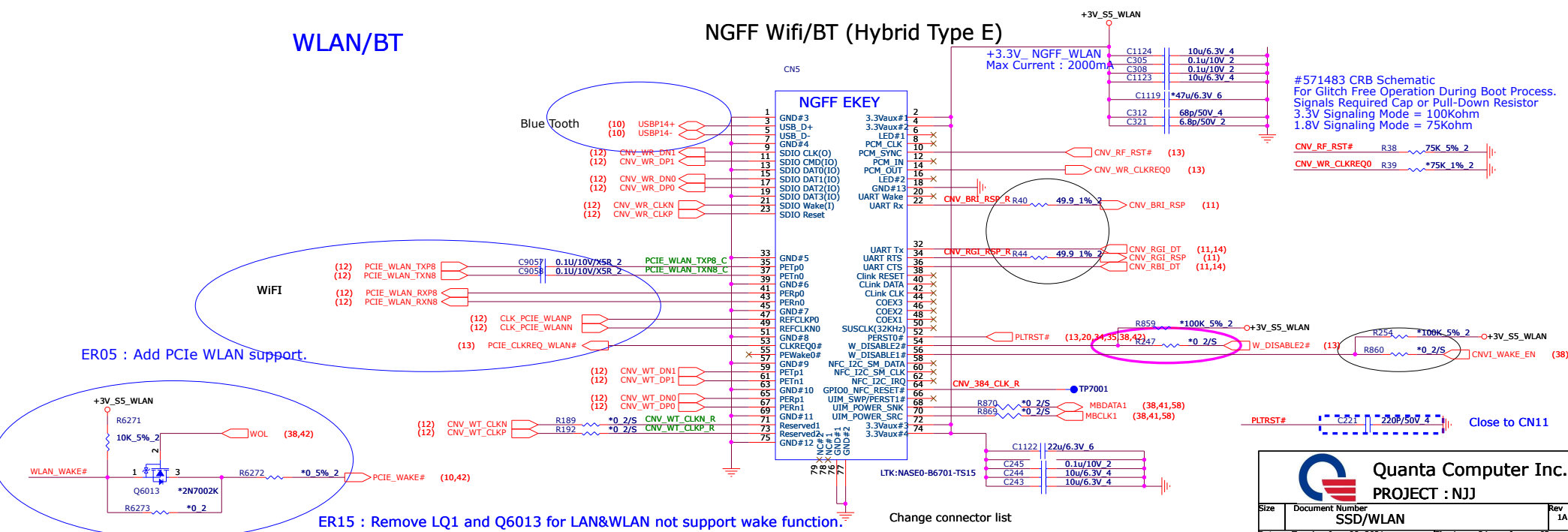
Quanta Computer Inc.
PROJECT : NJJ

Size	Document Number	Rev
	HDD/LED	1A
Date:	Tuesday, June 08, 2021	Sheet 33 of 62

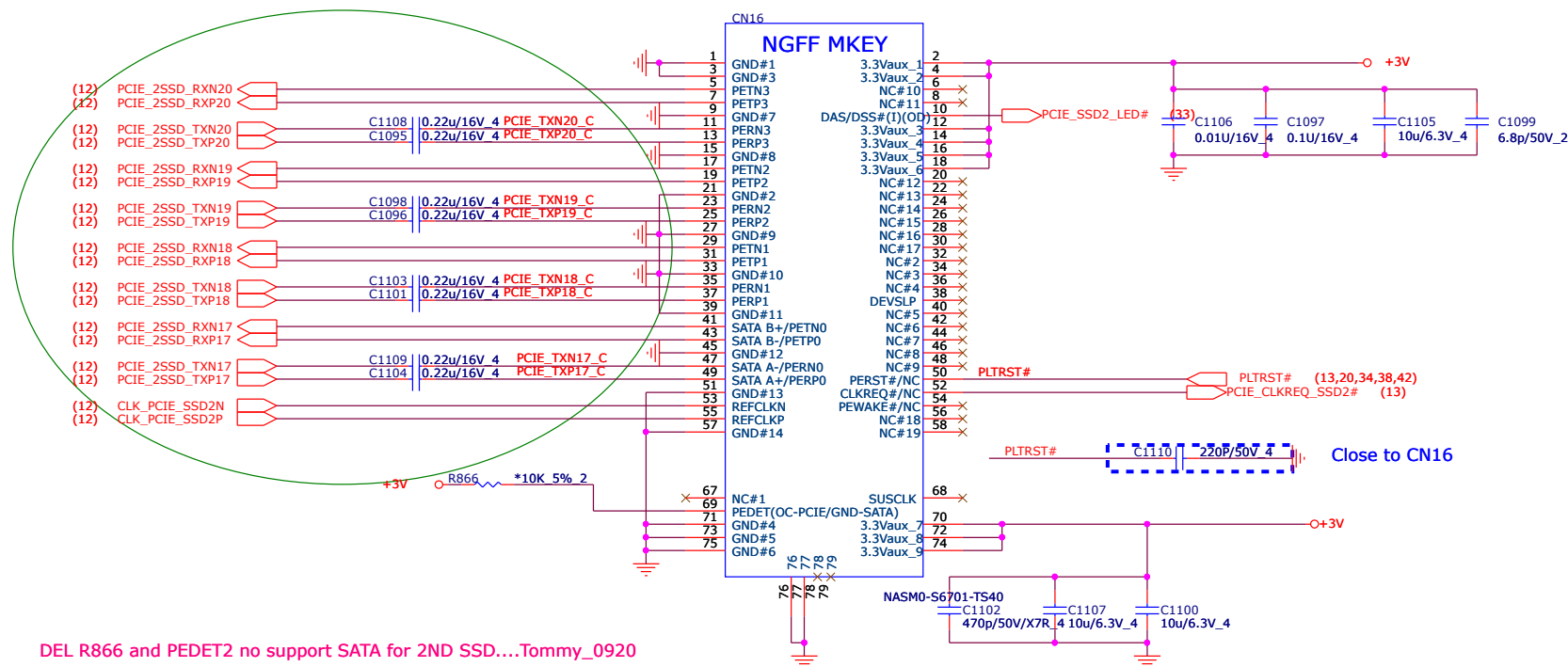


WLAN/BT

NGFF Wifi/BT (Hybrid Type E)



PR17 : 2nd SSD change from PCIE21~24 to PCIE17~20

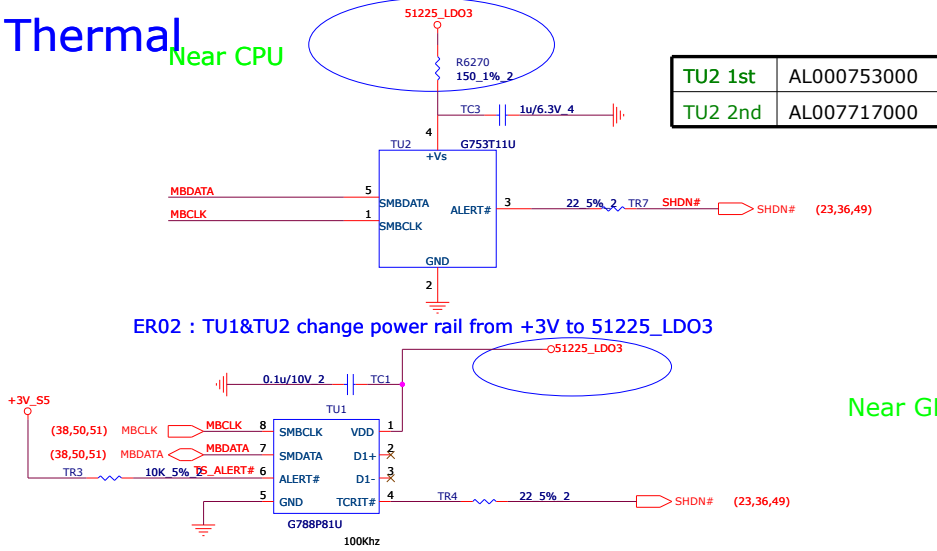


DEL R866 and PEDET2 no support SATA for 2ND SSD....Tommy_0920

Change connector list

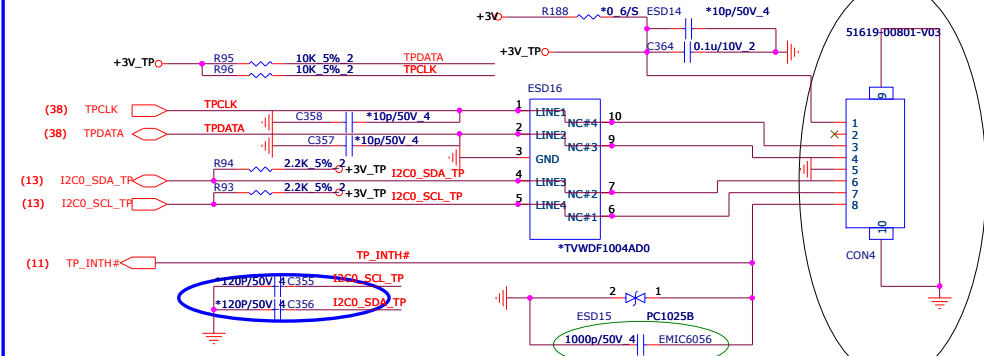
Thermal

Near CPU



Near GPU

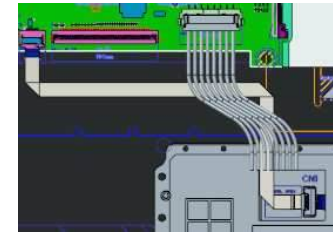
Touch Pad Connector AA type

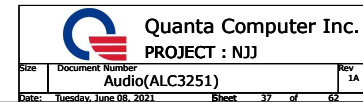


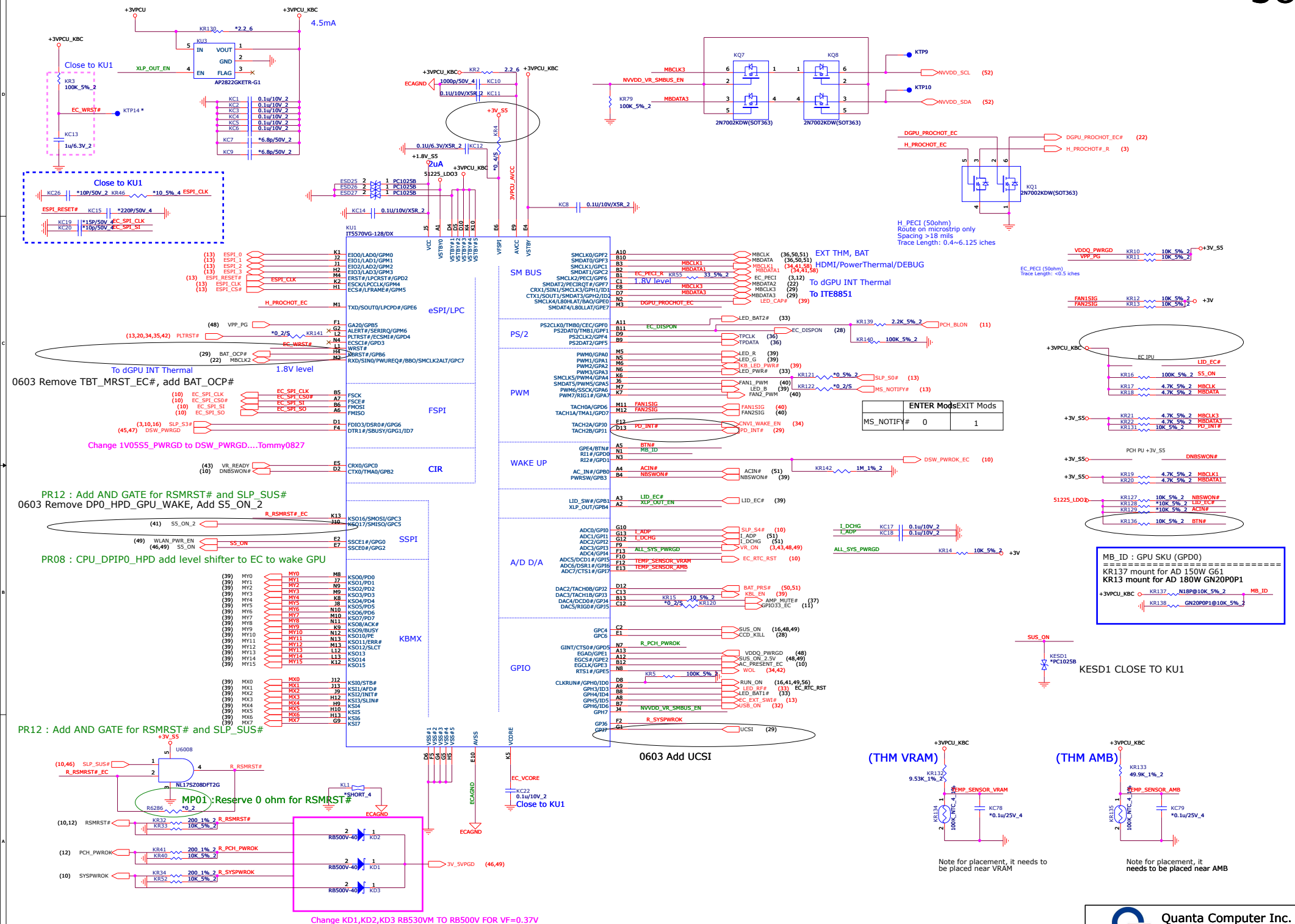
PR13 : TP_INT# add 1000p for EMI

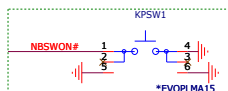
Change connector list

ER-029: Change C355,C356 to no-mount for fix TP timing issue....1122.

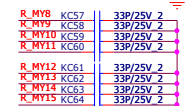
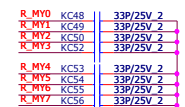






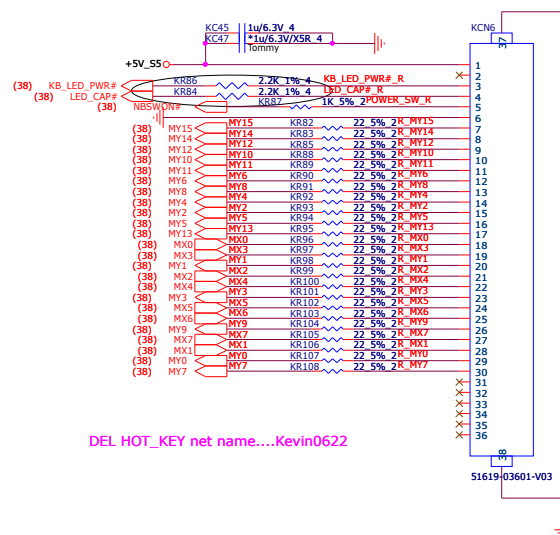


Reserve PSW1 for SR/ER debug



KEYBOARD Con.

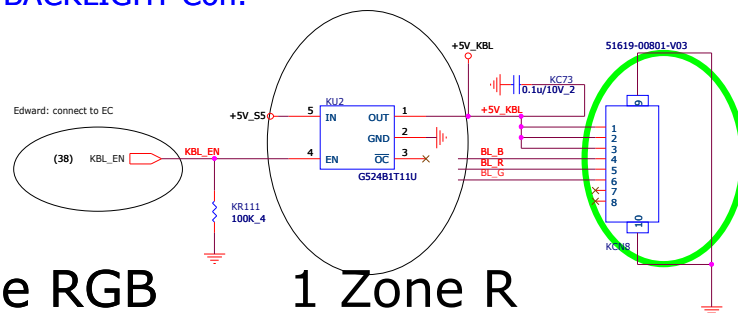
PR-E10:KR84, KR86 change from 220 ohm to 2.2K ohm for ID KB LED brightness request.



DEL HOT_KEY net name....Kevin0622

KEYBOARD BACKLIGHT Con.

8/7 Change to footprint.

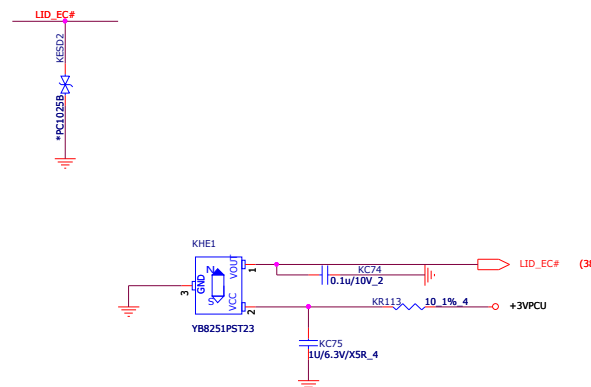


1 Zone RGB

1 Zone R

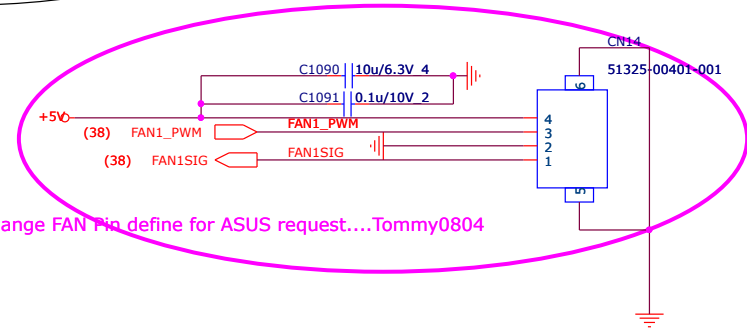
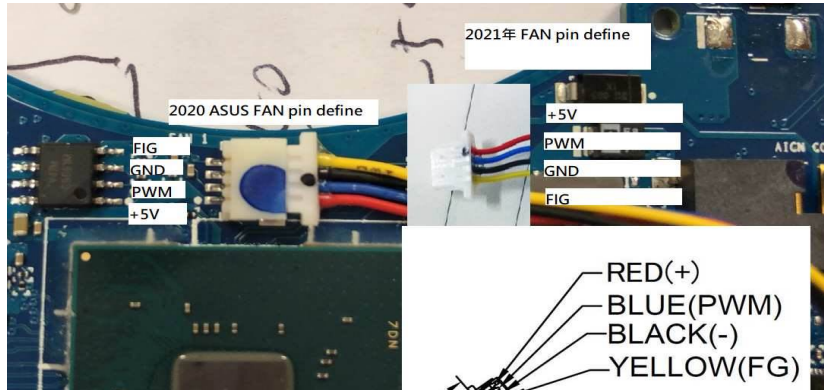
Del KQ15/KQ13 for no support Red backlight....TOMMY

ESD23 CLOSE TO KHE1

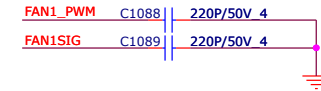


FAN1 for CPU

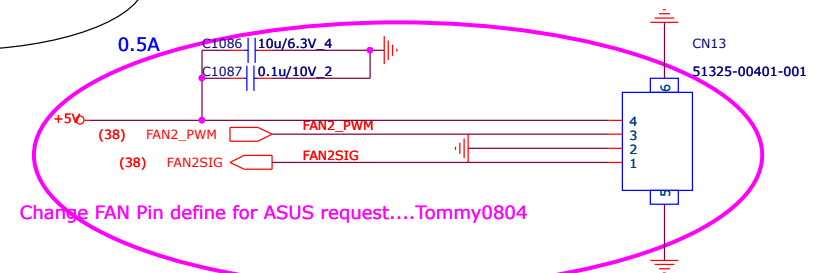
Add +12V power rail and change CAP to 25V....Kevin0619



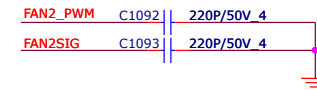
Change FAN Pin define for ASUS request....Tommy0804



FAN2 for GPU



Change FAN Pin define for ASUS request....Tommy0804



Quanta Computer Inc.
PROJECT : NJJ

ER-011:Change no mount:HQ3, NO USED....1113



HR1
10K_5%_2



(4) INT_DDIB_TXDN → INT14 0.1u/10V_2

(4) INT_DDIB_TXCP → INT15 0.1u/10V_2 INT_DDIB_TXCP_L

(4) INT_DDIB_TXCN → INT16 0.1u/10V_2 INT_DDIB_TXCN_L

+1.2V_HDMI

HC18 4.7u/6.3V_4 0.01u/10V HC19 20.1u/10V_2 HC21

INT_HDMI_HPD HR37 100K 5% 2

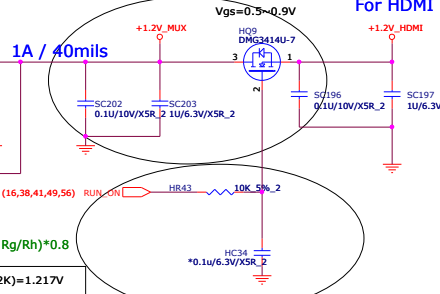


(11,14) INT_DDIB_SCL 4



0603 Add +1.2V_MUX/SC202/SC203/HR43/HQ9/HC34

For HDMI re-driver 0.13A / 20mils



ER-004:Change +1.2V to +1.2V_HDMI power rail name....111

²PR07 : HDMI re-driver PS8209 change to PS8409 for Jitter issue

ER-026: Change 2.1ohm to 5.1ohm for fix TDR issue....112

ER11: HDMI TMDS Resistor change from 5.1R to 0R, and HL1 change to HCM2012GD500AE base on EA report.

PR-E08:HDMI DDC pull-up resistor change from 2.2K to 3K for HDMI protocol issue

HPD and +5V HDMI use TPUC0521NE only

ER-007:ADD DISCHARGE FOR to +1.2V_HDMI power rail name....1113

Internally pull up $\approx 150K$

UD34 4.7K EM 250 UD32 4.7K EM 3.1

- HR30 mount to enable HDMI Pre-Emphasis

Internally pull up $\sim 150\text{K}$

DC coupling enable; Internal pull up, 3.3V I/O.
L: DC coupling input
H: Default, AC coupling input

Receiver equalization setting; Internal pull up , 3.3V I/O.
L: Compensation for channel loss up to 13dB
H: Default , Compensation for channel loss up to 17dB
M: Compensation for channel loss up to 11dB

```
Output pre-emphasis setting; Internal pull up, 3.3V I/O.
L: Pre-emphasis =2.5dB
H: Default, No Pre-emphasis
```

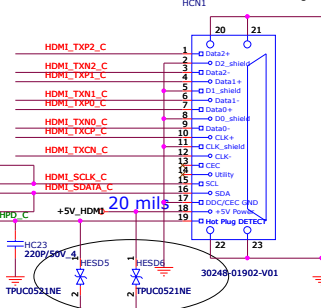
I2C Slave Address selection; Internal pull down, 3.3V I/O:
L: Default, Slave address 0x10-0x2F.
H: Alternative slave address 0x90-0x9F, 0xD0-0xDF.

```
HDMI_ID enable ; Internal pull down , 3.3V I/O.
L: Default, HDMI ID enable
H: HDMI ID disable
```

EMI Solution

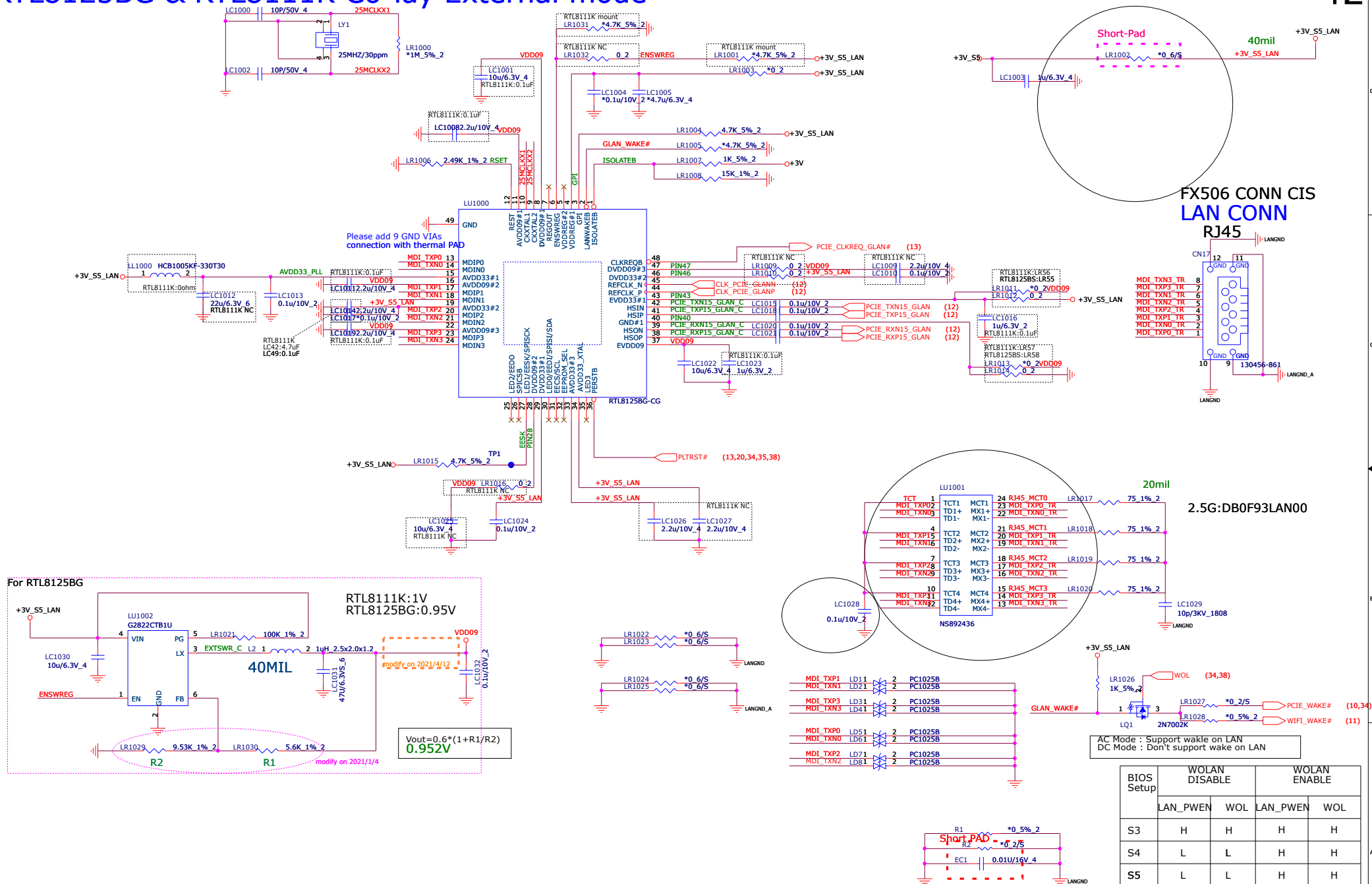


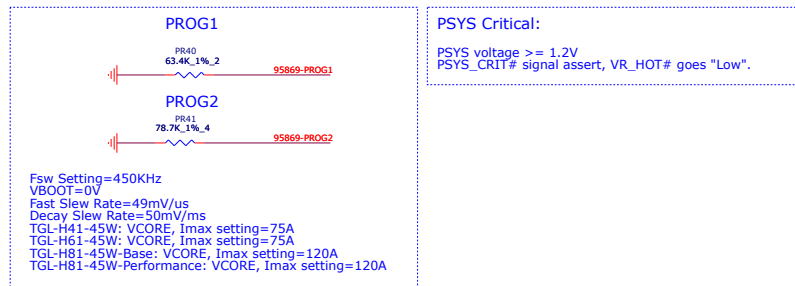
FP & PN changed



RTL8125BG & RTL8111K Co-lay External mode

42





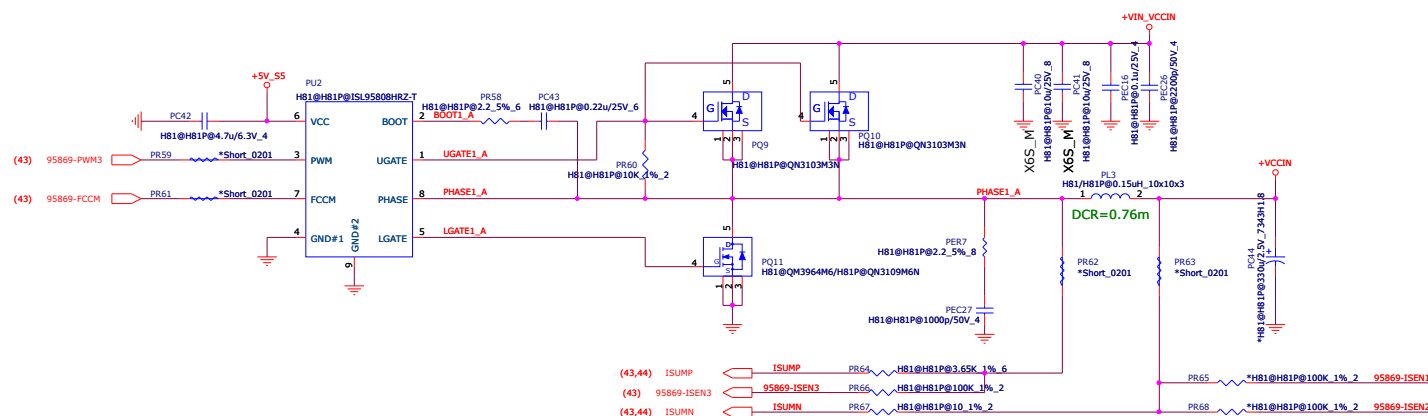
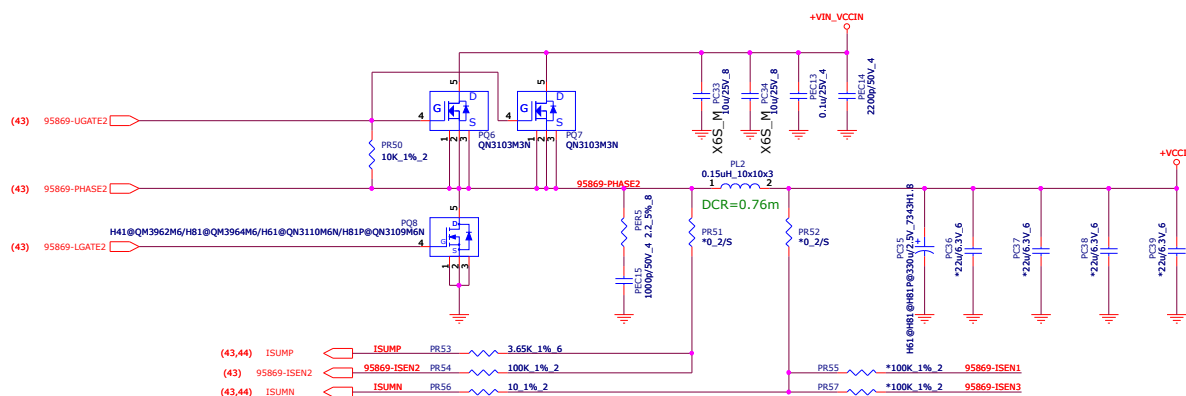
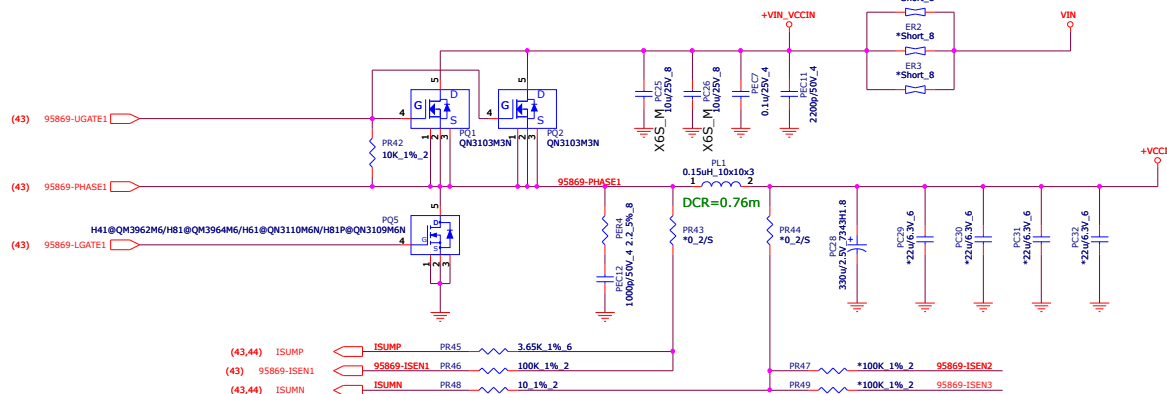
	H81P	H81	H61	H41
PR32	95.3K_1%_4(CS39532FB03)	95.3K_1%_4(CS39532FB03)	110K_1%_4(CS41102FB13)	110K_1%_4(CS41102FB13)
PR25	3.48K_1%_4(CS23482FB12)	3.48K_1%_4(CS23482FB12)	2.61K_1%_4(CS22612FB15)	2.49K_1%_4(CS22492FB22)
PR16	536_1%_4(CS15362FB13)	536_1%_4(CS15362FB13)	536_1%_4(CS15362FB13)	536_1%_4(CS15362FB13)
PQ5				
PQ8	QN3109M6N(BAM31090000)	QM3964M6(BAM39640000)	QN3110M6N(BAM31100000)	QM3962M2(BAM39620000)
PQ11				
PR21	NA	NA	NA	NA
PC9	0.022u/16V_4(CH32203KB11)	0.022u/16V_4(CH32203KB11)	0.5%_2(CS00001JE18)	0.5%_2(CS00001JE18)
PC14	0.02u/16V_4(CH3203K1B00)	0.02u/16V_4(CH4223K1B00)	0.1u/16V_4(CH4103K1B18)	0.1u/16V_4(CH4103K1B18)
PC15	68n/16V_4(CH3683K1B09)	68n/16V_4(CH3683K1B09)	82nF/16V_4(CH3823K1B00)	82nF/16V_4(CH3823K1B00)
PC35	330u/2.5V_7343H1.8	330u/2.5V_7343H1.8	330u/2.5V_7343H1.8	NA
PJ2	SL95808HRZ-T(AL095808003)	SL95808HRZ-T(AL095808003)	NA	NA
PC42	4.7u/6.3V_4(CH5471M9B00)	4.7u/6.3V_4(CH5471M9B00)	NA	NA
PR58	2.2_5%_6(CS-2203J913)	2.2_5%_6(CS-2203J913)	NA	NA
PC43	0.02u/25V_6(CH4224K1900)	0.02u/25V_6(CH4224K1900)	NA	NA
PR60	10K_1%_2(CS31001FE14)	10K_1%_2(CS31001FE14)	NA	NA
PC40				
PC41	10u/25V_8(CH6104KEA03)	10u/25V_8(CH6104KEA03)	NA	NA
PL3	0.15uH_10x10x3(CV+15*0MZ12)	0.15uH_10x10x3(CV+15*0MZ12)	NA	NA
PR64	3.65K_1%_6(CS23653F912)	3.65K_1%_6(CS23653F912)	NA	NA
PR66	100K_1%_2(CS41001FE08)	100K_1%_2(CS41001FE08)	NA	NA
PR67	10_1%_2(CS01001FE00)	10_1%_2(CS01001FE00)	NA	NA

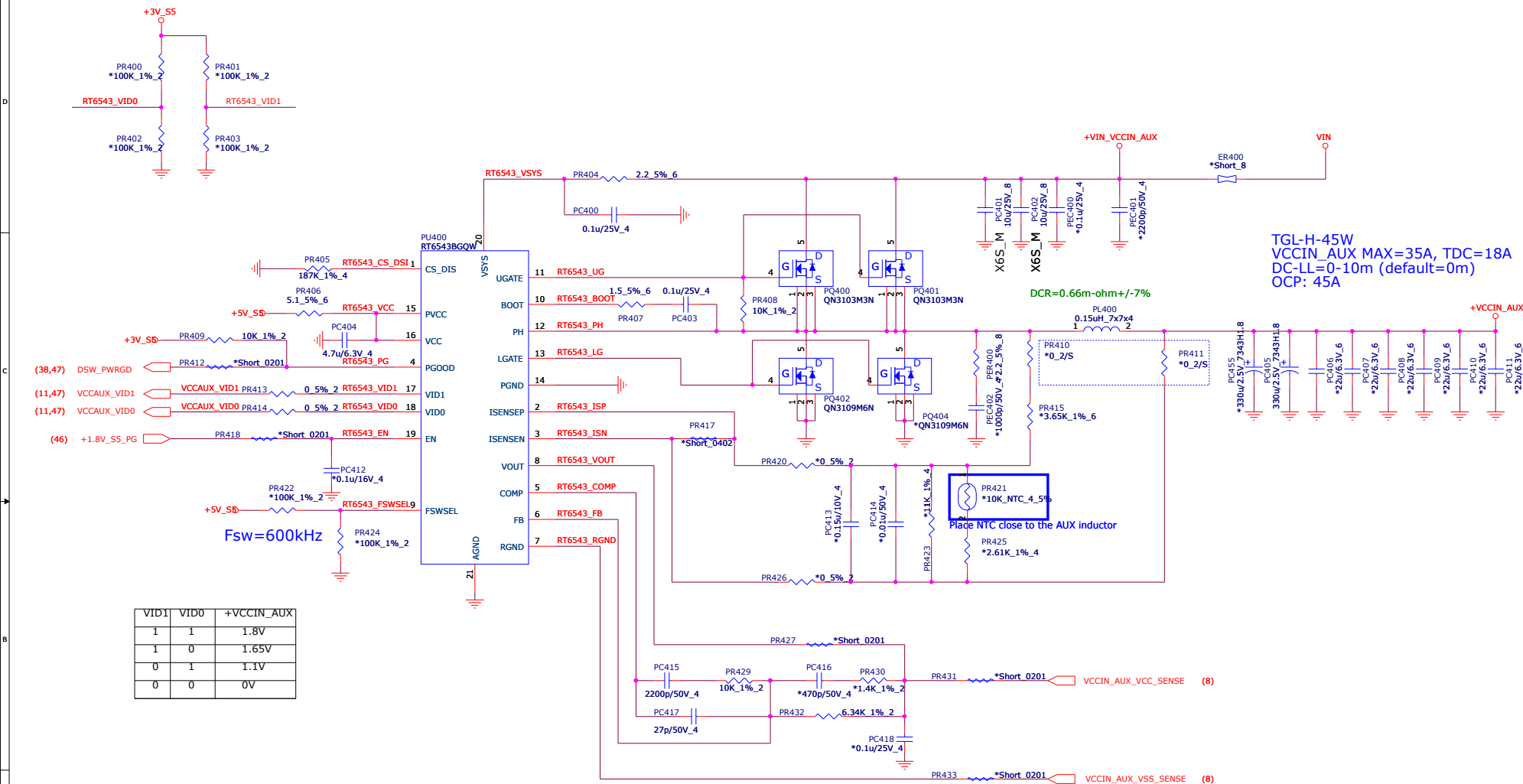
VCCIN

H41@ TGL-H-45W (4+1):
VCORE MAX=36A, TDC=28A
DC-LL=1.5m AC-LL=2.6m
H61@ TGL-H-45W (6+1):
VCORE MAX=74A, TDC=45A
DC-LL=1.5m AC-LL=2.3m

H81@ TGL-H-45W (8+1 BaseLine):
VCORE MAX=87A, TDC=51A
DC-LL=1.5m AC-LL=2.0m

H81P@ TGL-H-45W (8+1 Performance):
VCORE MAX=105A, TDC=61A
DC-LL=1.5m AC-LL=2.0m

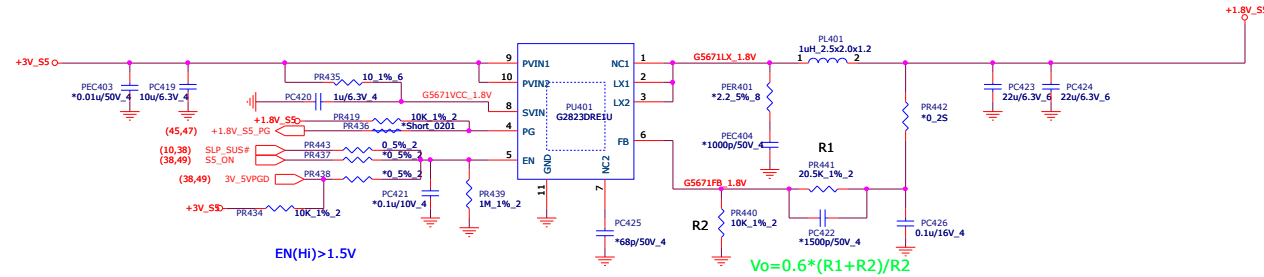


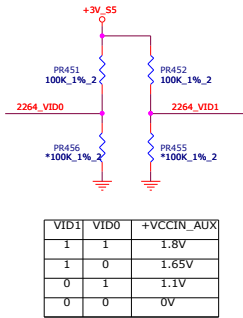


VID1	VID0	+VCCIN_AUX
1	1	1.8V
1	0	1.65V
0	1	1.1V
0	0	0V

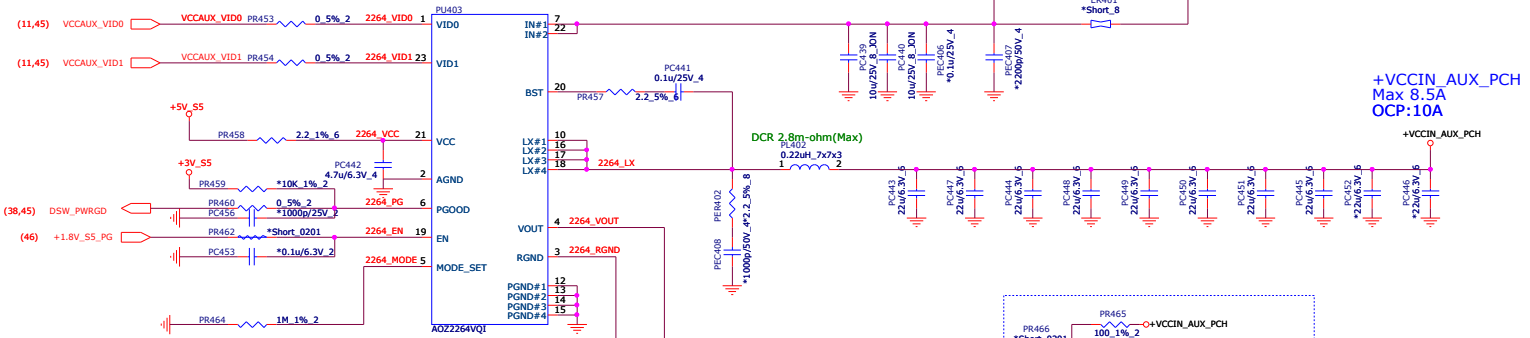
+1.8V_S5

1.8V +/- 5%
OCP: Min 4A
TDC: 2.672A

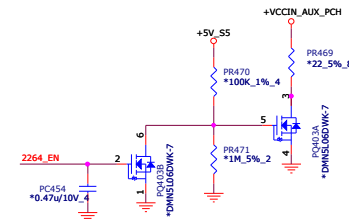




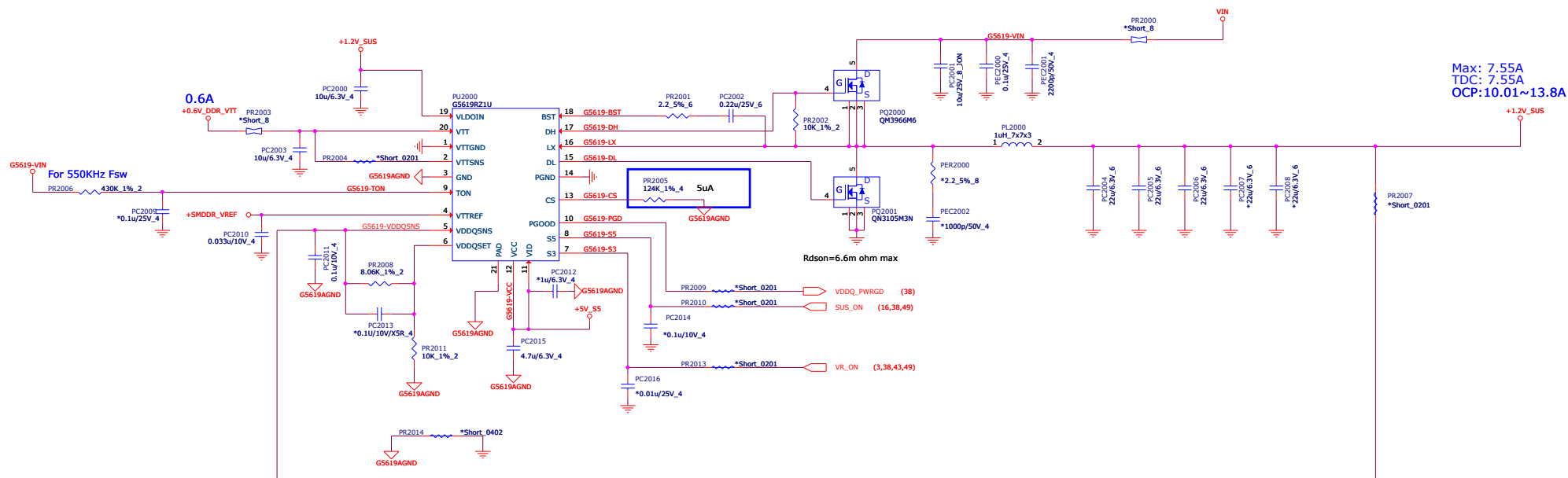
VID1	VID0	+VCCIN_AUX
1	1	1.8V
1	0	1.65V
0	1	1.1V
0	0	0V



MODE_SET	Auto-SKIP	Decay Down	Recomand Resistor
5V	OFF	ON	1M
2.0V	OFF	OFF	400k
1.0V	ON	OFF	200k
0V	ON	ON	0

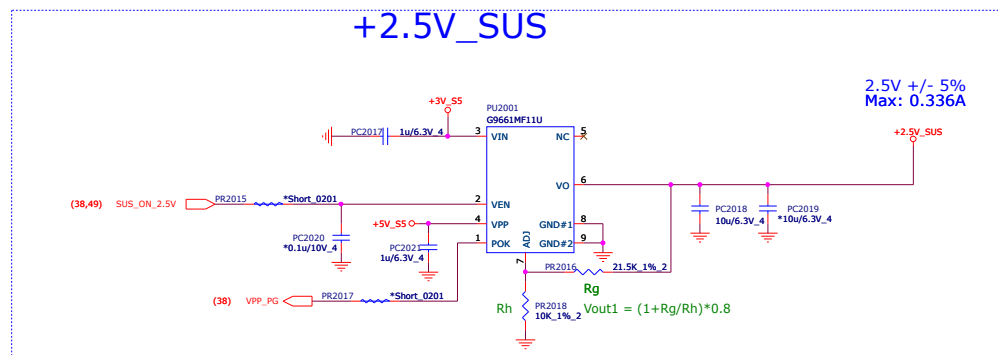


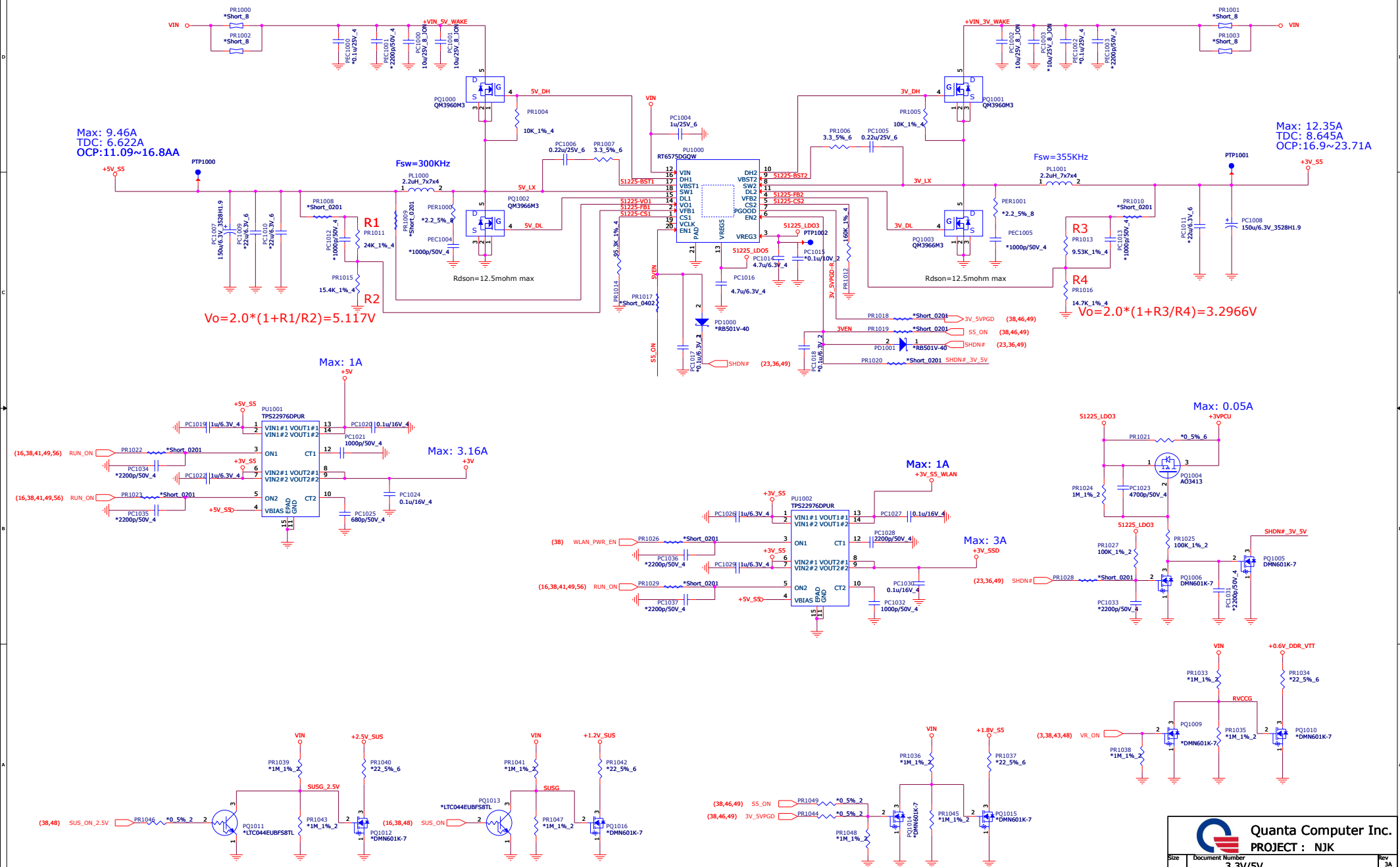
1.2VSUS & VTT_MEM



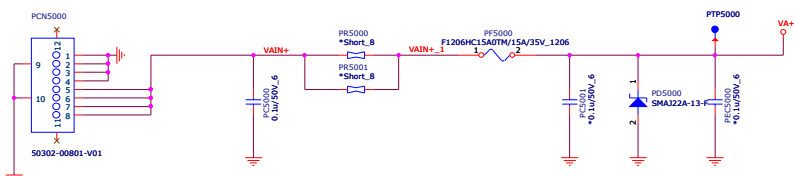
STATE	S3	SS	+1.2V_SUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/SS	0	0	Off	Off	Off

+2.5V_SUS



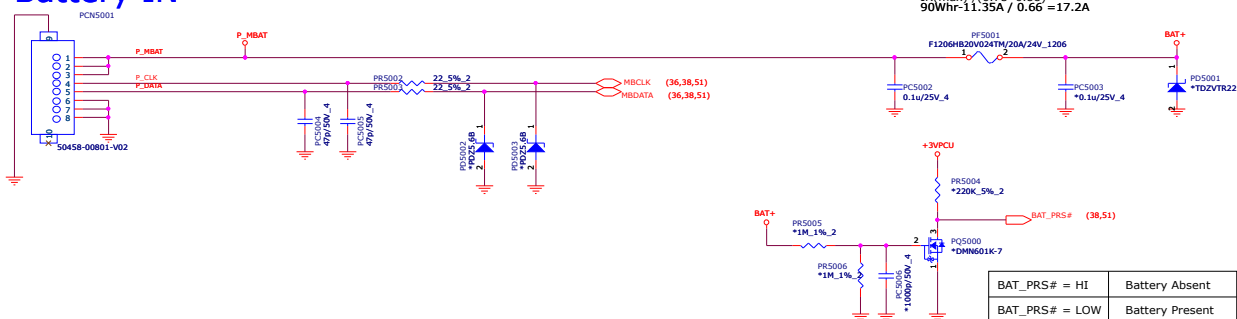


AC IN (On-Board DC-Jack)

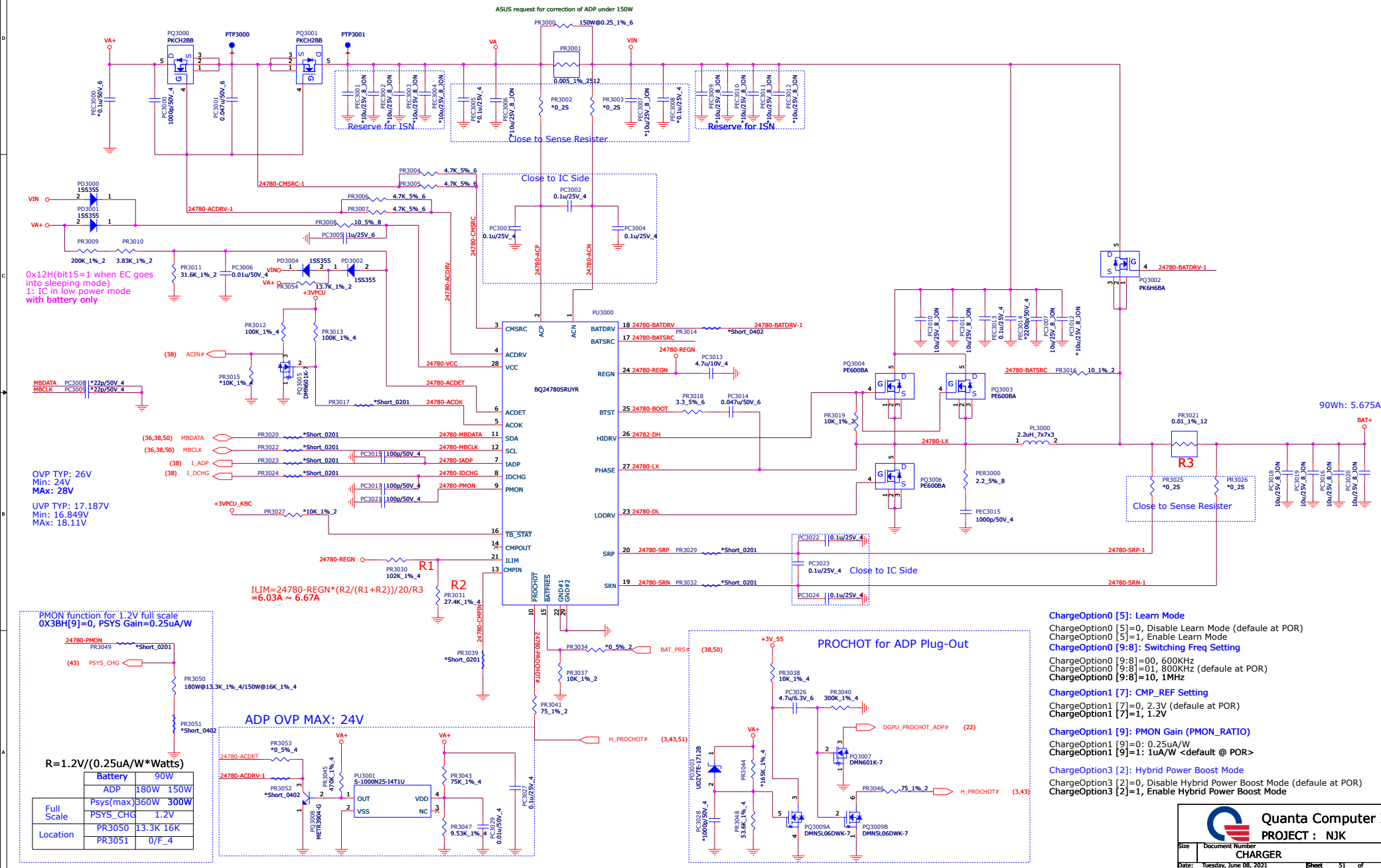
$$\text{Fuse Rating} = \frac{180\text{W}}{19.5\text{V}} \div 0.66 = 13.98\text{A}$$


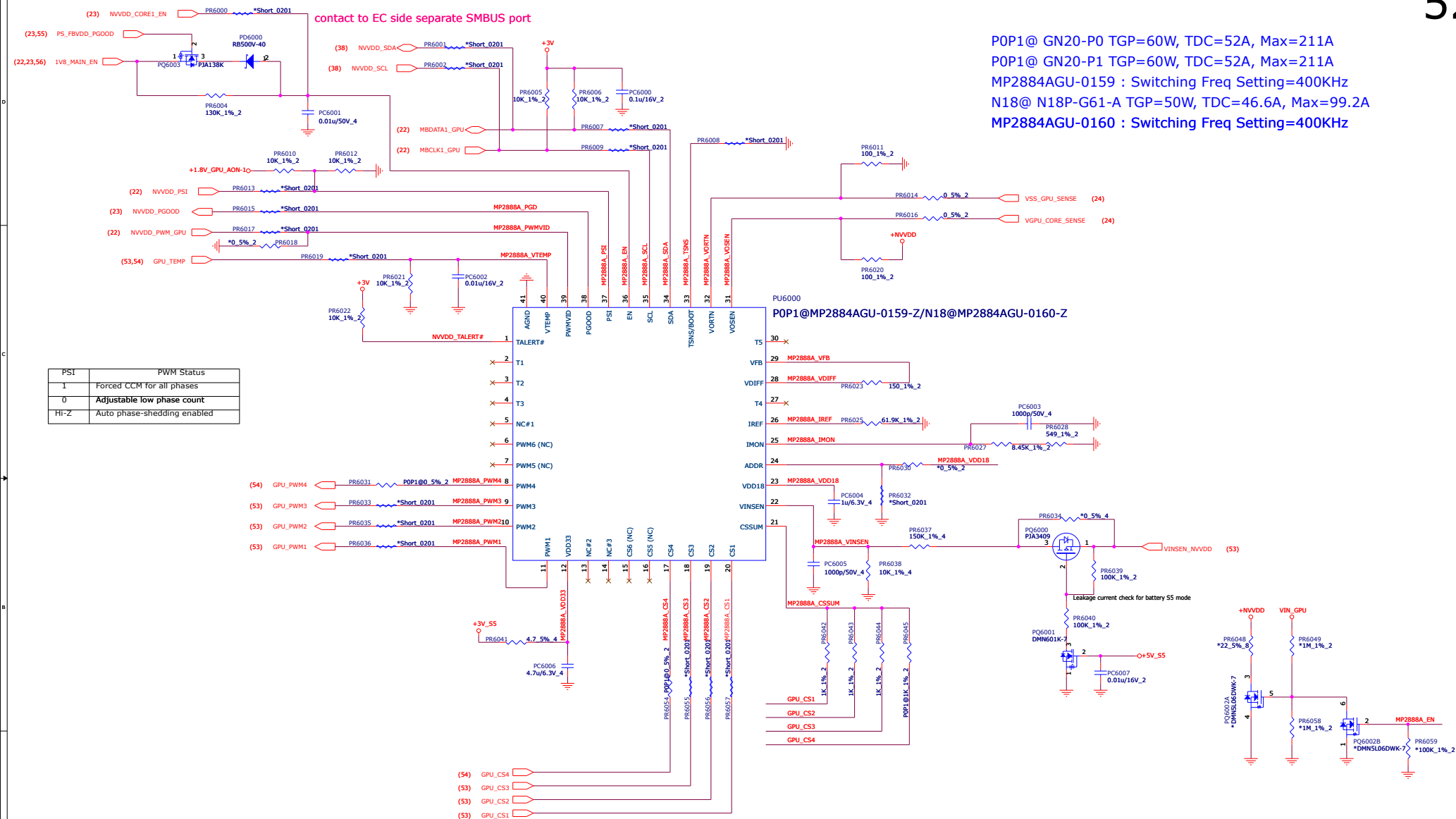
Battery IN

Fuse Rating =
 $IR(max) / (0.75 * 0.88)$
 $90Whr - 11.35A / 0.66 = 17.2A$



BAT_PRS# = HI	Battery Absent
BAT_PRS# = LOW	Battery Present



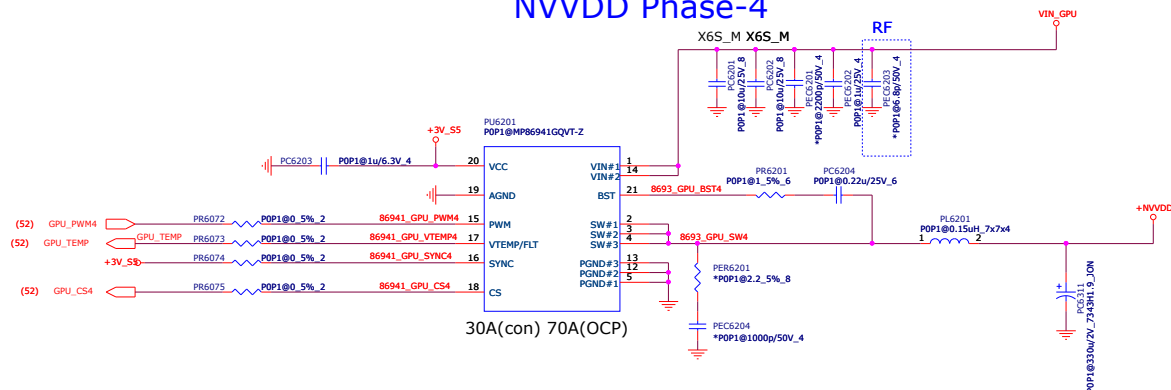


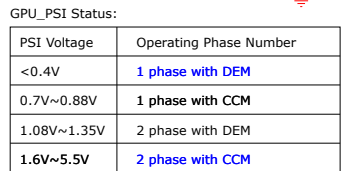
POP1@ GN20-P0 TGP=60W, TDC=52A, Max=211A
 POP1@ GN20-P1 TGP=60W, TDC=52A, Max=211A
 MP2884AGU-0159 : Switching Freq Setting=400KHz
 N18@ N18P-G61-A TGP=50W, TDC=46.6A, Max=99.2A
 MP2884AGU-0160 : Switching Freq Setting=400KHz

The schematic diagram illustrates the power supply section for the X65_M X65_M module. It features the PM6101 MP86941QQT-Z power management IC, which is configured to regulate the input voltage (VIN#1) and provide a regulated output (VIN#2) to the X65_M X65_M module. The IC is connected to various external components, including capacitors (PC6103, PC6101, PC6102, PC6104, PE6101, PE6103, PL6101, PL6102, PL6103, PL6104) and inductors (L1, L2, L3, L4). The output voltage is 0.75V, and the output current is 1.5A. The diagram is labeled with (S2) and (S2,S3) indicating specific test points or components.

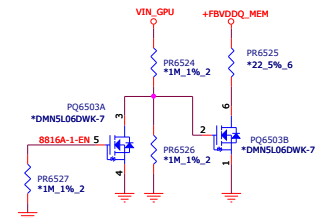
[illegible][illegible]

NVVDD Phase-4



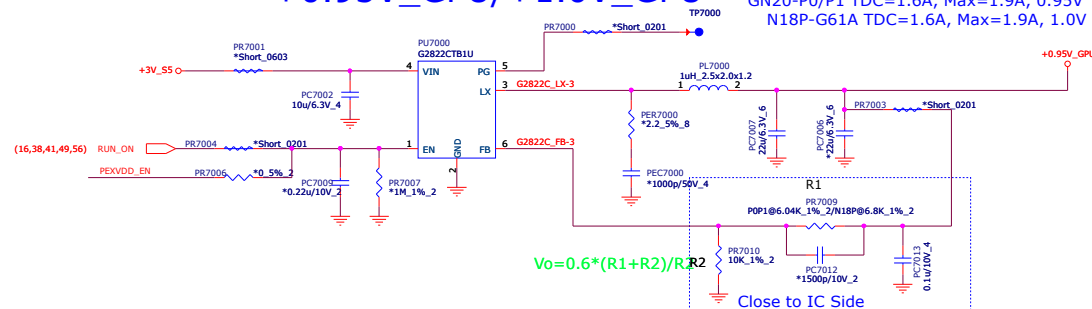


MEM_VDD_CTRL	R2	R3	FBVDDQ
0	18.7K (CS31872FB19)	1.8K (CS21802FB10)	1.20V
1	18.7K (CS31872FB19)	1.8K (CS21802FB10)	1.25V



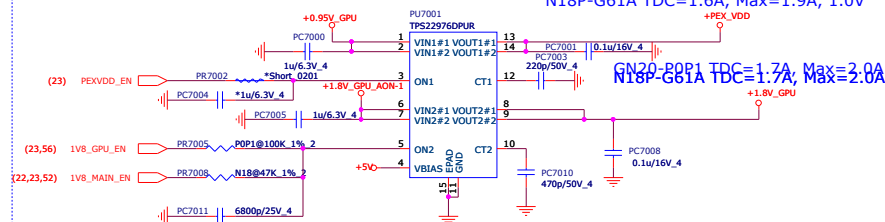
+0.95V_GPU/+1.0V_GPU

GN20-P0/P1 TDC=1.6A, Max=1.9A, 0.95V
N18P-G61A TDC=1.6A, Max=1.9A, 1.0V



Load Switch for GPU

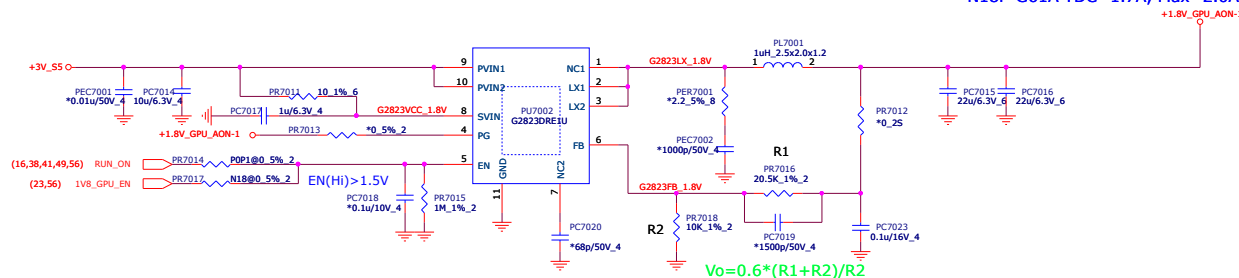
GN20-P0/P1 TDC=1.6A, Max=1.9A, 0.95V
N18P-G61A TDC=1.6A, Max=1.9A, 1.0V



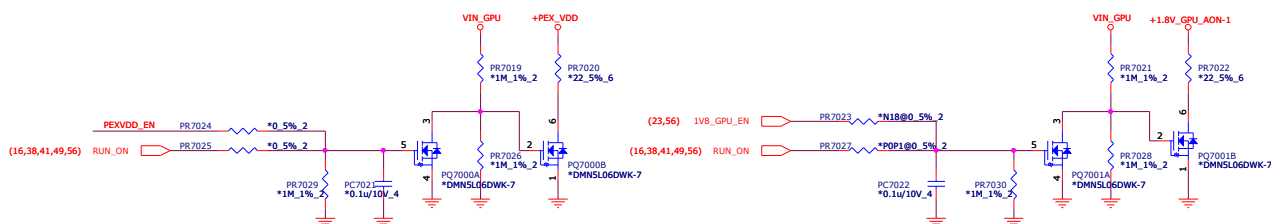
+1.8V_GPU_AON-1

GN20-P0/P1 TDC=1.7A, Max=2.0A
N18P-G61A TDC=1.7A, Max=2.0A

1.8V +/- 5%
OCP: Min 4A



Discharge



1V8_GPU_AON

1V8_MAIN_EN

+1.8V_GPU

NVVDD

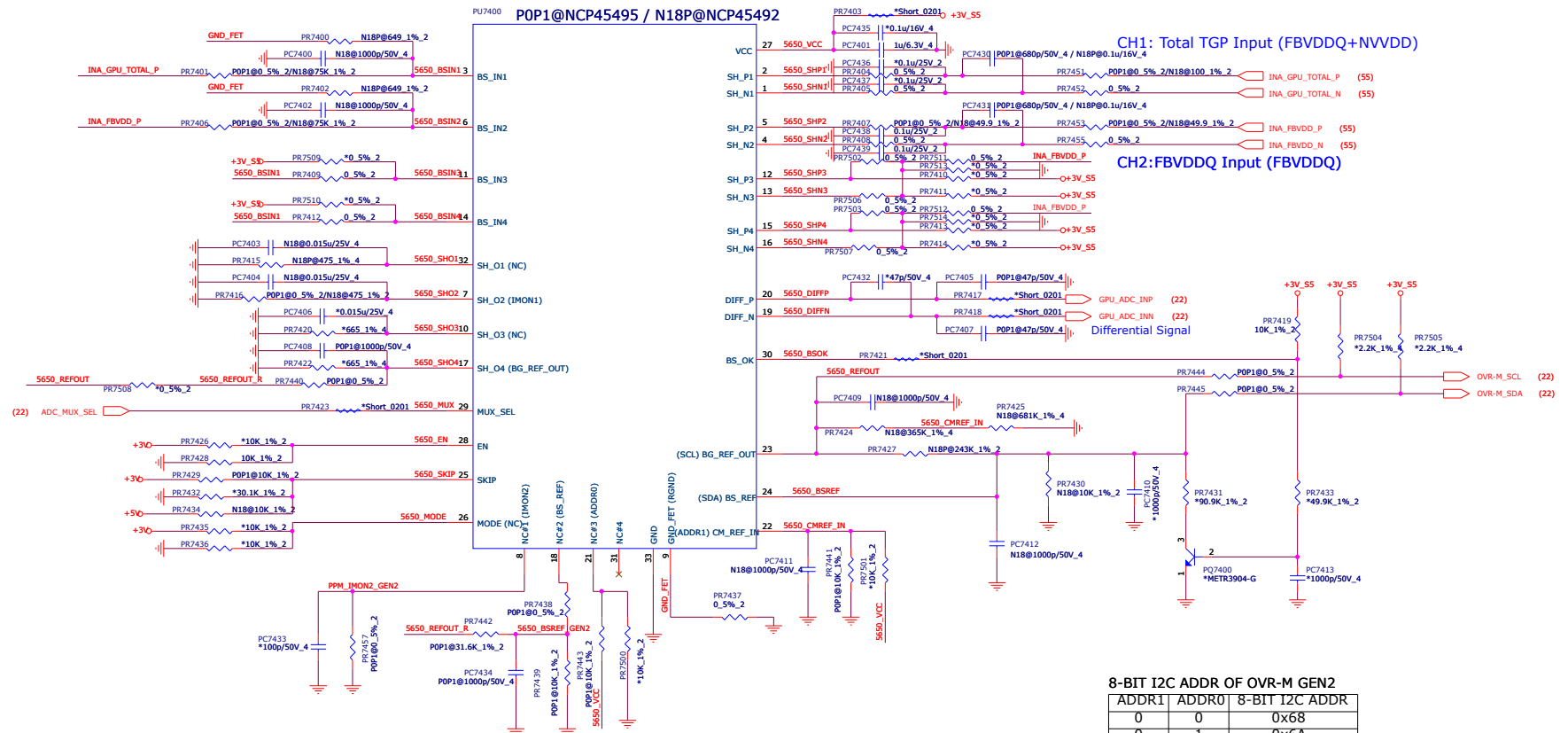
PEX_VDD

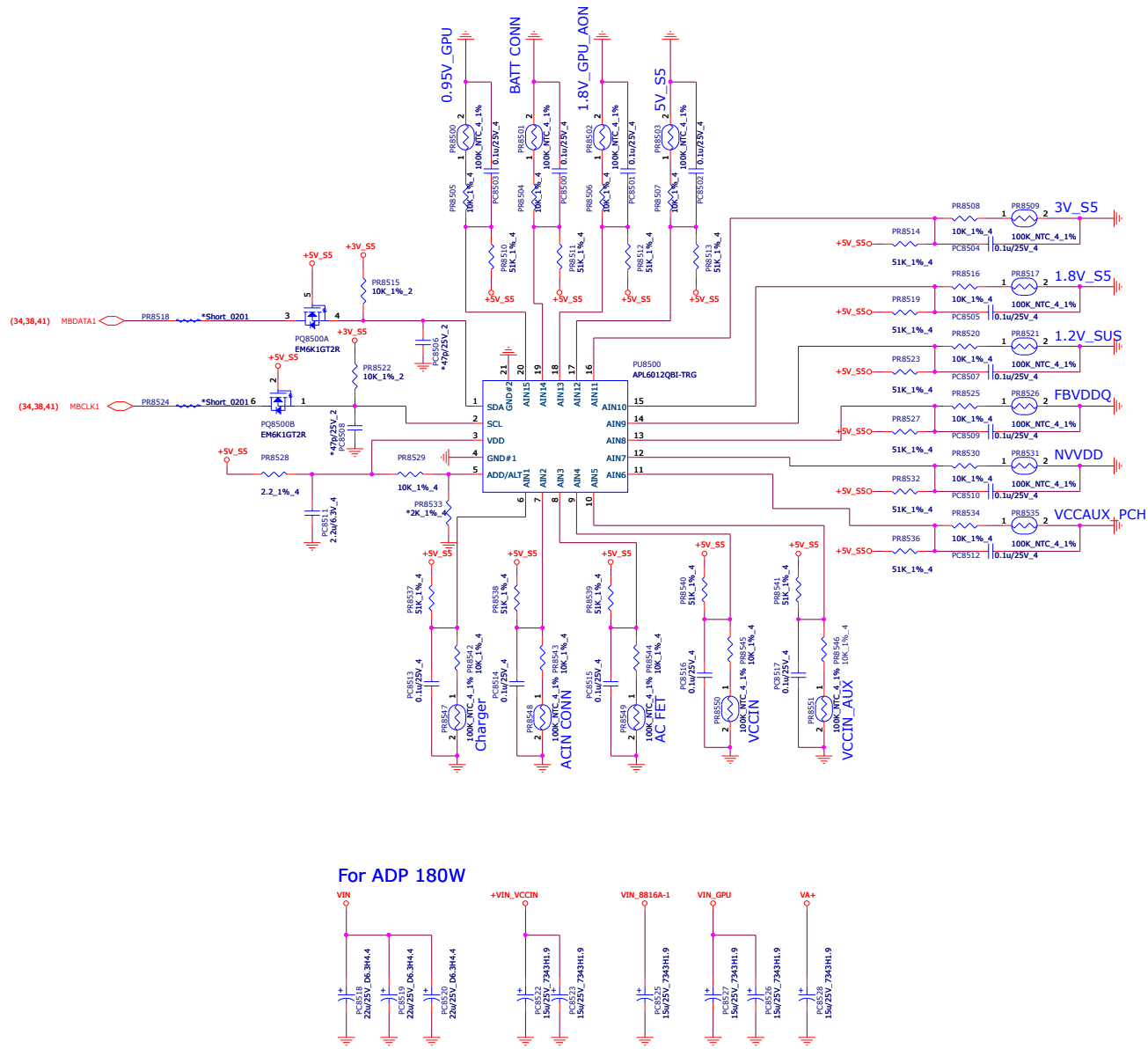
FBVDDQ

< 20ms

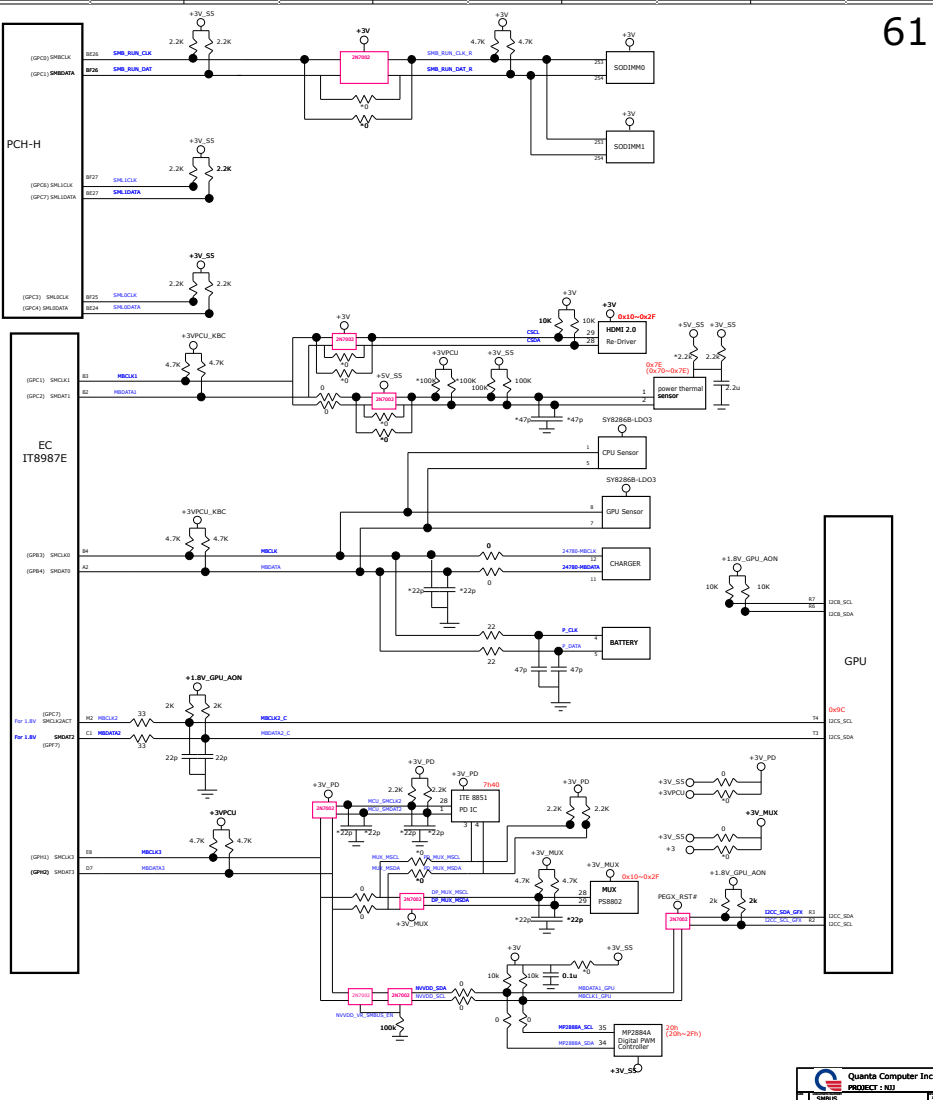
< 4ms

OVR-M GEN1/GEN2









OS status	S0	S0ix	S3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	
H/W status	S0	C10	S3	S4 (Win10 off) RTC wake Enable WOLAN Enable	S4 (Win10 off) RTC wake Disable WOLAN Disable	S5 (Fast Startup "y")	S5 (Fast Startup "x")	
RUN_ON	H	H	L	L	L	L	L	
+3V	H	H	L	L	L	L	L	
+5V	H	H	L	L	L	L	L	
+0.675V_DDR_VTT	H	H	L	L	L	L	L	
+VCCSA	H	H	L	L	L	L	L	
+VCC_GFX	H	H	L	L	L	L	L	
+VCC_CORE	H	H	L	L	L	L	L	
C10_GATE	H	L	L	L	L	L	L	
+1.05V_VCCSTG	H	L	L	L	L	L	L	
+0.95V_VCCIO	H	L	L	L	L	L	L	
+1.2V_SUS_C10(VCCPLL_OC)	H	L	L	L	L	L	L	
SUS_ON	H	H	H	L	L	L	L	
+1.05V_VCCPLL/+1.05V_VCCST	H	H	H	L	L	L	L	
+1.05V_SUS	H	H	H	L	L	L	L	
+1.2V_SUS	H	H	H	L	L	L	L	
SUS_ON_2.5V	H	H	H	L	L	L	L	
S5_ON_2	H	H		H	L	L	L	
+1.05V_S5	H	H		H	L	L	L	
S5_ON	H	H		H	L	H	L	
+3V_S5	H	H		H	L	L	L	
+1.8V_S5(From PCH)	H	H		H	L	H	L	
+5V_S5	H	H		H	L	H	L	